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DIGITAL DESIGN

SYSTEMS ARCHITECTURE, INTEGRATION AND APPLICATIONS

MARCH 1984

LAN STANDARDS EMERGE

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- DEC COMPATIBILITY
- PERIPHERAL CONTROLLERS

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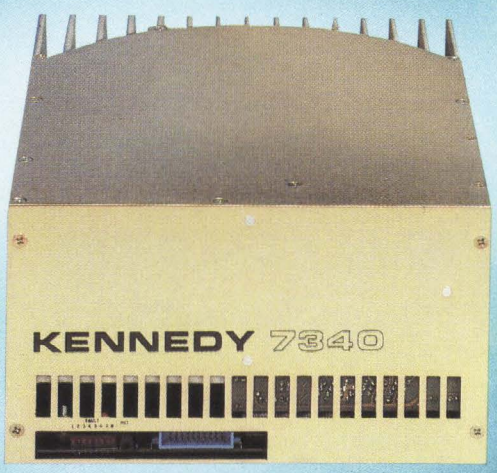

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CPU used_____
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Z8581

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MARCH 1984
VOL. 14, NO. 3

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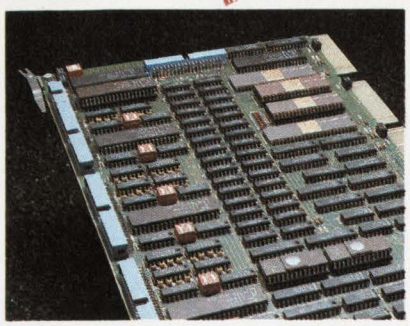
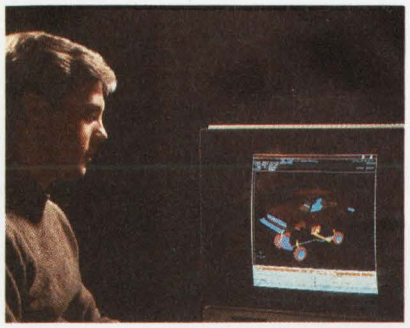


p. 41 *(Photo courtesy Simpact)*



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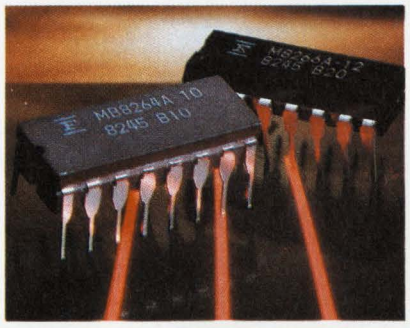

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Cover

Integrated Network Architecture is Digital Communications Associates' (DCA) networking philosophy which incorporates complete network transparency, virtual circuit switching, error-controlled data transmission, comprehensive network management, and compatible modular hardware. From its inception, DCA realized the importance of designing compatible modular communications products that could be easily upgraded or repaired so that downtime is minimized. Digital Communications Associates, Inc., 303 Technology Park, Norcross, GA 30092, (404) 448-1400, photography by Arrington Hendley, Atlanta, GA (see p. 70).

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PERIPHERALS

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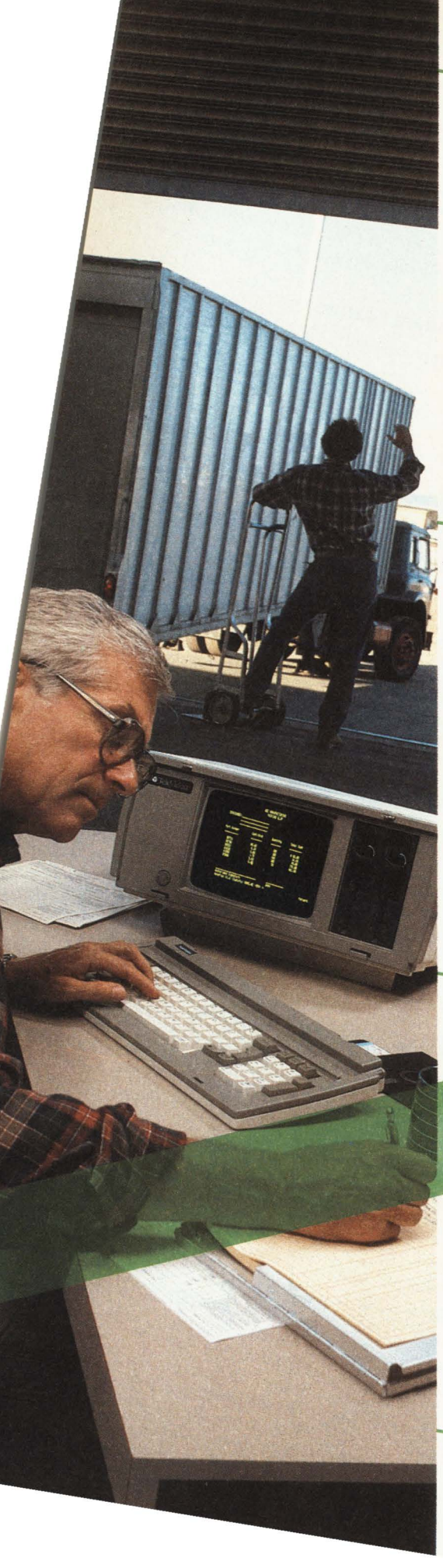

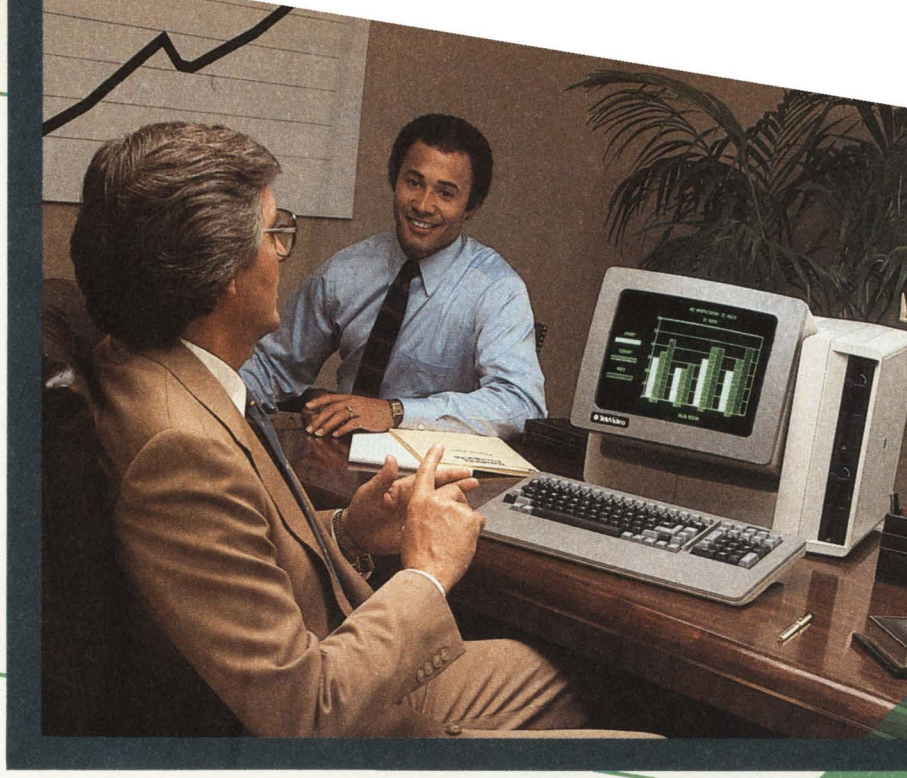

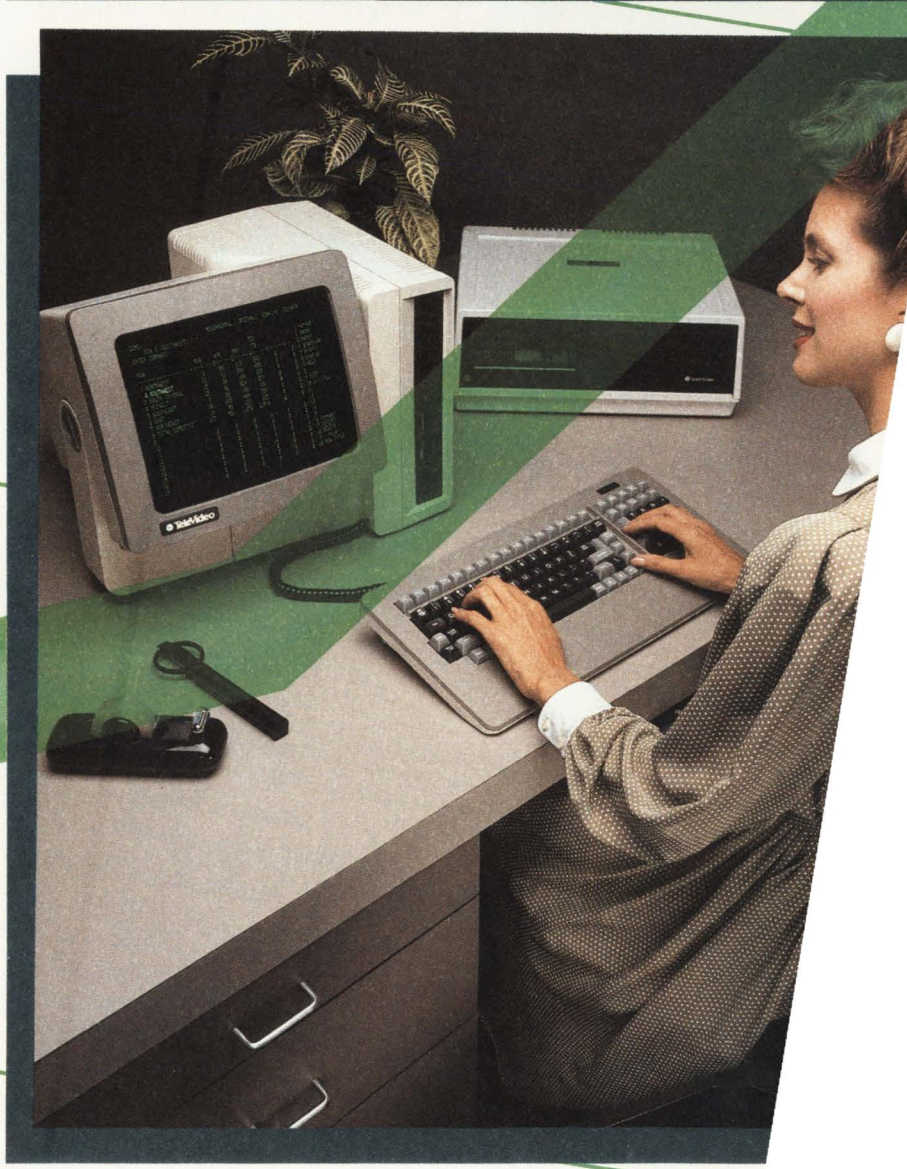

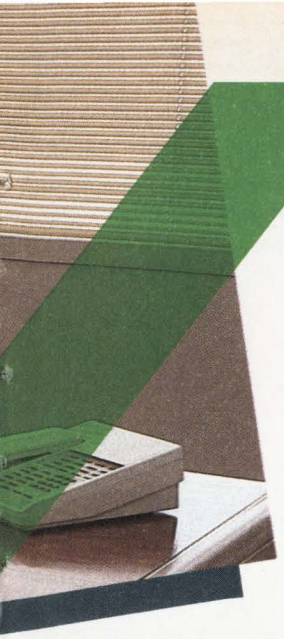

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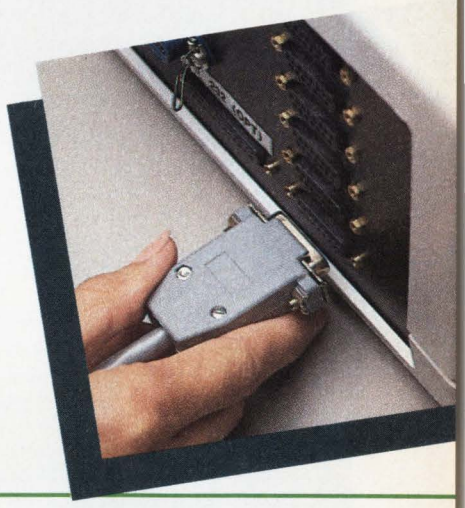

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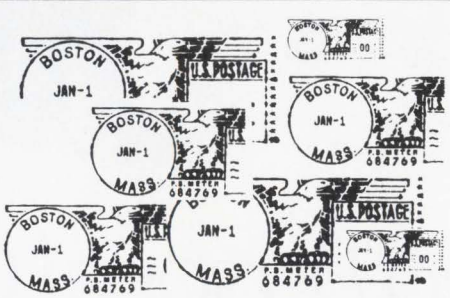

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Our 5480 Series of color raster terminals and workstations aren't the only ones with 4096 colors. But the colors have never looked so good. Because resolution has never been higher.

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Currently, our terminals can be driven by many of the leading software products. And the list is growing rapidly. Because Lundy is committed to an aggressive third-party software development program to provide the most comprehensive application packages.

Lundy will help you see more in graphics.

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A company you can count on to help you see more in graphics—and get more out of graphics—both now and in the long term.

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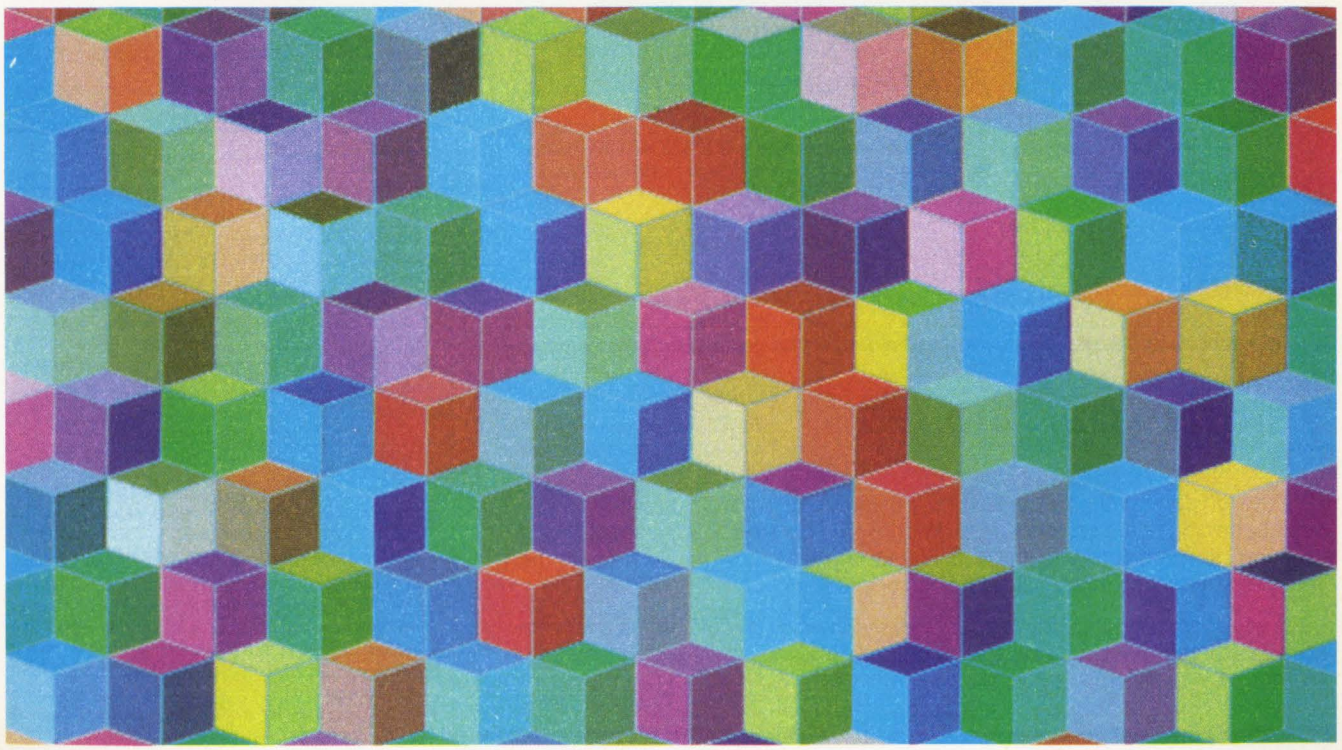

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Digital Design is your forum — your inputs help keep the magazine interesting and vital to the design community. So let us know how we're doing and how we can serve you better in the future. We want to know what you like or dislike about *Digital Design*, the subjects you'd like to see us address, how you feel about the problems you face every day as design professionals.

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Our 3000 family of printers has an impressive list of features. But the most prominent new change on our printers is our new name.

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And Genicom will also offer other products including our 2000 teleprinters and the soon to be introduced 4000 shuttle matrix printers. You'll find we have the same complete product line we had with GE.

Genicom. We have proven products, experienced personnel, established manufacturing facilities and service network, plus a new commitment to excellence that stands behind our new name.

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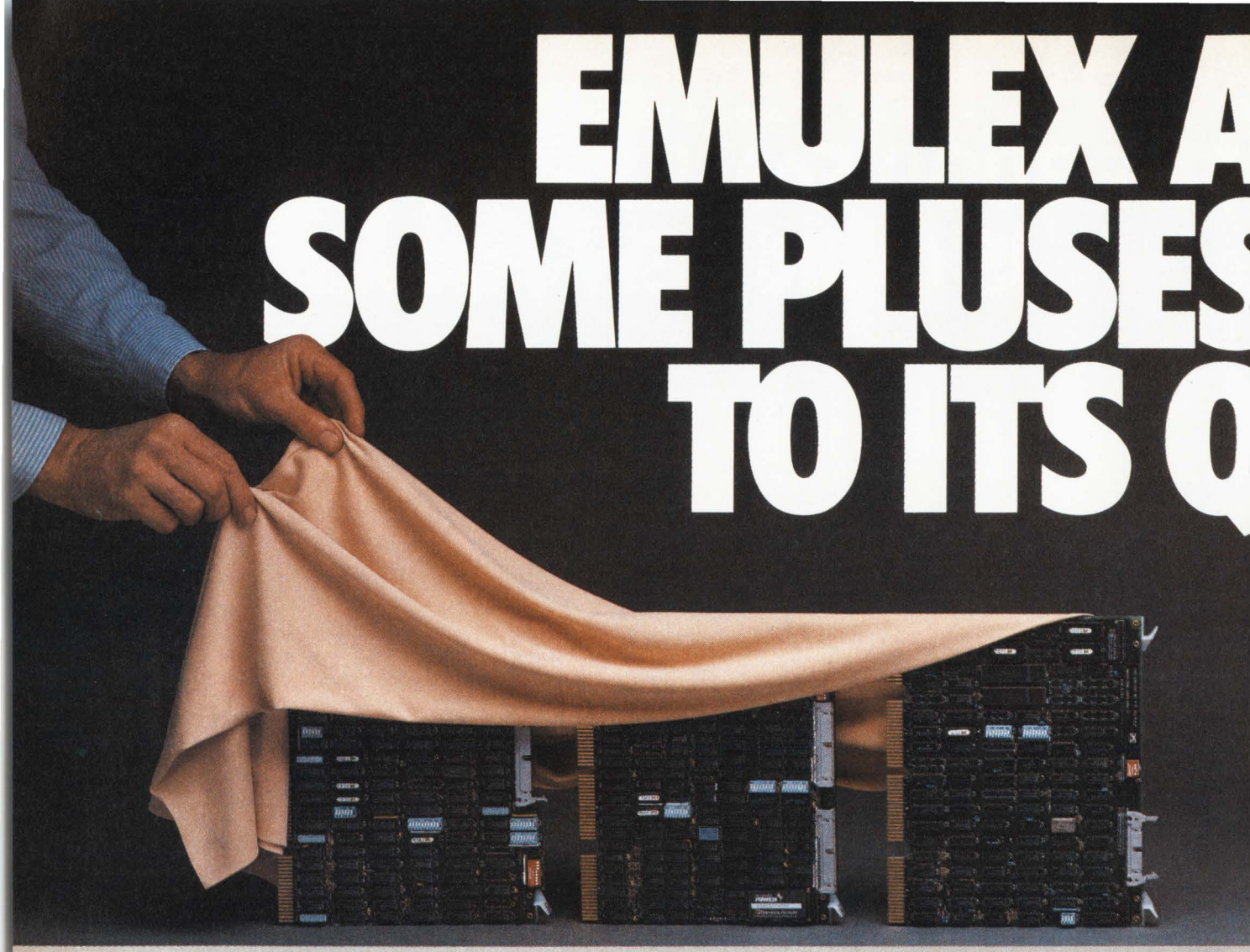

New UC02 emulating host adapter using Mass Storage Control Protocol (MSCP).

New CS02 multiplexer for LSI-11 through 11/23 PLUS and MICRO/PDP-11 computers.

New TC05 tape coupler for CDC Sentinel ¼" streaming tape drives emulates DEC TS11.

Once again, Emulex gives you more, while charging you less. We're introducing three new controllers for QBus users, and reducing prices on four of our most popular products.

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Also available is our TC05 tape coupler featuring DEC TS11 software transparency and standard operating system support on your QBus. It allows you to interface CDC Sentinel ¼" streaming tape drives without using special streaming software.

Last, but not least, is the UC02 emulating host adapter, with unique features like automatic drive sizing, command stacking, seek ordering and error control.

By using the Mass Storage Control Protocol (MSCP), the UC02 allows the operating system to utilize the precise characteristics of the Winchester disk drive without patches or modifications to the operating system. The UC02 plugs into any single quad width QBus slot and provides you the versatility of using the Small Computer System Interface (SCSI) bus.

NOW, THE PRICE REDUCTIONS.

First, we've slashed 33% off the price of our TC02 TS11-compatible tape coupler.

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TC02 TS11-compatible tape coupler.

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Also available for QBus users are two storage subsystems.

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EDITOR'S COMMENT

In the course of visiting manufacturers across the country during the winter months, I have gained a perspective on the computer and electronics industries that many of you may already have. The great sense of activity apparent in new companies and increased sales is viewed against a background of several highly visible failures and increasing insecurity about the long term health of the American economy. The economic success of our industry is also a stark reflection of the continuing decline of what the popular press calls the smokestack industries. Even the "clean" industry of high technology is recognized as having problems of seasonal changes in employment, industrial pollution, displacement of workers through offshore migration of manufacture and so on. It may not be unreasonable to draw parallels with the turn-of-the-century's reaction to the industrial revolution, at the period when new technologies were being consolidated into the hands of businessmen.

The computer industry, however, eludes easily drawn analogies for it is far from a mature technology. On the contrary, this industry is so complex that it has spawned a secondary industry whose sole concern is forecasting the growth and viability of technology. The changes occurring today are almost Byzantine in nature, and change is so rapid that products often do not lend themselves to easy explanation. One of the hardest questions we of the trade press face is how we should sort through all of the available information to best serve the reader.

Among my observations in this regard is that the "technologist" of today is not the "simple engineer" of yesterday. Today's designers and engineers have a heightened sense of the worth of their labor and demand a greater share in its rewards. The time, however, of the company operating from a garage seems to have ended, and more creative engineers sacrifice control of their ideas to acquire the financial means to pursue them. In other cases, engineers respond to the financial rewards of marketing technology by abandoning their work. This migration leads from designer to applications engineer, to technical sales support, and finally to marketing. As technology becomes more complex and buyers demand quality support from manufacturers, this may be inevitable, but one cannot help wondering what portion of the 20,000 engineers and programmers we lack each year are created by the shift into technical support and marketing.

One prominent individual participating in this progression has noted the difficulty in retaining any standard of values, trying to "keep ones head" during this rapid cycle of change. For instance, job titles often seem incongruous with the age or experience of the employee. Companies find, often in hindsight, that one individual may have been an invaluable contributor to the design or programming team. On the other hand, a young professional is often unwilling to leave a company for a more challenging position because of the responsibility he has or because of the financial equity that relative seniority may have brought. These pressures make people one of the most crucial considerations of our industry.

Another observation relates to the environment in which people and technology are maturing. One survey in 1983 identified 50 centers of high technology growth where infrastructure, industry, education, government, and location support development, particularly of the computer and electronics industries. While my observation of high tech centers lacks empirical basis, my emotional response to visits is a feeling of building momentum – if only because of the amount of new construction. This is especially true on the West Coast. One individual pointed out to me that the "silicon valley is becoming an administrative and research center" as technical manufacturing continues to shift to the Pacific Basin. I'm inclined to think of the San Francisco-Santa Clara corridor as setting the role for all of the other high technology areas. This is overly simplistic, since education and research centers across the country continue to influence and drive computer technology, but technology sharing tends to occur between the valley and other centers. There is a common set of sometimes unrealistic expectations and demands on the individuals involved in these centers. In this, the valley also tends to set the pace, perhaps due to its geographical concentration.

It is the echo of the interaction between the people and the environment that creates difficulty for its participants. Overnight millionaires created by public offerings, rapid turnover of employees, and salaries proportionate to pressure or potential, add to the perception of what is reasonable. These perceptions become more acceptable in light of the individuals need to look at long term financial security or purchasing a home.

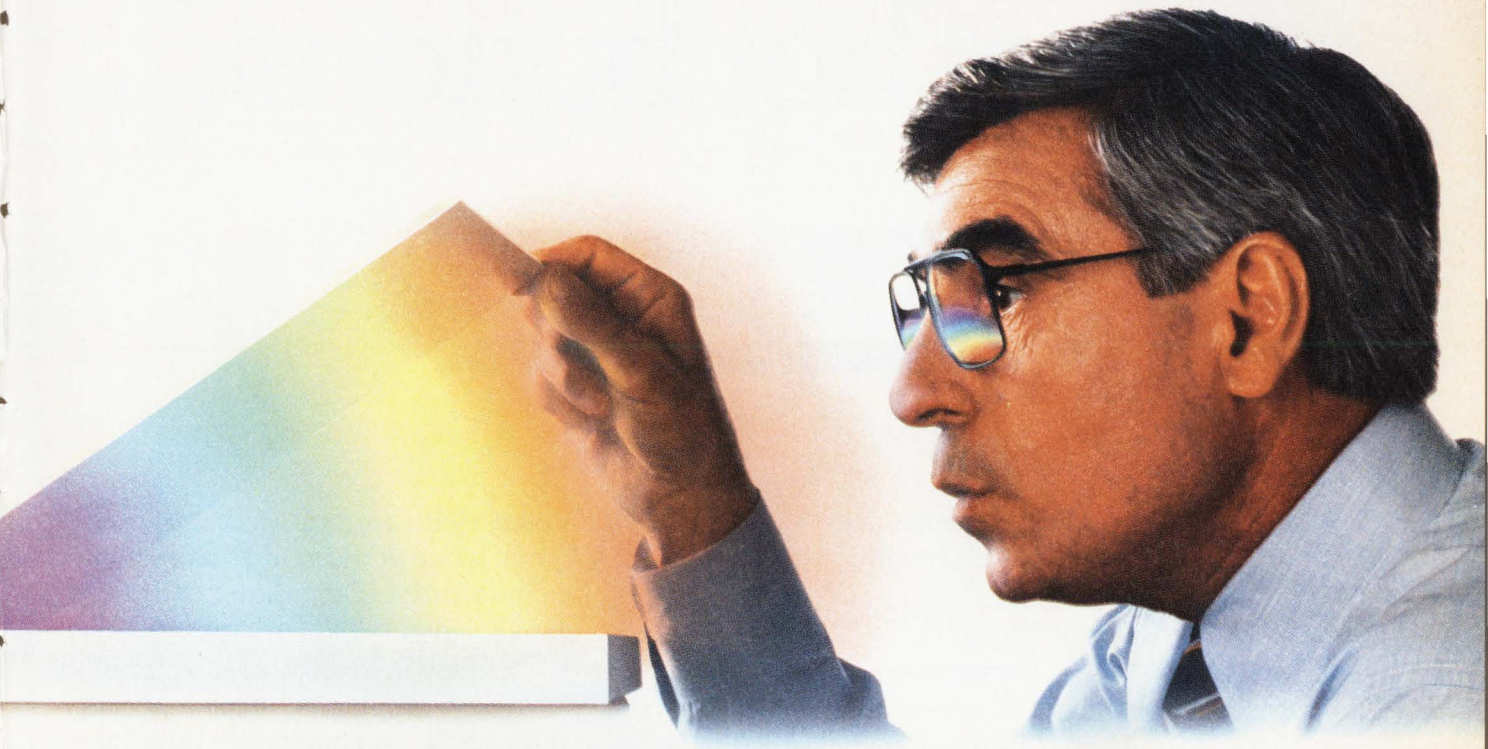
Given the points raised above, perhaps we should be more understanding of the sometimes confusing view that Wall Street takes of the computer industry. Some of the actions of venture capitalists, brokers, and advertising groups cause all of us to pause in abject wonder at times. Several examples here are illustrative; the image of venture capitalists participating in companies with competing technology, wild fluctuations of stock disproportionate with the actual value of a company, and the gratuitous involvement of merger brokers. We are perplexed by the precipitation of second or third hand interpretations of what a technology means, or of what impact it will have. The investor looks on in similar wonderment, attempting to synthesize the effects of technology. From this perspective, investing in several approaches to the same goal may be wise. Depreciation or inflation of a company's value may similarly reflect real concern for profit-making by brokers for their clients. Mergers may bring capital or management skill to companies otherwise unable to promote valuable designs.

In the last analysis, the value of our contribution to technology today may depend upon our ability to look at both near term profitability and longer term impacts of design and engineering. Our ability to refrain from celebration of high technology's success and concentrate upon its implications has become a necessity for the long term health of the industry. If we tie progress of the computer industry to the generations of microprocessors for the purpose of looking forward, some of the noise is reduced.

This period of transition, is critical to the long term development of computers and electronics, but it lacks the glamour of periods of dramatic change. It is a time when the editor, designer, manufacturer, banker, and supplier must inquire whether or not we are concentrating on the unrealistic environmental aspect of our industry or looking critically upon our activities and their effects.

Jerry Borrell
Editor-in-Chief

The Newest Innovation in Controller Technology From the Oldest Name in Multifunction Controllers.



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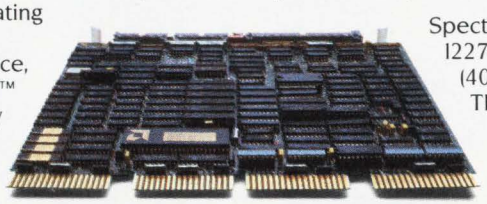

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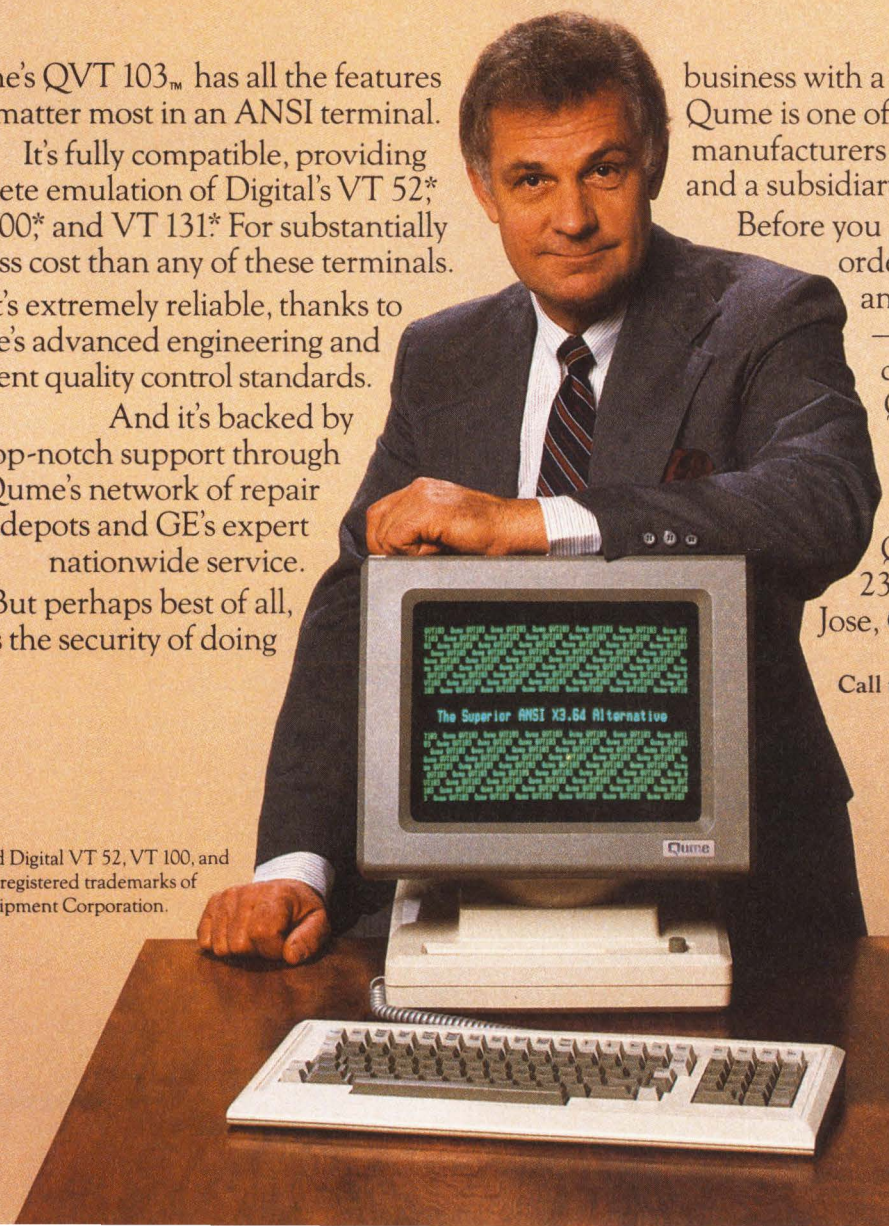

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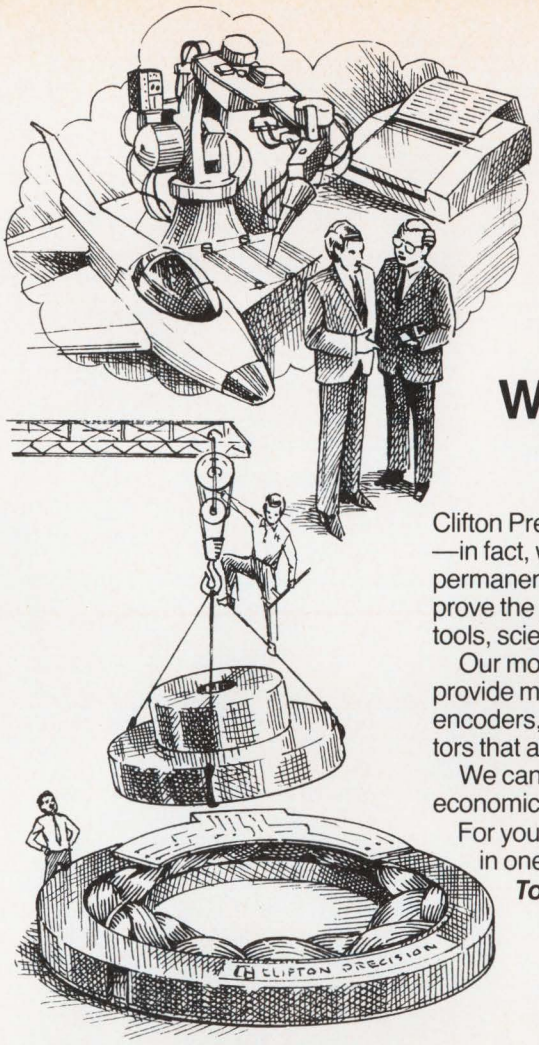

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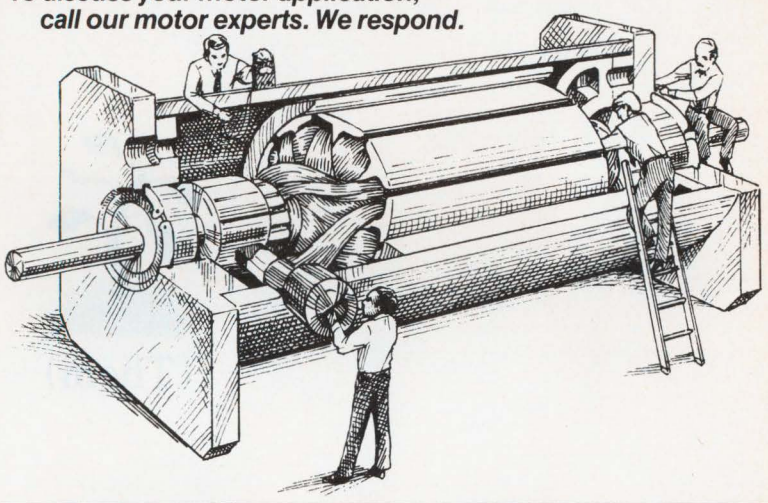

For stepper and commercial brushless dc motors, call Jim Chandler at Murphy, NC (704) 837-5115

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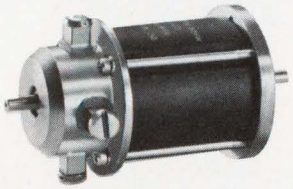

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Frame sizes from ¾″ to 4″. From ceramic-magnet, alnico-magnet, to rare-earth magnet designs, Clifton PM motors drive equipment ranging from computer peripherals, machine tools and robotics, to high performance missiles.

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NEWS UPDATE

SX-2000

Mitel Corp. has received approval to sell the SX-2000 Integrated Communications™ System in three major markets—U.S., U.K. and Canada. Mitel met all requirements of the U.S. and Canadian telecommunications authorities as well as those of the British Telecom. Shipments will begin early in 1984.

Graphics-Standards Program

Graphic Software Systems Inc. announced that 15 manufacturers of microcomputer-peripheral equipment have agreed to participate in their program to develop and use Virtual Device Interface (VDI) graphics standards. The VDI standard permits application software to treat all graphics devices identically, avoids having to modify application software in order to use different types of computer peripherals and is embodied in GSS-Drivers software—software programs that permit interaction between application programs and a computer peripheral such as a printer, plotter or terminal.

CAD/CAM Contract

Control Data Corp. has signed a multiyear OEM contract with Ramtek Corp. to supply the components for its new expandable family of integrated CAD/CAM workstations. The ergonomic workstation, planned for delivery in mid-1984, is based on Ramtek's series of high-performance display generators. It includes a high resolution (1280 × 1024), 60 Hz, non-interlaced color graphics display; separate alphanumeric display; fast vector transforms; and 3-D display file.

Unix 4.2 BSD

Integrated Solutions Inc., a manufacturer of QBus-compatible 68000 and 68010 CPU board sets and systems, will offer Unix 4.2 BSD, a Unix version from the University of CA at Berkeley. IS will provide an upgrade kit for customers wishing to move to 4.2 from System III and will offer 4.2 on their "Optimum series" of 68010 based systems.

Polaroid Technology For Floppies

Polaroid Corp., Perfect Data Corp. and PermaByte Magnetics reached a cooperative agreement to produce and market a full line of floppy disk media. The agreement calls for the dedication of each of the participants' primary areas of expertise to the project. Polaroid will apply its film coating technology to the magnetic coating of web stock used in the manufacture of floppy disks. Media supplied by Polaroid will be converted into finished disks by PermaByte Magnetics, using advanced finishing and packaging facilities. Perfect Data Corp. will market and distribute the product in the U.S. and selected international markets.

Gate Array Second Sourcing

Texas Instruments and Fujitsu Limited, in a step toward industry standardization, have entered into an alternate sourcing agreement covering the design, manufacture and marketing of Fujitsu bipolar and CMOS gate arrays. Under this agreement, Fujitsu grants TI a non-exclusive, worldwide license to manufacture and market bipolar arrays ranging from 240 to 1100 gates and CMOS arrays from 440 to 8000 gates. In return, TI will provide Fujitsu with its Transportable Design Utility (TDU) which is a computer-aided design system that supports rapid gate array design.

Computer Experts

The American Society of Mechanical Engineers predicts that expert systems may some day work alongside design engineers in the design of new machines and devices. An expert system is a computer program that has captured the experience, knowledge, and judgment of human experts in a field; has organized that expertise for use by other practitioners; and will retain thousands of previous technical decisions not normally remembered by human designers.

Flat Panel Venture

Burroughs Corp. and Telex Computer Products, Inc. intend to form Plasma Graphics Corp., a jointly owned company to manufacture and market a line of advanced flat panel information displays for use with computers and electronic instruments. The Plasma Graphics flat panel display is an easy to read, slim profile, and light weight device capable of depicting graphical information with applications in office workstations, personal computers and transportable computers.

Interface Standard Approved

A proposed standard for intelligent device interface for data cassette drives was unanimously approved by members of the Working Group for Data Cassette Compatibility (D/CAS). The proposed standard, D/CAS-5, is patterned after the QIC-02 interface adopted for use on quarter-inch cartridge streaming tape drives, and will enable connection of D/CAS compatible drives to QIC-02 controllers.

"DADS" Development

Aeronautical Systems Division's Deputy for Aeronautical Equipment has awarded two contracts totaling $16 million for development, testing and evaluation of a Digital Audio Distribution System called "DADS." Contracts for this tri-service (Air Force, Army, Navy) program, managed by the Air Force, went to Telephonics Corp. of Huntington, N.Y., for $8.6 million; and to Magnavox Government and Industrial Electronics Co. of Fort Wayne, Ind., for $7.4 million. The contracts are for a two-phase developmental program.

DMA Contract

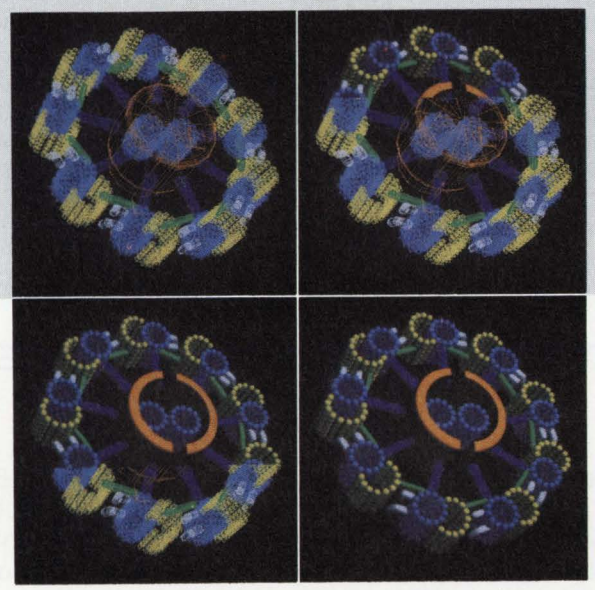
DMA Systems Corp. signed a one-year contract to provide Compugraphic Corp. with Micro-Magnum™ removable 5.25-inch Winchester disk drives. Compugraphic will incorporate the Micro-Magnum drives into the new Modular Composition Systems (MCS) electronic typesetters.

Contracts For SKY

SKY Computer, Inc. (Lowell, MA) has recently signed OEM contracts incorporating the SKY Fast Floating Point Processor (FFP) into various systems products. Callan Data Systems (Westlake Village, CA) will integrate the SKY-FFP-M and Micro Number Kruncher into its Unistar UNIX System-V environment. Integrated Solutions, Inc. (Campbell, CA) is using the SKYFFP-Q for its Q-bus based MC68000 system running UNIX System III. A $2M contract with Sun Microsystems, Inc. (Mountain View, CA) supplies the SKYFFP-M for integration into Sun's 68010-based, Multibus microcomputers running UNIX.

Image manipulations in seconds, not hours.

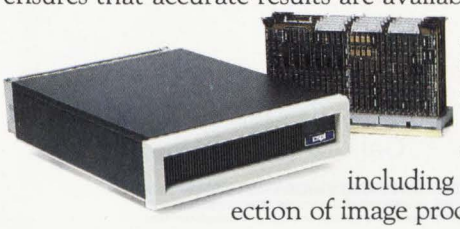
With Mini-MAP™...The Array Processor For The Graphics OEM



Courtesy of Al Barr, Raster Technologies, Inc.

For tough image processing problems like pixel rotation, image reconstruction, or hidden line removal from wire frame models, Mini-MAP gets results in seconds, not hours. Attach a Mini-MAP to a PDP-11 or VAX UNIBUS and you have an interactive number cruncher that is ideal for image processing, CAD/CAM, solid modeling, medical imaging, and animation.

Shared memory simplifies programming and provides the unprecedented throughput necessary for truly interactive image processing of complex algorithms. 32-bit DEC floating point arithmetic, along with 7 MFLOPS of number crunching power, ensures that accurate results are available quickly.



A scientific subroutine library of over 225 FORTRAN callable routines including an expanding selection of image processing algorithms is available for Mini-MAP. For optimum performance, high-level FORTRAN control languages are provided for both the host and Mini-MAP.

Memory is expandable up to 16 MBytes. Configurations include a four-board set with DEC-type backplane or fully packaged systems.

System integrators are finding Mini-MAP is the most cost-effective number crunching solution for image manipulation. Write for information or **call toll free 1 800 325-3110 for fast action.**

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NEWS UPDATE

Semiconductor Shipments Reach $11 Billion

SAN JOSE, CA—January 1984—Worldwide semiconductor shipments by U.S.- and European-based manufacturers grew 17.3% to a record $11.0 billion in 1983, according to a statistical survey sponsored by the Semiconductor Industry Association (SIA). Based on fourth quarter 1983 bookings, SIA projects that 1984 worldwide semiconductor shipments will reach $14.5 billion, up more than 30% over 1983, and may approach the record 36% growth rate registered in 1979.

XENIX For NS16032 μP

In a joint statement Microsoft Corporation and National Semiconductor Inc. announced that the XENIX operating system will soon be available for National Semiconductor's new NS16032 microprocessor. XENIX is Microsoft's licensed version of AT&T's UNIX operating system specifically designed for the microcomputer marketplace to provide multiuser, multi-tasking capability. Microsoft Corporation is the largest licensee of UNIX from AT&T.

Intel Seeks Software

Intel Corp. will provide 50 of its new 286/310 supermicro systems to independent software vendors (ISVs) to enable them to write software for the systems. The 286/310, designed for OEMs, is a supermicro that uses Intel's iAPX 286 microprocessor and 80287 numeric coprocessor with Multibus architecture. The supermicro comes with either the Xenix or iRMX operating system; Intel is seeking software that will run on each.

DCA Acquires Rixon

Digital Communications Associates, Inc. (DCA) has acquired Rixon, Inc., a subsidiary of Schlumberger Limited, for $27 million. Rixon (Silver Spring, MD) manufactures low and high speed modems and data communications networking and multiplexing equipment. Rixon's sales including those of its Canadian affiliate approximated $34M for 1983.

SyQuest Secures $2.5M

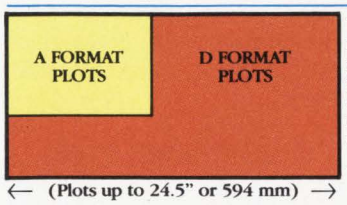
SyQuest Technology has been awarded a contract worth approximately $2.5 million to supply Santa Clara Systems (San Jose, CA) with its line of 3.9" Winchester disk drive products. Under the terms of the contract, Santa Clara Systems will purchase SyQuest's SQ306R removable 5-Mbyte Winchester drives and Q-Pak cartridges. Santa Clara Systems will incorporate the SQ306R drives into eight models of its Mini-Mega fixed/removable hard-disk subsystems.

Value Added Remarketing

Matra Datavision (Burlington, MA) has signed a Value Added Remarketing (VAR) agreement with IBM for the 43xx family of high performance computers and the new IBM Model 5080 intelligent raster workstation on which Matra's EUCLID full function CAD/CAM System Software runs. Matra will now provide a "total IBM" solution for EUCLID users.

At last. A plotter designed to run both cut sheet and roll media.

The most flexible "D" format 8-pen plotter ever.



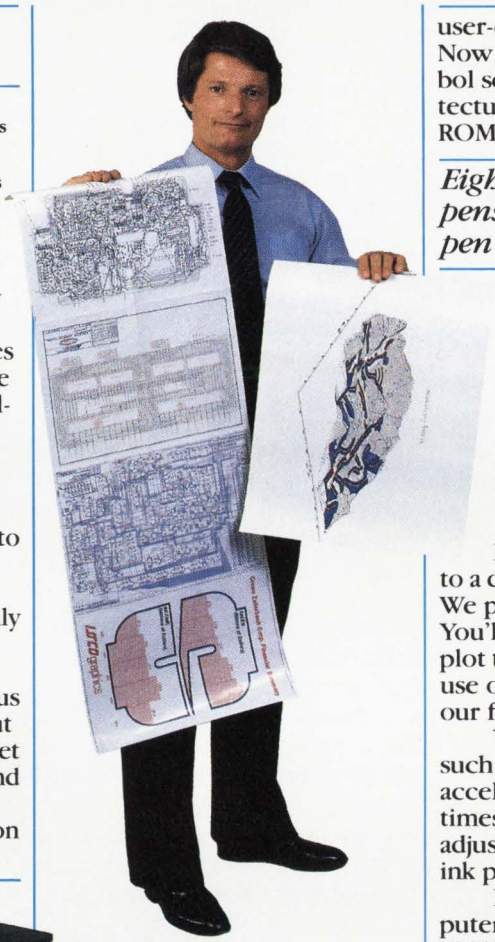
Now you can create virtually any size plots you want up to 24.5" wide, including ANSI sizes A-D and ISO sizes A4-A1, on cut sheet or roll media. Use standard bond paper, glossy bond, vellum, clear film or mylar.

Run dozens of entirely different plots automatically thanks to a built-in microcomputer that can be pre-programmed to plot on roll media up to 170 feet. Then quickly switch to cut sheet plotting – great for your pre-printed forms. The ZETA 822 is the only plotter that can do both.

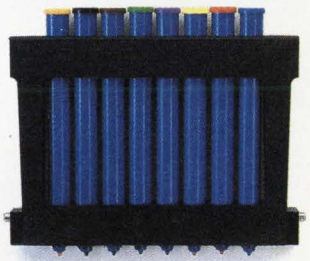
Best of all, we've got line quality and throughput at a price that makes us the cost-effective choice for just about anybody's plotter applications. You'll get vector independent speed of 25 ips. And 2 g acceleration insures the plotter reaches top speed fast. With resolution of one-one thousandth's of an inch.

Change character sets just by plugging-in a ROM chip.

Our firmware character generator produces typeset quality lettering similar to the popular Helvetica font with user-controlled proportional spacing. Now you can add special character symbol sets for both engineering and architecture simply by plugging in a new ROM chip.



Eight color, carriage-mounted pens eliminate time-consuming pen changes.



Incredibly, some plotters still grind to a dead stop to change pens. Not ours. We put all eight pens on the carriage. You'll be amazed at what that does for plot throughput. And when you want to use our liquid ink option, just snap in our four-pen cartridge.

You have total user control over such variables as speed, pen pressure, acceleration and pen up/down delay times. Touch controls automatically adjust the ZETA 822 for perfect liquid ink plots.

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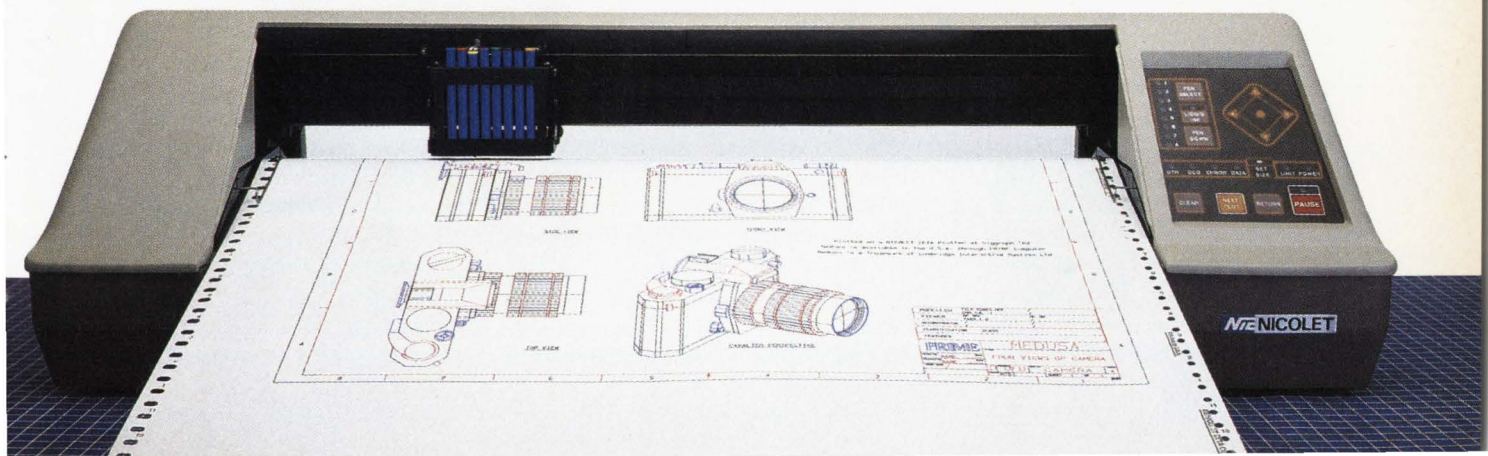

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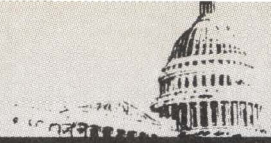


High Tech Carries Tax Burden

by Anne A. Armstrong

A group of 20 high technology electronics companies have just completed a study of the current tax policies which govern their business and concluded that the tax burden on high technology companies is 40 to 75 percent higher than on the average U.S. corporation. The group, which is called the Ad Hoc Electronics Tax Group, prepared a report of its findings for the American Electronics Association, the Computer and Business Equipment Manufacturers Association, the Electronics Industries Association, the Scientific Apparatus Makers Association, and the Semiconductor Industries Association.

More than a year in preparation, the study contends that many of today's tax policies are not well suited to help the nation's economy move toward an internationally competitive technology-based economy. The report analyzes in detail how the U.S. tax code treats research and development expenditures, investments in equipment, employee equity programs and taxation of investors in high-tech companies. In each case, the report discusses alternatives and makes recommendations.

For example, the report says the research and development tax credit should be made permanent and should be available to new companies just getting underway. Employee equity programs that permit workers to share in the growth of companies through stock options have many stringent regulations which should be eased.

The ad hoc group companies have not limited their proposals to what they believe is politically acceptable, yet they have not just written a wish list of what would be good for the industry. The group says that recommendations for change are made only when the benefits are substantial and the impact on the federal government's revenue situation is not unrealistic. The report is expected to form the basis of a push by the associations and their member companies for substantial tax reform.

Among the companies included in the Ad Hoc Electronic Tax Group are Advanced Micro Devices, Apple Computer, Control Data, Data General, Digital Equipment, Harris, Hewlett-Packard, Honeywell, IBM, Intel, NCR, Prime Computer, Sperry, Tandem, Tektronics, Varian, Wang and Xerox.

DOD Investigates Semiconductor Chip Deals

The Department of Defense's Criminal Investigative Service has indicated that an investigation is underway of several large and small manufacturing companies and wholesalers for various types of fraud involving computer chips. Brian Bruh, head of the Defense Criminal Investigative Service, would not identify any of the companies involved at this time.

He said, however, that four types of abuse are being looked at—altering certificates to show chips have been tested when they had not, changing records to extend the shelf life of certain chips, salvaging chips from scrapped equipment and reselling them as new, and substituting chips built to civilian specifications for those required by military specs.

One company was turned in on the Defense Fraud Hotline; the others were uncovered as part of other investigations.

Reshaping AT&T

Trying to follow the AT&T divestiture is a little like trying to keep track of the pea in the old shell game. The hand does seem quicker than the eye. In a flurry of reorganization announced as the divestiture began, AT&T broke up its manufacturing arm Western Electric and tucked parts of the old giant into a new umbrella organization called AT&T Technologies.

Into this new division go Bell Laboratories, Network Systems, Technology Systems (which includes components, electronic systems, computer systems and federal systems), AT&T International, Consumer Products, and the separate subsidiary AT&T Information Systems. AT&T Technologies takes over the old Western Electric role of manufacturing and, in addition, will assume control of product development and marketing as well.

The purpose of the shifts is to reshape the organization along several business product lines that will put product development, manufacturing, and marketing under the same management. Closer ties are being established between Bell Labs and the new divisions to allow shorter product development time and quicker response to market conditions.

Franklin And Apple Settle

A 20-month copyright violation suit that was beginning to drain the resources of both parties has finally been settled out of court as Franklin Computer Corp. agreed to pay Apple Computer $2.5 million for using several of Apple's operating system programs.

The suit began in 1982 when Apple charged Franklin Computer with copyright violations in its Apple look-alike, work-alikes Ace 1000 and 1200. Franklin countered with an antitrust suit claiming that operating systems embedded in computer chips cannot be protected by copyright and that Apple was trying to drive Franklin out of business. Early rounds in the legal battle went to Franklin, who was permitted to keep selling its computer despite protests from Apple.

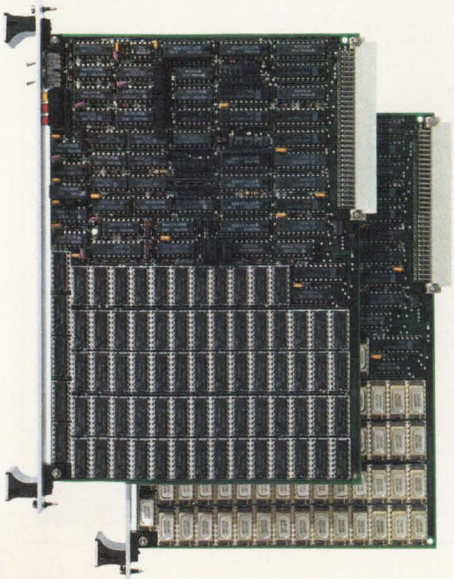
Last September, however, an appeals court in Philadelphia ruled that even software embedded on a read-only chip can be copyrighted under current law and directed Franklin to stop using Apple's software. Franklin said at the time it would appeal the decision.

In addition to the cash payment to Apple, Franklin has agreed as part of the settlement to stop using the Apple DOS operating system. Both companies have agreed to use an independent mediator instead of the courts to resolve any future differences.

A Franklin spokesman said the company would begin shipping a new operating system on machines in April. The company says that if it weren't for all the commotion raised by the lawsuit, most users would not notice any difference in the company's products.

Copyright experts in Washington see the court's decision and Franklin's abandonment of further litigation as encouraging signs that computer software can be copyrighted even when it is embedded in a chip.

In the VME board race get the pole position with FORCE



Our Racing Team: DRAM-1, DRAM-2

512KB Dynamic RAM VMEbus Board SYS68K / DRAM-1

- Storage capacity: 512 kbyte (two banks of 256 kbyte each) with byte parity
- Special error recovery mode: using the two banks in a software programmable tandem-like security arrangement
- Access time: write: 210 ns max
  read: 320 ns max
- Control/status register provides read/write, run/local, error, and parity check information
- Fully VMEbus compatible
- Run / Local function and parity check Enable / Disable switch and error indication
- Price/Performance ratio: 3.28 $ / kbyte

2 MB Dynamic RAM VMEbus Board SYS68K / DRAM-2

- Storage capacity increased to 2 Mbyte (two banks of 1 Mbyte each)
- Other features same as SYS68K/DRAM-1
- Price/Performance ratio: 3.90 $ / kbyte

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Other FORCE products of the SYS68K VMEbus family:
3 powerful CPU's, Static RAM boards up to 512 kbyte, Floppy / Winchester Controller and SASI Interface, Multichannel Serial I/O, Power Supply, Backplanes and fully integrated Systems as well as powerful software.

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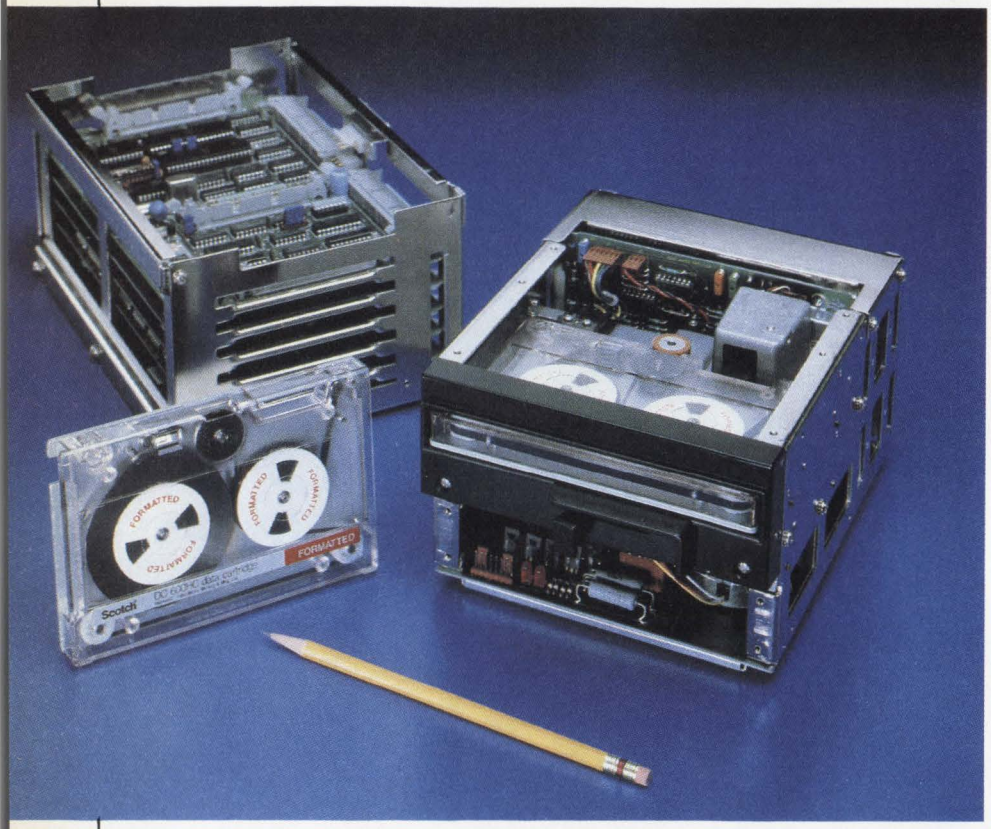
Disk Back-up Saves Space And Power



A single PC board containing the new industry standard SCSI (Small Computer Standard Interface) is now available with 3M's HCD-75 High-Capacity Data Cartridge system. It replaces a five-board controller module, offering lower power consumption.

In adhering to the Small Computer Standard Interface (SCSI) for data cartridge systems, 3M's Data Recording Products Division has taken its former controller module for the HCD-75 System and reduced it from a five board configuration to a single 6″ × 12″ board.

The HCD-75 system used for rigid-disk back-up in either the streaming or start-stop mode has used, until recently, a 3M-unique interface. The interface is still available as an alternative to the SCSI.

Not only is space reduction achieved, but the new single board controller offers lower power consumption (approximately 2/3 of previous rate) therefore lowering cost. 3M has priced the controller approximately 50% lower than presently available controllers.

The HCD-75 system has a minimum average asynchronous data transfer rate of 35 Kbytes per second, with a burst rate of up to 2.67 Mbytes per second. Data transfer 16-bit compatibility is offered with the 3M unique interface, and 8-bit compatibility with the SCSI. During all read operations, error-detection/correction routines ensure error rates of less than one unrecoverable error in 10^{10} bits.

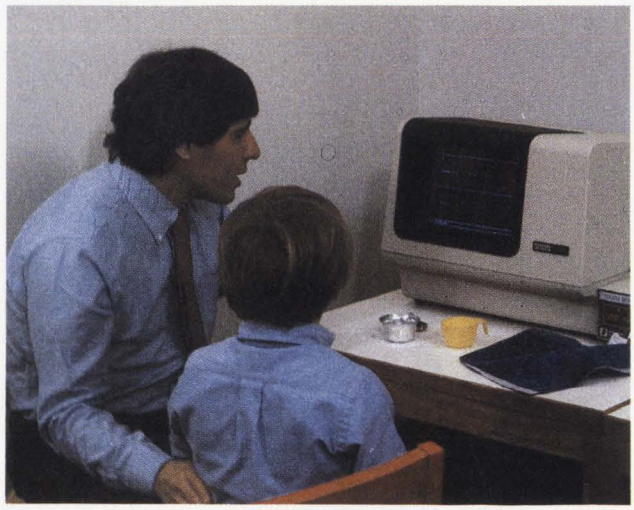
3M has also recently introduced the DC 300XL/P, a 450-foot, ¼″ data cartridge for use with a wide variety of advanced data cartridge drives. The DC 300XL/P cartridge is for systems designed to record information on 310-oersted media at signal densities of up to 10,000 flux transitions per inch (ftpi). Final testing of the DC300XL/P cartridge will be performed at 10,000 ftpi. Other enhancements include an improved drive belt, extra tape processing and enlarged load point and early warning holes. *–Hanrahan 3M Corporation*

Write 235

Dual Processor Architecture Advances The Art Of Speech Output

A recent burst of media attention has been directed toward Digital Equipment Corp's text-to-speech converter called DECtalk. Developed by the co-efforts of Dennis Klatt of the Massachusetts Institute of Technology and DEC, the system uses a three tiered software approach to synthesize speech that is of the highest quality industry has yet seen.

Klatt developed the prototype for DECtalk at MIT using a Digital Equip-



Dr. Howard Shane of Children's Hospital in Boston, MA uses DECtalk's touch screen which allows speech-impaired children to select words and sentences and "talk" with human-sounding speech.

Datacube video controller gives 20/20 vision to computers with special needs.

When it comes to video acquisition and display, this subsystem is as versatile as they come. The VG-123 is designed to handle even the most demanding applications . . . in a far more cost effective manner than any custom-made board imaginable.

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Features include high spatial resolution—768H x 512V x 8, alphanumeric overlay plane, individual pixel plane protect, pan, zoom, scroll, black and white or color images stabilized by an advanced phase-locked loop. Plus full computer access to display memory for analysis, enhancement or remote transmission.

If you have a special video processing problem, chances are the VG-123 can handle it. Call or write for full details. Datacube Incorporated, 4 Dearborn Road, Peabody, MA 01960, Tel: (617) 535-6644.

VG-123 beats doing it yourself.

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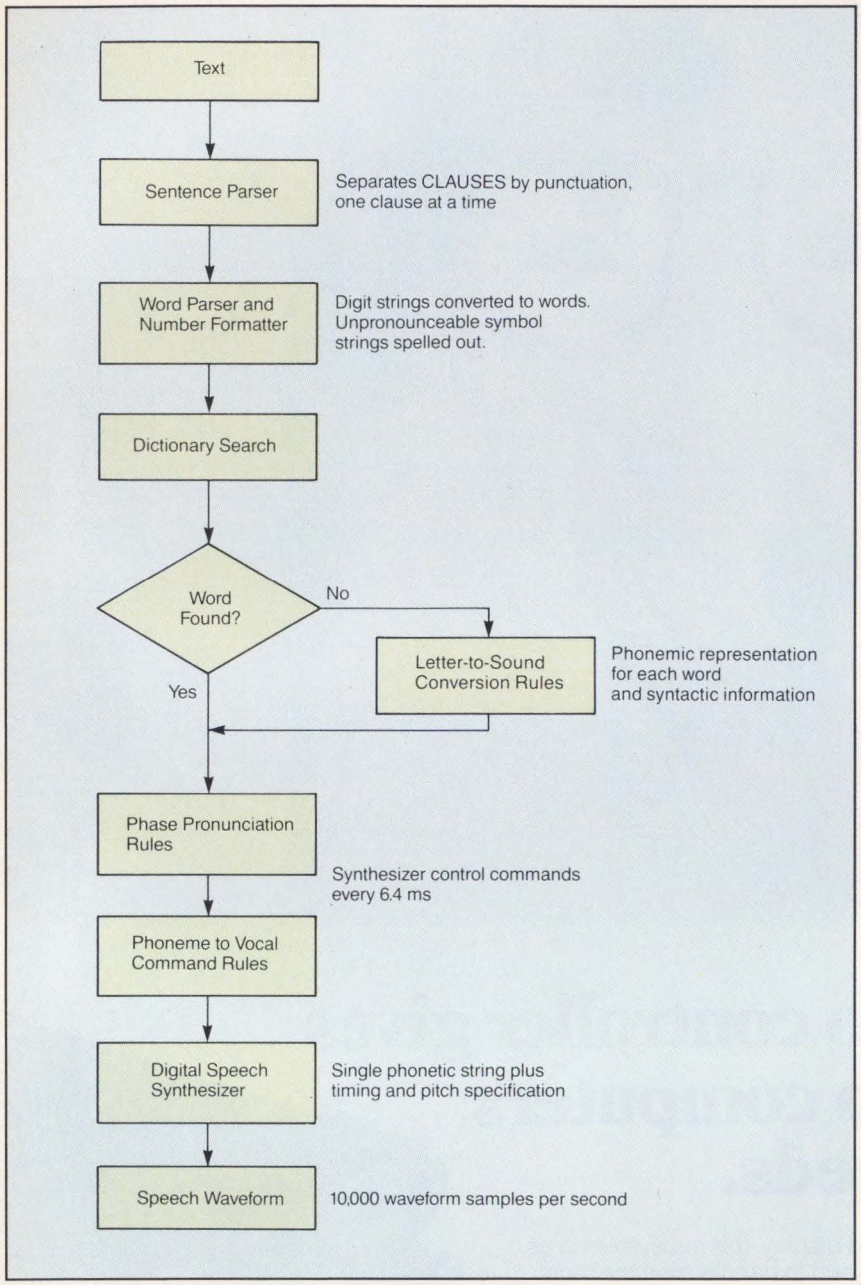


Figure 1: Text to speech conversion process utilized by DECtalk. Words are entered as text and run through three processing levels where they are synthesized into speech.

Corp's text-to-speech converter called DECtalk. Developed by the co-efforts of Dennis Klatt of the Massachusetts Institute of Technology and DEC, the system uses a three tiered software approach to synthesize speech that is of the highest quality industry has yet seen.

Klatt developed the prototype for DECtalk at MIT using a Digital Equipment PDP-11/60 Minicomputer, a high speed array processor and limited memory. What evolved at DEC under Klatt's guidance, was a board that contains a Motorola 68000 microprocessor and a Texas Instruments digital signal processing chip, the TM32010. The Motorola chip was selected because of its addressing range (10 Mhz clock and can address 16 Mbytes of memory), and the TI chip because of its speed. The computation rate required by DECtalk's digital signal processor is 36 multiplications every 100 msecs. All software for the two processor board is written in C and the system is compatible with a terminal that uses standard ANSCII text.

DECtalk uses three processing levels to turn text into speech. The first takes 8-bit ANSCII text and extracts digital representations of speech sounds. In the next level the digital representations become recognized as the input, and acoustic parameters are calculated. In the final stage, voice input is synthesized from the mathematically determined parameters.

The digital representations that are determined in the first level of processing correspond to individual phonemes. In turn the phonemes are extracted from ANSCII text, by a pronunciation lexicon, which can be viewed as a dictionary of possible phoneme combinations or words.

The phonemic representations determined on the first level are then passed on to the second, where they are modified on the basis of syntactic analysis. During this time, rules for intonation, duration and stress are applied by the lexicon.

Phonemes are approached sequentially and evaluated by a process called target selection. It is important that the transitions between phonemes are fluid as natural speech is, and this is done by a process called smoothing. A total of eighteen control parameters are calculated for each phoneme in the second level process.

Once the parameters are determined and smoothing is accomplished the phoneme sequences in the form of digital representations are passed with their parameters to the voice synthesizer. Voice synthesis is accomplished by digital signal processing. The voice synthesizer can be looked at like an electronic model of the voice tract. There is a white noise input source which corresponds to unvoiced speech and aspiration noise in the human vocal tract. This noise input source travels to the two resonators in the voice synthesizer which produce the voiced sounds. They operate by looking at three things concurrently; the current phoneme's input, the previous phoneme's output, and the output of the phoneme previous to that.

To date, this sequence outlines the architecture of the most sophisticated and high quality text to speech system available. A natural progression is for DECtalk to be available in other languages.

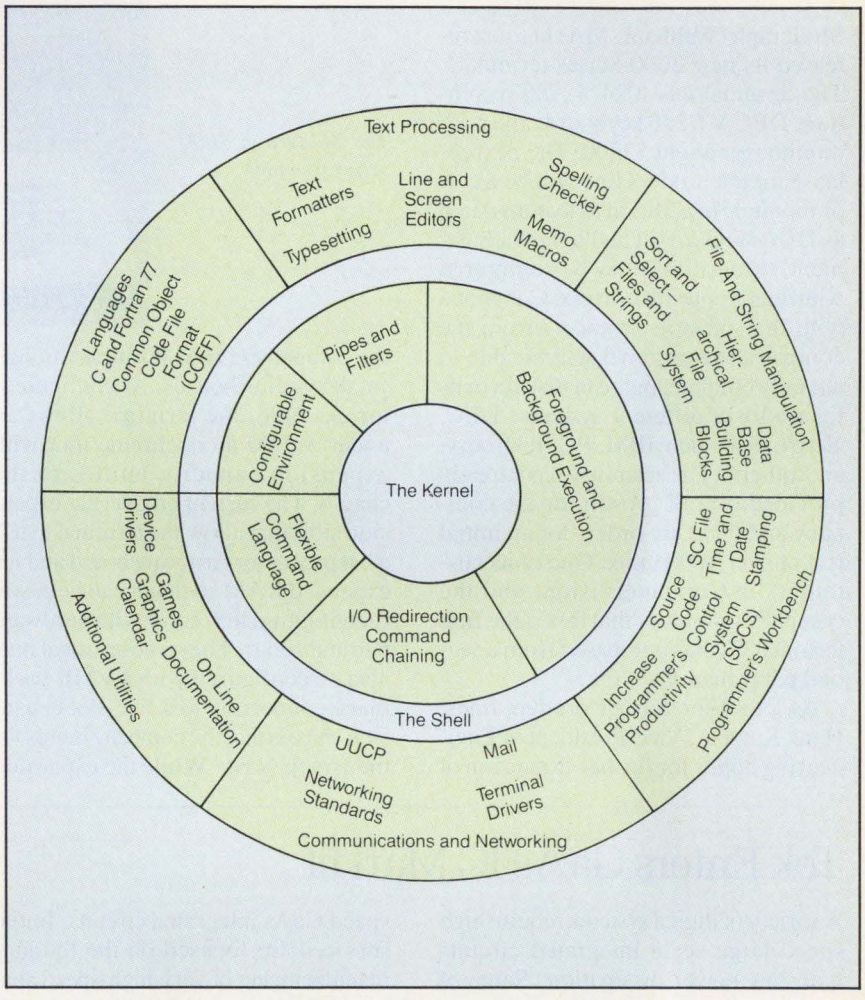
– Coville **Write 231**

Porting DOS To UNIX On M68000 Systems

Continuing improvements in high-performance 16/32-bit microprocessors, high-density RAM chips, and rotation mass storage units now greatly enhance the performance of compact, integrated desktop systems. With appropriate interfaces, peripherals, and standardization of popular operating system software, these systems may become specialized designer's workstations.

Motorola Semiconductor Product's VME/10 Microcomputer System is the first member of a modular family designed to provide a complete transition from 8-bit development systems to MC68000-family hosts. In a move to enhance standardization of operating system software, Motorola has commissioned Digital Research, Inc. (DRI) to implement its Concurrent DOS operating system on Motorola's VME/10 Development System. According to Motorola, this will enable full portability of application software between UNIX System V (which is already operating on the VME/10 and CP/M – Concurrent DOS on M68000-based systems. Because of Concurrent IBM DOS (disk operating system) mode, the application software library developed for these systems in a high-level language will be portable to the VME/10 as well.

The recently signed agreement calls for Motorola and DRI to develop 19 software packages for the VME/10 in CP/M and Concurrent DOS. Concurrent DOS which is written in "C" language, is a multi-tasking operating system which provides PC/DOS support. It includes windowing, LAN supports, graphics, and is designed for single or multi-user microcomputers. Concurrency means the user can accomplish several tasks at the same time with windowing permitting multiple screens to be displayed simultaneously. Seven of the packages to be developed will support the VME/10 UNIX System V operating system. The packages being developed include DRI's popular programming languages. These language products provide the application portability from CP/M and Concurrent DOS to UNIX System V on the VME/10. The packages, CP/M, Concurrent DOS, and library of languages, to be fully maintained and supported by DRI, will be marketed by both organizations.



The Standard UNIX-derived Operating System for the M6800 Microprocessor Family. It offers a small compact kernel, which provides process scheduling and I/O facilities to all programs. In addition, a powerful command shell for interactive system controls and an extensive set of utility programs for many tasks.

When the project is completed, by the end of the year, it will be possible to port source-code from Concurrent DOS to UNIX System V, or vice versa, with little or no code conversion required. This results in significant time and monetary savings for designers, manufacturers, and users throughout the product development cycle, allows new products to enter the market earlier, and provides for continued use of software products on absolute systems. These activities herald the increased usefulness of software which, once developed on one system can be easily transported to another.

During the first quarter, a number of CP/M products will be introduced for users who plan immediate design-ins. These include: CP/M 68K – VME/10, Digital Research C, Pascal MT+, and CBasic Compiler.

Concurrent DOS and UNIX System V/68 products to be available by the end of the year will offer a wider range of languages and utilities for most applications, yet will be a source-code compatible with CP/M-68K languages. Additionally, a port to CP/M-68K is a precursor to a port to Concurrent DOS-68K.

– *Hanrahan*

New Volley Fired in Early Release For Summer Trade Shows

The Modgraph 3000 series terminal.

Modgraph (Waltham, MA) has just released its new 3000 Series terminals. The terminal has 1024 × 780 resolution, DEC VT 240 keyboard, and a 15″ monitor for about $2800. The next release for the product line will be a color monitor. In addition to features such as DIN standard tilt and height adjustment, the terminal may be configured with dual floppy disk drives. Combined with the software protocols from the company, the terminal will be able to not only emulate, but read disk formats for up to 18 different systems: DEC, Xerox, Televideo, IBM, PC, Tektronix, and others. The terminal has already provided overall growth for the company and there are orders for an initial run of over 3000 units. One of its customers is Computervision, and the company points out that this is the first terminal CV has purchased from a second party manufacturer.

As a tool for further product lines, Hank Kunicki, Vice-President of Engineering hopes for further expansion of the company's OEM business through small systems houses. As configured, for example, the terminal allows an under $3,000 monochrome unit with expansion capacity built into the chassis. The current product has expansion slots that allow the terminal to use a list processor firmware board and for expanded RAM so that it can be easily reconfigured into color with hardware pan and zoom. The same terminal may also be configured with a VME backplane connection to a five-slot expansion chassis that the company builds for the Israeli Navy. While the expansion chassis is currently shipped with support for 1280 × 1024 × 60Hz, and 64 bits of pixel memory, its compact size and high reliability give the company the capability of expanding into performance ranges comparable with much larger manufacturers.

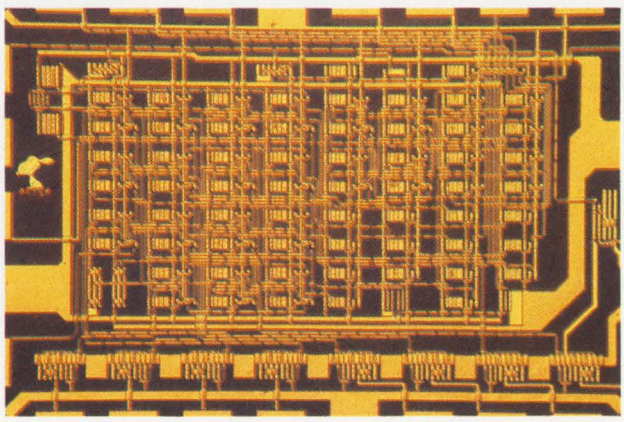
One of the keys to the company's success is the use of the Signetics Microcontroller Chip (8X305) which combines bit-slice technology with an 8-bit microprocessor capability. Other engineering features include built-in expansion capability for 256K RAM chips.. — *Borrell* **Write 236**

Tek Enters GaAs IC Market

A variety of digital systems require high speed large scale integrated circuits with low power dissipation. Some of these applications are in the areas of high speed digital signal processing and high speed computers. GaAs technology is attractive for implementing LSI level circuits due to its ability to build low poser gates with reasonable speeds.

Tektronix, Inc. traditionally a manufacturer of high performance test and measurement equipment has recently become heavily involved in GaAs technology development. Recently they have announced that GaAs ICs will be sold on a contract basis to customers outside the company in selected markets. The decision to make GaAs IC's available to outside customers is predicated on the belief that applications of this technology extend far beyond the company's own product lines.

In conjunction with this business decision is the announcement of the formation of a new business entity to serve the needs of customers requiring high-speed GaAs integrated circuits. Initial services are focused on the foundry manufacturing of very-high-speed analog and digital circuits, using the Tektronix high-yield, depletion-mode process. This includes digital gate arrays and custom devices operating at clock frequencies up to 4 GHz with gate counts up to 500. The analog version of this process supports on-chip precision resistors, inductors, and capacitor components, and can be designed to yield analog circuits operating to 12 GHz with complexity above 50 transistors. Tektronix has established a comprehensive IC process design package and consulting service to aid customers. — *Tektronix* **Write 234**



A gallium arsenide MSI 8-bit Multiplexer and Demultiplexer circuit capable of 3 gigabits/second performance.

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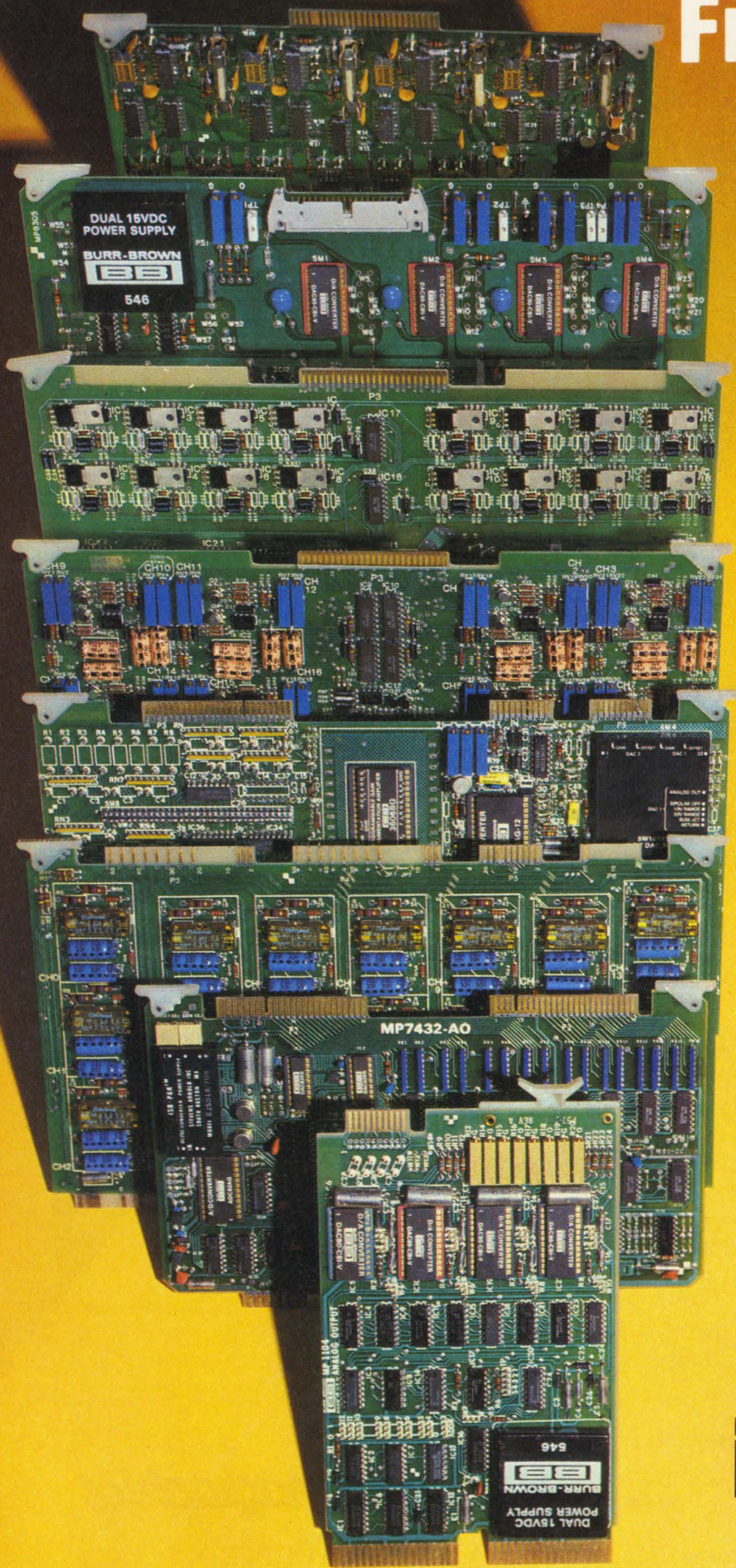

More than 60 different analog/digital I/O boards provide a variety of off-the-shelf, plug-in quick solutions for sensor-to-microcomputer bus compatibility. Designed - proven in Intel Multibus™, Motorola Micromodule, DEC LSI-11 and Zilog MCB/MCS (and others), these boards offer the important features that save you time and money.

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- Optical isolation on inputs - output relay isolation
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NEW TIMING FUNCTION BOARD has optical isolation and optional input debouncing . . . up to 15 channels, 16 bits per card . . . software programmable cascading of counters up to 80 bits. Use for clock, pulse counting, pulse frequency and pulse-width measurements. 60+ boards are described in a new Microcomputer I/O Board Brochure . . . ask for it!

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Apple Unveils 32 SuperMicro Family

Apple Computer recently introduced its Apple 32 SuperMicro family, including the much-anticipated Macintosh and a series of enhanced Lisa computers.

One of Apple's design goals for Macintosh was to produce a low-cost, powerful personal computer with built-in Lisa technology. Apple believes it has accomplished this by building into Macintosh all the basic hardware requirements and by providing a way to expand the system through software.

Apple is supporting the work of independent software vendors to develop Macintosh programs. Apple expects its development program will make at least 500 software packages available for Macintosh by the end of the year. Currently Lotus Development is rewriting its popular Lotus 1-2-3 for Macintosh, and Microsoft Corp. expects nearly 50% of its applications revenues in 1984 to come from Macintosh software. More than 100 major software and peripheral vendors are developing packages for Macintosh, including Software Publishing Corp., Continental Software, Ashton-Tate and Sorcim Corp.

Software from these major developers will spur Macintosh sales in two of its primary markets – small and medium size businesses. To reach these business customers, Apple will sell Macintosh through the 3,000 dealerships already selling Apple products. The company expects that nearly 85% of Macintosh sales will come through retail channels.

Before the end of this year, according to industry analyst Jean Yates of Yates Ventures (Palo Alto, CA), worldwide sales of Macintosh could total 350,000 units this year, with 70% of sales going to business, 20% to colleges and universities and 10% to home users. A $20 million, automated factory designed to handle the high volume of expected orders has been built in Fremont, CA.

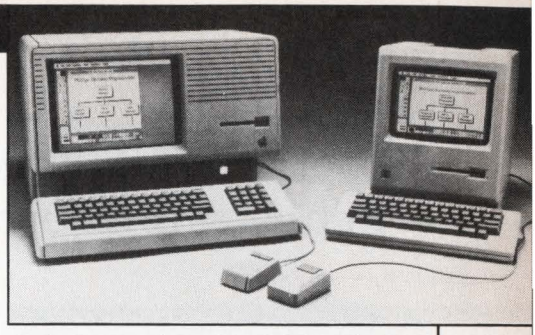
Based on the advanced, 32-bit architecture developed for Apple's Lisa computer, Macintosh, along with three powerful new Lisa 2 computers, forms the basis of the Apple 32 SuperMicro family of computers. All systems in the family run Macintosh software.

Macintosh uses its built-in user interface software and high resolution display to simulate the actual desk-top working environment – complete with built-in notepads, file folders, a calculator and other office tools.

The basic Macintosh includes a main unit housing a 9", 512x342 pixel, black on white display; a central processor; a built-in disk drive; two serial ports; built-in sound and speech hardware; a keyboard and a mouse.

Based on the 32-bit Motorola 68000 microprocessor, Macintosh supports a variety of sophisticated capabilities, including fast, bit-mapped graphics. Macintosh has 192 Kbytes of ROM and 128 Kbytes of RAM. Built into every Macintosh ROM is Lisa technology with pull-down menus, windows and graphics routines.

For Mass storage there is a 3½" disk drive with diskettes holding 400 Kbytes to each side. Apple's new Lisa 2 series of computers also use the 3¼" disk drive enabling Lisas to run Macintosh programs. Macintosh retails for $2,495.



Apple Computer's new Lisa 2 (left) and Macintosh are part of an expanded family of compatible products called the Apple 32 Supermicro System. Products in the family incorporate Lisa Technology, 32-bit microprocessors, high-resolution bit-mapped graphics and mouse pointing devices, and all run Macintosh software.

The Lisa 2 series of computers completes the family of 32 SuperMicros. Lisa 2 has 512 Kbytes of Internal memory and a 3½" microdisk drive for mass storage. The Lisa 2/5 and 2/10 share these features but offer additional mass storage: the 2/5 has an external disk and the 2/10 has a built-in 10 Mbyte hard disk. Each computer in the Lisa 2 series can run Macintosh programs.

Write 238

Proprietary VLSI and Multi-Processor Architecture Extends Raster Product Line

Figure 1: The Model One/80 is the heart of a high-performance graphics system for mechanical and electrical CAD, simulation, modeling, and geophysical applications.

Figure 2: The Model One/10 graphics terminal combines monitor, keyboard and controller in an attractive desktop package.

Software compatibility across the line is an integral part of any interactive graphics product line. Raster Technologies (N. Billerica, MA) has extended their price/performance spectrum with the addition of two compatible extensions to its Model One family of graphics systems.

The Model One/80 combines a 16-bit microprocessor, a high-speed bit-slice processor and proprietary VLSI accelerators to provide graphics functionality. Drawing more than 70,000 one-centimeter random vectors a second, the Model One/80's hardware-supported double buffering provides vector drawing rates up to 115 million pixels per second. The performance of the Model One/80 has been optimized for graphics applications running on 32-bit workstations and computers. Prices for the Model One/80 begin at under $20,000.

Available with a resolution of 1280 × 1024 with either eight or 24 bits of image memory, the Model One/80 sports refresh rates of 60 Hz noninterlaced, while 30 Hz versions are available for use with standard RS-343 monitors.

The Model One/80 bipolar processor and hardware accelerators execute most common graphics functions. Commands such as moves, draws, filled and unfilled rectangles, pixel image transfers and area moves are processed directly by these specialized processors with no microprocessor intervention. The microprocessor serves as an on-board self test device which can perform multiple levels of diagnostics at system power up and service. These internal diagnostics can isolate faults to the sub-module level, and indicator lights on each printed circuit board show successful completion of self test.

The Model One/80 has been designed for applications in mechanical and electrical CAD, simulation, modeling and geophysical applications and is an ideal graphics system for 3D applications that require shading and hidden-surface removal.

Raster has slotted its Model One/10 terminal into the market for personal design stations in distributed engineering and scientific applications due to its local processing capability and low cost.

The Model One/10 uses a 16-bit microprocessor and proprietary VLSI processors to achieve its vector writing performance of over one million pixels per second. VLSI hardware performs image memory refresh and timing, video refresh at 60 Hz noninterlaced, and hardware vector clipping and picking. High-speed local display capability is offered and VT-100 capability is a standard feature. Prices for the Model One/10 begin at under $6,000.

The Model One/10 and Model One/80 provide the same software development environment that characterizes the other members of the Model One family and will support the same selection of third party graphics packages that have been adapted to previous Model/One products. The command-set includes 125 commands with primitives for all standard functions and provide CORE and GKS functionality.

Raster does not have plans to enter the general-purpose graphics workstation market, fully intending to remain a specialized graphics peripheral product. Their focus will remain on OEM contracting and their current customers include Gould, Landmark Graphics, Genigraphics, and Cadmus.

– Hanrahan

Raster Technologies, Inc. **Write 232**

Any Way You Look at it, the GX-100 is Best-

As a Graphics Terminal,

The Modgraph GX-100 Graphics Terminal offers the serious graphics user extensive capabilities for little more than the cost of an intelligent alphanumerics terminal.

The GX-100 provides an easy to view 15" screen, ***two*** pages of 768 × 585 resolution, Tektronix® 4010/4014 emulation, printer and digitizing tablet support, and a full range of well thought-out graphics features. The GX-100 runs PLOT-10™, MEDUSA™, TEMPLATE™, MACCS™, DOGS, DI-3000™, AIDS, TELL-A-GRAF® , DISSPLA® , and others.

For text applications the GX-100 emulates the VT100, VT52, and ADM-3A. ***Two*** independent pages of alphanumerics hold ***six*** scrollable screens of text to meet your alphanumeric needs as well.

For superior graphics and versatility, the GX-100 has been chosen by a wide range of CAD/CAM, education, and business users.

Or as a Graphics Workstation.

The GX-100 terminal expands into the GX-100 F5 workstation, adding local processing capability to increase productivity. You can start with a terminal and later retrofit to a workstation.

The workstation includes dual 5 1/4" floppy disks, and CP/M™ and can be run on-line with your CPU or locally with stand-alone graphics packages such as GraphTalk™, DRGRAPH™, and DRAW™. Our unique disk controller reads and writes 15 different disk formats for ready compatibility with many available text and graphics programs.

All this for a surprisingly low price of under $4,500 for a complete system.

Discover what the serious graphics user already knows...any way you look at it, the GX-100 is best.

Modgraph

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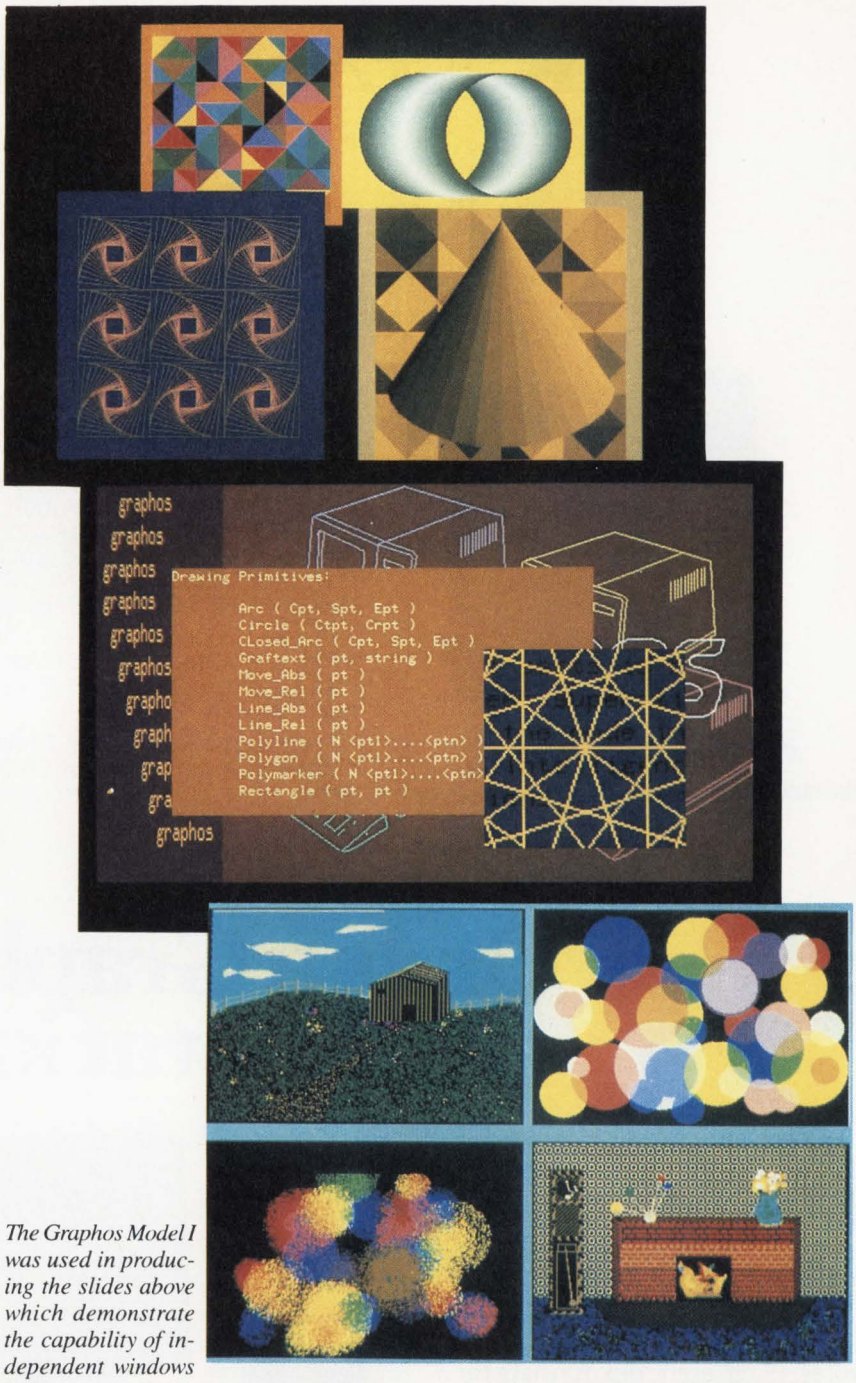
Enhancements In Color Windowing

Ithaca Intersystems, manufacturer of graphics terminals and Z-80 based computer systems, is readying two new product lines for the summer graphics shows that will expand its line of multiple windowing graphics terminals. With a current order backlog of over 200 units for its GRAPHOS products line, the company is announcing its GRAPHOS II and III. The company's products currently compete in the Tektronix 410X performance arena, but its costs are significantly lower. Aimed at initial product environments in process control, statistical analysis, slide presentations, and geographical/geological use, it is found in VAX/sophisticated end user markets.

The new product lines will provide both higher performance (the GRAPHOS III) at a higher cost and at a lower cost (the GRAPHOS II), similar performance to its existing product lines. The new products reflect design changes in hardware. Higher cost ECL parts have been replaced with TTL logic. TTL parts requiring lower power have allowed the company to make use of a hybrid power supply built and designed by the company itself, further lowering cost. Finally, there is a great deal of mechanical simplification in the card cage, wiring, and communications to the monitor.

The company will continue to make use of the Motorola 68000, offering the same 6.3 MHz processor on the lower cost terminal, and a 12 MHz on the higher performance system. The S-100 bus has also been dropped for a proprietary design which has allowed mechanical simplification. Jeff Moskow, Director of Engineering, points out that while implementing a formal bus standard requires greater hardware overhead cost due to the need for bus arbitration, bus connection, and a card cage, the design must have greater quality to insure that the loss of flexibility through the open architecture does not limit the system's use. Like many others such as Lexidata, Raster and Metheus, the company has moved to a single board processor with the unique exception of daughterboard connectors for the main board which allow the system user to plug in cards for either mouse or tablet interface.



The Graphos Model I was used in producing the slides above which demonstrate the capability of independent windows with up to 16 colors each, or features such as independently scrolling test. The final slide was produced with a paint program and shows the use of pattern attributes for textures.

While the company does not compete with the fast draw times of the three above-mentioned companies, it does have an individual niche for windowing that many of the workstation manufacturers and integrators desire. Despite its low cost, the company is able to support up to 16 independent windows on a screen through hardware, unlike the software windowing of firms such as SUN, Apollo, and others. Each of these virtual screens has up to 4 bits of pixel memory for 16 colors, which allows the terminal to offer up to 256 colors with multiple windows displayed simultaneously. The companies investment in firmware for its ROM segment memory also provides graphics features such as color look-up table management, screen refresh, window management, and attributes.

– Borrell **Write 237**

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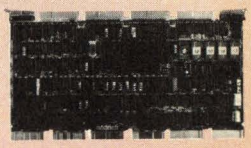

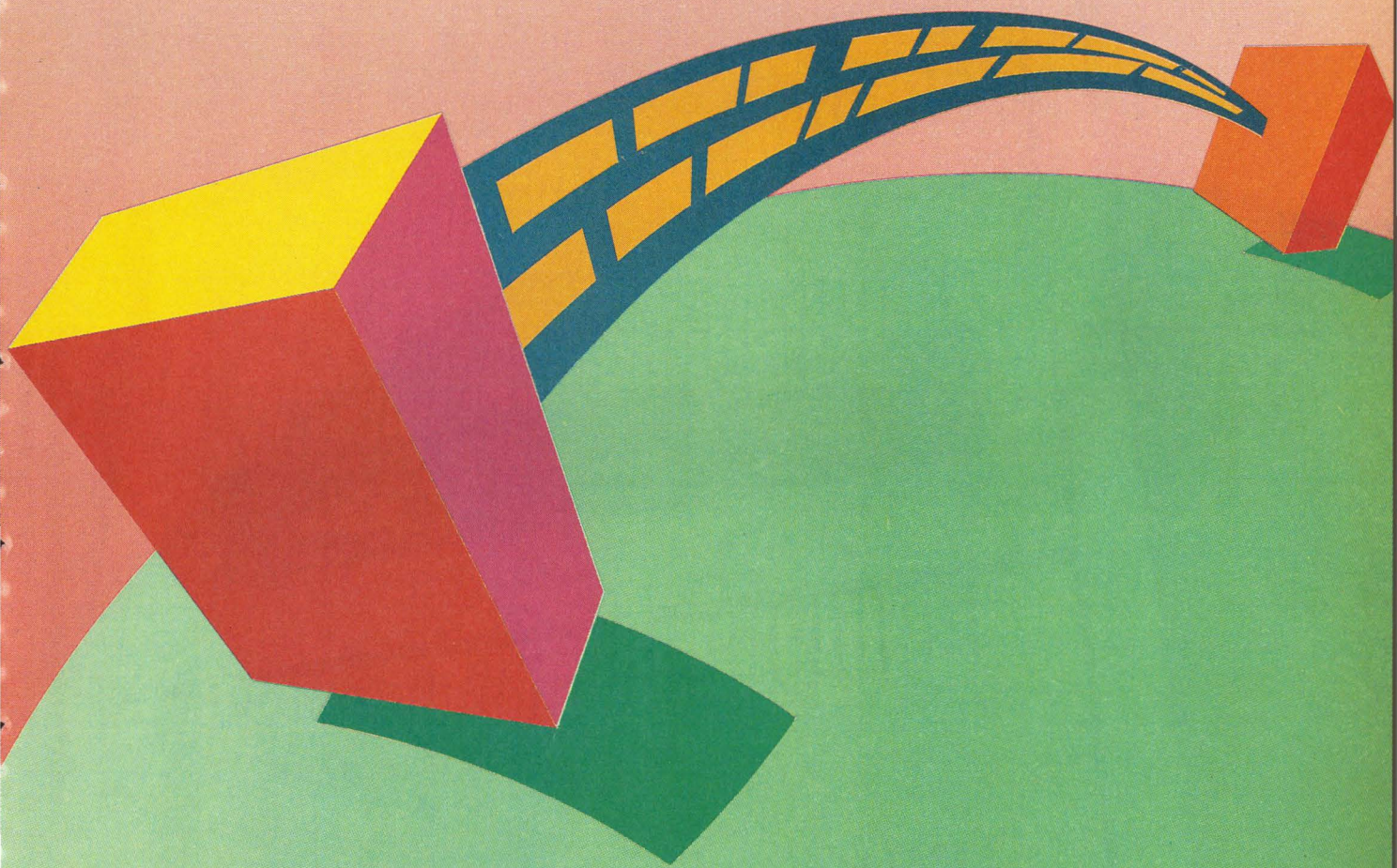

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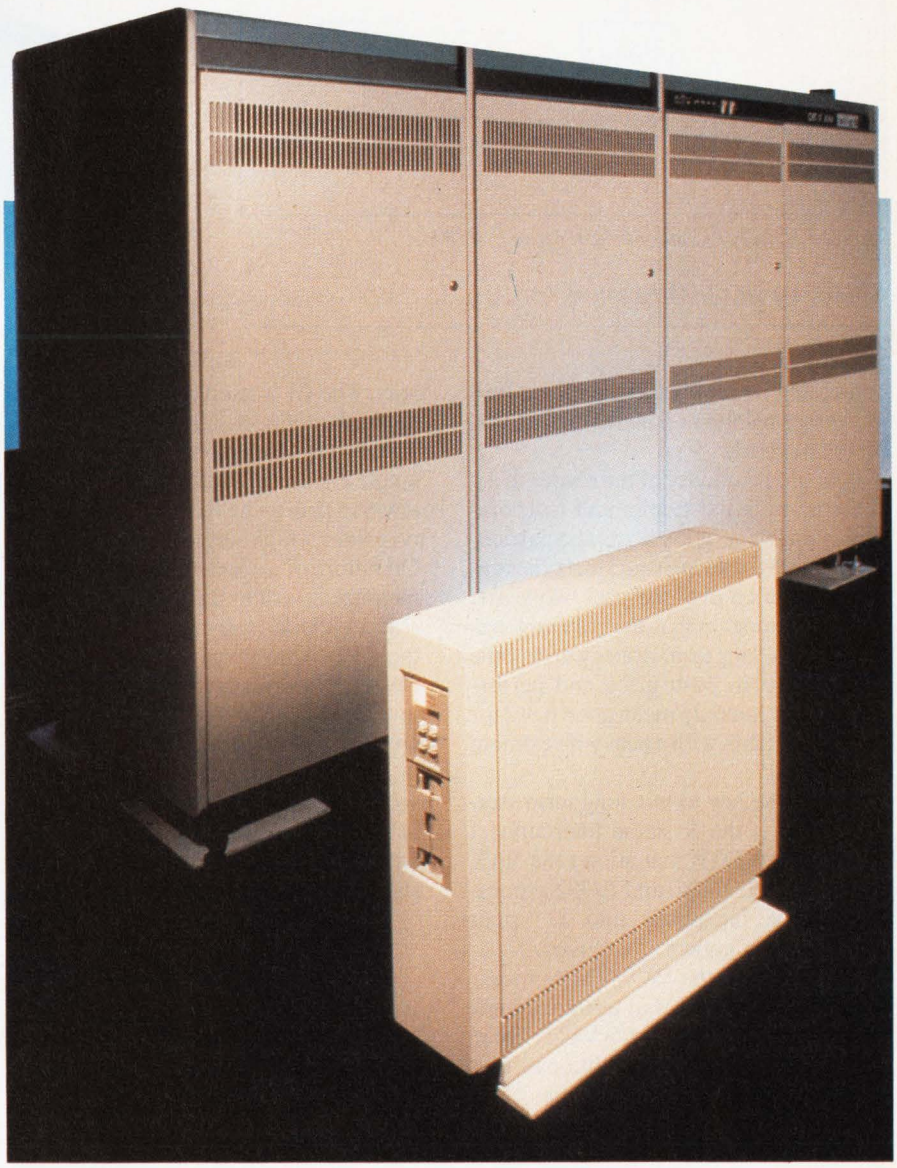
DEC Compatibility Takes On New Meaning

Fault-tolerance, intelligent subsystems and multiprocessing have surfaced in DEC's higher-end systems.



DEC's 11/780 shown against the microVAX 1.

by Dave Wilson,
Senior Technical Editor

Perhaps more than any other single factor, Digital Equipment's VAX architecture has been one of the unique strengths of the company over the past few years and will continue to be so. 1983, however, saw competition for the VAX line coming thick and fast from both application-oriented systems integrators such as Apollo, and from vertically integrated companies such as Intel, HP and Data General.

Companies of the former class usually take the best available commodity products and integrate them into systems, standardizing on microprocessors such as the 68000, buses like the Multibus, and industry compatible disks.

The vertically integrated company, on the other hand, is traditionally Digital's old competition, having the resources to create specifically tailored hardware and match it to their own software. Because they are not bounded by a fixed set of choices for either hardware or software, they can build a total solution that may be more competitive than any sum-of-the-pieces solution.

The competition against the VAX on these two fronts has been born out of the realization that traditional timesharing systems will evolve into distributed networks of computing nodes communicating with each other over a common network architecture. The user of these systems will have little or no awareness of where computations are taking place.

One example of this strategy is Syte Information Technology's (San Diego, CA) claim against the VAX. "We intend to prove that multiple, tightly coupled microcomputers with state of the art software are superior in performance to superminis like the VAX 11/750 and the 11/780," said Syte's President Peter Shaw when his company's 1600-based workstation was announced. Syte's Global Environment Manager (GEM) System software creates a "virtual environment" giving each user immediate access to the

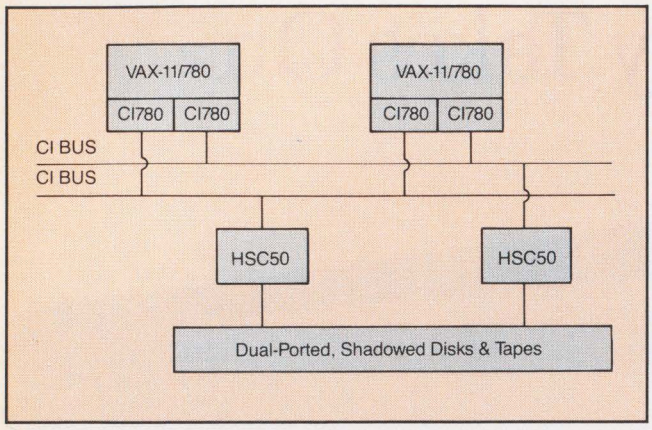
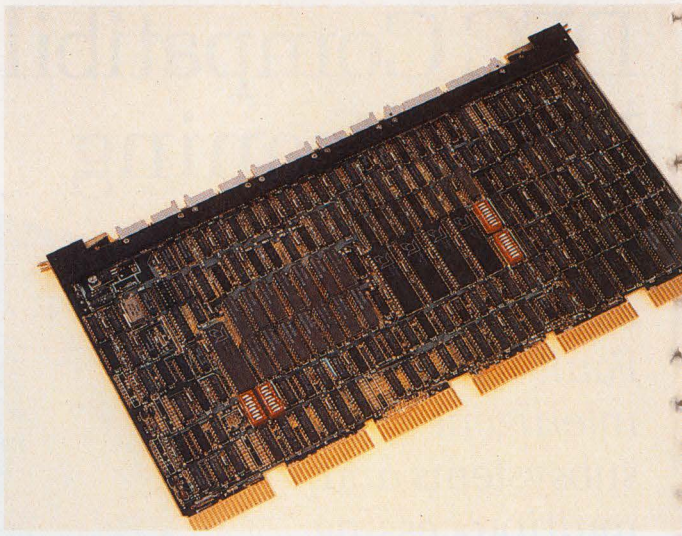


Figure 1: A fully redundant cluster using 11/780s.



Right: Dataram's UDA50 controller.

computing power of other stations as well as to other resources (such as disk drives) on the network.

It would be unwise of the reader to assume that Digital Equipment Corporation is unaware of these trends, particularly in light of the new product offerings it has unveiled over the past two years. Rather, it appears that the company has developed a long term strategy to become competitive in both price and performance that can only mean good news for Digital's OEMs with a heavy investment in software.

Part of the key to this long term strategic plan is the Systems Interconnect architecture (DSI) that allows the VAX 11/750, 11/751, 11/780 and 11/782 processors to be integrated into a system configuration known as a cluster.

In addition to the VAX/VMS processor(s), mass storage and terminal communications capabilities, a VAX cluster system includes four additional elements—the Computer Interconnect, a dual-path high bandwidth bus, the CI750 and CI780 intelligent CI port controllers, the HSC50 intelligent storage server and a Star Coupler that serves as the central hub of the cluster and the interconnection point for all cluster nodes.

Fault-tolerant computing

VAX clusters can be configured to withstand the failure of various components in the cluster and yet maintain a level of system availability that is determined by the level of hardware redundancy in the cluster and the features of the VMS operating system that are used. A fully redundant cluster comprises two identical processors. The CI is itself a dual path redundant interconnect. Each mode (CPU or HSC50) is connected to both paths of a single CI. In this configuration there is always a path to the HSC50 mass storage, no matter which single component fails. On failure of a specific volume an error message is sent to the user.

If a CPU fails, local mass storage on the CPU is no longer accessible to the cluster. However, the integrity of data and investment in CPU time can be maintained despite such a failure by using data integrity and check pointing tools provided by VMS. As long as there is still a path to the journal or checkpointing data on mass storage, the recovery and/or restart can take place at another node in the cluster, but the restart must occur on an identical CPU. VMS software components can identify the failure of a VAX cluster hardware element and then take action to keep the rest of the cluster operating despite the failure.

The Computer Interconnect (CI) itself is a 70Mbit per second dual path packet bus used to transfer serial data between the nodes of a VAX cluster. Up to 16 nodes can be connected to the CI and each node can be a VAX or an HSC50 mass storage server.

The physical interconnections are the CI750 and the CI780 computer interconnect adapters and a Star Coupler unit. The adapters are microprogram-controlled intelligent devices that per-

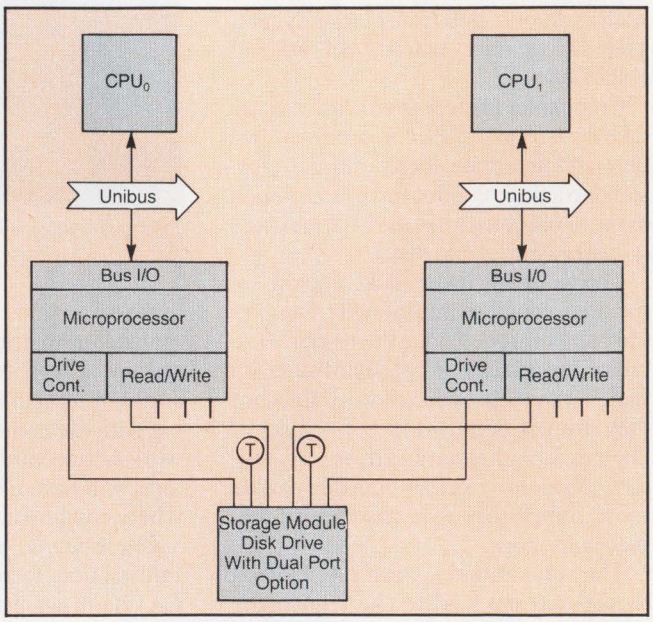


Figure 2: Dataram's Industry First: A UDA-compatible controller and dual ported-configuration.

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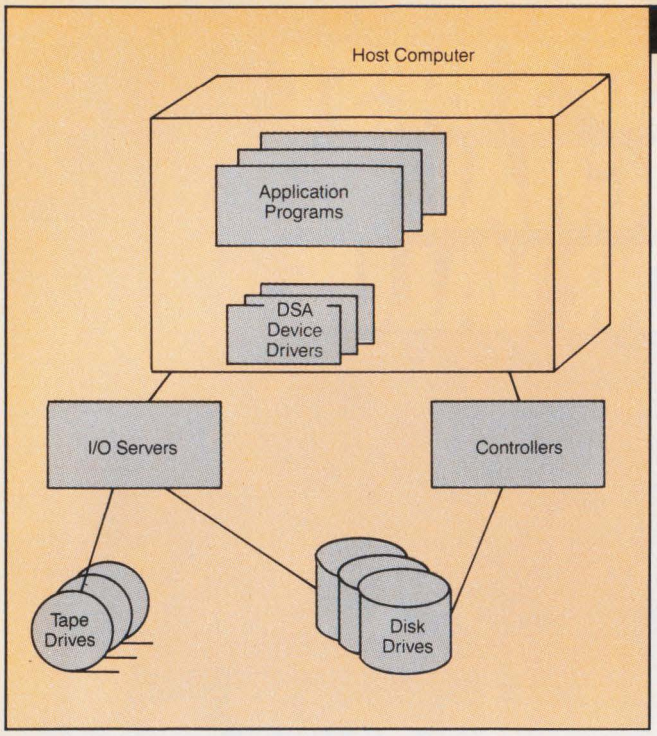

Figure 3: A breakdown of the Digital Storage Architecture.

form the functions of fully buffered communications ports. Messages are transferred in blocks of data between the CPU memory and other nodes within the VAX cluster by the VMS and DECnet software. The star coupler connects together all CI cables from the individual nodes into a radial or star arrangement that has a maximum radius of 45 meters.

The HSC50 (Hierarchical Storage Controller), a self-contained mass storage subsystem, connects one or more host processors to a set of mass storage disks or tapes. Itself a cluster node, the HSC50 communicates with host CPUs via the CI and uses Digital's Mass Storage Control Protocol for host communications. Initially, Digital is offering VAX cluster configurations in which each HSC50 controller can provide storage access for as many as four processors. Later they will offer VAX clusters where each HSC50 will provide storage access to additional processors.

The new Digital Storage Architecture and Mass Storage Control Protocol has not only been implemented in the HSC50 for CI systems, but in the UDA50 for Unibus systems as well. Furthermore, the recently announced RC25 8" disk subsystem embedded in the new VAX 11/725 also provides most of the DSA capabilities, an indication that DEC will take care of the architecture down to its MicroVAX line as well.

The intelligence of the HSC50 and UDA50, as well as the controller design, assure that the Unibus will not be saturated with data. According to Loius Finnegan at Aviv, (Woburn, MA) the same can be said of the Q-bus, particularly with the advent of the 11/73, KXT11-C and microVAX. Yet other changes are expected in this area from DEC that will maximize the use of existing Unibus and Q-bus structures.

Intelligent Storage

Within the DSA framework, DEC separates mass storage functions into 3 specific layers. In addition, the DSA defines standard interfaces between the host computer system and the controllers and between the controllers and the storage devices. The DSA itself greatly reduces the host computer's role in mass storage control; the central processor treats disk and tape drives as simply classes of devices, i.e. disk or tape, and the controller handles all the specific characteristics of each drive, like cylinder and tracks.

Under the DSA, the bulk of mass storage functions are handled within the intelligent controller layer. By coordinating the activities of all devices attached to it, the controller optimizes performance of the entire subsystem. Another responsibility of the controller is to present the host computer with manageable workloads. Because data transfers from stor-

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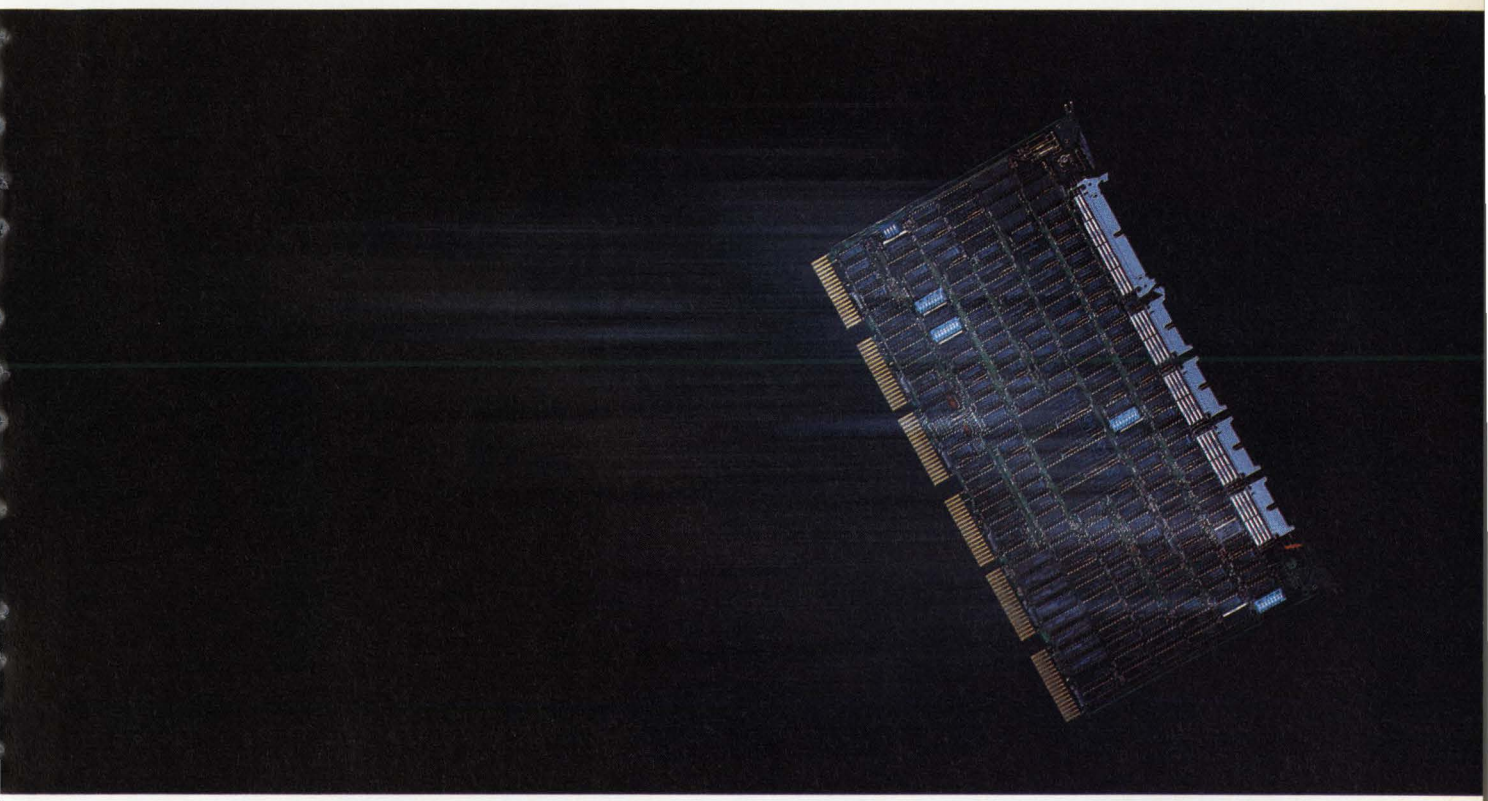

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DEC Compatibility: Performance Advantages Become Tougher To Design In

In the existing DEC compatible world, vendors must offer some performance advantage over DEC lines to survive. In the future, especially in the disk and tape controller area, this may take considerably more investment than it has in the past, due to the intricacies of architectures that DEC has, and will, announce.

Digital Equipment does not always view its compatible vendors as competition. In some cases a product is endorsed and sold by DEC in the UK, which is often a testing ground for DEC domestic.

One example of this philosophy is DEC's relationship with Virtual Microsystems (Berkeley, CA), who currently offer a product line that allows all of the DEC minis (11/02 through VAX) to run micro applications under MS-DOS, CPM-86, CPM-80 and the p-system. The Bridge Systems eliminate many of the disadvantages currently associated with microcomputers—their isolation from one another making shared data awkward or difficult, and the justification for purchasing high quality peripherals. The result is that as a task under the operating system of the host, any minicomputer user can, from a dumb terminal, address Bridge add-on boards and execute standard microcomputer software.

The announcement of DEC's three new VAX systems (see **Table 1**) over the past few months should also provide substantial opportunity for add-in, add-on vendors and systems integrators, not least of all because DEC chose to build the systems around its existing bus structures, the Q-bus and the

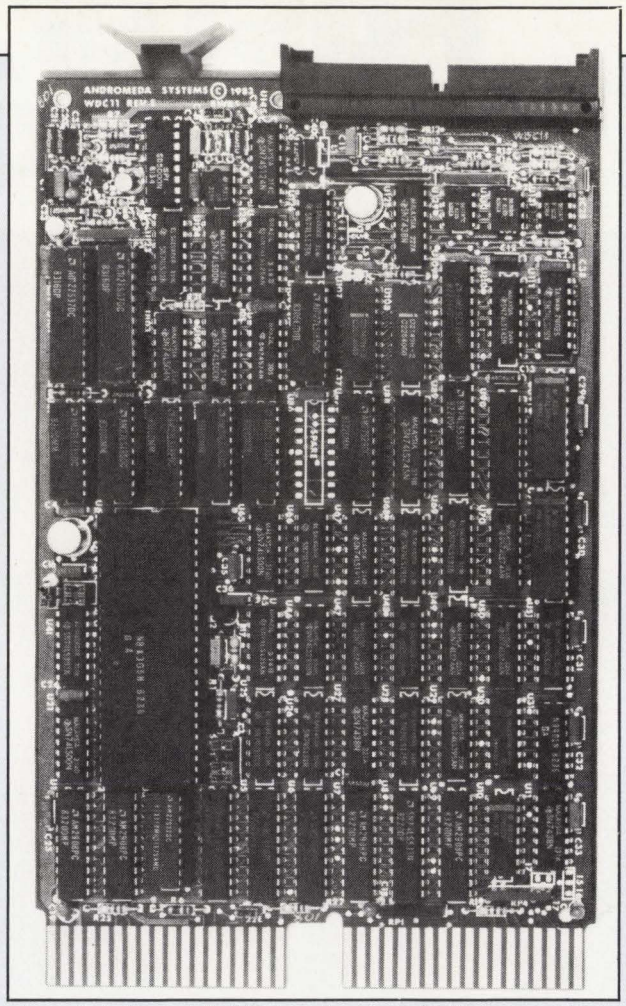

Figure 1: Andromeda's Q-bus card supports DMA systems removable drives.

	Micro/PDP-11	MicroVAX I	VAX 11/725	VAX-11/730 SBB
BUS	Q-Bus	Q-Bus	UNIBUS	UNIBUS
FPA	YES	NO	YES	YES
DISK Size FRS Capacity	5¼" 10MB/28MB	5¼" 10MB/28MB	8" 52MB	14" 1.5GB
BACKUP MEDIA	Floppy	Floppy	Removable Disk	Removable Disk or Tape
OPERATING SYSTEM	All PDP-11 Operating Systems	MicroVMS MicroVAX ULTRIX VAXElan	VMS VAX ULTRIX	VMS VAX ULTRIX
PRICE	5-13K	10-20K	25-37K	56-70K
GRAPHICS	NO	Planned	VS100	VS100
Decimal	Hardware	Software	Hardware	Hardware
Floating Pt.	Hardware	Hardware—F/G Software—D/H	Hardware—F,D,G,H	Hardware—F,D,G,H
PDP-11 Compatibility Mode	N/A	NO	YES	YES
Software	All PDP-11 Operating Sys	MicroVMS VAXElan MicroVAX ULTRIX	VMS VAXElan VAX ULTRIX	VMS VAXElan VAX ULTRIX

Table 1: Architectural Comparison of the new DEC Machines.

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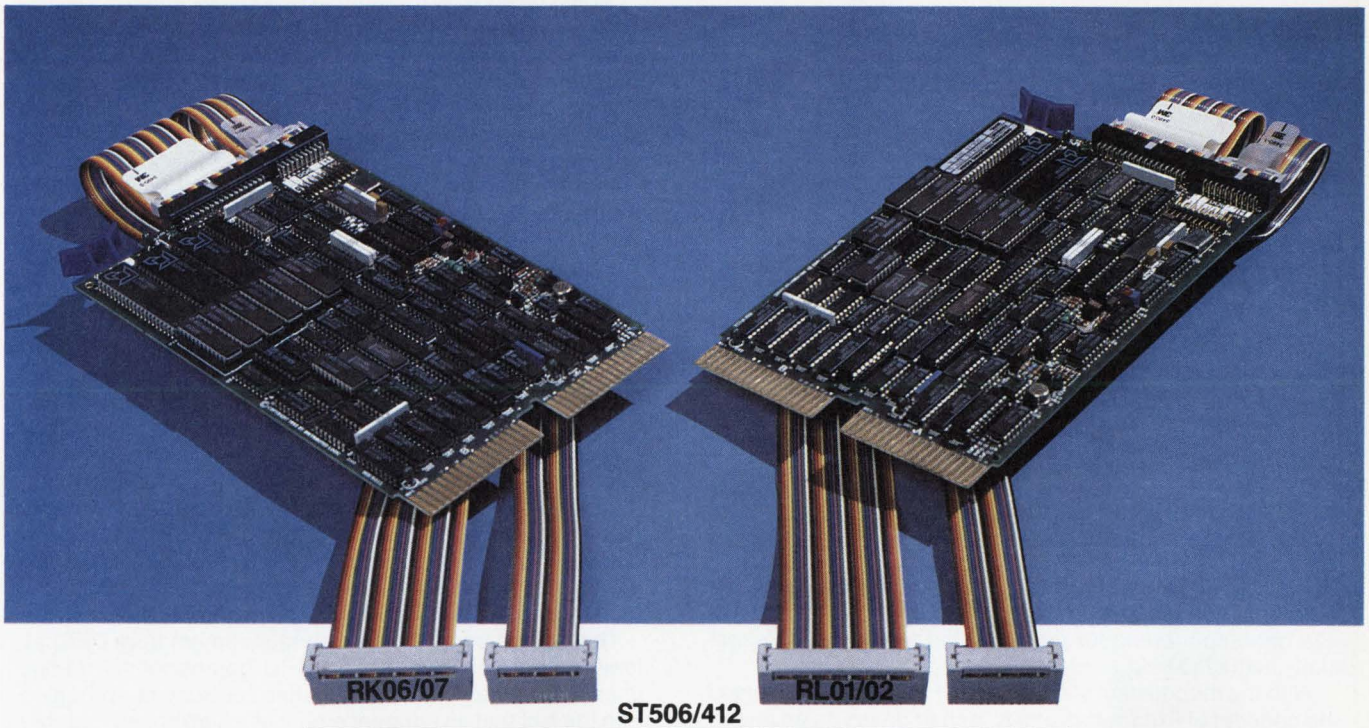

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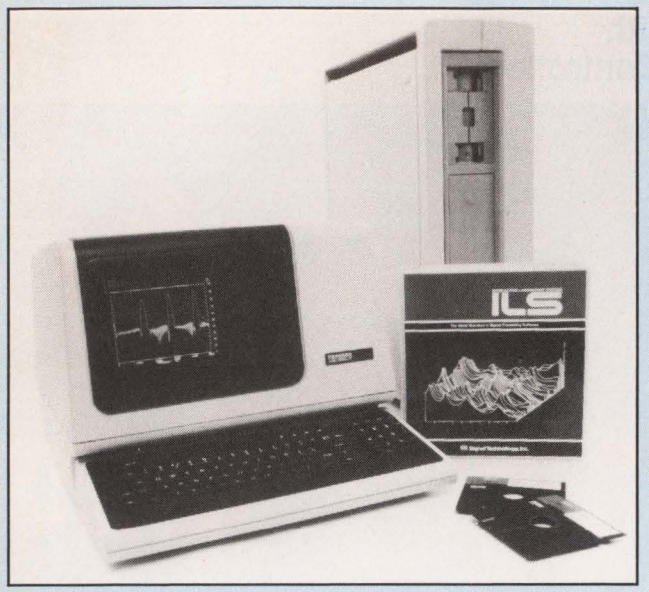

Figure 2: Signal Technology's Workstation.

Unibus. The product area that may benefit most from this decision may be the design workstation. A whole new market has been opened up for products that already exist, especially in the I/O field.

With the introduction of the RC25, DEC has acknowledged the concept of fixed/removability in their drives as an important one. So too have Andromeda Systems (Canoga Park, CA) whose WDC11-H gives the systems integrator the ability to interface the Q-Bus to the DMA Systems micro-magnum 5/5, the WDC11-H will emulate two RL01 units per drive (one fixed, one removable). It can support up to four phsyical drives and up to 42 Mbytes storage capacities using future drives (**Figure 1**).

Signal Technology (Goleta, CA) is a fine example of the new sorts of companies that might emerge due to DEC's recent product introductions. Combining a Micro/PDP-11 with a Sky Computer array processor, the company offers a workstation that can run either the RSX-11M/M Plus operating system or the RT-11 operating system. The DEC system offers 10 Mbytes of storage and the ability to support up to 10 terminals. By packaging their Interactive Laboratory System's (ILS) Signal Processing Software with the DEC PDP-11, Larry Pfiefer, the company's President, claims a cost reduction of 40% over the standard ILS in source form (**Figure 2**).

If DEC's new machines create a new workstation market, then that market will in turn open up new opportunities for DEC compatible terminals, especially ones that can support color graphics. DEC has already announced that they will provide software emulation for the VT100 and Tektronix 4014 on the 11/725, and many prodcuts are already available that will fall right into that market niche. One of these is the CIE (Irvine, CA) CIT-467 that allows simultaneous use of DEC alphanumeric software commands, the Tektronix 4027A color graphics command structure and the Tektronix 4010/4014 emulation mode. In addition the terminal's Tek personality provides rectangle/polygon/circle/arc/pie command functions and is compatible with 4027A graphics primitives.

The most important recent announcement from DEC, allowing other vendors to build CPU boards for the Q-bus (breaking off the exclusive hold it has held for years) coupled with the fact that an announcement of a high speed memory path for the CD interconnect is expected soon, should not only protect the existing market share held by the bus in the 16-bit world until DEC's BI bus arrives, but give existing third parties even greater scope for product design.

age devices typically occur in uneven bursts, the controller must first smooth these irregular bursts before presenting data to the host. The controller also enhances data integrity by validating data transfers, performing error recovery and reporting errors to the host.

At the drive level within the DSA, the actual recording and playback of data occurs. The drives are also responsible for controlling mechanical motions, such as seeking.

Under the DSA, Digital has defined a standard disk interconnect (SDI) from drive to controller. Its properties include radial interconnections that allow the user to disconnect a drive for maintenance and repair without disturbing the operation of other drives in the subsystem. All SDI drives are implemented with standard dual access which allows the user to interconnect a drive to two controllers. Drives monitor their own environment and will shut down if there are any threats to data integrity.

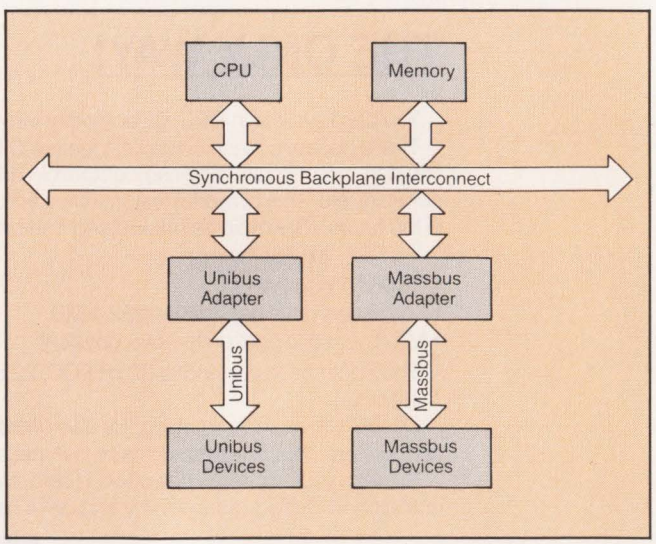

Figure 4: Basic bus configuration of the 11/780.

Until recently, using the Digital Storage Architecture meant being tied exclusively to products from DEC. The complexity of the interface has proven a somewhat difficult task for the DEC-compatible houses to overcome, an issue that has been augmented by the lack of available documentation from DEC itself.

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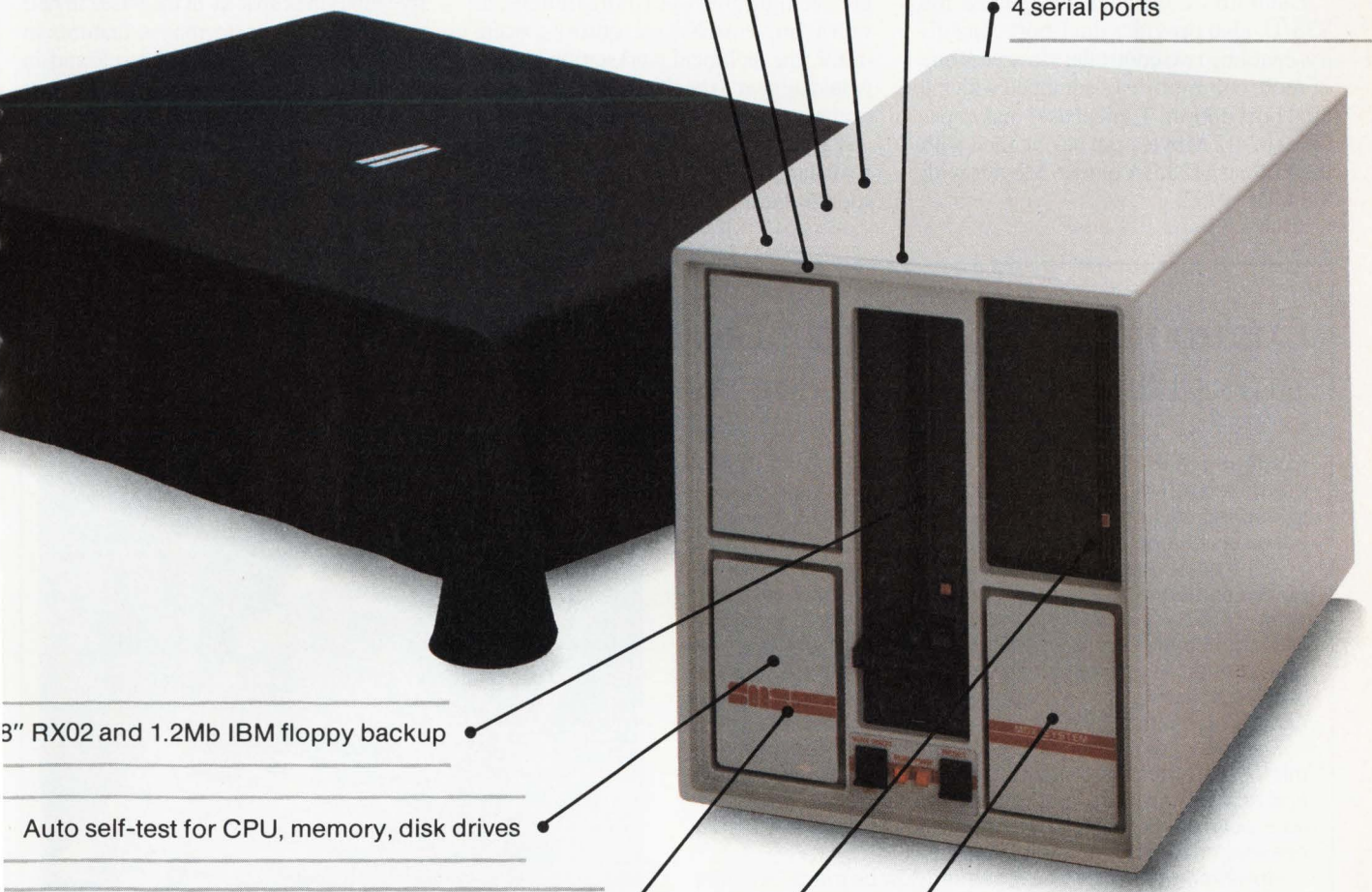

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the first UDA50 compatible product from Dataram (Cranbury, NJ). This PDP-11 Unibus or VAX Unibus controller operates with up to four SMD disks having serial data rates of up to 15 Mbytes per second. The Dataram UDA controller is a packet driven firmware intensive intelligent controller that presents the disk as a set of error free contiguous blocks to the host system. The attached disks can be of any size because the subsystem parameters are passed between the UDA and the host by Digital's Mass Storage Control Protocol.

Dataram's controller, designated the S35/U, also provides dual-port capability, enabling two controllers to access one or more common disks equipped with the dual port option. Typical user disk capacities of 412 Mbytes can be obtained with the Fujitsu M2351A or 68.6 Mbytes with the CDC 9762.

Networking

Last year's announcement of three new VAXs indicates Digital's awareness that the computer industry is moving towards systems environments with distributed networks of computing nodes. Furthermore, it seems evident that some of the powerful systems architectures already described may be brought directly down to these lower cost VAXs.

One product that has already exemplified this is the 11/725, the smallest of Digital's Unibus-based VAX systems. Although the VAX can be used in both single and multiple user configurations, as well as implemented as a network concentrator, the technical workstation market would appear to be the one with the most excitement surrounding it at present.

The 11/725 by itself does not constitute a workstation, but can be configured as such by adding either a black and white VS100 or a display offered by a third party vendor such as Tektronix, Megatek, Lexidata, AED, Ramtek, etc. In addition, Digital's VAX station display services software will include multi-windowing software, allowing the user to perform multiple tasks concurrently on one screen, software emulators for the VT100 and Tektronix 4014, and a human interface that will include a digitizing tablet.

As mentioned earlier, embedded in the VAX 11/725, Digital has packaged the RC25, a 26 Mbyte fixed/26 Mbyte removable disk subsystem that provides five times the capacity of the RL02 in half the space. The performance features in the RC25 closely match those found in the higher end UDA disks. With an average 35ms seek time that can go as low as 20ms due to the seek ordering algorithm implemented by the intelligent resident controller, the RC25 may be offered as a

Communications Processor Design Links DEC Micro With Zilog Peripherals

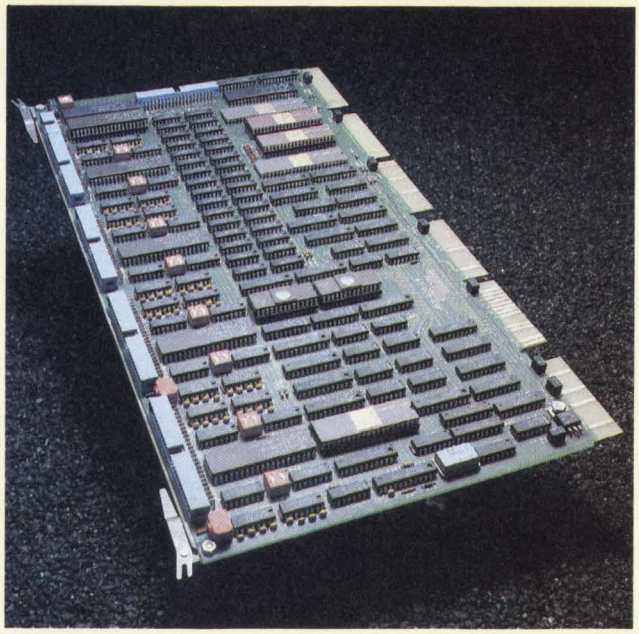
Computer manufacturers have traditionally supported commonplace forms of data communications, providing simple, low-speed asynchronous formats and a few inflexible, higher-speed synchronous protocols at a considerable cost to the user.

In the past, special computer communications problems required solutions that necessitated expensive, custom hardware front-ends and dedicated minicomputers to meet the communication channel's realtime protocol and electrical requirements. Additionally, these types of systems required extensive amounts of special purpose software, usually in assembly or machine languages to obtain the speed necessary.

The recent availability of LSI communications devices and microprocessors have made a significant reduction in the cost and size of hardware required for communications processors, but the inflexibility and high software costs of their predecessors have remained the same.

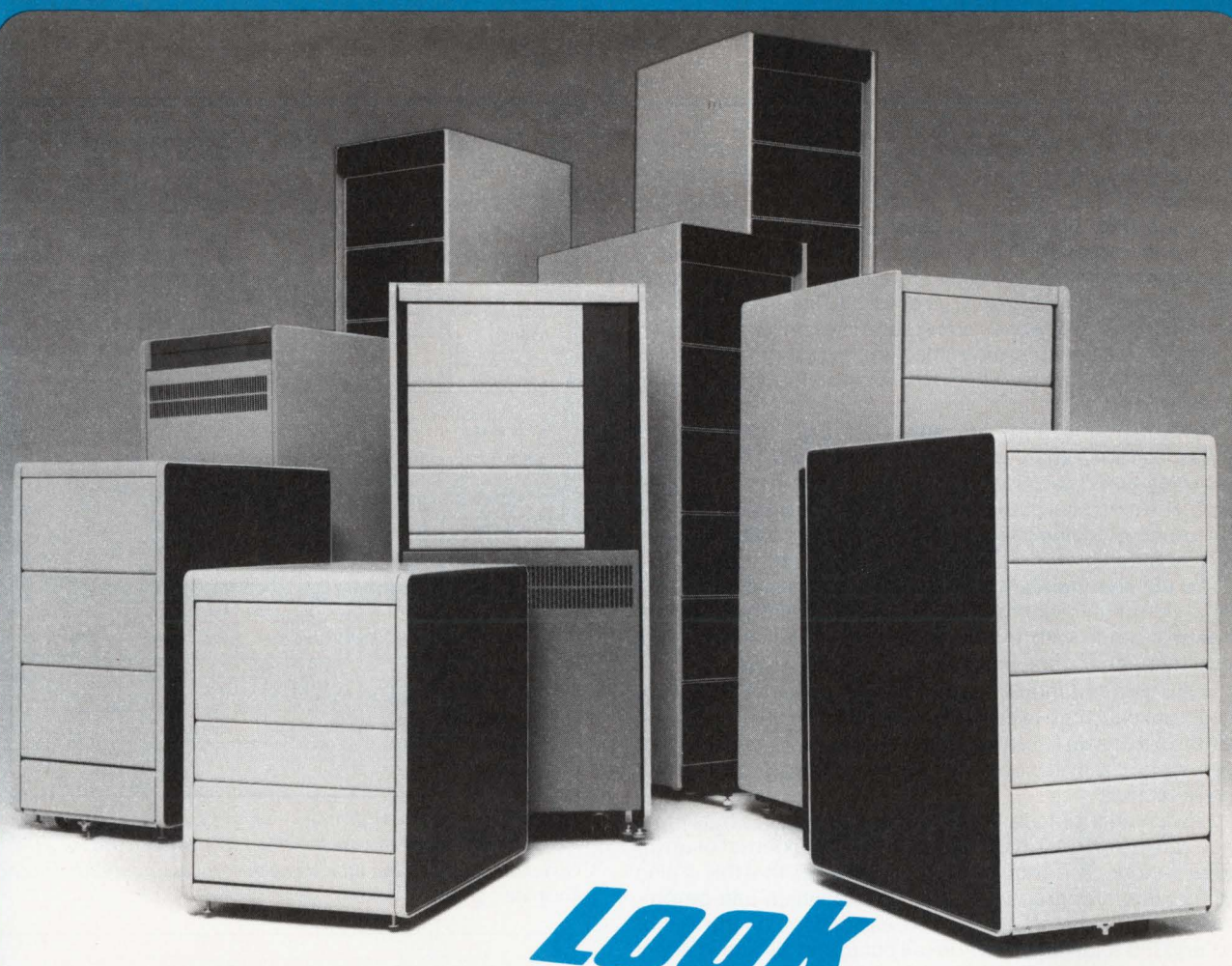
However, significant advances can now be made because of DEC's decision to market their PDP-11 on a chip. Simpact (San Diego, CA) realized that an inexpensive communications processor could be built for DEC processors which would execute the same instruction set as the host computer. Their product, called the ICP1600, combines the DEC Micro/T-11 microprocessor, 256K RAM and LSI and MSI support on a single board, front-end communications processor for PDP-11 or VAX computers with an 18 bit Unibus. The board installs in a general purpose slot within the Unibus' backplane, providing eight programmable communications ports.

The Micro/T-11 is housed in a 40 pin package. The processor executes the PDP-11 instruction set and can address 64 Kbytes of memory. The instruction set compatibility allows the user to migrate existing host-based programs to the ICP1600 with a minimum of reprogramming. Simpact's development system can be used to generate or modify code in a familiar environment with the aid of the host's development tools.



The ICP1600 Intelligent Communications Processor from Simpact is built for DEC processors and executes the same instruction set as the host computer.

Two important design features enhance the Micro/T-11 microprocessor as it is used in the ICP1600. First, the Micro/T-11 bus signals are converted to a Zilog Z-Bus (**Figure 1**). Sec-



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ond, the Micro/T-11's address space is expanded from 16 bits to 22 bits by using a subset of DEC's memory management scheme.

The ICP1600 memory is connected to the Micro/T-11 processor by the Z-Bus. The hardware implementation of memory management does not require any additional time to convert a 16 bit virtual address to a 22 bit physical address. This allows all memory, up to 4 Mbytes, to respond like cache memory, resulting in a faster processing time. Simpact claims that benchmark programs have run 1.5 times faster on the ICP1600 than on the PDP-11/24.

The communications processor has eight on-board full-duplex, serial I/O channels which are independently programmable for either asynchronous or synchronous mode of operation. The electrical outputs are selectable between balanced and unbalanced line characteristics to support protocols such as RS-232C, RS-449, RS-422, RS-423 and MIL-188C.

The I/O channels are designed around four Zilog Z8030 Serial Communications Controller devices which provide two channels, each with independent programming registers, baud rate generators, and modem control signals.

In the asynchronous mode, the channels can support a maximum baud rate of up to 38.4KBPS. Character frames can be from 5 to 8 data bits in length with 1, 1½, or 2 stop bits. Odd, even, or no parity is supported along with break generation and detection.

In synchronous mode, the channels can support a maximum baud rate of up to 400KBPS using either an external or an internal data clock. It should be noted, however, that this is also the maximum aggregate character rate which can be processed by the Micro/T-11. The processing load on the Micro/T-11 and the total data rate from all concurrently active serial channels must be considered when determining the maximum baud rate which is feasible for a specific application.

Both bit and byte protocols are supported within the synchronous mode. Monosynch (one synch character of 6 or 8 bits), Bisynch (two synch characters of 6 to 8 bits) or External Synch modes are supported under byte oriented protocols. SDLC/HDLC bit oriented protocols are also supported with flag generation/detection, zero insertion/deletion, I-field residue handling and abort generation detection. Any channel can act as a secondary station in SDLC loop mode. In synchronous mode, error checking can be done automatically by either CRC-16 or CCITT polynomials. The CRC generator and detector can be preset to all ones or all zeros.

Any channel can be programmed to encode and decode in NRZ, NRZI, bi-phase space (FMO) or bi-phase mark (FM1) codes. All on-board channels have modem control signals.

The ICP1600 has an 8 bit parallel I/O port (CIO port B and C) which can be used to connect to peripherals like a printer or IEEE 488 bus instruments. Handshake signals are provided for inter-locked strobed, 3-wire or pulsed operation. The signals are brought to a 16 pin ribbon cable connector and are low power Shottky TTL logic levels. Power (+5 VDC) and ground are also brought to the connector to assist in buffering or conditioning the signals as may be required by the peripheral.

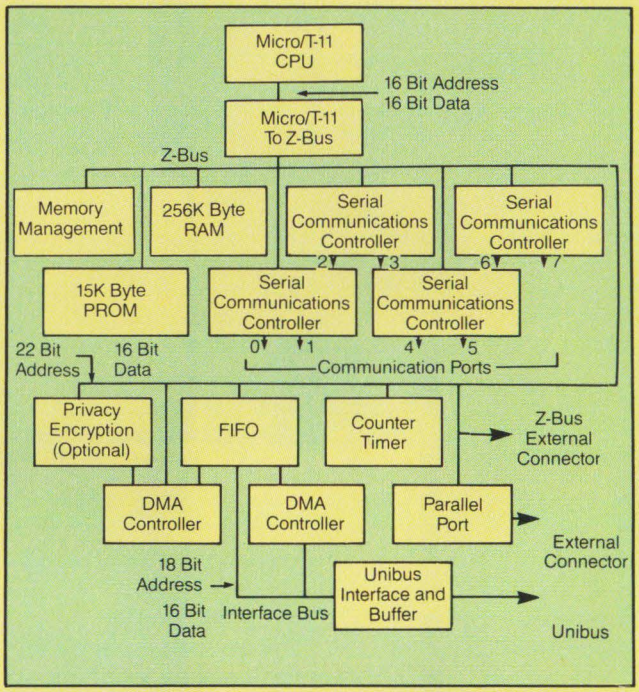

Figure 1: This diagram illustrates a unique feature of Simpact's Communications Processor which is that it combines a Micro/T-11 Processor and Zilog Z-Bus, increasing the processing speed of the host computer.

The 3-wire Handshake is not available in the bi-directional mode, but the port's direction can be changed under software control of the Micro/T-11 allowing bi-directional IEEE 488-type transfers to be made.

For program development, Simpact has a Real-Time Executive (RTX) with device drivers for the ICP1600 and a Sysgen program which creates down-loadable images on the host.

The ICP1600 was designed to support only Unibus computers, but Simpact has taken of DEC's emphasis on the Q-Bus line for new low-end products, such as the MicroVAX 1. Simpact is developing a Q-Bus version of the communications processor which will have shared memory with the host and act as one or more co-processors in the host system. Simpact has also responded to another DEC announcement, the PDP-11/70, by currently developing a code-compatible communications processor for both the Unibus and Q-Bus.

DEC's decision to market the T-11 chip has opened the way for manufacturers such as Simpact to significantly reduce the cost of hardware and software required for communications processors, while increasing their flexibility and processing speed.

— *Coville*

Write 301

stand-alone option for other Digital systems in the near future.

Interestingly, when the 11/725 is configured in a network to larger VAXs, not only can the same application software be run on both machines but the user can dynamically select which system is needed at any time and do so using the same command language and application software on both systems.

Future Directions

Since Digital Equipment is primarily a subsystems house, it is not surprising that the concepts of fault-tolerance, intelligent subsystems and multiprocessing have surfaced in its higher-end products to date. However, the global picture described earlier necessitates that these concepts be found at the board and chip level as well.

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VLSI devices will reduce the size of the VAX.

How this will be achieved is, of course, open to much speculation at present. However, the announcement of the MicroVAX 1, DEC's continued support of the Unibus (now for the high-speed drives as well), the announcement of a VMS operating system that can support multiprocessing, and the disclosures of several chips at the ISSCC aimed towards VLSIing important parts of the VAX 11/780 architecture all point in a common direction – a modular small systems version of the 11/780 that will retain hardware and software portability between high-end machines.

One interesting feature of the VAX 11/780 architecture is the synchronous backplane interconnect (SBI), a data path that links the central processor, the memory subsystem and the hardware adapters provided for the Unibus and Massbus. The SBI provides checked parallel information transfer synchronous with a common system clock period of 200 ns. Using this clock period,. the SBI achieves a maximum information transfer rate of 13.3 Mbits per second.

At the ISSCC in February, Mr. W.N. Johnson from Dec discussed a 5-chip implementation of the VAX 11/780. The design included 1,220,500 transistors and operated with a 200ns microcycle. His colleague, Mr. R. Shuman described a 32-bit bus interface chip that had a bus bandwidth of 13 Mbits per second (the bandwidth of the SBI bus).

Clearly, the VLSIing of these devices is not only a firm indication that existing high end VAXs like the 11/780 will turn up in smaller packages, (like the MicroVAX 1) but that support of these two bus structures may also find their way down to the low end as well. It may be that the industry rumor of the BI bus refers to the backplane interconnect structure of the 11/780 series. □

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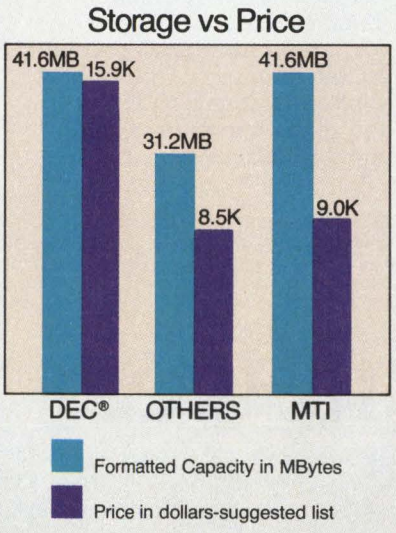

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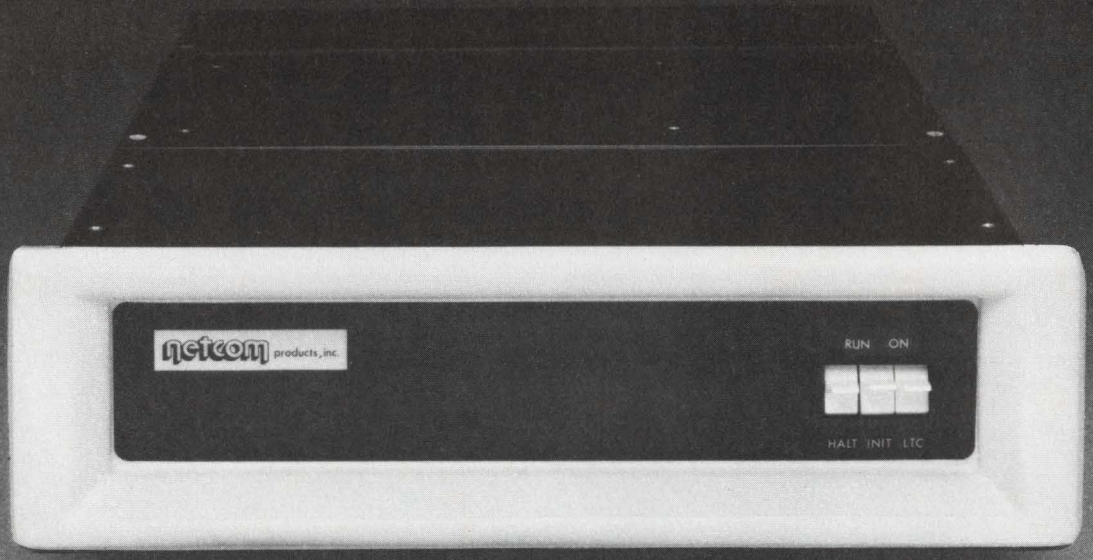

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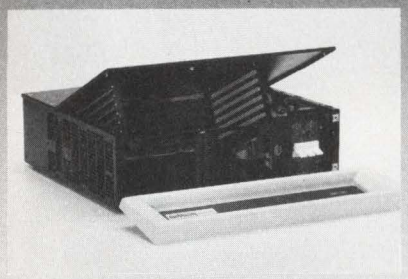

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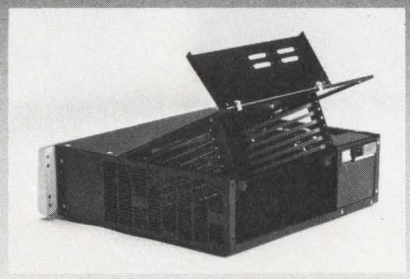

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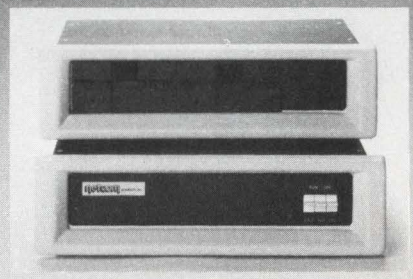

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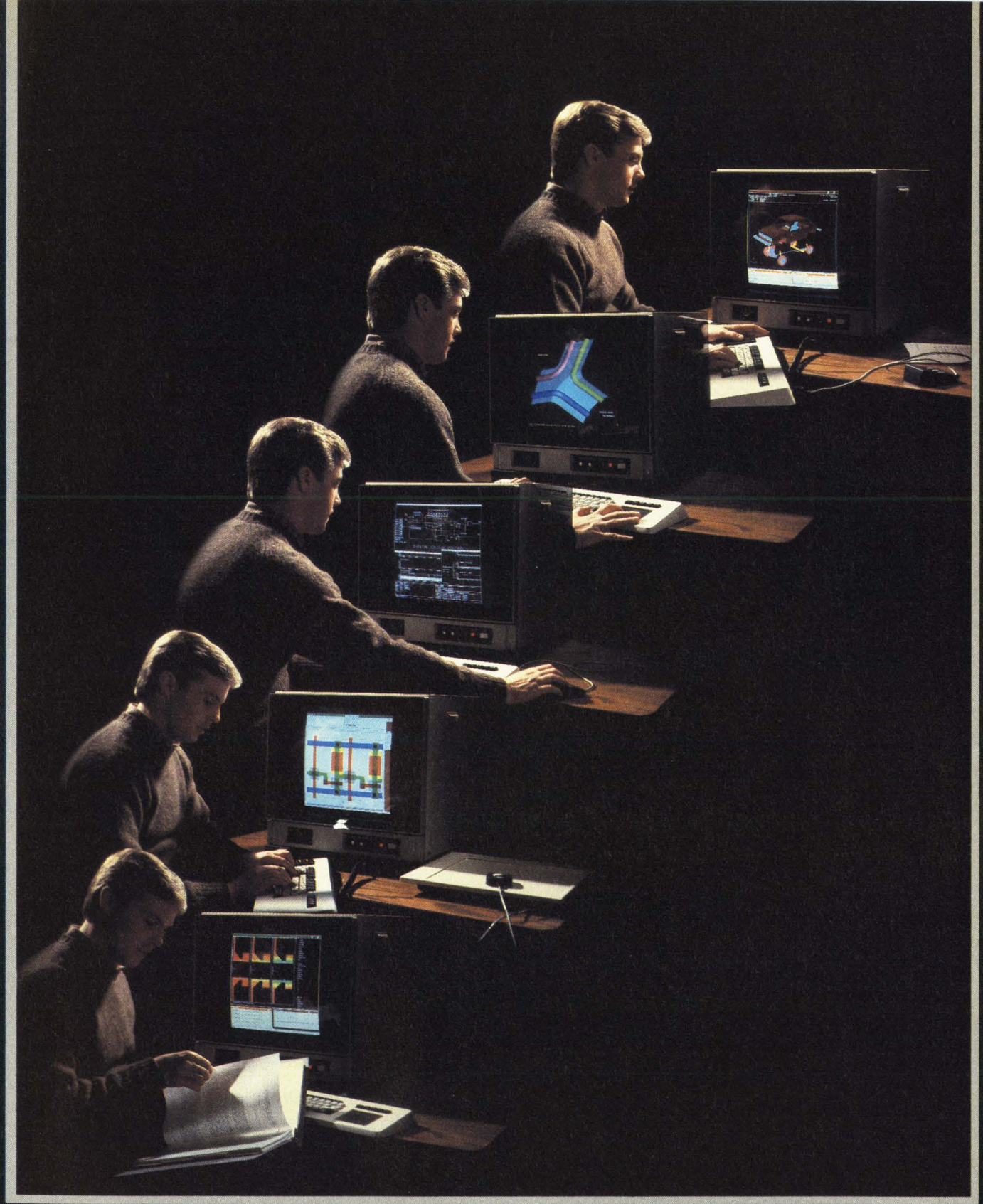


Designer's Guide Series **SMALL SYSTEMS**

The 68000-based Universe 68/05 from Charles River Data was one of the first machines to incorporate cache.

Designer's Guide To Small Systems

by David Wilson, Senior Technical Editor and Andrea Coville, New Products Editor

Small systems optimized for the UNIX environment incorporate a number of innovative design techniques.

Mainframe and minicomputer users have long been frustrated by the lack of a standard operating system. Traditionally, hardware vendors created proprietary designs and operating systems that locked their customers into their particular product line, and then leveraged additional sales off their own expensive software. The large initial investment in a system made switching prohibitive and kept other vendors' software off limits. The advent of UNIX as a standard operating system allows the UNIX user the flexibility to use software developed by many vendors.

The continuing and growing use of UNIX over the past decade demonstrates its usability as a powerful operating system and many improvements and refinements have been made to the system to produce the current version. As the UNIX software and hardware base expands, more applications software will be developed and supported by an increasing number of vendors. Today, it is not only the mainframe and minicomputer manufacturers who are supporting the operating system, but microprocessor based multi-user system vendors as well.

Opening photo, page 57 – Apollo Computer Inc.'s Color Graphics Workstation Computational Node running (lower left to top); Swanson Analysis System's ANSYS®, VLSI Technology's VTI-VLSI Design System, CAE System's CAE-2000 Package, PDA Engineering's PATRAN-G, GE-CAE International's GEOMOD®. Photo Copyright 1983, Steve Grohe, Boston, MA.

Minicomputers and the UNIX operating system were designed to use high-capacity, high-speed disk drives and extensive rewrites into relatively modest amounts of memory in the same manner as mainframes. This extensive disk activity and memory management required solutions to the problems of multi-user multi-tasking environments. Usually the solution was hardware in the form of intelligent disk controllers, channels and complex memory management. UNIX was designed around these hardware solutions. With the drastic drop in memory prices, and the less-expensive but slower Winchester disk drives, microcomputers present a different design environment. Designers of UNIX based microcomputers have to take this into account to present a product with a reasonable price/performance ratio.

UNIX On Microcomputers

Figure 1 shows a traditional microcomputer. A single microprocessor provides the computing power for the whole system. Memory and peripherals are attached to a single system bus. Often, the bus is simply an extension of the microprocessor's own data and address buses. The processor accesses memory over the system bus, fetching instructions and data. I/O devices are also accessed over the bus. Generally, they appear to the microprocessor as special memory locations within its address space. All processing performed by the system, from handling terminal and disk I/O to executing system routines and user programs, is handled by the microprocessor.

When UNIX is implemented on this single processor architecture several key parameters of system performance are degraded, including terminal I/O handling, disk I/O access, communications support, and CPU speed.

Each character typed or displayed on the system causes an interrupt that must be serviced by a terminal drive program. As the number of users rises, the simple task of handling terminal I/O consumes most of the microprocessor's resources.

Sophisticated operating systems are disk intensive. Powerful, hierarchical file systems, a wealth of utility programs and commands, and multi-user memory management are powerful user convenience features that generate many disk accesses as system load increases. If communications are active, protocol handling becomes a CPU intensive and time critical task. Timely handling of communications traffic as it arrives requires CPU interrupts. This in turn decreases performance for other tasks on the system.

Multiple I/O Processors

Raw CPU speed is also an important performance parameter, especially if the CPU is supervising low level I/O activity. For microprocessors with single speeds, the single system bus can also become a performance bottleneck. The net effect of these performance characteristics is a dramatic slowdown of the system's response time as additional tasks and users are added to the system. When the workload increases, or more than a few users are on the system, the single microprocessor chokes on servicing I/O and system overhead, dramatically decreasing the CPU bandwidth available for user task execution.

Instead of relying on a single microprocessor, the Plexus

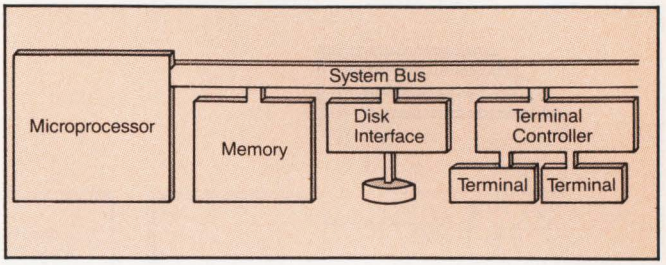


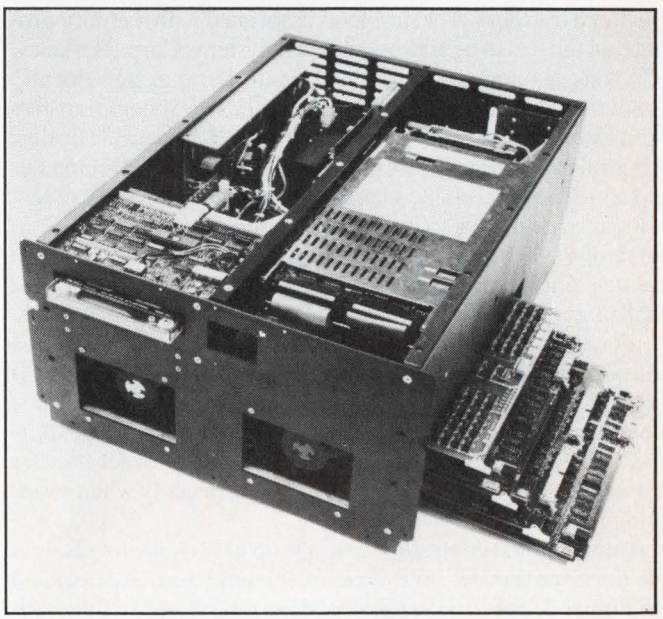
Figure 1: Conventional microcomputer architecture.

Computers' architecture (**Figure 2**) incorporates intelligent I/O processors that offload all I/O processing from the main job processor. In this way the system workload is distributed among several processors that can perform their tasks in parallel. As the number of users grows, more processing power can be added to the system to keep the response times low.

At system startup, the UNIX operating system is loaded into the job processor. Then portions of UNIX are downloaded into each of the I/O processors for execution. The result is a UNIX operating system that is distributed across multiple processors for execution – system management in the job processor and I/O management and drivers in the I/O processors. The architecture actually uses "soft" I/O processors that have their programming instructions in alterable RAM rather than in ROM.

The main system memory is located on a separate memory bus, allowing direct access by the job processor without Multibus handshake overhead. Using a separate memory bus relieves the bottlenecks associated with single bus designs, and is one of the features of newer bus standards such as Multibus II and the VME. These buses will essentially be freed up for strictly I/O related activity.

In the Plexus case, DMA access to main memory is arbitrated with job processor access by dedicated bus arbitration circuitry. The Cadmus 9000 series of distributed UNIX systems also features a proprietary bus (the S-bus) for high speed memory-to-memory transfers, as well as the optimized Q-bus. The Q-bus



The Plexus machine incorporates intelligent I/O processors.

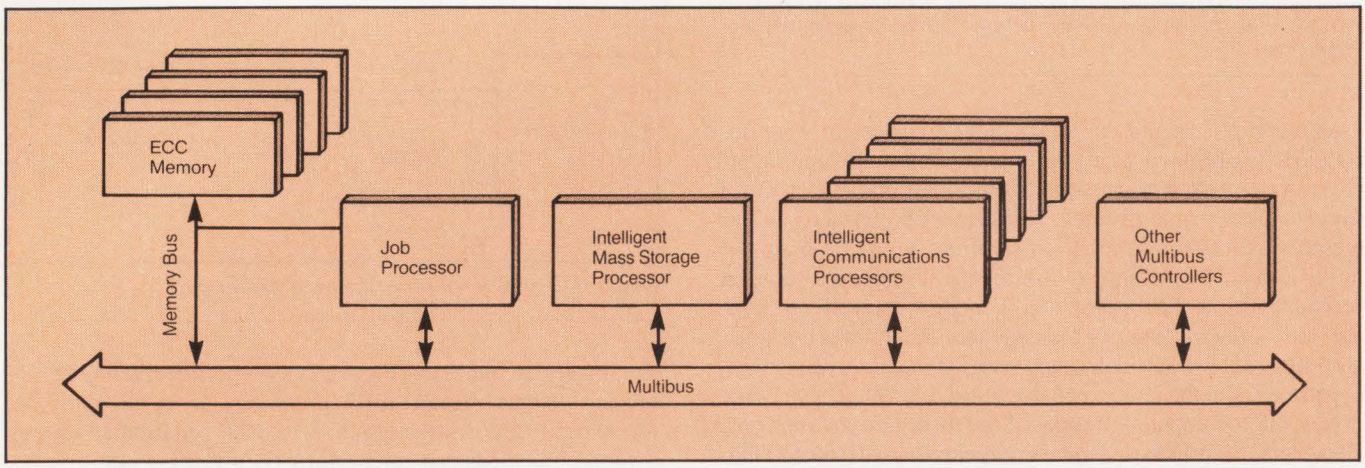


Figure 2: Plexus' multiprocessor architecture.

was chosen over the Multibus in this case due to its cost and physical size, as well as the wide variety of available software and hardware from the large number of Q-bus suppliers.

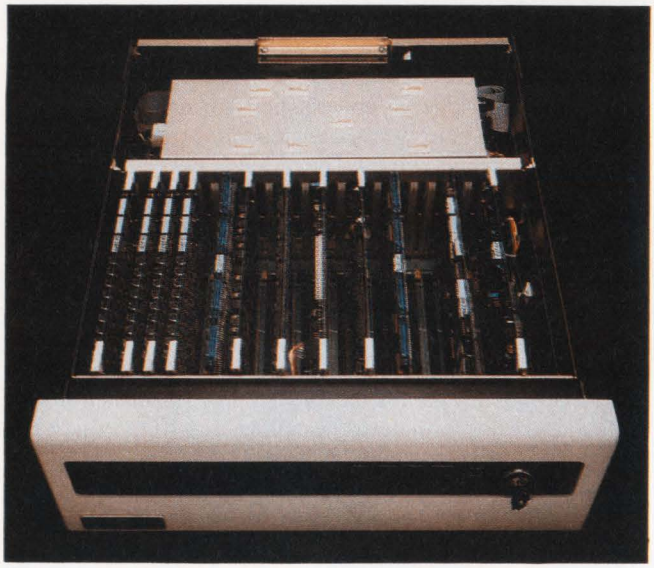
Memory

Perhaps the biggest bottleneck in the UNIX system is the disk subsystem; it consequently presents the greatest opportunity for improvement in system performance. The high demand for the disk subsystem is a result of the operating system, applications, data, and "swapping programs" in and out of the working memory. Since the operating system requires from three to 12 Mbytes of disk space, a floppy system is out of the question for real-time use.

The UNIX system will allow more programs to run concurrently than the physical memory would allow. This is accomplished in the operating system by moving programs in and out of the memory to a special area on the disk called the swap area. This area is composed of contiguous areas, rather than linked areas on the disk. Optimum management of the swap area dictates moving this data into and out of memory in real-time multisectored transfers. The problems associated with memory protection must also be addressed. Dual Systems Corp. (Berkeley, CA) has developed an SMD disk controller that significantly improves disk system throughput for the file system transfers and swapping operations called for in UNIX systems. The disk controller is used in Dual's 68000-based model 83/80 computer system. The controller contains circuitry which enables all sectors on a given disk to be transferred in a single disk rotation, regardless of the position on the track over which the head first settles, and regardless of the order in which the sectors are encountered.

For example, if the controller desires to read sectors three through 20 on a track, and the head first settles (after seeking) in the middle of sector eight, the controller transfers sectors nine through 20 first, and then reads sectors three through eight during the remainder of the revolution. This out-of-order transfer capability results in higher throughput, especially when swapping in UNIX.

Conventional controllers can take up to two disk rotations to do the same transfer (or even more if interleaved) as illustrated in **Figure 3,** due to the additional dead time wasted while waiting for the first wanted sector to appear. Dual's controller uses



Dual Systems 83/80 includes an SMD controller that significantly improves disk system throughput.

this time to read any other wanted sectors which may pass under the head. These out-of-order transfers may be performed during both read and write operations. During a typical swap operation, in which one full track is written, the controller would complete the transfer in essentially one rotation after the head encounters the header of any sector on the track. A conventional controller would take a minimum of one rotation, a maximum of two rotations, and a typical time of one and a half rotations. Hence the controller improves the throughput by typically 33% for such a transfer. Obviously, for less than full track transfers, there would be less improvement, and for isolated single block transfers there would be none.

Operating Speed

The design of any system must provide for the full bandwidth utilization of all critical system resources, such as memory and buses. The surest approach to achieving maximum operating speed is to identify recurring operations, determine their frequency and concentrate the hardware design accordingly. Mem-

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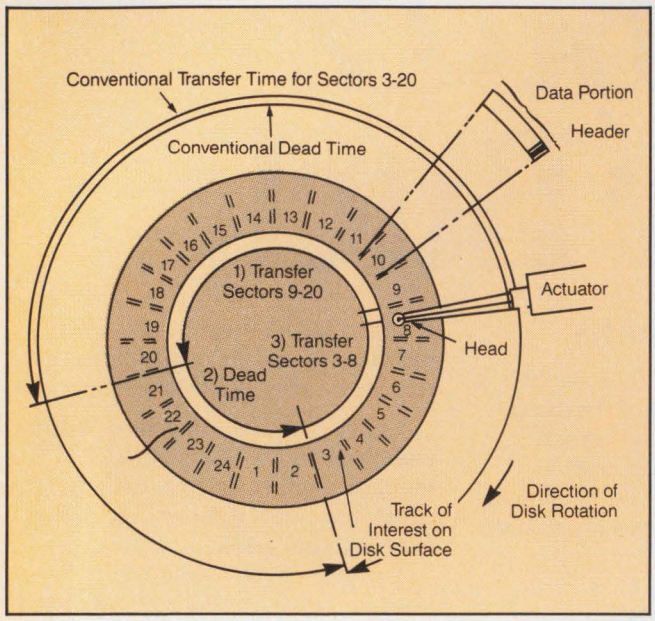


Figure 3: Dual Systems' controller performs out-of-order transfers.

ory access duration, as we have seen, becomes a very significant factor in system throughput. Such techniques as the use of local memory and memory caches can help alleviate some of the limitations that the system bus may have.

The time spent on accessing off-board memory can seriously degrade fast buses between processors. This is especially true if DMA devices and processors must work with a very slow or a very busy memory because they will retain control of the bus until the memory responds. In these instances, an intermediate FIFO buffer memory can match memory and bus speeds and improve the performance, for it will free the bus for further traffic while the request is being processed by the off-board memory. Indeed, the primary consideration in the design of the Series 2000 machine (**Figure 4**) from Zentec (a XENIX-based computer) was the total latencies involved with reading and writing data to RAM. The actual access times were determined by four factors: the RAM access time, the bus arbitration time, the MMU and the PPU propagation delays and the priority of the bus contender.

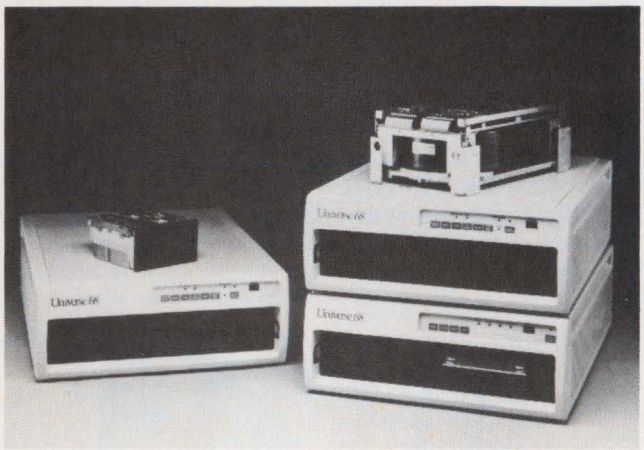
With the RAM and bus bottleneck in mind, Zentec chose the Intel 8086 because of its pipelining capabilities. The usual steps taken by a microprocessor in processing an instruction include fetching an instruction from memory, decoding the instruction, fetching operands, executing the instruction and storing the results in a register or memory. Each of these steps usually requires a machine cycle. The 8086 uses a bus interface unit (BIU) and an execution unit (EU). The BIU prefetches words from memory and stores them in an instruction pipe. Up to six bytes may be stored in the pipe. The EU takes the instructions out of the pipe and executes them asynchronously to the BIU. When the pipe is less than full, the BIU fetches additional instructions, independent of the EU. This pipelining can significantly increase the overall processing speed and RAM access times.

In addition, the 8086 need not wait for a fetch to start executing. Allowing instructions to be prefetched and decoded, minimizing the delay involved in receiving instructions from memory is the reason why the designers of the NS16032 chose to incorporate an 8-byte FIFO queue. Consequently, when the CPU is running sequential instructions with a few branches, the system is less sensitive to what is happening in memory because the next instruction is always available.

If memory is not immediately available and the CPU must therefore enter a memory access wait state, the 16032 may either continue processing its available data or fetch a new instruction from the internal queue. Overall speed is improved with this prefetch mode because it minimizes the number of times the CPU has to come to a complete halt to wait for instructions or data to be fetched from memory.

High-Speed Caches

Designers can dramatically increase system operating speed by dedicating a high-speed cache memory to the exclusive use of the local CPU. High-speed caches should be at least fast enough for no processor waits to be required. With software optimization, the program will run from cache most of the time, possibly



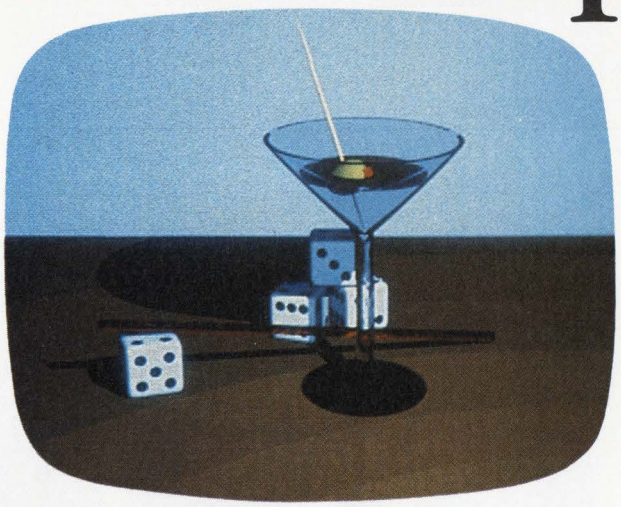
The Universe 68/35 (left) and the 68/67 (right) from Charles River Data use high-performance large capacity Winchester drives.

making CPU speed many times faster than when the program runs from main memory alone. Good small cache designs can result in upwards of 90% utilization during normal program routines. When each CPU in a system is equipped with its own cache, high system speeds can be achieved even though the memories and the buses are slow in comparison with the CPU.

Charles River Data Systems was one of the first manufacturers of microprocessor-based computers to incorporate cache in its design (**Figure 5**). The Universe 68/05 cache interfaces the 32-bit Motorola VERSAbus to the 16-bit data pin structure of the 68000. Cache hits are detected by indexing an array of high-order physical address bits with the low-order address bits, and then comparing them to the high-order bits of the address register. A single-bit test then ensures that the cache entry was not invalidated by a DMA write operation.

Of importance again in this design was the use of a 68000 I/O processor that manages synchronous and asynchronous devices, parallel printers, and other character oriented devices. The I/O processor also includes 4 Kbytes of local dedicated RAM for I/O programming and character buffering. The communications subsystem offloads interactive terminal activity from the central processor and system bus.

We were going to compare Vectrix graphics to IBM's. Unfortunately, there is no comparison.



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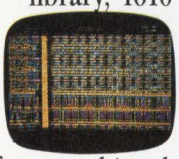

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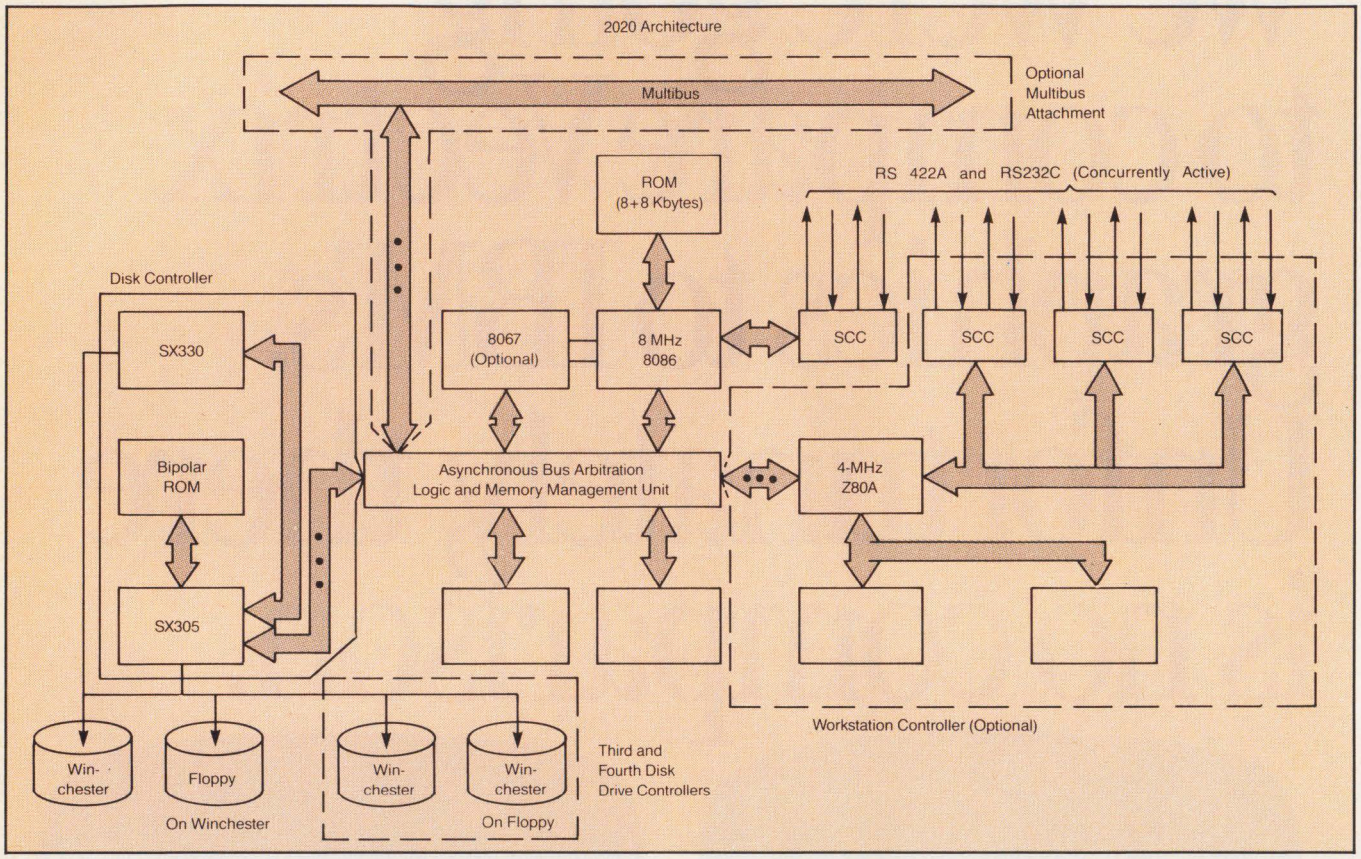

Figure 4: The heart of the Zentec 2020 machine.

Compatible Software

Many manufacturers, responding to the popularity of the UNIX operating system, offer compatible software environments. Apollo Computer, for example, has developed AUX, a UNIX System III-compatible software environment with Berkeley 4.2 enhancements. In weighing the costs and benefits of supporting each UNIX feature, Apollo tried whenever possible to justify implementation. For those features the company did implement, the goal was to provide behavior identical to UNIX. For example, the AUX unlink call does not delete a file until the last process holding the file open closes it. Any features that are only partially supported, or not supported at all, were felt to be functions seldom used by UNIX programs or whose absence detracted very little from the usefulness of AUX.

For example, the link system call is not supported. Instead of UNIX-style "hard" links, AUX supports symbolic, or "soft" links. A soft link, rather than pointing directly to an object, points to a pathname. When the naming server encounters a soft link, it automatically inserts the specified pathname in place of the link component and continues its search. Unlike a hard link, a soft link can span physical volumes and can never refer to an out of date version of an object. At the call level, Apollo found that no more than half a dozen UNIX programs used the link system calls. When link was used, it was either called to rename

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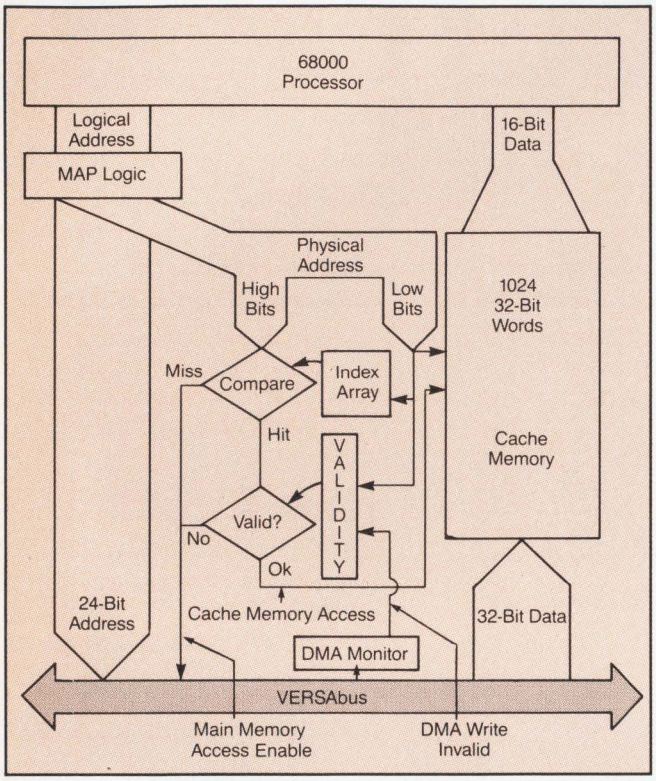

Figure 5: The Universe 68/05 cache.

The Intellimac system will support UNIX and ADA, which the company feels is a superior environment.

a file before an unlink call or used as part of a lock routine. To satisfy the first condition, Apollo added a rename routine; for the second, a lock routine was added that user programs can call.

Apollo found it difficult or impossible to implement UNIX features that violate principles of abstraction and information hiding. For example, the Domain system does not allow programs to read system data structures directly; programs call system services to obtain the needed information. The company concentrated on supporting the UNIX user and program environments and decided not to implement the administrative and operational environments. For example, the acct. system call was not implemented. This records process execution statistics such as CPU time used, the name of the program and so on.

Some of the changes made correct bugs. Some UNIX programs, for instance, carelessly reference through nil pointers; in a Domain process, user programs cannot read location zero. A few programs depend on automatic variables having an initial value of zero. Still others contain machine dependent code that fails on any Motorola 68000-based system. Although Intellimac (Rockville, MD) also supports UNIX (Version 7 now and System 5 in the Spring) on its 68000-based computer line, (**Figure 6**), it is not alone in thinking that superior capabilities and increased programmer productivity can be realized from a different environment.

In Intellimac's case that environment is Ada, and the company is currently developing and testing a level 0 operating system to support the company's real time Ada compiler and to support parallel processing operations. This multi-tasking system, designated the Intellimac Parallel Executive is primarily intended for use with the Ada programming language. It is designed to

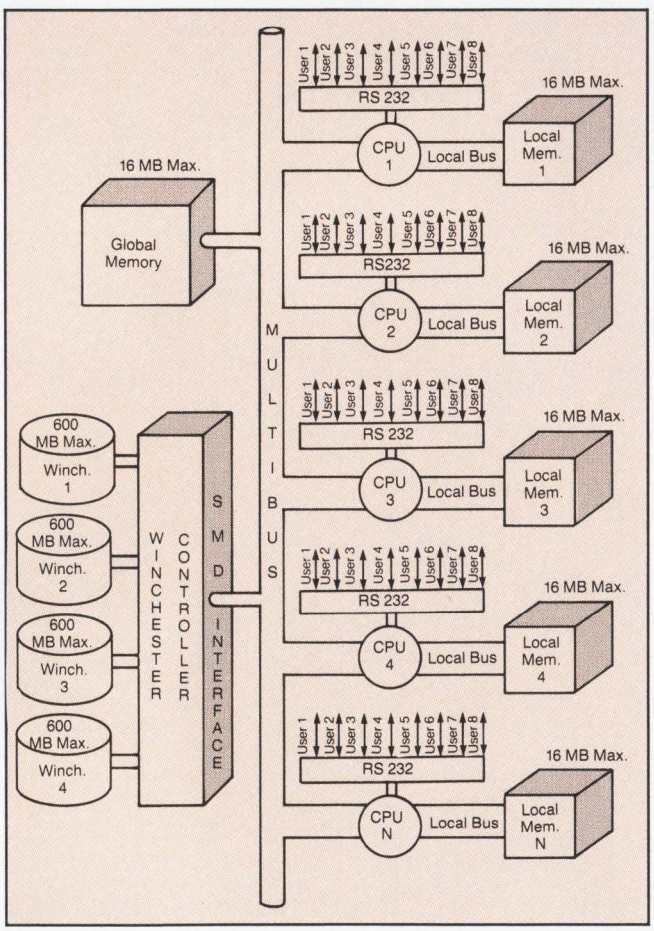

Figure 6: Intellimac's multiprocessor architecture.

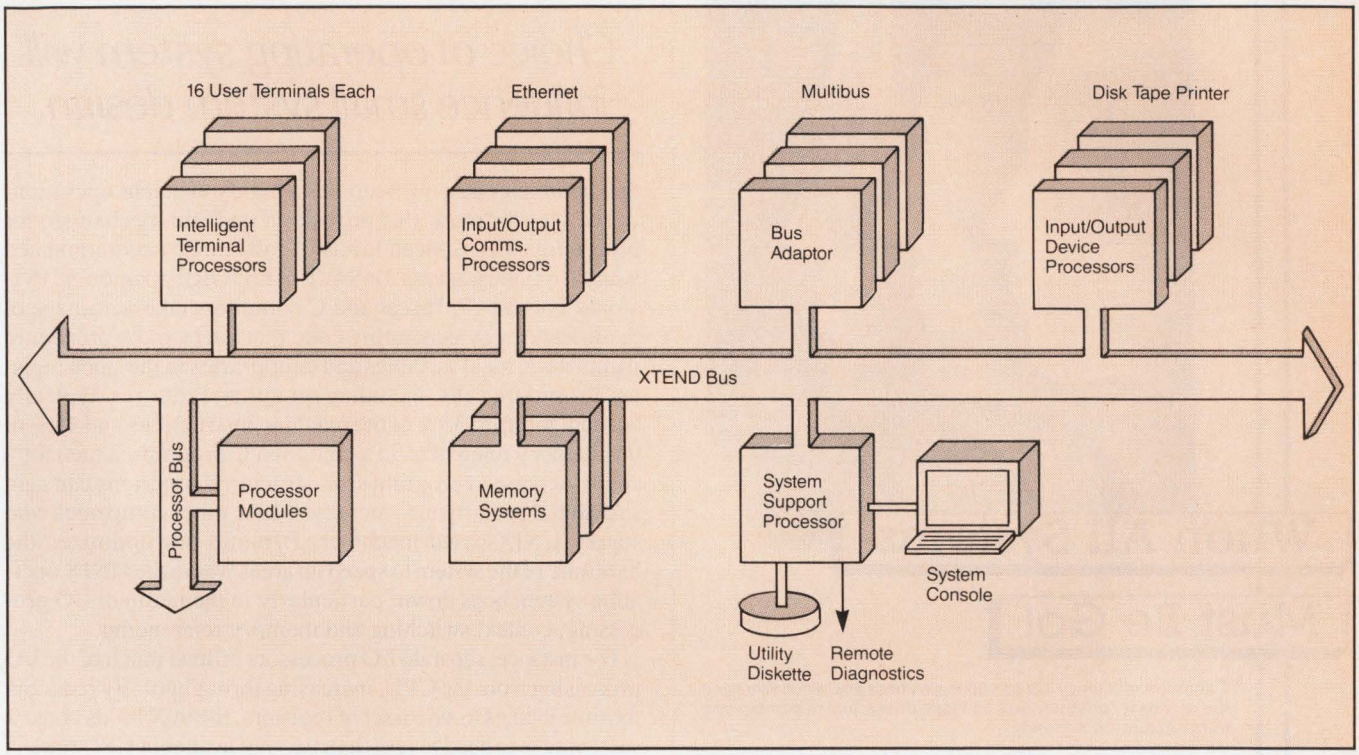

Figure 7: Pyramid Technologies 90X superminicomputer uses RIC architecture.

work with one or more processor systems running on the same bus. The company feels that this approach to system software in the Ada parallel processing environment is the best way to prepare for the coming fifth-generation of non-Von Neumann types of computer architectures. If future generations of computer systems employ operating systems other than UNIX, then they may also employ radically different sorts of processor hardware. For the near future, however, it would appear that the large existing UNIX base may slow these developments, and it is likely that one will continue to see hardware configurations optimized for the UNIX environments. In the short term, small systems will continue to emulate the design principles used in their larger brothers, the minis and mainframes. Today it is still useful to look at developments at the high end to appreciate what one day may be found in less expensive machines.

It has been demonstrated, for example, in many leading computer science institutions that the performance of complex instruction set computers can be surpassed by reduced instruction set designs in high level language environments. To improve performance at the high end, newer superminicomputers, such as Pyramid Technologies' 90X (**Figure 7**) have employed such techniques, and it will not be too long until such designs may be found in lower cost machines. Pyramid's 90X uses RISC research as the basis for its register-intensive architecture. The instruction set is designed for fast execution of the most common high-level language constructs. In most cases, operands are contained in registers, so that memory references are minimized. The computer uses 528 registers, each with 32 bits, implemented in stack form with 16 levels of 32 registers each, plus 16 global registers. A register window makes a subset of the registers at each stack level accessible to the next level, so

Choice of operating system will influence small system design.

that parameter passing becomes a highly efficient operation.

The register stack also provides a uniform mechanism for procedure calls. Sixteen levels of call can be accommodated without memory access for SAVE-RESTORE operations. Pyramid's Fortran 77, Pascal and C compilers take advantage of these features by generating code that keeps most procedure parameters, local variables and temporaries in the stack register. Procedure calls, including set ups and restores, typically account for up to 33% of the machine instructions and 45% of the memory references in a compiled C program. Thus, for a slight increase in program size, structured programs can gain substantial performance increases. Like other companies who supply UNIX-based machines, Pyramid has optimized the hardware of the system to speed up areas where the UNIX operating system bogs down, particularly in the realm of I/O processing, context switching and memory referencing.

For instance, separate I/O processors offload much of the I/O processing from the CPU, increasing throughput. By reducing the time it takes to save a set of registers, the 90X holds context switching overhead to less than 0.6% of available CPU time in a fully loaded system. The major components (processor, memory, I/O processors, systems support processors) communicate with each other and transfer data over a proprietary synchronous bus. The XTEND bus consists of a full 32-bit data path and a 32 Mbyte/second bandwidth. On the bus, I/O requests are standardized through the use of the intelligent I/O processors which act on message-based I/O commands. In addition to reducing CPU overhead, the exclusive use of message-based I/O and IOPs in the system allows future expansion by giving additional symmetric or asymmetric CPUs the ability to share memory and peripherals in a tightly coupled fashion. The XTEND bus also accepts industry standard Multibus controllers and peripherals via a microprocessor-based channel adapter.

Conclusion

The designer of next-generation machines will not only need to be aware of the latest 32-bit microprocessors and support devices available from the semiconductor houses but will need a greater appreciation of what is available to him in terms of custom and semicustom work in order to optimize the performance of his system even more. Features such as tightly coupled processors, I/O processing and caching will play an important role, as will the next generation of bus structures. Interestingly, some of the features of Multibus II, such as its synchronous nature, high bandwidth and message passing support may become some of the leading influences in the design of lower-cost increased performance systems. □

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Local Area Networking Becomes A Standard Feature

by Julie Pingry, Editor

Over the next several years, no single network medium, access method or set of protocols will be "the standard." There are not only several established proprietary networks that will remain popular, but several standard network specifications either just out of IEEE standards committee, nearly final or taking shape.

For the past couple of years, LANs have been the focus of interest and intense efforts on the part of many communications and computing equipment manufacturers. The larger companies and coalitions may once have envisioned their particular networking scheme would dominate and even replace others. But as networking develops, the desirability of various schemes is apparent.

Local area networks have been available for some time now, both from LAN system vendors such as Network Systems (Brooklyn Park, MN), Ungermann-Bass (Santa Clara, CA) and Sytek (Mountain View, CA), and built into a few popular workstations, notably Datapoint (San Antonio, TX) and Apollo (Chelmsford, MA). And there are thousands of networks in operation now, tying like and unlike machines together.

The use of microprocessors in devices once totally dependent on a host computer for processing power and the proliferation of personal computers as individual workstations have made transparent virtual circuit communications between a variety of devices extremely advantageous. Although most of the LANs installed now may be linking like devices or devices from one manufacturer (like DECnet or Wangnet), the main thrust of local area networking over the next few years will be the heterogeneous network.

Standards

As with so many aspects of technology, the interoperability of equipment from various manufacturers requires adopting standards. In the US, the IEEE 802 committee has been a driving force in local networking standards. Newly adopted IEEE standards for networks operating from one to 20 Mbits/sec include the 802.3 CSMA/CD (Carrier Sense Multiple Access/Collision Detection) bus, the 802.4 token passing bus and the 802.5 token ring standards. The 802.3 was the first adopted, and it follows the Ethernet specification originated by DEC, Intel and Xerox closely. The token bus is also final; token ring has been the target of IBM's efforts, and has been several months behind in finalization. The 802.1 and 802.2 Standards apply to all of the configurations (**Figure 1**) and has been several months behind in finalization.

The feasibility of silicon implementations of network controllers and components, of course, depends very heavily on the semiconductor firm's assurance that the design will be stable and usable over a long period of time, so that quantity production can be undertaken. Standards are, thus, essential to the development of network chip sets that allow costs and size to drop. The adoption of the 802.3 standard was accompanied by the announcement of several VLSI LAN controller chips to approximate the spec.

802.3 Ethernet chips and token passing controller chips are available, though newer token passing controllers will undoubtedly appear around mid-year to meet the IBM/TI specs. These chips and the physical links provide through level 2 of the ISO Open Systems interconnect model (OSI) (**Figure 2**).

The main obstacle left to transparent networking is upper level protocol software and standards. Several firms are actively working on protocols through level 4, and a few major network software systems are documented through all seven layers.

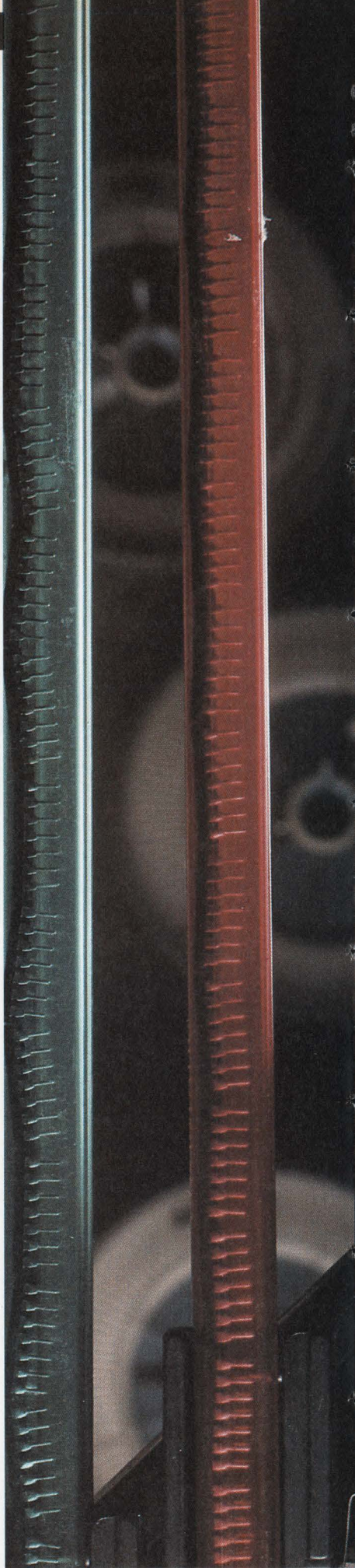

Photo courtesy Data Communications Associates, Norcross, GA

VLSI controllers and high-level software will allow a LANs to link hundreds of devices, from mainframes to PCs, terminals and peripherals, as though directly connected.

One performance difference between the current implementation of these standards, at a raw data rate of 10 Mbits/sec, is a factor of the access method. CSMA/CD (carrier sense multiple access with collision detection), as the name implies, senses the signal on the LAN bus and a node transmits whenever it is ready; since it can sense when it has collided with another node's transmission, it will retry, or contend, as C & D in **Figure 3**. This scheme is ideal for networks that are used relatively infrequently, but may have large files to transfer. A token passing scheme, on the other hand, passes permission to transmit packets to nodes in the ring on a regular schedule; this deterministic method assures each node that it

CSMA/CD and token passing are combined for varying network load requirements on Applitek's UniLAN system.

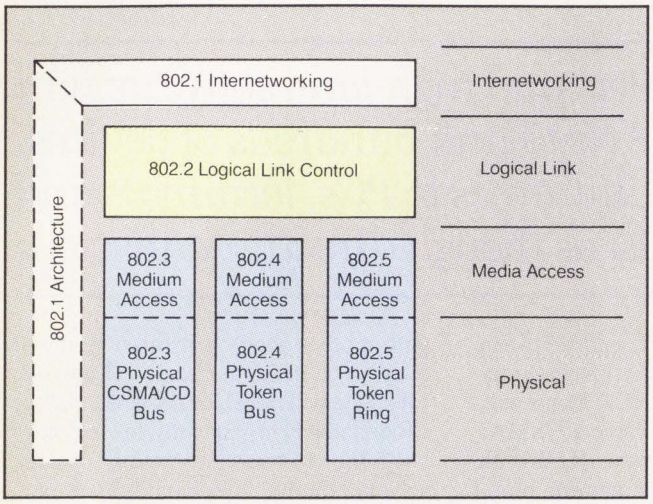

Figure 1: The 802 committee of the IEEE has defined five standards for local area networks; three different access methods and topologies are included.

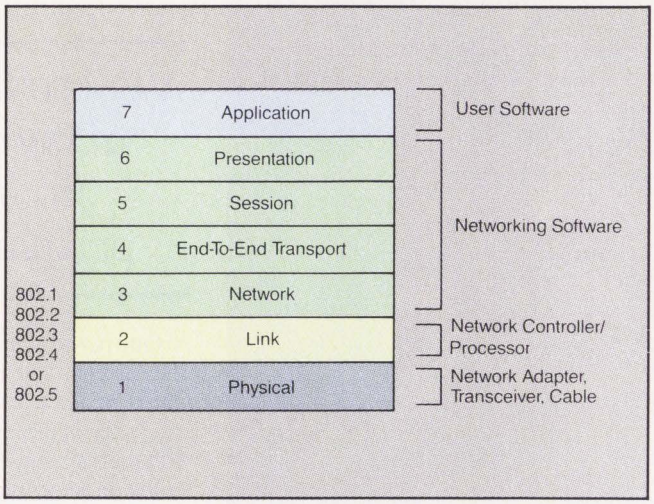

Figure 2: ISO Open Systems Interconnect (OSI) reference model for local area network protocols, and the relationship of the IEEE 802 standards to the model.

will be able to transmit within a certain maximum amount of time. In the CSMA portion of **Figure 3**, node D does not get the bus to transmit. This assurance can be crucial to the time-dependent operations prevalent in industrial and process control environments.

Ethernet-type CSMA/CD systems also use more network time to accommodate the collision detection function. Generally, the difference is too small to matter, but a very high speed data transfer, such as a graphic display for CAD/CAM or very high speed memory transfers can be adversely affected by the amount of network space used for the actual networking.

One firm has recently announced a non-standard network offering combining access methods, so that when a network becomes too heavily loaded, nodes are guaranteed access. UniLAN from Applitek (Wakefield, MA) claims true 10 Mbit/sec network throughput, as it switches from contention to guaranteed access for heavy traffic. Though this scheme appears to take advantage of the

Protocol	Raw Data Rate (Mbits/sec)	Manufacturer	Part	Specifications & Features
Ethernet CSMA/CD	10	Seeq	8001	Strict adherence to Ethernet spec. Provides addressing, CRC generation/detection, auto retry, data encasulation.
Ethernet CSMA/CD	10	Fujitsu/ Ungermann-Bass	MB8795A	CMOS 64-pin gate array of Ethernet link layer. 3 8-bit ports for separate transmit, receive and command status channels.
Ethernet			MB502A	Manchester encoder/decoder. 100 MHz bipolar ECL/Schottky chip using digital PLL.
CSMA/CD incl. Ethernet	10	Intel	82586	Ethernet link layer with 24-bit memory addressing with DMA, buffer management, diagnostics; allows non-Ethernet protocols through 0-6 address bytes, HDLC options, 8 or 16-bit data bus; optimized for Intel processors.
Ethernet			82501	Manchester encoder/decoder. Includes watchdog timer, testing and diagnostics.
Ethernet CSMA/CD	10	AMD Mostek	AM7990 MK68590 LANCE	Ethernet link layer with 24-bit memory addressing with DMA, buffer management, diagnostics; usable with several bus structures and processors; designed by DEC.
CSMA/CD	1.25 2.5	Harris	HD-15530B HD-15531B	LSI CMOS Manchester II encoder/decoder for the MIL-STD-1553 bus or other similar bus. 15531B is higher speed and for industrial rather than military use.
ARC	2.5	Standard Microsytems	COM9026	ARCNET link level controller. Packet acknowledgement, address decode, CRC generation/detection, auto network reconfiguration.
Token Passing HDLC	1	Western Digital	WD2840	MOS/LSI token passing controller. Dual DMA, error detection and diagnostics.

Table 1: Networking chips available as of the beginning of 1984 and some features.

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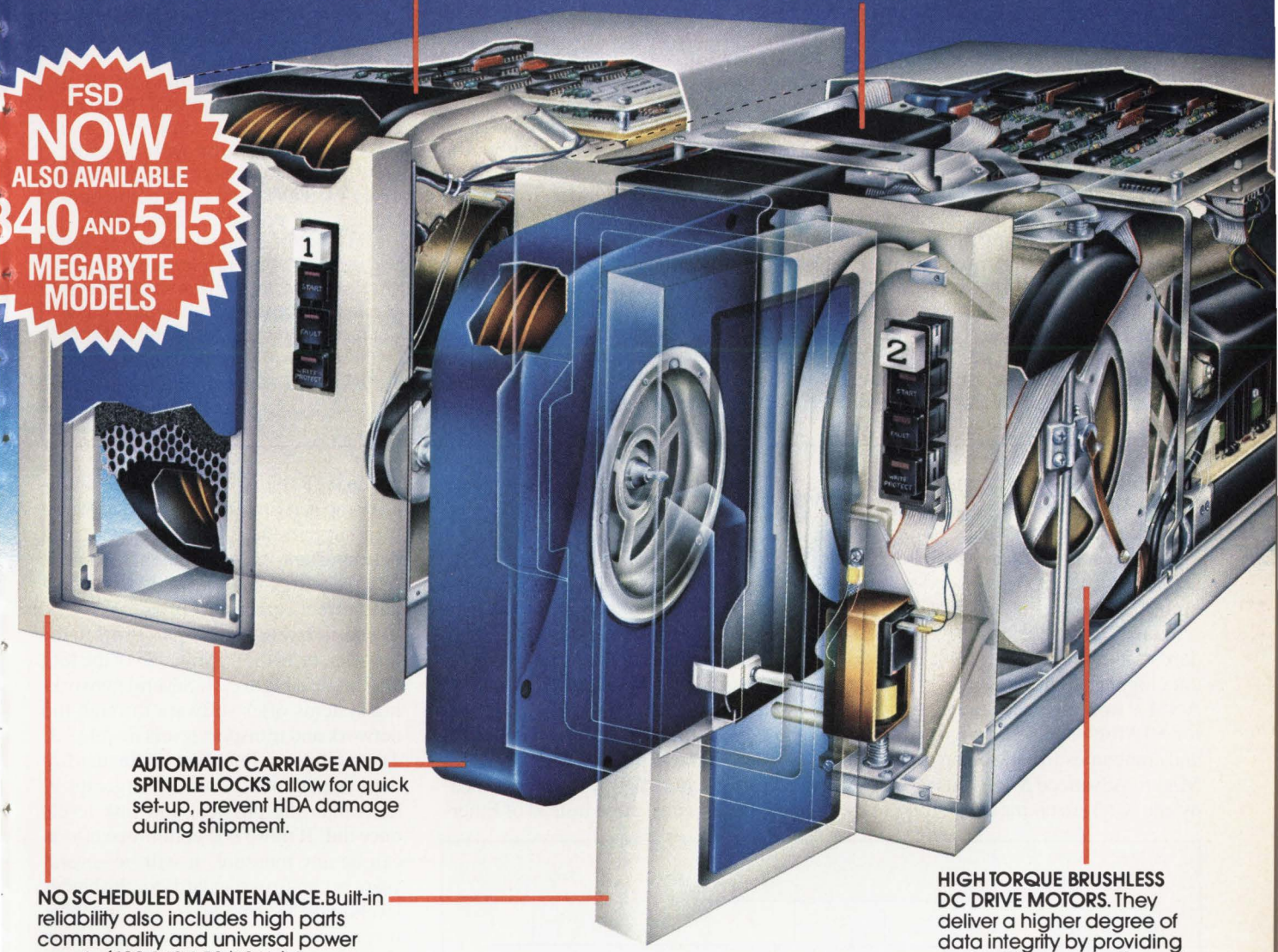

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Networking of applications between products with diverse processors, operating systems and networking hardware is now possible in either XNS or TCP/IP with Version 2.0 of FUSION. Virtual terminal, file transfer, network management and other services are available to users of networks running Network Research's (Los Angeles, CA) FUSION at the application level of either an ARPA TCP/IP or a Xerox XNS Ethernet network. The package's two-part architecture allows network users more than one higher-level protocol simultaneously, as well as allowing those protocols to run on non-Ethernet networks.

The two parts of FUSION are the applications themselves and a network socket manager, on which all of the applications reside. Sockets are the endpoints of network connections; the socket manager performs board-level device interfaces, data and buffer management, queuing, timing and operating system interface. The comprehensive socket base allows applications to be developed simply and to run efficiently. Application-to-application transfers across a network can have a throughput of over 1 Mbit/sec; datagram transfers can be even faster. By using multiple sockets, both TCP/IP and XNS can be used on one device for a gateway.

FUSION currently operates on the 8088 running MS DOS and 8086, 16032, 68000, PDP-11, VAX 750 and VAX 780 UNIX systems. Most popular versions of UNIX are supported, and a package for VMS has been announced, to be available soon. Ethernet networking hardware from four major vendors, soon to be five, can be driven by FUSION, as well as some non-Ethernet hardware, including TTY phone line networks.

Further interoperability is the goal of development at Network Research, according to their President, Howard Gordon. With the socket manager as a device driver in the software system, further applications can be developed with relative ease. Other protocols, processors, operating systems and network controller boards may well be accommodated by FUSION packages in the future, providing choices for upper-level networking.

Write 302

best of both major access methods, there is some debate as to how many applications need the gain in access time more than the standard protocol. Another point is that for truly heavily loaded systems, even 10 Mbit/sec may not be adequate.

As may be expected, there are standards efforts in the works to accommodate higher speed networking, as well. ANSI is working on token ring standards for 50 Mbit/sec and above networking, and companies from Proteon (Waltham, MA) to Advanced Micro Devices (Sunnyvale, CA) are taking active roles in the standards efforts and developing products for high speed networking.

At the other end of the spectrum, for small networks of low speed devices, even the 10 Mbit/sec rate of current token and CSMA systems is overkill. Western Digital's VLSI controller for a 1 Mbit/sec token network uses proprietary protocol, but these 2 to 250 station nets can be linked to standard networks. The proposed Cheapernet or C-net standard is very similar to Ethernet, but operates at 1 Mbit/sec and uses thinner, less expensive RG 59 coax cable instead of Ethernet coax. Rapidly dropping costs of microcomputers and other computing equipment suggests that the C-net standard may be important in environments where a relatively small number of these systems need direct communications.

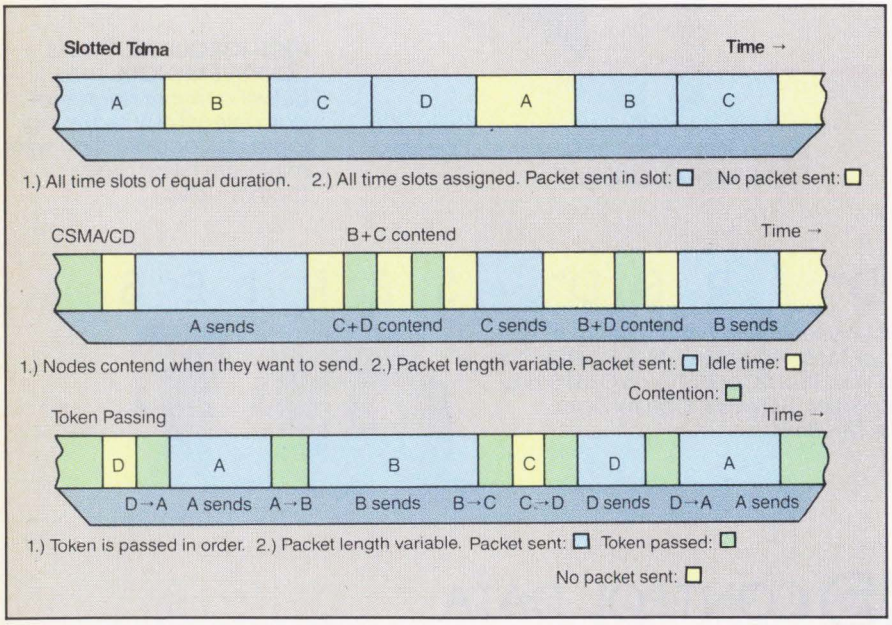

Figure 3: Diagrams comparing CSMA and token passing traffic and overhead; note that node D still has not gained access to the bus in the CSMA example.

The next big standards efforts will, however, be in the upper levels of the ISO OSI model (**Figure 2**). Several networking systems offer software through the network and transport levels (levels 3 & 4), or will soon. But efforts to standardize these upper levels pose even larger problems than the physical and link levels once did. If those 802 committee efforts can be any measure, it will be several years before firm standards for the higher levels of the ISO model are set; and there is some doubt as to whether application level networking will ever be standard.

Still, two protocols are fairly well documented, Xerox's XNS and the Department of Defense TCP/IP (box above); several manufacturers are structuring networks around these or the ISO protocols. Bridge Communications (Cupertino, CA) and ACC (Santa Barbara, CA) are prime examples of companies incorporating XNS at higher levels. Once some standard networking system at the 4th and 6th levels of the ISO model (the 5th, or session level, can be skipped in some cases) is implemented in firmware, almost any device can be integrated on a network in a transparent manner.

VLSI Network Controllers

At this writing, Ethernet controllers and

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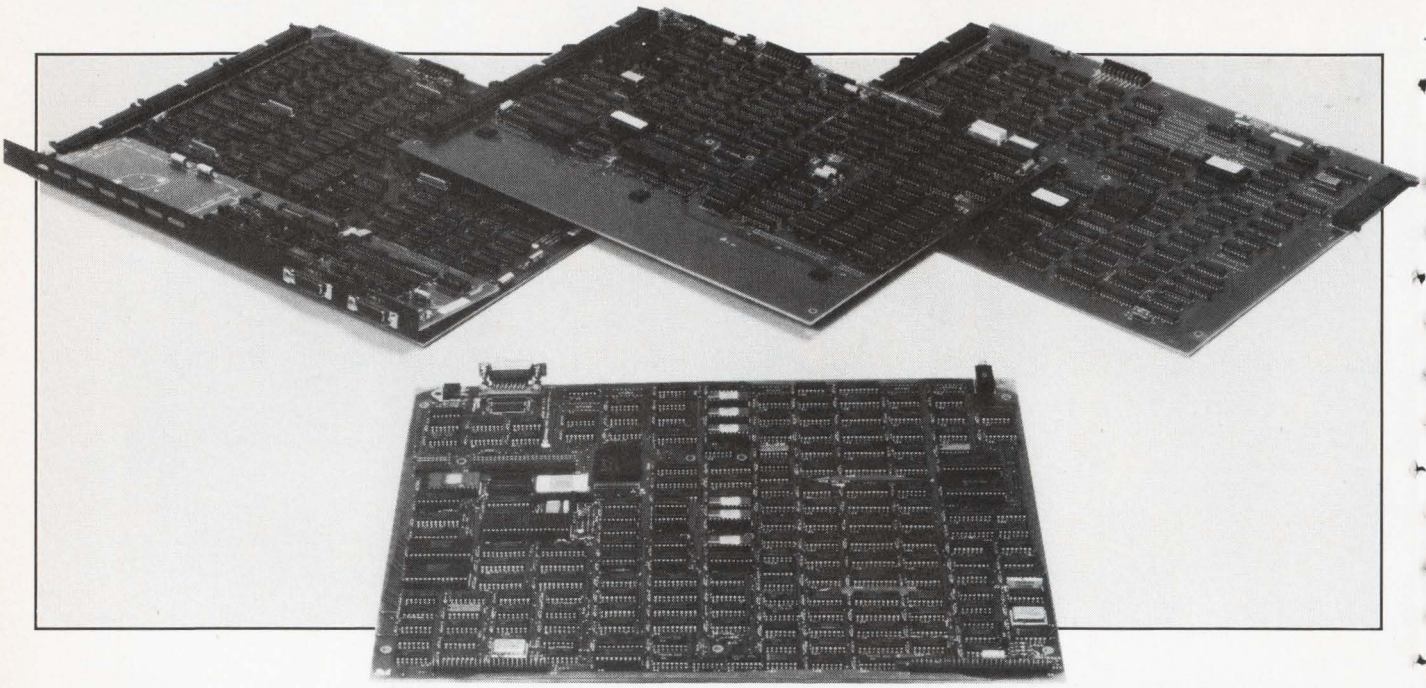

Figure 4: With VLSI, the board in the foreground, Model 150 from Ungermann Bass using Ethernet chips from Fujitsu, can functionally replace the three boards in the background.

encoders/decoders (the Ethernet/IEEE 802.3 spec calls for Manchester encoding) are available as VLSI chips from several sources. There are also token LAN controllers available, although the specifications from IEEE committees are not totally finalized. These chips have all gone through fairly long development cycles, and customers have anxiously awaited shipments, especially on the more highly integrated controllers.

The various Ethernet controller chips and their relative capabilities and specifications are listed in **Table 1**. As can be expected, Intel's network chips are especially well suited to work with the Intel processors, and although 3Com (Mountain View, CA) actually designed the Seeq (San Jose, CA) chip, they were one firm on the list for the first deliveries of the LANCE chip. The LANCE chip was also a joint development effort; this one involved DEC's design and both AMD (Sunnyvale, CA) and Mostek (Carrollton, TX) producing the chips for automatic second-sourcing. The Ethernet controller chips are in initial shipping stages; by virtue of their simple no-DMA designs, Fujitsu (Santa Clara, CA) and Seeq claim greater flexibility and have avoided some of the troublesome complications of initial production. Ungermann-Bass and Fujitsu developed the chip used on the 150 Network Interface Unit that replaces three boards, shown in **Figure 4**.

For Datapoint's ARCnet (Attached Resource Computer), Standard Microsystems (Hauppauge, NY) produce the COM 9026 VLSI 2.5 Mbit/sec token bus controller. Though ARCnet is not a *de jure* standard, Datapoint has offered the system on its equipment for such a long time and the Datapoint devices have been sold in such large quantities, that VLSI has proven practical. Another controller chip for token passing networks is available from Western Digital (Irvine, CA) to control a 1 Mbit/sec LAN. This chip has gone onto a networking board in a WD joint effort with Percom Data (Dallas, TX).

The quantity production of VLSI devices for token passing ring networks, however, will come as soon as the IEEE 802.5, and more to the point, IBM, specifications are complete and final. For this chip, Texas Instruments (Dallas, TX) will manufacture the chip to IBM specifications. And the only clues to the final design of this system are IBM's contributions to the IEEE 802.5 committee discussions and the paper IBM presented at the Telecom '83 show in Geneva. Several semiconductor manufacturers have indicated that they are at the ready to produce chips for the IBM design as soon as it hits the public, offering the same capabilities as TI very soon after that announcement.

As ever with VLSI to replace discrete parts, these chips, especially in conjunction with monolithic encoder/decoders for Ethernet, are driving both costs and sizes for devices providing network capability down dramatically. As other networking standards are established, both at higher and lower speeds and perhaps for totally different architectures, chips will be designed to meet these needs. Perhaps even more significant will be the inclusion of upper level protocols as firmware as they become standard.

Efforts to put network transceivers onto single chips are also underway, but the transceiver is much more difficult to put into silicon. At least one of the Ethernet chip manufacturers hopes to incorporate the encoder/decoder into the controller chip. But the transceiver could not be included into this chip, due to voltage difference. Increasing integration of network functions into monolithic packages will no doubt continue, allowing integration of standard networking functions and interoperability in a variety of computers, terminals and peripherals.

Network Media

The VLSI controllers fulfill the Link or layer 2 of the ISO OSI model; at the first level, the physical connection has been a matter of discussion. As with the access methods, networking manufacturers have

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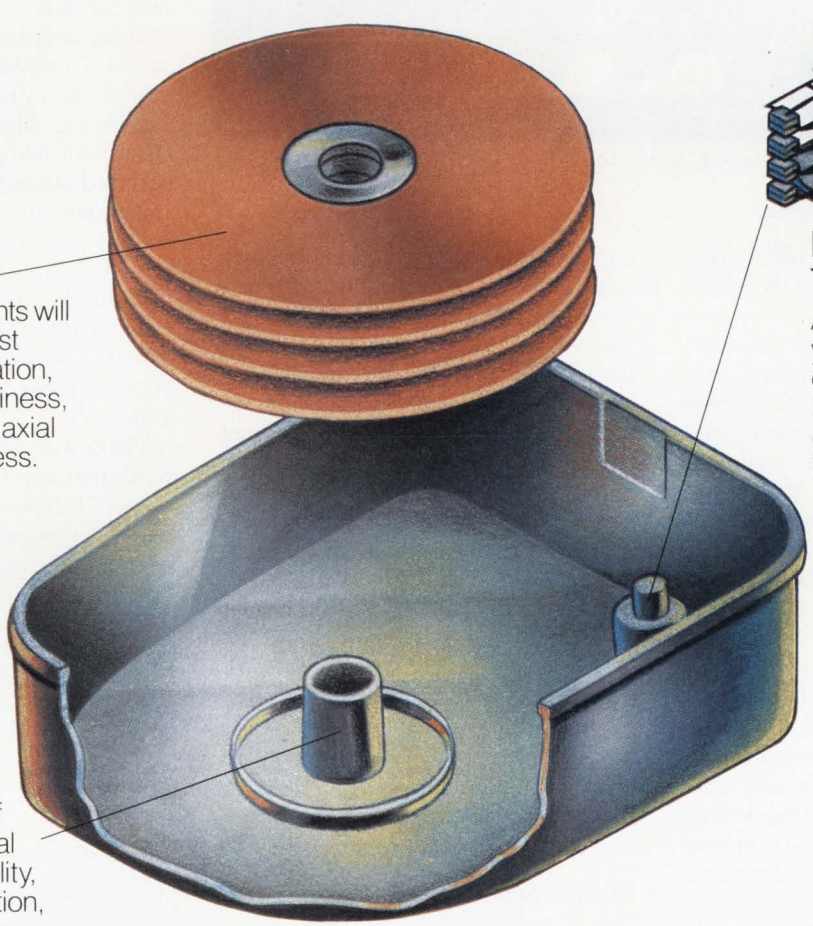

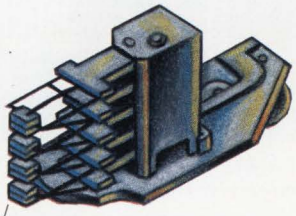

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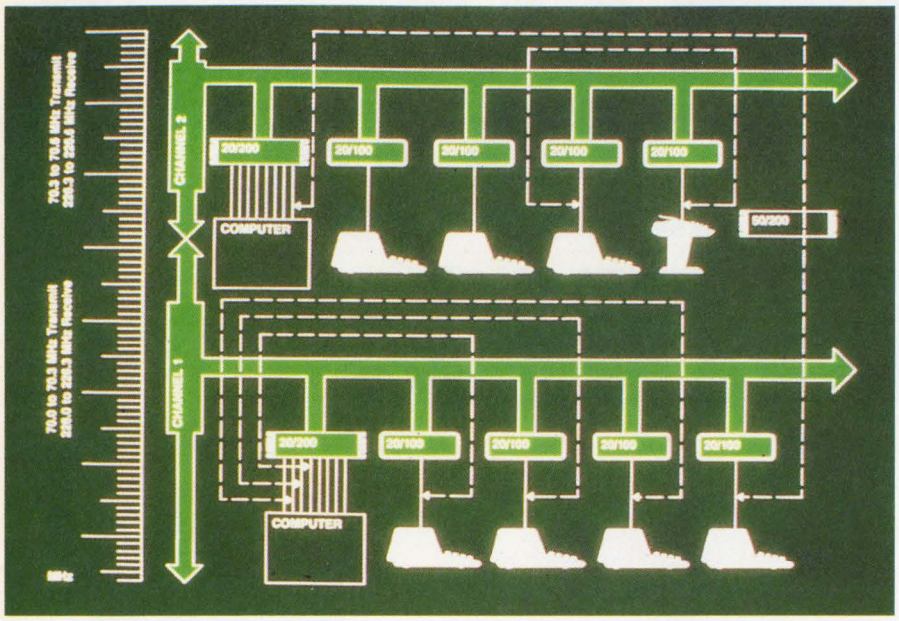

Figure 5: In broadband systems like Sytek's LocalNet 20, the large bandwidth is divided into transmit and receive channels.

agreed that no one medium will be best for every application and that the media will coexist.

Most of the networks available now use baseband coaxial cable as the medium. Broadband systems using CATV cable are useful for very large systems and those for carrying combined signals, especially if video is desired. And several vendors offer fiber optics links, as well.

Although broadband requires analog engineering, the modems and cable are well known and available in quantity due to the cable TV industry. A broadband LAN divides the huge available cable bandwidth into individual channels (**Figure 5**). Sytek, TRW, 3M and others have produced very large networks in broadband cable through the use of multiple channels. A single channel such as that of a baseband system can overload with nodes, damaging access times and accuracy.

Fiber optics is another possible medium for networking. Although not very well suited to bus topologies, since tapping an optical signal causes degradation, fiber optic networks of both ring and bus types have been successfully implemented by making only the logical connection that and keeping the physical topology a star, as in **Figure 6.**

Point-to-point optical links allow high data rates and are especially useful in areas where electrical interference or security are problems. Cadmus' networking scheme is designed for either baseband coax or fiber media. For larger networks, Cadmus interconnects stars in a "snowflake" topology. Equipment for fiber transmission is available at costs that are not exorbitant now. But the environment must demand either high speed transfers, high security or electrical immunity at the moment. The Japanese have installed several sophisticated optical networks, and the experimental network at Xerox PARC (**Figure 6**) may become a product in the not too distant future.

Large suppliers of local area network equipment such as Ungermann-Bass will accommodate any medium in a network, because each application environment will dictate different priorities that can best be met by various topologies, media and access methods.

Interoperability

At this point, because no standard networking software is available above the link level, even networks conforming to the same IEEE standard, such as the 802.3 Ethernet, are not necessarily interoperable. Ethernet implementations from various vendors transferring packets may be of little use now, since the specification only covers the physical and link layers of the ISO OSI model.

The overhead from networking software could rapidly dwarf the access times attributable to the physical and link levels. Streamlining software that will allow any given vendor's machinery to intercommunicate over a transparent local area network will be a task that many firms and computer hardware designers will struggle with for some time to come, no doubt.

Truly transparent networking will be achieved through the higher levels of the ISO OSI model (**Figure 1**). The application layer may always depend on individual machines or environments, but levels 3 (Network) through 6 (Presentation) are levels of networking software, and will need to go through the same standardization process that the past several years has seen for layers 1 and 2.

Since everyone now agrees that several standard networks will coexist, a major need for networking will be bridges and gateways to allow the various standard and established proprietary networks to be linked as though one system. Gateways and bridges are already getting attention and development from most LAN vendors. This is an indication that everyone, including the Ethernet supporters who feel that as the longest-established standard it could take precedence, know that no one networking scheme will dominate universally.

The best documented networking software protocols are the Department of Defense TCP/IP and Xerox's XNS. ISO pro-

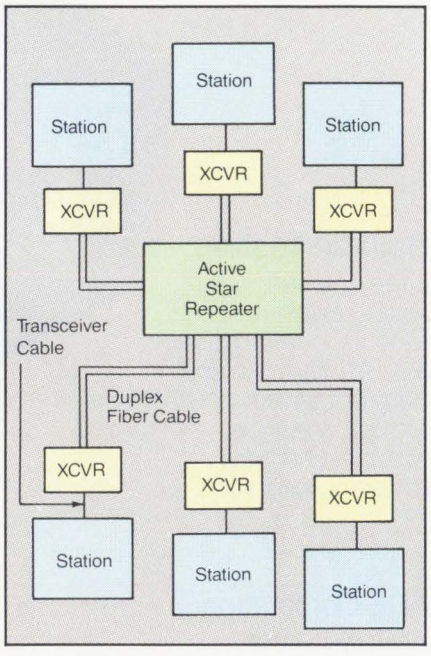

Figure 6: A fiber optic network installed at Xerox's Palo Alto Research Center uses an active star configuration to network office equipment.

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3	1	IDP
2	0	ETHERNET x.25 LEASED LINES
1		

Figure 7: The XNS protocol covers ISO model levels three through seven, providing an immediate solution to some higher level network protocol needs.

Figure 8: The Excelan Nutcracker provides extensive monitoring and control functions by simulating actual network usage.

tocols are also being developed through all of the OSI model layers, but are not yet as well defined; IBM's SNA is not a true LAN protocol system, but rather a master/slave interface protocol.

Though it is generally agreed that whatever protocol IBM finally uses will be a significant de facto standard, many are not waiting for IBM to incorporate overlying network protocols.

Bridge and ACC have adopted the Xerox XNS protocol for their work above the link level. **Figure 7** shows how XNS maps into the ISO model; XNS can use nearly any medium for ISO level 1, and several protocols (Ethernet is often used in examples, since Xerox PARC is where Ethernet was originally developed).

As various networking vendors develop higher level software, system designers will have better chances for purchasing a networking scheme that will allow customers transparent networking to existing equipment. For the present, designing in networking functions, even to connect similar devices, requires some intensive software development. At the application level, probably for the foreseeable future, the closest one could hope to standards would be for narrow applications, or within networks of the same kind of computer.

Until some higher level networking software is standardized, bridges between incompatible networks will allow interoperability. Those firms retaining a proprietary networking scheme always will be eager to get connections into the few standard networks. Bridges into the IBM architecture will be prevalent, but since Ethernet has such a strong hold already, some are guessing that even IBM will provide Ethernet access.

Bridges allow departmentalized decisions about what sort of LAN best suits the immediate environment and needs, while providing any station at least partial access to all of the peripherals and processing at the wider location. Since a large majority of communications are at a local level, a bridge might not have to be transparent at all levels to be useful. And the optimizing of networks on a very small area brings advantages not only through network type, as witnessed by proprietary network schemes, but also by size. A small number of nodes on a network improves chances of immediate access on a CSMA system and decreases the time to pass a token on token passing systems.

Broadband links, by virtue of their multiple channels, can handle many nodes on a network. Several network vendors, including Corvus and Ungermann-Bass, envision broadband backbone systems to link smaller baseband nets. For interconnecting geographically distant networks, fiber optics has been suggested, since it needs fewer repeaters and is immune to lightning strikes.

Another valuable feature of separate networks is the relative ease of monitoring and control. Failures in a transparent network can be difficult to track down, and with subnets for areas, diagnosis of problems could be easier. Though comprehensive network diagnostic tools that hook onto a network like the Excelan (San Jose, CA) Nutcracker are being developed (**Figure 8**), most networking schemes for lower end equipment will include control in the node and software.

Interoperability of networks that are not within the same general area can be achieved through gateways to global networks, both public and private. Much development work is underway to implement X.25 internetworking, and Western Digital has a silicon implementation. Using a standard like X.25 gives network users access to services such as Telenet and others, as well as a method of internetworking.

Just as Ethernet and other standard link level systems have brought the manufacturer-independent communications environment closer, each level of software for networking will increase the interoperability of all types of equipment. Stan-

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dard VLSI controllers combined with the higher-level software that will be available over the next several years will allow a single LAN to link hundreds of devices from mainframes to PCs, terminals and peripherals as though they were directly connected.

Separate network processing prevents network overhead from becoming a burden on the system.

Building Machines to Network

One obvious effect of networking on the design of computer systems is that many more will be integrating networking capabilities as a standard feature. VLSI controller chips and their use in board configurations becoming available from many sources for standard networks allow fairly easy implementation of the physical and link layers of the OSI model.

Fewer new proprietary networks will probably be developed, though those already developed generally do optimize performance for the type of equipment into which they have been designed. The Datapoint ARCnet at 2.5 Mbit/sec is slower than many of the newer systems, but for the data processing environment in which Datapoint terminals generally operate, the speed is rarely challenged. At the other end, the sensitivity and quantity of graphics and CAD/CAM screen fills has pushed Cadmus and Apollo to use token passing systems with relatively low network overhead to leave as much transmission space as possible for the actual information being transferred.

Ingenious schemes such as the Stratus (Natick, MA) network can accommodate special needs. The Stratus protocol, designed only to link their fault-tolerant computers in situations where assured transmission is essential, is a contention ring system. Although stations on the network contend for access to the ring, transmitting nodes can simply add to a packet indefinitely, should the network become heavily loaded. Since the network is a ring, the transmitting node knows that the entire net has received the packet it sent when it receives it again and can then strip it off the beginning of the packet.

An important aspect of network design is keeping the network processing separate. Network functionality is not a totally simple matter, and care should be taken to see that the processing needed to implement a network is provided. Using the computer processor for networking may work for a while, but especially as networking software becomes more comprehensive and network capabilities allow extensive transparent access or even running applications across a net, the processing overhead of the network will become a burden on the system.

Including a networking function is only the very beginning of the changes that networking could bring to system design, however. Since a transparent LAN allows every user access to at least some of the processing power and data resident in the larger computers on the network, networked stations can be optimized for a particular task and still use generalized programs over the network. Each node, then, can be built for the tasks most often performed at that location and depend on the other devices connected for the functions that they have been each optimized to perform (**Figure 9**).

At the low end of the spectrum is the widespread use of the personal computer. Allowing every user some general computing power locally as well as the capabilities for specific tasks, the desire to connect PCs and allow them access to programs on mainframes will be a driving force in the LAN market.

An interesting use of PC networks is for resource sharing, generally meaning sharing of peripherals. The diskless node is operating on several networks, from 3Com to Cadmus to Santa Clara Systems (San Jose, CA). Sharing the expense of mass storage between several network nodes is desirable, particularly as node costs drop when costs for mechanical parts of peripherals probably will not. For PCs used as office workstations, sharing a printer can also be economical. If network software really does get to the applications level, software sharing could become a tangle for publishers and a joy for networked users.

Transparent networking makes security more difficult, however. By their very nature, many LANs allow all nodes to see data transfers. Methods for encryption over networks are being developed, and will, no doubt, become important at

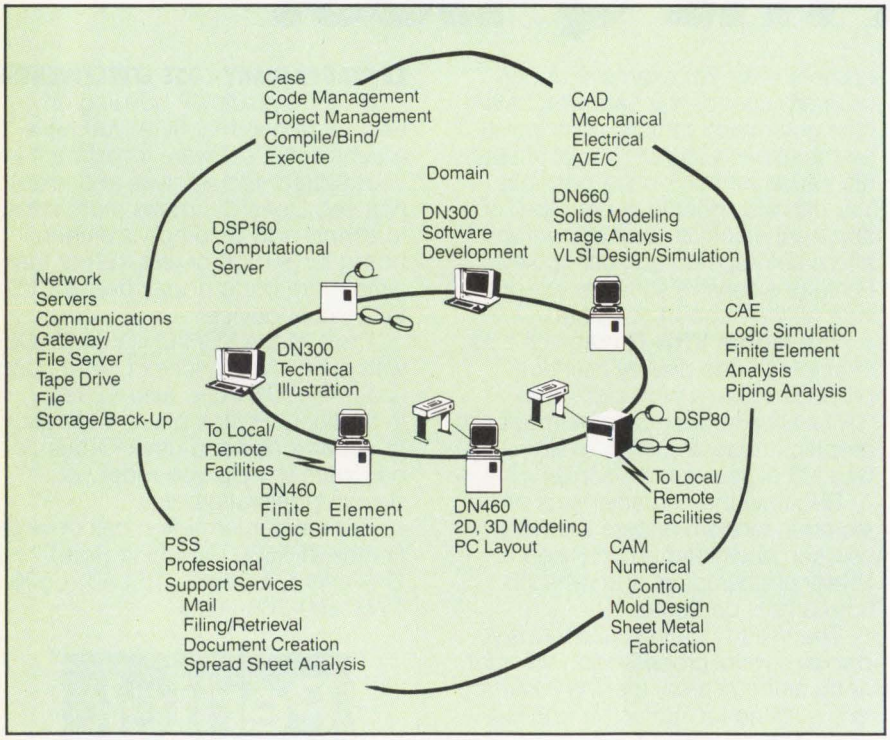

Figure 9: Resource sharing and workstation optimization are possible with LANs such as Apollo's Domain, which uses token passing over inexpensive coaxial cable.

many levels. Security and access levels will be particularly essential in interconnected network environments. The variety of network standards may facilitate keeping certain levels of information within subnetworks for the time being, but the spread of LANs could have a big positive effect on the market for encryption and security equipment.

Networked Work

As Bob Metcalfe, one of the developers of Ethernet and now President of 3Com, points out, networking is still trying to catch up and allow PCs all of the services that minicomputers provide in a distributed processing environment. Newer transparent networks and software mean that soon, new applications for the power of networked machines will appear.

There are several views of what this will mean for networks and users. Makers of token passing equipment generally indicate that over the next few years, network use could become heavy enough that the probabilistic nature of CSMA systems like Ethernet will set limits on these networks' efficiency. That is, that at very heavy loading, nodes on a CSMA bus will too frequently find the bus busy to keep up with the guaranteed access on a token system.

Promoters of networks other than Ethernet are sure to point out that despite the 10 Mbit/sec raw data rate of the system, maximum actual data transfers are at 30-50% that. Even Ethernet manufacturers admit that the actual rate is about 50%, but they generally contend that the portions of a network that will be more heavily loaded will use other network types to accommodate that, and that normal office environments will rarely, if ever, reach such heavy loading.

The much heralded paperless office will be near when LAN systems are in place. Electronic mail is only the beginning of this. With access to stored information over the net, file transfers can be repeated as needed, and printouts could be reserved for data that has already been worked on by the local node. Broadband coaxial or fiber optic systems or system sections can extend the vision to include video and voice on a local area network. □

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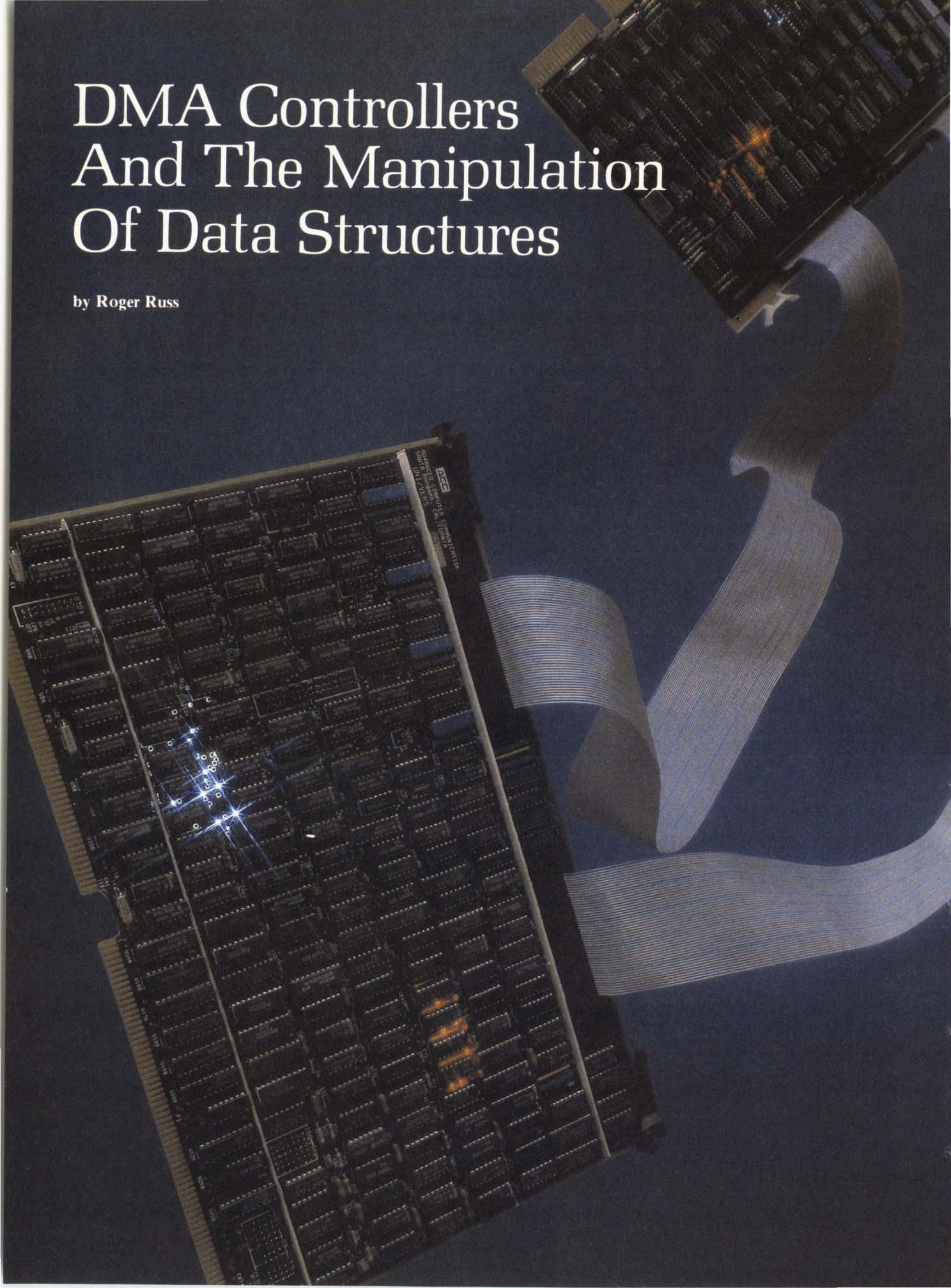
by Roger Russ



Board level products now exist which feature 16-bit microprocessors, 256K bytes of RAM, I/O controllers and data bus interfaces. Many products are compatible with the new data busses, including disk controllers, interfaces to other busses, large memory arrays and network interfaces. The structure of these busses permits multiple processors, and the impact of this is being felt at the system level. Problems such as resource sharing, coprocessor communication, interrupt handling and job allocation provide new challenges.

An example of a 16-bit microprocessor and its corresponding data bus is the Motorola 68000 and the VERSAbus. A device currently available to allow data transfers between the VERSAbus and Digital Equipment Corporation's UNIBUS is the UNI/VERS interface. As shown in **Figure 1**, the interface consists of two printed circuit boards: The V-Board, which plugs into a standard VERSAbus backplane, and the U-Board, which plugs into a UNIBUS SPC (Small Peripheral Controller) slot.

The UNI/VERS provides a simple data link between any VERSAbus based system and any PDP-11 or VAX system. Currently, the only other available method of connecting these two types of systems is serial I/O. This interface is a high speed alternative: a 4 Kbyte program can be loaded into VERSAbus memory from a host PDP-11 or VAX in the time it takes one typical instruction to be transferred at 9600 baud.

A PDP-11 or VAX system may be CPU bound by specific processing tasks that could be off-loaded to a 68000 through the UNI/VERS. UNIBUS systems can take advantage of the multiprocessing capabilities on the VERSAbus by using a UNI/VERS, and VERSAbus network controllers can be easily attached to PDP-11 systems. Conversely, VERSAbus based CPUs can take avantage of the wide range of peripheral controllers available on the UNIBUS through this interface.

A general problem encountered when connecting two busses is how to deal with two memory organizations. If the designer is lucky, the memory organizations will be identical.

The UNI/VERS was designed with the limitations and advantages of each bus in mind. Since the VERSAbus is a more recently designed data bus than the UNIBUS, it has higher performance characteristics, including higher bandwidth, lower deskewing times, larger memory addressing range, more interrupt levels, more DMA priority levels and provisions for multiprocessor systems.

To take advantage of these features, the main DMA control structures reside on the VERSAbus. This allows the UNI/VERS to be a peripheral device to a processor on the VERSAbus, and allows the UNIBUS's 256 Kbyte addressing range to be memory mapped onto the 8 Mbyte VERSAbus.

The UNIBUS has practical bandwidth limitations; any particular DMA device will probably not be able to exceed a throughput rate of 500 Kbytes on a moderately loaded PDP-11 or VAX system. For this reason 500 Kbytes was chosen as the target rate for the interface. This rate can be considerably higher during VERSAbus to VERSAbus DMA transfers because the UNI/VERS does each part of the transfer separately. The VERSAbus

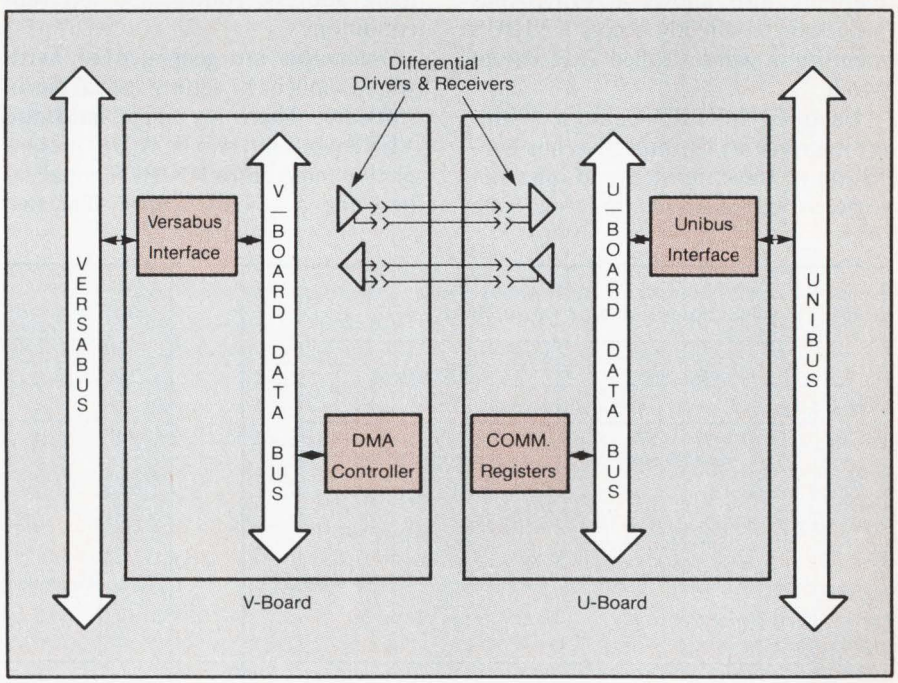


Figure 1: UNI/VERS uses two boards for data transfer between VERSAbus and UNIBUS SYSTEMS.

Roger R. Russ is currently a senior technical staff member at ACC (Advanced Computer Communications), 720 Santa Barbara St., Santa Barbara, CA 93101, where he is responsible for hardware-related design and development. Mr. Russ holds a BS in physics from Harvey Mudd College.

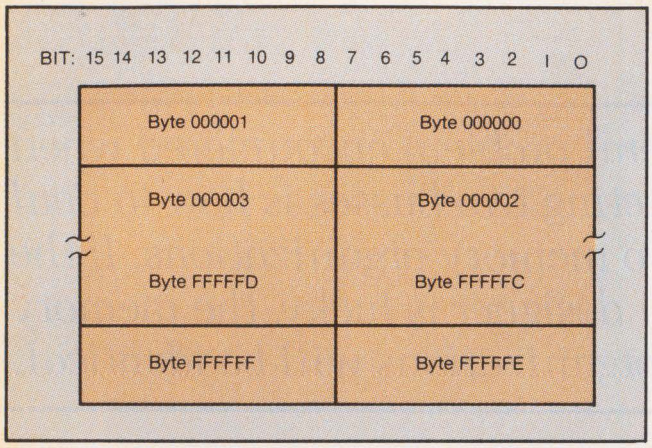


Figure 2a: VERSAbus memory organization: byte address.

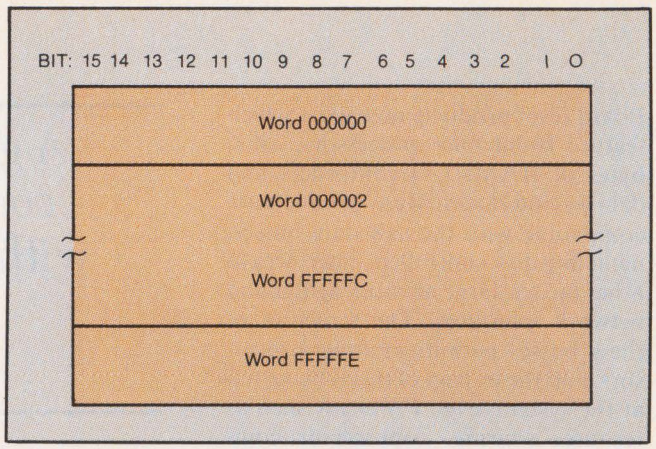


Figure 2b: VERSAbus memory organization: word address.

transfer is done without maintaining bus mastership on the UNIBUS, and vice versa.

Mapping the UNIBUS onto the VERSAbus allows DMA Mode to be quite simple. The VERSAbus processor loads source and destination addresses, a transfer count, a GO bit and then waits for completion. Since there is nothing unique about the UNIBUS addresses, the DMA controller does memory-to-memory moves anywhere within the VERSAbus address range. If an address lies within the UNIBUS memory map, the next cycle of the DMA controller will generate a UNIBUS DMA cycle. Memory mapping also allows a VERSAbus processor to directly access UNIBUS memory in what is called Transparent Mode.

Each UNI/VERS board contains an interface to its respective bus consisting of slave, master, and interrupt logic, as well as an internal three state bus. The remaining features of the boards differ greatly. Generally, the V-Board may be thought of as the master board in bus-to-bus transactions. Although the U-Board becomes UNIBUS master, control is generated by the V-Board. This makes the U-Board the slave for any data transfer.

In DMA Mode, bus cycles are generated by the V-Board's DMA Controller. If the current address is a non-UNIBUS address, a VERSAbus DMA cycle is generated. Otherwise, a signal is passed to the U-Board asking for a UNIBUS cycle. The boards communicate through a set of differential drivers and receivers by signals that include data, address, control and interrupt conditions.

Interrupts are generated by hardware events or by setting special bits in software. There are three hardware VERSAbus interrupts: A DMA completion interrupt, a UNIBUS initialization and a UNIBUS error. The two software interrupts on each bus are bits set by a program on one bus which create an interrupt on the other bus. This allows a VERSAbus program to signal a UNIBUS program and a UNIBUS program to signal a VERSAbus program. Each side has two interrupt bits; there are two unique vectors on each bus.

The V-Board contains the DMA Controller, which is designed with SSI and MSI parts to be simple. An important influence in this style was unavailability of a DMA device compatible with the 68000 microprocessor during development. The DMA Controller contains five registers: The Control Register, the Source Address Register, the Destination Address Register, the Transfer Count Register, and the Data Register. A DMA transfer is accomplished by loading the necessary values into the Source and Destination Address Registers and the Transfer Count Register. Then the GO bit is set

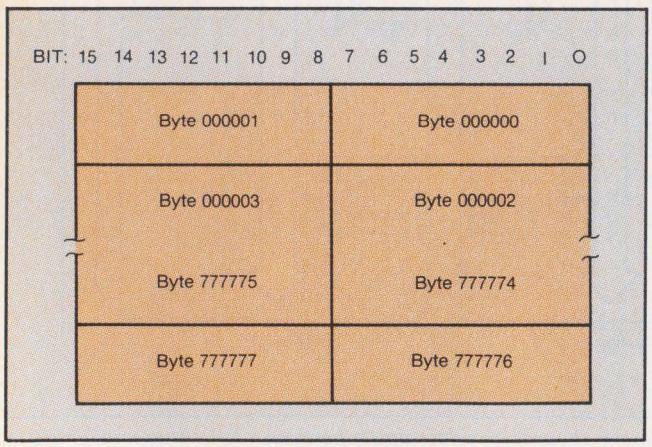


Figure 3a: UNIBUS memory organization: byte address.

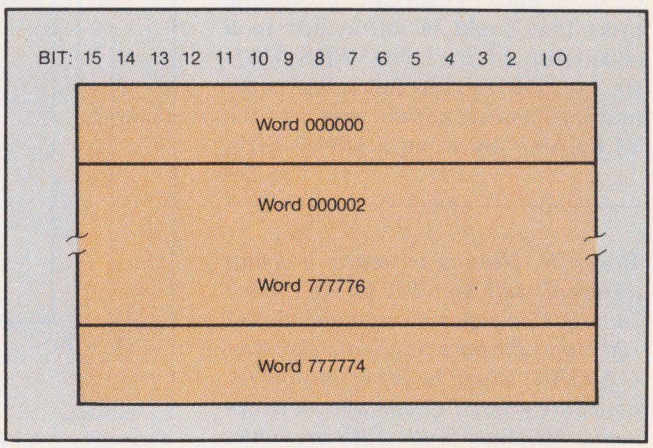


Figure 3b: UNIBUS memory organization: word address.

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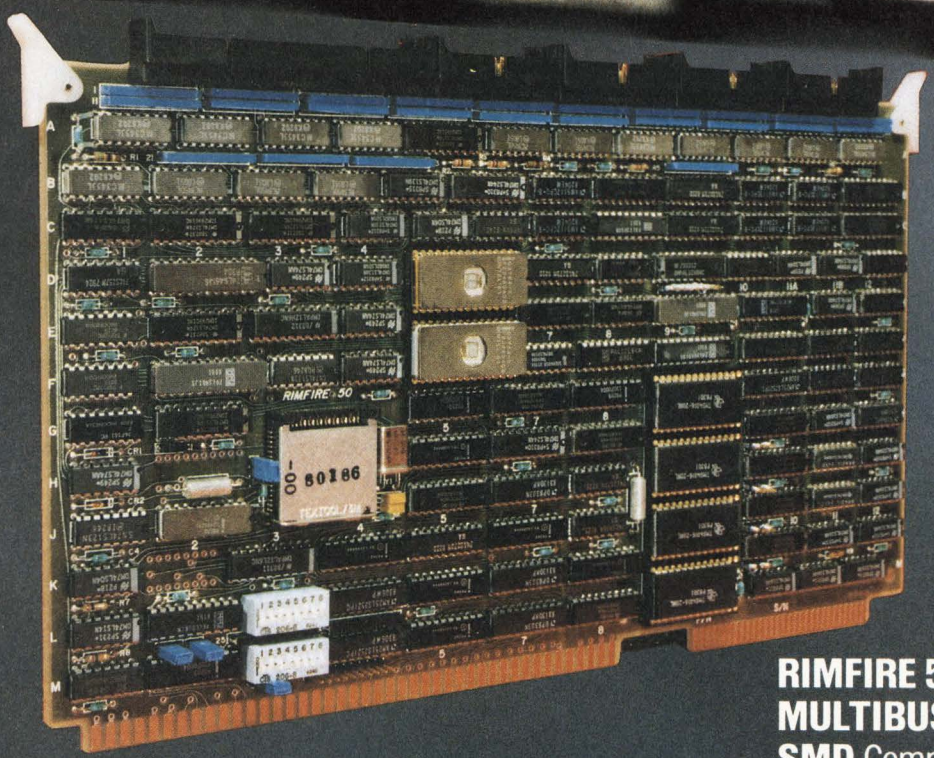

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in the Control Register. When the transfers are complete, the DMA completion interrupt occurs.

The U-Board contains a set of sixteen Communication Registers which are accessible from each bus as device registers. There is one hardwired register and fifteen user definable registers. The hardwired register contains two bytes: The first byte is writable only from the UNIBUS, and the second byte is writable only from the VERSAbus. The UNIBUS byte contains a DMA Enable bit, a Reset bit, two Interrupt bits and an Interrupt Enable Bit for each interrupt from the VERSAbus. The VERSAbus byte contains the two VERSAbus-to-UNIBUS Interrupt bits.

The fifteen "soft" registers may be used in any manner suitable to the application. A practical use is to define a subset of the registers to emulate a standard UNIBUS type DMA device. This allows the program in the PDP-11 or VAX to treat the UNI/VERS as if the Communication Registers were actually DMA Registers. The parameters are put into the Communication Registers, an interrupt is sent to the VERSAbus, and the DMA transfer is accomplished. The VERSAbus process then sends an interrupt to the UNIBUS. The PDP-11 or VAX program can treat this interrupt as a DMA completion interrupt; so, from the PDP-11 or VAX program's point of view, the UNI/VERS is a normal DMA device.

In a system level example, the UNI/VERS connects a VAX to a high speed serial network. A VERSAbus Processor Board (V/PB) communicates with a process running in the VAX through the Communication Registers on the U-Board. When a DMA transfer is necessary, the V/PB initializes the V-Board DMA Registers, and the UNI/VERS transfers the data from UNIBUS memory to VERSAbus memory located on the V/PB. The remaining data transfer from the VERSAbus to the network is controlled by the V/PB through the use of a High Speed Serial I/O Daughter Board (D/HSIO). This system configuration relieves the VAX of network protocol processing and takes advantage of the buffering space available on the VERSAbus.

A general problem encountered when connecting two busses is how to deal with two memory organizations. If the designer is lucky, the memory organizations will be identical.

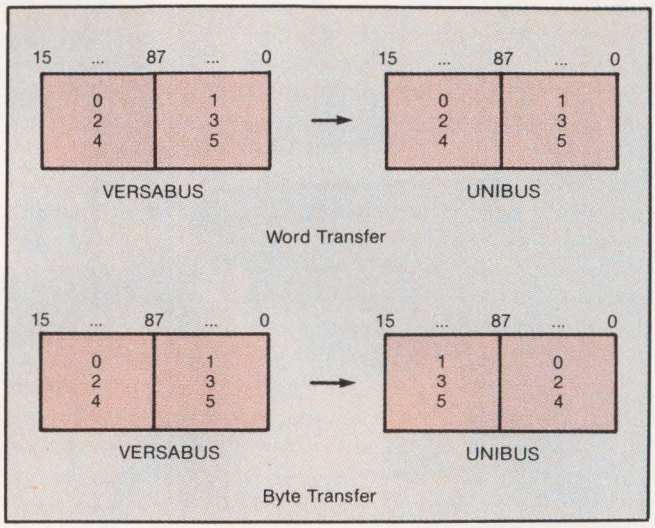

Figure 4: Byte vs. word transfer, VERSAbus to UNIBUS.

In the case of the VERSAbus and the UNIBUS, the memory organizations differ. **Figure 2** shows the VERSAbus memory organization: the number base is hexadecimal and the address range is 16 Mbytes. Bits are numbered from right to left with the least significant bit being bit 0. All word addresses are even. Byte addresses may be odd or even; the even address contains bits 8 through 15 and the odd address contains bits 0 through 7. **Figure 3** shows the UNIBUS memory organization. The number base is octal and the address range is 256 Kbytes. As with the VERSAbus, bits are numbered from right to left with the least significant bit being bit 0. All word addresses are even. Byte addresses may be odd or even. The significant difference between the two busses is that the UNIBUS byte addressing scheme is opposite that of the VERSAbus. That is, the even byte address in the UNIBUS contains bits 0 through 7 and the odd byte address contains bits 8 through 15.

Since both byte and word accesses are supported on both busses, it is not clear whether byte or word order should be preserved. **Figure 4** shows how the transfers are different. Each example is a six byte transfer from the VERSAbus to the UNIBUS. In the top of the diagram, word order is preserved. The most significant bit of the word remains the same in both busses, but the byte ordering is now swapped on the UNIBUS. This type of transfer is desirable for data structures of word length, because numerical word length integrity is maintained. In the bottom half of **Figure 4**, byte transfers are shown with consecutive bytes being transferred in increasing byte address locations. The resultant order of the bytes is opposite that of the word transfer case. The most significant bit of the word no longer remains in the same place, but the byte ordering is correct. This type of transfer would be more useful for byte data streams, as no reorganization would have to be done by the UNIBUS processor.

The UNI/VERS supports both word and byte transfers. Word transfers are accomplished exactly as shown in **Figure 4**: the transfer length is 16 bits and each bit number remains the same on both busses. To support byte ordering, a parallel set of transceivers was added between the VERSAbus and the internal three state of the V-Board (see **Figure 5**). By setting control bits in the Control Register, either set of transceivers may be enabled.

For word transfers without any control bits on, the even byte of the VERSAbus is enabled onto the high byte of the internal bus and latched in the most significant half of the Data Register. Simultaneously, the odd byte is enabled onto the low byte of the internal bus and latched in the least significant half of the Data Register. When the data is transferred to the UNIBUS, no other rearranging of the bytes is done. The other set of transceivers may be used by setting a control bit in the Control

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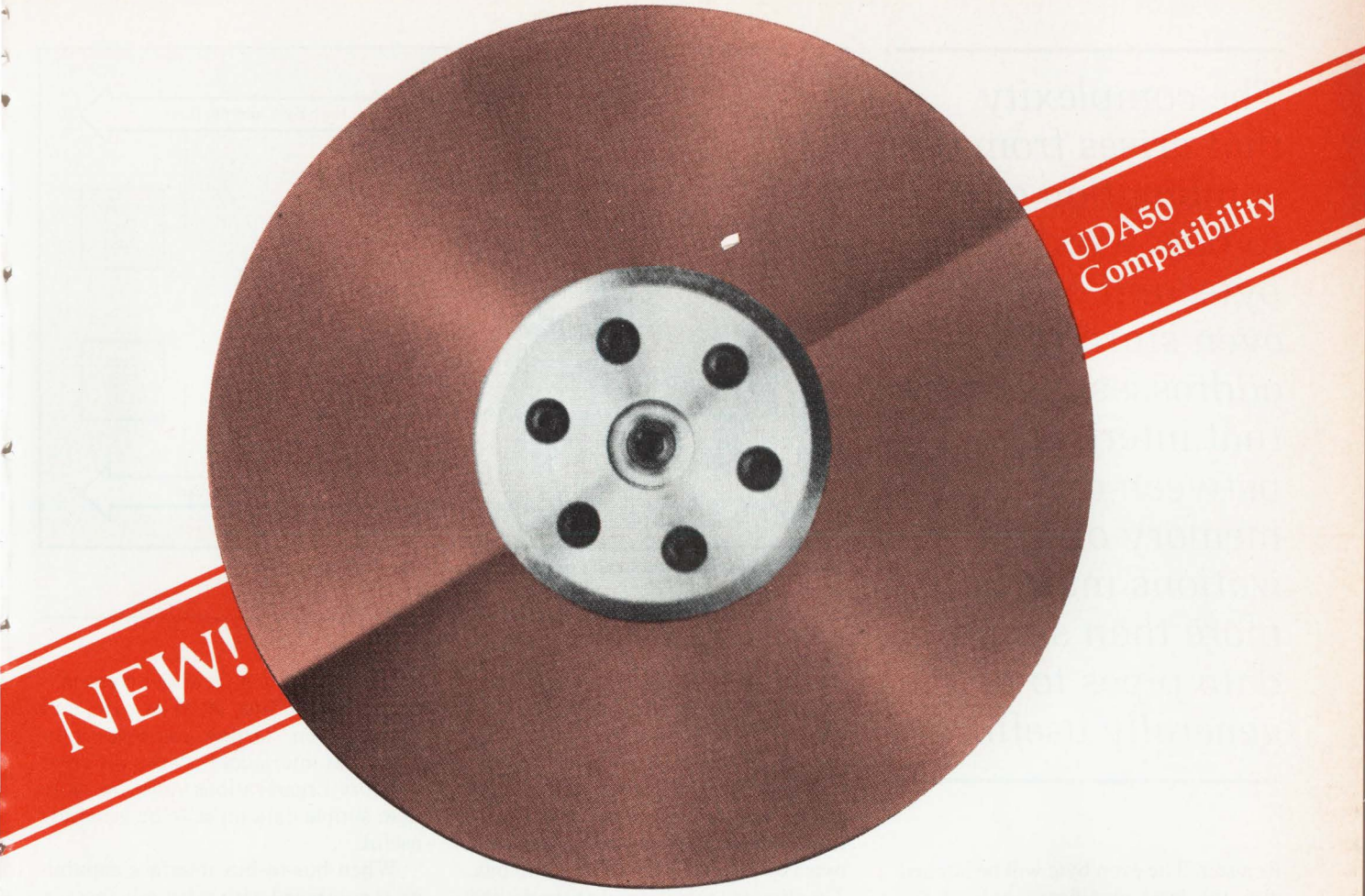

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The complexity that arises from the combination of bus to bus, word or byte, and odd or even starting addresses indicates that interfaces between different memory organizations must be more than simple data pipes to be generally useful.

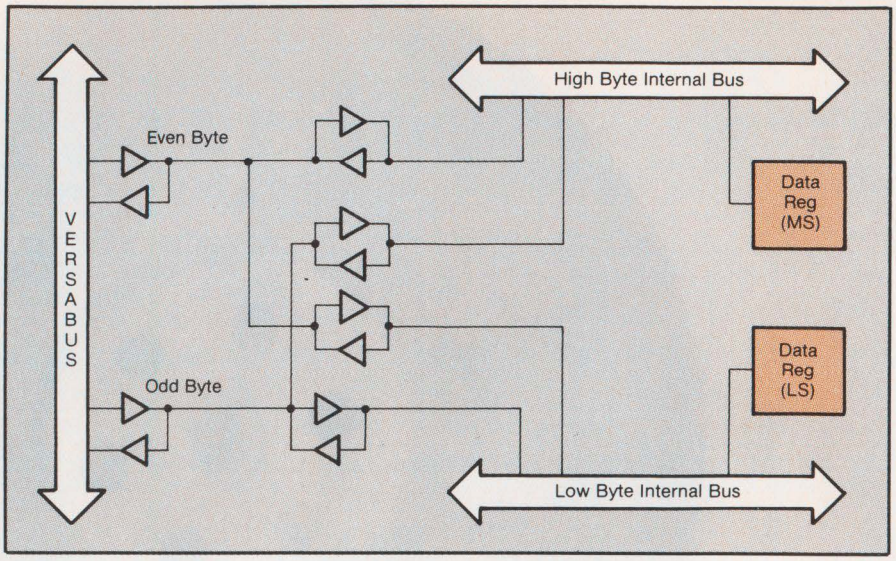

Figure 5: Parallel transceivers provide internal byte buffering.

Register. The even byte will be latched into the least significant half of the Data Register, and the odd byte will be latched into the most significant half of the Data Register. In word mode, either transfer depicted in **Figure 4** may be used.

Byte transfers are more complicated than word transfers because the source or destination buffers may begin on even or odd addresses. Restricting the discussion to VERSAbus to UNIBUS transfers will show how the UNI/VERS supports the different cases. To support all the possible cases, two control bits are used. There is one control bit for the Source Address Register and another for the Destination Address Register. Each bit inverts the least significant bit of its respective address register if it is set. If it is not set, there is no effect. For example, if the Source Address Register contained 20000 and the Destination Address Register was 30000 with the Source Swap Bit off and the Destination Swap Bit on, then a byte would be transferred from 20000 to 30001.

Of the 16 cases of VERSAbus to UNIBUS data transfers, only those with an odd number of bytes are critical, because even transfers lengths have redundant cases. An example of an even address to an even address with both swap bits off is basically the byte transfer case of **Figure 4.** If the source buffer had its byte ordering reversed, the DMA controller could reorder the bytes by setting either of the swap bits. The choice would depend on the desired structure of the buffer's last byte. If the buffer contains an even number of bytes, the choices are equivalent. The remaining permutations involve an odd address in either or both of the source or destination buffers. Some of the data structures seem unlikely, but they could result from a byte data stream originating from a memory organization different from that of the VERSAbus.

For example, if a byte data stream entered the VERSAbus coming from a memory organization similar to the UNIBUS, an interesting structure could result. By relocating the buffer in the UNIBUS, the UNI/VERS could preserve the byte ordering on the odd byte boundary, or, in another case, preserve the byte ordering on an even boundary.

The UNI/VERS interface is capable of reorganizing data structures in either direction between the UNIBUS and VERSAbus, and also in VERSAbus to VERSAbus block transfers. This represents 48 possible cases. UNIBUS to UNIBUS reorganization is not supported, since the DMA controller resides on the VERSAbus. The complexity that arises from the combination of bus to bus, word or byte, and odd or even starting addresses indicates that interfaces between different memory organizations must be more than simple data pipes to be generally useful.

When bus-to-bus interface capability is combined with other advances in technology, a useful bridge between systems can be established. UNIBUS based systems can be combined with VERSAbus based systems through a link that will organize data structures during DMA block transfers, so the new technology can be easily linked to established systems. □

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Intelligence Migrates Toward Small Systems Peripherals

There is a steady trend toward equipping disk storage subsystems with intelligence.

by Mike Cashman,
West Coast Technical Editor

Steady advances in LSI and VLSI circuitry are changing the makeup of peripheral devices and their relationship to systems as a whole. In no other segment of the industry is this trend as obvious as in the disk storage sector, and the quickly moving 5¼" Winchester marketplace is developing at a breakneck pace. New systems interfaces involve hooking up to a board or a box which is a lot smarter than the controller or peripheral of just several years ago.

Virtually every source interviewed for this article agreed that there is a steady trend toward equipping peripheral subsystems with intelligence, notwithstanding that what used to be called a control function capability is now called intelligence. Many agree that future disk devices will have on-board integral controllers, or at least a set of chips (1 to 4 in number) which won't take up very much space. What the sources don't agree on is who will be supplying and/or installing the chips. Will it be the disk drive manufacturer, driven by a need to get into a more value-added business? Will it be

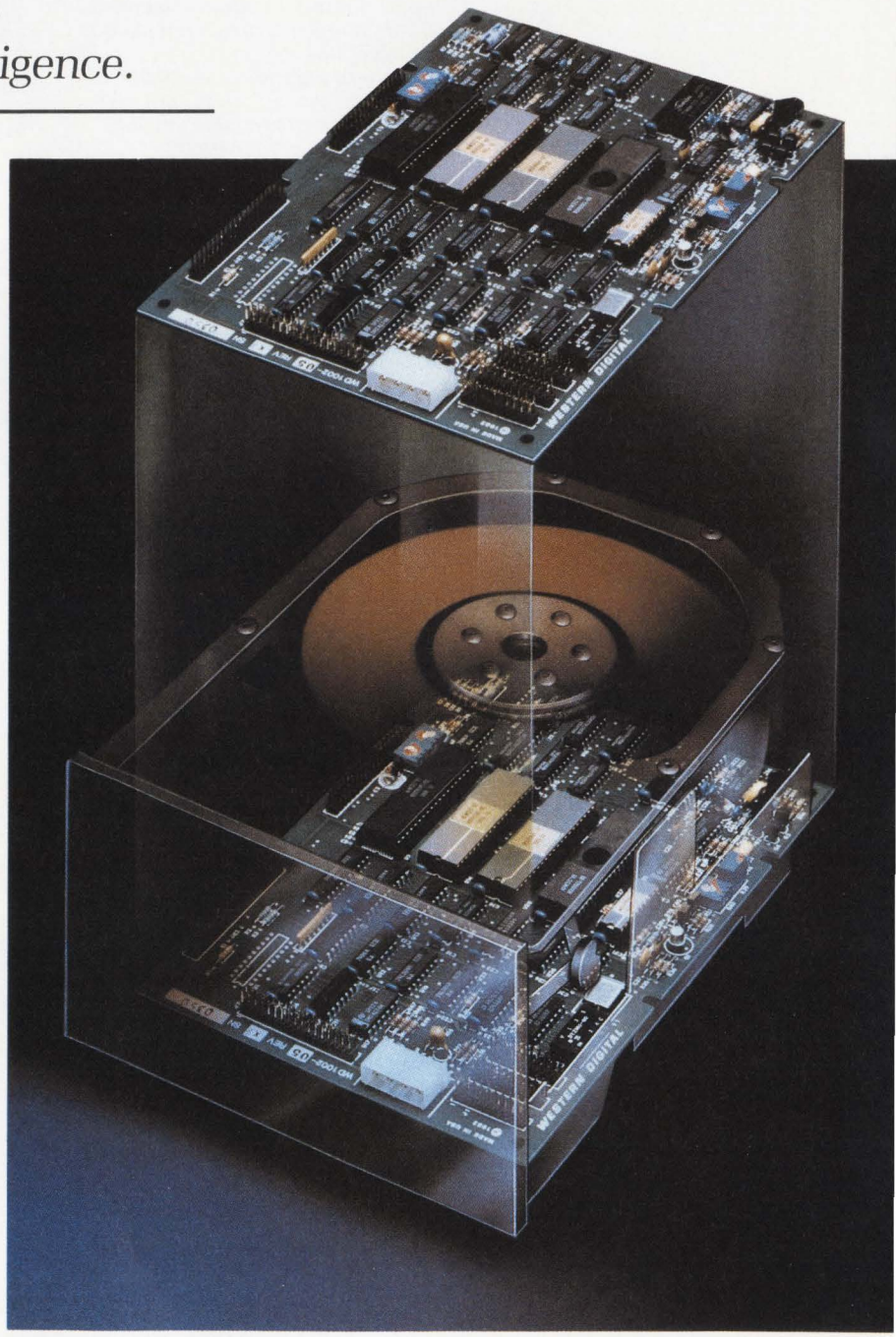

Figure 1: Plug compatible with the industry standard SASI interface, the WD1002-SHD interfaces up to two Winchester disk drives to a host processor. The board is a stand-alone VLSI intensive SASI solution based on the WD1010 single-chip Winchester disk controller and additional Western Digital VLSI components. (Photo courtesy Tokyo Electron Limited.)

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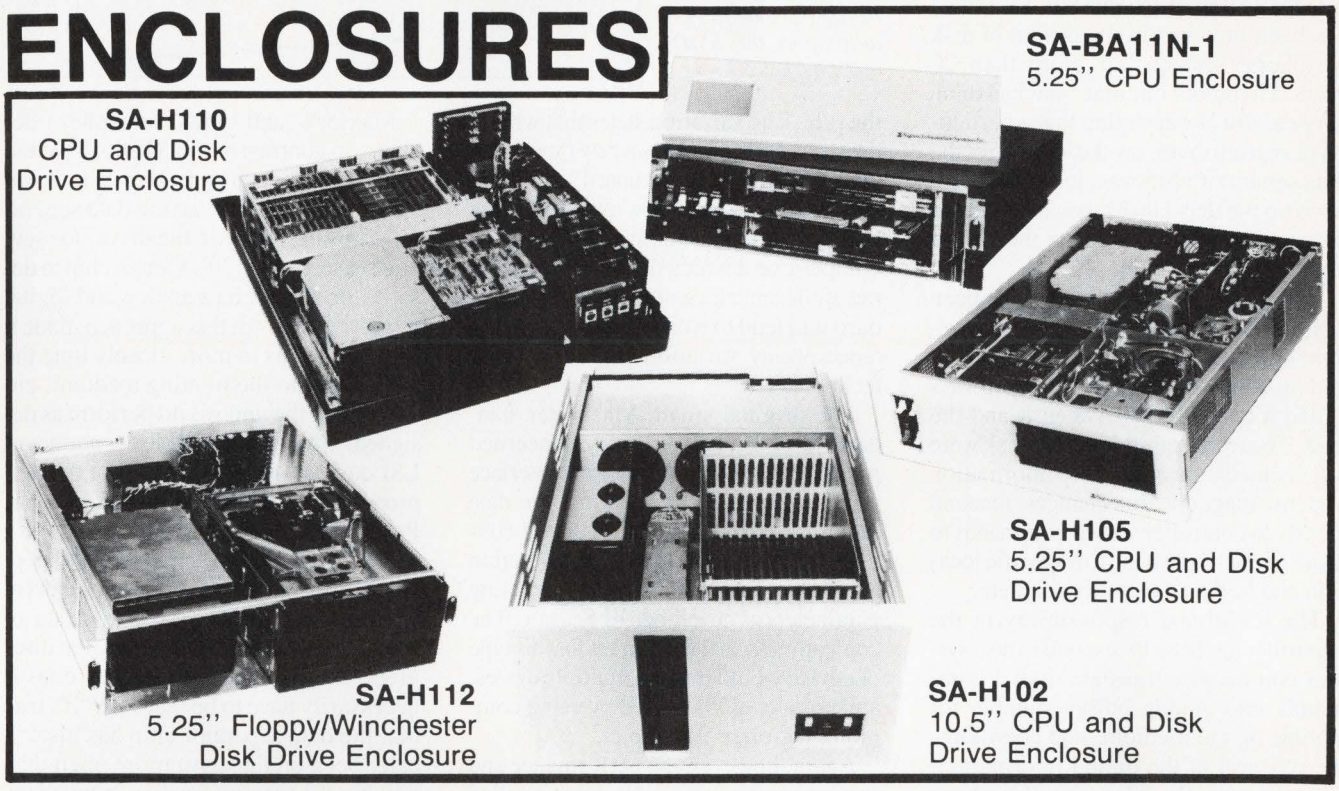

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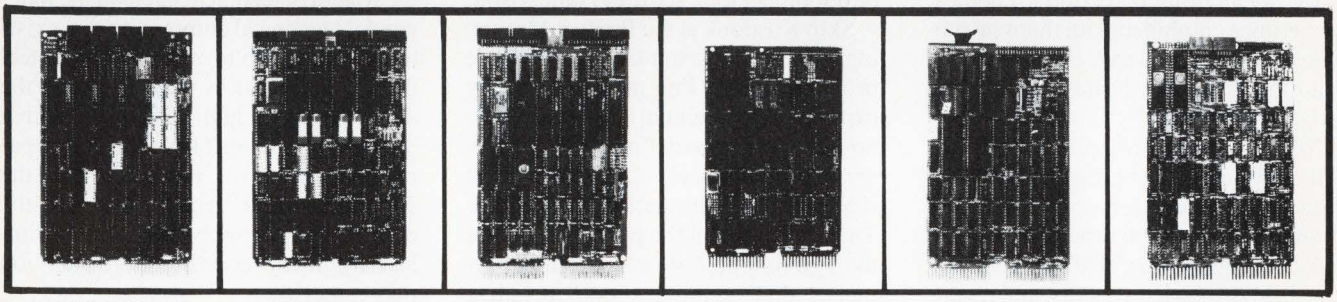

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the systems integrator who has, in the past, solved the problem by going to the disk controller manufacturers and will now be able to do it in-house with a few chips? Or will it remain the controller manufacturers?

I. Dal Allen of Priam (San Jose, CA) has been involved in the design of disk peripheral systems for more than 20 years. He points out that "one has to be very careful about stating that a particular design attribute, say the location of the data separator chip was, in the past, *always* on the drive itself, because even in the early years of the industry there were lots of design variations."

Over the years, disk systems have been designed as a truly cooperative subsystem, based on a rotating storage medium and a controlling device (not always called a controller) between it and the host. The responsibilities of the disk were largely mechanical; to store information as dense magnetic flux changes, respond exactly to controller-issued commands to move a read/write head to a specific location and begin reading/writing, etc.

The traditional responsibility of the controller has been to respond to host system commands, translate digital commands into analog pulses suitable for storage on the medium, and coordinate the retrieval of the digital information. Over the years these functions have been elaborated a great deal, and new functions have been added. Today, a variety of error detection/correction schemes, sometimes combined with maps of substandard storage areas, can operate in many cases without the host CPU having to become involved.

This was not always so, and as Priam's Allen observes, "The capability of peripherals dictate systems performance—more than the central processor does, in most configurations." This is especially true in micro-based systems, and it's difficult to conceive of a more critical peripheral in any size system's performance than its disk storage subsystem.

Enter Standards

Alan Shugart some years ago said that he was "dismayed" at what had become of his original floppy disk design. He reflected that much of the simplicity and orientation toward an inexpensive product had been designed out of the system in search of higher performance.

Standards seem to be a variation of The Golden Rule: He who has the gold makes

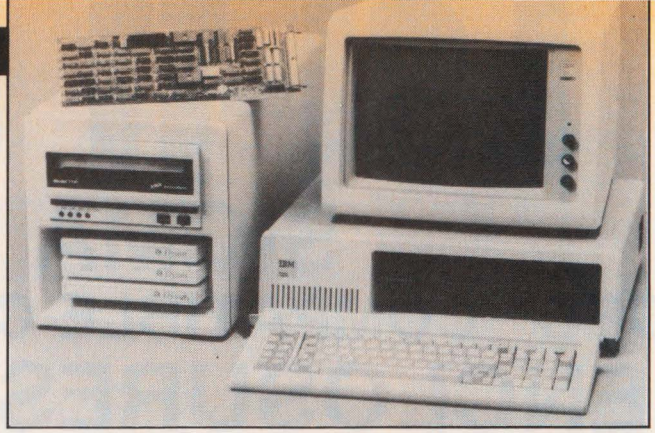

Figure 2: High performance rigid disk controller, the Maverick SMD PC-80 from Interphase Corporation is the first rigid disk controller for the IBM PC or PC look-alikes to support the SMD disk interface.

the rule. The variation states that whichever company develops a new type of device sets a *de facto* standard. The standard will make the new type of device easier for the marketplace to accept all competitive devices that operate within the same interface standard. The standard will tend to work against the acceptance of any variations on the original technology.

The original small Winchester standard was broadcast to every concerned party. This is the familiar ST506 interface standard which stipulates that the data separator chip be mounted on the controller board. This was the best solution to a set of engineering and marketing parameters as developed by Seagate. The company saw that the market for this type of device would involve multiple drives, and costs could be pared by using common controller electronics.

Again, however, the performance and capacity ranges covered by what is called a 5¼" Winchester disk drive vary enormously, making the "dismaying" floppy development look static by comparison.

Skip Kilsdonk is the Product Marketing Director at Maxtor Corp., at this time probably the leading maverick in fully exploiting the potential of 5¼" disk technology. "It helps to define the electronics and standards issues in this environment if one envisions the market as a pyramid. The broad base of the pyramid includes the high volume, low or 'standard' performance disk manufacturers, including Seagate, Tandon, Miniscribe, DMA Systems and others. I'd give this base of the pyramid an upper (arbitrary) capacity limit of perhaps 20 Mbytes. The middle of the pyramid includes companies manufacturing drives with roughly 20 to 60 Mbytes of capacity. This would include Atasi, Priam, Evotek, and others. I'd put ourselves and any other manufacturer in the top of the pyramid, anything above 60 Mbytes of capacity." So the product called a Winchester can vary from a 5 Mbyte device all the way up to Maxtor's 380 Mbyte disk.

Maxtor's (and other companies') designs, in contrast to the ST506, have the data separator chip on the disk drive. "Our engineers felt that the data separator chip should be on the drive, for several reasons. First, it's a tough chip to design, for it combines analog and digital circuitry. Second, this approach made it possible for us to more closely tune the electronics to the rotating medium, ensuring that the unit would perform as designed. Given the favorable economics of LSI curves, we decided to take this approach," says John Klonick, Manager of Product Marketing for Maxtor.

While many engineers feel that keeping the data separator chip on the drive makes sense for the top two strata of Kilsdonk's pyramid, Priam's Allen disagrees, saying that the design doesn't necessarily have to be that way. "It's true that the data separator chip has historically been on the drive more often than not, but the reasons for that, in my view, may not be the most obvious. Those were the old mainframe days, and there wasn't the wealth of technical talent in the independent technical community that exists today. I would point out to those who feel that data separators have to be on the drives to ensure high performance, that the IBM 3330 didn't have the data separators on the drive; the chip was in the 3333 head-of-string box." To Allen, the data separator chip issue is just a pointless argument receiving more attention than it merits.

Again, there are disagreements. "Above about 15 Mbits transfer rate, propagation delay really becomes noticeable," says Joe Jaworski, Director of Advanced Planning for disk controller manufacturer Western Digital (Irvine, CA).

OEMs typically select the disk device performance attributes first (with an eye toward whether controllers are available), and then select the desirable controller. Most controller companies with large in-house development staffs would probably echo Western Digital's Jaworski. Jaworski says his firm doesn't care where the

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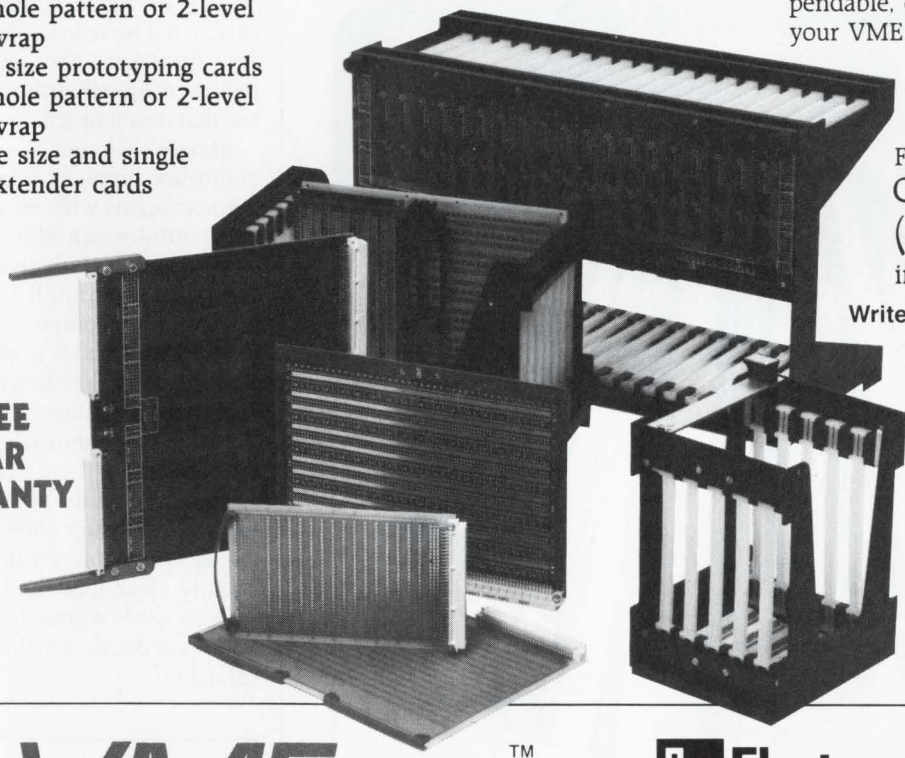

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electronics are. His firm tries to figure out what the market preference is for various types of drives, as that will usually lead to increased controller sales.

Integral Drive Controllers

The trend toward smarter disks is more than the location and distance between the rotating medium and the data separator chip. In the age of VLSI, what would be the implications of a complete controller offered as a single chip, or a small chip set? If it were offered directly to large volume systems integrators, would this be a severe blow to the controller houses?

It appears, in fact, that an announcement of this type of device may be close at hand. One source we contacted turned us toward Motorola's Austin, Texas facility regarding just such a product. The source indicated that Motorola had been previewing this chip set around the Silicon Valley to potentially interested parties. Apparently, Motorola has been able to deal with the attributes of different manufacturers' disk drives in a single package. There are also strong rumors that NEC is working on a gate array product that might conceivably be for the same market. The best guess from several sources as to which company might be considering these chip packages for integrating into their equipment pointed to Apple Computer.

"That's very interesting," says Western Digital's Jaworski. "We see the market as being 85% ST506 interface for the foreseeable future; maybe Motorola came to the same conclusion. It's certainly possible to put the chips on the drive, but my experience has been that large volume buyers tend to prefer bare-bones mechanisms, figuring they can do the interfacing cheaper themselves. Still, I think there will be room in the market for everyone. I really didn't think we'd see this development until the end of the decade."

John Smith, Director of Hardware Products at Emulex, feels that a totally VLSI controller is a risky development. "Sure there's a trend for intelligence to migrate out to the peripherals, but somebody is banking that the disk device it will control will be around for a long time. I have to believe that whatever is announced will address a single device, and not multiple devices."

Maxtor's Kilsdonk says that technological developments will make it easier in the future to put the controller on the drive, but that "we just aren't seeing the demand for a product like that, at least not yet. There are advantages and some disadvantages in taking that approach, and one has to remember that the good controller people can do wondrous things with their economies of scale. Xebec, for example, has got it down to the science of having robots assemble their controllers."

One source observed that a complete disk controller would up system reliability because it would enable the disk manufacturer or integrating OEM (or both) to test the disk/controller as a complete integral unit. He also thought that a complete level of interconnections would be obviated.

"I've heard all this before," says Bill Horton, Vice President of Engineering at Adaptive Data Energy Systems (Pomona, CA), a controller supplier. "Disk people like to talk about putting controllers on drives, but we're in a very different business from them. We can build that controller cheaper than they can. I just don't see that development as a threat."

Maxtor's Klonick does feel that some controller suppliers might be forced to come to terms with the development of the controller on a chip. "The little companies, with no in-house design sophistication, might come in for some trouble." Adds another source, "a single controller chip still needs a phase lock loop, which is not easy to design, so the capable controller manufacturers will probably take the chip controller announcement in stride."

It's clear that the emergence of a single disk controller chip will be an interesting development when it bows. It is equally clear that marketing forces at various levels within the manufacturing strata will decide whether it is a successful debut. □

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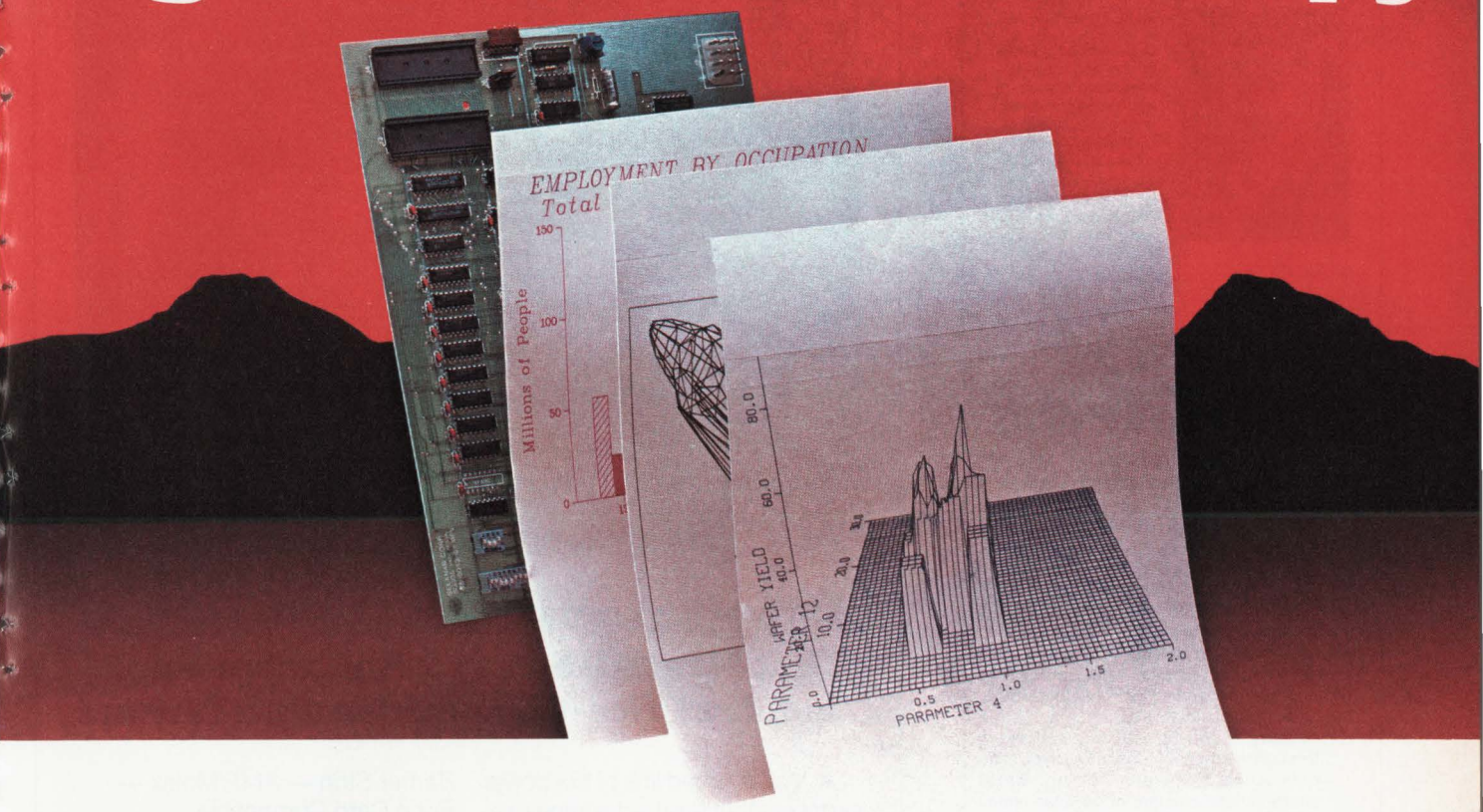

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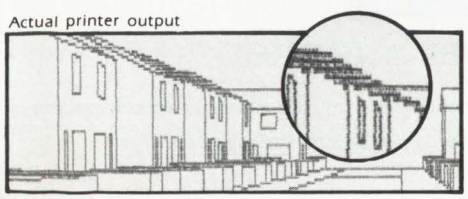

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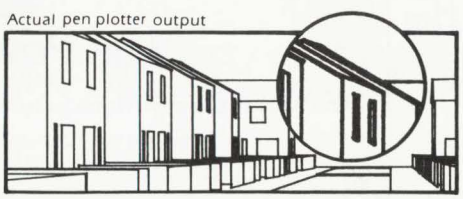

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Rx FOR HEALTH

INSTALLMENT THREE

By Lawrence Lee, MD

Dr. Lee is a leading Southern California Internist, specializing in cardiology. He is a co-founder and board chairman of LH Research, Inc. This column is presented as a public service for better understanding of topical medical problems and possible solutions.

HERPES!

SIMPLEX TYPE 2 VIRUS

In our last column we discussed HERPES SIMPLEX 1, which occurs primarily above the waist.

HERPES SIMPLEX 2 (HSV-2) infects people primarily below the waist, usually in the genital areas (penus, vulva, cervix). HSV-2 is frequently acquired during close contact between infected and susceptible individuals during the sexually active periods of life. The incubation period is the same as for HSV-1; from as little as two days to two weeks. The pathogenic mechanisms are the same for HSV-1 and HSV-2. There are three basic phases:

(1) **Primary Initial Infection**–Virus enters through the mucocutaneous surface (skin or mucous membrane), giving rise to characteristic clusters of vesicles (small blisters), and commonly associated with fever, local lymph node enlargement, pain on urination, tired feeling and local and/or radiating pain to thigh or buttock area. The vesicles will normally remain up to two weeks.

(2) **Latent Infection**–After initial healing, the virus enters the sensory nerve and is harbored in the body of that sensory nerve in a dormant stage until . . .

(3) **Reactivation of Latent Virus**–This occurs when some trigger mechanism, such as menstruation, skin trauma, sexual activity, fever, anxiety or other unknown mechanisms come into play to reactivate the virus in the sensory nerve. The virus then migrates down the nerve to produce the typical cluster of vesicles. Prior to the outbreak of these vesicles, the person usually experiences some itching, burning or pain at the site. The frequency and intensity of these recurring lesions are highly variable from individual to individual. Once latent infection is established, the virus persists for a prolonged period of time–and in some individuals for life.

The most serious complication of HSV-2 is infection of the newborn, who lacks immune defense mechanisms. Thus, the passage of a child through an infected birth canal can cause a massive viral infection and possibly death.

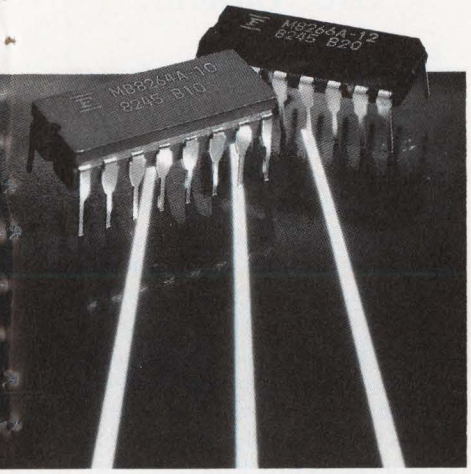
In our next column, we shall discuss diagnosis and latest treatment of HSV-2.

LH RESEARCH

The Power Supplier.

This is the third in a series of columns by Dr. Lee on medical subjects of current interest, although perhaps not fully understood, by the public. If you have a question, please write Dr. Lee at LH Research, Tustin, CA 92680.

DRAMs And EEPROMs Offer New Applications for μPs



DRAMs and EEPROMs are expected to compete in some application areas, though not in the near future.

The photo to the left is of Fujitsu's MB 8266A 64K DRAM.

by Ram Appalaraju

Though not in the near future, dynamic RAMs and EEPROMs are expected to compete in some application areas. At present, EEPROMs are preferred in applications related to distributed processing, that require easy in-circuit programmability and versatility. However, insufficient standards in EEPROMs is, at present, a big drawback. The large die size associated with EEPROM is mainly responsible for its high cost. Further, if EEPROMs are to compete with dynamic RAMs, they should perform at a very high rate. Most of the EEPROMs in the market today have WRITE/ERASE cycle times of 10ms, as against 150-200ns for dynamic RAMs. Hence a drastic improvement in technology of EEPROMs must take place if the EEPROM market is to broaden. However, EEPROMs are expected to take over from UV EPROMs in the near term.

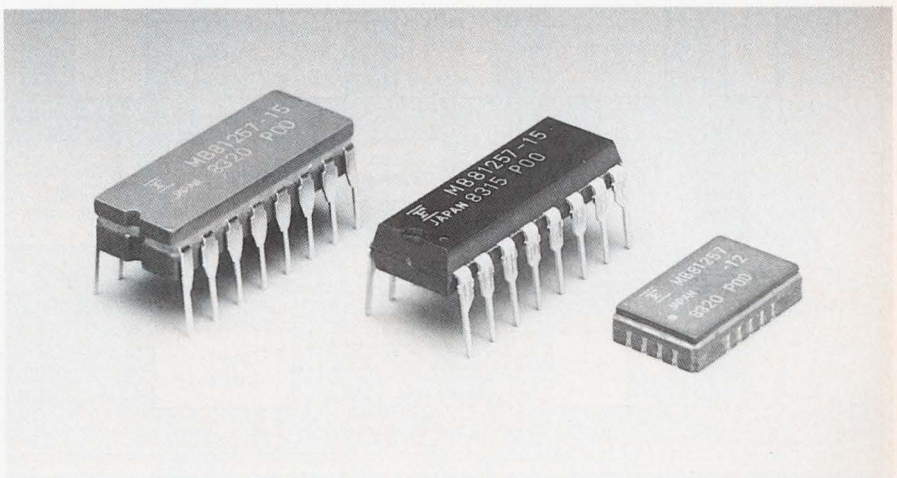
Dynamic RAMs have established themselves in applications requiring fast-processing and large memory, and today, they are used both in personal computers and large computer systems. The advent of 256K dynamic RAMs would further improve the market. The low cost associated with the device is largely responsible for its success. Dynamic RAM fabrication techniques are well-advanced to offer these high density chips. In terms of speed, however, static-RAMs (35-50ns) prove superior to dynamic RAMs (150-200ns).

When users are less concerned with space and cost than with speed and reduced complexity, static RAMs prove a viable alternative. Simpler to design with than dynamic RAMs, statics are far behind dynamics in terms of capacity.

Applications which involve use of graphic displays require a high memory system bandwidth. The bandwidth of the memory system is defined as total number of bits delivered from a memory in a given time span. Bandwidth may either be improved by operating the memory system in a nibble mode or by incorporating a static column dynamic RAM architecture. Both are applicable to the generation of high-speed serial bit streams for video display systems.

A considerable part of the cycle time is the memory access time. To reduce this, the systems can be supported by cache memory, that sits between the CPU and main memory. The cache contains a copy of previously selected blocks of main memory for faster reaccess to data and instructions. Design criteria for implementing include the technique of how cache is mapped to main memory, the number of words (block size) transferred from main to cache memory as a result of a miss, the number of locations available in cache for a given word in main memory to be written, etc. In cache-oriented systems, it is desirable to fetch the addressed word first so that the CPU can continue and then fetch the words. Nibble mode supports this type of operation because the four word block consists of the addressed word and the other three words as neighbors.

The nibble mode scheme is implemented by INMOS IMS 2600/Fujit-



Fujitsu's MB 81257 256K DRAM.

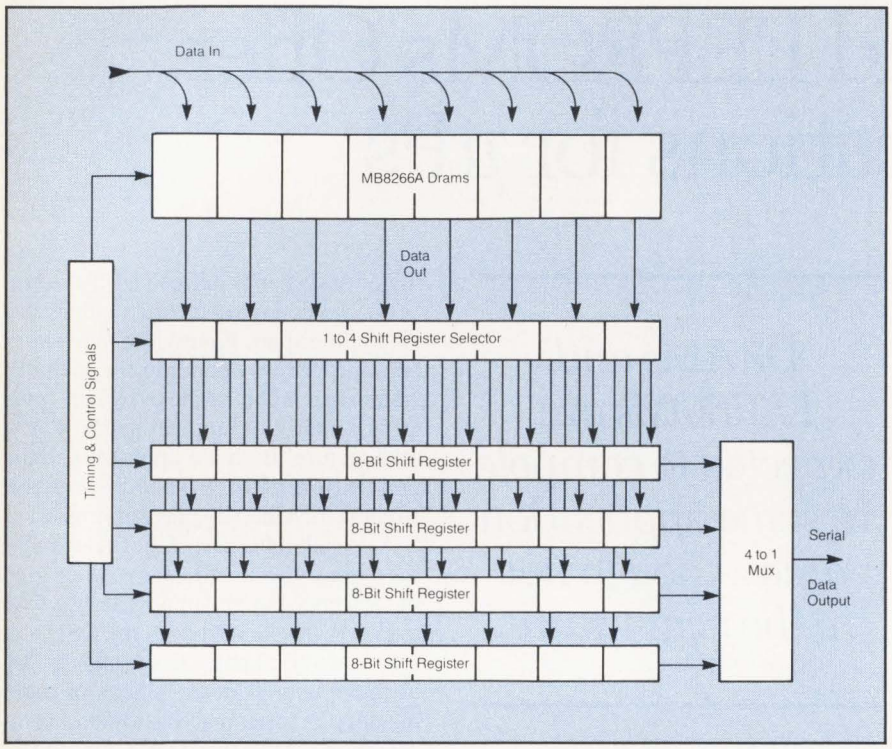


Figure 1: Fujitsu's MB 8266A operating in nibble mode provide a high speed serial output for video display systems.

The problem that is associated with RAMs is that they are volatile.

su's MB 8266A. The nibble mode improves memory bandwidth by using data bursts – moving data in blocks instead of single words. Fujitsu's MB 8266A obtains data bursts by using an interleaved memory system. This consists of two or more parallel rows of memory that are accessed in quick succession. By interleaving two memory rows each operating in nibble mode, a continuous data stream at a rate of one word every 60ns.

The nibble mode uses an on chip address counter to sequentially select up to 4 bits, compared with page mode which requires external column address for each bit that is accessed. Although nibble mode is less complex to implement than page mode, page mode operation is not limited to 4 bits per cycle – up to 50 bits per cycle is possible.

To generate high speed serial bit stream for video display systems, eight MB 8266As are used with each operating in nibble mode with each successive byte of data loaded into its appropriate shift register. The shift registers are then unloaded serially to form a data stream with rates up to 12ns per bit (**Figure 1**).

INMOS' IMS 2600 is designed to interface to the IBM personal computer. The display format is chosen to be resolution compatible with the 640 × 200 format of IBM color graphics monitor adapter (**Figure 2**).

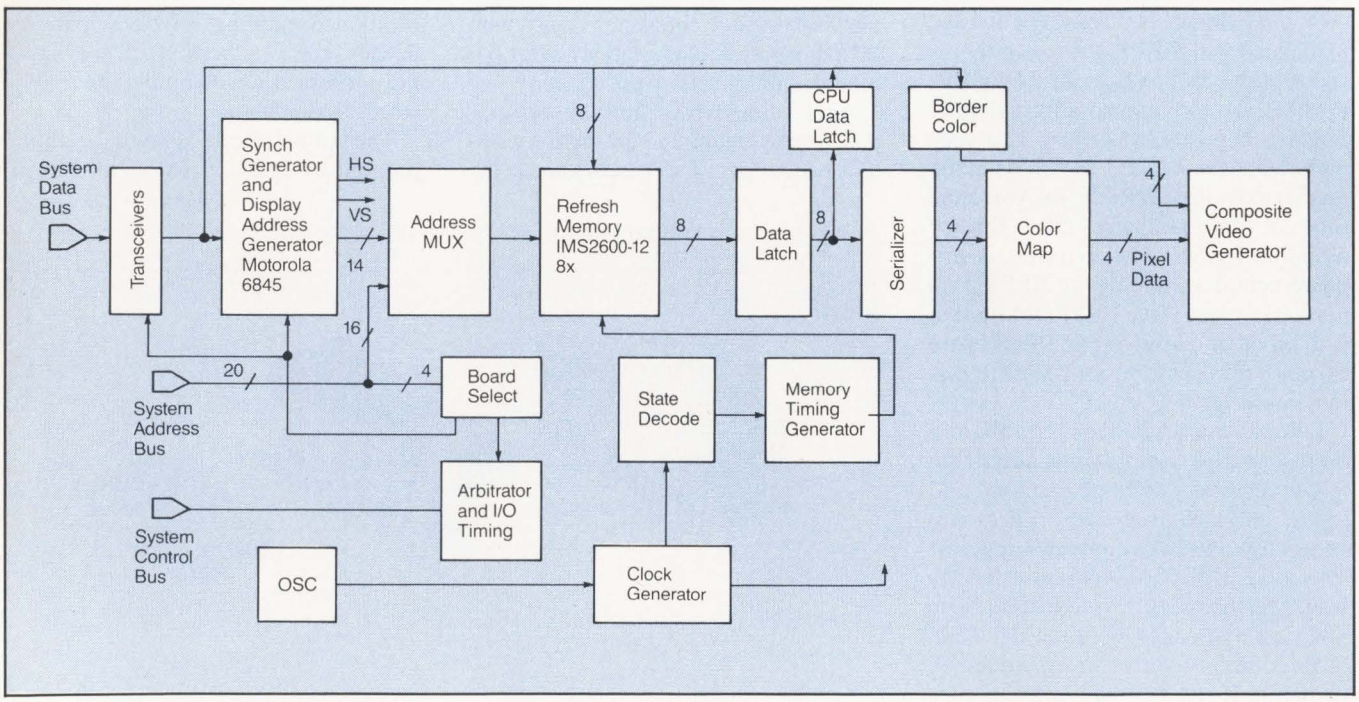
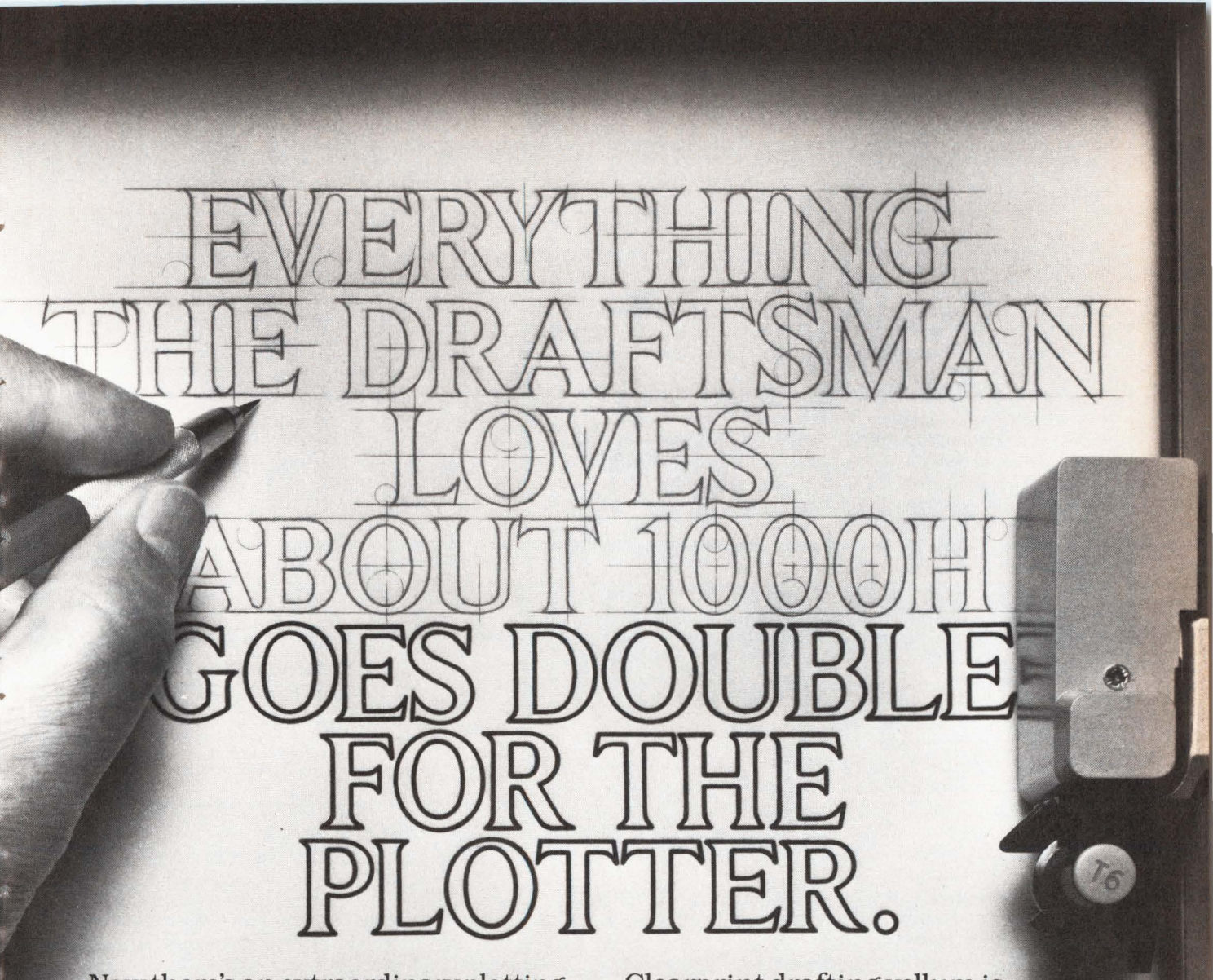


Figure 2: Block diagram of display board.



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256K DRAMs Have Arrived

The ISSCC held in February 1984 released, among other things, the much expected 256K dynamic RAMs. The contributors of the D-RAMs include Mostek Corp. (Carrolton, TX), National Semiconductor, (Santa Clara, CA), Fujitsu Laboratories, Mitsubishi LSI Research/Development Laboratory, Atsugi Electrical Communication Laboratory and NEC, all of Japan.

The 256K DRAMs are result of the efforts by the designers to realize the smallest die with the fastest access time and the widest operating margin. Implemented in high density polysilicon technology with NMOS transistor structure, the DRAMs operate at an access rate of 50-75 nsecs. The 256K DRAM from Mostek is designed by minimizing column access and row active time. The result is that the device allows 512 bits of page mode data to be read or written in a single RAS cycle at a cycle rate comparable to current nibble mode schemes.

The high density design of these DRAMs has resulted in use of almost the entire cell area for storage capacitance. This according to National Semiconductor results in improved signal strength, refresh time and soft error immunity. The other features of the 256K DRAM from National Semiconductor include a fast word line response without using silicides, ability to operate in nibble mode, etc.

Superior packing density is obtained by Fujitsu by incorporating stacked capacitor cell structure to give an improved integration. Organized in 256K × 1 bit the DRAM has the peripheral circuits designed with almost the same design rules for the cell. The capacitance coupled bit line cell structure allows up to 1 Mbit level DRAMs. The circuit inherent to the cell has a sense amplifier shared by two pairs of folded bit lines and is switched by row address to match the cell pitch (**Figure 1**). Row decoders and drivers are laid on both sides of the cell array, driving one of two word lines.

The 256K DRAM will be available in the second quarter of 1984. It's been speculated that the device will attain popularity at a rapid rate. The personal computer craze will probably be responsible for it.

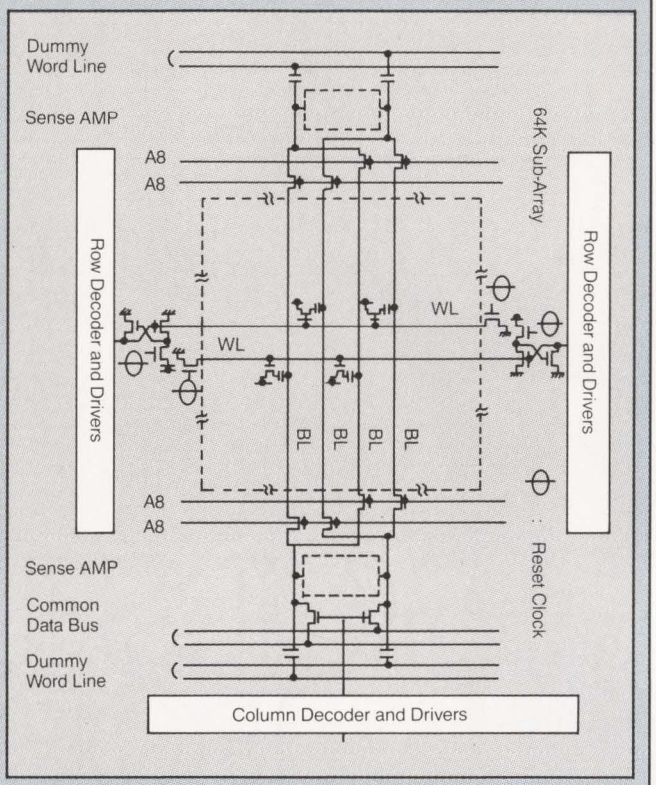


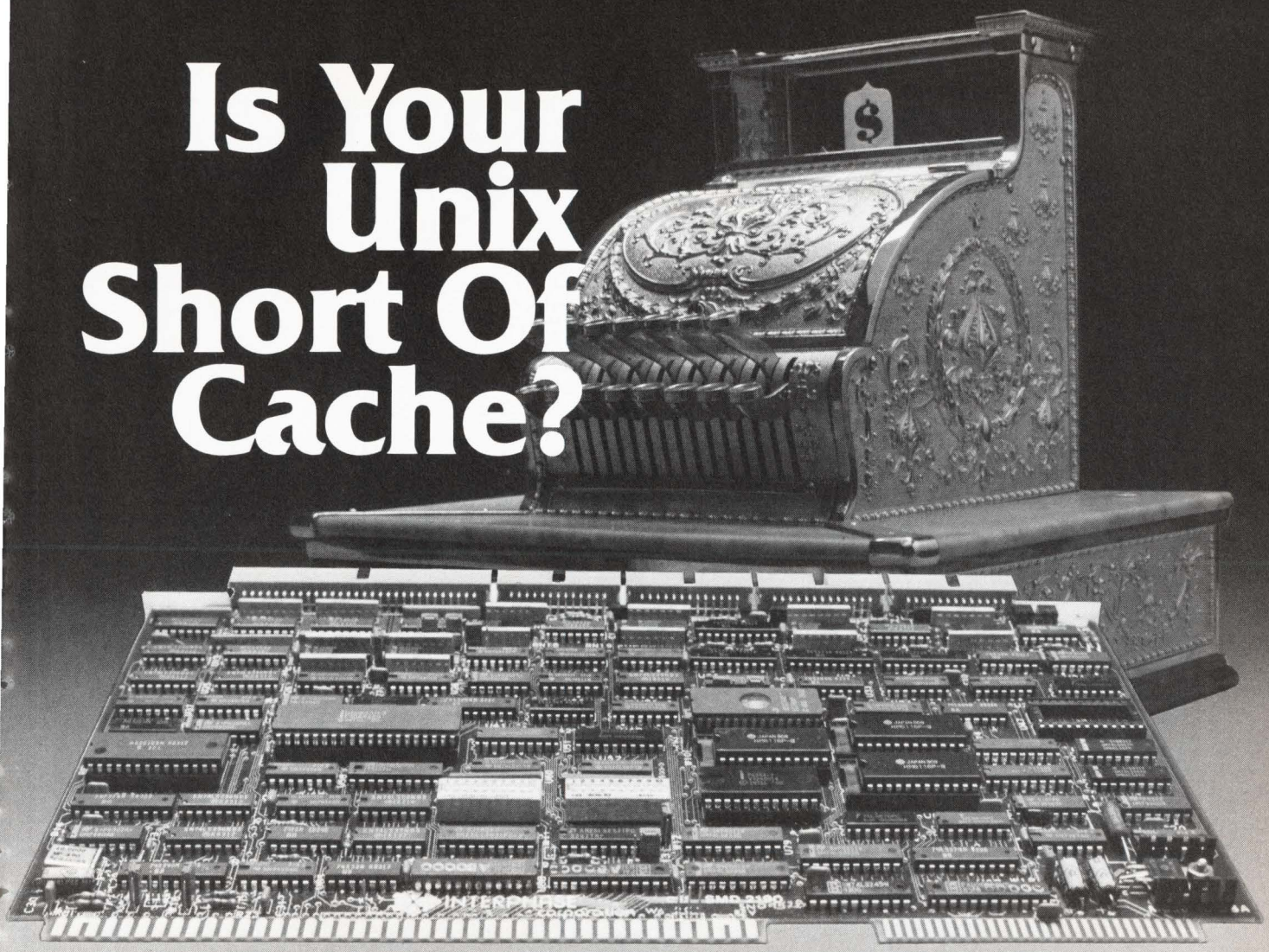
Figure 1: Fujitsu's peripheral circuit layout for CCB cells. A sense amplifier block includes precharge and active restore circuits.

INMOS' IMS 2630 (DRAM) is aimed at providing an economical alternative to SRAM interfacing in microprocessor systems. The 2630 eliminates most of the complications (usually additional logic circuitry) associated with DRAMs. The inherent speed of the IMS 2630 helps to eliminate the need for microprocessor wait states during memory operations. The odd/even interleaving of the 2630 enables dynamic memory refresh cycles to be hidden. The operation is based on partitioning of the dynamic memory into odd and even word address banks. As program execution accesses one bank, the unselected bank performs a refresh cycle. Additional components required for interfacing are a PAL16R4 and some 74LS series logic. In the case of IMS2630 an iAPX186 the interfacing components are PALIGR4 and on 74L5393 counter (**Figure 3**).

Dynamic RAMs have established themselves in applications requiring fast-processing and large memory and today, they are used both in personal computers and large computer systems.

The other memory organization for high speed, high performance applications such as mainframe memory, buffer memory, etc. is static column DRAM. Fujitsu's MB 8281 is implemented in N-MOS technology, organized as 64K one bit words. Intel's static column DRAM are in CHMOS-D III technology. The advantages of this technology over NMOS technology include higher density, speed, lower power consumption, noise immunity, etc. The 51C64 and 51C65 are in this category. The 51C64 operating in nibble mode allows all 256 data bits with a selected row to be randomly accessed at a high data rate. The graphics memory systems use a cycle stealing method. The graphic information (pixel data) is read from the memory at a rate greater than is

Is Your Unix Short Of Cache?



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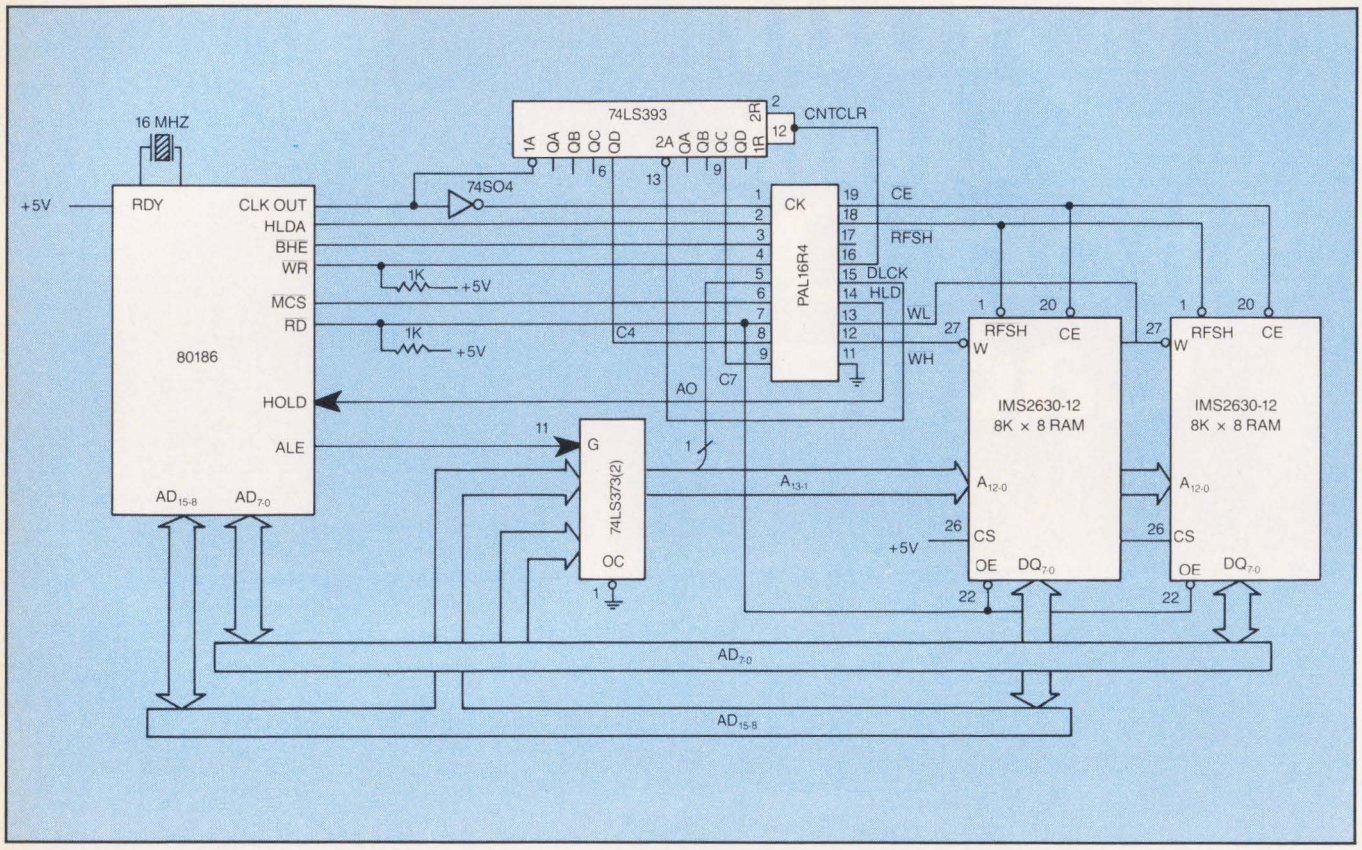

Figure 3: The INMOS IMS 2630 in iAPX186 System.

required to refresh the display. This information is stored in a video output register where the data is resynchronized to the pixel clock and is output serially from the registers at the required rate.

EEPROMS

One of the important expectations of a memory is to retain the data indefinitely with power off. This requirement is responsible for the outcome of ROM. However, a ROM is not accessible for data changes. The later innovations resulted in ultraviolet erasable programmable ROM. In-circuit programming, however, was not friendly until the invention of electrically erasable programmable Read Only Memory (EEPROM). The problem with EPROMs is that they required an ultraviolet source to erase the present data. The EEPROM also required a high voltage for erasing and reprogramming.

SEEQ's 5133 and 5143 are ultraviolet erasable EPROMs organized as 8k × 8 and 16k × 8 respectively. These devices may be programmed using an intelligent algorithm or with conventional 50 msec programming pulse. The intelligent programming is faster than byte programming. (The initial program pulse width is one milliosecond, followed by a sequence of one millisecond pulses. A byte is verified after each pulse.)

INMOS' IMS 3630 is a EEPROM which provides a solution to easy in-circuit programmability. Fabricated with INMOS' advanced NITROX process, the IMS 3630 allows in-system operation with a single +5 volt supply. The high voltage required for erasing programming is generated by the on-chip high voltage generator. Functionally the 3630 has commands to Read, Load byte, Program/Erase initiate and Program/Erase terminate.

Single chip microcomputers have started to emerge since last year. The chip houses a CPU, RAM and in-circuit programmable EEPROM. SEEQ Technology's 72720 houses a self-adaptive EEROM. The 5V 2K × 8 EEPROM program memory has provision to be expanded off-chip using the processor's full expansion mode. Also external EEROM can be programmed with the same instruction used to alter on-chip EEROM.

The memory market at present is occupied by RAMs (static and dynamic), ROMs, EPROMs and EEPROMs. Though each product in general, has its own market, the state-of-the-art has to be maintained to remain in the product competition. The rapid increase in the applications will result in volume of production of the memories to soar upward.

Many of these applications are likely to benefit from the considerable investment being placed on lower power CMOS devices by the major semiconductor houses, if this can be achieved at the performance, density and cost of their NMOS counterparts. □

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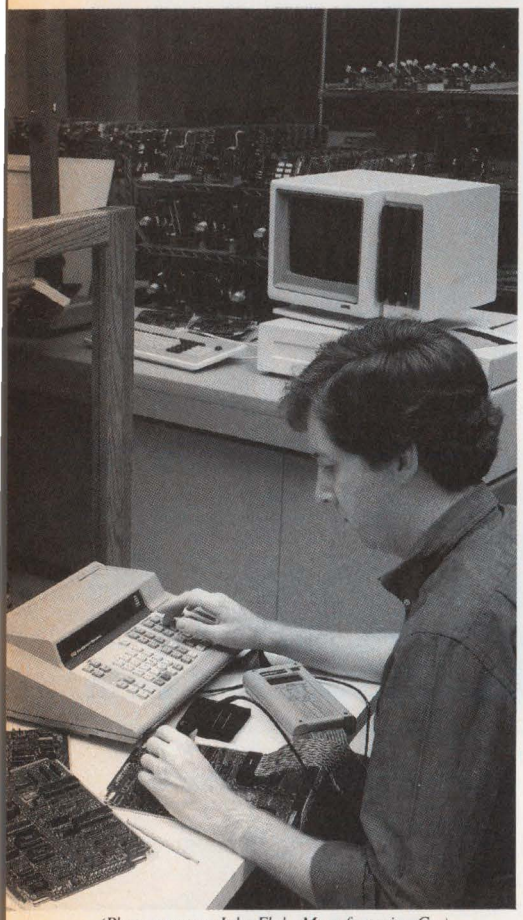
Bypassing In-Circuit Test Of Microprocessor-Based Boards



(Photo courtesy John Fluke Manufacturing Co.)

by Mike Major

The ever increasing sophistication of computerization has generally resulted in corresponding advances in productivity. However, the shadow that has plagued this growth has been an accompanying complexity, and, therefore, cost in test procedures.

In the early days of radio, tube circuits could be easily tested with voltmeters and signal generators. The arrival of transistors in the '50s and '60s made things a bit more difficult, but testing logic levels with a voltmeter was still straightforward. In the late '60s, transistors were combined into logic circuits which were simple to test, since the logic circuits were sequential. The signal put in one side would come out the other, or, if not, could be traced back to the fault, probably with an oscilloscope. In the '70s, sequential logic circuits were combined more and more with integrated circuits, starting out on single chips, for boards with many chips and many functions.

When microprocessors came onto the boards also, the testing problems began. The microprocessor talking to the many small chips that were, in turn, talking back made testing complex, and this bidirectional communication has been taking place at ever increasing speeds.

The late '70s saw the beginning of varied attempts to cope with this situation. One of the most established is reference board testing, in which identical patterns are applied to a known good board and the unit under test (UUT). If both outputs to a stimulus are the same, the UUT is known to be a good board. If not, a tracking procedure is evoked. Usually, the point in the loop that fails with the lowest test count coincides with the origin of the fault.

This process has been automated, and there are many automated test equipment (ATE) systems on the market. One of the largest manufacturers in this field is the John Fluke Mfg. Co., Inc. (Everett WA). To understand their philosophy, it's helpful to first review the three main approaches to board testing now in practice, namely continuity, in-circuit, and functional.

Test Methods

Continuity testing accesses every single point on a PCB, measures these points relative to each other and verifies that all traces are correct, with no opens or shorts. This type of testing is normally done on a PCB before components are installed, but advanced systems can go a step further and measure for correctness of installed components such as transistors, capacitors, and inductors. Since a continuity testing system must be able to measure every node on a PCB, the most practical interfacing technique requires a vacuum-actuated bed-of-nails fixture.

With a fast continuity tester and functional tester, testing averages typically reach 98%.

In-circuit testing does everything that continuity testing does, but more. Using the electrical technique of guarding, it isolates one component at a time and tests this device apart from the rest of the board. This tremendously increases the speed of testing parts. In-circuit testing, however, also utilizes the bed-of-nails interface, and, like continuity testing, does not verify the overall functionality of the UUT.

Functional testing uses a different interface. It starts from the board edge, stimulating the assembly into performing all of its functions. This interface is less expensive than the bed-of-nails technique for in-circuit testing, which requires the utmost precision and more wiring. Functional testing is also more comprehensive than continuity or in-circuit testing, in that it exercises every possible UUT function.

Despite the popularity of in-circuit testing in many quarters, Fluke bypasses this approach and instead advocates a combination of continuity and functional testing for optimum results. They maintain that this combination attains the quality of in-circuit testing with much greater cost-effectiveness.

The reasoning is that, typically, 70% of all faults will be found in the manufacturing defects categories of shorts, opens, component orientation, missing compo-

Mike Major is President of Major Enterprises, Yelm, WA

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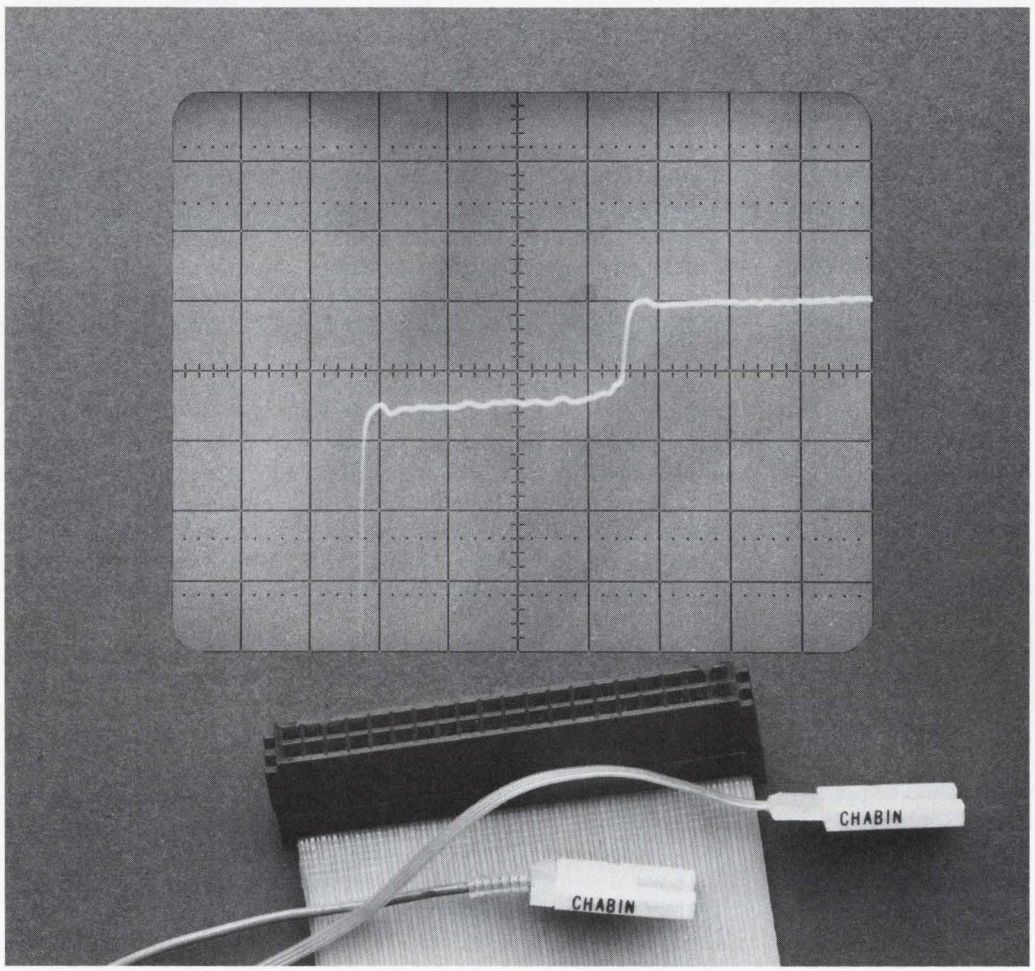

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nents, and wrong components. These can be handled by a continuity tester. The remaining 30% of all faults are functional failures, whether simple functional, speed-related, performance specification-related or load-related. Since these failures are recurring, the best solution, according to Fluke, is purchasing the two different systems to solve the spectrum of testing problems, rather than choosing a simple in-circuit tester.

The Automated Systems' Continuity Tester/Model 3200A is used to prescreen UUT PCBs and remove all manufacturing faults. The Model 3050B Automated Systems' Functional Tester is then used for testing and diagnosis of any dynamic faults not found in continuity tests. Even though the functional test detects and diagnoses any PCB fault, the continuity tester pinpoints the origin of almost any manufacturing fault more quickly. This means that the functional tester is used to diagnose faulty components only, resulting in less clipping and probing to find manufacturing faults on the UUT. Time and expense are saved in this process.

The continuity tester can determine only 50 to 70% of all faults, but at a speed of 10,000 points per second, is considerably faster than the scan speed of a circuit tester. Adding the 3050B functional tester, testing averages typically reach 98%.

A third product, the 9010A Micro System Troubleshooter, is a portable, low cost tester designed to both work in the same test environment described above and also serve as a handy service instrument.

Continuity Testing

The 3200A uses proprietary "QuickChip" scanning switch circuits to improve test speed. Each custom complimentary MOS chip has 32 pairs of intelligent solid-state switches. With only one software instruction, these switches check each test point's integrity with respect to all other test points.

An 8086 microprocessor-based 16-bit solo board computer controls the continuity tester. Backed by 64 Kbytes of RAM, the test processor detects opens, shorts and resistive leakage on bare and loaded circuit boards as well as backplanes, card cages, cables and harnesses.

Up to 65,536 test points are arbitrarily distributed among four test stations. Each station, which simultaneously tests the same or different programs, is equipped with a Remote Operator Control (ROC) unit featuring a 35-column fault printer, pass-fail lamps, data-entry keyboard with four-digit display, and a cycle-test key for easy fixture debugging.

When microprocessors came onto the boards, the testing problems began.

Interfaced to an off-line programming station, the 3200A generates and edits its own test programs. The programming station includes an Intel 8085 eight-bit microprocessor, CRT, keyboard and 64 Kbytes of RAM, plus dual eight-inch floppy disks. Half of the 2.5 Mbytes of storage on the disks is available to the user for test program storage.

System software selected from menu-driven displays can, using an optional "Learn" probe, assign discrete alphanumeric test-point names. The probe is placed in contact with a test point while the operator enters the assigned name on the keyboard. This permits simple random fixture wiring. In contrast, when using a wire list, test heads on most fixtures are hard-wired from an interface block to the spring-loaded probes, making changes difficult.

Different units under test, such as backplanes, card cages or harnesses, can be tested simultaneously on each station. Paddleboards consisting of an extender card with added-on scan module are inserted into motherboard connectors and daisy-chained together.

Using data derived from loaded PC boards, the 3200A pinpoints many errors resulting from missing, backward, and wrong ICs, transistors, diodes, and other components with low-voltage breakdown characteristics. These components are protected from damage because the stimulus voltage and the tolerance range are programmable.

The dual-threshold capability which assigns limit tests to opens, shorts, and leakage is also programmable. For testing loaded boards for opens and shorts, there is a programming range of 50 ohms to 10,000 ohms. For any other UUT, the programming range for opens is 5 Kohms to 100 Kohms, and for shorts from 50 ohms to 6000 ohms.

Functional Testing

A clue to the 3050B Digital/Analog Functional Test System's extensive testing capabilities is its unique system architecture, with three dedicated processors and a 16-bit microprocessor for overall system control. The three dedicated processors are the Pin Processor, which controls the operating modes of all Driver/Receiver pins in real time; the Auto Sequence Processor which generates, in real time, nine classes of automatic patterns; and the Test Step Processor that manipulates each step of the test program. This program, in turn, controls stored sequences and automatic patterns.

Automatic sequences can be generated at rates up to 4.99 MHz in internal control mode and 9.99 MHz in external control mode, while stored sequence testing can be performed at a data rate up to 2 MHz.

Using the known-good board as the test reference data base, identical stimuli are applied to the board-edge connectors on the reference board and the UUT. The resulting I/O data from both boards are then compared in real-time. No reference data or responses need be stored. Consequently, exhaustive test stimuli, as well as on-board software (stored in ROM or EPROM), can be used to comprehensively test and diagnose the board. In fact, faults on even complex PCBs can be automatically diagnosed to a faulty component, testing well past the nodal level.

Even advanced bus-oriented boards with self-clock microprocessors are testable with fault coverage approaching 100%. Both high-speed, real-time reference testing and Cyclic Redundancy Check (CRC) signature analysis are used by the tester. In addition, the 3050B permits optional parametric digital/analog measurements using the IEEE-488 compatible support module facility.

To test and diagnose complex board assemblies, the 3050B provides a pin masking facility which allows the masking of information on any pin or group of pins during any test step or group of test steps. This facility simplifies the programmer's

job when microprocessor-based boards must be test programmed.

The tester can interrogate a failed pin/node state at the time of failure. Operating at 5 MHz, the system can detect a failure, then halt to interrogate the pin/node, noting the failure condition logic state. This detection capability includes all 240 I/O pins and the clip/probe circuits.

A 30-character operator display panel and a two-color matrix printer with reversible character orientation are included with the system. The two-color printer outputs instructions; "within-limit" data are black and failure data are red.

Three software systems also come with the functional test system. The Test Management System (TMS) uses adapted ATLAS, an English-like language, for custom control of test and diagnostic routines and peripheral devices. An interesting aspect to TMS is its Principle Procedure, which is a user-defined sequence of code not related to testing the board but to managing the test of the board.

The Automatic Diagnostics Software (ADS) confirms the quality of the test program, for both the manager and the programmer. One feature is "leapfrogging", a way for the test engineer to add his intelligence to the test program. With leapfrogging, he can start in the middle of the board, as opposed to only the edge.

The Automatic Fault Emulation (AFE) offers state-of-the-art, high-resolution PCB diagnostics, including the emulation of hard and soft failures, the calculation of both stimulus and fault coverage, and the highlighting of circuit areas for test improvement.

Service/Test

While the 3200A and 3050B are high volume testers, the new 9000 Series Micro-System Troubleshooter is a low volume production test and service tool for microprocessor-based systems. It has been introduced for people that can't afford a large scale tester, but also can't afford to be without an automated tool to help deal with ever increasing complexity. This is important now that microprocessors are being built into even low cost and low volume consumer products.

Unlike traditional board testers, the 9010A (the major model of the 9000 series) works from the microprocessor socket. It automatically learns the memory map of a microprocessor-based product, then uses this information to test similar products.

This memory map can be entered manually through the front panel keyboard or loaded to memory from a mini-cassette or via the optional RS-232 interface. If the memory map of the UUT is not known, the Learn algorithm may be used on a known-good board to identify and store the RAM, ROM and I/O addresses.

Using these basic descriptors, the four built-in functional tests let the operator automatically check the electrical integrity of the microprocessor bus, the read/write capability of I/O registers, the data in ROM and the operation of RAM. There's also a fifth test, a more extensive RAM check, to locate pattern-sensitive failures. These tests cover perhaps more than 50% of the components on most boards, however this device troubleshoots only digital, and not analog circuitry.

If the problem lies outside the kernel, the troubleshooting functions isolate failures ranging from simple read/write data operations to automatically generated patterns such as walking ones/zeros and digitally incrementing ramps. They can be repeated, looped, continued or stopped under the operator's control. Once off-the-bus logic has been stimulated, the troubleshooting probe can be synchronized to track the failure to its source.

This troubleshooting tool is designed for the technician unfamiliar with the complex technology on which today's products are based. Since nearly everything is focused on the microprocessor, it can mimic basic read/write functions and so convey its probe/pulse activities to the operator in an exceedingly user-friendly fashion.

Market analysis shows that whereas the market for signature analysis over the next few years is about $15 million, the potential for low-cost, easy to use testers is ten times that much.

Perhaps the same forces which are minimizing computerization complexities for end users might also do the same for testers. □

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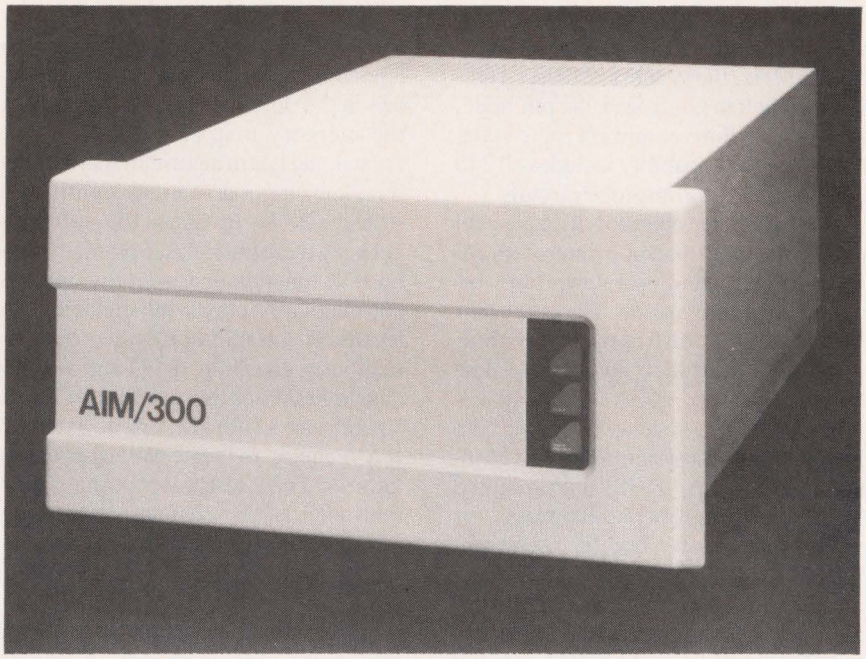
New Controller Technology Enhances Disk Access Performance

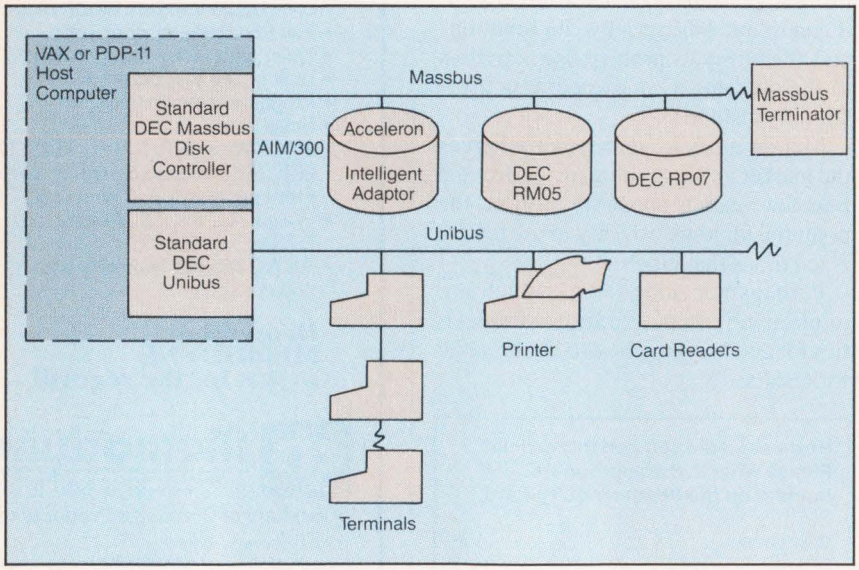
Disk drive data storage performance has become a crucial factor in computer system throughput and response time. Recently, Acceleron introduced a high speed disk controller technology that can be used to greatly reduce disk access time, a major component of disk performance. This new technology is expected to profoundly simplify both the management of present computer systems and the design of new computer and disk architectures.

Acceleron has developed the concept of on-line automatic data relocation (patent pending), refined it and implemented it in a high performance Winchester disk drive, the AIM/300™. It is the first production disk drive to combine proprietary, high speed data relocation with normal systems operations in a manner completely compatible with standard disks available on Digital Equipment Corporation's PDP-11 and VAX computer systems. The drive consists of a 315 (256 formatted) Mbyte Winchester disk with an embedded single board MASSBUS adapter containing the logic and semiconductor memory necessary to both emulate a standard DEC RM05 drive and accomplish its own performance mission. The rack mountable drive can be attached to a standard DEC MASSBUS controller such as an RH70 or RH750 along with standard DEC disk drives. It is transparent to both the standard DEC and Unix operating systems and stand alone utility software in the sense that no alterations in this software are required. In addition, the AIM/300's relocating capability does not require any special power failure or recovery precautions because the data and their physical locations are always stored on the magnetic media of the disk itself. In cases of power failure, these locations are recovered by the AIM/300 during its normal power-up and self-test sequence.



The AIM/300 high performance Winchester disk drive.

All of the data accessible at a single physical position of the actuator is commonly called a "cylinder". Even during periods of heavy system utilization, the AIM/300 can relocate two cylinders of data to each other's position on the disk in 5.3 seconds including the time spent read checking the data bit by bit for absolute integrity. After relocation to adjacent positions, the seek time between two actively used cylinders can be reduced to 3.6 milliseconds from a typical "arm contention" seek time of 29 milliseconds. The AIM/300 also employs high speed caching. Both standard and look ahead algorithms are used during periods when the semiconductor memory is not being used for relocation. Standard caching is used to put commonly used, high activity data in the fast semiconductor memory. Look ahead caching is used when sequentially read data make anticipatory retrievals from the magnetic disk to the semiconductor profitable. If a subsequent access request is within the semiconductor memory, the data can be accessed in less than a quarter of a millisecond. Both single and multiple blocks of data can be transferred at up to 1.2



Acceleron's AIM/300 combines proprietary, high speed data relocation with normal systems operation.

Mbytes per second from the magnetic media and 1.6 Mbytes per second from the semiconductor memory.

The AIM/300's transparent relocation capability, called DYNAMIC DATA RELOCATION™, is specifically designed for disk I/O bound, heavy transaction oriented computer systems. It is more than the simple relocation of high usage data around the center of the disk. DYNAMIC DATA RELOCATION™ incorporates sophisticated statistical forecasting techniques and selection criteria so that the movement of data can be made quickly to the most advantageous positions on the disk.

In the event of power failures, the AIM/300 automatically recovers the correct physical locations of the logical data from information stored on the non-volatile disk media when the system power is restored. Normally, the AIM/300 utilizes its semiconductor memory for high speed caching and read look-ahead buffering. In high usage periods when two or more users are extensively contending for the use of the disk, the AIM/300 will additionally relocate the appropriate data in order to reduce the average access time.

The MASSBUS adapter within the AIM/300 incorporates a single proprietary bit-slice microprocessor with an instruction cycle time of 160 nanoseconds. The high speed of this advanced bipolar microprocessor is required to meet the performance demands of a unique, high-level language and a multi-tasking operating system which are resident on the adapter itself. The adapter software implements all of the performance and compatibility features of the AIM/300 as well as providing automatic data error detection and correction, and the transparent handling of media flaws on the disk. The software also supports automatic adapter and disk self-tests, and front panel optimization selection.

The DEC MASSBUS was selected as the most appropriate means for the attachment of the AIM/300 because it is the highest speed disk transfer bus available to both PDP-11 and VAX computers. Use of the MASSBUS also ensures that there will be no interference with the operation of other system devices such as terminals and tape drives. The high speed bit-slice design of the AIM/300 adapter can be easily and inexpensively adapted to different data buses, processors, and, most importantly, to multiple disk drives with multiple disks. Similarly large systems can now fully utilize smaller numbers of large capacity disks without the purchase of additional disks to avoid arm contention. Most importantly, present system managers can accomplish the task of disk subsystem optimization by simply making sure that data files are loaded within logically contiguous areas of the disk using standard system backup and restore facilities. Related files which formerly had to be placed on several disks to avoid arm contention can now be placed on one disk for convenience, security and logical integrity without sacrificing performance.

Write 233

– Richard Scott, Acceleron, 2356 Walsh Ave., Santa Clara, CA 95051

Power MOS FETS Speed Up Horizontal Sweep

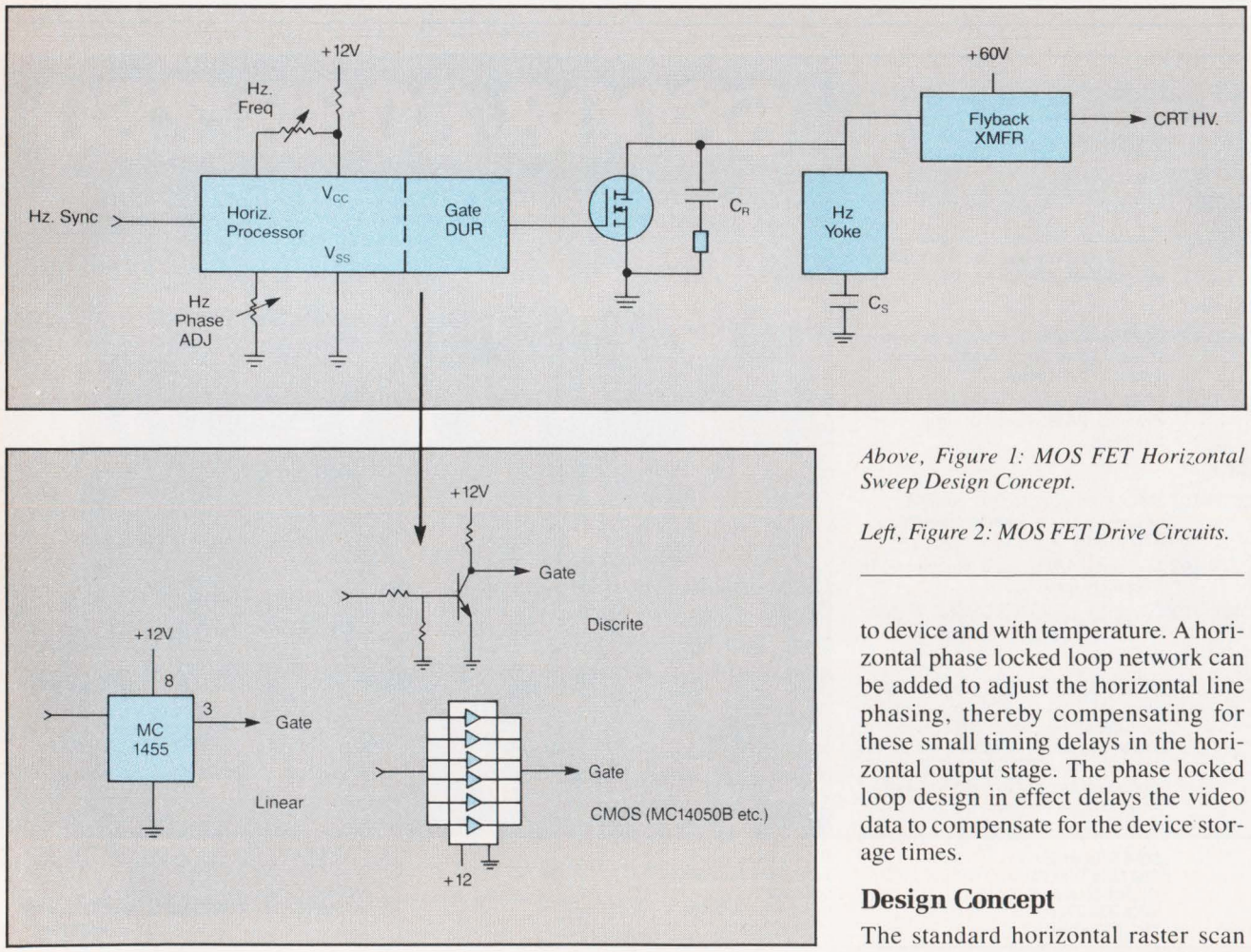
High resolution computer CRT display terminals require faster horizontal sweep rates than the standard 15 KHz rate used in low resolution monitors. A bipolar power transistor has been the traditional unit for driving the horizontal output stage, with the power MOS FET not considered because of voltage limitations and pricing. However, this is changing rapidly as new power MOS FETS are being introduced monthly along with price reductions. The high voltage power MOS FET offers many advantages over power bipolar transistors, and is becoming more economically justifiable for certain types of high frequency switching applications, such as high resolution video monitors.

The power MOS FET can be used to control high frequency CRT sweep designs with a very simple voltage drive circuit as compared to the complex bipolar current drive circuit. The power MOS FET drive circuit does away with the horizontal driver transformer stage along with the need for base current wave shaping networks. Also, the horizontal output MOS FET design offers increased reliability and faster switching times than similar bipolar designs. The power MOS FET design can be driven from a CMOS IC, does not require critical parameter screening, does not exhibit storage time, and does not require a phase locked loop to monitor the retrace voltage pulse for correcting device-induced timing errors.

Design Review

A key design consideration for a CRT raster scanned system is the turn-off response time of the horizontal output device. In a 30 KHz horizontal scan circuit, the power MOS FET horizontal output device will track to within 100ns of the horizontal oscillator output pulse. A bipolar transistor may be able to switch off in a time of 100ns or less with appropriate base drive design, but due to the bipolar's inherent minority carrier operation, the bipolar will still exhibit a storage turn-off time of several hundred nano-seconds. This is due to the saturated mode of operation in the bipolar output transistor. The base drive must be set to insure that the device is fully switched on, which requires that the bipolar output device be driven into the saturation region. Therefore a typical saturation time delay of 800ns or 2.4% of the horizontal line period at a 30 KHz rate, is added to the retrace time period.

Adding to the problem is the fact that the 800ns nominal storage time is not a fixed constant; it changes from device to device and with temperature. A horizontal phase locked loop network can be added to adjust the horizontal line phasing, thereby compensating for these small timing delays in the horizontal output stage. The phase locked loop design in effect delays the video data to compensate for the device storage times.



Above, Figure 1: MOS FET Horizontal Sweep Design Concept.

Left, Figure 2: MOS FET Drive Circuits.

Design Concept

The standard horizontal raster scan

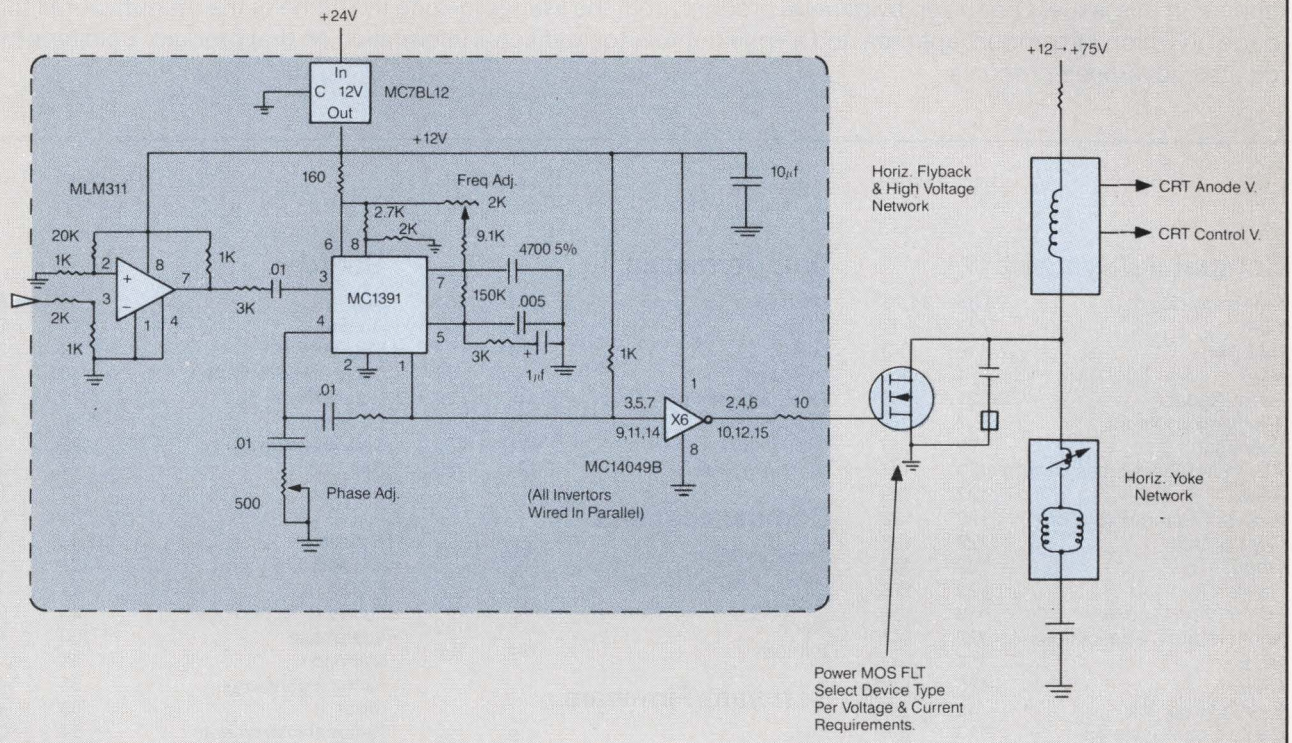


Figure 3: MOS FET Horizontal Circuit.

system is used in this design, that is, the horizontal yoke and flyback transformer are both controlled by one input device. In effect the horizontal yoke inductor is in parallel with the flyback transformer when calculating the total inductance switched by the power MOS FET. The block diagram of the design concept is shown in **Figure 1**. The horizontal drive signal can be supplied from either a free running oscillator or the internal computer logic. There are several horizontal processor linear integrated circuits available, including the Motorola MC1391. The problem is that none of these devices is presently designed to drive a MOS FET power unit directly; some type of an interface or buffer circuit is required. Three power MOS FET drive circuits are shown in **Figure 2.**

Circuit Description

The design presented in **Figure 2** eliminates the driver transformer and driver transistor plus associated passive components which would be required with a bipolar horizontal output device. A MLM311 comparator is used to invert and level shift the incoming positive going horizontal synchronization pulse. The comparator output is AC coupled to the MC1391 horizontal processor. the MC1391 consists of a phase comparator and voltage controlled oscillator with adjustable duty cycle. The phase comparator of the MC1391 is connected to the incoming conditioned horizontal synchronization pulse and the output of the MC1391's internal oscillator. An error voltage is applied to the oscillator timing control voltage to lock the external synchronization pulse to the oscillator. The duty cycle of the MC1391 oscillator output is set to provide a 63% "ON" time to the power MOS FET gate.

Essentially, the prime requirement for driving the power MOS FET for this horizontal scan output design is to insure sufficient gate on voltage and a fast turn off transition. Since the power MOS FET has a high gate input impedance, the gate voltage requirement is easily met with little wasted power. The off transition requires that the power MOS FET's internal 1000pf gate capacitance be discharged very quickly. This is accomplished by using a single hex CMOS inverter with all the gates wired in parallel. As mentioned before, other devices can be used to drive the MOS FET.

Summary

A high frequency horizontal MOS FET design has been demonstrated that uses off the shelf components. Since the power MOS FET is a majority carrier device, it does not suffer from second breakdown nor storage time. The second breakdown is a critical parameter for the reliability of the horizontal output device. The power MOS FET offers outstanding performance in this area, making it a good candidate for a high performance CRT sweep output design. A small scale integrated circuit can be used to drive the power MOS FET. This IC could also contain the horizontal processor function. By eliminating the transformer driver stage, system costs are reduced, reliability increased and the monitor's power consumption lowered by 1 to 3 watts.

– by Richard Valentine, Strategic Marketing, Motorola Inc. Semiconductor Products Sector. **Write 230**

Product Index

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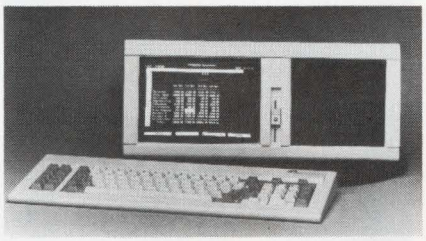
COMPUTER SYSTEM

Based on 37.5 Mbyte NuBus

The Nu Machine, a computer system, is based on the 37.5 Mbyte NuBus and is suited for applications requiring multiple or special purpose processors. The Nu Machine may be configured with a 68010- based processor with cache memory and/ or user-designed processors, and features a UNIX-based operating system, high resolution graphics display, mass storage peripherals, and a MultiBus subsystem. The Nu Machine is supplied with a 10 MHz 68010 processor with 4 Kbyte, 45 cache memory, and a memory-management system implemented in hardware. The NuBus supports 32-bit data transfer and addressing and can support future 32-bit microprocessors. The processor-independent NuBus also allows systems to be designed using other standard microprocessor families or special-purpose instruction sets. It has an 800 × 1024 pixel 15-inch 60Hz non-interlaced black-and-white display and bit-mapped graphics controller. Two Winchester disk storage systems are available; a 474 Mbyte Winchester disk subsystem with 18 msec access time and an 84 Mbyte disk with 20 msec access time. For disk backup, 1/2″ streamer and 1/4″ cartridge units are available. The NU Machine is offered in two configurations. Prices are $36,240 and $53,470. **Texas Instruments,** Dallas, TX **Write 145**

PORTABLE MICROCOMPUTER

80186-Based



The Transportable Solution is a transportable version of Pronto Computers Series 16 80186-based microcomputer. The System combines an 8-MHz 80186 processor with a proprietary bus, and operates under the MS-DOS 2.11 operating system. The microcomputer has applications in graphics and telecommunications and contains 256K RAM and 36.1 Mbytes of formatted storage. The system includes serial and parallel I/O ports, a clock calendar, and 16K ROM with system diagnostics. Price is $3,950. **Pronto Graphics,** Torrance, CA **Write 133**

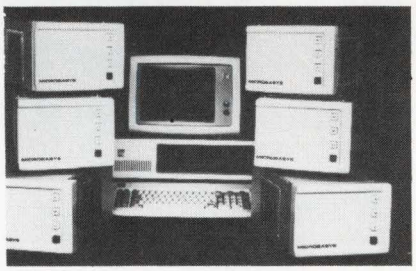
CAD/CAM SOFTWARE

For Mechanical and Intelligent Applications

Mechanical Application Software is a combination of the mechanical and schematic entry applications software modules, running on Telesis hardware. Users may create a standard symbol library and drawings are stored on either disk or magtape. The mechanical software module features a 2D floating point database which provides seven digits of accuracy. The system allows users to define drawing scales, to create real-time construction lines across the full bit map, and to momentarily remove designated lines from the display. The system draws solid, thin, break, and user-definable center lines, as well as ellipses, and it generates dash, phantom, and cutting line fonts in real-time with fixed pixel ratios. The system's dimensioning complies with ANSI standards, and it can be executed with either a single automatic command, or a set of three commands. The intelligent schematic application module automates the schematic design process and includes a logical design rules check program. **Telesis,** Chelmsford, MA **Write 127**

DISTRIBUTED CONTROL SYSTEM

For Hostile Environments



Microbasys is a SBC-11/21 based distributed control system that can be hosted by the IBM PC and DEC Professional personal computers as well as by VAX, DEC 11's and larger Adac systems. The hardware/ software package can be located in hostile environments in or close to the work area. It provides real-time measurement and control capabilities in stand-alone or distributed network applications. The software, I/O BASIC, is pre-programmed for I/O functions and presents a code for user communications with A/D inputs and outputs and concurrent I/O operations and program execution. The operating system and higher level language intelligence for Microbasys is resident in PROM on the SBC-11/21 CPU. Included in the architecture are a DEC SBC-11/21 Falcon CPU and an 8 Kbyte battery-backed CMOS RAM board. **Adac,** Woburn, MA **Write 139**

CAD SYSTEM

16 Mbytes Addressable Memory

CADalayst 200 is a turnkey CAD system for drafting illustrating and engineering applications. The system has a 32-bit parallel processing architecture and supports 16 Mbytes of addressable memory, has a vector refresh display, and choice of light pen or data tablet. The 200 can field upgraded to other CADalayst models. The system can support peripherals such as electrostatic and pen plotters, laser printers, telecommunications equipment, CRT phototypesetters, and digitizers. Price is $50,000. **Information Displays,** Armonk, NY **Write 138**

PORTABLE COMPUTER

With Built-In Printer

The PC Traveler is a portable computer developed for technical and business professionals. It has an AC gas plasma display, with an 80 column × 25 line format. It uses an Intel 80186 16 bit CPU unit. The Traveler comes with a printer designed into the terminal. It prints 80 or 132 characters per line and supports multiple print fonts, character sets and dot addressable graphics. It has a 6.2 Mbyte cartridge disk drive and half height diskette drives are available. **Strategic Technologies,** Norcross, GA **Write 149**

GRAPHICS WORKSTATION

For VLSI And PCB Design

The Coloware systems 11/10 color graphics workstation was designed for applications in VLSI and PCB design. The system is comprised of a color graphics terminal with 1024 × 768 resolution, a detached keyboard, a 19″ color monitor and a DEC LSI-11 CPU with memory management. It includes a resident 5¼″ Winchester and floppy disk mass storage system. Optional graphic input devices include an optical mouse and an 11″ by 11″ data tablet with either a stylus or crosshair cursor. The workstation is compatible with Tektronix PLOT 10 software and operating system software includes Digital Equipment RT-11 and RSX-11M. It is also compatible with the applications software provided by vendors including ISSO, PDA Engineering, and Precision Visuals. Price is $25,995. **Advanced Electronics Design,** Sunnyvale, CA **Write 137**

MULTI-USER MICRO-SYSTEM

6 MHz CPU

The QDP-400 Multiuser TurboDOS system is a high performance multi-user system which features a 6 MHz Z80B CPU for the Master CPU and a Z80A CPU for each of the two to five individual Slave CPU's. The QDP-400 Master CPU has 256K of RAM with 128K for each of the user workstations. It is compatible with CP/M and MP/M application software. The QDP-400 is available with a six-slot, S-100 mother-board that accommodates double-height boards. It has 300 Mbyte hard disk storage and an 8″ floppy disk. Price is $9,995. **QDP,** Cleveland, OH **Write 143**

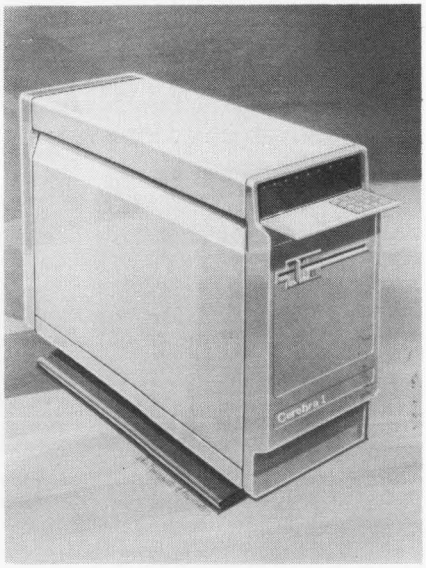
IBM COMPATIBLE COMPUTER

With Built-In LAN

The PCterminal functions as an intelligent terminal in an IBM PC network and has a built-in local area network. An optional floppy disk drive allows users to run programs locally, as well as over the network. The PC terminal has a monitor, keyboard, an 8088 microprocessor, both serial and parallel interfaces, four expansion slots for peripheral cards and 64K of RAM memory. The terminal runs under both IBM-DOS and a Santa Clara Systems' version of MS-DOS called SCS-DOS. Up to 16 PCterminals can be connected to one IBM PC or IBM XT in a network. Price is $1,295. **Santa Clara Systems,** San Jose, CA **Write 150**

MULTIUSER SYSTEMS

8 Kbyte Cache Memory



The Cerebra Systems are multi-user systems based on the National Semiconductor NS16032 32 bit microprocessors. The Cerebra I is a VAX-750 class systems, while the Cerebra II is a VAX-780 class system. Cerebra systems use Multibus and each system includes 8 Kbyte of 45ns cache memory. The Cerebra I has 2 Mbyte of main memory, 84 Mbyte disk storage, 16 lines of intelligent serial controller, and either cartridge tape or floppy disk for interchange/backup. The Cerebra II adds a second CPU with cache, 8 serial lines and an additional 1 Mbyte of memory. Price is $36,895. **Unidot,** Golden, CO **Write 146**

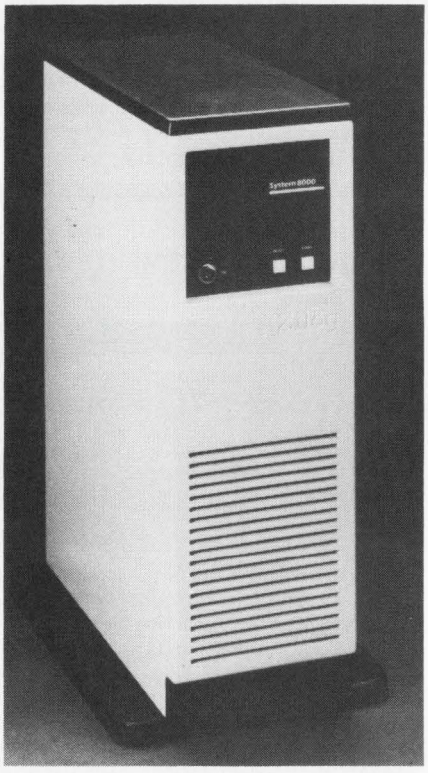
MICRO TO MAINFRAME SOFTWARE

IBM-Compatible

MegaFile is a filing system with relational data base functions and multiple spreadsheet capability for the IBM mainframe user. MegaFile is designed to run on mainframe systems using 3270-type terminals and when integrated with MegaCalc, MegaFile gains access to the memory capabilities of the IBM mainframe. A three dimensional matrix permits the simultaneous access, manipulation and merging of data from thirty spreadsheets. The data bases can be downloaded to IBM personal computers. **Megagroup,** Irvine, CA **Write 132**

SUPERMICROCOMPUTER

Supports Eight Users



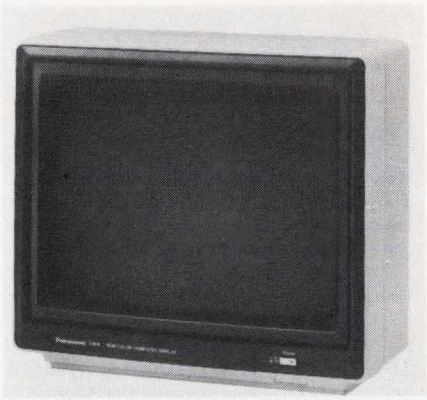
The Model 11-Plus offers 66 Mbytes of disk storage in a eight-user package. The Model 11-Plus has a 33-Mbyte Winchester disk drive with a disk-access time of 30 msecs. The system has 512 Kbyte parity memory and a 17 Mbyte tape cartridge for backup. Price is $18,950. **Zilog,** Campbell, CA **Write 141**

ERRATA

In the January, 1984 issue of *Digital Design*, in the article "The Design Of A High Performance Multibus Memory Board," the opening photo on page 78 was incorrectly labeled. The memory board is from Central Data Corporation not Control Data Corporation as the caption reads.

DISPLAY

With Reversable Character Background



By touching a key, the Model DT-H103 video computer display has the capability to reverse the color of the background and characters. The DT-H103 has an 80 character by 25 line screen which measures 10″ and has a resolution of 760 by 570 pixels. The display is compatible with Panasonic, IBM, Apple III and NEC personal computers with a 20-pin square connector. **Panasonic,** Secaucus, NJ

Write 134

DISPLAY TERMINALS

Emulate Tektronixs Graphics Mode

The Series TDV 2200S are editing/display terminals which feature and 70 Hz refresh rate and add-on communications controllers, which enable the terminals TDV 2200S to commuicate through packet-switched networks using the X.25 protocol. The series can be equipped with 56 Kbytes of memory and will store eight pages of data. They can transmit by character, page, block or line/field. A plug-in card turns the TDV 2200S into a bit-map raster screen display with 684 × 384 point resolution. This configuration emulates the Tektronix 4010 and 4014 for vector drawing and point plotting. The terminals are plug compatible with most terminals. Price is $1,875. **Tandberg Data,** Armonk, NY

Write 136

32-BIT COMPUTER SYSTEM

MC68000 Based

The Micro/32 is a 32-bit computer system that features a MC68000 micro-processor and the Regulus, operating system which accommodates all UNIX software. Regulus has user source compatibility with UNIX V6, 7 and SYSTEM III, and supports all UNIX kernel features, multi-key B-tree ISAM and VAX/PDP-11 cross support. The MDB MICRO/32 utilizes the Motorola MC68000 processor with 32-bit data and address registers, coupled with dual MC68451 memory managers having 64 segments of associatively mapped memory and 512KB RAM. The MDB-M32 has four asynchronous serial ports, two of which have modem control, and a parallel Centronics interface printer port. System memory can be expanded by use of dual size 512 KByte memory modules up to a total of 4 Mbytes. Price is $11,995. **MDB,** Orange, CA

Write 142

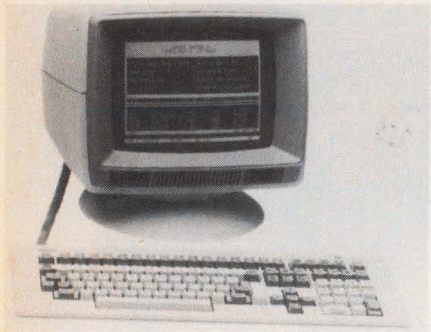
WORKSTATION

Documents Programmable Controllers

This PC workstation is designed for programmable controllers and consists of a desktop computer with a color monitor and printer. Documentation generated by the workstation includes texted ladder diagrams and customized drafting for controller equipment drawings. The stand-alone desktop computer includes a 16-bit processor and 512 Kbytes of program memory. It has a 16 Mbyte Winchester disk with a 5¼" minifloppy disk drive for data storage. Price starts at $21,000. **Gould,** Andover, MA
Write 147

VIDEO TERMINAL

With Two Display Memories



The ADM 12 conversational/block mode video display terminal provides a choice of 80 × 48 or 158 × 24 display memories. Its keyboard has 16 programmable function keys and six programmable edit and transmission keys. The ADM 12 has an 80 character per line × 24 line display and visual aids such as reduced intensity, underline, blink, blank and reverse video. **Lear Siegler,** Anaheim, CA
Write 135

GRAPHICS SOFTWARE

Multiwindowing Capability

Multiview is graphics and multiwindowing software that drives Momentum's OEM 32/4 workstation. The 32/4 has twin M68000 microprocessors; one dedicated to graphics, the other to data processing. The user can select 16 windows for concurrent graphics manipulation and processing. MultiView supports UNIX plot, spline and Plot-10 graphics, as well as the SIGGRAPH core and Momentum enhanced interfaces and libraries. Because of Tektronix emulation modules, the software is portable and upward compatible. Software updates do not require changes in hardware or firmware, and upgrades are available on floppy disk. **Momentum,** San Jose, CA
Write 131

CAD/CAM System

Access Customized Programs

The Advanced Graphics Workstation Model III is a 32-bit stand-alone graphics system which can also be linked in a local area network. The system has standard hardware and software interfaces for users to access third party software or write their own customized programs. The AGW III is based on Apollo Computer's 32-bit computer utilizing a bit slice processor. **Auto-trol Technology Corporation,** Denver, CO
Write 130

WORKSTATIONS

MC8000-Based

The HP 9000 Series 200 family of workstations have been upgraded with an MC68000 CPU, increasing their processing speeds. The HP-UX operating system for the Series 200 computers features HP Pascal and FORTRAN 77 compilers, a device-independent graphics library and extensions of the operating system taken from the Berkeley 4.2 version to UNIX. A "C" language compiler, command sets, intrinsics and utilities are included in HP-UX. The Motorola 12.5-MHz central-processor chip replaces an 8-MHz processor. The workstations have 16 Kbytes of cache memory and memory-management hardware for multi-user and multi-tasking applications. An upgrade kit is available to convert existing models to the faster processor and the HP-UX operating system. **Hewlett-Packard,** Palo Alto, CA
Write 126

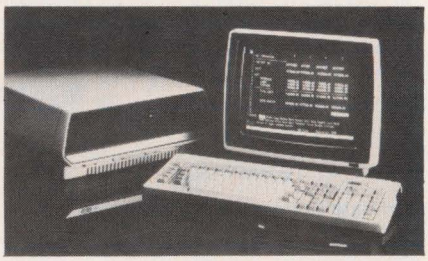
WORKSTATION

With 500 Kbaud Interface

The ICEM Ergonomic Workstation displays 200,000 transformed vectors per second and simultaneously can display 16 to 4096 colors. The workstation has a 1280 × 1024 pixel color graphics display with 60 Hz non-interlaced refresh, a separate alphanumeric display, keyboard, and data tablet. All units are compatible and provide a 3D display file with 512K to 2,000 Kbytes of RAM. A 500 Kbaud host interface links the Workstation to a Control Data CYBER 170 mainframe. Prices start at $30,000. **Control Data,** Minneapolis, MN
Write 128

SUPERMICROCOMPUTER

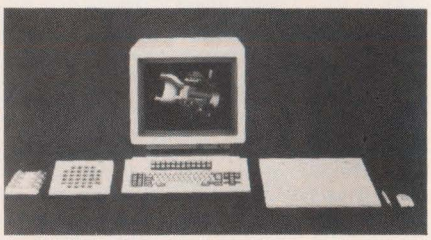
Accommodates Nine Users



The 986 supermicro accommodates nine users (10 RS232 ports), offers one Mbyte of main memory, and can be configured into a network using Altos' networking software. The system includes an integral port for twisted pair cabling, and will accept the forthcoming Ethernet chip set. The system's 8086 processor runs at 10 MHz, and utilizes two Z-80 processors to handle direct memory access. It has a Winchester drive with 45 msec access time and one Mbyte of main memory. **Altos,** San Jose, CA
Write 129

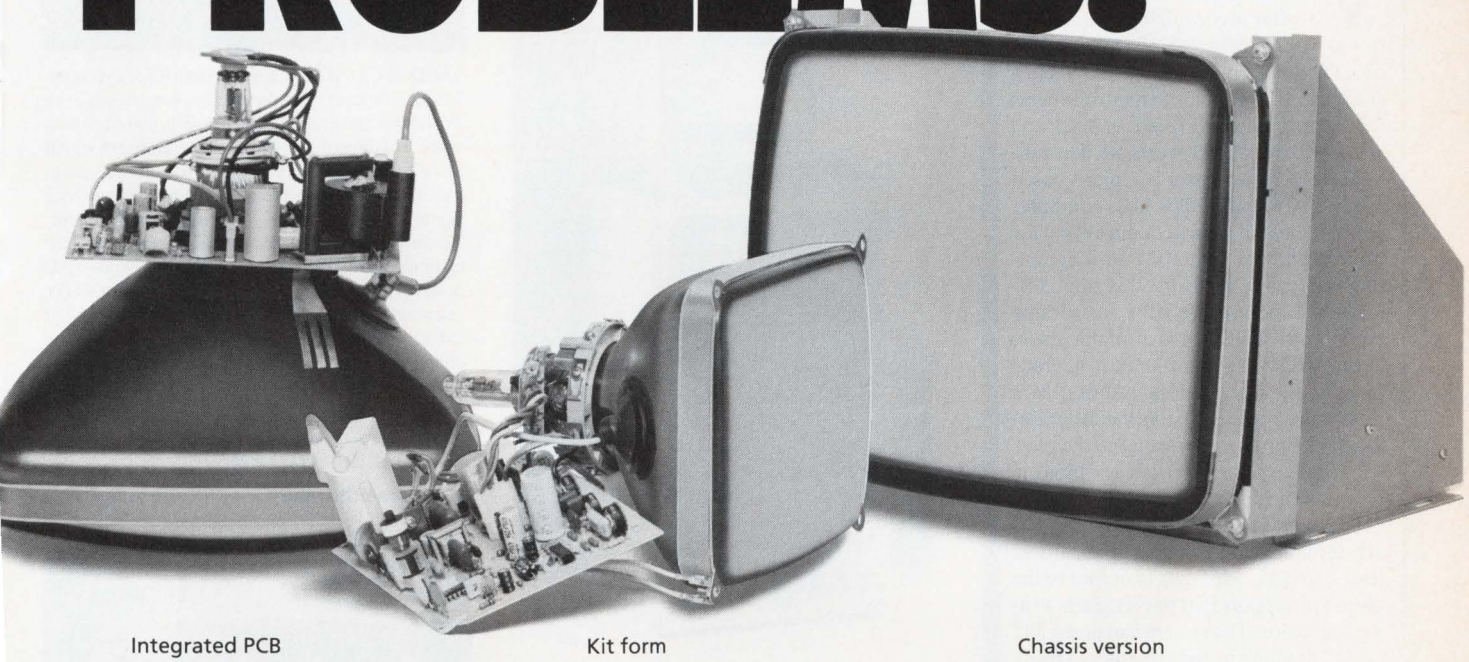
SOLID MODELING SYSTEM

For IBM 5080 Graphics Terminal



The SynthaVision solid modeling process has been enhanced to run on the IBM 5080 Graphics System, an interactive computer graphics terminal with monochromatic displays and graphics architecture. The system is the only solid modeler that is compatible with CADAM. Users can implement SynthaVision without additional hardware or software. Synthavision has applications in engineering design and analysis and features the ability to generate color shaded images of products before they are manufactured. **Mathematical Applications,** Elmsford, NY
Write 144

WE SOLVE PROBLEMS!



Integrated PCB

Kit form

Chassis version

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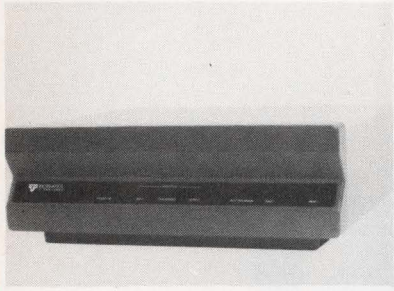
Write 26 on Reader Inquiry Card

PERIPHERALS

PLOTTER DISK DRIVE

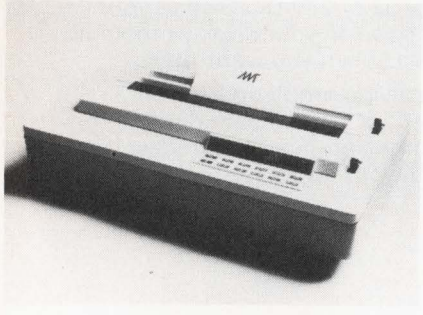
Plots Color In Eight Minutes



Versatec's random element processor and IBM on-line plotting controller are available with an optional 40-140 Mbyte 5.25" Winchester disk. The disk options enable the electrostatic plotting systems to handle longer, more complex plots in color or black and white with less CPU overhead. The random element processor is a micro-based accessory that offloads host computer data ordering and raster conversion for minicomputers. The IBM on-line plotting controller performs this same offloading function for IBM mainframe computers. The disk is available as an option with new systems or as an upgrade in existing installations. Acting as a raster data buffer, it spools the raster image for a high speed transfer to the plotter. On-line electrostatic color plotting requires the disk option and Versaplot Color Random software. Color elements are separated on the host, then transferred to disk. Plot data is output to the plotter to support four passes, each writing one color. The system can plot a 34" by 44" drawing in eight minutes; a black and white drawing in less than 90 seconds. Resolution is 40,000 points per sq. in. Price is $13,500 for the disk option. **Versatec,** Santa Clara, CA **Write 175**

DOT MATRIX PRINTER

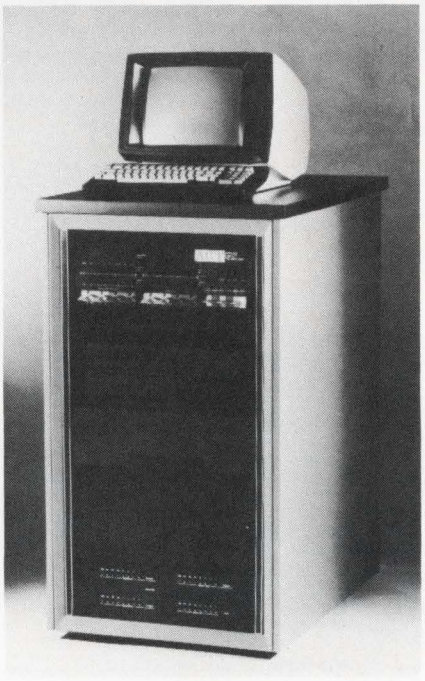
Three Print Modes



The AMT Printer has three modes of print quality to select from. In the letter mode output is printed at 45 cps. For data and high speed drafts, printing speed is 250 cps. For general documents a memo mode prints a 16 × 72 matrix at 100 cps. The AMT Printer supports multiple fonts and pitches and under software control, can change from font to font, or from alphanumerics to graphics. Documents using a mixture of fonts and graphics can be printed. With the color option installed, documents can be illustrated with color graphs and charts. Graphics dot addressability of 240 vertical by 480 horizontal dpi is available for 3-D graphics. The printer can also produce overhead transparencies. **AMT,** Newbury Park, CA **Write 164**

ANALOG TEST STATION

For Hard Disk Drives



The Analog Test Station for hard disk drives performs analog certification of head to media interface. Each ATS consists of a software-driven operator console and two test slots, allowing for the simultaneous analog testing of two disk drives. Two four-up slave devices can be added bringing the total number of parallel test parts to 10. The test station incorporates a menu-driven operator console and main test station which includes a 10 Mbyte Winchester hard disk drive and 1 Mbyte floppy disk drive. Price is $28,000. **Applied Circuit Technology,** Anaheim, CA **Write 159**

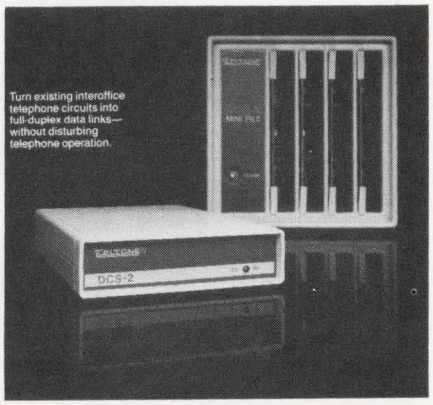
COAXIAL DOUBLER

For IBM 3274 Controller

The Coaxial Doubler is a connecting module that enables users of the IBM 3274 computer controller to add or move terminals without special tools, adjustments, or equipment. The doubler transmits signals from any two ports of an IBM 3274 controller over a coaxial cable which can then be shared by any two IBM 3270 peripherals. The doubler requires no external power. Prices is $490 for a pair of doublers. **Fibronics,** Hyannis, MA **Write 158**

LOCAL DATA NETWORK

9600 BPS Transfer Rate



The Data Carrier System transfers RS232-C compatible data over existing PABX voice circuits at an asynchronous speed of 9600 bps. The unit combines voice and data on the PABX pair, sending a signal to the centralized data equipment location. A termination card removes the data and passes the voice signal onto the PABX switching environment. Because data is directed to the centralized EDP equipment, telephone lines continue to operate if AC power is removed. The system is approved for PABX telephone systems. The network can be expanded to hundreds of data channels, and equipment can be changed without port adjustments. **Telthone,** Kirkland, WA **Write 156**

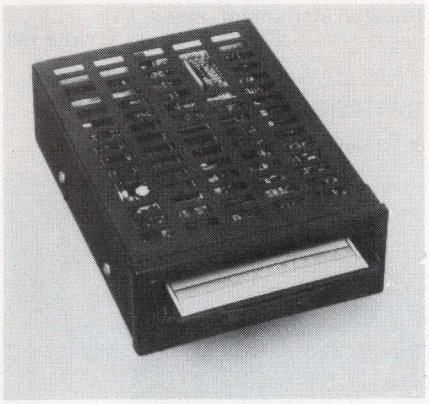
HARD DISK SYSTEM

10 Mbytes Storage

The DataSafe-16 is a Winchester disk system for Intel Intellec Series II, III and MDS-800 microprocessor development systems. It provides 10 Mbytes of formatted storage and three directories. Compatible with Intellec's ISIS-II operating system, the DataSafe-16 has 78,336 available blocks. Data transfer rate is 625 Kbytes/sec with an average access time of 85 msec. The Z80A microprocessor-based controller includes 32-bit ECC with transparent 11-bit burst error correction. The DataSafe-16 includes a Multibus adapter card which occupies one slot in the host chassis and conforms to IEEE 796 specifications. A print spooler option allows printing while programming. The 256K buffer holds 2000 disk blocks, or about 60 to 80 pages, and can be filled in five minutes. Prices is $6,500. **Winchester Systems,** Woburn, MA **Write 178**

FLOPPY DISK DRIVES

One Mbyte Double Sided Storage



Models 321 and 322 are microfloppy disk drives which use a 5.25″ interface and 3.25″ flexible media. The models have single-sided 500 Kbyte and double-sided one Mbyte storage capacities. The microfloppies have a track-to-track access time of six msec and MTBF of 12,000 hours under typical usage. Major components include a direct drive spindle motor and a lead screw head-actuator that records at 140 tpi. The drives are plug compatible with double-sided and density, 96 tpi, 5.25″ drives. Users can download 5.25″ software packages to the unit's 3.25″ diskettes with no modification. Prices are (321) $155, and (322) $190. **MPI,** Chatsworth, CA **Write 177**

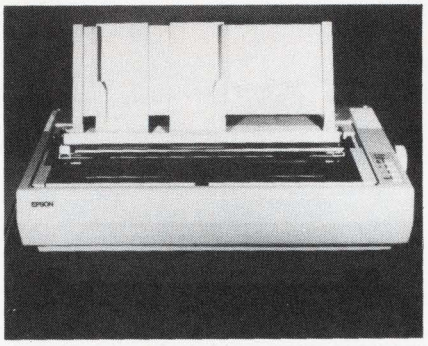
METRIC ELECTROSTATIC PLOTTER/PRINTER

Prints At 475 Lines/Minute

The Quadramet Series of printers/plotters print at speeds of 475 lines/minute and plot at 2.54 cm/sec. The writing head contains four offset rows of writing styli and during printing operations each dot appearing on the paper will overlap adjacent dots at 50%, increasing line smoothness. The 9000 Series uses a precision dynamic toning system, which gives each page 50 applications of freshtoner. The integral paper takeup holds 100 ft of completed plots and has a sensor which will stop the plotter if the area is full. It has built-in self-diagnostics and software programmed in FORTRAN. **Benson,** San Jose, CA **Write 166**

DOT MATRIX PRINTER

60 To 200 CPS Printing Speed



The LQ-1500 is a serial dot matrix printer with applications in letter quality correspondence, drafting and graphics. The LQ-1500 has a 24-pin head and printing speed that ranges from 200 cps to 60 cps. The 136-column printer has character sets comprised of 96 ASCII characters, 13 international character sets and 96 italic characters. The user can create any character or symbol which can be defined within a 37 × 24 matrix. Resolution ranges from 9 × 17 dpi to 240 dpi. Printing is bi-directional with logic seeking. Available interfaces are Centronics 8 bit parallel and RS232C and 488/GPIB. **Epson,** North Hollywood, CA **Write 165**

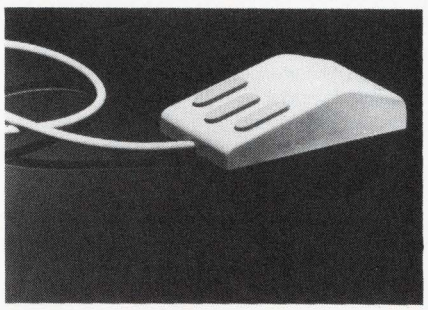
HARD DISK STORAGE

For Apple Macintosh PC

Mac Disks are hard disk storage systems designed for the Apple Macintosh PC which ranges from 5 to 32 Mbytes in storage capa ity. Mac Disk has applications in accounting and database management. Mac Disk is accompanied by Mac Link, a local area networking system that will allows 255 Macintoshes to share hard disk storage and other resources such as printers and plotters. **Darong,** Sunnyvale, CA **Write 173**

MOUSE

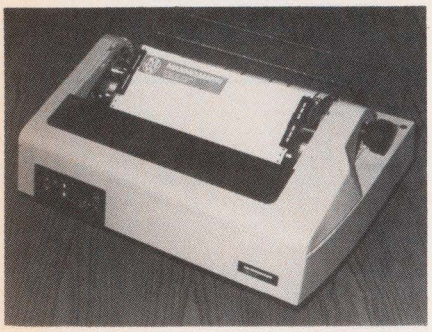
Requires No Adaptive Hardware



The Keytronic mouse can plug into a computer terminal's RS232 port, or if it is channeled through a Keytronic keyboard, requires no adaptive hardware. The mouse incorporates a solid-state strain gauge sensing element, rather than optical sensors or mechanical wheels or balls. The Keytronic mouse operates on any surface so no special pad is required. The Mouse will come in tandem with made-to-order keyboards for original equipment manufacturers' applications. **Keytronic,** Spokane, WA **Write 180**

SERIAL PRINTER

For Mini- And Microcomputers



The MT-440 is a serial dot-matrix printer for minicomputer and high-performance microcomputer applications. The dot-matrix printer runs at 400 cps in the draft mode and 100 cps in the letter-quality mode. The bar-code printing model runs at 270 cps. It has a tabbing feature that allows the print head to travel at speeds of up to 650 cps when bypassing blank portions of a line. The MT-440 family includes models for draft report and data-processing applications, letter-quality printing and bar-code printing. Four-color printing capability will be available. The MT-440 uses a 9x7 dot matrix for draft-quality print and an 18x40 matrix in the correspondence-quality mode. It prints at 10, 12 or 16.7 cpi. Full dot-addressable graphics capability is standard. Price is $2,395-$2,995. **Mannesmann Tally,** Kent, WA. **Write 181**

FULL-DUPLEX MODEM

Microprocessor Based

The R2424 is a microprocessor-based full-duplex modem that operates over the DDD network or two-wire private lines. The R2424 operates synchronously or character asynchronously at speeds of 2400 or 1200 bps. For alternate voice/data operation, a front-panel talk/data switch is included to allow calls to be answered manually with the telephone or automatically under the control of the data terminal eqiupment. The R2424 can perform such tests as analog and digital loopback, remote digital loopback, local self-test, and end-to-end self-test. Eleven front-panel LED's monitor the EIA interface status, test status, error detection and incoming calls. The R2424 is also available as an RV.22 bis for international applications. **Rixon,** Silver Spring, MD **Write 169**

FLOPPY DISK DRIVE ANALYZER

Utilizes Crystal-Based Oscillator

The MFX-500 works with all major floppy disk drives. It performs all mechanical and electronic test functions and calibration measurements without a scope. Calibration accuracy is provided by a crystal based oscillator, with the test results, measurement values and test program shown on a vacuum fluorescent alphanumeric display. All calibration operations can be performed without the use of an oscilloscope. Features include user specified tests, external printer port and RS232 port. The MFX-500 supports 8″, 5¼″, and 3″ series drives, single- or double-density, single- or double-sided as well as 48 or 96 TPI formats. Price is $2495. **Wilson Laboratories,** Orange, CA **Write 161**

FACSIMILE TRANSCEIVER

CCITT GII Compatible

The DataFax 2000 is a GII facsimile transceiver which is capable of communicating over private or public telephone circuits with any CCITT GII Fax machine. The machine is portable allowing remote users to obtain information from the field. The Data Fax 2000 utilizes a patented Acoustic/Magnetic Coupler which attaches to any phone receiver, allowing transcription over pay phones, hotel phones, or from remote phone installations, without the need for dedicated phone lines or AC power. **Data East USA,** Santa Clara, CA **Write 171**

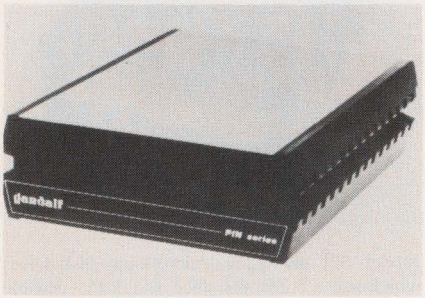
PLOTTER

For Surveying And Graphics Applications

The CPS-19 plotter can access and be driven by 100 graphics software packages for microcomputers. The CPS-19 will produce design and drafting graphics using the IBM PC and AutoCAD or the Apple IIe and Cadapple. Applications may be generated using a CP/M or MS/DOS based microcomputer. The CPS-19 requires no operator intervention between drawings. The plotter can produce, in one uninterrupted span, 33 E size or 600 A size drawings. **Houston Instrument,** Austin, TX. **Write 163**

SWITCHING MULTIPLEXER

X.28 Support



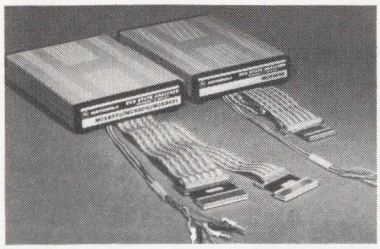
The Pin 9101E is a packet switching multiplexer which is designed to provide access to X.25 public switched networks for asynchronous terminals or computer systems with asynchronous ports. Up to 16 asynchronous devices, running speeds from 50 to 9600 bps, can be connected via EIA RS232C CCITT V.24 V.28 interfaces to the network through a synchronous link. It is certified for operation on all major networks. Features include; autobaud, Hewlett-Packard protocol support for ENQ/ACK block mode terminals, X.28 support to allow users to control asynchronous channel configurations, aggregate input rate of 57.6Kbps, and break handling and remote profile selection. Price ranges from $2,650 to $5,250. **Gandalf Technologies,** Wheeling, IL **Write 168**

2400BPS DIAL MODEM

For Remote Computer Applications

The DialNet 3000 Model 3024 2400 bps modem is designed for use over dial-up telephone lines. It can be used for remote computer access applications and can support either asynchronous or synchronous terminals. The originate/auto-answer modem complies with CCITT Recommendation V.22 bis when operating at 2400 bps. A switch-selected 1200 bps fallback mode, compatible with Bell 212-type modems is standard. At power-own, the modem performs a self-test, which includes analog and digital loopback testing, and the utilization of a test pattern generator that can be used with the loopbacks. Remote digital loopbacks can be invoked from either end of the communications link. Price is $795. **Micom,** Chatsworth, CA **Write 170**

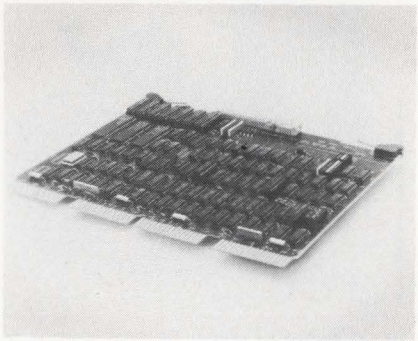
BUS STATE ANALYSER
For M6800 Chips



The Real-Time Bus State Analyser supports MC68008, MC68010 and MC68451 chips. The M68BSA1-1 is a redesigned version of the MC68000 BSA1 Personality Module. The module supports the MC68000 and expands its support to the MC68010 virtual memory MPUS and the MC68451 MMU. The Personality Module has two cable and probe/connector assemblies; one plugs into an MC68000 or MC68010 socket, and the other mates with an MC68451 socket in the user's system. Price is $3,500. **Motorola,** Phoenix, AZ

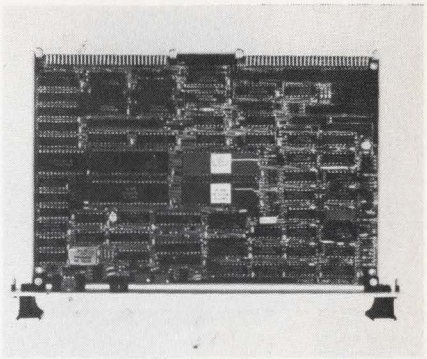
Write 201

MAGNETIC TAPE COUPLER
22 Bit Addressing



The Model DQ 342 is a 1/4″ magnetic tape coupler, that interfaces a CDC 1/4″ Sentinel streaming cartridge drive, with the DEC LSI-11-11/23PLUS and MICRO/PDP-11 computers. The controller is complete on a quad printed circuit board that contains the circuitry for TS-11/TU80/TSV05 compatibility under RT-11, RSX-11 and RSTS operating systems. The controller features 22-bit addressing for 4 Mbyte addressing, block mode DMA, switch selectable interrupt vector and register address, plus DMA four word burst size. Price in quantities of 100 is $1,085. **Dilog,** Garden Grove, CA **Write 207**

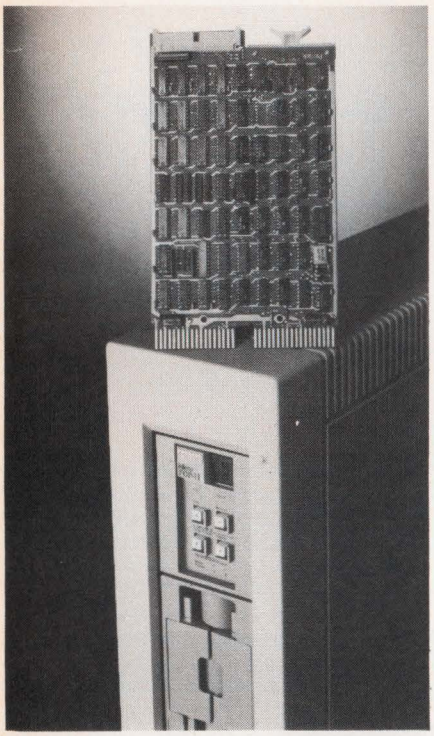
WINCHESTER/FLOPPY CONTROLLER
VMEbus Compatible



The SYS68K/WFC-1 is a VMEbus compatible Winchester/Floppy Controller. The board controls 4 5¼″ floppy drives and 3 5¼″ Winchester drives. The WFC-1 allows programmable sector size up to 1 Kbyte and provides automatic track formatting for hard disks. The access address and the address modifier are free selectable. The board generates two different interrupts with jumper selectable interrupt levels 1 to 7 and programmable autointerrupt vectors. The data transfer rate is 5 Mbit/sec. **Force,** Santa Clara, CA **Write 199**

DMA INTERFACE

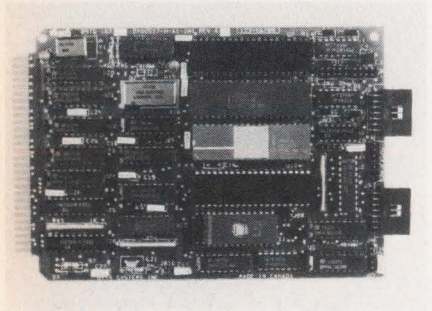
800 Kbyte/Sec Transfer Rate



The Micro-11 is a DMA interface for DEC Micro-11 computers. It offers 22-bit addressing, enabling the user access to the 4MB RAM capacity. The DMA-Q is designed for applications which require access for floppy disks, hard disks, CCD memory, bubble memory, printers, graphic displays, voice synthesizers, and data acquisition devices. Data can be transferred at up to 800K words/sec. Price is $575. **Peritek,** Oakland, CA **Write 206**

PROCESSOR CARD

1 Mbyte Memory Addressing



The DST D-187 processor card is an 8088-based product incorporating the 80130 RMX processor, two RS232C serial channels and optional 8087 math coprocessor. The card provides one 28-pin bytewide socket for RAM/EPROM/ROM, and on-board memory may be disabled under software control. Contents of dynamic RAM are preserved during reset. 1 Mbyte memory addressing is supported and the DSTD-187 provides transparent dynamic RAM refresh. Both Z80 and 8088 bus architectures are supported by the DSTD-187 and 8 MHz versions are available. Price is $584. **dy-4 Systems,** Ontario, Canada **Write 188**

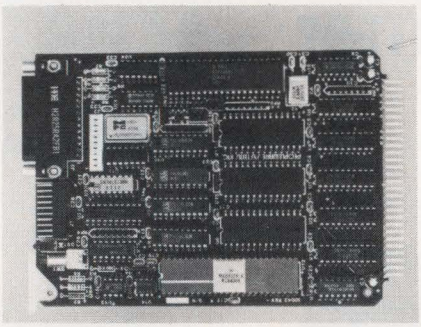
TERMINAL BOARD

For S-100 Bus

The VC8024 CPU-Video Terminal board is designed for the S-100 bus. The VC8024 can be used as a smart video terminal card or as a stand alone CPU board in small system applications. The VC8024 is controlled by an on board Z80A microprocessor supplied with memory, maximum of 16K EPROM and/or 4K of RAM, and I/O ports. The video portion is implemented using a SMC5037 video controller and SMC8002A attribute controller. A separate 2K×12 video memory allows four simultaneous video attributes to be displayed for any of the characters on the screen. The video format displayed is 80×24 with a 7×12 character matrix. Three display modes are supported. Price is $49.98. **EMS,** Irvine, CA **Write 191**

STD BUS MICROPROCESSOR

32 Kbyte On Board Memory



The 68008-based STD bus microprocessor runs at 8Mhz. STD bus signals (address data and control) are buffered for expansion. The microprocessor has three 28-in JEDEC sockets and 32 Kbyte of on-board memory. One socket is configured for either a 2764 or 27128 type EPROM. Off-board memory access is aided by a decoder/driver that selects memory boards via a front connector. A total of one Mbyte can be accessed. **Peopleware Systems,** Minneapolis, MN **Write 194**

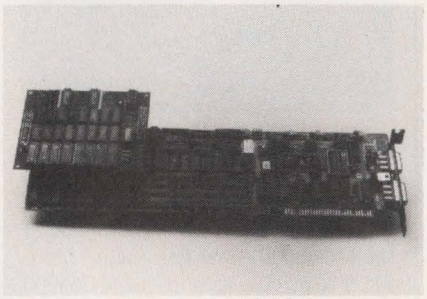
DISPLAY CONTROLLERS

For VMEbus Graphics

The IV-1651 VMEgraf and the IV-1653 VMEcrt are dual – width VMEbus board controllers. Applications range from system consoles to advanced CAD/CAM graphics and process monitor displays. The IV-1651 supports color bit mapped graphics displays of up to 1024×1024 or 1280×768 resolution. The controller features a down-loadable character set and transparent access dual port memory. These boards may be used independently or together for most VMEbus CRT display requirements. **Ironics,** Ithaca, NY **Write 198**

IMAGE ACQUISITION AND DISPLAY MODULE

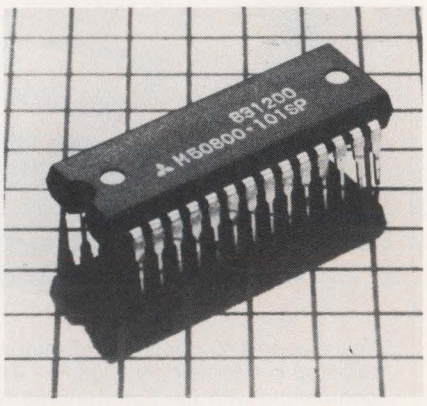
Displays 30 Frames/sec



The Frame Grabber is a real-time video image acquisition and display module for the IBM PC and PC XT. The Frame Grabbér converts an analog video signal (RS-170) from a camera to digital data at a 10 Mhz rate, and stores the resulting 6-bit pixel data in an on-board 512 × 512 frame memory. It can simultaneously acquire and display 30 frames per second. Each location in the on-board frame memory is 8 bits deep and stores 6 bits of digital data with the remaining bits enabling 2 planes of graphic overlays. These graphic overlay planes can be used for generating and positioning text or graphics on the image without disturbing the stored video data. The frame memory is mapped into the IBM PC address space, enabling access to the stored image and facilitating image processing by the IBM PC. Price is $2,995. **Imaging Technology,** Exeter, NH. **Write 192**

CMOS SPEECH SYNTHESIZER

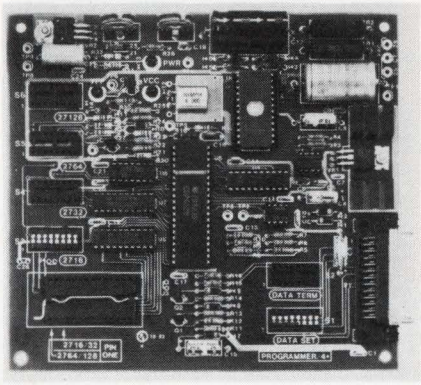
32K Bit ROM



The M50800 is a single chip speech synthesizer. It is a speech or melody synthesizer which produces male and female voices on the same chip. The 28 pin shrink package device is designed using a 3um design rule. The chip contains a 32K ROM, clock oscillator, D-A converter and speaker driving circuitry. The onboard ROM provides a speech synthesis time of 15 to 18 seconds and up to 64 words of vocabulary. The chip can also generate a melody tone with a three octave range for 60 seconds. The speech vocabulary can be expanded by adding external memory, and is limited only by the size of the external ROMs used. **Mitsubishi Electronics,** Sunnyvale, CA **Write 193**

EPROM PROGRAMMER

Converts Small To Large EEPROMs



The Programmer 4+ is an EPROM programmer which features an RS232 serial interface and is usable with any computer or dumb terminal. The Programmer 4+ is a single board unit and can handle all 1K through 16K EPROMS. The Programmer 4+ comes with a manual, schematic, and floppy disk with all software and source code. Under user-friendly, menu driven software control, the unit will Test, Read, Program EPROMS, Save To and Read From disk in either ASCII, hex or object code. User may convert small EPROMS into a larger one and vice versa. 8" and 5¼" disks available for most CP/M computers. Price is $199.95. **Periphco,** Santa Clara, CA

Write 202

A/D PERIPHERAL IC's

Performs Conversions in 10 Msecs

The TLC540 and TLC541 are 8-bit, serial-output, A/D peripheral integrated circuits that can perform A-to-D conversions in 10 Msecs and 19 Msecs, respectively. On-chip features include an 8-bit, successive-approximations A/D converter, a 12-channel multiplexer, 11 analog inputs, sample-and-hold circuitry, three data registers, and microprocessor-control logic interfacing with an on-chip, three-line, TTL-compatible serial I/O port. The chips provide a built-in self-test mode and the capability for simultaneous R/W operation. The sample-and-hold circuitry is software programmable. **Texas Instruments,** Dallas, TX

Write 211

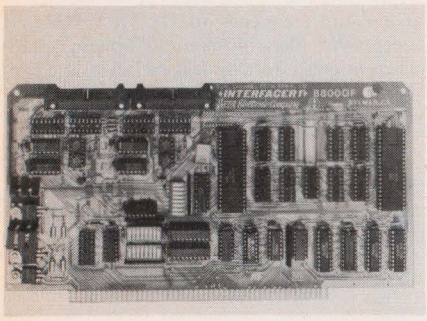
COUNTER/TIMER MODULE

Provides Up/Down Counting

The DMS251 Dual-Channel Counter/Timer/Clock Module features 2 independent 16-bit counters and an internal oscillator in a microprocessor bus compatible package. The DMS251 is programmable to provide-up/down counting, pulse/frequency counting time interval measurement, and clock output operating modes at rates of up to 1 MHz. The DMS 251 will accept inputs of 10 volts without damage, with a minimum pulse width of 100 nsecs, and at a count frequency of DC to 1 MHz. It accepts 90° phase differential 2-phase (quadrature) signals from optical encoders, and provides a direction indication output to the processor. **Di-an,** Cheshire, England. **Write 197**

I/O BOARD

S-100 Bus Compatible

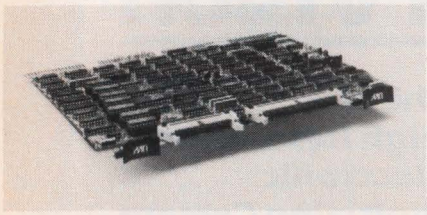


The model 8800GF serial interface is designed for IEEE696/S-100 bus systems and provides two independently-addressable I/O ports for either RS232C communications or optically-isolated 20mA ports with internal or external current sources. With RS232C, jumpers permit master operation in Data Terminal Equipment mode for modems or slave operation for Data Communications Equipment mode for terminals and printers. An on-board 5.0688 MHz crystal oscillator permits switch-selectable data transmission rates from 50 bits/sec to 19.2K BPS. The 8800GF employs type 1602 UART for parallel-to-serial, serial-to-parallel conversion, error detection and serial-data formatting. Character frames can be 7-bits or 8-bits long with odd, even, or no parity and one or two stop bits. Price is $370. **Vector Electronic,** Sylmar, CA

Write 196

FLOPPY DISK CONTROLLER

Emulates Four DEC RX02 Subsystems



The MX22 is a DEC compatible 8″ Floppy disk controller for Unibus-based systems. The MX22 is a quad sized board which emulates up to four DEC RX02 floppy disk drive subsystems. The 8″ and 5¼″ drive interfaces allow the user to choose four of either 8″ or 5¼″ drives, or choose two 8″ and two 5¼″ drives. The MX22 requires a single Unibus SPC slot when interfacing with the PDP-11 series computer. Features include self diagnostics, on-board bootstrap and power-fail protection. Price is $1,045. **MTI,** Placentia, CA

Write 209

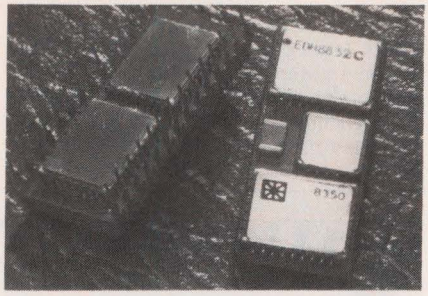
FLOATING POINT CHIP SET

8 Mflop Performance

The WTL 1033 Floating Point Arithmetic Logic Unit is a VLSI circuit designed for use in high-speed, floating-point processors. It operates at 8 Mflop and is compatible with the IEEE 754 floating-point standard. The 8 chip set features add, subtract, multiply and absolute value capabilities, and handles conversion to and from 24-bit fixed-point arithmetic. **Weitek,** Sunnyvale, CA **Write 189**

CMOS RAM

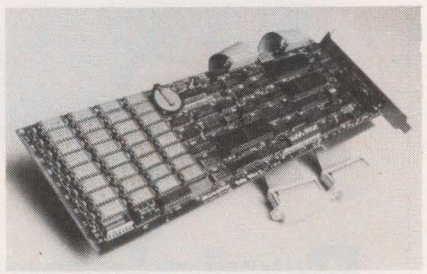
200 Nsec Access Time



The EDH8832C is a 32K × 8 bit static CMOS Ram for computer instrumentation applications. The unit is pin compatible with JEDEC bytewide memory pinout. The EDH8832C is also EBM-pack compatible and conforms to industry standard 28 pin 64K RAMS and possesses 64K RAM CMOS characteristics. The EDH8832C has address access times of 120, 150 and 200 ns. **Electronic Designs,** Hopkinton, MA **Write 208**

ADD-ON MULTIPROCESSING BOARD

256 Kbytes RAM

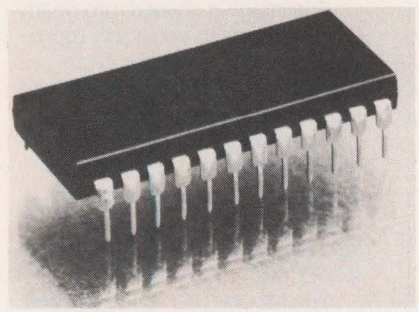


The Baby Blue II is a multifunction board for the IBM PC, PC-XT, TI Professional and IBM compatible personal computers. The board includes two serial ports, a Centronics-compatible parallel printer port, clock/calendar with battery backup and 256 Kbytes of expansion RAM. The Baby Blue II supports background processing, and can independently compile, print, or communicate, while normal system operations continue in the foreground. Price is $695. **Microlog,** Suffern, NY

Write 195

NON-VOLATILE RAM

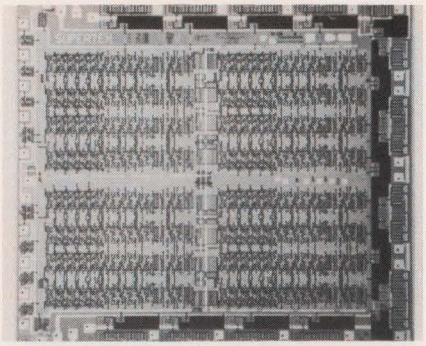
300 ns Access Time



The NCR 52001 is a byte wide NVRAM which operates from a 5-volt power supply. The 1K device consists of a 128 × 8 RAM array with a duplicate EEPROM array for backup. Typical access time is 300 ns for each device. Price in quantities of 100 is $15.02. **NCR,** Dayton, OH **Write 204**

FLAT PANEL DISPLAY DRIVERS

16 Grey Scale Levels

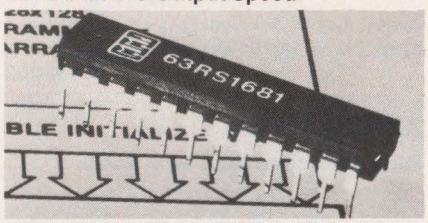


The HV01 and the HV02 are electroluminescent flat panel display drivers. Their design is based on proprietary HVIC technology which combines high voltage DMOS devices with high noise immunity and low power silicon-gate CMOS circuitry on one chip. The HV01/HV02 chip set offers 16 levels of gray scale compatibility and are available in 40 pin DIP's, 36 pin leadless chip carriers and in die form. Price in quantities of 1000 is $35. **Supertex,** Sunnyvale, CA

Write 205

2K × 8BIT PROMS

15 ns Clock-To-Output Speed

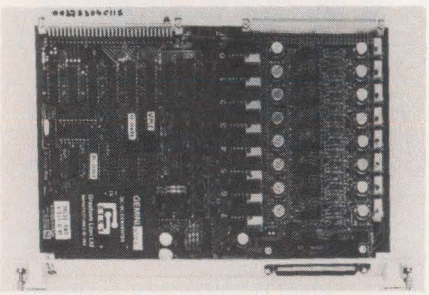


The 63 RS/RAI681 and 63R3/RAI681A are two 2048 word-8-bit PROMs. They are available with synchronous or asynchronous enable and have clock-to-output times of 20 ns and 15 ns. **Monolithic Memories,** Santa Clara, CA

Write 186

12-BIT D/A CONVERTER BOARD

3 Msec Conversion Time

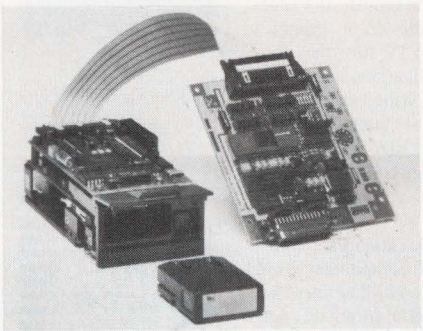


The DSSE8DA12 8-channel, 12-bit D to A converter board is VMEbus compatible and has a conversion time of Msecs. The user can select each of the operating channels by software. All 8 channels are latched, and each channel can be independently configured for either a current or a voltage mode. Input modes are jumper selectable and include bipolar (−5V/+5V; −10V/+10V), unipolar (0V −5;0V −10V), and 0−20 mA, 4-20 mA current loops. Inputs and outputs are isolated by opto-isolators and a DC/DC converter. The board takes two consecutive memory locations. Price is $1875. **Data-Sud Systems,** Tempe, AZ

Write 210

BUBBLE MEMORY ADAPTORS

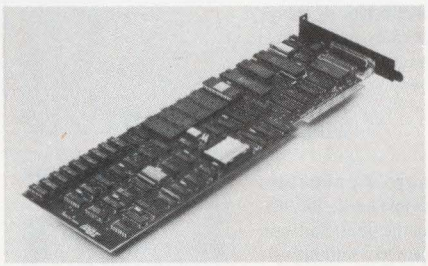
64 Byte Block Transfers



The FBM-A002 and FBM-A003 bubble-memory adapters interface Fujitsu 1 Mbit bubble memory cassette systems and 4 Mbit bubble memory cards to RS232C and GPIB. The FBM-A002 interfaces with RS232C and the FBM-A003 with GPIB. The transfer systems for both adapters support 64-byte block transfers. Baud rates of 1200, 2400, 4800, 9600 and 19200 are selectable. Price in quantities of 1000 is $194. **Fujitsu,** Lake Bluff, IL **Write 203**

SINGLE BOARD COMPUTER

64K RAM



The I-Bus RI88 Single Board Computer uses an Intel 80188 processor and operates at 4.77MHz. The RI88 is upward compatible with software written for the IBM PC's 8088 processor, but allows the use of the 80188's enhanced instruction set. The RI88 board includes the processor, 64K of RAM, 160K of user EPROM, and an RS232C serial console port. An I/O System ROM supports the software interrupts used by the IBM PC, allowing much of the IBM PC software to be directly executed by the system. Also available is a debugging routine in ROM, called I-Bug, which includes utilities for downloading programs developed on an IBM PC or an 8086/80186 development system. Price is $795. **I-Bus Systems,** San Diego, CA **Write 187**

SINGLE CHIP MICROCONTROLLER

Military Version

The MC8751H single-chip microcontroller is the EPROM version of the MDC8051AH 8-bit microcontroller fabricated on HMOS IE. The MC8751H has features such as: 4K ROM; 128K RAM; 32 I/O lines; two 16-bit timer/counters; serial and an on-chip oscillator and clock circuitry. The MC8751H is compatible with the TTL family, as well as with the MCS-80 and MCS-85 peripherals. It provides hardware support for 1 bit variables as a separate data type. Price in quantities of 500 is $300. **Intel,** Chandler, AZ **Write 190**

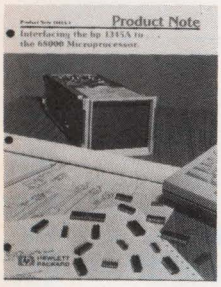
DISK CONTROLLER

With Four Connect Ports

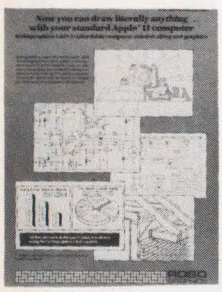
The BMX-1 disk controller is plug compatible with the Burst Multiplexor Channel on Data General minicomputers. The fully emulating BMX-1 allows users to select any SMD interfaced disk drive for use with the DG S-140, S-280, and MV Series CPUs. The BMX-1 has four disk drive connect ports with software configurable drive characteristics on a port by port basis. The BMX-1 ensures data integrity and error recovery through an on-board 32 bit ECC, offering error detection with burst error correction to 11 bits in length. ECC error logging with status reporting, offset positioning, and strobe Early/Late are supported. Price is $4,995. **Custom Systems,** Minnetonka, MN **Write 200**

New Literature

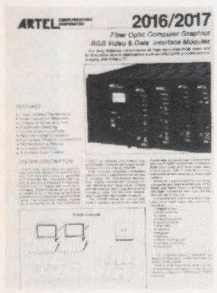
Emulating System Brochure. This brochure from Nanodata Computer Corp. describes the QM-1, a host system for general purpose emulation. It evaluates CPU's, I/O controllers, multiprocessors, and networks. The QM-1 has an 82 nsec cycletime and two writable control stores. The system allows microprogrammers to build emulators for programs development and system analysis. Emulators can perform event counting and timescaled to reflect real time performance for synchronous digital devices.
Nanodata Computer Corp. **Write 267**



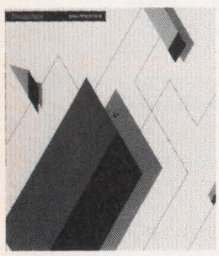
Product Note For Display Integration. This product note from Hewlett-Packard is a guide for OEM designers to use when interfacing a digital display to a microprocessor in a computer-based instrumentation system. It provides schematics, programming code, and an operational description of the general purpose interface and outlines procedures that can be applied when working with other microprocessors as well.
Hewlett-Packard **Write 268**



CAD Brochure. This four-page brochure from Chessell-Robocom Corp. explains how designs are created and modified, images stored, and drawings recorded by using Robographics CAD-1 software. The brochure describes schematics, mechanical drawings, architectural layouts, and business presentations which can be produced with the CAD-1. It covers drafting and includes a listing and description of system features.
ROBO Graphics **Write 253**



Fiber Optic Bulletin. This bulletin from Artel Communications Corp. describes fiber optic plug-in transmit/receive modules. Applications include CAD/CAM, process control, imaging and military C^3. The bulletin explains how the modules transmit color or monochrome video and simultaneous bi-directional RS-232C or TTL digital data two miles over optical fibers. The bandwidth accommodates 1280 × 1024 pixel resolution. BNC input/output connectors are plug compatible to all monitors and display generators.
Artel **Write 263**

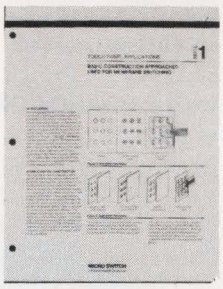


Data Communications Catalog. This product catalog from Timeplex details their line of data communications network products. The catalog describes individual product capabilities. Timeplex builds data communications networks on a turnkey basis and can design, stage, integrate, install, and maintain the complete data network.
Timeplex **Write 265**

IC Data Book. This 736-page book from Precision Monolithics, Inc. provides technical data for their line of linear products. Products include; operational amplifiers, instrumentation amplifiers, voltage followers/buffers, voltage comparators, matched transistors pairs, voltage references, D/A converters, analog switches/multiplexers, sample-and-hold amplifiers along with special function and communications products.
PMI **Write 255**

Color Graphics Data Sheet. This two-page data sheet from Reliance Electric Co. describes how the AutoMate 35 programmable controller interfaces with the REACT Industrial ColorGraphics system to provide color graphics capability. The AutoMate 35 PC furnishes constant visual updates of applications being controlled. Interfacing is accomplished via the AutoMate 35 Intelligent Peripheral Communications Card (IPCC) and a modified EIA RS-232 cable to the REACT ColorGraphics console.
Reliance Electric **Write 264**

R&D Catalog. This 98-page catalog of electromechanical equipment and components from American Design Components illustrates and describes items useful in R&D, protoype engineering, maintenance and testing. All are available for immediate off the shelf delivery. Items include transducers, accelerometers, fractional HP, AC, DC and stepping motors, blowers and fans, relays, and counters.
American Design Components
Write 258



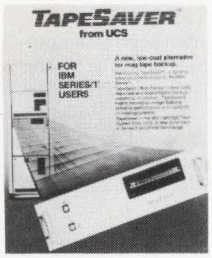
Touch Panel Application Note. Micro Switch discusses membrane touch panel technology in three application notes. Note one, reviews four basic approaches to the construction of membrane switching; flexible/vented, flexible/unvented, and rigid/control unvented. The second application note considers the effects of electrostatic discharge (ESD) on semiconductors devices and the final note reviews parameters of usage, sealing and environment to be considered when selecting gold or silver contacts.
Micro Switch **Write 260**

Communications Software Application Note. This application note from Gould, Inc. discusses procedures for users of the 9520 Software Development System who want to communicate with a Data I/O System 19 prom programmer using HCOM communications software. There are two procedures, one for uploading from and the other for downloading to the prom programmer. Each procedure provides step-by-step instruction for the communication process.
Gould **Write 251**

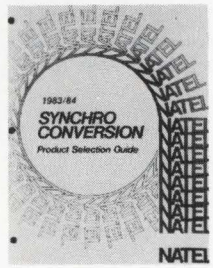
Color Display Brochure. This four-page brochure describes Systems Research Laboratories' Model 2106 In-line Color Display. The display features 100 MHz video bandwidth, preconverged tube/yoke assembly, factory magnetic tuning, selectable line/frame rates, and a 64 kHz horizontal frequency option.
Systems Research Laboratories
Write 259

Protocol Converter Brochure. This 12-page color brochure describes Micom's Micro7400 Protocol Converter, a device which enables 12 asynchronous terminals to access IBM mainframes. The brochure illustrates product features and applications. Also included are descriptions of features which are not available to users of IBM 3270s, such as the ability to switch terminal data to either of two IBM hosts or between an IBM host and minicomputer ports in response to commands entered at the user's keyboard.
Micom **Write 256**

Database Service Brochure. This four-page brochure explains Tech-Doc, a computer-based reference system designed to help improve engineering productivity and quality by reducing component research time and providing a range of options. Offered as a subscription service with bi-monthly updates, specification information on the database is detailed on a separate two-page sheet. The literature also explains micro-index, a microcomputer-based indexing system.
Inacom **Write 254**

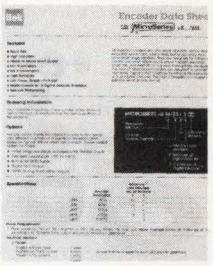


Magnetic Drive Data Sheet. Ultimate Computer Services' data sheet describes the Tapesaver, a method for IBM Series 1 users to store and retrieve data on ¼" magnetic tape cartridges. The UCS system consists of a cartridge tape drive, controller, power supply and a single-board attachment card that fits into one input/output slot on the IBM Series 1. Included are system highlights and interactive system capabilities.
Ultimate Computer Services **Write 261**

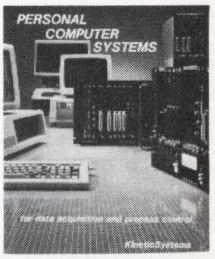


Synchro Conversion Brochure. This 20-page brochure from Natel Engineering describes the features and applications of synchro conversion hybrid and modular products. Several of the highlighted products are designs from Natel, others are alternate source products for converters currently available from other manufacturers.
Natel Engineering **Write 257**

Encoder Data Sheet. This data sheet describes Itek's LSI Microseries Model 17/23 encoder. The encoder is designed as a digital (o/5V) interface for a microprocessor or digital decoder that can output in parallel, serial, or byte format. Listed in the specs are quanta/revolution, sampling rate, and the operating speed. Options include mechanical and electrical interfaces.
Itek **Write 262**



Data Acquisition Brochure. This brochure from Kinetic Systems describes their line of I/O modules for industrial and laboratory interface process requirements. The modules include multiplexers, signal conditioners and A/D converters. The modules permit IBM, Apple or DEC systems to be used for both stand-alone and distributed process control. The modules can be used wherever computing power is needed to scan inputs, digitize signals, store data and display graphics.
Kinetic Systems **Write 266**



Data Communications Catalog. This 36-page catalog and buyers guide profiles International Data Sciences' line of handheld test equipment, data switches, modems and cables. Products include an RS-232 test set, an analog test set and 212A and 103/113 compatible modems. Product descriptions feature illustrations, schematic diagrams, photos, specifications and pricing information for both standalone and rack mount models.
IDS **Write 250**

Calendar

April 3-5

CAD '84 6th International Conference and Exhibition on Computer in Design Engineering. Brighton, UK. Contact: Joanna Wexler, Butterworth Scientific Ltd., PO Box 63, Guildford, GU2, 5BH, UK. Tele. 0483-31261.

April 9-12

ATE Northwest Conference. San Mateo, CA. Contact: Morgan-Grampian Expositions Group, Two Park Ave., New York, NY 10016. (212) 340-9780.

April 18-20

The 7th Annual Rocky Mountain Data Processing Expo and Conference. Denver, CO. Contact: Industrial Presentations West, Inc., 3090 So. Jamaica Ct. #304, Aurora, CO 80014.

April 19

California Computer Show. Palo Alto, CA. Contact: Norm DeNardi Enterprises, 289 S. San Antonio Rd., Los Altos, CA 94022. (415) 941-8440.

April 23-27

Compdec, Computer Data Engineering Conference. Los Angeles, CA. Contact: Compdec, IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. (301) 589-8142.

April 24-25

ACM Sigsoft/Sigplan Software Engineering Symposium on Practical Software Development Environments. Pittsburgh, PA. Contact: Peter H. Henderson, Dept. of CS, SUNY at Stony Brook, Stony Brook, NY 11794. (516) 246-5000.

April 24-27

Computer Graphics Tokyo '84. Tokyo, Japan. Contact: Executive Travel, 1801 E. 79th St., Bloomington, MN 55420. (612) 854-2620.

April 29-May 4

1984 SPIE Conference: Applications of Artificial Intelligence. Washington, D.C. Contact: John Gilmore, Artificial Intelligence Branch, Georgia Tech EES/EML/EOD, Atlanta, GA 30332. (404) 894-2000.

May 1-4

Designing with 16-Bit Micros. Washington, D.C. Contact: Ruth Dordick, Integrated Computer Systems, 6305 Arizona Place, PO Box 45405, Los Angeles, CA 90045. (213) 417-8888.

May 3-6

The Mid-West Apple/IBM PC Expo. Chicago, IL. Contact: Northeast Expositions, 822 Boylston St., Chestnut Hill, MA 02167. (617) 739-2000.

May 7-10

1984 IEEE International Symposium on Circuits and Systems. Montreal, Canada. Contact: IEEE, Service Center, 445 Hoes Lane, Piscataway, NJ 08854.

May 8-10

CAM-I International Spring Seminar Computer Integrated Manufacture. Montreux, Switzerland. Contact: CAM-I, Inc., Conference Services, 611 Ryan Plaza Drive, Arlington, TX 76011. (817) 860-1654.

May 13-17

Computer Graphics 84, The National Computer Graphics Association's Fifth Annual Conference and Exposition. Anaheim, CA. Contact: Education Coordinator, National Computer Graphics Association, 8401 Arlington Blvd., Fairfax, VA 22031 (703) 698-9600.

May 14-17

ICC 84, International Conference on Communications (IEEE et al.) Amsterdam, The Netherlands. Contact: T. A. C. M. Classen, Philips Research Laboratories, PO Box 218, 5600 MD Eindhoven, The Netherlands. Tele. (31)40-742131/742236 or E. T. Andrews, Bell Laboratories, Crawford's Corner Rd., Holmdel, NJ (201) 949-3143.

May 14-19

Expotech International. Houston, TX. Contact: D. Stewart Larson, Expotech International, 2033 M St., N.W., Washington, D.C. 20036. (202) 467-5866.

May 15-17

Electro 84, High Technology Electronics Exhibition and Convention, and Mini-Micro Northwest (IEEE et al.) Boston, MA. Contact: Electronic Conventions, Inc. 8110 Airport Blvd., Los Angeles, CA 90045. (213) 772-2965.

Advertiser Index