

# EDN

High-temperature,  
rad-hard op amps

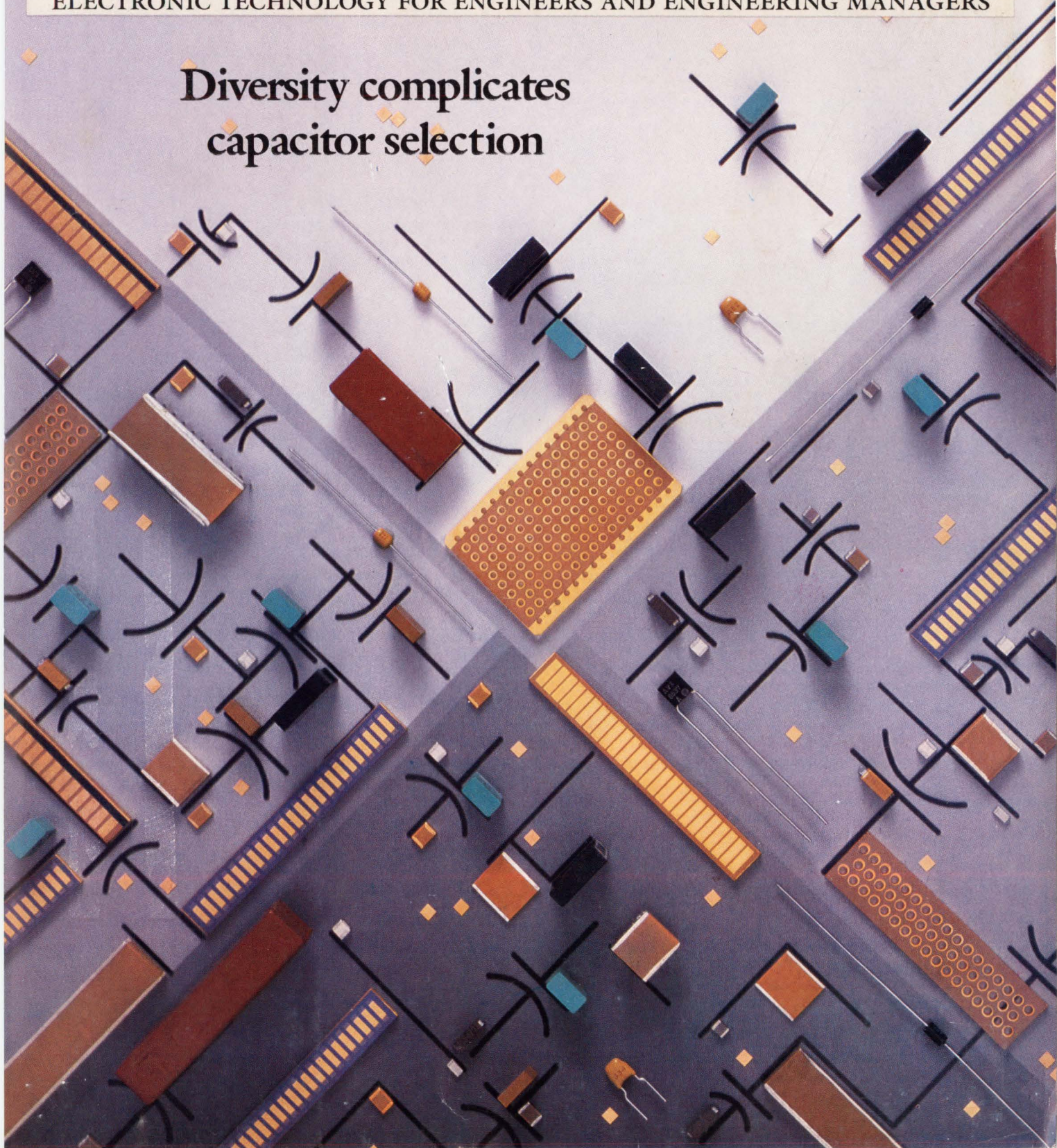
Encryption ICs

Designer's Guide to  
EDIF—Part 1

Technical-article  
database index

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

## Diversity complicates capacitor selection





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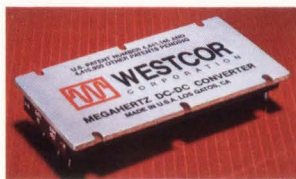
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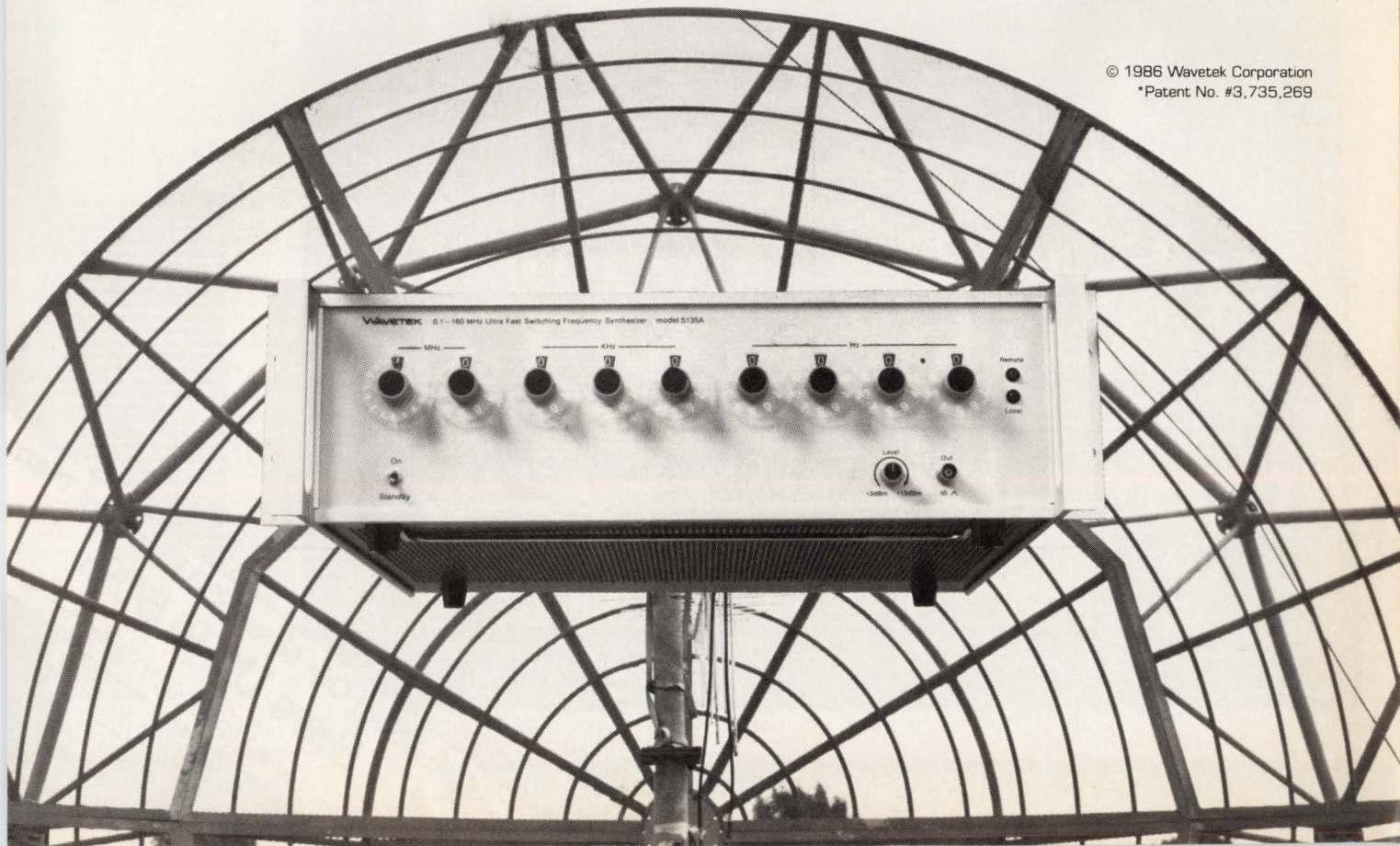
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Circle 3 for Demonstration

Circle 42 for Literature



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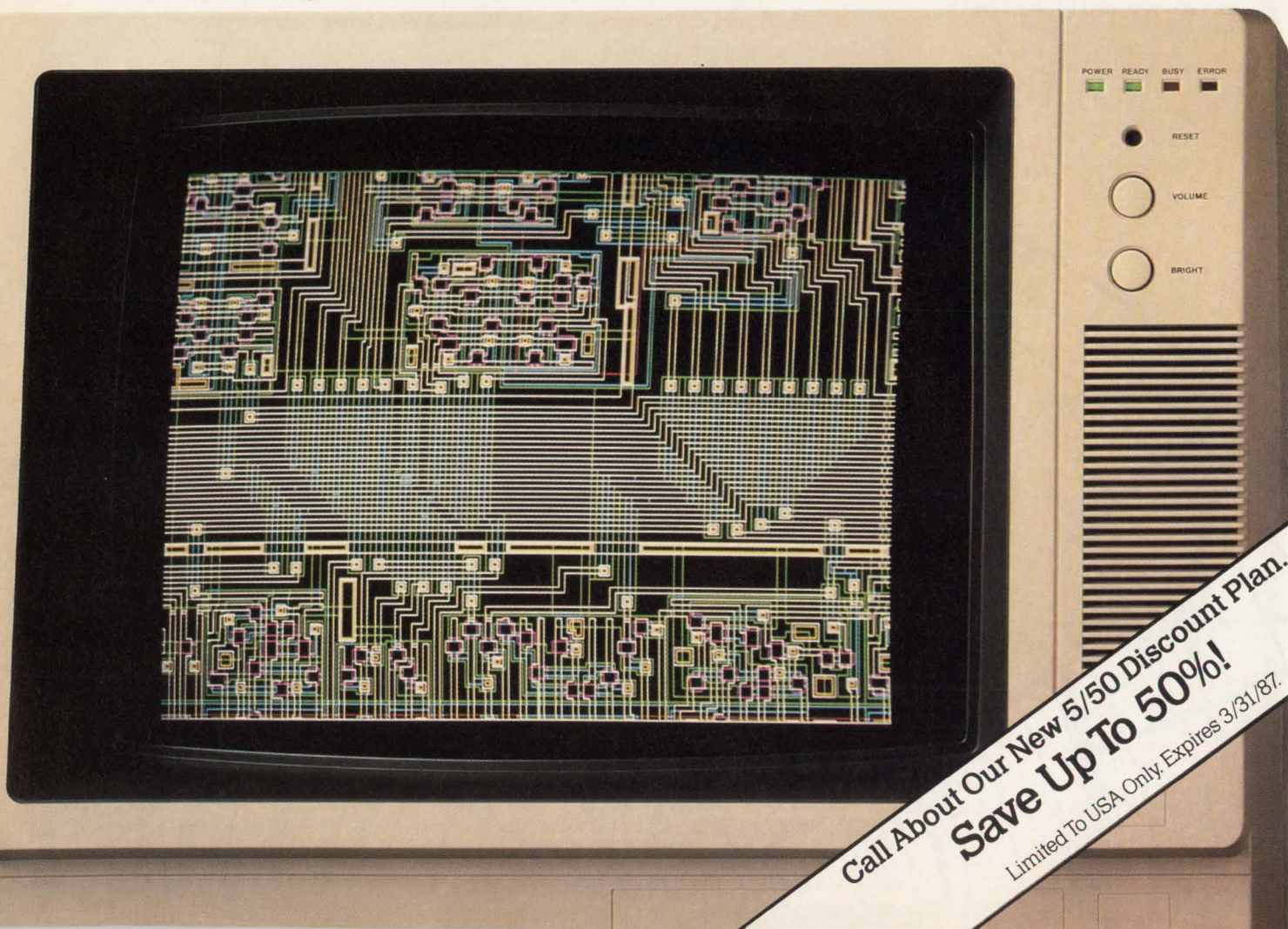
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*On the cover: You can bypass a variety of problems by populating your pc boards with capacitors, but selecting the best capacitor type for a given application isn't a trivial task. See pg 116. (Photo by Visual Conspiracy, courtesy AVX Corp)*

## DESIGN FEATURES

### Special Report: Capacitors

116

Choosing capacitors often involves a tradeoff among cost, performance, and mounting considerations. This report discusses the parametric and physical aspects of several types of capacitors that are suitable for soldering to pc boards, and it presents a representative sampling of recently introduced devices.—*Bill Travis, Senior Editor*

### Composite amplifiers yield high speed and low offset

139

You can find an op-amp technology that excels in any one performance area, but today's applications often demand high performance in several areas. You must therefore employ some ingenious circuit-design techniques to circumvent the limitations.—*Jim Williams, Linear Technology Corp*

### Designer's Guide to EDIF—Part 1

153

The existence of a standard data format would help design engineers transfer data easily between CAE/CAD systems, or to and from a device manufacturer. The Electronic Design Interchange Format (EDIF) proposes to be such a standard.—*Esther Marx, Hart Switzer, and Mike Waters, Motorola Inc*

### ISDN terminals simplify data transmissions

167

The Integrated Services Digital Network (ISDN) digitizes voice signals to provide a complete digital link from end user to end user. The result is a common communication link—the telephone system—that provides access to all forms of communication. A recently introduced IC set can simplify the implementation of ISDN terminals.—*Tony O'Toole, Advanced Micro Devices*

### Flexible PGA designs require few components

181

Programmable-gain amplifiers (PGAs) add great flexibility to data-acquisition systems yet require only a few components. You can use PGAs in your circuits to amplify low-level signals precisely, to reduce common-mode signals, to limit signal bandwidth, and to minimize amplifier offset effects.—*Akavia Kaniel, Intech Inc*

### EDN Technical-Article Database Index

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EDN's semiannual database index lists articles published from May through October 1986 in EDN, Electronic Design, Electronics, Electronic Products, Computer Design, and Digital Design.—*EDN Staff*

*Continued on page 7*

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## SPECIFICATIONS

**MEASUREMENT AND CONTROL OPTIONS:** analog input, analog output, status I/O, counter/totalizer, sequence-of-events

**ANALOG MEASUREMENT SPEED:** 1,000/s

**SIGNAL CONDITIONING:** dc and ac voltage, current, thermocouple, RTD, strain

**STORAGE:** 400 Kbytes floppy disk, 3 Mbytes RAM, 2 Mbytes non volatile RAM

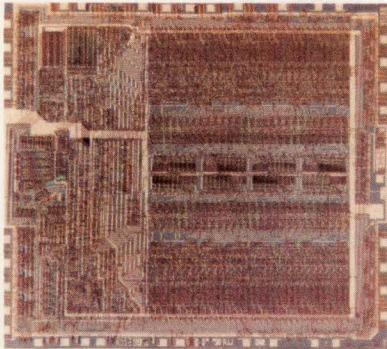
**INTERFACES:** RS-232-C, RS-422, IEEE-488, parallel

**TOUCH-SENSITIVE DISPLAY:** 640 x 224 dots, 60 touchkeys

**SOFTWARE:** BASIC, FORTRAN, Flare application packages

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*If you're designing a system that will handle sensitive data, you might require a cryptographic means of protecting the data against unauthorized access. To help you implement such a scheme, you can select one of several ICs (pg 63).*

## TECHNOLOGY UPDATE

### Availability of cryptographic ICs augurs the increasing use of data encryption 63

As the need for data encryption becomes increasingly evident because of the increase in traffic over satellite and microwave links, cryptographic schemes must be commercially available and economically feasible.—*Chris Terry, Associate Editor*

### Specially processed operational amplifiers meet rad-hard and high-temperature needs 75

Military and aerospace applications have placed severe environmental demands upon analog components for some time, but don't overlook the possibility of using the parts specially processed to meet those demands for your own, more terrestrial, and in some cases even subterranean, applications.—*Jim Wiegand, Associate Editor*

## PRODUCT UPDATE

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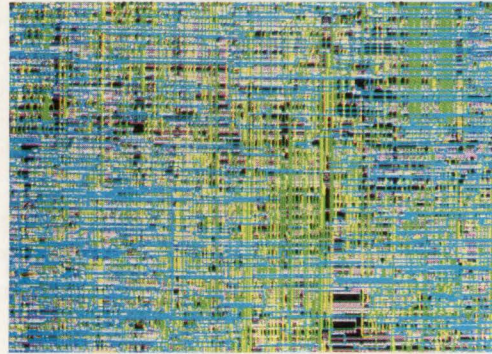


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## EDITORIAL

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Though it's meant to help US IC makers, the US-Japan Semiconductor Trade Agreement is filling Japanese coffers and driving US manufacturing offshore.

## NEW PRODUCTS

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Laid-off engineers find the experience painful but survivable.—*Deborah Asbrand, Associate Editor*

## LOOKING AHEAD

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Market for optical computers to be worth \$1B by 2000 . . . AI reaches factory floor: Market to top \$1.7B by '90.

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STAY

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16K SRAMs		
Device	Process	Access Times
IMS1400M (x1)	NMOS	45, 55, 70ns
IMS1420M (x4)	NMOS	45, 55, 70ns
IMS1403M (x1)*	CMOS	35, 45, 55ns
IMS1423M (x4)	CMOS	35, 45, 55ns

64K CMOS SRAMs	
Device	Access Times
IMS1600M (x1)*	45, 55, 70ns
IMS1620M (x4)*	45, 55, 70ns
IMS1624M (OE, x4)*	45, 55, 70ns
IMS1630M (x8)*	45, 55, 70ns

MILITARY DRAMs		
Device	Process	RAS Access Times
IMS2600M (64Kx1)	NMOS	100, 120, 150ns
IMS2800M (256Kx1)	CMOS	80, 100, 120, 150ns
IMS2801M (256Kx1)	CMOS	80, 100, 120, 150ns

\*Also available as Low Power Battery Backup CMOS SRAMs with Idr of 10µA (typical Icc at 2V at 25° centigrade).

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We are the world leader in CMOS and NMOS static RAMs, in 16K, 64K and 256K byte wide memory products. We make the fastest 2K x 8 at 35 ns and also a 4K x 4 static RAM at 35 ns. We pioneered the 8K x 8 CMOS static RAM and are now offering a 64K x 1 (55 ns) and 32K x 8 CMOS static RAM.

But we make more than static RAMs. As you can see from the chart, we have a complete line of DRAMs, CMOS, and NMOS ROMs, EPROMs, and one time programmables. And they are all in volume production today.

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We were also the first to introduce the 1 Mb DRAM and we're now the market leader. We were one of the first suppliers of the 256K CMOS static RAM. We were a leader with the 256K ROM and within a year of introduction, we shipped more than all other suppliers combined. And we are matching that with our 1 Mb CMOS mask ROM.

So you can see that we have the capability to supply the memory products you want—when you want them.

That's memory power; that's Toshiba.

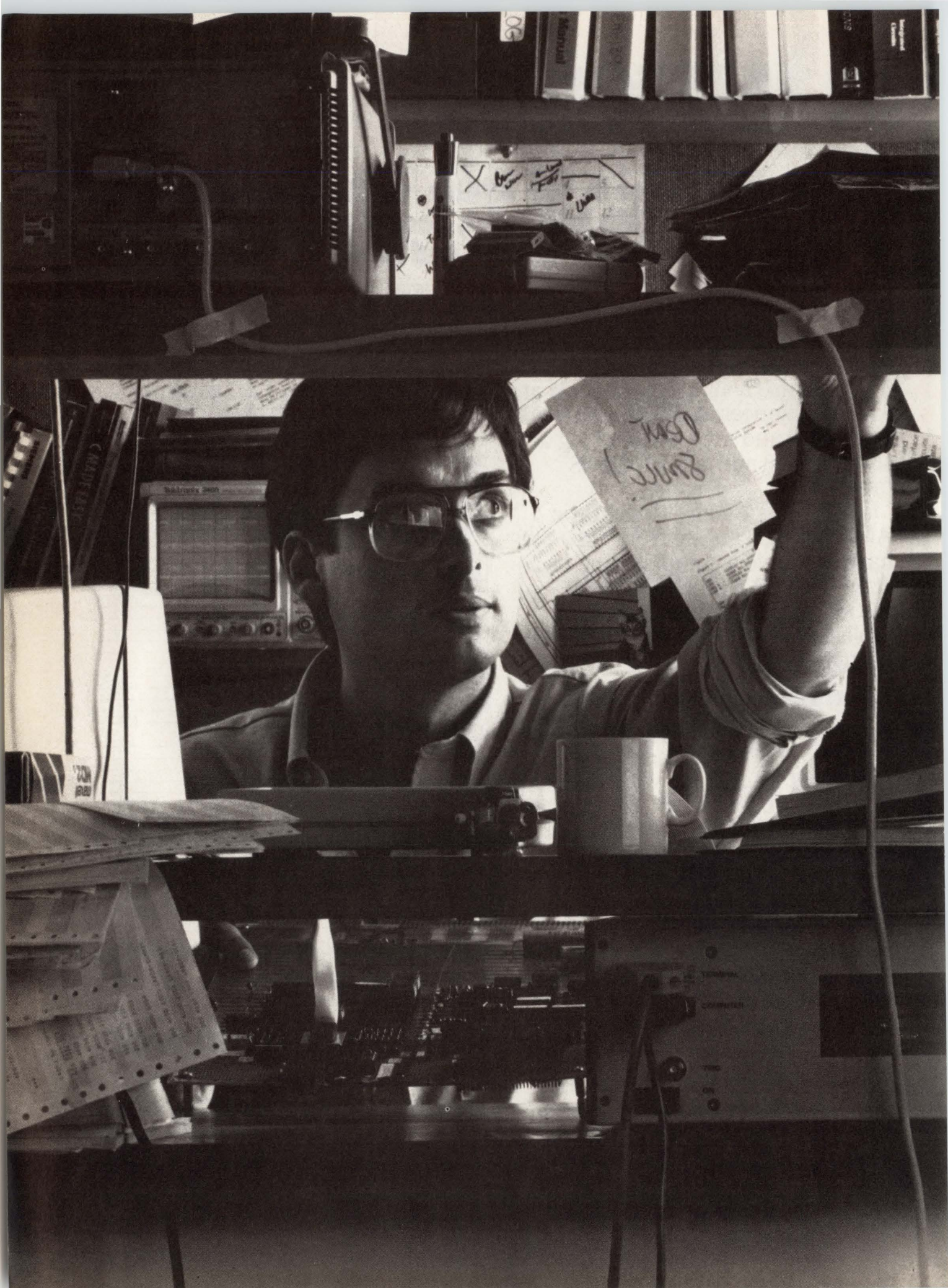
### TOSHIBA MEMORY PRODUCT SUMMARY

PART NO.	ORG.	PROCESS	SAMPLES	PROD.	SPEED	SORTS AVAILABLE (ns)	PACKAGE OPTIONS
<b>DYNAMIC RAMS</b>							
TMM4164AP	64KX1	NMOS	YES	YES	150	200	P
TMM41256P	256KX1	NMOS	YES	YES	120	150	P/T
TMM41257P	256KX1	NMOS	YES	YES	120	150	P/T
TMM41464P	64KX4	NMOS	YES	YES	120	150	P
TC511000P/J	1MbX1	CMOS	YES	2Q*86	100	120	P/J
TC511001P/J	1MbX1	CMOS	YES	2Q*86	100	120	P/J
TC511002P/J	1MbX1	CMOS	YES	2Q*86	100	120	P/J
TC514256P/J	256KX4	CMOS	YES	2Q*86	100	120	P/J
TC514258P/J	256KX4	CMOS	YES	2Q*86	100	120	P/J
<b>STATIC RAMS</b>							
TMM2114AP	1KX4	NMOS	YES	YES	120	150	P
TMM2016AP	2KX8	NMOS	YES	YES	90	100 120 150	P
TMM2016BP	2KX8	NMOS	YES	YES	90	100 120 150	P
TMM2015AP	2KX8	NMOS	YES	YES	90	100 120 150	P
TMM2015BP	2KX8	NMOS	YES	YES	90	100 120 150	P
TMM2064P	8KX8	NMOS	YES	YES	100	120 150	P
TMM2063P	8KX8	NMOS	YES	YES	100	120 150	P
TC5504AP	4KX1	CMOS	YES	YES	200	300	P
TC5514AP	1KX4	CMOS	YES	YES	200	300	P
TC5516/17AP	2KX8	CMOS	YES	YES	200	250	PFY
TC5517/18BP	2KX8	CMOS	YES	YES	200	250	PFY
TC5517/18CP	2KX8	CMOS	YES	YES	150	200	PFY
TC5565P	8KX8	*CMOS	YES	YES	120	150	PFY
TC5565AP	8KX8	*CMOS	2Q*86	2Q*86	100	120	PFY
TC5563AP	8KX8	*CMOS	2Q*86	2Q*86	100	120	PFY
TC5564P	8KX8	CMOS	YES	YES	150	200	PY
TC55257P	32KX8	*CMOS	YES	YES	100	120 150	P
<b>HIGH SPEED STATIC RAMS</b>							
TMM2018D	2KX8	NMOS	YES	YES	35	45 55	D
TMM2068D	4KX4	NMOS	YES	YES	35	45 55	D
TMM2078D	4KX4	NMOS	YES	YES	35	45 55	D
TC5561P	64KX1	*CMOS	YES	YES	70		P
TC5562P	64KX1	*CMOS	YES	YES	45	55	P
<b>EPROMS</b>							
TMM2764D	8KX8	NMOS	YES	YES	150	200 250	D
TMM2764DI	8KX8	NMOS	YES	YES	150	200 250	D
TMM2764AD	8KX8	NMOS	YES	YES	150	200	D
TMM27128D	16KX8	NMOS	YES	YES	150	200 250	D
TMM27128DI	16KX8	NMOS	YES	YES	150	200 250	D
TMM27128AD	16KX8	NMOS	YES	YES	150	200	D
TMM27256D	32KX8	NMOS	YES	YES	150	200	D
TMM27256DI	32KX8	NMOS	YES	YES	150	200	D
TMM27256AD	32KX8	NMOS	YES	YES	150	200	D
TC57256D	32KX8	CMOS	YES	YES	200	250	D
TMM27512D	64KX8	NMOS	YES	YES	200	250	D
<b>ONE TIME PROGRAMMABLES</b>							
TMM2464AP	8KX8	NMOS	YES	YES	200		PF
TMM24128AP	16KX8	NMOS	YES	YES	200		PF
TMM24256AP	32KX8	NMOS	YES	YES	200		PF
TMM24512P	64KX8	NMOS	2Q*86	2Q*86	250		PF
<b>MASK ROMS</b>							
TC5364/5/6P	8KX8	CMOS	YES	YES	250		P28
TMM23256P	32KX8	NMOS	YES	YES	150		P28
TC53257P	32KX8	CMOS	YES	YES	200		FP28
TC53512P	64KX8	CMOS	YES	2Q*86	200		P28
TC531000P	128KX8	CMOS	YES	YES	200		P28
TC532000P	256KX8	CMOS	YES	2Q*86	200		P32
P-PLASTIC C-CERAMIC F-FLAT PACK D-CERDIP Y-DIE T-PLCC J-SOJ							
*CMOS = 4 TRANSISTOR CELL LOW POWER							

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UNIX-oriented workstations	UNIX	8086/88,	FORTRAN	Locaters
· Apollo	XENIX	80186/188	PL/M	Compilers
· Sun	MS-DOS	and 80286	Assembler	Symbolic debuggers
· IBM AT		68HC11,		Source-level debuggers
MS-DOS workstations		6800/2/8,		Emulators
· PC		6809/9E,		
· PC XT		68000/8/10		
· PC AT		and 68020		
		Z80, MK3880/4		
		and Z8001/2/3		
		NSC-800		

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**CIRCLE NO 154**

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PAL Family	Generic Part Number	Std MIL Drawing	Replacement JAN Specification Part #	
<b>Small 20 Combinatorial</b>	PAL10H8MJ883B	8103501RA	M38510/50301BRXA	
	PAL10H8ML883B	81035012C	M38510/50301B2XC	
	PAL10H8MF883B	8103501SC	-	
	PAL12H6MJ883B	8103502RA	M38510/50302BRXA	
	PAL12H6ML883B	81035022C	M38510/50302B2XC	
	PAL12H6MF883B	8103502SC	-	
	PAL14H4MJ883B	8103503RA	M38510/50303BRX	
	PAL14H4ML883B	81035032C	M38510/50303B2X	
	PAL14H4MF883B	8103503SC	-	
	PAL16H2MJ883B	8103504RA	M38510/50304BRX	
	PAL16H2ML883B	81035042C	M38510/50304B2X	
	PAL16H2MF883B	8103504SC	-	
	PAL16C1MJ883B	8103505RA	M38510/50305BRX	
	PAL16C1ML883B	81035052C	M38510/50305B2X	
	PAL16C1MF883B	8103505SC	-	
	PAL10L8MJ883B	8103506RA	M38510/50306BRX	
	PAL10L8ML883B	81035062C	M38510/50306B2X	
	PAL10L8MF883B	8103506SC	-	
	PAL12L6MJ883B	8103507RA	M38510/50307BRX	
	PAL12L6ML883B	81035072C	M38510/50307B2X	
	PAL12L6MF883B	8103507SC	-	
	PAL14L4MJ883B	8103508RA	M38510/50308BRX	
	PAL14L4ML883B	81035082C	M38510/50308B2X	
	PAL14L4MF883B	8103508SC	-	
	PAL16L2MJ883B	8103509RA	M38510/50309BRX	
	PAL16L2ML883B	81035092C	M38510/50309B2X	
	PAL16L2MF883B	8103509SC	-	
	<b>Medium 20A</b>	PAL16L8AMJ883B	8103607RA	M38510/50401BRX
		PAL16L8AML883B	81036072C	M38510/50401B2X
		PAL16L8AMW883B	8103607SA	-
PAL16R8AMJ883B		8103608RA	M38510/50402BRX	
PAL16R8AML883B		81036082C	M38510/50402B2X	
PAL16R8AMW883B		8103608SA	-	
PAL16R6AMJ883B		8103609RA	M38510/50403BRX	
PAL16R6AML883B		81036092C	M38510/50403B2X	
PAL16R6AMW883B		8103609SA	-	
PAL16R4AMJ883B		8103610RA	M38510/50404BRX	
PAL16R4AML883B		81036102C	M38510/50404B2X	
PAL16R4AMW883B		8103610SA	-	
<b>Medium 20A-2 1/2 Power</b>		PAL16L8A-2MJ883B	8103611RA	M38510/50407BRX
		PAL16L8A-2ML883B	81036112C	M38510/50407B2X
	PAL16L8A-2MW883B	8103611SA	-	
	PAL16R8A-2MJ883B	8103612RA	M38510/50408BRX	
	PAL16R8A-2ML883B	81036122C	M38510/50408B2X	
	PAL16R8A-2MW883B	8103612SA	-	
	PAL16R6A-2MJ883B	8103613RA	M38510/50409BRX	
	PAL16R6A-2ML883B	81036132C	M38510/50409B2X	
	PAL16R6A-2MW883B	8103613SA	-	
	PAL16R4A-2MJ883B	8103614RA	M38510/50410BRX	
	PAL16R4A-2ML883B	81036142C	M38510/50410B2X	
	PAL16R4A-2MW883B	8103614SA	-	

#### Military Package Designators:

R = 20 lead 1/4 x 1 1/16 dual-in-line  
S = 20 lead 1/4 x 1/2 Flatpack  
2 = 20 Terminal .350 x .350 Leadless Chip Carrier

K = 24 lead 3/8 x 3/8 Flatpack  
L = 24 lead 1/4 x 1 1/4 Dual-in-Line  
3 = 28 Terminal .450 x .450 Leadless Chip Carrier

#### MMI Package Designators:

J = Ceramic DIP  
F = Bottom Brazed Flatpack  
L = Leadless Chip Carrier  
W = Cerpak  
JS = 24 pin Cerdip



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PAL Family	Generic Part Number	Std MIL Drawing	Replacement JAN Specification Part #	
<b>Medium 24A</b>	PAL20L8AMJS883B	8412901LA	M38510/50501BJX	
	PAL20L8AML883B	84129013C	M38510/50501B3X	
	PAL20L8AMW883B	8412901KA	-	
	PAL20R8AMJS883B	8412902LA	M38510/50502BJX	
	PAL20R8AML883B	84129023C	M38510/50502B3X	
	PAL20R8AMW883B	8412902KA	-	
	PAL20R6AMJS883B	8412903LA	M38510/50503BJX	
	PAL20R6AML883B	84129033C	M38510/50503B3X	
	PAL20R6AMW883B	8412903KA	-	
	PAL20R4AMJS883B	8412904LA	M38510/50504BJX	
	PAL20R4AML883B	84129043C	M38510/50504B3X	
	PAL20R4AMW883B	8412904KA	-	
	<b>Medium 24XA Exclusive OR</b>	PAL20L10AMJS883B	8412905LA	-
		PAL20L10AML883B	84129053C	-
PAL20X8AMJS883B		8412906LA	-	
PAL20X8AML883B		84129063C	-	
PAL20X10AMJS883B		8412907LA	-	
PAL20X10AML883B		84129073C	-	
PAL20X4AMJ883B		8412908LA	-	
PAL20X4AML883B		84129083C	-	
<b>Medium 20A-4 1/4 Power</b>	PAL16L8A-4MJ883B	8506501RA	-	
	PAL16L8A-4ML883B	85065012C	-	
	PAL16R8A-4MJ883B	8506502RA	-	
	PAL16R8A-4ML883B	85065022C	-	
	PAL16R6A-4MJ883B	8506503RA	-	
	PAL16R6A-4ML883B	85065032C	-	
	PAL16R4A-4MJ883B	8506504RA	-	
	PAL16R4A-4ML883B	85065042C	-	
<b>Medium 20B</b>	PAL16L8BMJ883B	8515501RA	-	
	PAL16L8BML883B	85155012C	-	
	PAL16R8BMJ883B	8515502RA	-	
	PAL16R8BML883B	85155022C	-	
	PAL16R6BMJ883B	8515503RA	-	
	PAL16R6BML883B	85155032C	-	
	PAL16R4BMJ883B	8515504RA	-	
	PAL16R4BML883B	85155042C	-	
<b>Medium 20B-2 1/2 Power</b>	PAL16L8B-2MJ883B	8515505RA	-	
	PAL16L8B-2ML883B	85155052C	-	
	PAL16R8B-2MJ883B	8515506RA	-	
	PAL16R8B-2ML883B	85155062C	-	
	PAL16R6B-2MJ883B	8515507RA	-	
	PAL16R6B-2ML883B	85155072C	-	
	PAL16R4B-2MJ883B	8515508RA	-	
	PAL16R4B-2ML883B	8515508SA	-	

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# Your move.



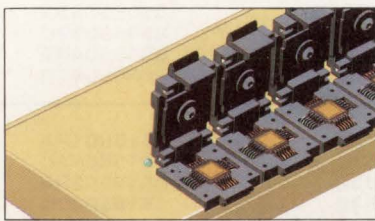
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# NEWS BREAKS

EDITED BY JOAN MORROW

## **COMPLIANT PINS ELIMINATE SOLDER IN PC-BOARD ASSEMBLY**

If you want to avoid soldering to attach edge connectors to multilayer pc boards, consider a compliant-pin edge connector from Viking Connectors Co (Chatsworth, CA, (818) 342-4330). Because the connection is mechanical rather than soldered, you eliminate solder touch-up from the assembly process. In addition, heat associated with solder is not concentrated in a small board area. The compliant section of the pin, which resembles the eye of a needle, provides a gas-tight joint without causing damage to the plated-through hole; individual pins can be removed and replaced several times. The technology is approved for military applications (MIL-STD-2166). Price is \$0.03 per contact (10,000).—Margery S Conner

## **2-CHIP MODEM OPERATES TO 2400 BPS**

The 89024 integrated chip set from Intel (Santa Clara, CA) consists of the 89026 processor and the 89027 analog front end. The chip set supports full-duplex operation for data speeds of 0 to 2400 bps and conforms to Bell 103 and 212A and CCITT V.21, V.22 A & B, and V.22 bis. The 89024 also includes the complete Hayes command set and can be used as a stand-alone modem without an external microcontroller. Samples are available now; production shipments are scheduled for the second quarter. The chip set costs \$35 (25,000).—David Shear

## **SERVO CHIP SET INCLUDES ANALOG AND DIGITAL CIRCUITS**

By using Silicon Systems' (Tustin, CA, (714) 731-7110) 3-chip set, which includes the SSI 567 servo demodulator, SSI 568 servo controller, and SSI 569 servo motor driver, you need only add a  $\mu$ P and passive components for a complete disk-drive servo-control system. Servo systems such as those used to control disk-drive head movement have typically required a pc board full of discrete components. The demodulator IC specifically targets dibit quadrature Winchester-disk servo applications, but the controller and motor driver chips will fit general-purpose servo systems for applications such as robotics. In Winchester-disk applications, the chip set targets designs that pack 1500 tpi max and operate at less than 20 msec average seek time. The company plans to ship samples of the chip set in the first quarter and production quantities in the second quarter. The 3-chip set will cost less than \$35 (10,000).—Maury Wright

## **DESIGNER'S KIT EASES BUILDING-BLOCK DSP EVALUATION**

Logic Devices Inc's (Sunnyvale, CA, (408) 720-8630) Designer Chips tool kit includes an application note and 11 high-performance devices and sockets that allow the engineer experimenting in digital-signal processing to create a high-performance FFT subsystem. You can then design a complete system that should sample at 2 MHz and perform a 1024-point complex FFT in 0.5 msec. The kit costs \$264, which is 40% less than the cost of the individual components.—David Shear

## **BOARD SIMPLIFIES IEEE-488 INSTRUMENT-CONTROL PROGRAMMING**

Operating as an intelligent IEEE multicontroller, the 500-IEEE from Keithley Instruments Inc (Cleveland, OH, (216) 248-0400) is an instrument-control card that lets you simplify the programming needed to control as many as 14 IEEE-488 instruments. Sporting its own  $\mu$ P, the \$650 board integrates high-level IEEE control into single-line commands, resulting in programs that are easy to read and write. The 500-IEEE plugs into a Keithley Series 500 scientific workstation or a Keithley System 570 data-acquisition workstation, instead of monopolizing a slot in your personal com-

# NEWS BREAKS

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puter. You can use the board to implement serial and parallel polling, provide low-level bus control, and handle the input and output of strings, numeric data, and arrays. Software-programmable terminators guarantee compatibility with all IEEE instruments.—J D Mosley

## **SOFTWARE OPTIONS SOLVE 16-BIT- $\mu$ P TRIGGER PROBLEMS**

Two software options for the Echo development system from Arium Corp (Anaheim, CA, (714) 978-9531), Firmbreak and Stacktop, solve triggering problems for 16-bit microprocessor-based designs. With the Firmbreak software addition to the Echo  $\mu$ P development system, you can insert a firmware-based trap point to debug software for 16-bit  $\mu$ P-based designs. Unlike hardware-based traps, which can be confused by a word that's prefetched but not executed, Firmbreak can recognize an instruction's execution; it then overlays the instruction with a software interrupt that vectors the program to debug code.

Because a 16-bit microprocessor doesn't determine a stack-relative variable's address until execution time, you can have trouble triggering on the variable or its value. (These variables make up 30 to 40% of program variables in C language.) Stacktop determines the dynamically allocated address, allowing you to trigger on the variable as it executes. Echo systems sold until March 15 will include the options in the price of \$12,980; after that date, the options alone will cost \$895.—Margery S Conner

## **PERIPHERAL-CONTROLLER CHIP TARGETS EMBEDDED APPLICATIONS**

Adaptec (Milpitas, CA, (408) 432-8600) now offers a peripheral-controller IC that includes a programmable storage controller, a dual-port buffer controller, and buffer addressing logic. The IC, Model AIC-610, targets manufacturers embedding a system-bus (IBM PC, VME Bus, etc) or SCSI-bus interface on a controller board. Designs that use the controller IC will support a 15-MHz data-transfer rate at the device and 1.5M-byte/sec bus transfers. You can program the chip to work with disk and tape encoding schemes such as 2,7 RLL; 1,7 RLL; and MFM. The IC performs 48-bit ECC and will correct errors 19 bits long. A 10-MHz version costs \$23 (1000). Expect shipment of the \$34.50 (1000) 15-MHz part in the second quarter.—Maury Wright

## **SECOND-SOURCE AGREEMENT COVERS CUSTOM GaAs**

Ford Microelectronics Inc (Colorado Springs, CO) and Vitesse Electronics Corp (Camarillo, CA) have announced an agreement to provide alternate sourcing for foundry production of custom LSI gallium arsenide ICs. This agreement begins at the design-rule level of the enhancement/depletion self-aligned gate process, allowing customers to have their circuits produced by either of the two suppliers.—David Shear

# There's more here than meets the eye.

Product	Resolution (Bits)	Conversion Rate (MSPS)	Bandwidth (MHz)
TDC1019-1	9	18	5
TDC1019	9	15	5
TDC1048	8	20	7
TDC1025	8	50	12.5
TDC1007	8	20	7
TDC1002	8	1.0	N/A*
TDC1001	8	2.5	N/A*
**TDC1047	7	20	7
**TDC1147	7	15	12.5
TDC1046	6	25	50
TDC1029	6	100	12
TDC1014	6	25	10
TDC1021	4	25	12.5
**TDC1044	4	25	

\* Successive Approximation

\*\* New

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# NEWS BREAKS: INTERNATIONAL

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## **TWO COMPANIES TO INTRODUCE 1M-BIT EPROMs, DEVELOP 4M-BIT DEVICES**

Thomson Semiconducteurs (Paris, France, TLX 204780) and SGS-Microelettronica SpA (Agrate Brianza, Italy, TLX 330131) both plan to introduce 1M-bit CMOS EPROMs this year. Thomson Semiconducteurs will present its 64k×16-bit 40-pin 27C1024 and the 128k×8-bit 32-pin 27C1001. Both devices, which are expected to sell at around \$25 (1000), will feature a 150-nsec access time and an operating current of approximately 50 mA. You can expect to see SGS-Microelettronica's 1M-bit EPROM offerings during the second or third quarter of 1987.

In addition, the two companies have entered into an agreement, as part of the European Eureka project, to jointly develop 4M-bit CMOS EPROMs using 0.8- $\mu$ m design rules. They will also study the feasibility of 16M-bit devices using design rules below 0.5  $\mu$ m. The development project, which is expected to run for five years, will cost each company around \$200 million.—Peter Harold

## **JAPANESE GOVERNMENT TO ESTABLISH SOFTWARE REGISTRY**

In an effort to stem piracy and protect the rights of software developers, the Ministry of International Trade and Industry and the Education Ministry will set up an organization for registering computer software. Scheduled to begin operation in April, the Software Information Center has approximately 60 companies and computer-related organizations as sponsors. The center will register and store applications programs and operating systems on microfiche for 50 years, a duration stipulated by a recent copyright law. The center will also study and collect data on how other countries handle software-piracy disputes.—Joan Morrow

## **VME BUS CPU CARD FEATURES 80386 $\mu$ P**

Based around a 16-MHz 80386  $\mu$ P, the CPU-386 VME Bus CPU board from Force Computers GmbH (Ottobrunn, West Germany, TLX 524190) allows you to implement 8086-family operating systems in a VME Bus hardware environment. The processor has zero-wait-state access to 2M bytes of onboard RAM and zero-wait-state access to additional off-board RAM via a local memory-expansion bus. The board also includes sockets for as much as 512k bytes of EPROM and an 80387 math coprocessor. Its VME Bus interface is VME Bus Rev.C1 compatible and provides slot-1 functions, which include SYCLK generation, a 4-level bus arbiter, and bus time-outs. It supports 8-, 16-, 24-, and 32-bit VME Bus transfers including unaligned transfers and dynamic bus sizing. The CPU-386 costs DM 14,950.—Peter Harold

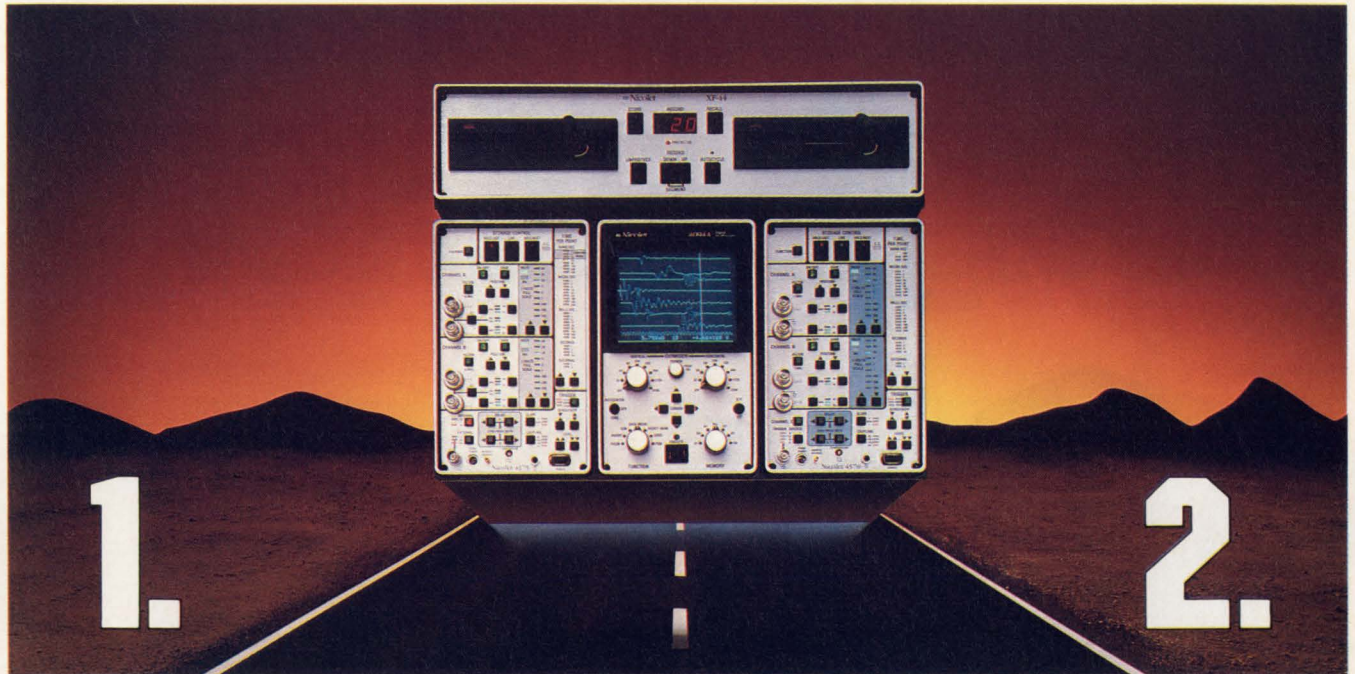
## **16-BIT HOME COMPUTER USES THE MC68000 $\mu$ P**

The X68000 home computer from Sharp Corp is based on Motorola's 68000 and features 1M byte of memory (12M bytes max). The ¥369,000 (\$2237) system uses a proprietary operating system and comes with a standard 512×512-dot display. The computer uses the virtual-screen method to allow expanding images to four times their normal size. It can also accommodate video digitizers and three-dimensional image adapters.—Joan Morrow

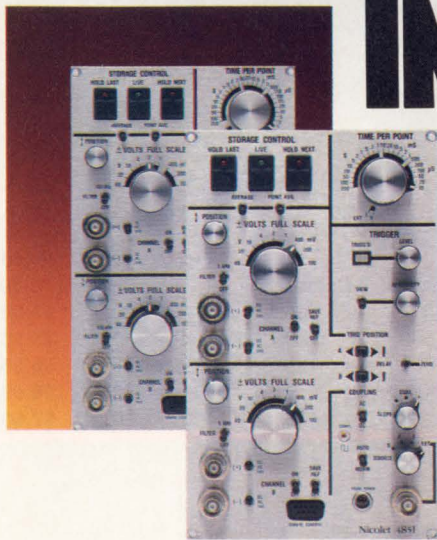
## **64k-BIT CMOS STATIC RAM HAS 25-nSEC MAX ACCESS TIME**

The M5M5187AP Series 64k-bit CMOS static RAM features a 25-nsec max access time and is organized as 64k words×1 bit. The device, which is housed in a 300-mil, 22-pin standard package, provides separate pins for input and output. The 3.69×6.35-mm chip samples for approximately ¥4800 (\$29).—Joan Morrow

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## The Analysis.

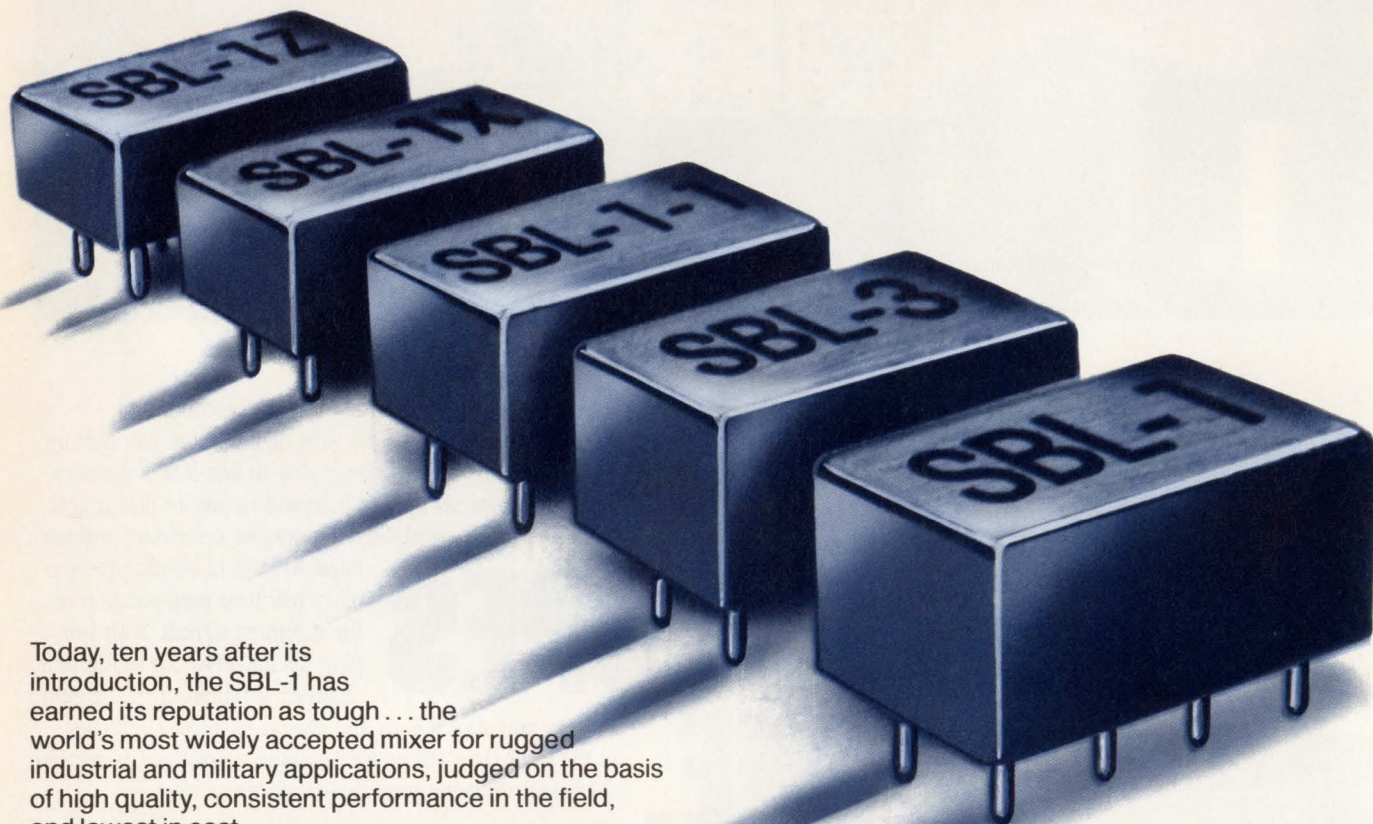
Expand and examine any waveform feature in detail. Use the dual cursors and numerics to measure the time or voltage of any point. Compare live or stored waveforms with each other or with pre-recorded references. Store signals on disk manually or automatically. Use pushbutton programs to manipulate the data or send it to your computer via GPIB or RS232 interface. Complete your report with a hardcopy plot using the XY/YT recorder or digital plotter outputs.

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## SBL SPECIFICATIONS (typ.)

Model	Freq. (MHz)	Conv. Loss	Isolation, dB		Price (10-49)
			L-R	L-I	
SBL-1	1-500	5.5	45	40	\$4.50
* SBL-1X	10-1000	6.0	40	40	\$5.95
SBL-1Z	10-1000	6.5	35	25	\$6.95
SBL-1-1	0.1-400	5.5	35	40	\$6.50
SBL-3	0.25-200	5.5	45	40	\$7.50

\* If not DC coupled.

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**CIRCLE NO 155**

LOW PASS	Model	*LP-	10.7	50	70	100	150	200	300	450	550	600	750	850	1000
Min. Pass Band (MHz) DC to			10.7	48	60	98	140	190	270	400	520	580	700	780	900
Max. 20dB Stop Frequency (MHz)			19	70	90	147	210	290	410	580	750	840	1000	1100	1340

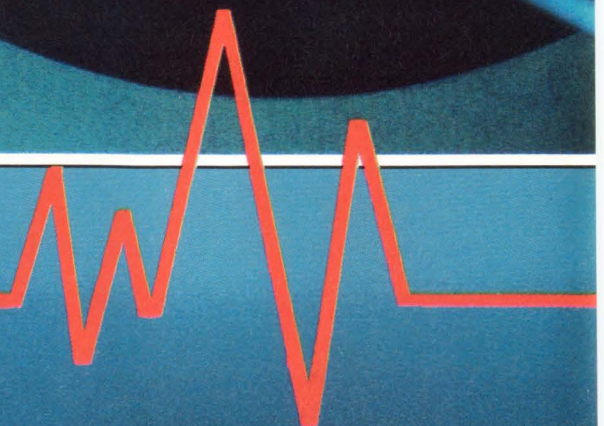
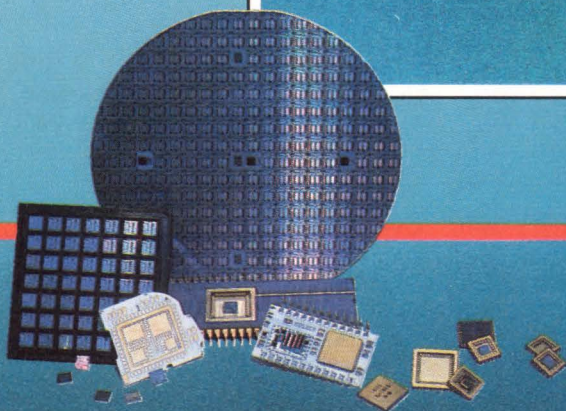
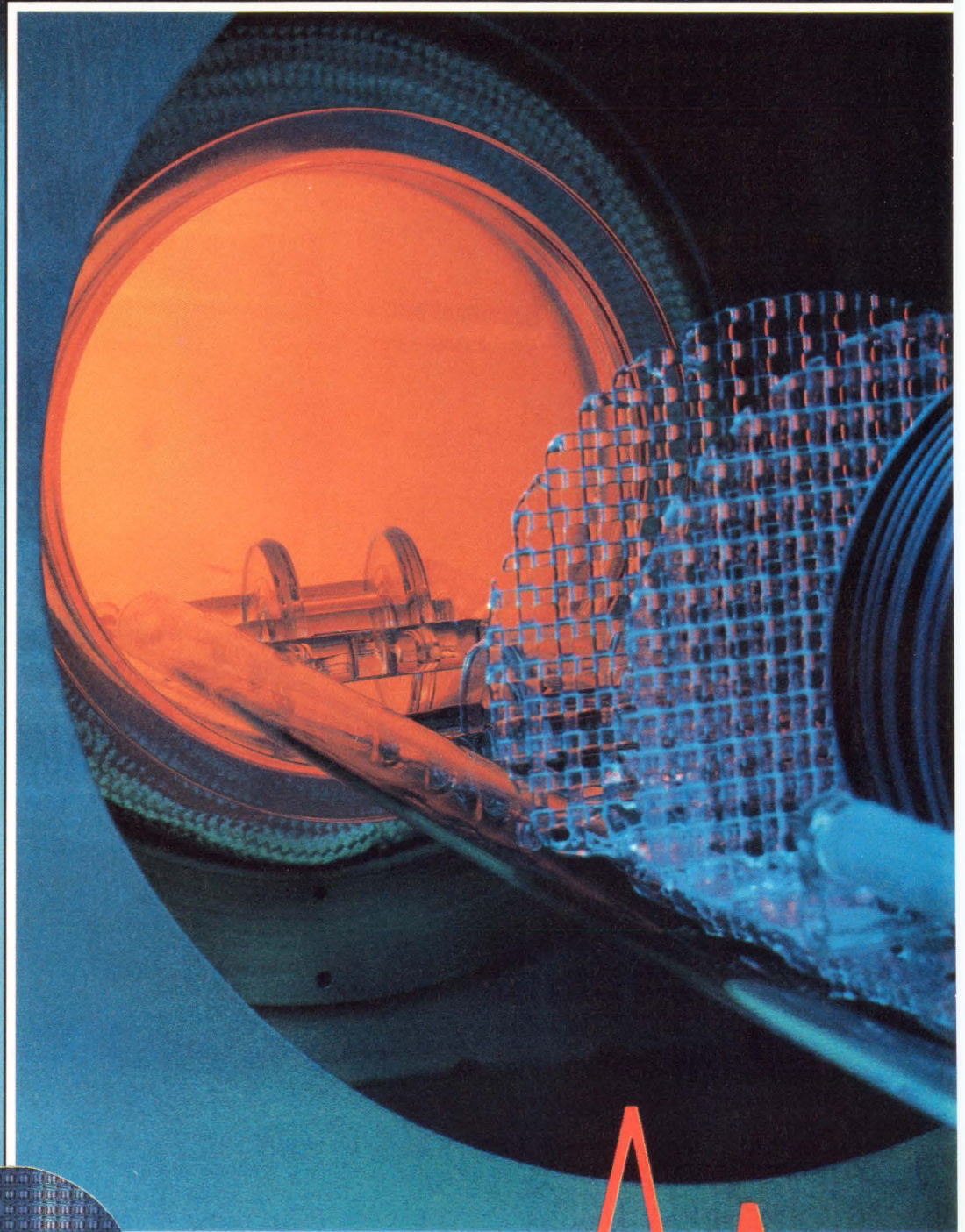
Prices (ea.): P \$9.95 (6-49), B \$24.95 (1-49), N \$27.95 (1-49), S \$26.95 (1-49)

HIGH PASS	Model	*HP-	50	100	150	200	300	400	500	600	700	800	900	1000
Pass Band (MHz)	start, max.		41	90	133	185	290	395	500	600	700	780	910	1000
	end, min.		200	400	600	800	1200	1600	1600	1600	1800	2000	2100	2200
Min. 20dB Stop Frequency (MHz)			26	55	95	116	190	290	365	460	520	570	660	720

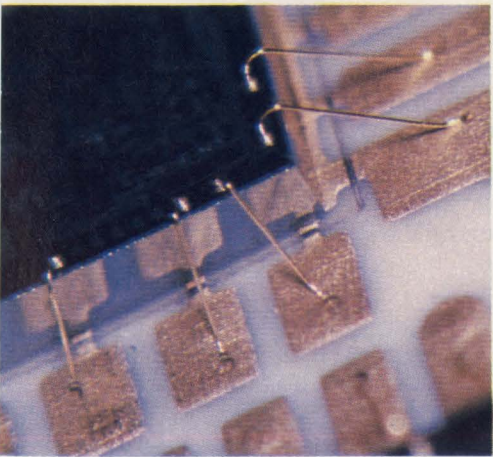
Prices (ea.): P \$12.95 (6-49), B \$27.95 (1-49), N \$30.95 (1-49), S \$29.95 (1-49)

\*Prefix P for pins, B for BNC, N for Type N, S for SMA *example: PLP-10.7*

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**2.** Our military certification. In addition to MIL-STD-883C, we were one of the first 12 companies to attain certification to MIL-STD-1772 by DESC; we expect to have full 1772 qualification by mid-1987. And we're the only company with multilayer cofired ceramics capabilities.

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increasing performance and reliability.

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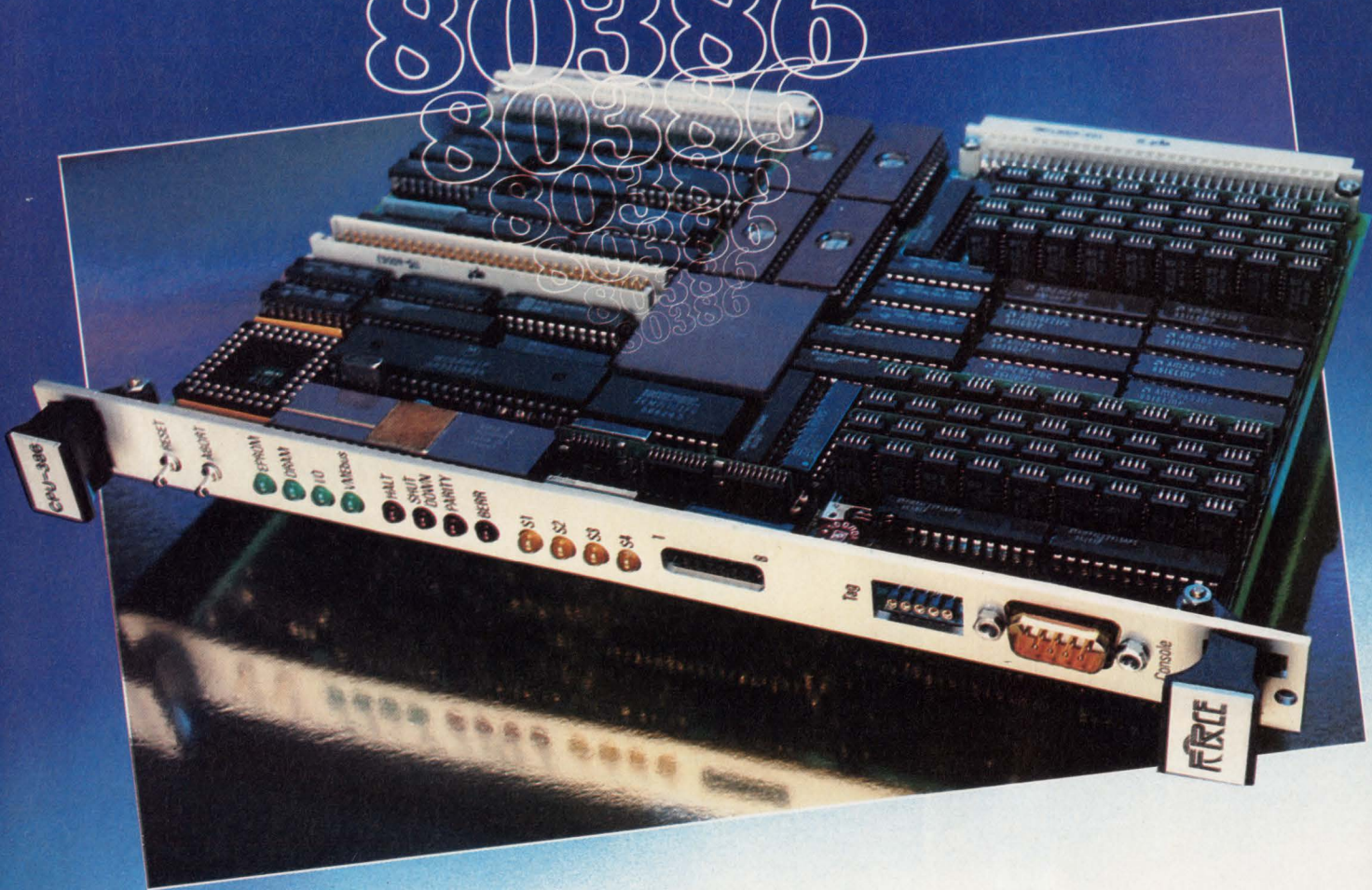
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CIRCLE NO 147



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# 80386



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Processor	68020*	68020*	68020*	68020*	80386*	80386*
Available frequencies	12.5/16.7/ 20/25	12.5/16.7/ 20/25	12.5/16.7/ 20	12.5/16.7/ 20	12/16/20	12/16/20
Number of wait states	0	0	1	1	0 (1 at 20 MHz)	
FPU	no	yes	no	yes	no	yes
MMU	no	no	yes	yes	yes	yes
Memory capacity	0.5 to 4 MB SRAM		0.5 to 4 MB SRAM		2 to 8 MB DRAM	
EPROM capacity	512 KB	512 KB	64 KB	64 KB	256 KB	256 KB
Serial I/O channels	3	3	3	3	3	3

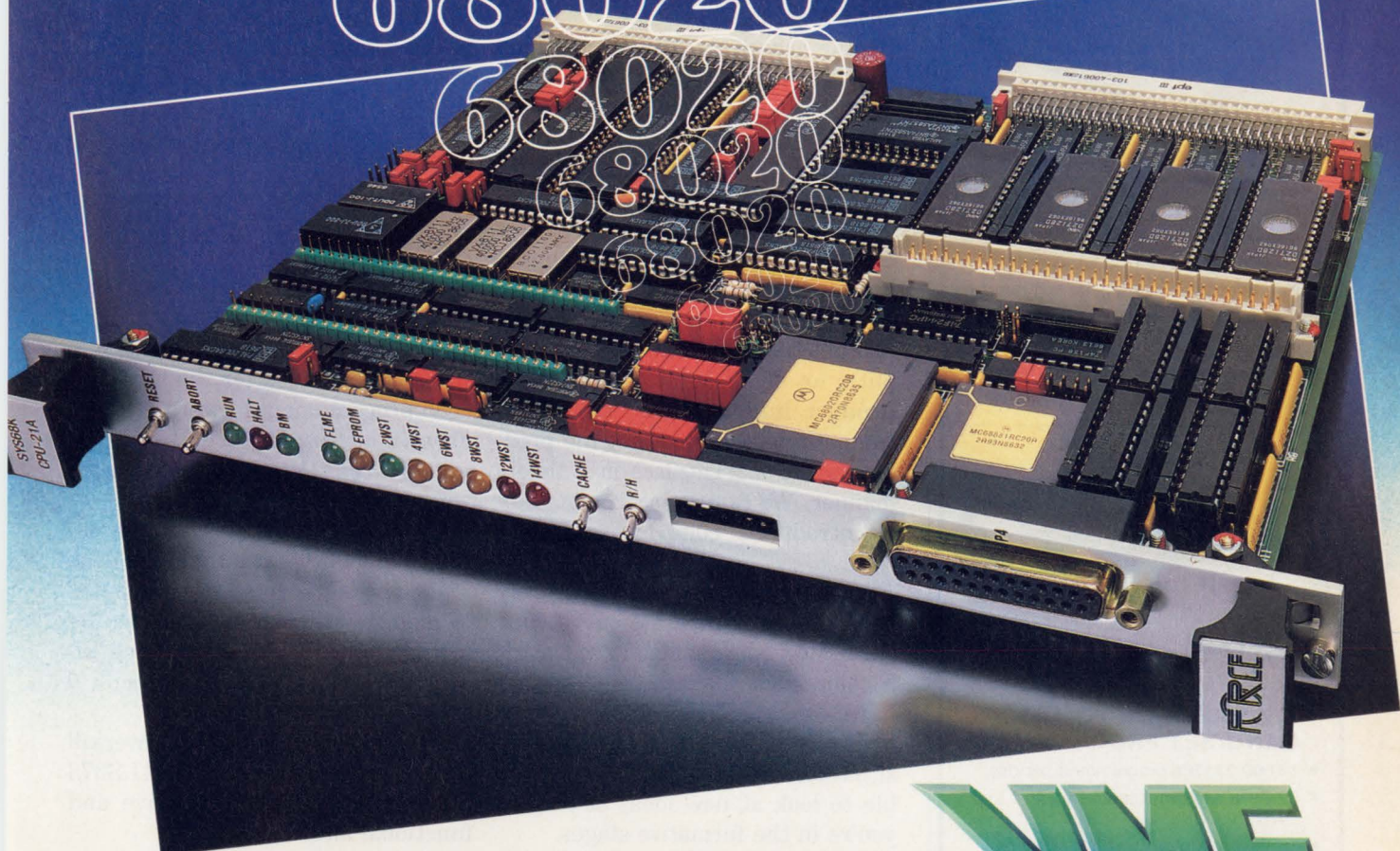
# 68020 ?

# 68020

# 68020

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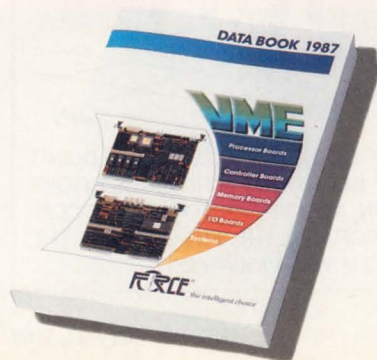
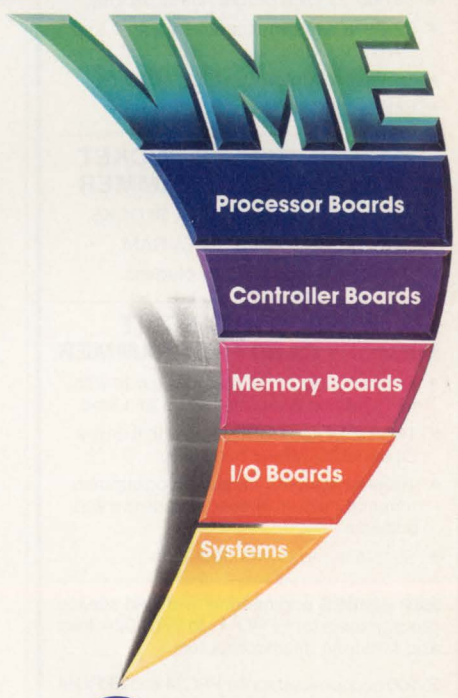
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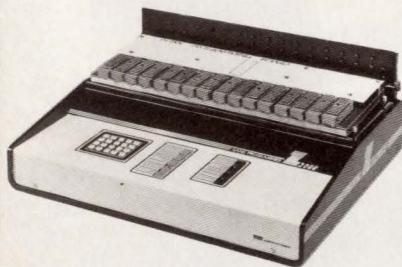
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# SIGNALS & NOISE

## OEMs can't design with vaporware

Dear Editor:

Please accept my compliments on your editorial in the May 1, 1986, issue of EDN (pg 49). I copied and circulated it throughout our company and received nothing but positive feedback on it.

Because we use a tremendous number of electronic components but do not manufacture any, we must rely entirely on component manufacturers for these parts. We put a lot of R&D into a product or product improvement, and to be competitive, we must get the product to the marketplace in a timely manner. We cannot incorporate "to-be-introduced" components in a design.

Your survey results accurately represent our interest curve. Our specifying curve amounts to this: If a component manufacturer doesn't have a part in hand, we don't want it. As for long-term planning, the situation is as you stated—it's feasible to look at new ideas as long as you're in the formative stages.

A situation similar to the one you describe occurs when a company promotes a nonexistent product to suppress competition, yet never delivers that product. We have been faced with that problem many times. Again, many thanks for an excellent article.

Sincerely yours,  
Craig Nelson  
Applications Engineer  
Multi-Amp Corp  
Dallas, TX

## Tips on designing with the 8035 $\mu$ C

Dear Editor:

I read the article "Use CMOS DACs to generate sine waves" (EDN, August 21, pg 167) with great interest, but the article seems to be incomplete. I would like to offer some tips or comments that might help someone who decides to build the 8035

microcontroller circuit described in the article.

First, from the article one would assume that the actual software generation necessary to facilitate constant look-up is an exercise left to the reader. It would have been more prudent to include a flow-chart, at worst, or a simple machine-language program in binary or mnemonic form, at best.

Because the 8035 uses quasi-bidirectional port structure, bank switching, and other unusual features, a good book for the would-be 8035 programmer is Intel's *MCS-48 Family of Single Chip Microcomputers User's Manual*, which helps you understand the processor.

Because the 2732 is easier to obtain, it should be used in lieu of the 2716. The 8035 can address 2k bytes of memory directly or 4k bytes by using memory-bank switching instructions (select memory bank 0 or 1).

The 8212 latch constitutes overkill for a simple system; the 74LS373 octal latch is a cost-effective and functional alternative.

Port pins 27 to 32 use 50 k $\Omega$  of internal pullups, making any external resistors unnecessary.

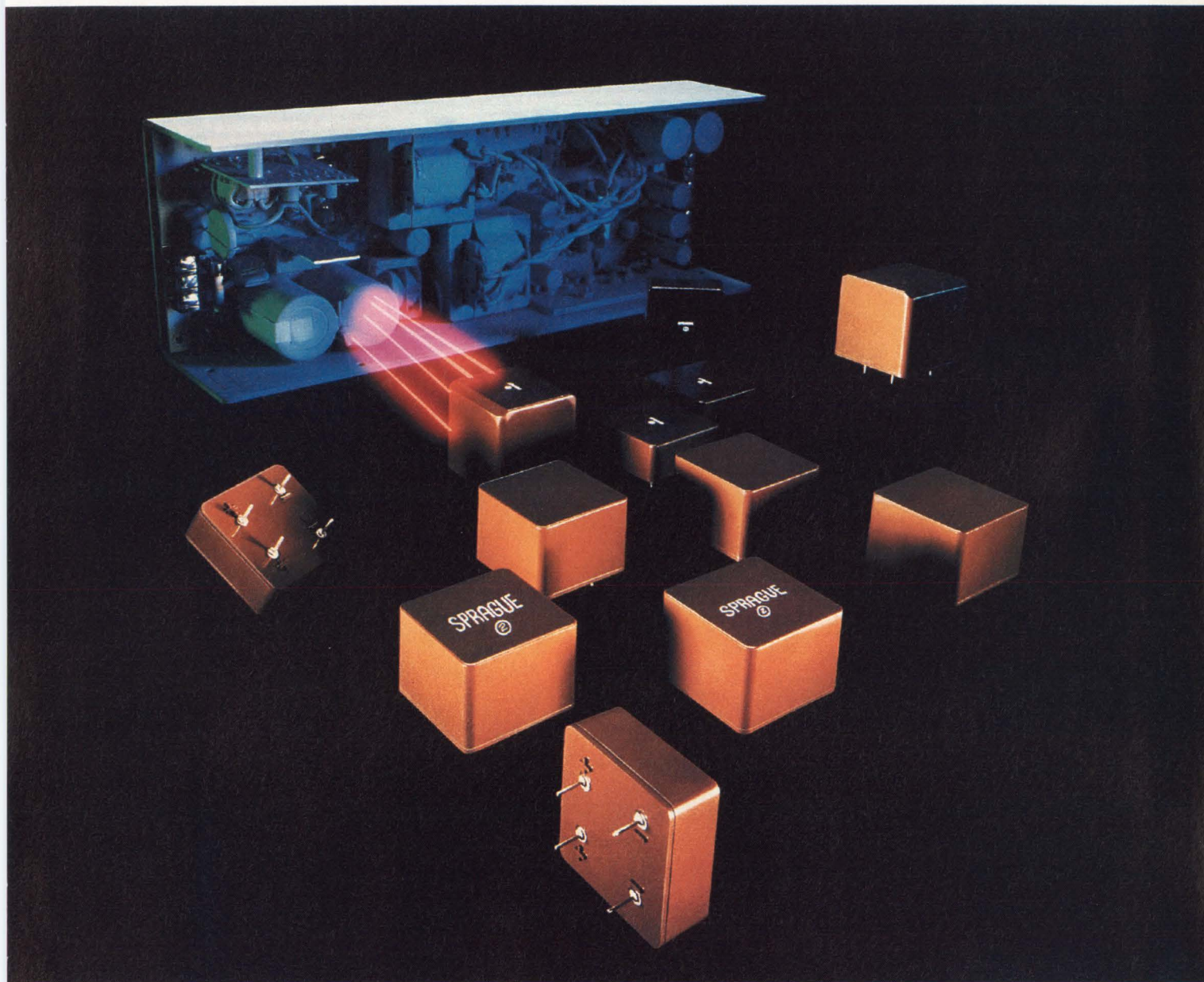
The instruction cycle is the useful clock sequence for this system and is the external crystal frequency di-

Text continued on pg 34



"BUT BOB, THIS IS 1987... YOU DON'T JUST BLURT OUT, 'THE LINES BROKE DOWN.' YOU'VE GOT TO USE THE CONTEMPORARY, 'THE INTEGRITY OF THE SYSTEM WAS VIOLATED!'"

# YOUR NEW SMPS CAPS.



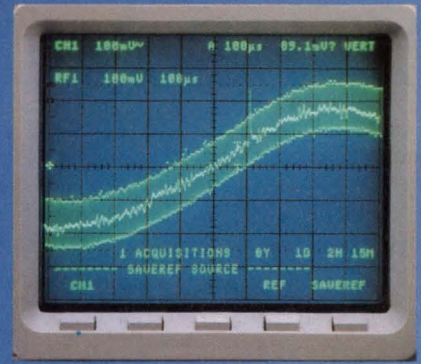
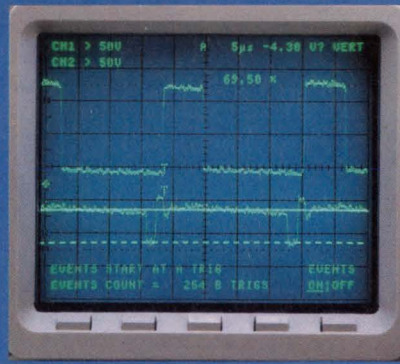
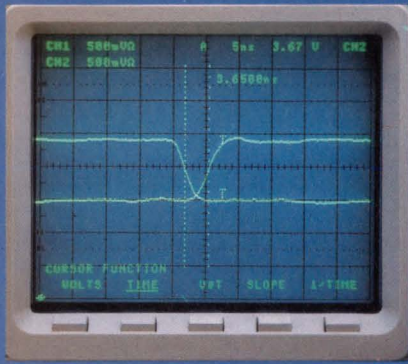
4SE-6138

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Sprague Type 88D computer-grade molded-case aluminum electrolytic capacitors are designed for switched-mode power supply input and output filter applications. Feature high package density, low ESR and low inductance. Polarity-keyed four-terminal packages ideal for PC board mounting. Internal bus bar design withstands high ripple current. Single-section capacitors in two case sizes: 1.625" x 1.625" x 0.690" or 1.181". Ratings from 47,000  $\mu\text{F}$ , 3 WVDC to 56  $\mu\text{F}$ , 450 WVDC. Dual-section capacitors in case size 1.625" x 1.625" x 1.576". Capacitance values from 330  $\mu\text{F}$  to 680  $\mu\text{F}$ ; voltage ratings 200 WVDC and 250 WVDC. Operating temperature range:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . Sprague Electric Company, a Penn Central unit. For applications assistance call your local Sprague sales office or representative. For Data Sheet 3161, write to Technical Literature Service, Sprague Electric Co., P.O. Box 9102, Mansfield, MA 02048-9102.



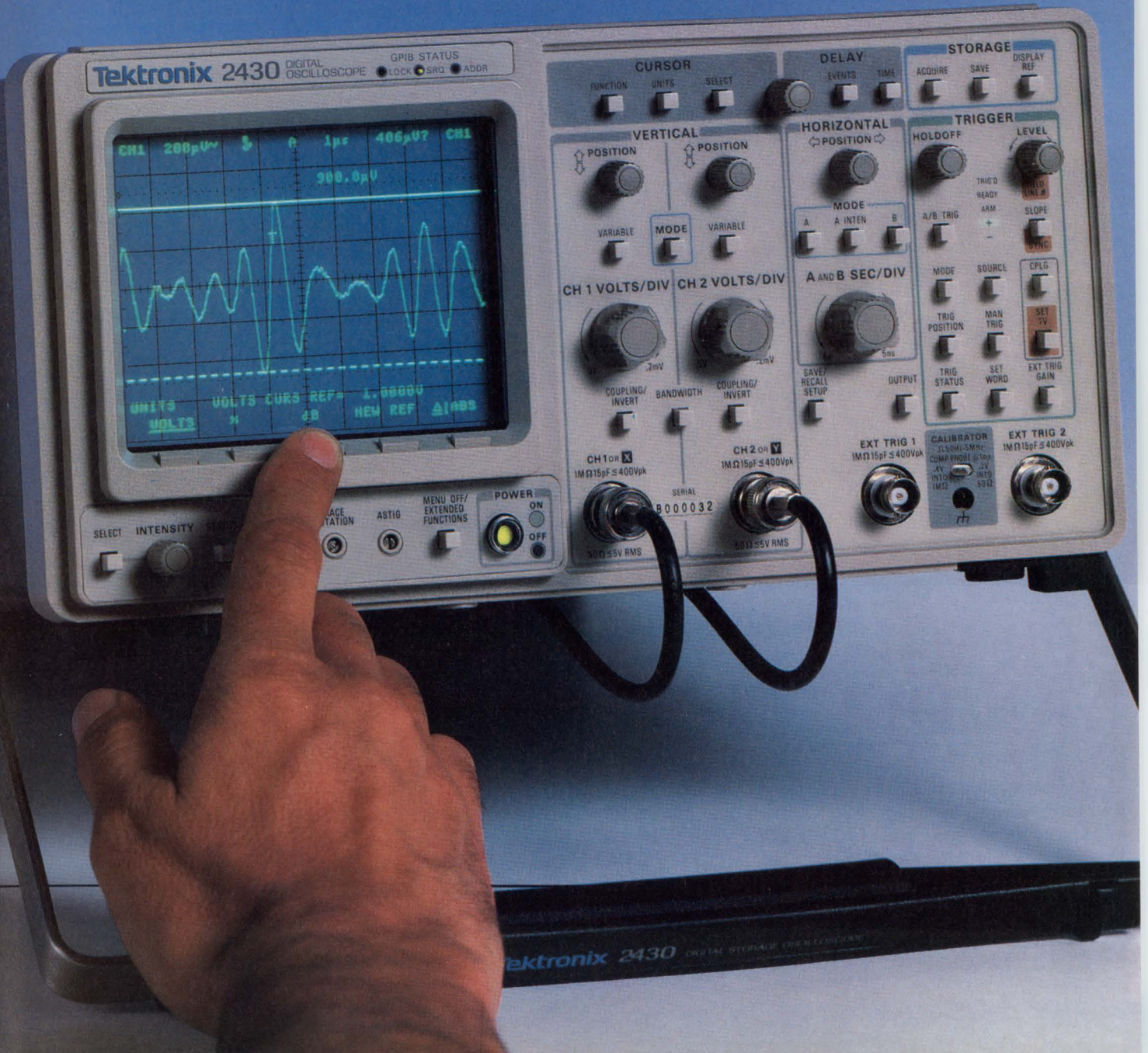
CIRCLE NO 130



With its 150 MHz bandwidth, 5 ns/div maximum sweep speed and 2-channel simultaneous acquisition, the 2430 displays TTL and ECL signals for risetime and coincidence measurements. (Above) The scope is used in 50 ohm input termination with a 500 ohm probe for an accurate measurement of propagation delay through an ECL inverter.

How long does it take a transformer to reach operating voltage? Using DELAY BY EVENTS, the 2430 lets you select the 254th (or any other) switching event of the pulse-width modulator in a high-efficiency power supply.

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Add 8-bit vertical resolution, 1K record length per channel and a 0.01% crystal-controlled timebase for making accurate measurements with ease.

The result: an advanced measurement package with many sophisticated capabilities built in especially for solving tough product design problems.

**All-purpose high performance at its affordable best!** The 2430 not only handily meets your general purpose measurement needs, it gives you a lot more. With digital



DAC glitches won't escape you with the 2430's enhanced ENVELOPE function. The peak-detecting ENVELOPE mode enables you to catch events as narrow as 2 ns, even with a single acquisition, at any sweep speed.

capabilities come powerful waveform manipulation functions ranging from waveform multiplication to high-resolution averaging.

It is also fully programmable via the GPIB. Complete talk/listen capabilities extend the scope's power and make it a valuable systems component for making automatic measurements. You can develop test procedures that can be used later on the manufacturing floor. Plus, the time-consuming task of waveform characterization, analysis and logging is simplified.

In addition, the 2430 can store waveforms and front panel setups in nonvolatile memory.

**The 2430 exhibits unusual power as a troubleshooting tool.** The patented peak detection circuit lets you capture glitches as narrow as 2 ns at any sweep speed with confidence—a level of performance available until now in only the most expensive instruments.

The 2430's envelope mode, which automatically captures and updates signal minimums and maximums, allows you to conveniently study signal variations such as jitter, drift and stability. It also monitors signal excursions outside user-defined limits.

Plus, a broad range of pretrigger selections available in all modes makes it possible to examine conditions leading up to an event. The crystal-controlled timebase allows you to delay by time and/or events for precise timing measurements in complex triggering modes. You can even trigger on digital words.

**Best of all, we've kept the 2430 easy to use.** From the simple, one-level menus for standard functions to the comfortable grouping of the front panel controls, the 2430 was designed to drive like the scopes you already use.



With full programmability you can improve repeatability and throughput—and reduce operator interface requirements.

The enhanced capabilities of the 2430's time and voltage cursors are another convenience, enabling you to make accurate measurements of all essential parameters.

**The reliability of the 2430 is underwritten with a 3-year warranty.** A variety of low-cost service plans can extend this coverage even further.

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CIRCLE NO 124

vided by 3, then divided again by 5. This instruction cycle is used in software-generated nested loops for time delays, etc.

I hope these tips will help in the design of a practical circuit.

*Sincerely yours,  
Joseph G Bogar  
Teledyne Microelectronics  
Los Angeles, CA*

## MIL-STD-883 S/R converters

Dear Editor:

The last sentence of the Technology Update article entitled "Synchro/resolver converters bring low cost and small size to motion-control systems" (EDN, October 30, pg 61) implies that Analog Devices and Natel Engineering are eligible to

supply hybrid synchro converters screened per MIL-STD-883.

In fact, Analog Devices' synchro/resolver converters are manufactured by its Memory Devices Div in the UK, but only the company's Wilmington, MA, and Greensborough, NC, facilities have been certified and scheduled for qualification. Natel Engineering is not certified or qualified, and as of October 2, 1986, the company has not even been scheduled for the initial audit.

According to the Defense Electronics Supply Center (DESC) list of companies involved in the MIL-STD-1772 program, ILC Data Device Corp is the only synchro/resolver-converter manufacturer that is permitted to supply MIL-STD-883 hybrids.

*Sincerely yours,  
Steve Muth, VP  
ILC Data Device Corp  
Bohemia, NY*

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## Oops

Readers of EDN's standard-cell directory (October 2, 1986, pg 63) who thought that SLOA and SLOB were rather uncomplimentary names for standard-cell products (see pg 78) weren't alone. In fact, the product lines, from Siemens AG, are called SCOA and SCOB.

Also, Table 1 in EDN's recent Technology Update on high-density EPROMs (October 2, pg 91) should have had the following head: "Representative 5V high-density UV-EPROMs." Whatever "μ-EPROMs" may be, EDN will be there to give you pertinent design information when they finally appear.

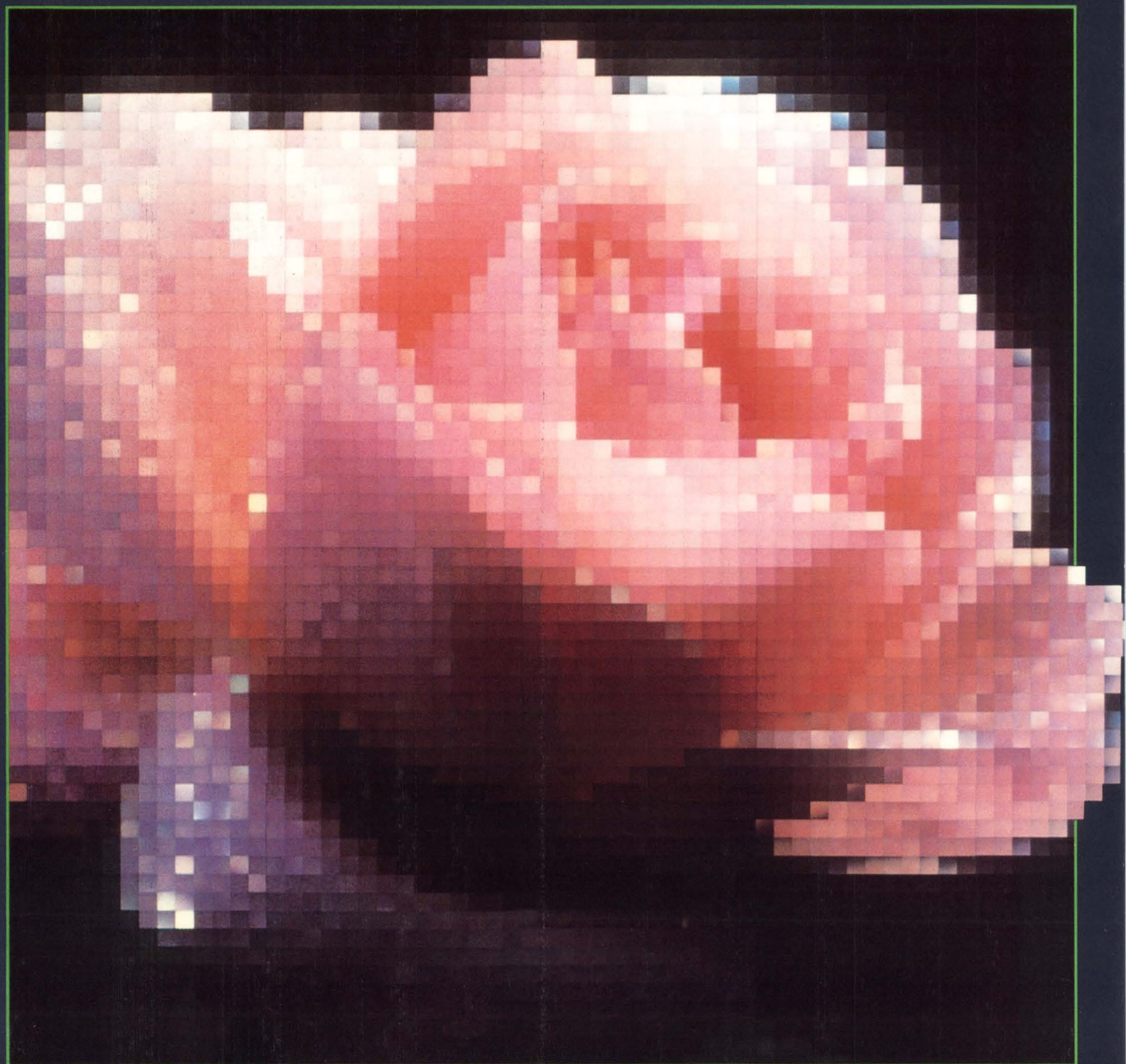
## WRITE IN

Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.

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as everyone knows,  
is analog.**




**Unless,  
of course,  
it's digital.**



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# Seeing it both ways is the beauty of Intersil DSP.

Should they happen upon a perfect rose, most people will wisely stop, sample its beauty, and move on.

But there's a certain breed of engineer who won't let it go at that. They'll find themselves overwhelmed by the desire to "process" the experience.

In an instant, they'll have labeled the rich color and velvet texture as "analog signals."

From there, it's just a matter of time before they've transformed the rose into a repeatable, verifiable stream of digital bits.

They can then commit this information to the perfect memory of a digital computer. From which it can be recalled, and its image replicated, on a high resolution color monitor.

The engineer can now enhance the flower's image. Perhaps try a different color. Or add a few petals. He might even use his new database to create a species of his own. All these fantastic calculations and transformations are one

example of the imaginative world of digital processing, or DSP.

In the last few years DSP has blossomed into one of the most exciting system design tools.

By moving from analog to digital processing of analog signals, engineers can overcome the drifts that plague analog circuitry. They can manipulate empirical data and explore engineering tradeoffs. And they can erect elaborate models using computer simulation.

But to do any of this effectively, the designer needs a DSP supplier who is comfortable in both the analog and digital worlds.

With over 17 years of analog leadership, and 20 years of corporate experience in DSP to draw upon, Intersil is uniquely qualified to work with the DSP engineer.

On the pages that follow, you'll see that Intersil, by taking an integrated approach to the DSP marketplace, has created your best, single source of complete DSP system solutions.

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# Intersil. Everything from A to DSP.



Every signal processing system has three elements: analog to digital conversion, digital processing and digital to analog conversion.

Knowing this, Intersil has taken the only logical approach to DSP: a complete, integrated system from a single supplier.

We intend to become the signal processing engineer's one-stop shop.

You might have expected this solution from Intersil. We've always chosen the systems approach to problems. Consider our work in instrumentation.

Working with instrument engineers, we've developed 17 families of "instruments on a chip." They perform all the functions for an instrument in a single CMOS part.

Given our history, you might also have expected that the DSP marketplace is very important to us.

After all, we've always worked in analog signal conditioning, data acquisition and data conversion. And we've integrated analog and digital functions on the same chip. A case in point is our monolithic 40- $\mu$ SEC 14-bit ICL7115 A/D Converter.

So today, when our traditional analog customers are moving into DSP, it just makes sense for us to help them bridge the gap.

**A new DSP company with  
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Going into DSP, we had a lot more than our own experience to draw on. Our parent company, General Electric, is a world leader in DSP research and development.

The GE Aerospace Group has spent tens of millions of dollars perfecting very high speed, very fine line geometry, digital ICs. And for 20 years, GE divisions have been working in all the classic DSP disciplines. Including radar, sonar and medical imaging.

So when we went into DSP, we didn't go it alone. We were in good company.



# Intersil. The DSP house built on a solid, analog foundation.

## **ICL7115 14-Bit High Speed CMOS Microprocessor-Compatible A/D Converter**

The ICL7115 is the first monolithic 14-bit resolution, fast successive approximation A/D converter. It uses thin film resistors and CMOS circuitry combined with an on-chip EPROM calibration table to achieve 13-bit linearity without laser trimming. Special design techniques used in the DAC and comparator result in high speed operation, while the fully static silicon-gate CMOS circuitry keeps the power dissipation very low.

## **ICL7151 10-Bit A/D Converter with Track and Hold**

The ICL7151 is a 10-bit A/D converter that achieves throughput rates of 60kHz with Two-Step Flash algorithm. A pipelined operation has been achieved with a switched capacitor technique that allows the device to sample new input voltages while a conversion is taking place. The ICL7151 requires a single reference input of +2.5V, which is internally inverted to -2.5V, thereby allowing an input range of -2.5V to +2.5V. The reference input to the device is internally buffered by a high speed CMOS amplifier, which greatly simplifies the external analog drive requirements for the device. A track and hold amplifier has been fully integrated on the front end of the A/D converter. The timing signals for the track and hold amplifier are generated internally, and are also provided externally for synchronization purposes. The ICL7152 is a faster version of the ICL7151; it has a throughput rate of 200kHz.

## **IM29C128 Finite Impulse Response Filter Controller**

The 16-bit FIR Filter Controller (FFC) provides all the data history, storage and programmable filter cycle control logic required to implement FIR filters of up to 128 filter points. When used in conjunction with an external filter coefficient memory, of up to 128 words by 16 bits, and an industry standard 16-bit Multiplier-Accumulator (MAC), the FFC provides the system designer with the ability to implement a powerful FIR filter with only three ICs. The FFC provides all the control signals required to operate the MAC and the coefficient memory as tri-stateable devices, allowing multiplexed usage of these resources.

## **IM29C510 CMOS 16 x 16-Bit Multiplier-Accumulator**

The IM29C510 is a high speed 16 x 16-Bit Parallel Multiplier-Accumulator that operates at a 65ns clock rate (more than 15 MHz Multiply-Accumulate rate). The two input registers accept an x operand and a y operand and yield a full precision product. Built with Intersil's AVLSI 1.3-micron CMOS process, the IM29C510 16 x 16-Bit Multiplier-Accumulator is pin and function compatible with the same speed, at one-sixth or less power dissipation, as bipolar versions.

## **ICL7134 14-Bit Multiplying Microprocessor-Compatible D/A Converter**

The ICL7134 combines a four-quadrant multiplying DAC using thin film resistor and CMOS circuitry with an on-chip EPROM-controlled correction circuit to achieve true 14-bit linearity without laser trimming. Microprocessor bus interfacing is eased by standard memory WRite cycle timing and control signal use. Two input buffer registers are separately loaded with the 8 least significant bits (LS register) and the 6 most significant bits (MS register). Their contents are then transferred to the 14-bit DAC register, which controls the output switches. The DAC register can also be loaded directly from the data inputs, in which case the registers are transparent. The ICL7134 is supplied in two versions. The ICL7134U is programmed for unipolar operation while the ICL7134B is programmed for bipolar applications.

## **ICL7121 16-Bit Multiplying Microprocessor-Compatible D/A Converter**

The ICL7121 achieves 0.0003% linearity without laser trimming by combining a four-quadrant multiplying DAC using thin film resistors with an on-chip EPROM-controlled correction circuit. Silicon-gate CMOS circuitry keeps the power dissipation very low. Microprocessor bus interfacing is eased by standard memory WRite cycle timing

and control signal use. The input buffer register is loaded with the 16-bit input and directly controls the output switches. The register is transparent if WR and CS are held low.

## **EVK-128 Data Conversion and FIR Filtering System**

The Intersil EVK-128 provides a moderate speed data acquisition, conversion and high speed digital filtering system for the IBM PC and most compatibles. Consisting of a board that occupies a single slot in the PC, the card digitally filters data with a filter length of 0 (unfiltered) to 128 taps, utilizing the Intersil IM29C128 Finite Impulse Response Filter Controller (FFC) and 29C510 16-bit multiplier-accumulator (MAC). Throughput is a function of required filter length, with an 80ns per tap processing rate. Included is a floppy disk with an easy-to-use menu-driven FIR filter design program for the PC, including coefficient calculations, time and frequency calculations and plotting capabilities and prompts for controlling the different modes of operation of the board. The package contains complete documentation, including detailed schematics, printed circuit layout, parts list, timing diagrams and applications literature. The user may copy any of this for his own system design, if desired.

### **On-Line Instructions**

Dial 1-800-345-7335 (in CT 203-852-9201). On any ASCII terminal or PC with a 300 or 1200-baud modem (EVEN or IGNORE parity, 7 data bits, 1 stop bit). At "Enter Response Code," type GEIATDSP.

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(2) OPTIONAL: EXTERNAL FREQUENCY SYNCHRONIZATION

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INPUT	OUTPUT SELECTION	SIZE
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	SINGLE (250 W) 5V,12V,15V,24V,28V	6.5×2.5×0.8
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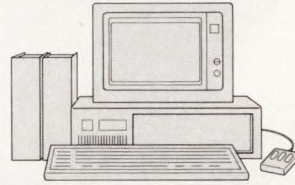
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## CALENDAR

**Modern Electronic Packaging**, Orlando, FL. Technology Seminars, Box 487, Lutherville, MD 21093. (301) 269-4102. February 9 to 11.

**Invitational Computer Conference/Computer Graphics Series**, San Jose, CA. B J Johnson & Associates, 3151 Airway Ave, #C-2, Costa Mesa, CA 92626. (714) 957-0171. February 10.

**Principles of Pulse Doppler Radar: High, Medium, and Low PRF** (short course), Atlanta, GA. Georgia Institute of Technology, Department of Continuing Education, Atlanta, GA 30332. (404) 894-2547. February 10 to 12.

**Invitational Computer Conference**, Raleigh, NC. B J Johnson & Associates, 3151 Airway Ave, #C-2, Costa Mesa, CA 92626. (714) 957-0171. February 19.

**Third Annual Symposium on Reliability**, Santa Clara, CA. Steve Cox, Reliability Inc, 710 Lakeway Dr, Suite 165, Sunnyvale, CA 94086. (408) 732-2394. February 19.

**Invitational Computer Conference/Computer Graphics Series**, Dallas, TX. B J Johnson & Associates, 3151 Airway Ave, #C-2, Costa Mesa, CA 92626. (714) 957-0171. February 24.

**Nepcon West**, Anaheim, CA. CEG, Box 5060, Des Plaines, IL 60017. (312) 299-9311. February 24 to 26.

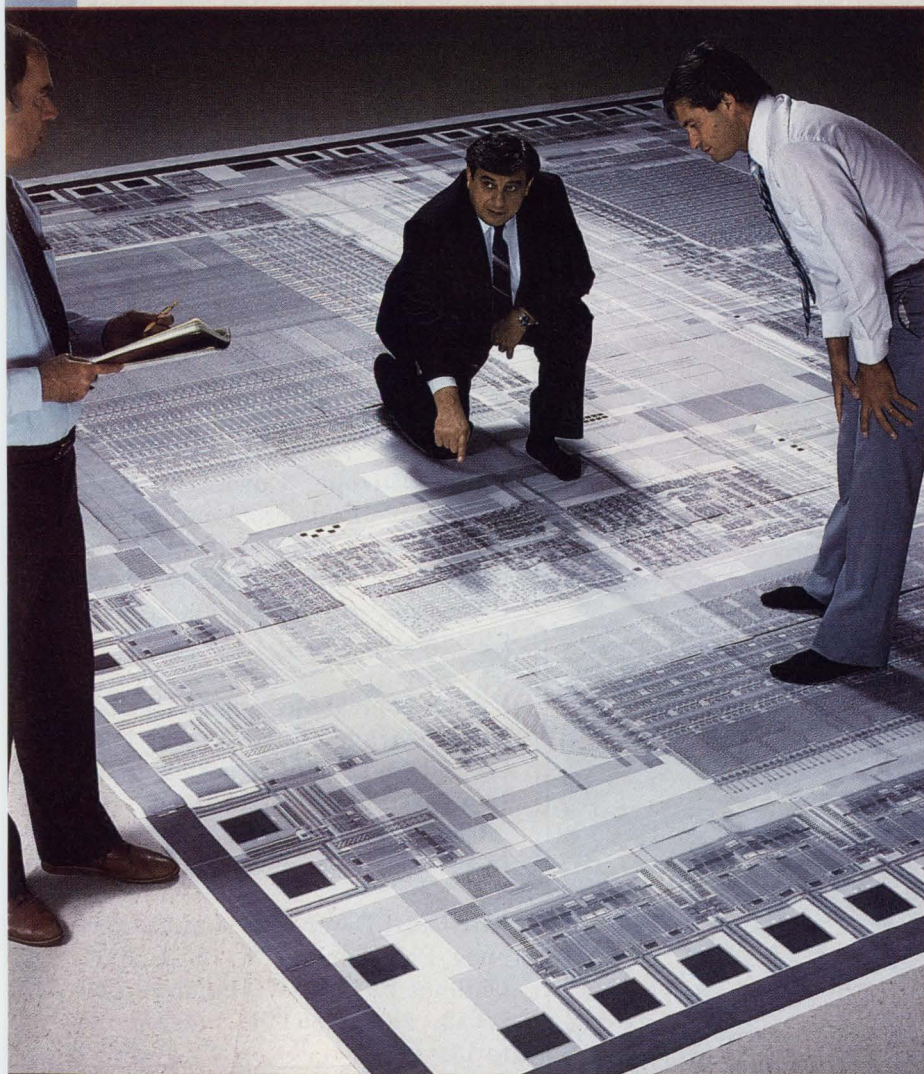
**ISSCC** (International Solid-State Circuits Conference), New York, NY. Lewis Winner, 301 Almeria Ave, Coral Gables, FL 33134. (305) 446-8193. February 25 to 27.

**West Lightwave Expo**, San Jose, CA. Lightwave, 235 Bear Hill Rd, Waltham, MA 02154. (617) 890-2700. February 25 to 27.

**Spring National Design Engineering Show and Conference**, Chica-

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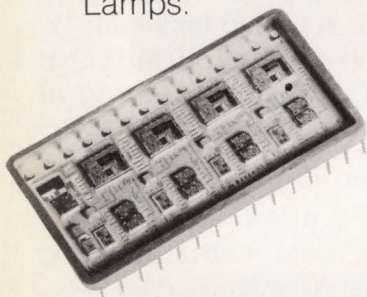
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go, IL. CEG, 999 Summer St, Stamford, CT 06905. (203) 964-0000. March 2 to 5.

**IEEE Applied Power Electronics Conference and Expo**, San Diego, CA. Melissa Widerkehr, APEC '87, 655 15th St NW, Suite 300, Washington, DC 20005. (202) 347-5900. March 2 to 6.

**Invitational Computer Conference**, Austin, TX. B J Johnson & Associates, 3151 Airway Ave, #C-2, Costa Mesa, CA 92626. (714) 957-0171. March 3.

**Comdex in Japan**, Tokyo, Japan. Interface Group, 300 First Ave, Needham, MA 02194. (617) 449-6600. March 3 to 5.

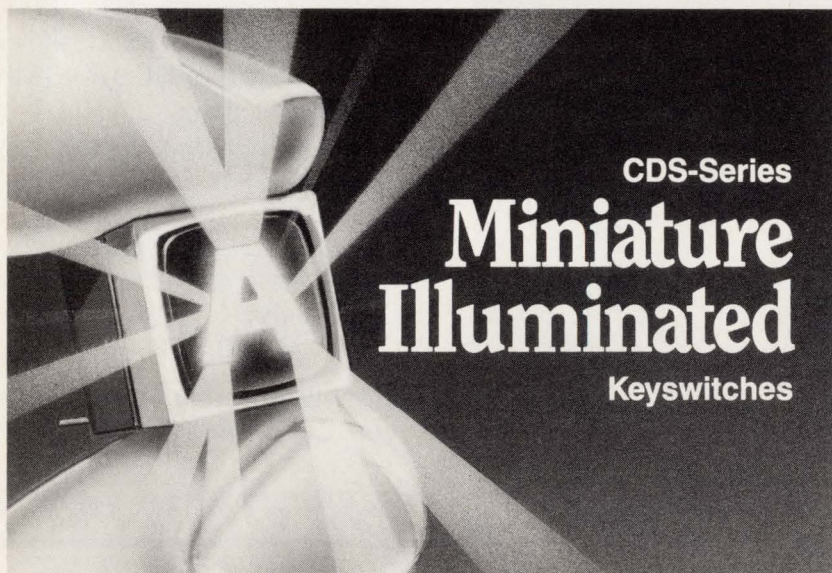
**Dexpo Europe** (European DEC-Compatible Exhibition and Conference), London, UK. Expoconsul International, 3 Independence Way, Princeton, NJ 08540. (609) 987-9400. March 3 to 5.

**Fourth Topical Meeting on Optical Data Storage**, Lake Tahoe, NV. Optical Society of America, 1816 Jefferson Pl NW, Washington, DC 20036. (202) 223-0920. March 11 to 13.

**Northeast Bioengineering Conference**, Philadelphia, PA. IEEE, 6411 Chillum Pl NW, Washington, DC 20012. (202) 785-0017. March 12 to 13.

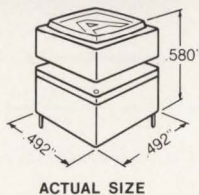
**Modern Electronic Packaging**, Torrance, CA. Technology Seminars, Box 487, Lutherville, MD 21093. (301) 269-4102. March 16 to 18.

**International Military Fiber Optic and Communications Exposition**, Washington, DC. Information Gatekeepers, 214 Harvard Ave, Boston, MA 02134. (617) 232-3111. March 16 to 19.



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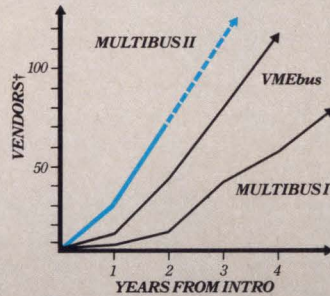
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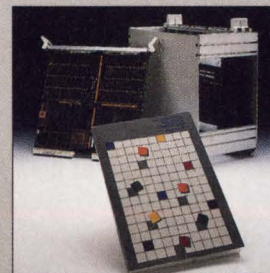
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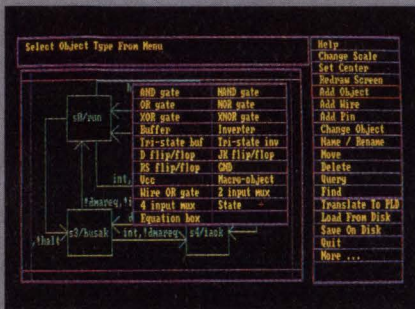
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# EDITORIAL

## Cancel US-Japan Semiconductor pact



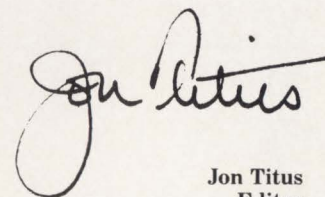
It's hard to believe, but economic suicide is the official policy of the US government and our native semiconductor industry. It's embodied in the US-Japan Semiconductor Trade Agreement. The government, as well as US chip manufacturers, want you to pay extra for Japanese ICs, and they want you to help Japanese semiconductor manufacturers make a profit.

Here's how this scheme works. Before the agreement, a Japanese company bent on selling chips in the US could sell an IC at less than cost. As a consequence, OEMs got bargains by paying less than the usual price for chips. Each purchase also caused a net loss for Japanese manufacturers. Because US chip manufacturers couldn't compete with the imported chips' low prices, the Japanese dominated the market even as they lost money. To protect domestic markets from what they call unfair foreign competition, US manufacturers asked for protection from the cheap chips that the Japanese were selling in the US. As a result, the US and the Japanese governments negotiated an agreement that sets an artificially high price for such chips.

In effect, the trade agreement sets up a semiconductor cartel; no manufacturer charges less than a minimum price for certain chips. OEMs who were happily paying \$0.75 for a chip must now pay a minimum price of, say, \$2.75. Instead of protecting the US semiconductor industry, the agreement angers OEMs and their customers, and it hoists the US semiconductor industry with its own petard. Because the agreement sets high prices for chips—beyond what the market would pay—Japanese suppliers go from losing money to reaping windfall profits from US buyers. Some of those profits fund research into new Japanese semiconductors for sale in the US.

The agreement doesn't address the glut of Japanese chips, nor does it cover sales outside Japan and the US. So, in that part of the rest of world where free market conditions exist, you can still buy cheap chips. It won't be long before US manufacturers shift production offshore to avoid the fixed high prices of imported Japanese chips.

It may be necessary to protect an industry for a short time, but such protection shouldn't fatten foreign competitors, and it shouldn't spur a drive to manufacture products outside the US. It's time to dump the US-Japan Semiconductor Trade Agreement and get back to head-to-head competition in the semiconductor industry. Some businesses will fail while others merge or take on foreign partners. Such is life in the competitive free market.

  
Jon Titus  
Editor

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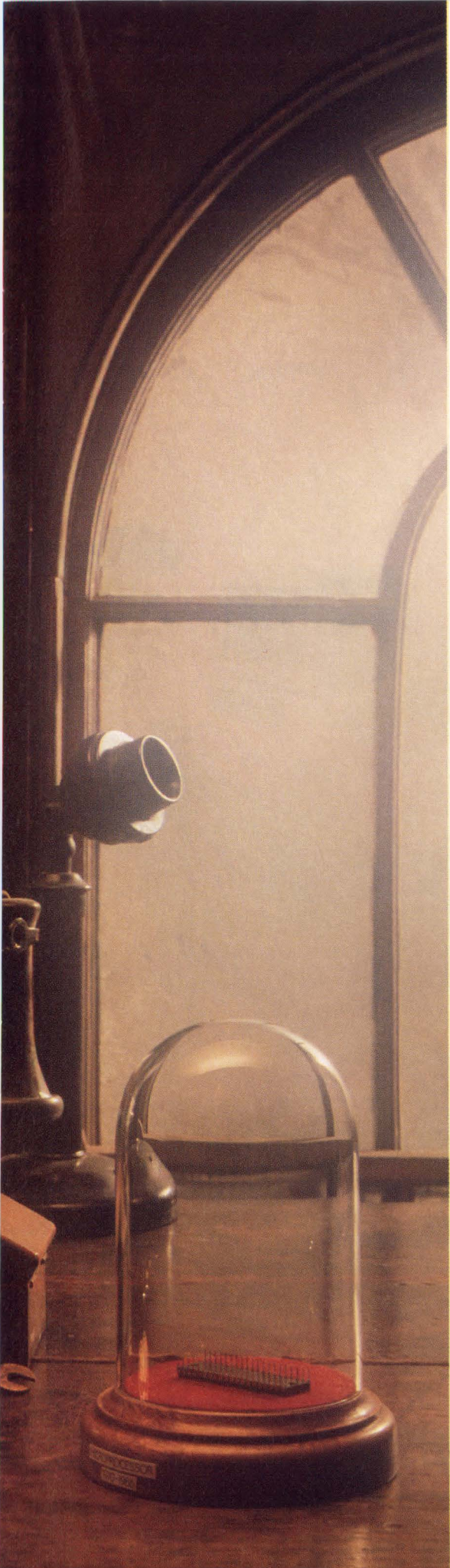
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IMS M212	16 bit DiscProcessor—1Kbyte—2 links
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IMS D701-2	IBM PC—Transputer Development System.
IMS D600	VAX/VMS—Transputer Development System.
EVALUATION BOARDS	
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IMS B003-1	Double Eurocard + 4 x IMS T414 + 4 x 256Kbyte DRAM.
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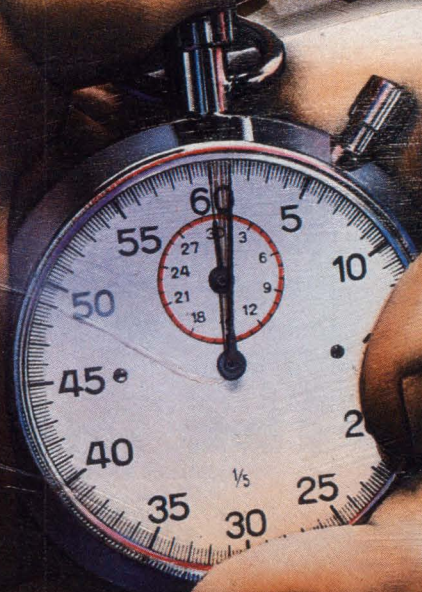
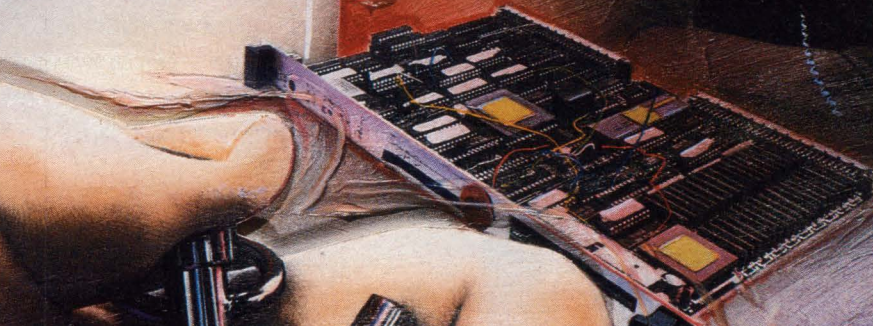
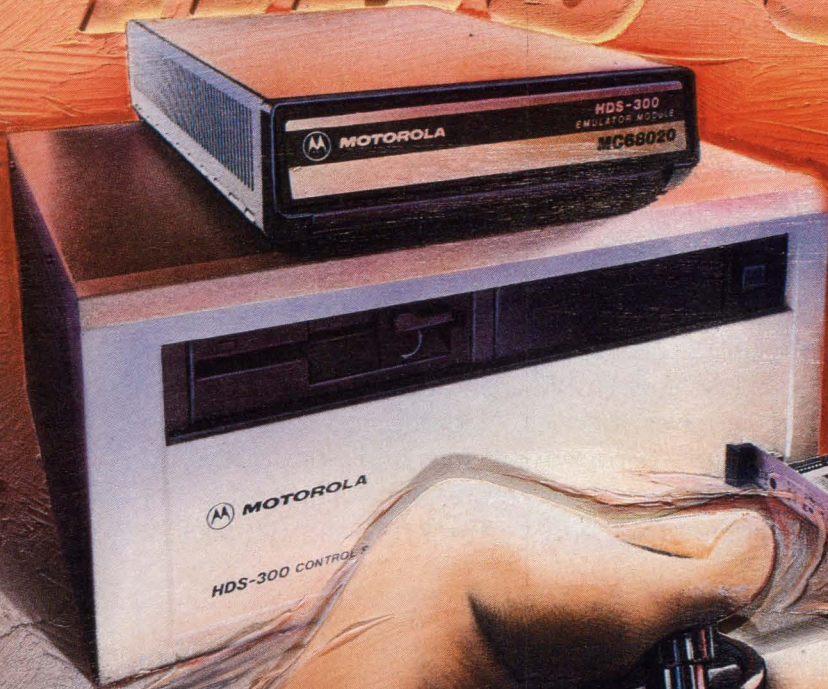
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CIRCLE NO 91



**MOTOROLA**

# HDS-300



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The HDS-300 development station is your ultimate emulation and analysis tool for system designs based upon Motorola's 8-, 16- and 32-bit families. It supports development of systems based on the MC68020, MC68010, MC68000, and MC68008 as well as the MC6801/03, MC6809, MC68HC05C4/C8 and MC68HC11 microprocessors.

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An array of labor-saving features includes real-time emulation to 25 MHz, coprocessor support, system performance analysis, and the unique ability to perform "C" language source-level debugging.

Powerful analysis/debugging capabilities, precise duplication of the application system configuration, and accurate, real-time, zero wait-state emulation generate great system-development versatility.

## Source-level approach enables high-level language debug.

HDS-300 source-level debug capability allows debugging of user code at the "C" statement level rather than the machine or assembly language level. And, debugging is enhanced with break-

points and other references made using labels, variable names, or statement numbers of the source code. Debugging is faster, since the familiar name of the variable can be used and the value of the variable is presented in the same type as the variable is declared. The emulator in mixed mode can also break "C" statements down to assembly language for even closer code inspection and debug.

## Host options are available.

The complete HDS-300 system includes a host, system hardware-development station and an emulator for the specific M68000 family processor in your target system. Available options include:

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emulator and provide a common user debug interface. This same friendly interface is provided across the complete family of emulators. The time you save here, alone, can substantially reduce time-to-market for your new design.

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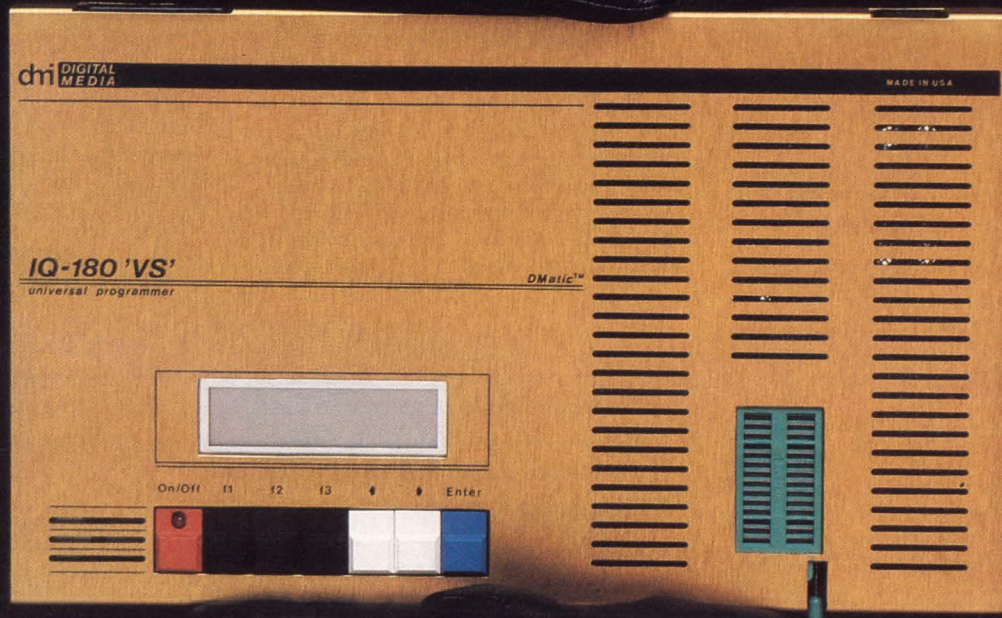
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CIRCLE NO 113

## Availability of cryptographic ICs augurs the increasing use of data encryption

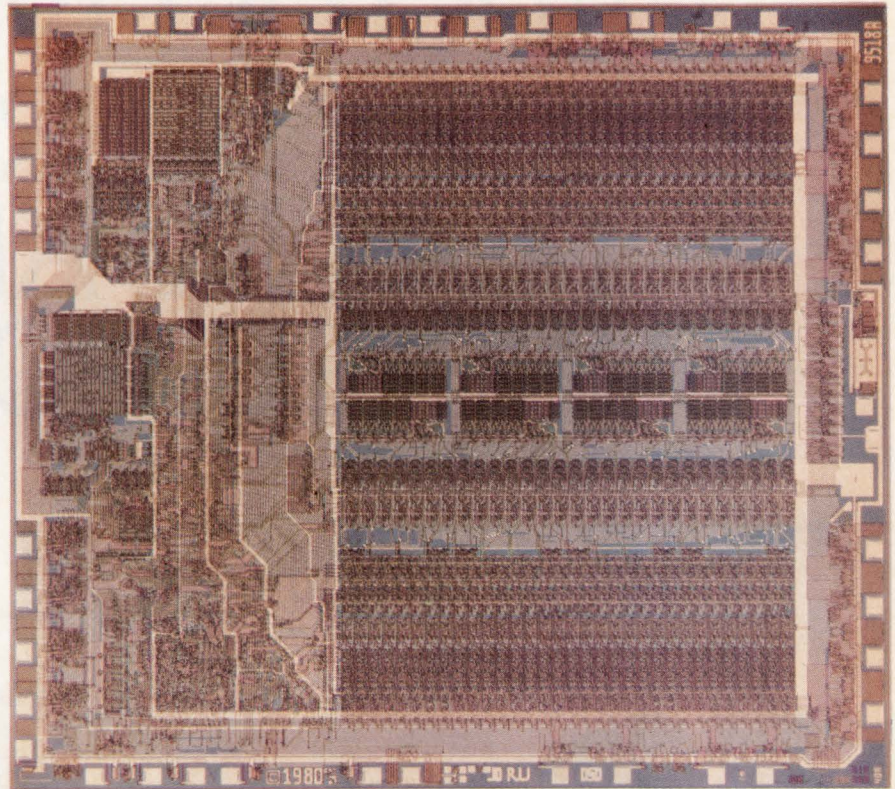
Chris Terry, *Associate Editor*

As the need for data encryption becomes increasingly evident because of the increase in traffic over satellite and microwave links, cryptographic schemes must be commercially available and economically feasible. Perhaps surprisingly, the government may provide the impetus for the increase in the use of cryptographic protection.

If you're designing a computer or telecommunications system that will handle sensitive data, your customer may require that you incorporate a cryptographic means of protecting the data against unauthorized access. Although you may be accustomed to thinking of cryptography as only necessary for government agencies with very large computer systems, cryptographic schemes for workstations and microcomputers are necessary, too.

Consider, for example, how commonplace distributed processing has become in the banking industry (especially where automatic tellers are in use). Also, the number of LANs is increasing. A growing number of local-area networks in small and medium-sized businesses handle data that certainly needs to be kept private; for instance, payroll documentation, personnel records, and new product designs require safeguards (not to mention the financial transactions that could give a clue to a company's stability or future plans).

Such data is, to some extent, protected against unauthorized access by the multilevel security precautions built into most large operating systems. These precautions are not always adequate, though. As long as the data stays within the system,



**This data-encryption processor, the AMD 9578/Z8068, is a variation of the 9568 chip and is designed for interfacing to AMD's 2900 bit-slice CPUs and to Zilog's Z80000  $\mu$ Ps.**

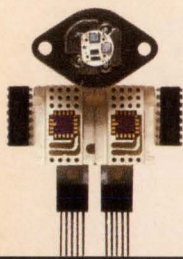
and as long as the passwords that allow the reading, creation, and modification of files are frequently changed and are properly managed, the data is safe against casual snoopers.

However, these same passwords must reside somewhere in the system, and a technically sophisticated snooper may be able to find and use them to read sensitive files that are stored in standard formats or to modify or erase these files. Thus, for complete security, the files themselves need to be stored in a form that is unreadable to a snooper, even if he has the passwords that allow access.

Finally, telephone lines constitute the medium for transferring data

from one node of a network to another or from one site to another—no matter what type of data it happens to be. Because phone lines are vulnerable to wiretapping and other interception techniques, sensitive data passing over them should first be scrambled in such a way that only the intended recipient can unscramble it.

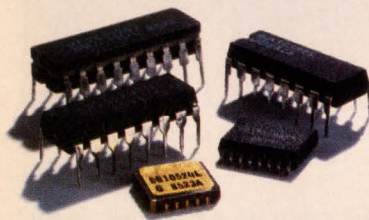
The process of turning clear (plain-language) text into cipher (scrambled) text is called encryption; decryption is the opposite process of unscrambling cipher text into clear text. Cryptology is the general term that embraces both cryptography (the designing of encryption/decryption schemes) and cryptanalysis (the process of break-



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# TECHNOLOGY UPDATE

A B C D E F G H I J K L M N O P Q R S T U V W X Y Z  
 X Y Z A B C D E F G H I J K L M N O P Q R S T U V W

CLEAR TEXT: MEET ME AT MIDNIGHT  
 CIPHER TEXT: JBBO JB XQ JFAKEDEQ

**Fig 1—The Caesar cipher is a single-alphabet substitution method.** The cipher alphabet is displaced from the clear alphabet and wraps around to the beginning, as shown here.

KEY: H E C T O R  
 ORDER: 3 2 1 6 4 5

CLEAR TEXT: M E E T M E  
 A T M I D N  
 I G H T J J

CIPHER TEXT:  
 E M H E T G M A I M D J E N J

**Fig 2—The Playfair cipher is a columnar transposition method.** The clear text appears in horizontal rows the same length as the key, with padding (JJ) to fill the rectangle. The cipher text is taken from the vertical columns in the numeric order determined by the order of occurrence of the key letters within the normal alphabet.

ing a cryptographic scheme so that you can recover messages not intended for your eyes).

Encryption (and by inference, decryption) uses either or both of two basic methods: substitution, in which each character of the clear text is represented by a different character or symbol (which may not appear at all in the clear text); and transposition, in which the cipher text contains exactly the same characters as the clear text, but in a different order—that is, the encrypted text is an anagram of the clear text.

The simplest examples of each of these methods are the Caesar cipher (Fig 1,) which Julius Caesar devised; and the Playfair cipher (Fig 2), which protected low-level communications during World War I. All of the cryptographic schemes available today rely on some sophisticated combination of substitution and transposition.

A person can quickly break a simple substitution scheme by comparing the characters contained in the cipher text with a frequency table, which shows the letters, digraphs, and trigraphs that appear most often in a particular language. Given time and skill, a person can manually break transposition ciphers; with the aid of a computer, such codes are easily decipherable. Thus, much more sophisticated cryptographic schemes are required in order to prevent computer-aided cryptanalysis.

Probably the most widely known scheme in use today, and one that is available in the form of an integrated circuit, is the Data Encryption Standard (DES). IBM developed the DES between 1973 and 1977,

and the National Standards Laboratory approved it for commercial and sensitive data in 1977.

At least two IC manufacturers are currently delivering production quantities of encryption devices that use the DES algorithms. The AT&T T7000 digital encryption processor and the AMD 9568 data ciphering processor are 40-pin DIP ICs that you can include in a microcomputer without much difficulty. In addition, the AMD chip is specifically designed to interface to the IBM PC bus. The AMD IC costs \$29.17 (100); the AT&T chip sells for \$43 (1000).

The DES specifies that both the

encryptor and the decryptor of a message must use the same key; the question that then arises is how to distribute this key securely. Actually, you need two keys: a master key that you change relatively infrequently (daily or weekly perhaps); and a session key, which you can change as often as you wish for

## Companies participating in Project Overtake

For more information on any of the cryptographic products associated with the National Security Agency's Project Overtake, contact the individual acting as liaison listed after each manufacturer.

**AT&T Technologies**  
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**Harris Corp**  
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 Jack Raymond  
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**Honeywell Inc**  
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 Jack O McCorkle  
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**Hughes Aircraft Co**  
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 Fullerton, CA 92634  
 Chuck McLoon (Bldg 688/L106)  
 (213) 802-4338

**IBM Corp**  
 Federal Systems Div  
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 A Louis Medin  
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# TECHNOLOGY UPDATE

outgoing messages and which can be different for every incoming message.

When you want to send a message to a remote station equipped with DES devices, you first encrypt the session key, using the master key, and send the session key over the line ahead of the message. The remote equipment decrypts the session key and stores the clear key in a register.

Every key consists of eight bytes, each having seven data bits and a parity bit (the LSB); the hardware does not check the parity of encrypted session-key bytes but does check the parity of the decrypted session-key bytes. The parity circuits activate a status line that tells you whether or not the session key

was correctly transmitted and loaded. The AT&T and AMD ICs have two session-key registers, and thus you can load your own session key in one register for encrypting outgoing messages and use the other register to hold the session key received with an incoming message.

There is some controversy as to whether or not this method of distributing keys is secure. On the one hand, sending the session key over a telephone line (even in encrypted form) is hazardous.

On the other hand, you can change the session key as often as you wish, and the receiver of a message doesn't need to know the contents of the key he'll use for decrypting the message because the

equipment will decrypt and load this key for use automatically. These precautions limit the number of people who know the key and that in turn increases security. However, it's difficult for two strangers who are unable to meet to set up a secure DES communications link because there's no secure way for them to agree on a key.

## Three modes are possible

The DES specifies three operating modes: electronic code book (ECB); cipher-block chaining (CBC); and cipher feedback (CFB); both AT&T's T7000 and AMD's 9568 chips provide all three modes. In the ECB mode, for any given key, encrypting the same 64-bit block of clear text multiple times will always

## Public-key/private-key scheme hasn't been broken

An alternative cryptographic scheme, and one that offers the advantage of providing unquestionable authentication of the originator, is the public-key/private-key scheme of Diffie and Hellman (Ref 1), proposed in 1976. In 1978, Rivest, Shamir, and Adelman, professors at MIT, published the RSA implementation of the public-key/private-key scheme (Ref 2). To date, the RSA algorithm has not yet been broken.

The public-key/private-key scheme uses a key computed from two very large prime numbers (greater than  $10^{100}$ ). Two of the key's factors constitute the public and private portions, respectively. The public portion resides in a public directory; each private portion remains known only to the individual who uses it.

If user X wishes to send a message to user Y, he first encrypts the text using his private key; he then looks up the public key and uses this to encrypt the signature portion of the message. User Y, upon receiving the encrypted message, uses his private key to decrypt the signature portion; then he looks up the public key of the sender and uses that to decrypt the text.

The security of this system derives from the certainty that factoring a very large number is a huge task requiring immense amounts of time—one estimation is about 4 billion years of Cray super-computer time to factor a 200-digit number.

Another advantage is that any two persons listed

in the directory can establish secure communications without having to arrange for secure distribution of a key (as would be the case if they used the DES). They could, in fact, use an electronic mail system (such as MCI mail).

Of course, the use of such large numbers has drawbacks as well as advantages. Because the algorithm is based on the multiple-precision processing of large numbers, it would be very expensive (and perhaps impossible, at present) to implement in hardware, and the software implementation is much slower than the inexpensive hardware implementations of the DES.

A successful implementation of the RSA algorithm has been done on an IBM PC; because the implementation is slow, however, you have to collect the entire outgoing cipher text in a disk file or memory buffer before passing it to a 1200-bps modem and, by the same token, you have to buffer incoming cipher text before decrypting it.

## References

1. Diffie, W and E Hellman, "New Directions in Cryptography," *IEEE Transaction on Information Theory IT-22*, November, 1976, pg 644.
2. Rivest R L, A Shamir, and L Adelman, "A Method for Obtaining Digital Signatures and Public Key Crypto System," *Communications of the ACM*, February, 1978, pgs 120-126.

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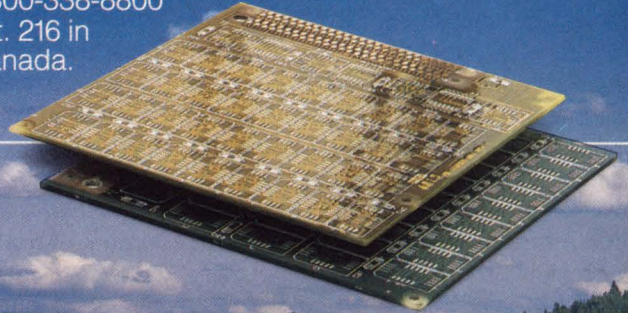
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# TECHNOLOGY UPDATE

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**Harris Custom  
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result in the same 64-bit block of cipher-text output. Although this mode violates a basic rule of cryptography—never encrypt the same message in the same way twice because doing so makes code-breaking easier—it does offer an advantage for intrasystem use in disk file encryption: You can read a file back one sector at a time.

In the CBC mode, the cipher output of each block modifies the encryption of succeeding blocks, so that successive encryptions of the same clear text block will produce different cipher text each time. This mode is inconvenient for encrypting a disk file because you have to read the whole file in order to examine one sector. However, two attributes make it ideal for synchronous-block data transmissions over phone lines: Security is intrinsically high, and any attempt by a snooper to intercept and modify the message during transmission corrupts the entire message and makes it indecipherable, thereby alerting the recipient to the interception attempt.

The CFB mode is similar to the CBC in that each block affects the encryption of subsequent blocks. However, the CFB mode is optimized for 8-bit data blocks instead of the CBC's (and ECB's) 64-bit blocks and thus is highly suitable for character-by-character asynchronous data links.

Although the DES provides a reasonably secure means, capable of implementation in fast hardware, of encrypting data and transmitting it over telephone and network lines at speeds as high as 1.5M bytes/sec, master key distribution is still a

problem. If there are  $n$  users on a network, each of whom desires secure communications with the other  $n-1$  users, then the network administrator has to arrange for the secure distribution of  $n(n-1)/2$  master keys each time a key change is necessary. An alternative scheme that solves this problem does exist but is not available in IC form (see **box**, "Public-key/private-key scheme hasn't been broken").

Also, not everyone believes that the DES's security is sufficient. Recently the National Security Agency (NSA) stated that it won't approve the DES when it becomes due for review as a federal standard in 1988. The reason, according to the agency, is that potential enemies have had 10 years in which to study and analyze intercepted communications that use the DES, and therefore they can longer guarantee the security of the standard.

The NSA's National Security Decision Directive (NSDD) 145, which President Reagan signed in 1984, provided the agency with the authority to develop new encryption standards for unclassified government data and to promote the adoption of the new standards by the private sector.

In March 1985, the NSA established the DCECP (Development Center for Embedded Comsec Products) with a charter to design embeddable Comsec modules that will help to secure communications. In conjunction with the 10 participating companies, the center has embarked on Project Overtake, a cooperative effort to standardize Comsec modules both for Type I data (classi-

fied) and Type II data (sensitive but unclassified government or government-derived). Off-the-shelf devices associated with Project Overtake include such products as a series of voice- and low-speed-data encryption devices, a series of data-encryption devices for computers, and a series of high-speed digital-data-encryption devices for mainframe, satellite, and microwave communication links.

OEMs intent on purchasing Comsec encryption modules have to qualify with the NSA on a need-to-know basis. You can obtain information and guidance on the most suitable modules for a given application and on qualification requirements from the liaison personnel at each participating company (see **box**, "Companies participating in Project Overtake").

## Tradeoffs exist, as always

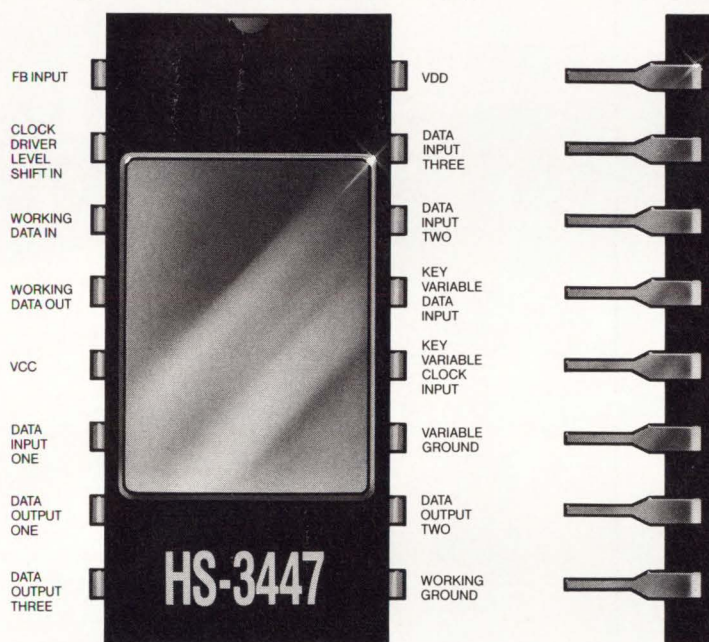
No matter what the future holds, when deciding on cryptographic alternatives for your particular application you'll have to consider the inevitable tradeoffs. If you're dealing with sensitive data at governmental levels, you'll have to use NSA-approved devices such as the Harris HS3447 Cipher-I IC for serial communications (\$137 in quantities of 500) or one of the Comsec modules, regardless of cost. If you need the security of large keys and can tolerate relatively slow operation, a public-key/private-key implementation might suffice. If you need to bring a product to market quickly and inexpensively, though, then incorporating one of the DES cryptographic processors into your system is probably the best approach. **EDN**

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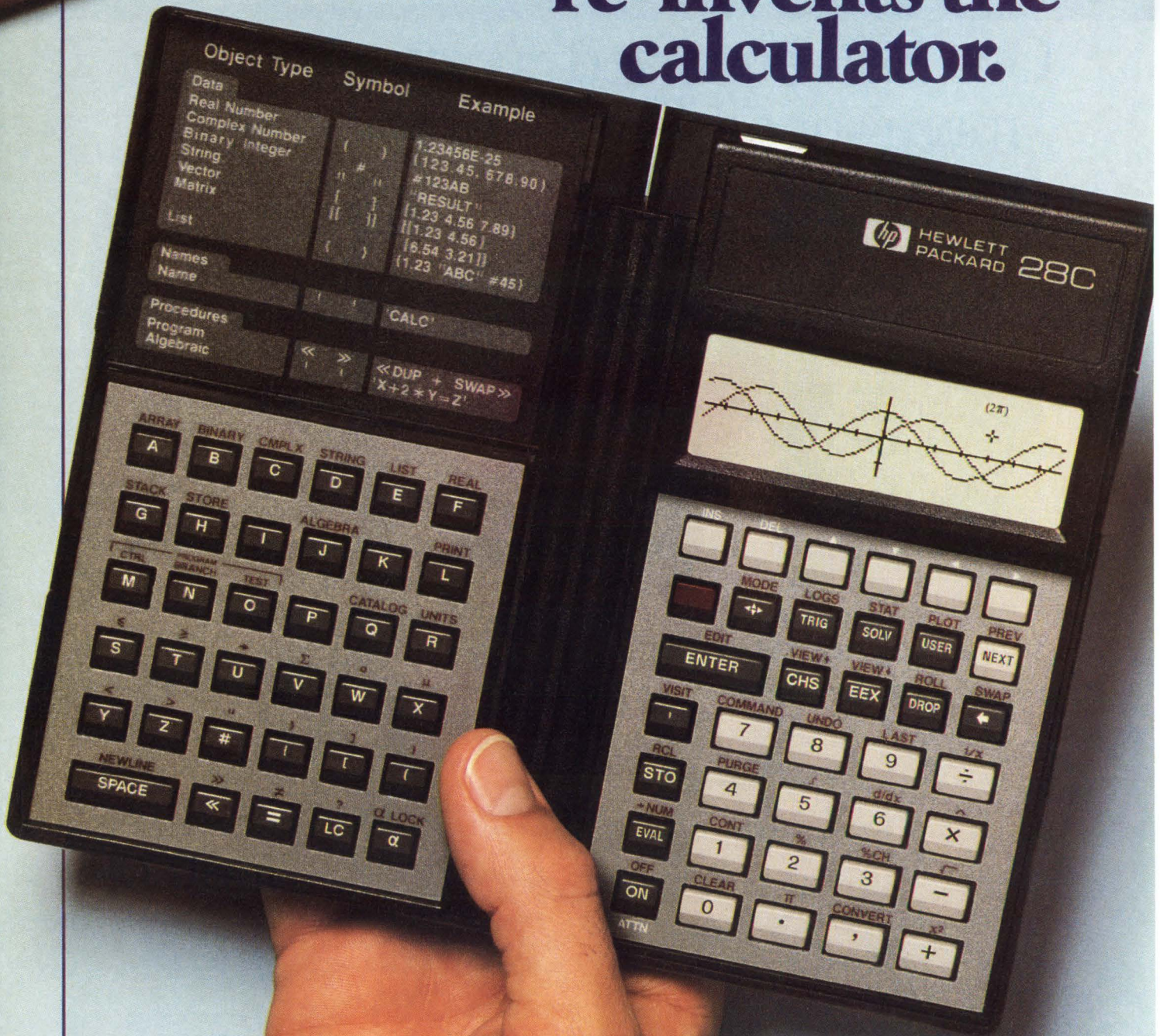
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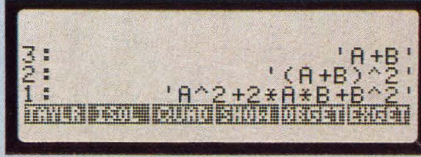
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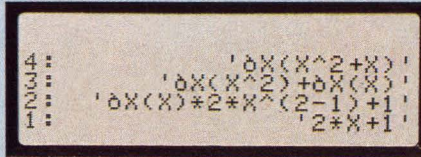
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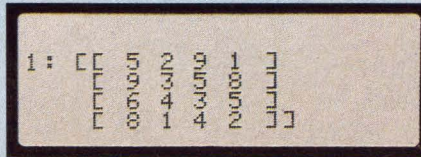
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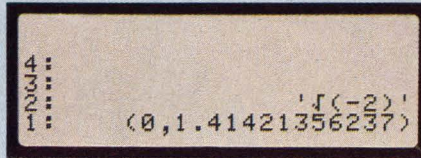
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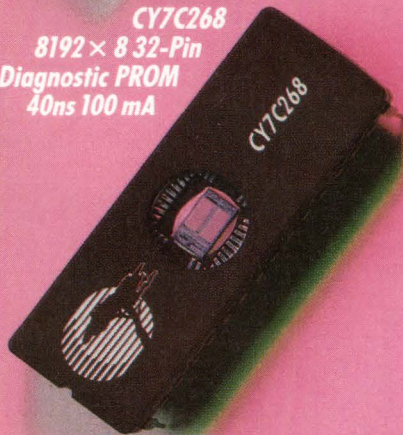
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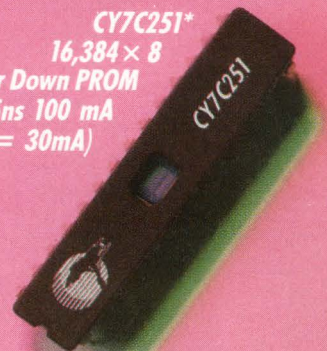
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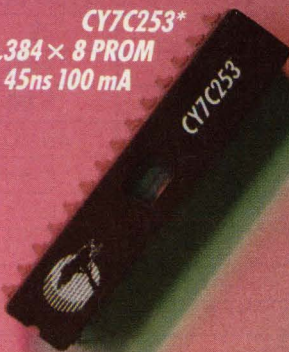
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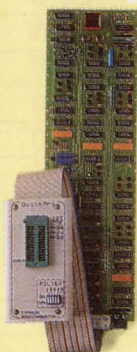
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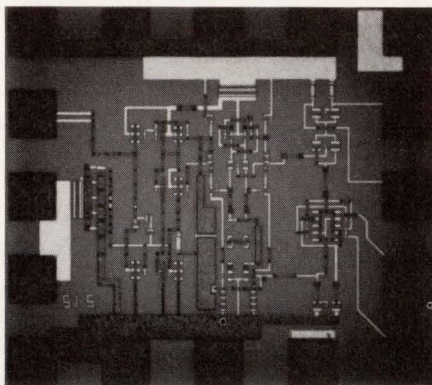
## Specially processed operational amplifiers meet rad-hard and high-temperature needs

Jim Wiegand, *Associate Editor*

Military and aerospace applications have placed severe environmental demands upon analog components for some time, but don't overlook the possibility of using the parts specially processed to meet those demands for your own, more terrestrial, and in some cases even subterranean, applications. The requirements of radiation hardening and high-temperature operation found in these environments are echoed in nuclear power stations and fuel-reprocessing plants, in high-temperature industrial control, in measurements of jet-engine parameters, and in down-hole measurements for oil exploration. Among the parts specially processed for such harsh treatment are a small number of operational amplifiers—some mature and some recently introduced.

Some of these op amps are better suited to high-radiation environments, and some are specifically for high-temperature settings. Some op amps blur the distinction, taking advantage of fabrication processes that address the problems associated with both high temperatures and high doses of radiation.

Different types of radiation, through their own mechanisms, adversely affect ICs in a variety of ways (see **box**, "A hardened IC is good to find"). In particular, exposure to radiation can degrade such op-amp parameters as open-loop gain, input bias current, input offset current, input offset voltage, slew rate, bandwidth, input impedance, and output power. IC manufacturers have devised ways of ameliorating the effects of radiation, and they can provide you with rad-hardened op amps for use in such environ-



*An impressive unity-gain stability spec of 150 MHz is the noteworthy feature of the AOP1510 op amp from Anadigics Corp. The op amp is fabricated with an inherently rad-hard GaAs process.*

ments as nuclear power plants and unshielded industrial x-ray equipment.

### Rad-hardened op amps

Anadigics Corp employs gallium arsenide in the manufacture of its AOP1510 op amp. GaAs is inherently rad-hard because of its semi-insulating substrate. Anadigics cooperates with customers in radiation testing of its devices, which occurs at third-party facilities (companies or national laboratories), but the company does not have radiation hardness data available.

In addition to exhibiting the rad-hard advantages of GaAs devices, the AOP1510, as you might imagine, sports some impressive speed specifications. The device operates with unity-gain stability to 150 MHz. The open-loop gain is 70 dB, and the slew rate is 500V/ $\mu$ sec. The settling time to within 1% is 30 nsec typ (when the sense resistance and the feedback resistance are both 1 k $\Omega$ ). The AOP1510 costs \$29 (this and all other prices cited in the article are for quantities of 100).

Burr-Brown Corp employs its

proprietary DIFET dielectric-isolation (DI) process in the manufacture of its op amps. The DI process counteracts the tendency of CMOS ICs to form leakage paths when subjected to radiation. Although the DI process typically doubles the number of steps involved in the production of ICs, and although this two-fold increase in manufacturing steps results in nearly an order of magnitude increase in wafer costs, the process pays off in radiation hardness. The OPA111 op amp has been tested by the Jet Propulsion Laboratory and found to be rad-hard at the  $1 \times 10^7$ -rad(Si) level, using cobalt-60 (Co60) and 2.5-MeV electrons as sources for irradiation. The parts also operate to the limit of their functionality, but with minor degradation, after being exposed to a fluence of  $5 \times 10^{13}$ N/cm<sup>2</sup> of 1-MeV equivalent neutrons.

(Just to lend a little perspective to these figures, the Galileo spacecraft, which will be exposed to a constant stream of radiation during its long journey to Jupiter, and to even higher levels as it comes in close to the giant planet, will be subjected to something less than  $3 \times 10^5$  rads.)

The OPA111 operates with an input bias current of 1 pA, 1  $\mu$ V/ $^{\circ}$ C of offset-voltage drift, 1  $\mu$ V rms of noise between 10 Hz and 10 kHz, an open-loop gain of 120 dB, and common-mode rejection of 100 dB min. The part costs \$9.75.

### Duals and quads

Also manufactured with the DIFET process, the \$15.25 OPA156A provides a 4-MHz min gain-bandwidth product, a 10V/ $\mu$ sec slew rate, and a settling time to within 0.01% of 4  $\mu$ sec typ. Burr-

# TECHNOLOGY UPDATE

Brown also offers the \$15.65 dual OPA2111 and the \$11.85 quad OPA404 op amps with DIFET processing.

For applications requiring high slew rates, you can use Elantec's 2500 or 2600 Series of DI-processed op amps. The \$24.64 EHA2-2520-8 op amp, for example, specs a slew rate of 100V/ $\mu$ sec. Like Burr-Brown and Analogics, Elantec doesn't have

in-house radiation test facilities. The company works with you to obtain the required testing at an off-site test facility, such as the JPL or Sandia National Laboratories.

## Programmable, wideband parts

The Custom Integrated Circuits Division of Harris Corp has provided rad-hardened ICs using the DI process for a number of

years. It currently offers the HS3516RH wideband op amp, the HS3530RH low-power programmable op amp, and the HS5104RH quad op amp. Each of the op amps delivers 10 mA of drive current, and all feature a 1V/ $\mu$ sec slew rate and a 15-kHz full-power bandwidth.

The \$220 HS3516RH provides unity-gain stability at frequencies greater than 10 MHz. It specs a

## A hardened IC is good to find

The two major types of damage to which an IC can fall victim are displacement damage and ionization damage. Displacement damage is caused by neutrons or heavy, charged particles, which interact with the lattice of the irradiated semiconductor material. As its name implies, displacement damage is marked by vacancies in the lattice structure or by interstitial atoms—that is, extra atoms forced between lattice sites. This type of damage is particularly harmful to bipolar ICs, because these defects decrease minority-carrier lifetime and carrier concentration, which in turn leads to beta degradation and increased reverse leakage currents across device junctions. In an op amp, the open-loop gain, input bias current, input offset current, input offset voltage, and slew rate are all adversely affected.

Gamma (photon) radiation is the primary source of ionizing radiation. Ionizing radiation produces its most noticeable effects in the gate and field oxides of CMOS ICs. The net effect is a threshold voltage shift and degradation in channel mobility. Photocurrents generated by ionizing radiation can also activate a low-impedance, high-current path from  $V_{DD}$  to ground in CMOS devices. This condition is known as latch-up, and it can destroy the device. Manufacturers now grow an additional epitaxial layer over the starting material of the bulk-CMOS wafer to eliminate latch-up.

## An untoward transformation

There's another problem caused by ionizing radiation. Immediately after ionization, recombination begins, but due to the applied electric fields, so does electron transport. Because electron mobility is roughly six orders of magnitude greater than hole mobility, the electrons will be swept out much sooner than the holes, leaving the holes behind to begin a transport process to the interface between

the silicon and silicon-dioxide layers. Some holes will pass into the silicon, while others will be trapped at defect centers near the interface. This buildup of positive charge will make it easier to create the n-channel (inversion layer), thus lowering the threshold voltage in an n-channel device; in the extreme, the n-channel device may even be transformed into a depletion-mode device.

On the other hand, a p-channel device becomes more difficult to turn on. The two main effects of ionizing radiation, then, are an increase in leakage current and a shift in threshold voltages, both of which are related to the radiation-induced inversion layer. Designers can counteract the increase in leakage current by forming guard bands around each n-channel device. They can also harden the gate and field oxides to lessen the shifts in threshold levels. Other semiconductor technologies—notably gallium arsenide and silicon on sapphire (SOS)—are inherently more resistant to the effects of radiation, and some parts using these technologies are beginning to work their way out of the lab.

## Measuring and testing rad-hardness

In order to evaluate the radiation hardness of a part, you need to know how to measure the radiation dosage and how to test the part in question for hardness. The energy transferred to a material by ionizing radiation is measured in terms of rads. One rad is equal to 100 ergs absorbed per gram of material. The total absorbed dose is called the gamma, and the dose rate, called the gamma-dot, is measured in rads(Si)/sec. Particles are referred to in terms of flux, the concentration of particulate flow is measured in particles/cm<sup>2</sup>/sec, and fluence is the time integral of flux in particles/cm<sup>2</sup>.

You can perform radiation testing with widely varying dose rates. According to MIL-STD-883C, method 1019, dose rates may vary between 1.67

# TECHNOLOGY UPDATE

slew rate of 22V/ $\mu$ sec and a settling time of 450 nsec to within 5% of the settled value. The \$155 HS3530RH operates with little variation in operating characteristics as the supply voltage ranges from 3 to 15V. The device operates from a supply current of 15  $\mu$ A max (assuming a load resistance of 75 k $\Omega$  and a set current of 1.5  $\mu$ A). You can program such parameters as power dissipa-

tion, slew rate, bandwidth, noise, and input dc specs via your selection of an external resistor or current source. The \$220 HR5104RH provides, in a quad-op-amp configuration, all the benefits of close parametric matching that normally come with monolithic construction.

Harris Corp subjects samples of these devices to a total-dose radiation level of  $1 \times 10^6$  rads(Si),  $\pm 10\%$ ,

from a gamma-cell-220, Co60 source or the equivalent. The test applies a supply voltage of  $\pm 15$ V to the devices and irradiates them at a rate of 50 to 200 rads/sec. Harris then performs parametric tests upon the devices within one hour after irradiation. Key parameters measured include open-loop gain, input offset voltage, and bias current.

The lot will be accepted only if the

rads/sec and 2500 rads/sec. (For greater precision, the requirements are currently being amended to  $200 \pm 100$  rads/sec.) A cobalt-60 (Co60) chamber subjects a sample to  $10^5$  rads/hour, which is closer to the irradiation of a nuclear blast than to that of a space environment. The rate of exposure is significant because of the annealing, or self-healing, effect exhibited by ICs. High dose rates don't allow annealing to take place. The manner of testing—parametric vs functional, in situ vs extrachamber, continuous vs intermittent measurement—as well as time delays between the exposure and the measurement will all have an effect upon results. You must address different radiation environments with appropriate system design techniques.

## Better in lead than dead

High-radiation environments of concern fall into three basic categories: nuclear event, space, and nuclear power or fuel-reprocessing plants. The most serious, "nuclear events," are characterized by high levels of x-rays or gamma rays and neutron flux for a very short period of time—typically  $10^{-9}$  to  $10^{-6}$  sec. The intense levels of x-rays can melt the gold metallization or gold bond used to attach the chip to the header. Because the flux from the blast drops off in a manner inversely proportional to the square of the distance from the blast center, the best way to avoid damage is to be far away from the blast.

If you don't have the luxury of locating your circuitry far from the nuclear blast, the next best thing you can do is shield your circuitry with lead, other conditions permitting. If the intensity of the radiation is not sufficient to melt the metallization, you must still take into account the ionizing effects in your system design. If the photocurrents are great enough, parasitic pnpn structures in your op amp may be triggered, and at extreme dose levels,

an excessive carrier population can momentarily approach the doping levels of the semiconductor material, transforming the semiconductor into a resistive element and allowing large, potentially destructive currents to flow.

Linear bipolar elements are most susceptible to this sort of catastrophic failure, and what you as a system designer need to do to prevent damage is to provide external current limiting. In addition, you should select high-frequency parts to allow for bandwidth degradation, and select capacitor values that will store no more than 10  $\mu$ J of energy to prevent them from supplying large currents to the op amp during periods of IC saturation.

## The tangible effects of damage

Neutron-bombardment damage manifests itself in the degradation of a number of performance aspects (mentioned in the main text), and you must make appropriate adjustments in your designs. In addition, electromagnetic pulse (EMP) is a phenomenon associated with a nuclear blast and consequently a cause of concern for system designers. Design precautions for EMP are the same as those for electrostatic discharge (ESD) protection—that is, electromagnetic shielding and resistor-diode networks.

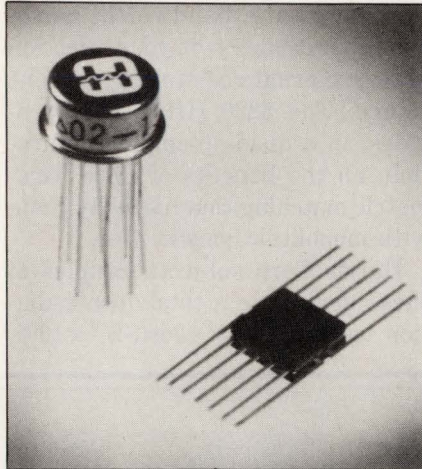
Total-dose radiation is an accumulation of low-level x-ray and gamma radiation that is typically encountered by spacecraft. CMOS parts have traditionally been more susceptible to this sort of radiation than have bipolar parts, because trapped charges in the gate and field oxides cause a shift in thresholds and in transconductances. Offset voltage, bias current, offset current, and open-loop gain will suffer the effects, and your design must take these effects into account.

# TECHNOLOGY UPDATE

sample meets specified limits on these parameters. For example, the HS3516RH must exhibit an open-loop gain that's greater than or equal to 80 dB, the input offset voltage must be less than 5 mV, and the bias current must be less than 400 nA at room temperature. The radiation environment for which the devices are suitable is one where the total neutron fluence ( $E > 10$  keV) is  $5 \times 10^{12}$  N/cm<sup>2</sup>, the gamma rate is  $1 \times 10^9$  rads(Si)/sec, and the total gamma dose is  $1 \times 10^6$  rads(Si) ( $1 \times 10^5$  rads(Si) for the HS5104RH).

National Semiconductor, in concert with the JPL, has developed rad-hard op amps for the Galileo spacecraft. The \$200 LM101A is a general-purpose op amp that features a guaranteed open-loop gain of 88 dB min. The \$220 LM108A is a precision op amp with a guaranteed offset voltage of less than 0.5 mV. The parts were designed to withstand a total dose of  $3 \times 10^5$  rads(Si). National participates in a monitored line program (a production-line inspection plan whereby samples of a product run are extracted and tested), and it has its own gamma cell for in-house radiation testing.

Precision Monolithics Inc offers three op amps that operate at total-dose radiation levels greater than



*Fully characterized for operation over 0 to 250°C, the HA-2620-1 from Harris is an extended-temperature version of a device that specs a 100-MHz gain-bandwidth product at 25°C and a 500-MΩ input impedance.*

$1 \times 10^6$  rads(Si). The OP-15, -16, and -17 are high-speed, FET-input devices. They cost \$6.50.

The dielectric-isolation process, which helps harden ICs against radiation-induced damage, also exhibits excellent high-voltage (to 500V) and high-temperature (200°C) operating characteristics. Telephone companies employ the process in their switching circuitry because of the high voltages in telephony.

DI-processed op amps are used in such high-temperature applications as "down-hole" sensing in oil-well

drilling, where the measurement of such parameters as density, pressure, and sound travel reveal clues to the nature of surrounding formations. In order to have signal conditioning as close to the sensors as possible, the op amps are sent down the hole with the drill, where temperatures reach 200°C.

Jet-engine manufacturers use these op amps to monitor critical performance parameters in engines. The manufacturing environment creates many high-temperature process-control situations, where extended-temperature op amps could be put to use. Clearly, then, if your application requires the increased accuracy that you can achieve by locating your circuitry at the source of your signals, you needn't be daunted by a 200°C environment.

## Play it safe

Although many of the previously mentioned rad-hardened parts are used in extended-temperature applications, they are often used with the knowledge that they are being operated outside the specified temperature range. For those who prefer a more conservative approach to circuit design, a number of op amps are specified and fully characterized for operation at temperatures as high as 250°C.

As is the case in highly irradiated environments, leakage currents are the bane of IC operation at high temperatures. In fact, junction leakage has a major effect on the performance of analog ICs at 200°C and above. Because leakage currents double with every 10°C rise in temperature, a junction that leaks just 50 pA at 25°C will leak 9 μA at 200°C. Linear-IC manufacturers can make adjustments for some of this increase in leakage currents by closely matching transistors (DI processing itself serves to lessen the overall leakage current). If, for example, leakage currents affect two sides of a differential stage, then the difference in leakages is all that degrades circuit performance; if the

## For more information . . .

For more information on the rad-hardened and high-temperature op amps described in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

**Anadigics**  
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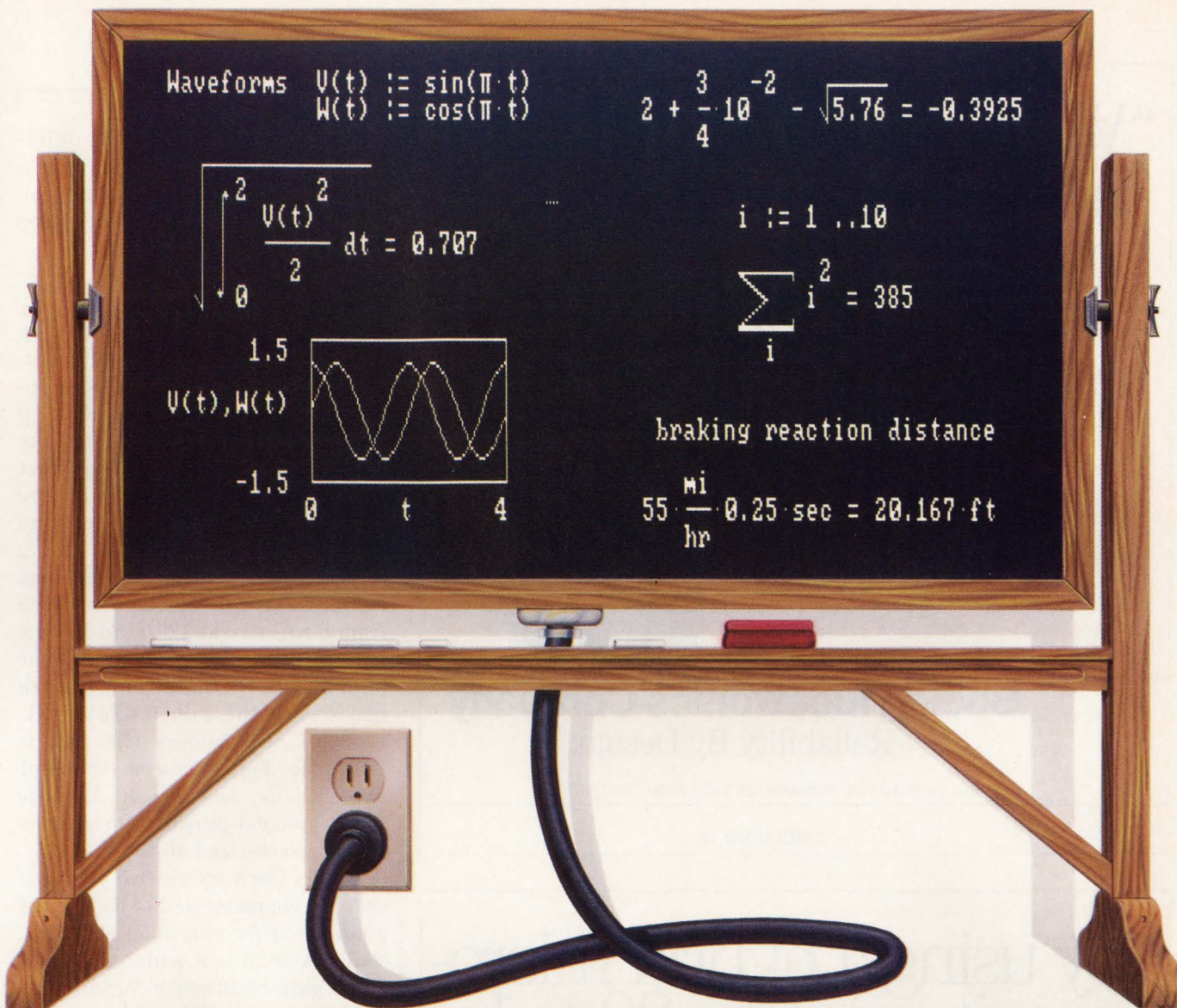
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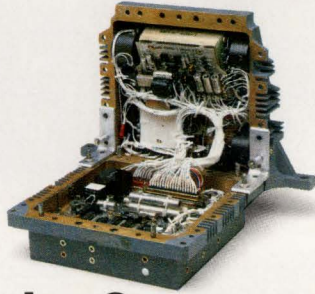
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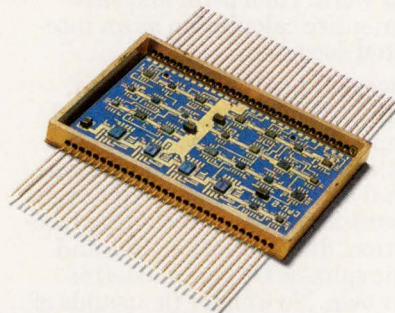


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pair is closely matched, the difference in leakage current will remain small even when the absolute volume of leakage current increases markedly.

### Spec'd to 225°C

Linear Technology offers four op amps that specify a maximum operating temperature of 225°C. For applications in which you must keep noise levels low, you can use the \$31.25 LT1007XH, which is a direct replacement for the OP-27. The \$22.75 LT1001XH precision op amp features a 100-dB CMRR and a 95-dB PSRR at 200°C. The bias current for the device increases from 8 nA max at 125°C to 100 nA max at 200°C. You can fulfill your high-speed, high-temperature needs with the \$18.60 LM118XH. At 200°C, the device's slew rate is 18V/μsec. For your less stringent applications, the \$11.40 LM101-AXH general-purpose op amp is fully characterized at 200°C.

Harris Corp offers two op amps that are characterized to 250°C and guaranteed for operation at 200°C. The HA-2620 is a wideband (100-MHz gain-bandwidth product at 25°C), high-input-impedance (500 MΩ) device specified for operation between 0 and 200°C. It costs \$54.35. The \$59.75 HA 2600-1 has very similar specs, with the exception that its operating temperature range is 0 to 250°C.

Burr-Brown Corp offers a trio of op amps—the OPA111HT, OPA27HT, and OPA37HT—that are specified for operation from -55 to +200°C. The \$59.90 OPA27HT and -37HT come with a mere 250-μV input offset voltage at 200°C and an average drift of 0.25 μV/°C. The \$37 OPA111HT specs a 65-nA bias current at 200°C and features the same pinout as the ubiquitous 741 op amp.

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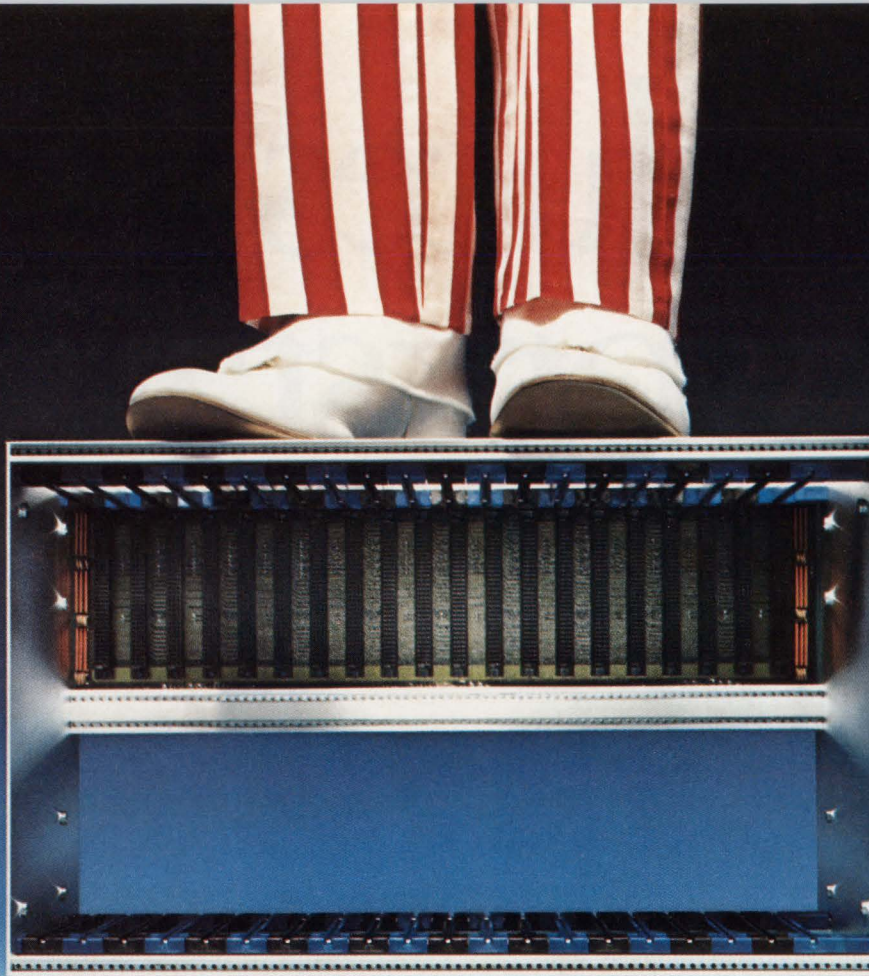
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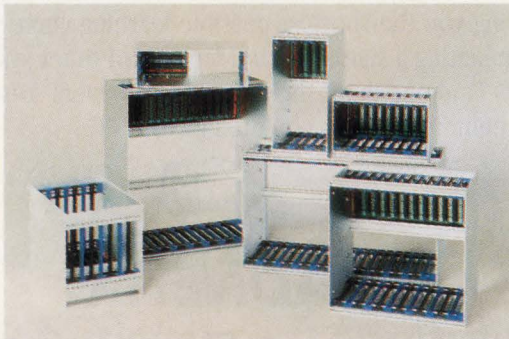


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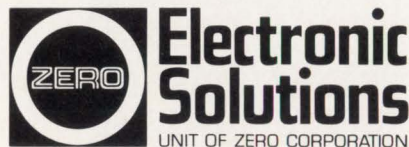
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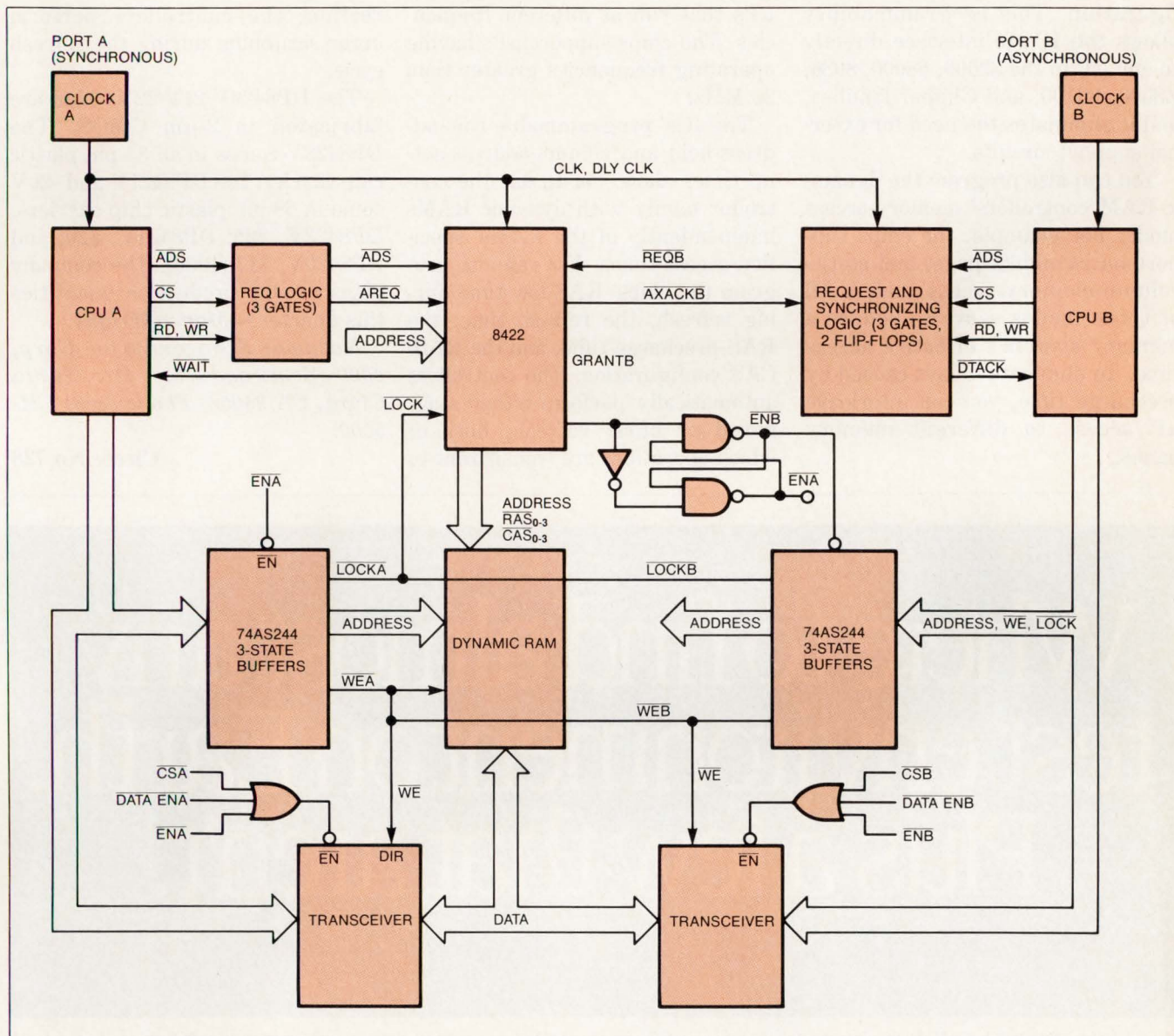
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 CIRCLE NO 97

## CMOS dynamic-RAM-controller ICs support 256k-, 1M-, and 4M-bit devices



Capable of addressing a 64M-byte array made up of 4M-bit dynamic RAMs, the DP8422V dynamic-RAM controller includes all the latches and drive circuitry necessary to provide a single-chip interface between a  $\mu$ P and a dynamic RAM. On-chip dual-port capabilities ease the integration of the DP8422V in DMA, LAN, graphics, and multiprocessor applications.

The DP8420V/21V/22V family of CMOS dynamic-RAM-controller/driver ICs supports 256k-, 1M-, and 4M-bit memory chips. You can program the controllers to access dynamic RAMs in a variety of modes. In addition, the ICs include single-

chip interfaces for popular 8-, 16-, and 32-bit  $\mu$ Ps. The controllers generate all access-control-signal timing, and they automatically refresh the dynamic RAMs.

The controller/driver family comprises the DP8420V, the DP8421V,

and the DP8422V, which support 256k-, 1M-, and 4M-bit dynamic RAMs, respectively. The three chips directly address and drive dynamic-RAM arrays as large as 4M bytes, 16M bytes, and 64M bytes, respectively. The DP8420V and

## PRODUCT UPDATE

DP8421V control single-port dynamic RAMs, and the DP8422V can handle single- or dual-port devices.

The products provide a single-chip interface between  $\mu$ Ps and dynamic RAMs. Because they're programmable, the controllers allow you to alter their control-logic configuration. This programmability allows the ICs to interface directly to any  $\mu$ P in the 32000, 68000, 8086, Z8000, 32100, and Clipper families, and it eliminates the need for external support circuits.

You can also program the dynamic-RAM controllers' memory-access mode. For example, the chips support burst/nibble, page, and static-column memory-access modes. All of these modes serve to reduce a memory system's effective access time. To eliminate delays caused by precharge time, you can interleave  $\mu$ P access to different memory banks.

The DP8422/21/20 controllers include four RAS (row-address strobe) drivers, four CAS (column-address strobe) drivers, a write-enable driver, and address drivers on chip. You can adjust the chips' control-signal pulse widths to facilitate interfacing the controllers to  $\mu$ Ps that run at different frequencies. The chips support  $\mu$ Ps having operating frequencies greater than 20 MHz.

The ICs' programmable row-address-hold and column-address-setup times allow you to use the controller family with dynamic RAMs independently of the RAMs' specified access times. You can also program the chips' RAS-low time during refresh, the refresh time, the RAS-precharge time, and the RAS/CAS configuration. The controllers automatically perform either staggered or burst refresh, both of which operations are transparent to

the system.

The controllers provide zero-wait-state operation at frequencies of 10 MHz and above. They also include programmable wait-state logic, which automatically inserts wait states in a CPU cycle. For systems requiring error detection and correction, the controllers perform error scrubbing during the refresh cycle.

The DP8420V/21V/22V chips are fabricated in 2- $\mu$ m CMOS. The DP8422V comes in an 84-pin plastic chip carrier; the DP8421V and -20V come in 68-pin plastic chip carriers. DP8422V, \$25; DP8421V, \$20; and DP8420V, \$17 (1000). The company plans to ship production quantities this quarter.—**Maury Wright**

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## Self-calibrating 16-bit A/D converter guarantees no missing codes to 50 kHz

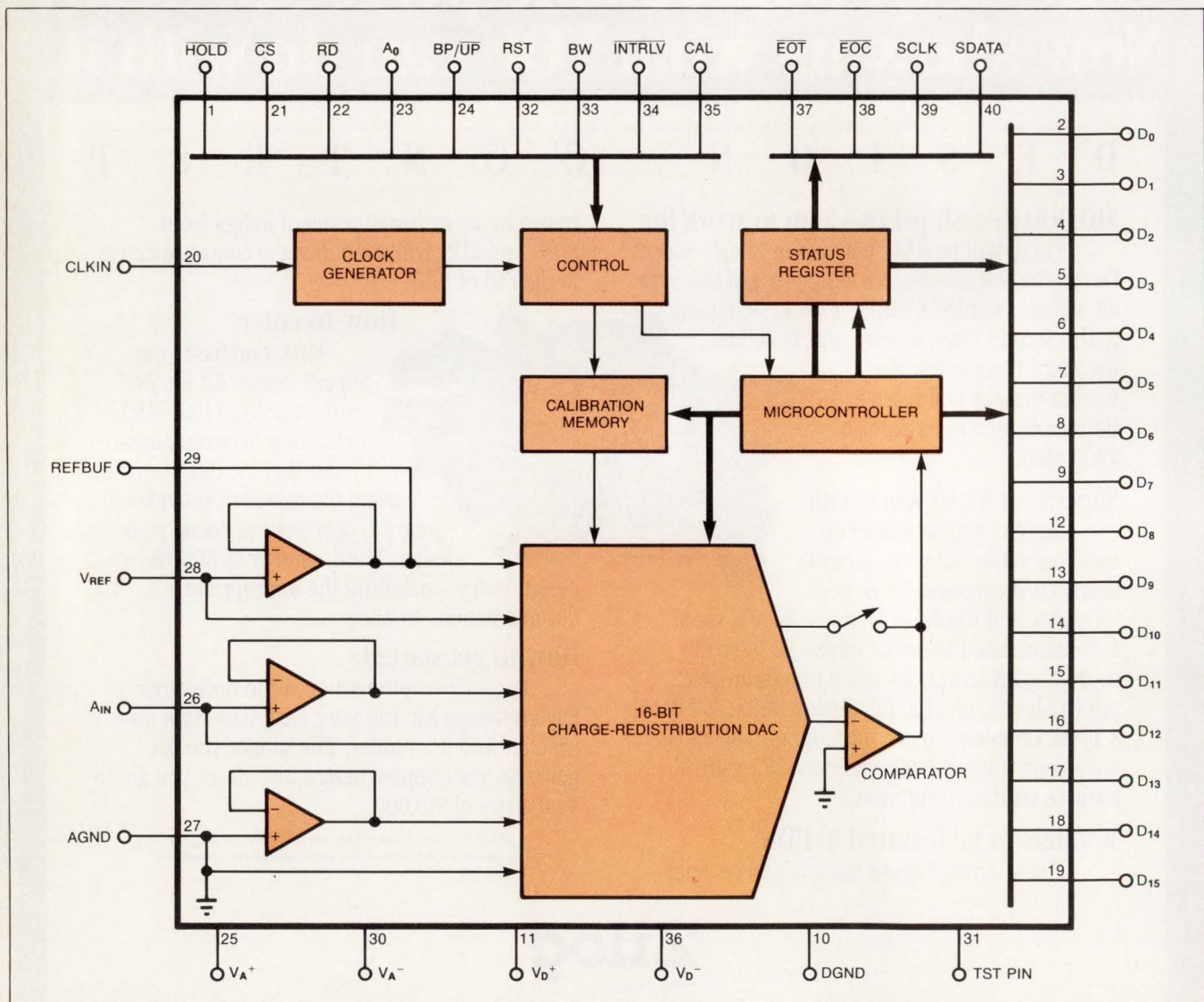
The CS5016 CMOS A/D converter provides a true 16-bit digital representation of a bipolar or unipolar analog signal in 16  $\mu$ sec at sampling rates reaching 50 kHz. The converter also features a self-calibration circuit that ensures maximum non-linearity of  $\pm 0.001\%$  of full-scale range over temperature. It specs no missing codes at 16 bits. Offset and

full-scale errors are  $\pm 3/4$  LSB max, so you don't need to perform any manual calibration.

The monolithic CS5016 contains a D/A converter, a conversion and calibration microcontroller, a clock, a comparator, control-I/O lines, and self-calibration circuitry. The converter dissipates 150 mW.

You can configure, control, and

monitor the CS5016 via its on-chip  $\mu$ P interface, or you can operate the chip independently of intelligent control. An input track/hold function that's inherent in the device's sampling architecture acquires an analog signal within 4  $\mu$ sec after each conversion, so the converter provides throughput rates as high as 50 kHz.



*Maintaining offset and full-scale errors within  $\pm 3/4$  LSB (max), the CS5016 A/D converter provides true 16-bit precision over temperature and a 16- $\mu$ sec conversion time at a throughput rate reaching 50 kHz.*



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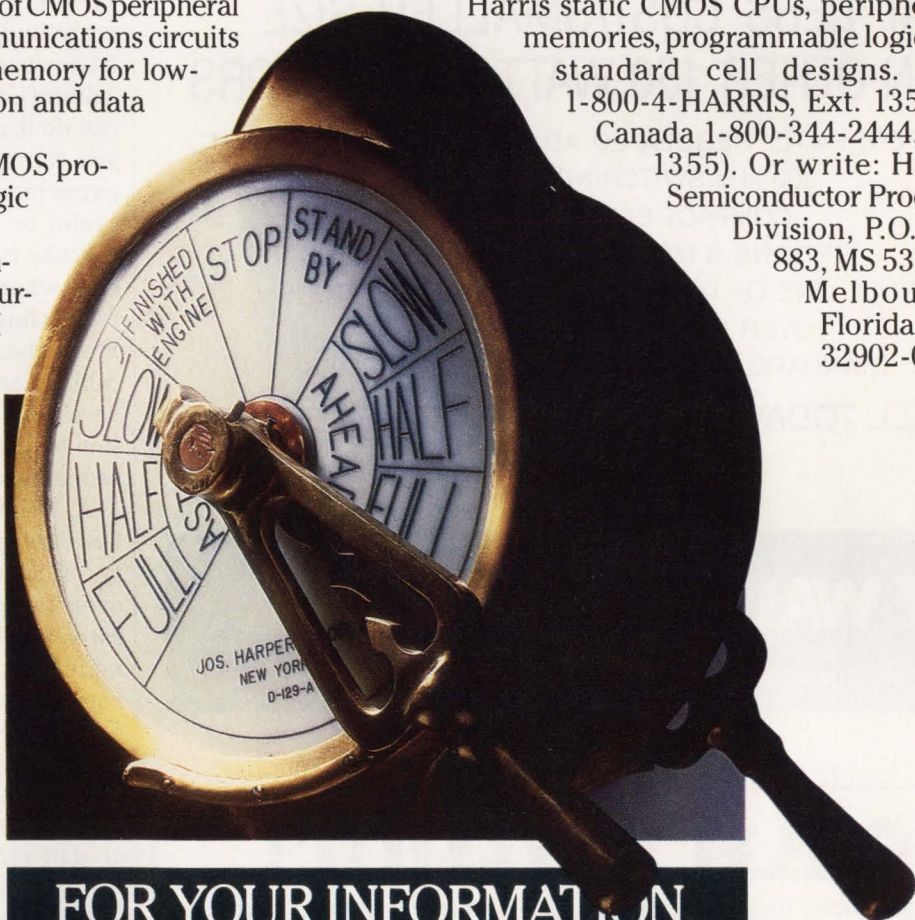
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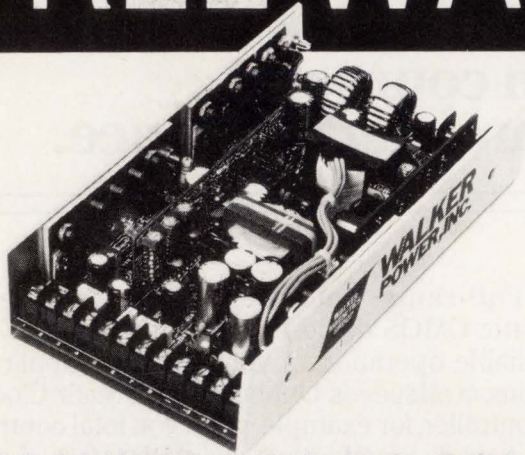


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CIRCLE NO 12

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## UPDATE

The converter uses the successive-approximation technique. However, the IC's charge-redistribution architecture improves on the successive-approximation technique, the manufacturer claims. The DAC is an array of binarily weighted capacitors that share a common node at the comparator's input. The conversion consists of manipulating the free plates of the capacitor array to either  $V_{REF}$  or AGND, so as to arrive at a binary fraction of capacitance that represents the converter's digital output.

This ADC lets you digitally select unipolar or bipolar input ranges. The self-calibration circuitry can operate under intelligent control or in a transparent mode. You can initiate calibration in one of three ways: You can do it arbitrarily after any reset, you can append a single calibration experiment to each conversion cycle, or you can allow the IC to execute a number of calibration cycles whenever the  $\mu P$  finds some free time between conversions. Even though the CS5016 performs calibration operations between conversions, it adjusts its transfer function only after completing the entire sequence of 72,192 operations.

A 14-bit version of the chip, the CS5014, specs maximum nonlinearity of  $\pm 0.003\%$  of full-scale range, over temperature, at throughput rates reaching 50 kHz. The CS5014 maintains offset and full-scale errors within  $\pm \frac{1}{2}$  LSB (max). The CS5014 and CS5016 both come in versions specified for use over 0 to 70°C, -40 to +85°C, and -55 to +125°C. The CS5014, which starts at \$45 (100), is available now in production quantities. Samples of the CS5016, which starts at \$140 (100), are available now; production quantities will be available at the end of the 1st qtr of 1987.

—J D Mosley

Crystal Semiconductor Corp,  
Box 17847, Austin, TX 78760.  
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Circle No 726

# If reliable computers are important to you, imagine what they mean to him.

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It's a monolithic 883C certified RAM available in volume off-the-shelf, with impressive performance features...

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*"Here we are, riding treetops,  
doin' 5-g turns, spins, stalls...  
what a control system."*

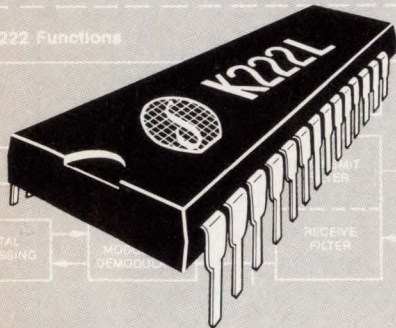
*"We can thank  
Harris for that."*



# SPOTLIGHT #24

IN A SERIES

## NEW + 5V/40mW 1200 BPS SINGLE-SUPPLY ONE-CHIP MODEM



### FEATURES:

- Single + 5V power supply, 40mW max. power
- Integrates both Bell 212A/103 and CCITT V.22/V.21 1200/300 bps standards
- Offers all synchronous and asynchronous modes including 600 bps operation
- Interfaces directly with industry standard  $\mu$ Ps (8051/8048)
- Provides wide dynamic range of 45 db, exceeding Bell specs
- Fully compatible with other SSI K-Series 1-chip modems for easy upgrades

Silicon Systems now offers the industry's only + 5V single-supply, low-power modem IC family. The new SSI K222L modem IC adds its + 5V single-supply capability to the K-Series family of products first introduced in 1985. The K222L integrates both the U.S. Bell 212A/103 and the CCITT V.22/V.21 1200/300 bps standards into one software configurable chip. This will permit users to build low-cost modems that can operate anywhere in the world.

Silicon Systems' K-Series modem family IC's are fully compatible, allowing 1200 bps modem designs to utilize any K-Series family member to meet different operating standards. In the same way, 2400 bps operation can be added using future SSI K-Series products.

Some of the SSI K-Series benefits to the user include: field upgradeability of the product, preservation of the user's hardware/software investments, reduction of user documentation requirements, and a general acceleration of the process of getting the end-user's product to the market faster.

For more information on the SSI K222L and the evolving SSI K-Series modem IC family, contact: Silicon Systems, 14351 Myford Road, Tustin, CA 92680. (714) 731-7110, Ext. 575.

*silicon systems*  
INNOVATORS IN INTEGRATION

## PRODUCT UPDATE

### Calculator symbolically manipulates equations

The HP-28C is the first electronic calculator that's capable of performing symbolic mathematics, according to the manufacturer. In addition to the expected numeric and math-function keys, the calculator sports an alphanumeric keyboard that includes an equals sign. The calculator needs an equals sign because you can enter equations in standard, algebraic order as well as in the company's reverse Polish notation (RPN).

The calculator uses algebraically entered equations in several ways. You can assign a name to each equation and execute the equation simply by invoking the name. Further, you can solve an equation for any symbolic variable after you enter values for the remaining symbolic variables in the equation. You can also apply algebraic manipulation to reduce or reformulate an equation. The unit handles calculations with complex numbers and matrices ex-

actly as it handles real numbers.

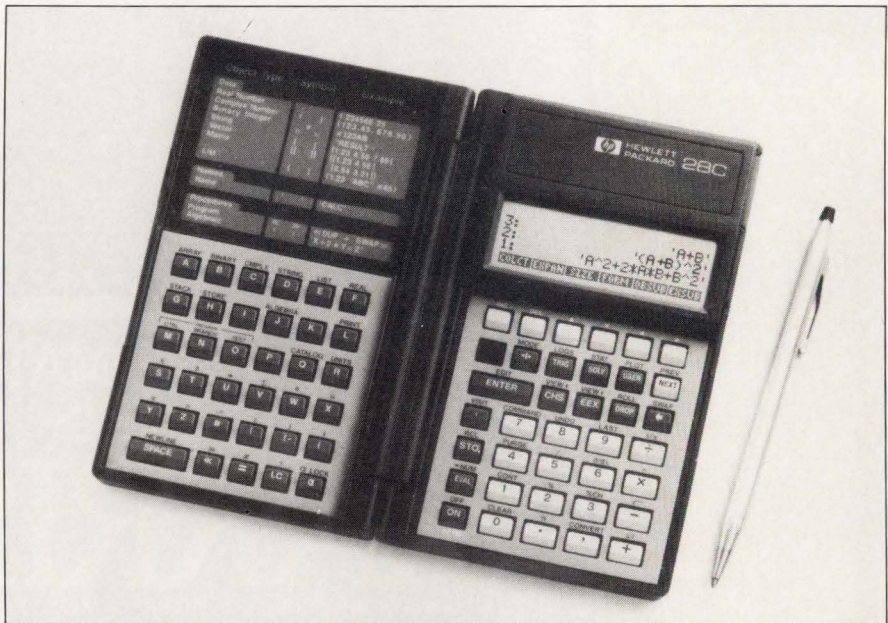
The calculator's 4-line, 23-character LCD can show stack entries, menu selections, and user-entered functions. You can edit incorrect entries instead of rekeying them.

The calculator has 128k bytes of RAM. It has no provision for off-line program storage or remote data entry. It does, however, have an unusual printer port that employs an infrared, wireless link to a companion printer.

The unit can print a graph of any single-valued function, and it can plot statistical data on its screen or on the printer. When open, the calculator's rigid plastic case measures 7.5x6.25x0.5 in. The calculator weighs 8 oz. HP-28C, \$235; printer, \$135.—*Charles H Small*

*Hewlett-Packard Co, Inquiries Manager, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office or (800) 367-4772.*

Circle No 725



Menu selections displayed on a 4-line LCD on the HP-28C scientific calculator replace many of the special-function keys found on other calculators.

# SILICON SYSTEMS FIRST AGAIN — WITH THE ONLY +5V SINGLE-SUPPLY LOW-POWER MODEM IC FAMILY



Now, Silicon Systems has achieved a major technological breakthrough with the SSI K222L. This high-performance 1200 bps, single-chip modem IC requires only a single +5 volt supply and dissipates less than 40mW of power.

The K222L adds its +5V low-power capability to Silicon Systems' K-Series family of single-chip modem IC's without compromising the high standards of performance for which these products are noted. It integrates the Bell 212A/103 and the CCITT V.22/V.21 data communications capability into one compact CMOS chip and includes all features needed for easy

use in intelligent modem applications. This advanced integrated circuit reduces the power required for the modem function by an order of magnitude below other IC solutions, and eliminates the requirement for higher voltages or a separate negative power supply.

The K222L makes possible a variety of new applications. It is ideal for low-power, low-voltage modems; battery-powered, portable modems; power-sensitive laptop PC's; and telephone-line-powered modems—or any application where space and power is at a premium.

Best of all: the K222L is part of the

K-Series family, so all existing 1200 bps modems designed with the Silicon Systems K212L or K221L can be easily upgraded by plugging the K222L into the same socket. And in the future—all modems designed with the K222L can be further upgraded to 2400 bps operation with the Silicon Systems K224L.

For more information on the K222L, or the other K-Series modem IC's, contact: **Silicon Systems**, 14351 Myford Road, Tustin, California 92680, phone: (714) 731-7110, Ext. 575.

Circle 41 for career information

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Circle 2 for product information

## Scanning head lets a plotter digitize drawings

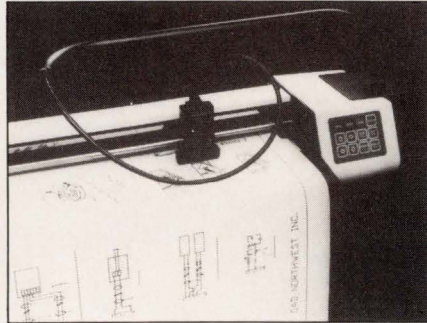
For \$2995, you can add a scanning input device, Scan-CAD (Model 128), to the manufacturer's DMP-50 Series drafting plotter. This scanning head will let you digitize drawings as large as 36x48 in. for storage in your IBM PC/XT, PC/AT, or compatible computer.

The scanning head converts an original hand-drawn or machine-generated hard-copy image to a raster data file that you can manipulate with a variety of software packages. By reading the raster file with AutoDesk's CAD/camera software, you can convert the file to vector data that's suitable for use with AutoCAD and other CAD software programs.

Installation of the input device takes only a few minutes; the scanning head snaps onto your plotter without modification of the plotter. The scanning head's cable plugs into a controller card that you install in scanning width on each pass is 0.6 in. The unit scans 1.2 in<sup>2</sup>/sec and offers 16 levels of gray scale. A replaceable incandescent lamp provides uniform lighting for the scanning unit.

Scan-CAD includes the snap-on one of your PC's full-length expansion slots. The Scan-CAD software interface provides step-by-step help lines to guide you through the scanning process and speed your familiarization with the system.

The device's scanning resolution is 200 dpi. The scanning head can detect lines as fine as 0.007 in. on media such as paper, vellum, acetate film, or blue-line. Although the scanning time depends on the complexity of the drawing, the device can scan a D-size drawing in about 12 minutes and an E-size drawing in about 24 minutes.



*The Scan-CAD digitizing input device snaps onto DMP-50 Series pen plotters. The scanning head lets you digitize drawings as large as 36x48 in. for storage in your IBM PC/XT, PC/AT, or compatible computer.*

The scanning head measures 2.8x2x1.4 in. and weighs 8 oz. The scanning head, 12 ft of cable, a cable-support assembly that clamps to the plotter's end cap, the scanner-controller card, scanning software, a document carrier, and an operation manual. To use Scan-CAD, you need an IBM PC/XT or compatible computer with at least 640k bytes of RAM and a hard-disk capacity of 10M bytes. However, the manufacturer recommends using an IBM PC/AT or compatible computer with 640k bytes of RAM, a 20M- to 40M-byte hard-disk drive, and a Hercules monochrome graphics card. You also need a Houston Instrument DMP-51/52, DMP-51/52 MP, DMP-56, or DMP-56A pen plotter.

—J D Mosley

*Houston Instrument, 8500 Cameron Rd, Austin, TX 78753. Phone (800) 531-5205; in TX, (512) 835-0900.*

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CIRCLE NO 14

# GRAYHILL MINIATURE PUSHBUTTONS: ALL THE FEATURES YOU WANT. SOME YOU PROBABLY HAVEN'T THOUGHT OF!



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  - N.O. or N.C.
  - molded-in terminals
  - impervious to flux contamination
  - water seal and over-travel available

## 46 SERIES

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  - momentary or alternate action
  - shaft and panel seal or total environmental protection

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## 30 SERIES

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  - overtravel or positive feel available
  - N.O. or N.C.
  - with or without shaft and panel seal

## 10 SERIES

- OUR HIGHEST RATED WIPING ACTION SWITCH**
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  - U.L. rated
  - wiping contact provides self-cleaning action
  - N.O. or N.C.

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  - Six bold colors
  - SPST, SPDT and DPDT circuitry

## 39-251

- FOR PC MOUNTING**
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  - terminals on DIP centers
  - low profile

## 7 SERIES

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  - snap-action
  - audible click

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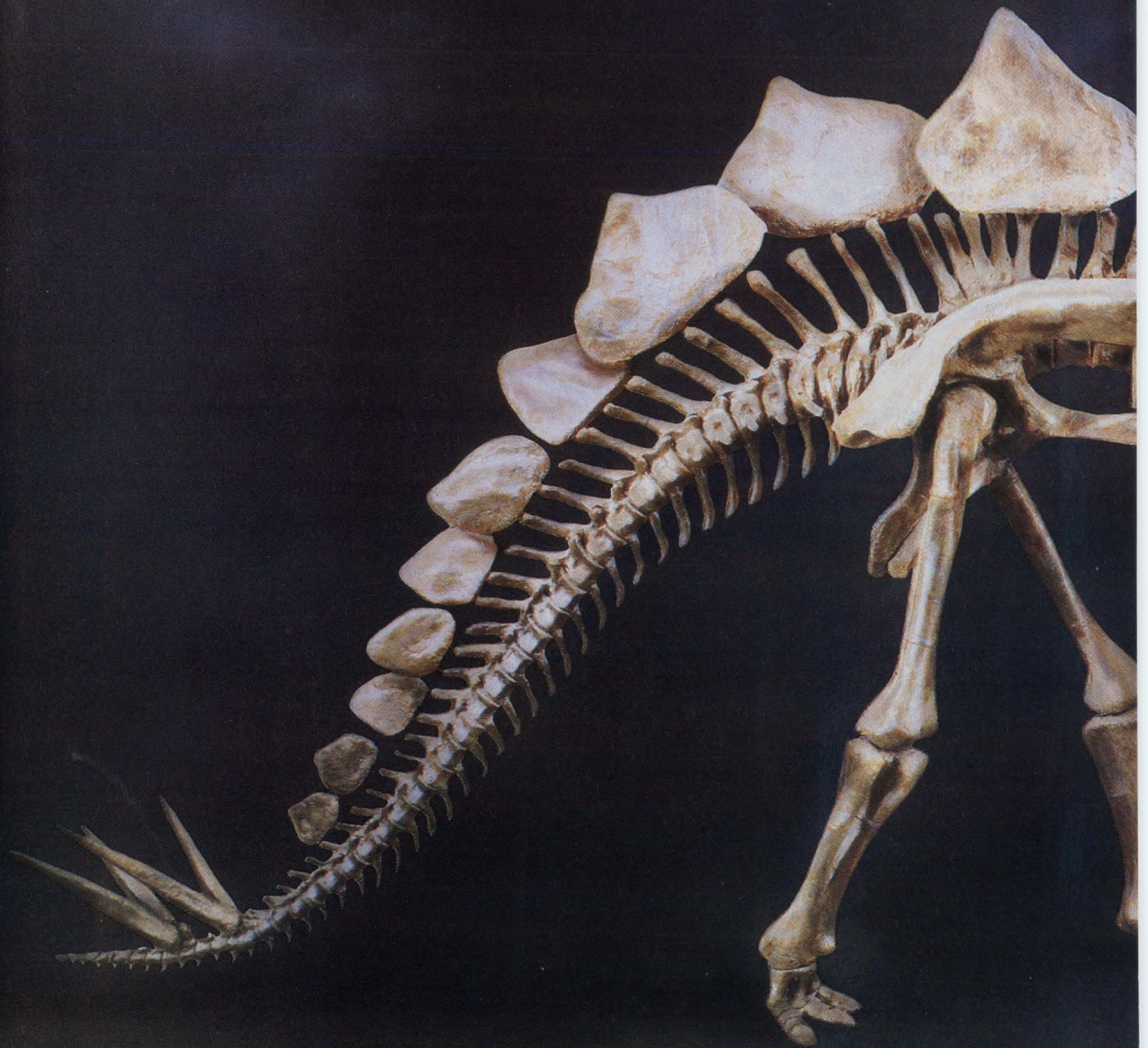
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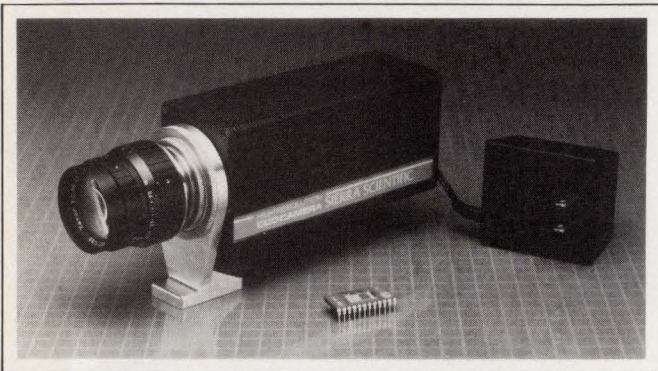
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CIRCLE NO 162

# READERS' CHOICE

Of all the new products covered in EDN's November 13, 1986, issue, the ones reprinted here generated the most reader requests for additional information. In case you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, or refer to the indicated pages in our November 13, 1986, issue.

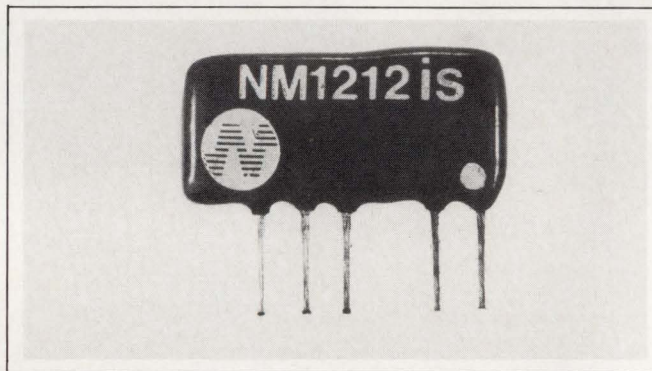


## ▲ CCD CAMERA

This charge-coupled-device (CCD) camera has 8-bit gray-scale capability and is compatible with the RS-170 signal standard for image processing (pg 319).  
**Sierra Scientific.**  
Circle No 715

## AI LANGUAGE

The Smalltalk/V programming language transforms an IBM PC or compatible computer into a programming environment similar to a dedicated AI workstation (pg 404).  
**Digitalk Inc.**  
Circle No 712

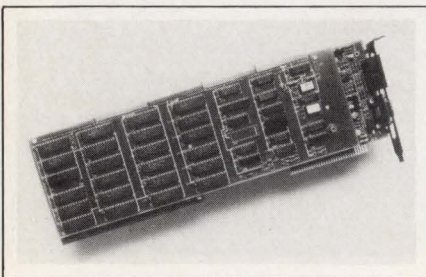


## DC/DC CONVERTERS

The NM0505i, NM1212i, and NM1515i dc/dc converters are capable of delivering as much as 750 mW and produce outputs of  $\pm 5$ ,  $\pm 12$ , and  $\pm 15$ V, respectively, from a 5V supply (pg 385).

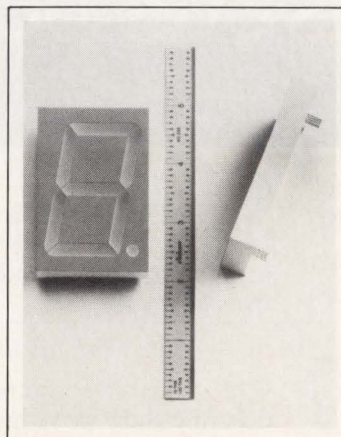
**Newport Components Ltd.**

Circle No 711



## ▲ FRAME GRABBER

The PC-1500 frame-grabber board lets your IBM PC or compatible computer acquire images in real time by capturing a video image in  $\frac{1}{30}$  of a second (pg 355).  
**Chorus Data Systems.**  
Circle No 713

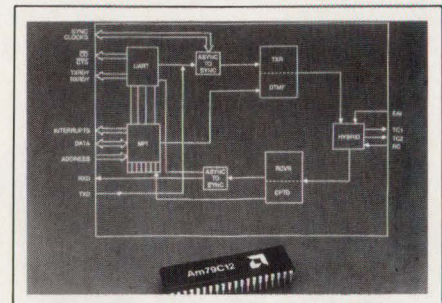


## ◀ LED DISPLAYS

The LR2351E and LR2352E LED displays feature 7-segment, 2.3-in. high-resolution red characters (pg 331).

**IEE Inc.**

Circle No 714



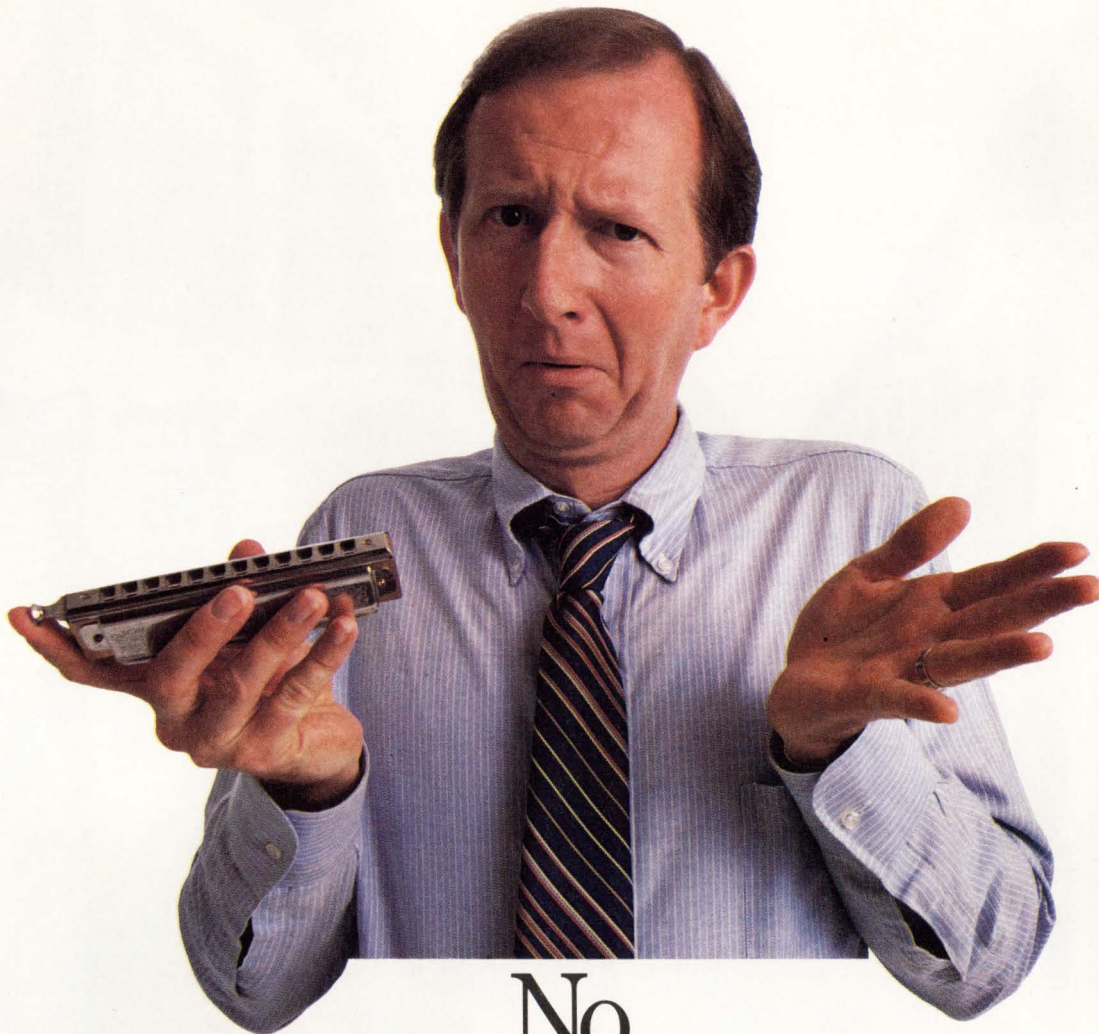
## ▲ CMOS IC

The Am79C12 incorporates a UART, a Bell 212A-compatible modem, and a 4- to 2-wire telephone hybrid on one CMOS IC (pg 110).

**Advanced Micro Devices Inc.**

Circle No 716

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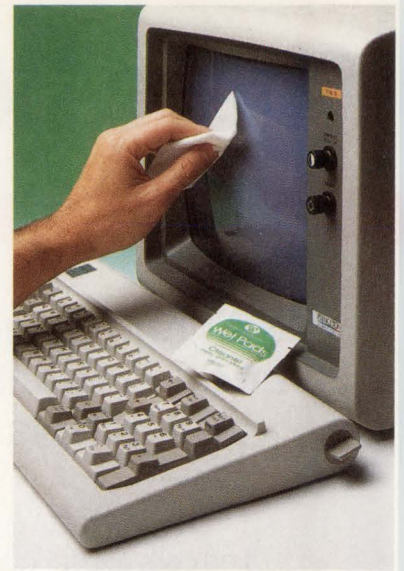
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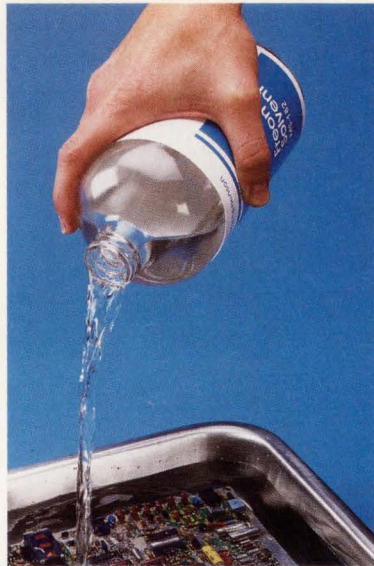
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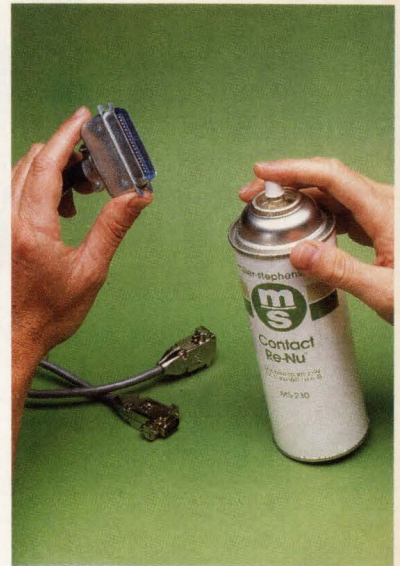
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## INTERFERENCE SUPPRESSORS General Technical Information

The tests described below are those among the tests which are significant for capacitors used as interference suppressors for which national approvals are required.

Standard	Test voltage in type test	Endurance test at $-55^{\circ}\text{C}/105^{\circ}\text{C}$
SEN 432901 (IEC 1611) X-application Y-application	1075 VDC 1 min 1500 VAC 1 min	$1.5 \times U_a$ $1.7 \times U_a$
EMKO (I/N, D, EII) X-application Y-application	1075 VDC 1 min 1500 VAC 1 min	$1.5 \times U_a + 1000 \text{ V}, 50 \text{ Hz}$ $0.1 \text{ sec each hour}^*$ $1.7 \times U_a + 1000 \text{ V}, 50 \text{ Hz}$ $0.1 \text{ sec each hour}^*$
SEV X-application Y-application	1075 VDC 1 min 3 kV surge** 1500 VAC 1 min 5 kV surge**	$1.25 \times U_a + 1000 \text{ V}, 50 \text{ Hz}$ $0.1 \text{ sec each hour}^*$ $1.7 \times U_a + 1000 \text{ V}, 50 \text{ Hz}$ $0.1 \text{ sec each hour}^*$
VDE 0566-1 X-application Y-application	1075 VDC 1 min (X, X <sub>1</sub> ) 4 kV surge (X1)** 1500 VAC 1 min	$500 \text{ V}, 50 \text{ Hz} + 100 \text{ V}, 50 \text{ Hz}$ $0.1 \text{ sec each hour}$ $1500 \text{ hours}^*$
IEC 85	2000 V 50 Hz 1 min Surge: 50 discharges from 1 nF capacitor charged to 10 kV	220 or 440 VAC 0.1 sec exp.
UL 1814 Across-the-line Antenna coupling and line-by-pass	120 V 60 Hz + 5 kV surge 50 discharges from 1 nF capacitor charged to 10 kV	220 or 440 VAC 0.1 sec exp.

\* figure 1  
\*\* figure 2

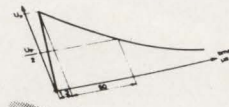
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## INTERFERENCE SUPPRESSORS General Technical Information

**RIFA**  
Figure 1. Endurance test  
According to IEC 384-14 the capacitor shall be recommended to a 220 Ω resistor during the 1000 V period.  
During an IEC-85 test no resistor shall be used.  
During 1985 some countries will make decisions of not using any resistor.

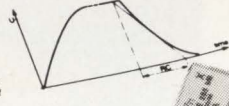


Figure 2. Surge voltage test



According to SEV  
Up for X cap = 5 kV  
Up for Y cap = 5 kV  
According to VDE and IEC 384-14  
Up for X1 cap = 4 kV

Figure 3. Charge/discharge test



According to VDE 0566/1 the capacitors shall be tested 10000 pulses at 100 V/us and 0.2 x U<sub>a</sub> for PHE 800 and PHE 810.  
RIFA tests the capacitors with metallized paper as dielectric 10 times the specified values in the article tables. 10000 pulses and X capacitors 630 VDC. IEC 85 and Y capacitors 1000 VDC.

## Capacitors 1986

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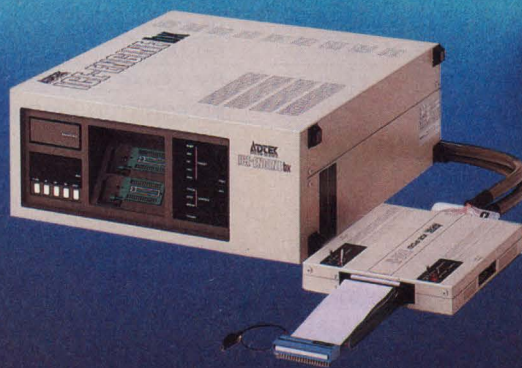
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# LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Last month's average (weeks)	Average (weeks)
<b>TRANSFORMERS</b>								
Toroidal	7	27	47	13	6	0	8.1	8.1
Pot-Core	0	33	34	17	8	0	8.2	6.9
Laminate (power)	5	36	36	18	5	0	7.7	9.0
<b>CONNECTORS</b>								
Military panel	0	22	56	11	11	0	9.6	3.6
Flat/Cable	23	50	18	9	0	0	3.9	3.4
Multipin circular	7	13	60	13	7	0	8.9	4.0
PC	12	41	29	18	0	0	6.0	5.1
RF/Coaxial	23	53	6	18	0	0	4.4	1.8
Socket	17	48	22	13	0	0	4.7	4.7
Terminal blocks	15	48	33	4	0	0	4.2	4.1
Edge card	15	50	20	10	5	0	5.5	6.1
Subminiature	10	40	35	10	5	0	6.5	5.1
Rack & panel	8	46	31	15	0	0	5.8	7.4
Power	14	50	22	7	7	0	5.7	5.0
<b>PRINTED CIRCUIT BOARDS</b>								
Single-sided	0	50	45	5	0	0	5.4	4.9
Double-sided	0	62	38	0	0	0	4.3	5.1
Multilayer	0	30	57	13	0	0	7.2	7.1
Prototype	0	89	11	0	0	0	2.7	2.2
<b>RESISTORS</b>								
Carbon film	50	24	21	6	0	0	3.1	2.2
Carbon composition	37	21	21	21	0	0	5.4	4.0
Metal film	38	27	29	6	0	0	3.8	3.8
Metal oxide	36	18	37	0	9	0	5.6	5.3
Wirewound	25	17	46	8	4	0	6.4	7.7
Potentiometers	23	20	40	13	4	0	6.6	7.7
Networks	31	27	31	4	7	0	5.6	5.2
<b>FUSES</b>								
	48	23	26	3	0	0	3.0	2.7
<b>SWITCHES</b>								
Pushbutton	20	33	40	7	0	0	4.9	5.4
Rotary	5	45	45	5	0	0	5.3	6.1
Rocker	17	39	35	9	0	0	5.0	4.6
Thumbwheel	13	27	33	27	0	0	7.5	8.2
Snap action	33	25	33	8	0	0	4.5	6.9
Momentary	7	43	43	7	0	0	5.4	5.7
Dual in-line	17	41	25	17	0	0	5.5	5.7
<b>WIRE AND CABLE</b>								
Coaxial	44	22	28	6	0	0	3.6	1.9
Flat ribbon	30	44	22	0	4	0	3.6	2.5
Multiconductor	23	53	18	0	6	0	4.0	1.6
Hookup	48	42	10	0	0	0	1.7	1.5
Wire wrap	40	33	27	0	0	0	2.8	2.1
Power cords	25	36	32	7	0	0	4.4	3.5
Other	0	80	20	0	0	0	3.2	5.3
<b>POWER SUPPLIES</b>								
Switching	0	25	50	20	5	0	9.0	5.2
Linear	11	22	44	17	6	0	8.1	4.8
<b>CIRCUIT BREAKERS</b>								
	17	31	35	13	4	0	6.6	5.7
<b>HEAT SINKS</b>								
	24	40	28	8	0	0	4.3	3.5

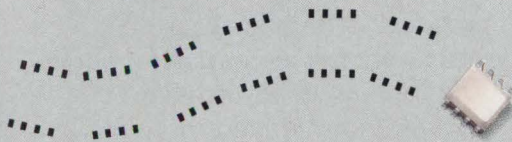
ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Last month's average (weeks)	Average (weeks)
<b>RELAYS</b>								
General purpose	23	27	31	15	4	0	6.5	5.5
PC board	14	27	27	27	5	0	8.3	7.1
Dry reed	18	9	37	27	9	0	10.0	8.7
Mercury	11	22	22	34	0	11	11.0	6.0
Solid state	17	33	17	28	0	5	8.2	7.6
<b>DISCRETE SEMICONDUCTORS</b>								
Diode	39	21	32	5	3	0	4.5	3.4
Zener	30	28	30	12	0	0	4.9	5.0
Thyristor	19	38	25	12	6	0	6.4	4.5
Small signal transistor	35	15	25	20	0	5	7.1	5.1
FET, MOS	5	45	30	10	5	5	7.8	7.1
Power, bipolar	31	25	38	6	0	0	4.5	6.7
<b>INTEGRATED CIRCUITS, DIGITAL</b>								
CMOS	11	33	34	15	7	0	7.6	4.5
TTL	36	24	32	4	4	0	4.7	4.5
LS	29	26	37	4	4	0	5.0	4.3
<b>INTEGRATED CIRCUITS, LINEAR</b>								
Communication/circuit	14	14	58	7	7	0	7.9	4.0
OP amplifier	11	31	31	23	0	4	8.0	6.5
Voltage regulator	19	35	23	19	0	4	6.8	4.5
<b>MEMORY CIRCUITS</b>								
RAM 16k	17	25	33	17	0	8	8.4	4.6
RAM 64k	19	38	25	12	0	6	6.7	4.5
RAM 256k	23	12	47	12	0	6	7.7	5.8
ROM/PROM	25	8	50	8	0	9	8.0	7.2
EPROM	13	33	33	17	0	4	7.3	5.5
EEPROM	19	19	37	19	0	6	8.3	7.8
<b>DISPLAYS</b>								
Panel meters	13	40	40	0	7	0	5.7	5.6
Fluorescent	20	10	30	30	10	0	10.0	8.5
Incandescent	25	0	50	12	13	0	9.3	8.4
LED	14	36	39	7	4	0	5.9	4.9
Liquid crystal	7	7	66	20	0	0	8.7	7.8
<b>MICROPROCESSOR ICs</b>								
8-bit	25	19	38	12	0	6	7.3	7.1
16-bit	5	32	42	16	0	5	8.2	4.3
<b>FUNCTION PACKAGES</b>								
Amplifier	28	18	27	18	0	9	8.3	6.0
Converter, analog to digital	0	37	18	36	0	9	10.8	10.2
Converter, digital to analog	0	20	50	20	0	10	10.7	11.3
<b>LINE FILTERS</b>								
	9	36	37	9	9	0	7.5	5.3
<b>CAPACITORS</b>								
Ceramic	23	33	34	10	0	0	4.9	5.0
Ceramic monolithic	12	38	42	8	0	0	5.4	5.5
Ceramic disc	17	42	29	8	4	0	5.6	4.3
Film	19	27	31	23	0	0	6.7	4.4
Electrolytic	17	34	31	14	4	0	6.3	6.3
Tantalum	19	23	36	19	3	0	7.2	6.3
<b>INDUCTORS</b>								
	12	24	35	23	6	0	8.6	6.3

Source: Electronics Purchasing magazine's survey of buyers

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1986 Hitachi is the first manufacturer that purchasing agents consider when buying CMOS RAMs, as reported by *Electronic Buyers' News*, Buyers' Preference Study.

1986 Hitachi rated the most preferred CMOS RAM vendor in *EBN's* Japanese Semiconductor Manufacturers' Benchmark Study. First in quality, customer service, technical assistance, trust, ease of doing business . . . and first in eight additional categories.

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# Capacitors



*Choosing capacitors often involves a tradeoff among cost, performance, and mounting considerations. This report discusses the parametric and physical aspects of several types of capacitors that are suitable for soldering to pc boards, and it presents a representative sampling of recently introduced devices.*

Bill Travis, *Senior Editor*

It's not a trivial task to select the best type of capacitor for a given application. The choice was once much simpler—for example, you'd be constrained to use an electrolytic type when you needed high capacitance. Now you can

obtain multilayer-ceramic capacitors (MLCs) having capacitance values that rival those of tantalum or aluminum electrolytic units. So to select the optimum type for your system, you must weigh

the various types' advantages and shortcomings, from the points of view of cost, performance, and physical configuration.

Since their introduction in the 1950s, multilayer-ceramic capacitors have made enormous progress in spec parameters, volumetric efficiency, and market acceptance. In fact, they're by far the first choice of system designers for local bypassing and decoupling ("local" in this sense

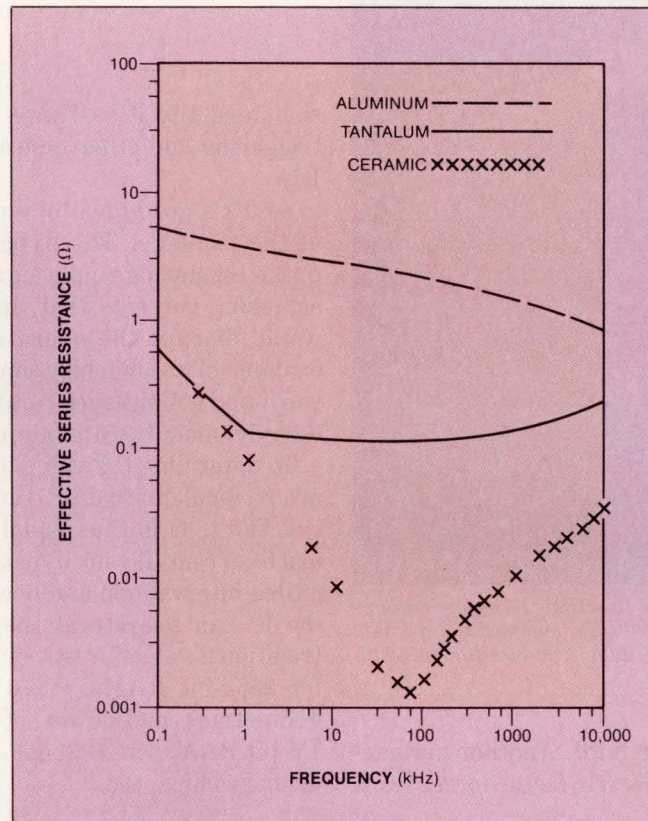
means adjacent to an IC). Their multilayer construction allows the devices to exhibit much greater capacitance per unit volume than do older, single-layer ceramic capacitors.

Advantages of MLCs over other capacitor types include lower effective series resistance (ESR) and effective series inductance (ESL) and much lower leakage currents. Fig 1 shows ESR vs frequency for 24- $\mu$ F aluminum-electrolytic, tantalum, and multilayer-ceramic capacitors. At 100 kHz, the MLC's ESR is about 1000 times lower than that of the aluminum electrolytic and about 50 times lower than that of the tantalum device. Low ESR is, of course, a desirable attribute for a switch-mode power supply's filter capacitors, and you can see from Fig 1's curves that the MLC holds a strong advantage over the other two types for high-frequency switchers.

In terms of leakage currents, aluminum-electrolytic and tantalum capacitors are veritable dc conductors when compared with multilayer-ceramic units. Consider, for example, some high-value MLCs suitable for switch-mode power-supply applications: For two MLC formulations, guaranteed insulation resistance is 100k M $\Omega$ ; for a third formulation, it's 10k M $\Omega$ . (However, both specs add the qualification "or 1000 M $\Omega$ · $\mu$ F, whichever is less." So, for a 100- $\mu$ F capacitor, you'd divide the 1000 M $\Omega$ · $\mu$ F by 100 and obtain 10 M $\Omega$ .)

Now consider the insulation resistance for aluminum-electrolytic and tantalum types. The equivalent spec for these types is expressed in terms of dc leakage current.

*Designing-in a capacitor involves much more than simply drawing the schematic symbol and scribbling a capacitance and voltage value next to it. When it comes to choosing actual devices, you'll face an array of products ranging from multilayer ceramics to aluminum electrolytics. Selecting the ones that best suit your application will involve subtle tradeoffs among price, performance, and physical configuration. (Photo on facing page, courtesy Sprague Electric Co)*



**Fig 1—Electrolytics and tantalums are no match for MLCs at high frequencies, as these curves show. The MLC's superiority in applications needing low series resistance is especially evident at frequencies of 100 kHz and higher. The low-ESR attribute is especially attractive in switch-mode power supplies that use high switching rates. (Courtesy AVX Corp)**

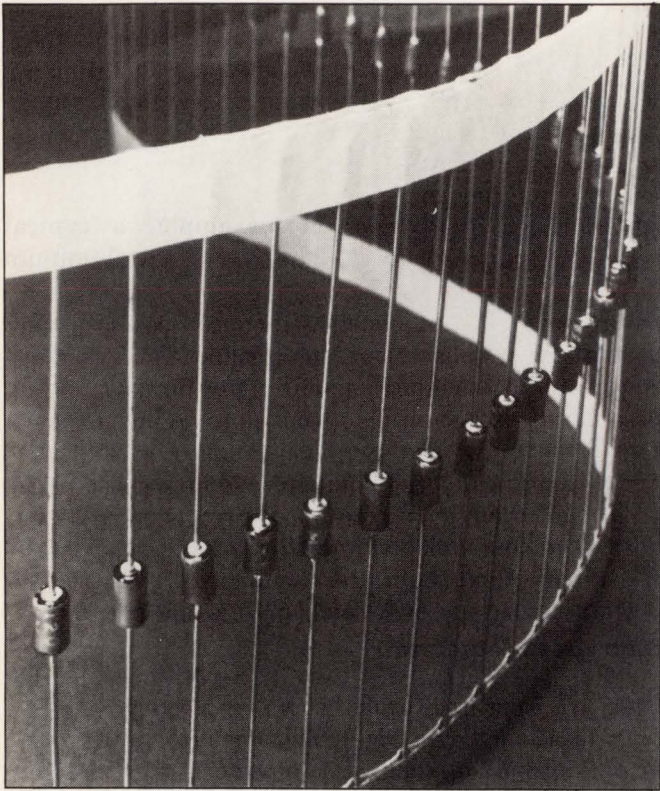
dissipation factor, temperature coefficient, and aging rate.

The most popular temperature characteristics for multilayer-ceramic capacitors are NP0 (also known as C0G), X7R, and Z5U. NP0 units have the lowest dielectric constant and spec a temperature coefficient of  $\pm 30$  ppm/ $^{\circ}$ C max from  $-55$  to  $+125^{\circ}$ C. X7R devices have capacitance values that vary no more than  $\pm 15\%$  over the same range. Z5U units have values that can vary by  $+22$ ,  $-56\%$  from  $10$  to  $85^{\circ}$ C. For X7R units, an additional characteristic called "BX" imposes a voltage coefficient on the capacitors. X7R devices having the BX characteristic can exhibit capacitance changes of  $+15$ ,  $-25\%$  from  $-55$  to  $+125^{\circ}$ C when full rated voltage is applied.

NP0 capacitors are suited for such stability-demanding applications as oscillators and timers. X7R and Z5U devices have much higher values and are therefore useful for bypassing, decoupling, and filtering. The higher values don't come without penalties, though. Dissipation factors (ESR divided by capacitive reactance) for X7R and Z5U units are 2.5 and 3% max,

For example, a typical 220- $\mu$ F, 20V aluminum type has a maximum leakage current (in microamperes) of 0.01 CV, where C is the capacitance in microfarads and V is the applied voltage. The leakage current is thus 44  $\mu$ A, for an effective insulation resistance of less than 500 k $\Omega$ . Tantalum types have similar leakage-current specs.

As their dielectric medium, MLCs use various formulations of barium-titanate ceramic. The different formulations yield varying dielectric constants. A capacitor's dielectric constant determines how much capacitance is obtainable in a given volume for a given number of layers. As in most choices, your selection of an MLC's formulation entails compromises. The higher the dielectric constant (and hence the higher the capacitor's volumetric efficiency), the greater the capacitor's dis-



**Resembling diodes in all but their function**, these multilayer-ceramic capacitors from Unitrode Corp come mounted in tape reels that allow you to take advantage of automatic-insertion machinery.

respectively, vs 0.15% max for NP0. Another parameter that gets worse as the dielectric factor increases is the aging rate.

Aging is the loss in capacitance per decade multiple of time. When you heat an X7R or Z5U capacitor to a temperature greater than its Curie temperature, the crystals in the capacitor's ceramic assume a certain orientation. You then measure the unit's value at 25°C and remeasure the value periodically. The crystal orientation then changes progressively. After one day, the value drops by an amount equal to the device's aging rate. After each decade interval—10, 100, 1000 days, and so on—the unit's value decreases by the aging-rate figure. An NP0 capacitor has zero aging rate; for X7R and Z5U units, the rates are 1.5 to 2% and 4 to 5% per decade, respectively.

### Bring on the bypasses

In any good system design, you shouldn't treat bypass capacitors in an "oh, by the way" fashion. This rule holds true for all systems—linear, digital, or mixed. In analog systems, any ripple on the power-supply lines can find its way to amplifiers' outputs because of the amplifiers' finite power-supply rejection ratios. This feedthrough can be particularly insidious at high frequencies, because PSRR for almost all amplifiers diminishes as frequency increases. In digital systems, large switching currents generated by fast transitions in memory chips and other digital ICs can produce intolerable glitches in the power-supply lines

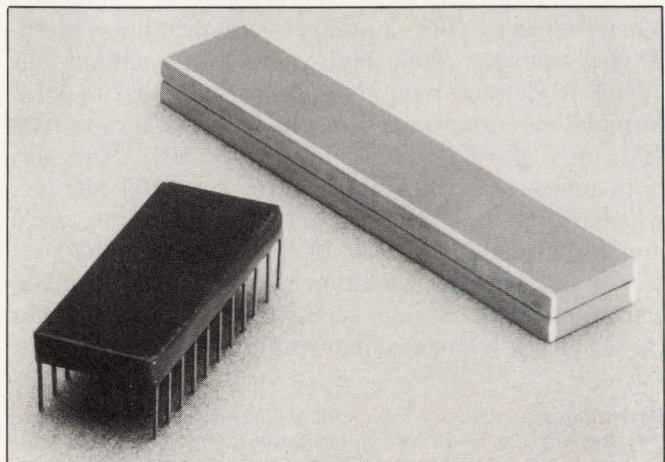
that feed the ICs. These glitches can produce false triggering and other undesirable effects in susceptible ICs.

So it's a good idea to bypass your ICs locally—right at the package. The bypass (decoupling) capacitors quash the analog ripple signals and sink and source the switching currents that, in the absence of bypassing, would disrupt the operation of your system. As an example of a commonly employed bypassing technique, you'll find a multilayer-ceramic bypass capacitor next to each dynamic RAM in all memory systems.

To determine the value of a bypass capacitor needed in a particular situation, remember the simple equation  $i=CdV/dt$ .  $C$  is thus equal to  $idt/dV$ . Determine how much current ( $i$ ) your bypass device must absorb during a time interval ( $dt$ ) and how much voltage change ( $dV$ ) the IC can tolerate at the capacitor's terminals. The traditional value for 64k-bit dynamic RAMs is 0.22  $\mu$ F; for 256k-bit RAMs, it's 0.33  $\mu$ F. Thanks to smaller geometries and lower storage-capacitor values in 1M-bit RAMs, the 0.33- $\mu$ F value will be valid for these memory chips, too.

### Bypass choices abound

In selecting a bypass capacitor to mate with an IC, you have a plethora of packaging-style choices. The choices include bare chips, 2-leaded DIPs, axial cylindrical units, under-the-IC styles, and surface-mount devices. Almost all MLC manufacturers offer bare-chip versions of their capacitors. To gain a feel for the sizes and value ranges available in unencapsulated chips,



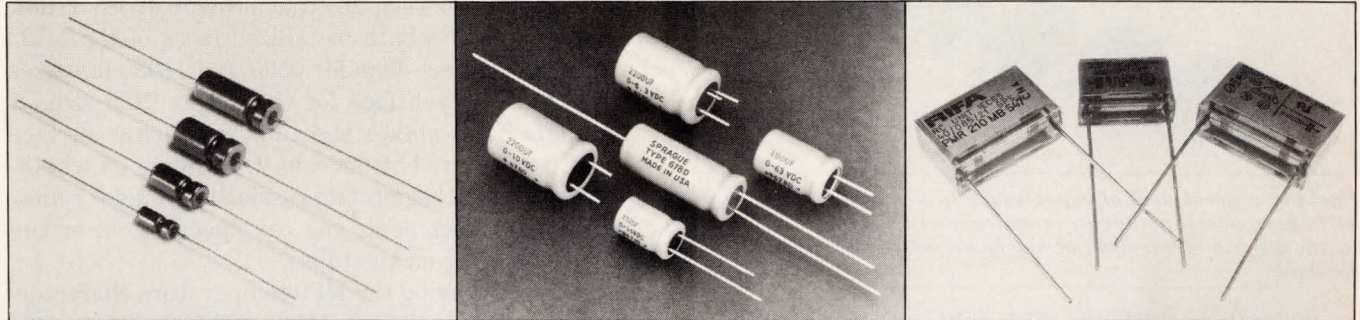
**Ideal for switch-mode power supplies and as entry-level decouplers for pc boards**, the SupraCap multilayer-ceramic capacitors from AVX Corp offer capacitance values previously attainable only from electrolytic units.



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*In terms of leakage currents, aluminum-electrolytic and tantalum capacitors are veritable dc conductors when compared with multilayer-ceramic units.*

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*The use of a tantalum-base metal case in these wet-tantalum capacitors from Tansitor Electronics Inc eliminates metal-migration problems inherent in designs that use a silver case.*

*Low ESR and high ripple-handling capability are the hallmarks of these aluminum-electrolytic capacitors from Sprague. Electrolytic devices offer very high capacitance values per unit volume (and per dollar).*

*Unlike most capacitors, these units from Rifa have a high ESR, which provides arc suppression for contacts in relays and switches. The devices are, in effect, a form of snubber.*

consider the units offered by two typical MLC manufacturers: Murata Erie North America Inc and Kyocera International Inc.

Chip-form MLCs from Murata Erie come in nine sizes. Seven of the sizes follow industry standards for MLC chips, and the numbering system adopted by Murata (and the industry) for these sizes is eminently logical. The first two digits, if you'll imagine a decimal point before them, denote the chip's length in inches; the last two, the width: A device designated 0805 measures 80×50 mils. Murata's seven industry-standard sizes are 0805, 1005, 1206, 1210, 1805, 1808, and 1812. The two nonstandard sizes are 60×30 and 220×200.

Ranges of available values for Murata's chips depend on the devices' voltage rating and temperature characteristic. The available working-voltage ratings for NP0 and X7R chips are 25, 50, 100, and 200V. Ratings are limited to 100V for Z5U devices. For the NP0 and X7R units, the capacitance values available are the same for 25 and 50V units; the Z5U chips offer slightly higher limits for the 25V capacitors.

For NP0 units having Murata's smallest chip size (60×30), the 25/50V units offer values ranging from 0.5 to 120 pF; 100V devices range from 0.5 to 82 pF. 200V chips are not available in this small size. For the largest chip size (220×200), values for 25/50V and 100V chips range from 910 to 10,000 pF; 200V capacitors range from 910 to 2200 pF. X7R chips rated at 25/50V have values ranging from 220 to 4700 pF in the smallest size and from 0.022 to 0.56  $\mu$ F in the largest.

Units having the Z5U temperature characteristic, naturally, offer the highest capacitance values. The dielectric constant for the Z5U ceramic formulation is three to five times higher than that used for X7R

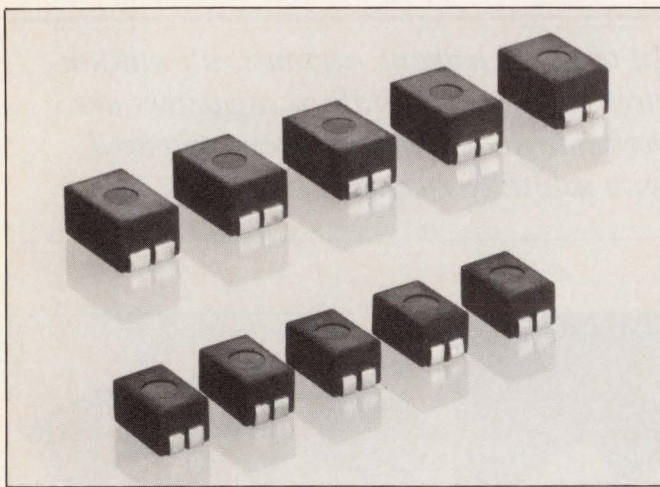
capacitors. For Murata's 60×30 chips, 25V devices offer values from 1000 to 15,000 pF; 50V units, from 1000 to 10,000 pF; and 100V units, from 1000 to 3300 pF. In a notable display of volumetric efficiency, 25V and 50V units measuring 220×200 have values from 0.82 to 1.5  $\mu$ F; 100V capacitors range from 0.22 to 0.39  $\mu$ F.

#### Chip sizes proliferate

Murata isn't the only company offering both industry-standard and proprietary chip sizes; Kyocera also does. The company's standard sizes are 0504, 0805, 1005, 0907, 1206, 1209, 1706, 1808, 1812, 1825, 2018, and 2225. In addition, the company manufactures 0704, 1505, 1805, 2708, and 2321 nonstandard sizes. Thickness for all sizes can range from 40 to 80 mils max. In addition, Kyocera offers a family of low-profile chips for height-critical applications; the thickness for these devices, available in all industry-standard sizes, is 30 mils max.

For Kyocera's 50V units having the NP0 temperature characteristic, values range from 1 to 390 pF for the smallest chip and from 2200 to 33,000 pF for the largest. NP0 devices having a 100V rating offer values from 1 to 270 pF for the smallest size and from 2200 to 22,000 pF for the largest. X7R chips rated at 50V offer values from 470 to 15,000 pF for the smallest size and from 0.1 to 1.2  $\mu$ F for the largest. X7R devices rated at 100V spec values of 470 to 5600 pF for the smallest chip and 0.1 to 0.56  $\mu$ F for the largest. The 50 and 100V units having the Z5U temperature characteristic offer values ranging from 0.1 to 3.9  $\mu$ F and 5600 pF to 1.2  $\mu$ F, respectively.

The most recent addition to Kyocera's chip-capacitor family is a device dubbed "the Suppressor." This capacitor is a Z5U chip that measures 125×100 mils in area



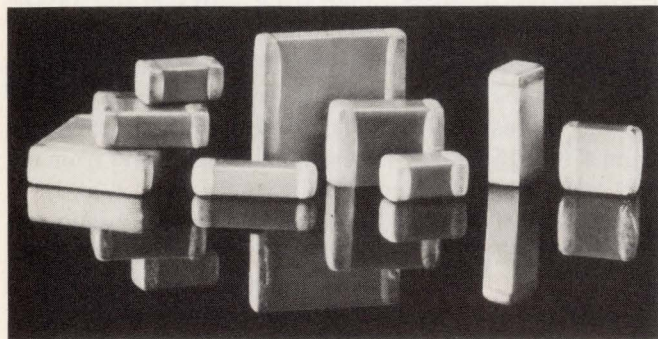
**Packing a great deal of capacitance in a small volume**, these surface-mountable multilayer-ceramic capacitors from Tokin America Inc use a ceramic material having an extremely high dielectric constant.

and 26 mils in thickness. The unit's capacitance is 0.33  $\mu\text{F}$ , the value universally accepted as the optimum one for noise suppression in 256k-bit dynamic RAMs. The chip's minimal thickness allows you to mount it directly underneath the RAM. The Z5U characteristic is not noted for temperature stability: For example, the specs guarantee a capacitance of 0.42  $\mu\text{F}$  min at 25°C with 5V applied, and this value drops to 0.2  $\mu\text{F}$  min over 0 to 85°C. However, the value is still 0.3  $\mu\text{F}$  min at 60°C, so the stability is perfectly adequate in most computer-system environments.

### More MLC configurations

Chip-type multilayer-ceramic capacitors, like the ones discussed so far, are ideal for hybrid-circuit applications and, often, for direct mounting to pc boards. However, in situations that impose large operating-temperature excursions, vibration, and mechanical shock, differences between the chips' coefficient of expansion and that of the medium they're mounted on can contribute to defective solder joints and electrical connections. A family of leaded, surface-mount MLCs from AVX Corp aims to eliminate the possibility of such defects.

The MLC chips, dubbed "Planar," carry tabs (Fig



**These 500V multilayer-ceramic chips** from Johanson Dielectrics Inc are available with NP0 or X7R temperature characteristics and offer a variety of chip dimensions. You can choose palladium or solder coating as the terminations.

2a) or ribbon leads (Fig 2b) that provide stress relief. The tabs connect to both metallized faces of the MLC chip: one tab to each face for 0805 and 1808 chip sizes and two tabs to each face for the larger 2225 size. A right-angle bend makes the tabs' soldering surface flush with the chip's bottom side. Depending on whether you plan to use thermocompression bonding or reflow soldering for attachment, you can specify gold or tin/lead-solder plating on the tabs.

Tabbed units having the NP0 temperature characteristic are available in values of 680 to 22,000 pF for a 50V rating and in values of 560 to 10,000 pF for a 100V rating. Values for X7R devices range from 10,000 pF to 0.47  $\mu\text{F}$  for a 50V rating and from 4700 pF to 0.15  $\mu\text{F}$  for 100V units. For the Z5U characteristic, 50V capacitors offer values from 22,000 pF to 0.56  $\mu\text{F}$ , and 100V versions offer values from 6800 pF to 0.27  $\mu\text{F}$ .

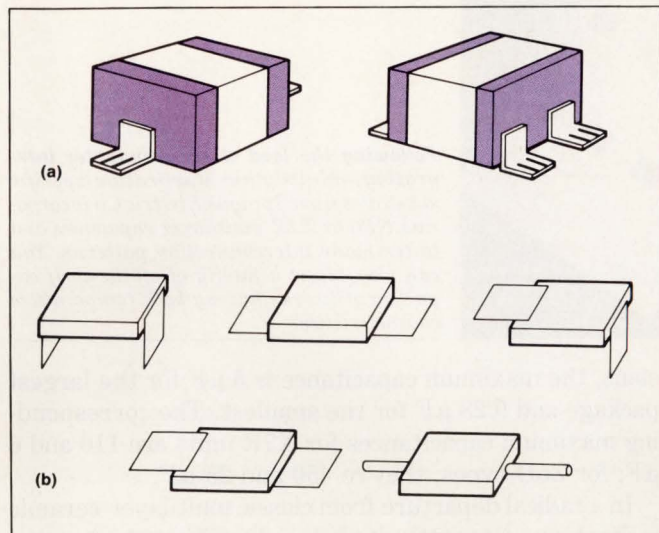
Ribbon-leaded units provide low inductance in high-frequency systems. Compare, for example, the added inductance of an MLC chip that has 93 $\times$ 4-mil ribbons with that of radial- or axial-leaded MLCs. For this comparison, assume 60-mil lead length (per lead) for the radial unit, 135 mils for the axial device, and 50 mils per ribbon for the ribbon-leaded chip. The resulting inductances contributed by the mounting leads are 1.5, 2.4, and 0.6 nH, respectively. The available values for the three temperature characteristics are the same for ribbon-leaded units as those described for the tabbed devices.

A popular configuration for multilayer-ceramic capacitors is the axial-leaded, cylindrical format. The main reason for the popularity of these devices is the large installed base of automatic pc-board stuffers; much like diodes and resistors, the axial units are available in tape-and-reel packaging form to accommodate the automatic-insertion machinery. Axial capacitors come in three packaging styles: conformal epoxy coating, molded epoxy, and diode-type glass packaging.

Glass packaging (Fig 3) is the housing method adopted by Unitrode Corp. The plugs contacting the silver terminations on the MLC chip use a borate/oxide-coated, copper-clad, nickel-iron material. Upon sealing under pressure and high temperature, two bonds emerge. The first, coming from a diffusion of the copper into the silver, is between the copper-clad plug and the chip termination. The second, hermetic bond is between the glass and the plug.

NP0 and X7R units offer voltage ratings of 50, 100, and 200V; Z5U devices come with 50 and 100V ratings. The units come in physical sizes ranging from 170 mils

The most popular temperature characteristics for multilayer-ceramic capacitors are NP0 (also known as COG), X7R, and Z5U.



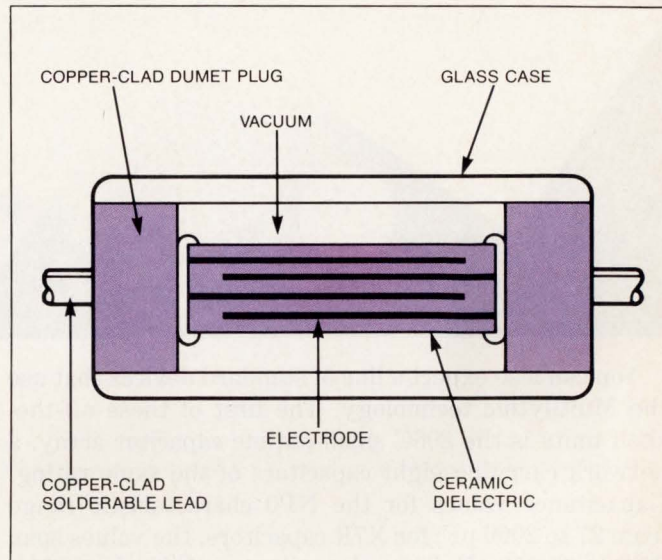
**Fig 2—Designed to relieve stress from dissimilar expansion coefficients, tab (a) and ribbon (b) leads on multilayer-ceramic capacitors can reduce failure rates in systems that experience large temperature excursions. As you can see, these units from AVX Corp are available in a variety of termination configurations.**

long, 100 mils in diameter to 400 mils long, 150 mils in diameter. NP0 capacitors in the smallest package have values from 10 to 680 pF; in the largest size, values range from 1500 to 10,000 pF. For the smallest and largest sizes, X7R devices have values of 390 to 1800 pF and 0.068 to 0.27  $\mu\text{F}$ , respectively. The value ranges for the smallest and largest Z5U units are 1000 to 18,000 pF and 0.15 to 1  $\mu\text{F}$ , respectively. A 0.33- $\mu\text{F}$  Z5U capacitor suitable for decoupling 256k-bit dynamic RAMs comes in a package that's 170 mils long. The unit costs \$0.055 (OEM qty).

### Welcome to Flatland

When you use a capacitor to decouple an IC, you want the capacitor to be as close to the IC as possible, and you want the MLC's leads to be as short as possible. The Kyocera chip already described offers one way to achieve this close proximity. Another method uses a concept called "Bitguard," developed by AVX Corp. This technique involves incorporating the MLC chip directly inside the IC package. Another way to achieve proximity and short leads is to use a flat, under-the-IC decoupling capacitor called "Micro/Q," manufactured by Rogers Corp.

These molded, flat units share the pc-board holes with the leads of the ICs they're bypassing. Available for several logic ICs and  $\mu\text{P}$  and  $\mu\text{P}$ -peripheral families, the \$0.45 (1000) units conform to the environmental and



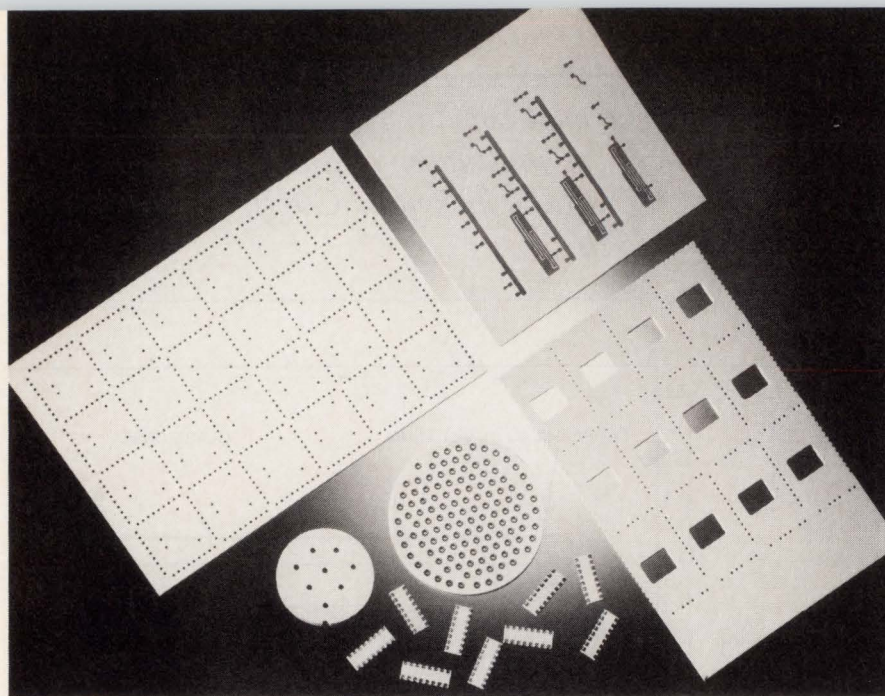
**Fig 3—Is it a diode? No, it's a capacitor. Glass-encased multilayer-ceramic capacitors from Unitorde Corp are suitable for placement by the same automatic-insertion machinery used for other axial-leaded, cylindrical components.**

general specs of MIL-C-39014D and MIL-STD-202F. The latest additions to the series, called Micro/Q II, are available with X7R ( $\pm 15\%$  max capacitance change over  $-55$  to  $+125^\circ\text{C}$ ) and Y5U ( $+22$ ,  $-56\%$  max change over  $-30$  to  $+85^\circ\text{C}$ ) characteristics.

Micro/Q II X7R units offer 0.01- to 0.1- $\mu\text{F}$  values; Y5U devices provide 0.05 to 0.3  $\mu\text{F}$ . The devices fit under 14-, 16-, 18-, and 20-pin, 300-mil DIPs. Capacitance ranges are the same for all sizes. The capacitance-value tolerance is  $\pm 20\%$  for X7R units and  $+80$ ,  $-25\%$  for Y5U devices. The dissipation factors for X7R and Y5U capacitors are 3.5 and 4% max, respectively; both types spec a 50V rating. Micro/Q II devices cost \$0.67 (1000).

### Arrays integrate capacitors

If it makes sense to integrate many semiconductor devices on a piece of silicon, then the same multiple-device concept might make sense for multilayer-ceramic capacitors. Sprague Electric Co is betting that multiple-MLC arrays make eminent sense. The company has set up a facility to manufacture substrates called Multilythics. These substrates can include a variety of capacitors, ground planes, and interconnection schemes. You can consider the Multilythic devices as application-specific substrates. Sprague seeks to enter into mutual development projects with customers seeking solutions for specific application needs.



*Following the lead of semiconductor integration, Multilythic application-specific substrates from Sprague Electric Co incorporate NP0 or X7R multilayer capacitors and tailor-made interconnection patterns. You can also expect a family of off-the-shelf capacitor networks having both temperature characteristics.*

You can also expect a line of standard devices that use the Multilythic technology. The first of these off-the-shelf units is the 806C small-outline capacitor array, a network carrying eight capacitors of the same rating. Capacitance values for the NP0 characteristic range from 27 to 2000 pF; for X7R capacitors, the values span 2000 to 47,000 pF. Operating voltage is 100V dc to 85°C and 50V dc at 125°C. The units cost \$1.50 (10,000); a kit that includes five 100-pF and five 10,000-pF capacitor arrays costs \$50.

### Smoothing the switchers

At first glance, the use of ever higher switching frequencies in switch-mode power supplies seems both desirable and straightforward. The higher frequencies should allow the use of magnetic devices that are smaller and lighter and filter capacitors that have lower values. However, problems arise when you use capacitors (and magnetic components, for that matter) in high-frequency circuits.

Aluminum-electrolytic and tantalum capacitors both suffer from high ESR and ESL, as compared with multilayer-ceramic devices, as Fig 1 shows. For high-frequency switchers, the inductive effect becomes predominant in determining the capacitor's impedance. The classic solution for reducing the filter capacitors' impedance in high-frequency switchers is to connect several electrolytic or tantalum units in parallel. You might find it more economical, however, to use high-value, multilayer-ceramic capacitors instead.

A line of capacitors called "SupraCap" from AVX Corp comes in DIP-style packages and offers capacitance values that are suitable for filtering high-frequency, switch-mode supplies. Each of the five package sizes—2.1×0.5, 1.6×0.95, 1.1×0.5, 0.43×0.41, and 0.28×0.27 in.—contains five MLC chips in parallel. You have a choice of four voltage ratings—50, 100, 200, and 500V—and the three popular temperature characteristics: NP0, X7R, and Z5U (200V limit). For NP0 ver-

sions, the maximum capacitance is 5  $\mu$ F for the largest package and 0.28  $\mu$ F for the smallest. The corresponding maximum capacitances for X7R units are 110 and 6  $\mu$ F; for Z5U types, they're 450 and 25  $\mu$ F.

In a radical departure from classic multilayer-ceramic technology, a recently introduced series of high-value MLCs from Marcon America Corp (a member of the Toshiba group) uses a ceramic material based on niobium oxide. The company claims the material has twice the dielectric constant attainable from conventional dielectrics (that is, barium titanate). Values and voltage ratings range from 0.1 to 47  $\mu$ F and 50 to 400V, respectively. Devices having CV products as high as 2350 are available.

To gain a feel for the volumetric efficiency of the niobium-based MLCs, consider the size of a 47- $\mu$ F, 50V unit: 28×10×7.5 mm (1.3×0.39×0.3 in.). The devices' temperature characteristics correspond to X7V (+22, -82% max value change over -55 to +125°C) or Y5U (+22, -56% max change over -30 to +85°C). Capacitance tolerances are  $\pm$ 20% and +80, -20%. A 10- $\mu$ F, 50V capacitor costs \$2.30 (OEM qty).

### More high-CV MLCs from Asia

While you're considering the Marcon-Toshiba high-CV MLCs, you can continue looking toward the East for yet another source of multilayer-ceramic devices that pack astounding amounts of capacitance per unit volume. A recent line of surface-mount MLCs from Tokin America Inc uses very thin layers and a ceramic material that boasts a dielectric constant of 20,000, vs the 4000 to 11,000 of other MLC manufacturers' Z5U ceramics.

In addition to having extremely high CV products—10 to 100  $\mu$ F at 25V working voltage—Tokin's surface-mount capacitors promise to be economical in high-volume applications. The manufacturer claims to use low-cost electrode materials (a silver-palladium mix), rather than the more costly pure palladium used in

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*The traditional bypass value for 64k-bit dynamic RAMs is 0.22  $\mu$ F; for 256k-bit RAMs, it's 0.33  $\mu$ F.*

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other MLCs. Sample prices are \$2.70 to \$8.90 for 10- to 100- $\mu$ F, 25V devices; \$3.80 to \$6.70 for 10- to 33- $\mu$ F, 50V units; and \$4.90 to \$5.70 for 10- and 15- $\mu$ F, 75V capacitors.

Multilayer-ceramic capacitors' attractive specs notwithstanding, the fact remains that for certain applications, aluminum-electrolytic or tantalum capacitors represent the optimum choice. For high capacitance values, aluminum and tantalum units pack more microfarads per unit volume—and per dollar—than multilayer-ceramic capacitors can.

Some aluminum electrolytics from Sprague Electric Co serve to exemplify the high CV products and low prices possible with electrolytic units. Series 678D miniature aluminum electrolytics have about twice the ripple-handling capabilities available from other Al devices (for example, Sprague's 672D family). Low ESR is the key to their ripple-handling ability. For example, a 1000- $\mu$ F, 16V capacitor has a maximum ESR of 66 m $\Omega$  at 40 kHz and 25°C. Typical of the low prices of aluminum electrolytics, this 1000- $\mu$ F, 16V capacitor costs \$0.232 (10,000). 678D units come in eight voltage ratings from 6.3 to 63V dc; the maximum capacitance values for the lowest and highest voltage ratings are 6800 and 680  $\mu$ F, respectively.

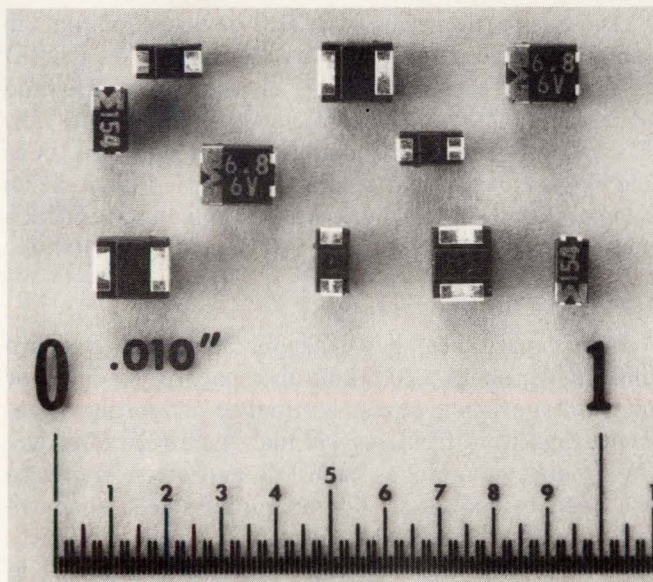
Instead of aluminum electrolytics, you might consider using solid-tantalum capacitors in applications that demand a lot of capacitance in a small package. Solid-

tantalum units from several manufacturers come in a chip format that lends itself to easy surface mounting. For example, a recent family called the 293D from Sprague Electric Co conforms to IEC QC300801/001, the new EIA industry spec for standard capacitance-range devices.

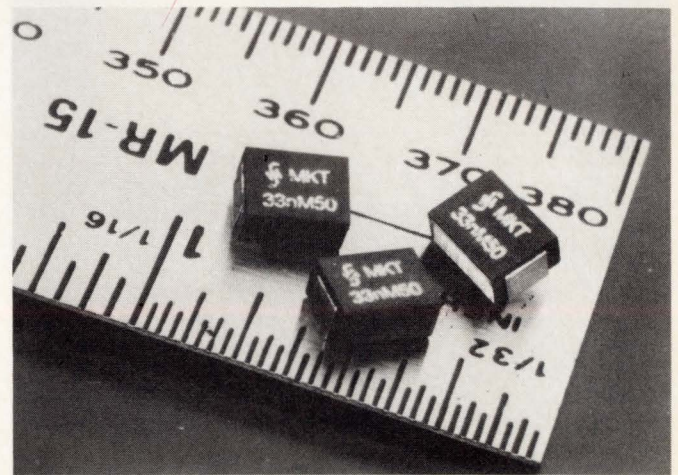
Models in the 293D Series (dubbed "Domino") come in four package sizes. They offer voltage ratings from 4 to 50V dc and capacitances from 0.1 to 100  $\mu$ F. The capacitors' operating-temperature range is -55 to +85°C; linear derating to 67% of rated voltage permits operation to +125°C. The company supplies the tantalums taped on 8- or 12-mm reels in conformance with EIA 481A for use with automatic-placement machinery. A 1- $\mu$ F $\pm$ 20%, 35V unit costs \$0.21 (1000).

Surface-mountable solid-tantalum capacitors are a specialty of Mepco/Centralab Inc. For example, the company's 49MC family of SM devices comes in four case sizes that conform to the EIA's proposed standard IS-28 for tantalum chip capacitors. Packaged in 8- and 12-mm carrier tape widths, the units offer values from 0.1 to 68  $\mu$ F and voltage ratings from 4 to 35V dc. The electroplated tin/lead terminations make the capacitors suitable for most solder-reflow applications. The typical price (for a  $\pm$ 10% capacitor rated at 35V) is \$0.32 (1000).

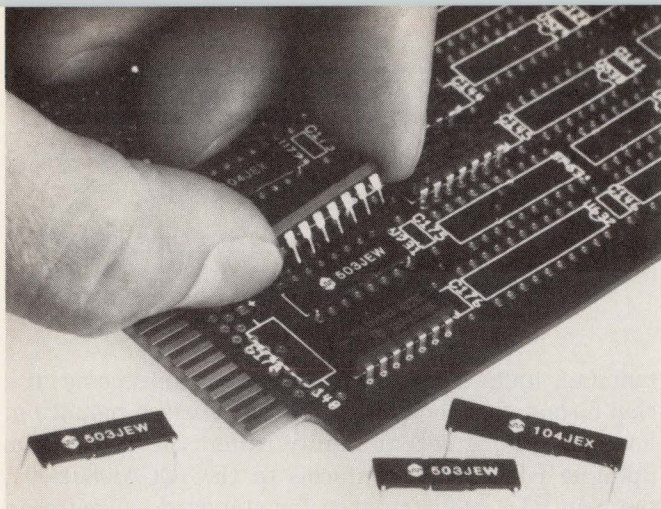
Another solid-tantalum chip series from Mepco/Centralab is the 49SC family. These units are similar to the 49MC devices but come in five case sizes and offer higher CV products: 0.47 to 100  $\mu$ F at 4 to 50V dc. The devices are pad compatible with MIL-C-55365/4



**Mounting solid-tantalum capacitors is easy** if you use devices like these SM units from Mepco/Centralab. The capacitors are suitable for mounting on pc boards, as well as for use in hybrid circuits.



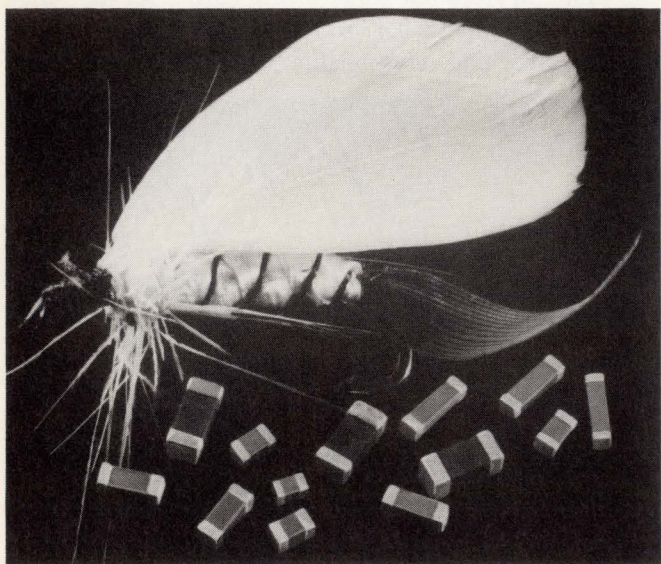
**High insulation resistance and pulse strength and low dissipation factors** are inherent in these surface-mountable, stacked-film capacitors from Siemens Corp. They're available in 12-mm tape format to accommodate automatic-placement machinery.



**Closeness is the key word in bypassing ICs.** These flat decoupling capacitors from Rogers Corp mount directly underneath the ICs they're decoupling, and they even share the pc board's holes with the ICs' leads.

(CWR-06) capacitors. Typical pricing for the 49SC Series (10% tolerance, 35V) is \$0.70 (1000). The company's 49BC family, dubbed "Blue Chip," is available in industrial or in established-reliability models. The latter devices are qualified to MIL-C-55365/4, style CWR-06, established-reliability failure-rate R. The chips come in eight case sizes and have ratings of 0.1 to 100  $\mu\text{F}$  at 4 to 50V dc. Typical prices for industrial and MIL-grade capacitors are \$2.21 and \$4.81 (1000), respectively.

Another specialist in surface-mountable solid-tantalum chips is Tansitor Electronics Inc. The company's SM family of solderable chips comes in six case sizes and ratings of 0.1 to 100  $\mu\text{F}$  at 4 to 50V dc. You have a choice of terminations for the SM Series devices: gold for conductive-adhesive bonding or 60/40 tin/lead solder for solder reflow, wave soldering, or vapor-phase soldering. The chips are packaged on 8- or 12-mm tape reels. Typical pricing (in 100s) for  $\pm 20\%$  units ranges from



**Much as a fly lures an unsuspecting trout,** these multilayer-ceramic chips from Corning Glass Works trap and kill glitches and ripple in electronic systems. If you provide the proper pads, the units are easy to mount on pc boards and in hybrid circuits.

\$0.50 in case-size 1 to \$1.40 in case-size 6.

If you need higher CV products than you can obtain from the solid-tantalum capacitors described so far, consider wet-tantalum devices, which use a sintered-anode, gelled-electrolyte design. Recent offerings from Sprague and Tansitor serve as good examples of what's available in wet tantalums.

A series of units from Sprague meets the requirements of MIL-C-39006/26; MIL-qualified (CLR75) devices are available. Ratings for the capacitors, designated 238D, range from 2200  $\mu\text{F}$  at 6V dc to 39  $\mu\text{F}$  at 150V dc; available tolerances are  $\pm 10$  or  $\pm 20\%$ . The manufacturer claims that the use of a tantalum-based metal case (vs the traditional silver case) eliminates the metal-migration problems inherent in older designs. The 238D capacitors withstand 1V reverse voltage, vs the 0.5V usually specified for wet-tantalum devices. A 56- $\mu\text{F}$ , 75V capacitor costs \$6.55 (1000).

Recent wet-tantalum units from Tansitor also use a tantalum-based case. The company's AR units conform to MIL-C-39006/25, type CLR81. The all-tantalum devices replace the silver-cased units that conform to MIL-C-39006/21, type CLR69. Four case sizes are available; capacitance values and working voltages span 6.8 to 2200  $\mu\text{F}$  and 6 to 125V dc. The devices withstand 3V reverse voltage. Typical prices for  $\pm 20\%$ -tolerance CLR81 units that satisfy failure-rate level M range from \$8.95 (100) in case-size 1 to \$16.80 (100) in case-size 4.

Another recent series of CLR81 devices that come in tantalum-based cases is Mallory Capacitor Co's CLR81 family. These capacitors, like Tansitor's, can withstand 3V reverse voltage. The company claims the units' low ESR allows them to withstand as much as three times the ripple current that similar silver-cased devices can handle. Prices for the established-reliability, DESC-approved devices range from \$13.57 to \$19.38 (1000).

#### Use MLCs for high voltages

High capacitance, low leakage, and small size are difficult parameters to obtain in capacitors needed for high-voltage applications. A number of multilayer-ceramic capacitors from several manufacturers offer the CV-product advantages of MLCs and often eliminate the need to use older, "doorknob" devices that are heavy, bulky, and difficult to mount. A family of chips from AVX Corp illustrates the capabilities of MLCs in high-voltage systems.

The bare chips come in NP0 and X7R formulations and in sizes ranging from 1808 (180 $\times$ 80 mils) to 3640

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*Differences between chip capacitors' coefficient of expansion and that of the medium they're mounted on can contribute to defective solder joints.*

(360×400 mils). NP0 devices have voltage ratings from 1000 to 5000V. Depending on chip size, the 1000V units offer capacitance values from 100 to 33,000 pF; 5000V devices have capacitances from 100 to 330 pF. You can obtain X7R capacitors having voltage ratings from 600 to 2500V. Capacitance values for 600V devices range from 560 pF to 1  $\mu$ F; for 2500V units, capacitance ranges from 100 to 4700 pF.

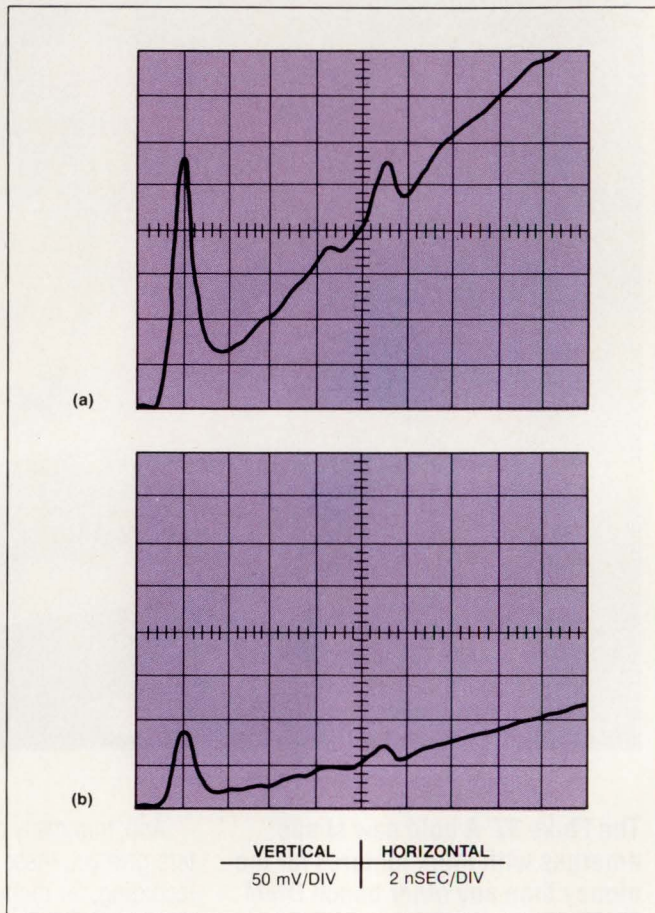
You can obtain an even wider range of ratings and bare-chip sizes from Centre Engineering. This company's high-voltage MLCs come in sizes ranging from 2518 (250×180 mils) to 6765 (670×650 mils); these units, too, offer NP0 or X7R temperature characteristics. NP0 capacitors rated at 500V range from 10 to 39,000 pF; 5000V devices have values ranging from 56 to 470 pF. For 500V X7R units, values range from 470 pF to 1  $\mu$ F; values for 5000V capacitors range from 1500 to 10,000 pF. A typical price for a 5000V, 10% X7R unit is \$0.95 (1000).

Finally, consider a series of 500V MLCs from Johanson Dielectrics Inc. Available in bare-chip sizes 1206, 1210, 1812, and 2221, the devices also offer NP0 or X7R temperature characteristics; their capacitance values range from 470 pF to 0.15  $\mu$ F. The units come with terminations of palladium or nickel-barrier solder coating. Prices range from \$0.29 to \$1.89 (1000), depending on chip size and value.

### High frequencies: Tough on caps

High levels of integration, coupled with the very high speeds of modern silicon and gallium-arsenide ICs, impose special demands on the high-frequency performance of capacitors. The most crucial need in these applications, of course, is for low inductance. Chip capacitors from several sources satisfy the low-ESL requirement.

Consider, for example, a series of low-ESL chips from AVX Corp. Designed for VLSI- and VHSIC-IC decoupling, the chips have aspect ratios and sizes that reduce series inductance from the 2 nH you'd usually encounter in MLCs to less than 0.5 nH. Fig 4 shows the result of applying a 200-mA/nsec current front to a standard 10-nF chip (a) and to a low-inductance chip of the same rating (b). The devices come with X7R or Z5U temperature characteristics and in case sizes of 0508, 0510, and 0612. In addition, AVX offers capacitors having a special temperature-characteristic formulation; the capacitance value for these devices peaks at 60°C. These devices have voltage ratings of 25 or 50V and capacitance values from 10 to 82 nF.



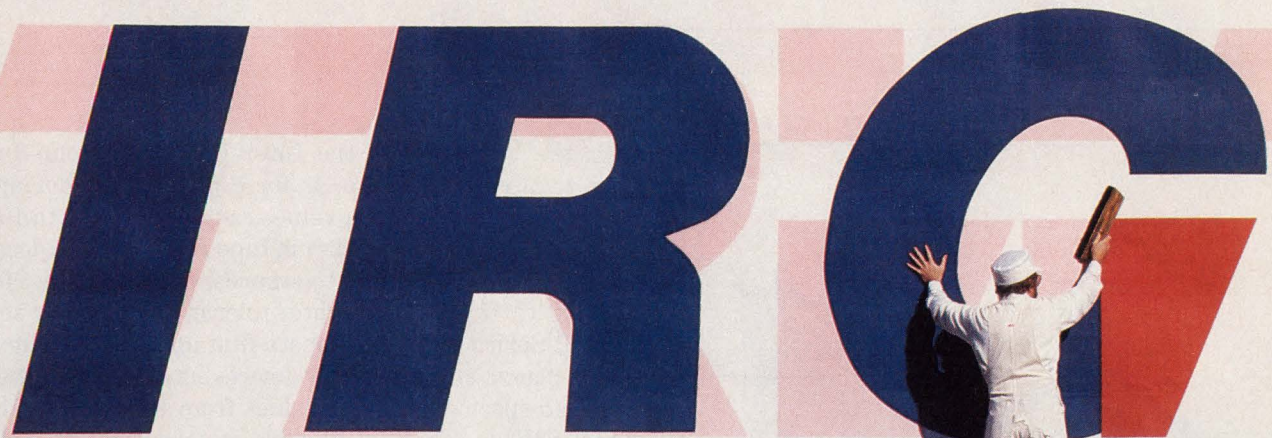
**Fig 4—Henries and farads sometimes don't mix, as these traces show. The voltages in the traces are the result of applying a 200-mA/nsec current front to a standard 10-nF MLC (a), and to a low-inductance chip of the same rating (b). (Courtesy AVX Corp)**

For extremely high frequencies, a line of NP0 chips and leaded units from Murata offers specified Q vs frequency. They come in two sizes: Model MA50 measures 55×55×55 mils, and Model MA60 measures 110×110×100 mils. The devices satisfy the tenets of MIL-C-55681B and come in 50 to 500V ratings. Capacitance values range from 0.3 to 2200 pF. A typical 100-pF device has a Q of 1000 at 100 MHz.

In the lofty gigahertz range, you have recourse to a series of single-layer ceramic capacitors from Dielectric Laboratories Inc. Designed for applications using frequencies from 100 MHz to 40 GHz, these devices come with width/length dimensions ranging from 5 to 60 mils. The chips' electrodes serve as terminations; a nickel-barrier electrode is suitable for soldering, and gold termination is available for die attachment and wire bonding. Voltage ratings are 50 and 100V, and



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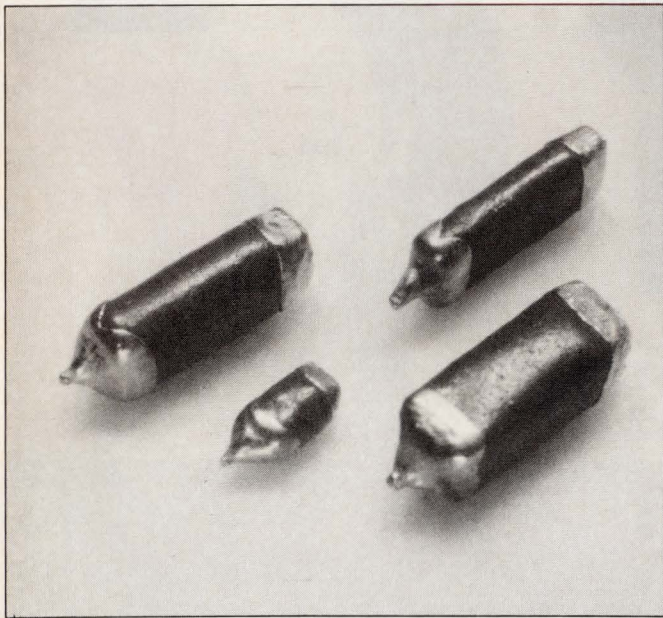


(Formerly TRW Resistive Products Division)

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*Axial-leaded, cylindrical capacitors are compatible with the large installed base of automatic pc-board stuffers.*

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*Suitable for surface-mounting techniques, these solid-tantalum chips from Tansitor Electronics Inc offer you a choice of solder or gold terminations. They're available in six case sizes.*

capacitance values range from 68 to 1500 pF.

Advances in multilayer-ceramic capacitors' CV products and SM-packaging convenience notwithstanding, devices using a metallized-plastic dielectric remain economical and otherwise advantageous in many applications. For example, the film units have a self-healing property—if a punch-through short circuit occurs because of the application of excessive voltage, the short circuit disappears (heals itself) upon removal of the overvoltage condition. Further, many film units are available in the same convenient SM packages offered by MLCs.

Some metallized-polyester capacitors recently introduced by Siemens Corp illustrate the capabilities of film devices. The company's MKT Series B32595 uses a stacked-film construction; the surface-mountable capacitors measure about 7×5.2×3 mm. They're available in 50V ratings ranging from 0.01 to 0.22  $\mu$ F. Offered in 12-mm tape format, the devices cost about \$0.30 (1000). A series of flame-retardant polypropylene-film capacitors from Siemens comes in an axial-leaded, cylindrical format. Model B33074—a \$0.20 (1000), 2200-pF device rated at 100V—operates from -40 to +85°C and finds use as a resonant-circuit capacitor in RF and IF applications.

Identical in size with 2225 multilayer-ceramic capacitors, MKS 01-SMD Series metallized-polyester devices

from the Wima Div of the Inter-Technical Group Inc have totally metallized ends for convenient soldering. The 50V dc units come in values ranging from 10 to 100 nF and are available on 12-mm tape reels. The devices, offered in  $\pm 10$  and  $\pm 20\%$  tolerances, operate from -55 to +100°C. If you need tighter tolerances, consider the FKC22 Series of polycarbonate-film units from Wima. These plastic-encased radial devices have a 5-mm (200-mil) lead spacing and offer values from 100 pF to 0.015  $\mu$ F at 63V dc. They're available in tolerances of  $\pm 10$ ,  $\pm 5$ , and  $\pm 2.5\%$ . Prices for the MSK 01-SMD Series start at \$0.16 (1000); the FKC22 Series begins at \$0.10 (1000).

In addition to the general-purpose bypass, filtering, and resonant-circuit capacitors mentioned so far, you can obtain capacitors that satisfy special requirements. A couple of examples are a line of high-temperature devices from Corning Glass Works and some units having a deliberately inserted series resistance from the Rifa Div of World Products Inc.

Corning's high-temperature glass-dielectric capacitors come in axial- and radial-leaded cases; these units are suitable for oil-well logging systems, semiconductor burn-in testing, geophysical probes, and other harsh-environment applications. One series, dubbed "Glass-K," operates over -75 to +200°C and offers values ranging from 270 pF to 0.1  $\mu$ F. According to curves in the data sheets, the devices offer three temperature characteristics; the three types lose about 20, 30, and 40% of their 25°C value at 200°C. Other high-temperature devices from Corning offer values ranging from 0.5 to 10,000 pF and operate from -60 to +200°C. These devices have a capacitance change of +4% at 200°C.

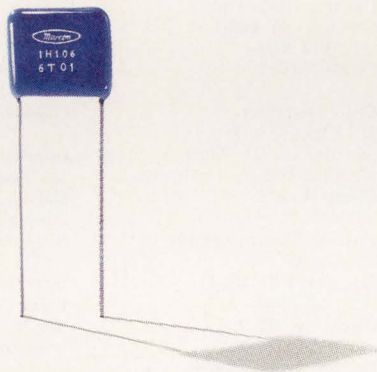
Finally, a series of metallized-paper capacitors from Rifa incorporates a series resistance for transient suppression in various applications. The PMR209 Series is available in capacitance values from 0.047 to 0.47  $\mu$ F and incorporates a 47 or 100 $\Omega$  resistor, according to your choice. The units are rated at 630V dc, 250V ac. Another line, the PMR210 family, is designed for click suppression; these units come in values ranging from 0.022 to 0.1  $\mu$ F, and they incorporate a 100 $\Omega$  series resistance. Prices for the PMR209 and PMR210 units start at \$0.63 and \$0.73 (OEM qty), respectively. **EDN**

*Manufacturers box begins on pg 130*

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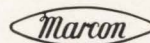
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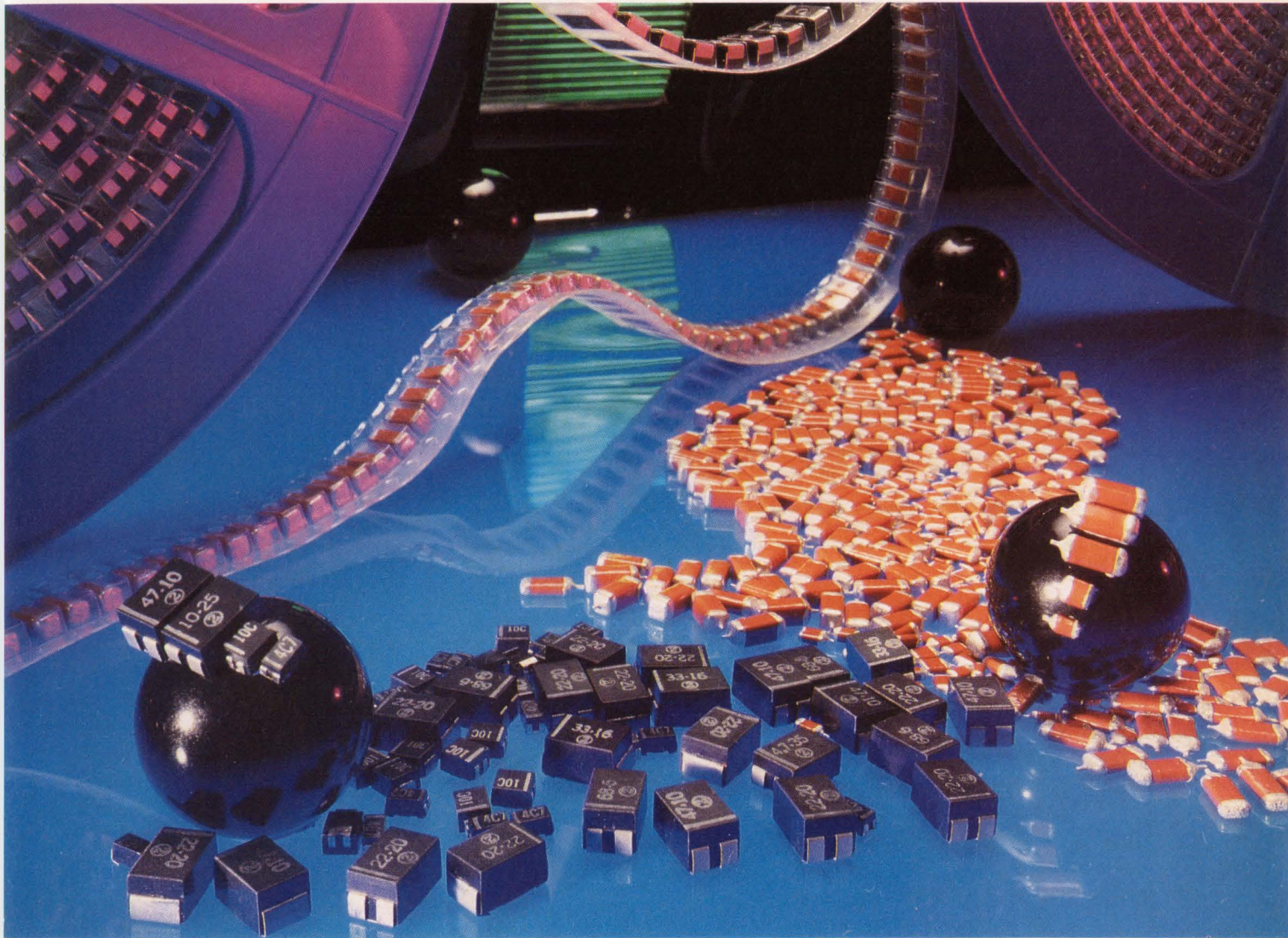
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(Continued on pg 132)

# SMT STANDARDS.



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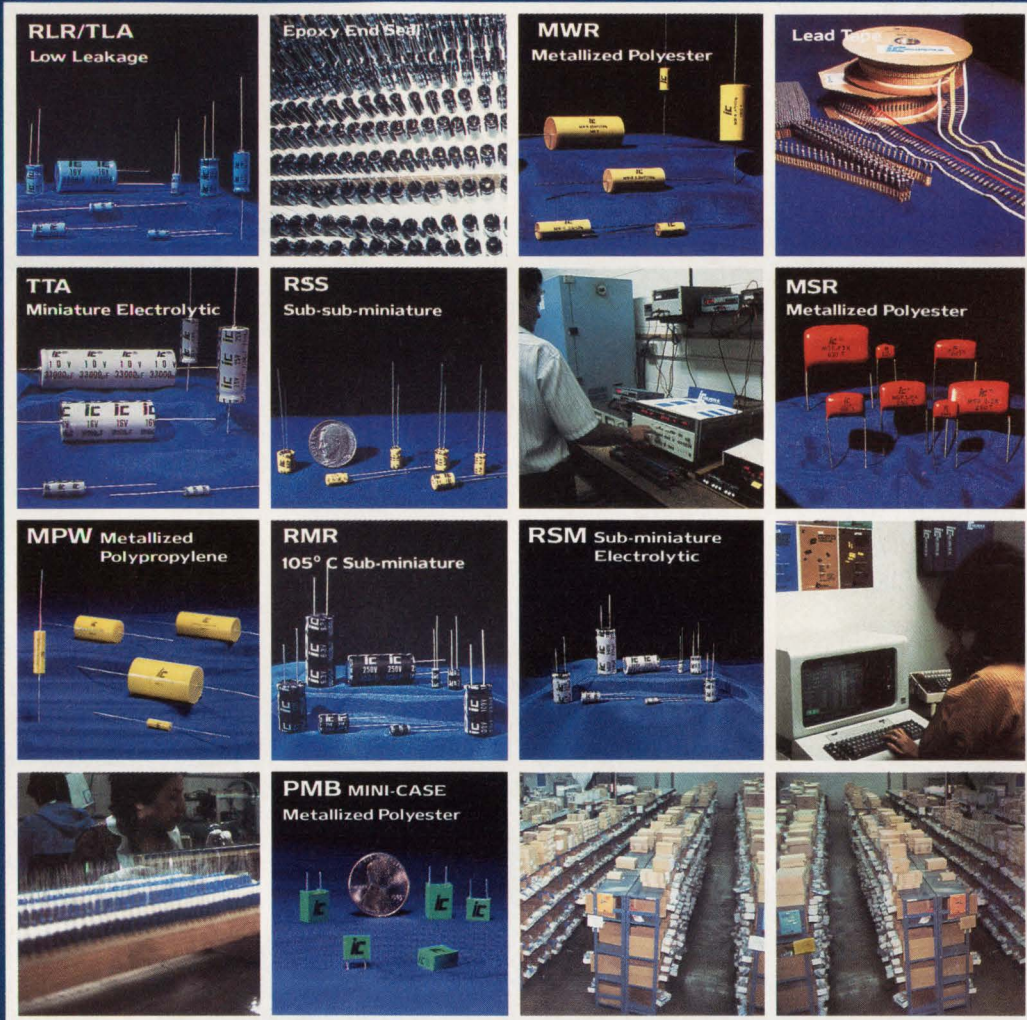
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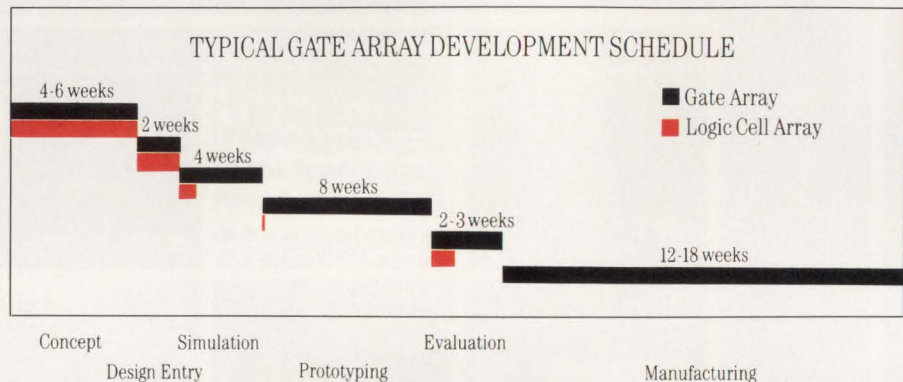
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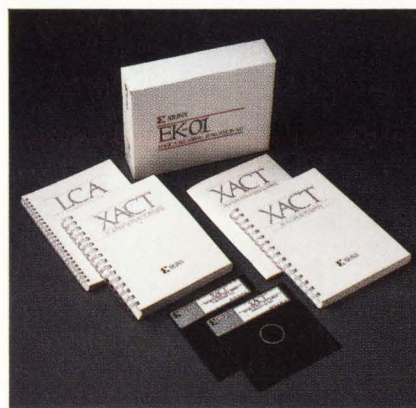
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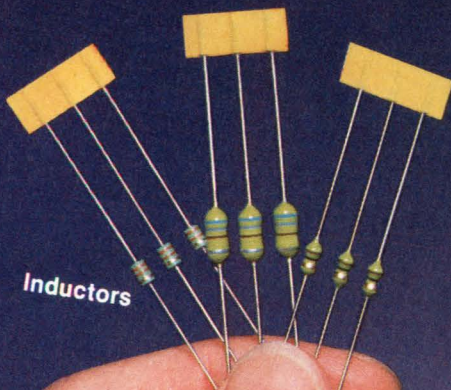
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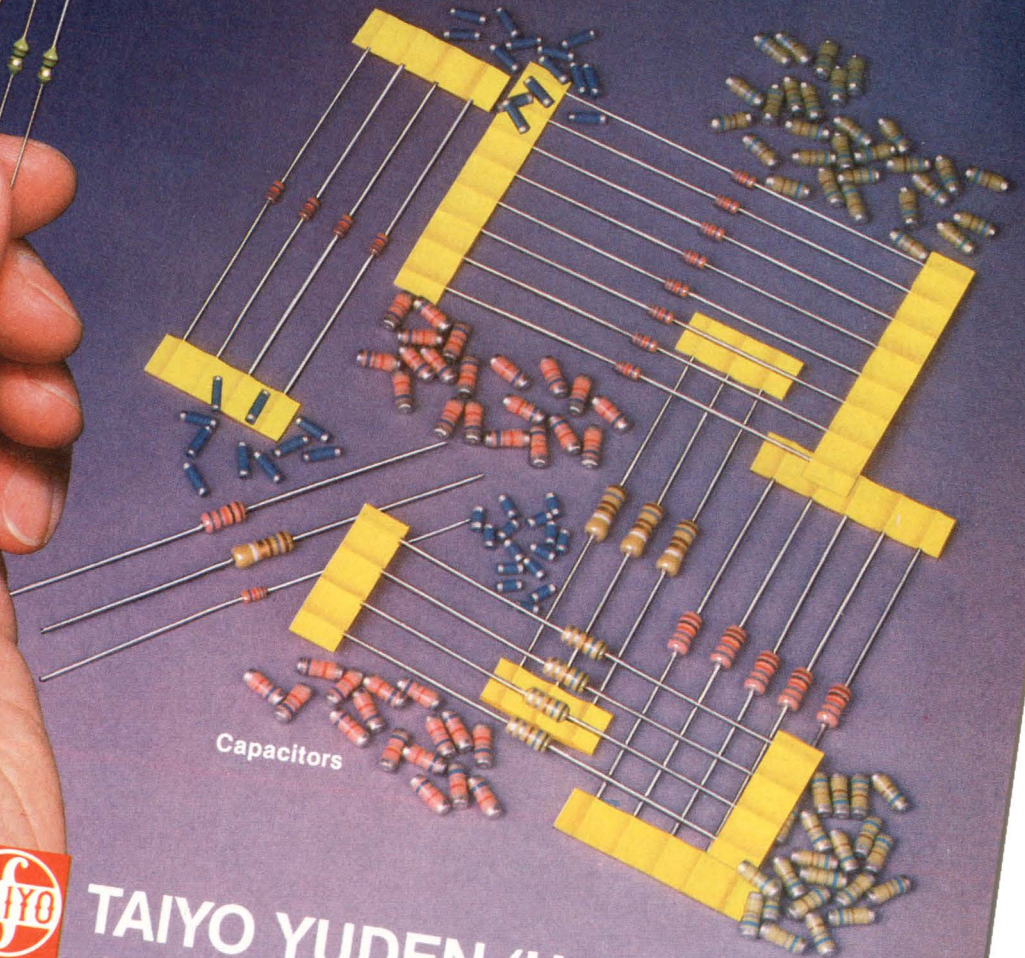
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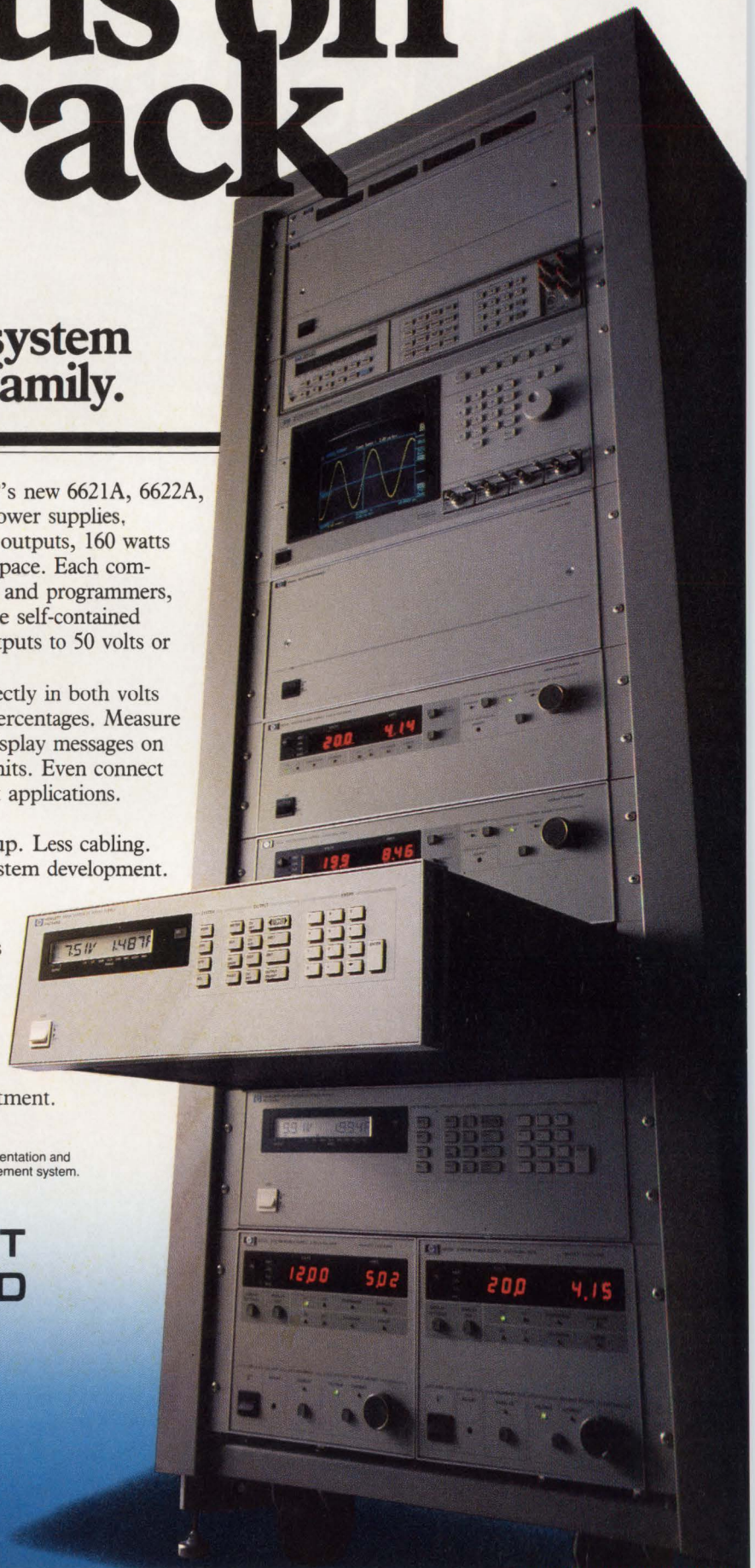
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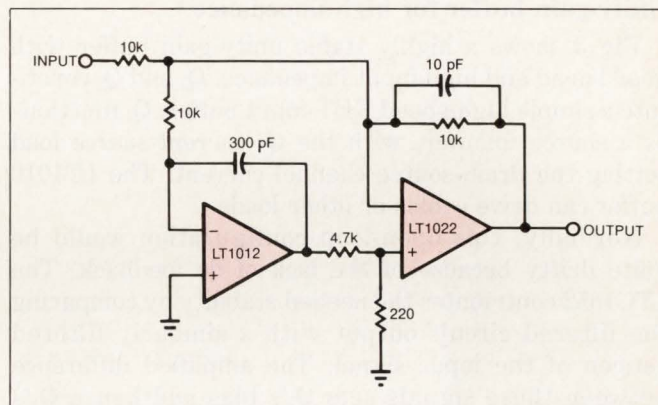
# Composite amplifiers yield high speed and low offset

*You can find an op-amp technology that excels in any one performance area, but today's applications often demand high performance in several areas. You must therefore employ some ingenious circuit-design techniques to circumvent the limitations.*

Jim Williams, *Linear Technology Corp*

Amplifier design is a study in compromise: A single device can't achieve optimal speed, drift, bias-current, noise, and output-power specs. Various families emphasizing one or more of these areas have evolved, but you might find that your application requires performance figures that can only be obtained with dedicated designs. If a single device can't provide the desired characteristics (high speed and dc precision, for example), you can configure a composite amplifier to do the job. Composite designs combine the best features of two or more amplifiers to achieve a level of performance unobtainable in a single device.

Fig 1 shows a composite amplifier made up of an LT1012 low-drift device and an LT1022 high-speed device. The overall circuit is a unity-gain inverter whose summing node is located at the junction of the three 10-k $\Omega$  resistors. The LT1012 monitors this summing node, compares it to ground, and drives the



**Fig 1**—This composite circuit combines low-drift and high-gain devices to form a unity-gain inverter. The LT1022 handles high-frequency inputs, while the LT1012 stabilizes the dc operating point.

LT1022's positive input, completing a dc-stabilizing loop around the LT1022. The 10-k $\Omega$ /300-pF network allows the LT1012 to respond only to low-frequency signals; the LT1022 handles high-frequency inputs while the LT1012 stabilizes the dc operating point.

The 4.7-k $\Omega$ /220 $\Omega$  divider at the noninverting input of the LT1022 prevents excessive input overdrive during start-up. The circuit's performance combines the LT1012's 35- $\mu$ V offset and 1.5V/ $^{\circ}$ C drift with the LT1022's 23V/ $\mu$ sec slew rate and 300-kHz full-power bandwidth. The bias current is approximately 100 pA.

Fig 2's circuit is similar to Fig 1's, but the former employs discrete FETs to more than triple the speed. In the circuit, IC<sub>1</sub>'s inputs are tied to the negative rail,

thereby turning IC<sub>1</sub>'s input stage off. The differentially connected FETs bias the second stage via IC<sub>1</sub>'s offset pins. This connection replaces IC<sub>1</sub>'s input stage, reducing bias current and increasing speed.

FET mismatch would normally result in excessive offset and drift, but IC<sub>2</sub> corrects this problem by monitoring the summing point (the junction of the two 4.7-k $\Omega$  resistors) and forcing Q<sub>2</sub>'s gate to eliminate the overall offset. The 10-k $\Omega$ /1000-pF network inhibits IC<sub>2</sub>'s response to low frequencies, and the 1-k $\Omega$  divider chain prevents overdrive to Q<sub>2</sub> on start-up. The 1-k $\Omega$ /10-pF damper network at the summing node helps ensure high-frequency stability. Fig 2b shows the pulse response; trace A is the input, and trace B is the output.

The slew rate exceeds 100V/ $\mu$ sec with clean damping. The full-power bandwidth is about 1 MHz, and the input bias current is approximately 100 pA. DC offset and drift specs are similar to those of the Fig 1 circuit.

#### Unity-gain buffer for high impedance

Fig 3 shows a highly stable unity-gain buffer with good speed and high input impedance. Q<sub>1</sub> and Q<sub>2</sub> constitute a simple high-speed FET-input buffer. Q<sub>1</sub> functions as a source follower, with the Q<sub>2</sub> current-source load setting the drain-source channel current. The LT1010 buffer can drive cables or other loads.

Normally, this open-loop configuration would be quite drifty because of the lack of dc feedback. The LTC1052 contributes the needed stability by comparing the filtered circuit output with a similarly filtered version of the input signal. The amplified difference between these signals sets Q<sub>2</sub>'s bias and hence Q<sub>1</sub>'s channel current, which in turn forces Q<sub>1</sub>'s V<sub>GS</sub> to the level required to match the circuit's input and output potentials. The 2000-pF capacitor at IC<sub>1</sub> provides stable loop compensation. The RC network at IC<sub>1</sub>'s output prevents that output from seeing high-speed edges coupled through Q<sub>2</sub>'s collector-base junction. IC<sub>2</sub>'s output is also fed back to the shield around Q<sub>1</sub>'s gate lead, bootstrapping the circuit's effective input capacitance down to less than 1 pF.

The LT1010's 15-MHz bandwidth and 100V/ $\mu$ sec slew rate, combined with its 150-mA output capability, ensure that the circuit in Fig 3a is fast enough for most applications. For applications requiring very fast performance, the alternate discrete-component buffer in Fig 3b should prove useful. Although its output is current-limited at 75 mA, the gigahertz-range transistors that the buffer employs provide an exceptionally wide bandwidth, fast slewing, and very little delay. Fig

3c shows the LTC1052-stabilized buffer circuit's response using the discrete stage: The response is clean and quick; the delay is less than 4 nsec; the slew rate exceeds 2000V/ $\mu$ sec; and the full-power bandwidth approaches 50 MHz. Note in Fig 3c that the rise time is limited by the pulse generator, not by the circuit. The offset, with or without the discrete-component stage, is set at 5  $\mu$ V by the LTC1052; the gain is about 0.95.

This last spec points out a factor that could lead to potential difficulty with the Fig 3 circuits: The gain is not quite unity. The circuit in Fig 4 maintains a high speed and low bias current while achieving a true unity-gain transfer function.

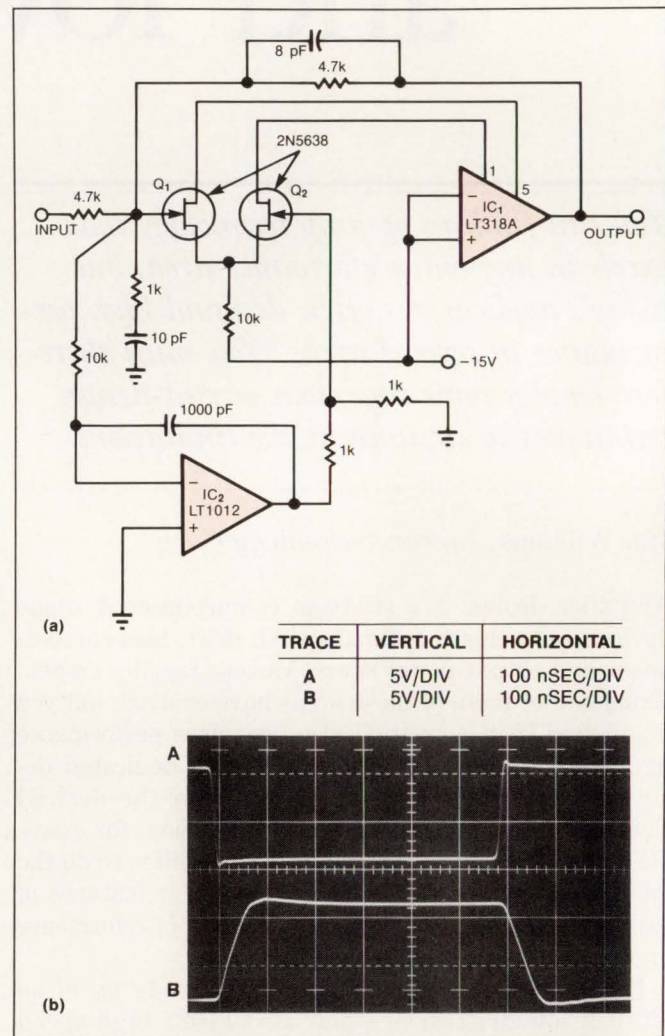


Fig 2—Otherwise similar to the Fig 1 circuit, this composite amplifier (a) employs discrete FETs to achieve a threefold speed improvement. The scope photo (b) illustrates the circuit's pulse response.

The use of discrete FETs can effect a three-fold improvement in a composite amplifier's speed.

In Fig 4's circuit, IC<sub>2</sub> provides dc stability for the I/O path, and IC<sub>1</sub> provides drive capability. Feedback is to Q<sub>2</sub>'s emitter from IC<sub>1</sub>'s output. The 1-k $\Omega$  adjustment allows precise setting of the gain to unity. With the LT1010 serving as the final output stage, the slew rate is 100V/ $\mu$ sec and the full-power bandwidth (1V p-p) is 10 MHz. The -3-dB bandwidth exceeds 35 MHz. For a gain of A=10 (that is, when the 1-k $\Omega$  variable resistor is set at 50 $\Omega$ ), the full-power bandwidth remains at 10 MHz, but the -3-dB bandwidth falls to 22 MHz.

If you include the optional discrete stage, the slew rate exceeds 1000V/ $\mu$ sec, the full-power bandwidth extends to 18 MHz, and the -3-dB bandwidth reaches 58 MHz. For A=10, full power is available to 10 MHz; the -3-dB point becomes 36 MHz. In Fig 4c, traces A

and B show the input and output without the discrete stage; traces C and D show the input and output with the discrete stage. With or without the discrete stage, the circuit should be more than adequate for driving video cables or data converters; the LT1012 maintains dc stability under all conditions.

### Fast amplifier delivers 1V p-p

Fig 5 shows another dc-stabilized fast amplifier that functions over a wide range of gains (typically from 1 to 10). It combines the LT1010 and a fast discrete stage within LT1008-based stabilizing loop. Q<sub>1</sub> and Q<sub>2</sub> form a differential stage that provides a single-ended input into the LT1010. The circuit delivers 1V p-p into a typical 75 $\Omega$  video load. At A=2, the gain is within 0.5

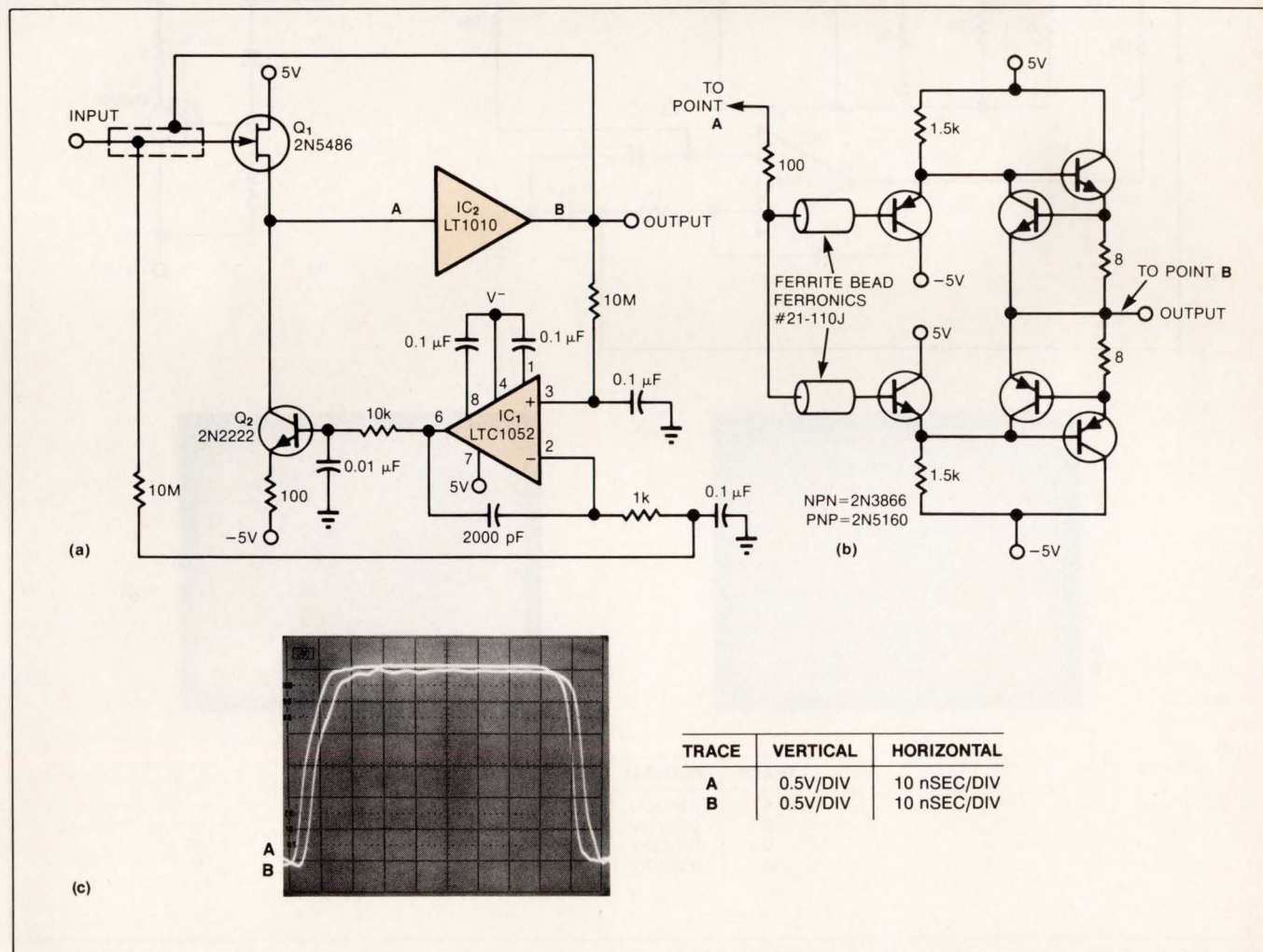
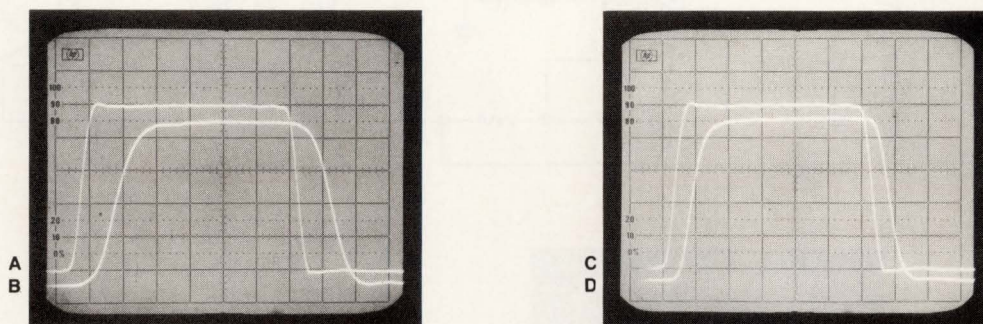
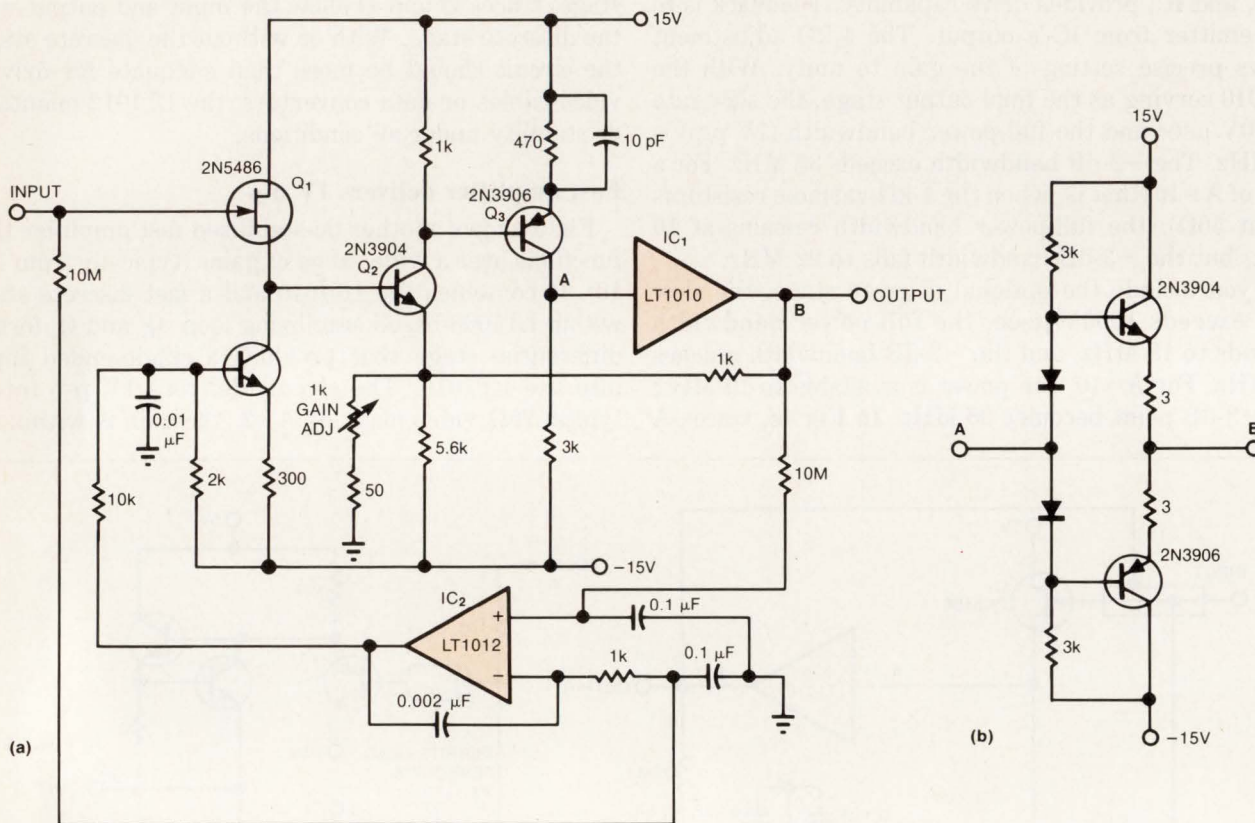


Fig 3—A FET input stage ensures high input impedance for this not-quite-unity-gain buffer (a). The LTC1052 contributes stability. A discrete-component output stage (b) increases the circuit's already impressive speed. The response is clean and quick (c).

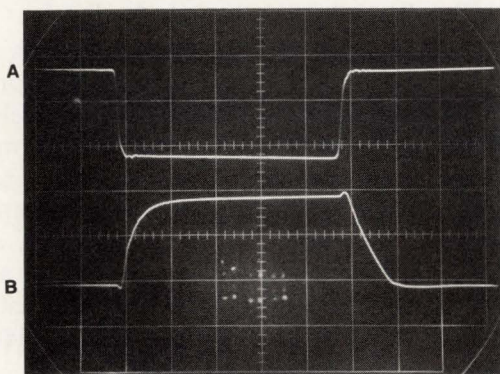
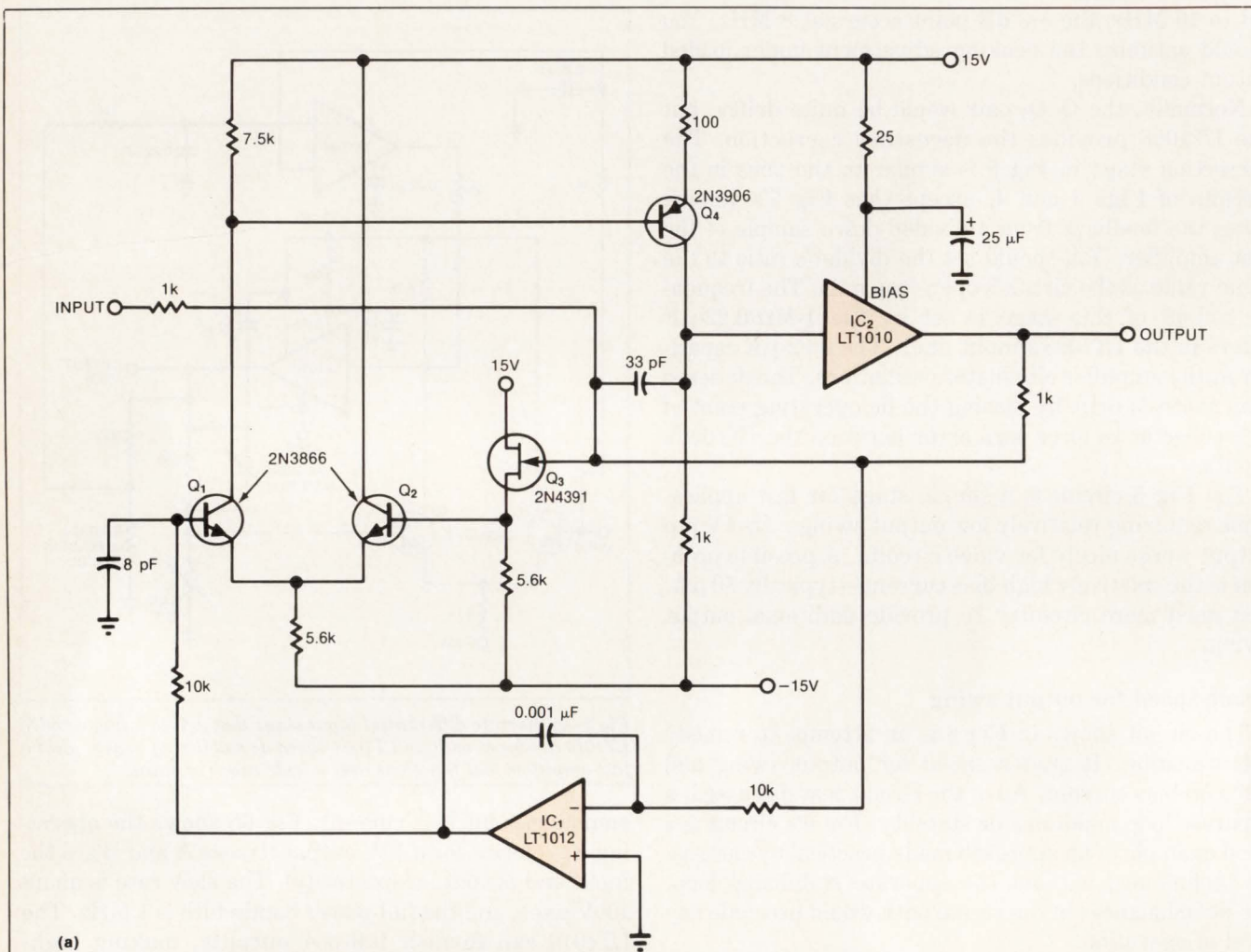


TRACE	VERTICAL	HORIZONTAL
A	0.2V/DIV	10 nSEC/DIV
B	0.2V/DIV	10 nSEC/DIV
C	0.2V/DIV	10 nSEC/DIV
D	0.2V/DIV	10 nSEC/DIV

**Fig 4**—This circuit (a) is somewhat similar to Fig 3's, but it has the additional advantage of achieving a true unity-gain transfer function. The optional discrete stage (b) extends the full-power bandwidth from 10 to 18 MHz. In the scope photos (c), traces A and B show the input and output without the discrete stage; traces C and D show the input and output with the discrete stage.







TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	100 nSEC/DIV
B	5V/DIV	100 nSEC/DIV

**Fig 6**—This circuit (a) offers wide output swing and low bias current, but it sacrifices speed. The photo (b) shows the response (trace B) to a pulse input (trace A).

*A current-mode feedback arrangement allows a circuit to maintain a fixed bandwidth over a wide range of closed-loop gain.*

complementary voltage gain to IC<sub>2</sub>, which provides the circuit's output. The feedback is from IC<sub>2</sub>'s output to IC<sub>1</sub>'s output, which is a low-impedance point.

#### Skewing ensures adequate loop capture

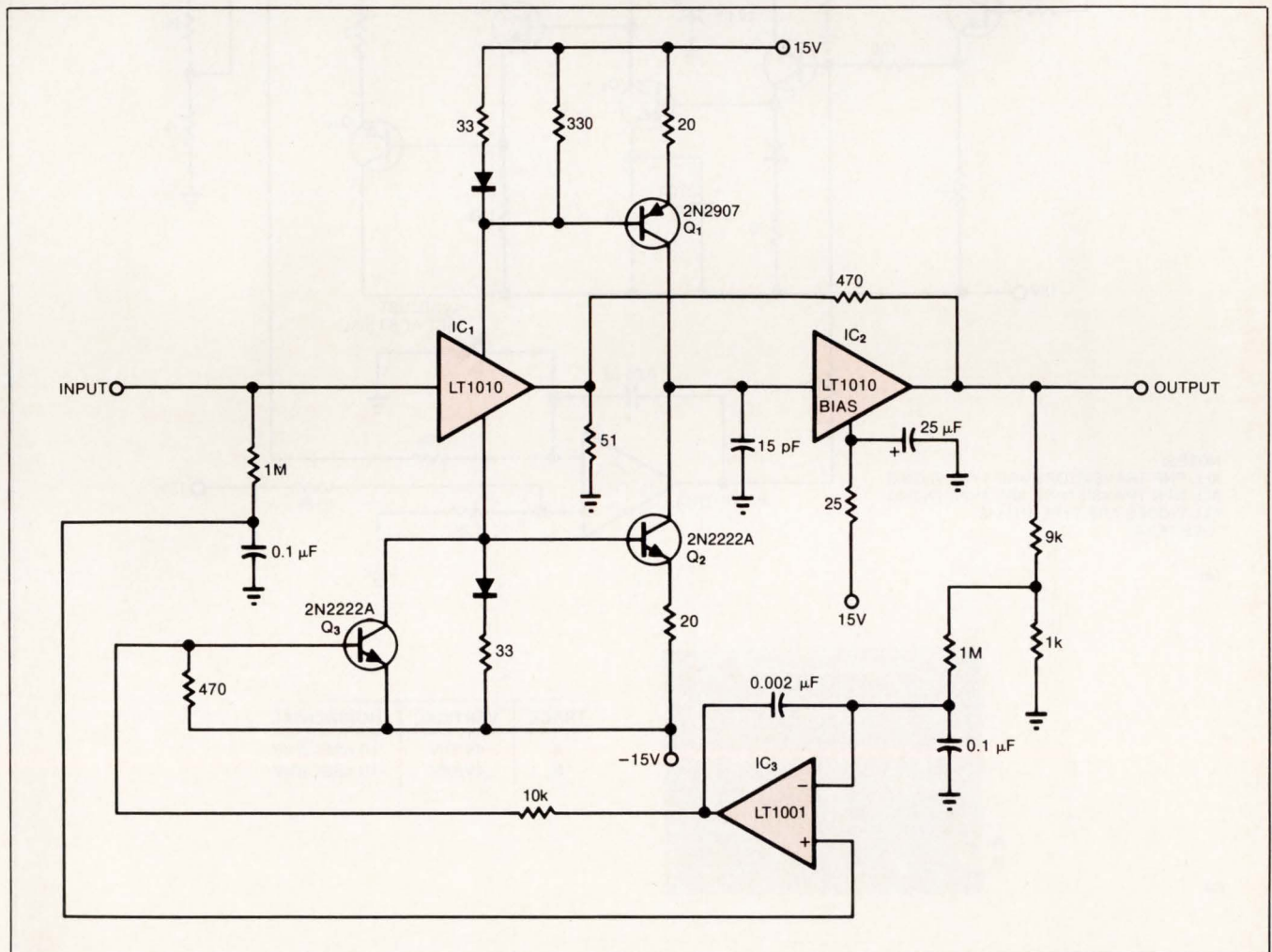
IC<sub>3</sub>'s stabilizing loop compensates large offsets in the signal path, which are dominated by a mismatch in Q<sub>1</sub> and Q<sub>2</sub>. Q<sub>3</sub> shunts Q<sub>2</sub>'s base bias resistor to correct for these offsets. Deliberate skewing of Q<sub>1</sub>'s operating point by the 330Ω resistor ensures an adequate loop capture range. The 9-kΩ/1-kΩ divider network that provides feedback to IC<sub>3</sub> determines the gain ratio of the circuit—in this case 10.

The feedback scheme makes IC<sub>1</sub>'s output look like the negative input of the amplifier, with the closed-loop

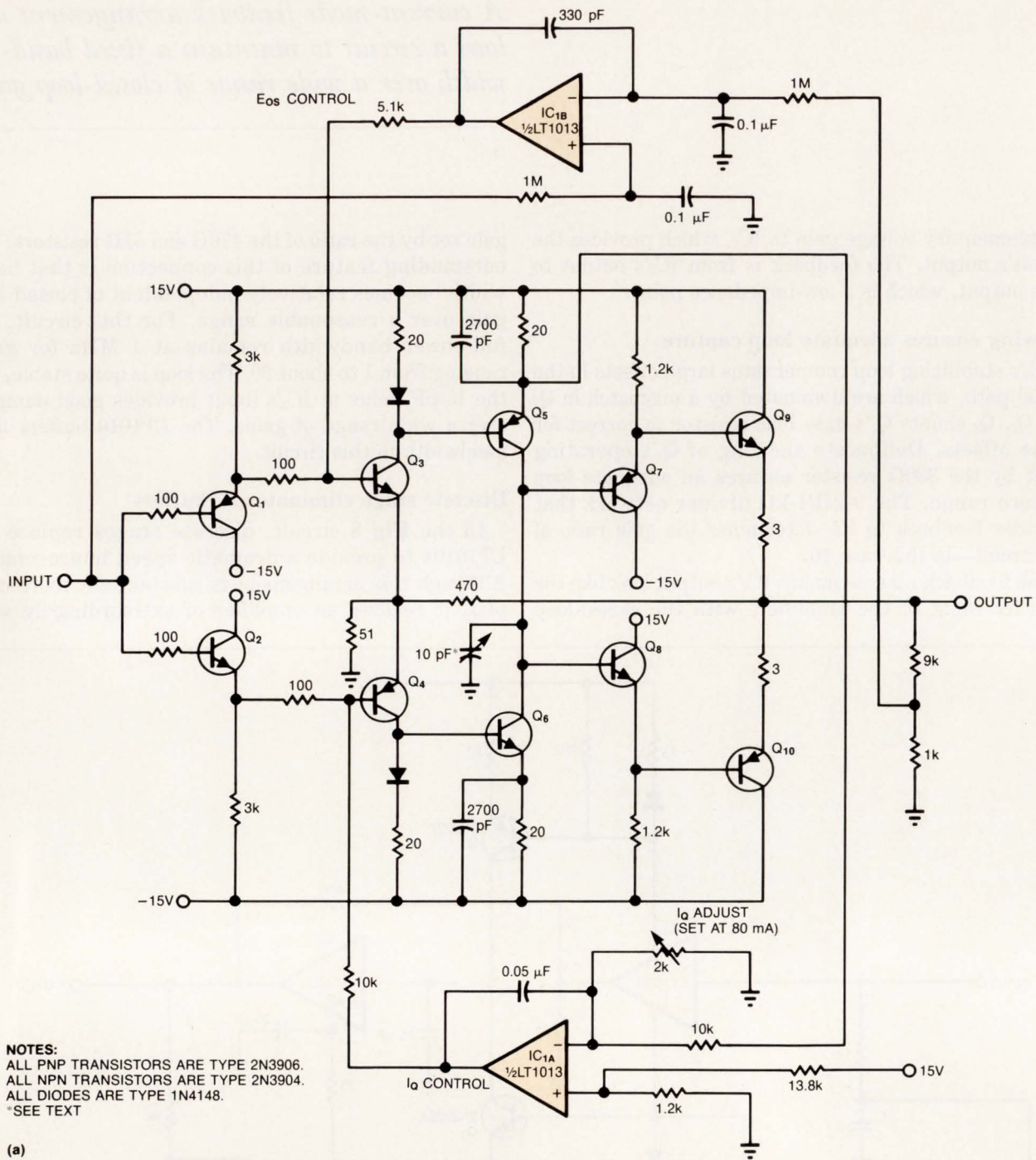
gain set by the ratio of the 470Ω and 51Ω resistors. The outstanding feature of this connection is that bandwidth becomes relatively independent of closed-loop gain over a reasonable range. For this circuit, the full-power bandwidth remains at 1 MHz for gains ranging from 1 to about 20. The loop is quite stable, and the 15-pF value at IC<sub>2</sub>'s input provides good damping over a wide range of gains. The LT1010 buffers limit bandwidth in this circuit.

#### Discrete stage eliminates IC buffers

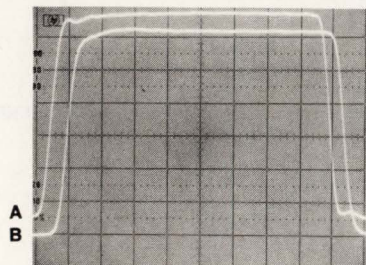
In the Fig 8 circuit, discrete stages replace the LT1010s to provide a dramatic speed improvement. Although this arrangement is substantially more complex, it realizes an amplifier of extraordinarily wide



**Fig 7**—This noninverting amplifier circuit employs current-mode feedback, which allows it to offer a 1-MHz full-power bandwidth for gains ranging from 1 to about 20.



(a)



(b)

TRACE	VERTICAL	HORIZONTAL
A	4V/DIV	10 nSEC/DIV
B	4V/DIV	10 nSEC/DIV

**Fig 8—Discrete transistors replace the LT1010 buffers in this variation (a) of the circuit shown in Fig 7. In response to a pulse input, a  $\pm 12V$  pulse output exhibits only about 6 nsec of delay (b).**

*Improvement in speed and offset specs constitutes the most common reason for employing composite techniques, but circuits excelling in other areas are also possible.*

bandwidth. This composite design comprises three amplifiers: the discrete wideband stage, a quiescent current-control amplifier, and an offset servo.  $Q_1$  through  $Q_4$  replace Fig 7's  $IC_1$ , although a complementary voltage gain is taken at the collectors of  $Q_3$  and  $Q_4$ .  $Q_5$  and  $Q_6$  provide additional gain, as do  $Q_1$  and  $Q_2$  in Fig 7's circuit.  $Q_7$  through  $Q_{10}$  form the output-buffer stage.

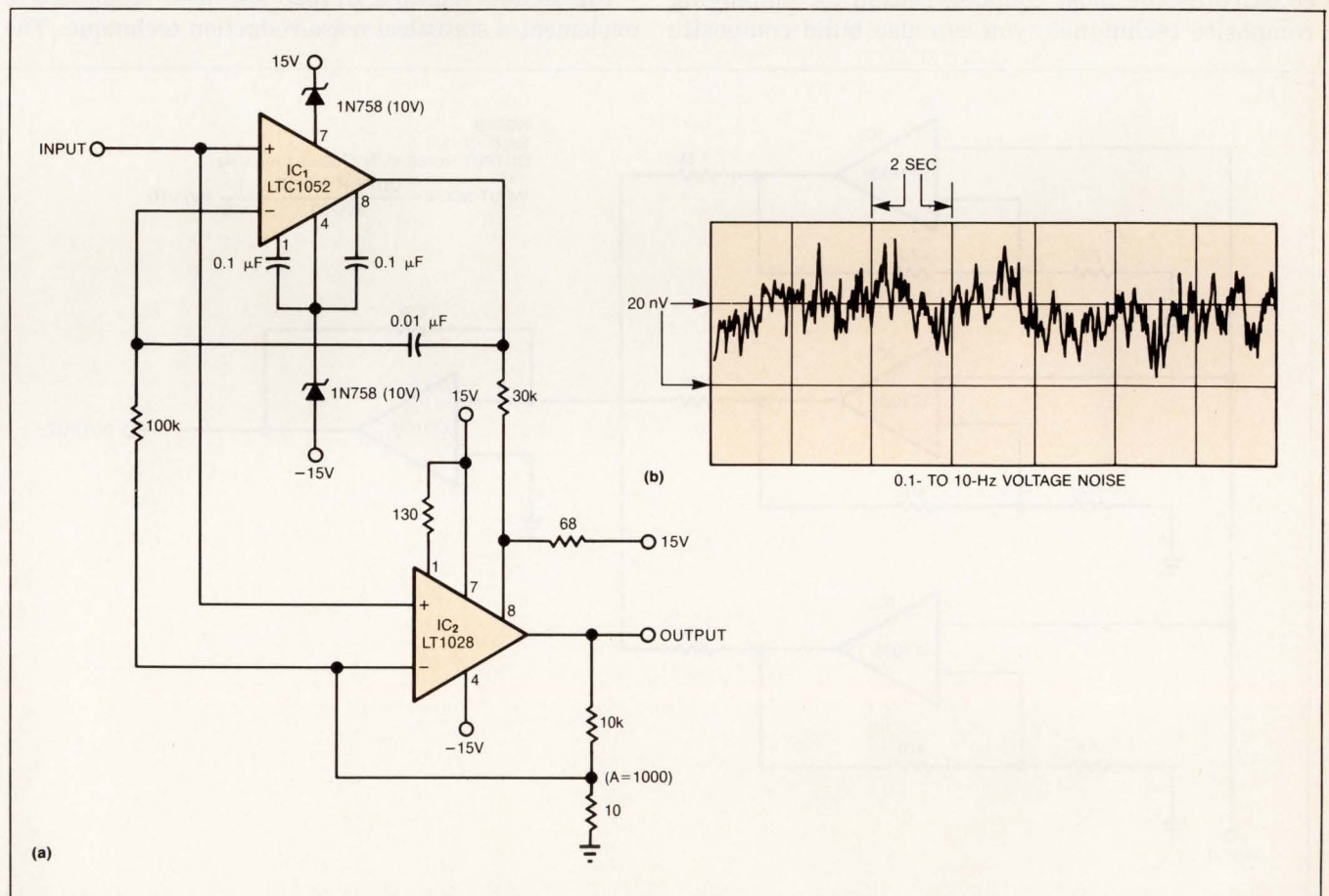
The feedback scheme is identical to Fig 7's, with summing action occurring at the  $Q_3$ - $Q_4$  emitter connection. To obtain the maximum bandwidth, the circuit must maintain a high quiescent current. Without closed-loop control, the circuit would quickly go into thermal runaway and destroy itself.  $IC_{1A}$  provides the required servo control of the quiescent current by sampling a resistively divided version of the voltage across  $Q_5$ 's emitter resistor and comparing it to a reference derived from the power supply.  $IC_{1A}$ 's output biases  $Q_4$ , completing a loop that forces fixed current

through  $Q_5$ . This action effectively controls overall quiescent current in the discrete stage.

Simultaneously,  $IC_{1B}$  corrects for offset by forcing  $Q_3$ 's base to equalize the dc input and output values at the discrete stage. Because the closed-loop gain is set at 10 (by the  $470\Omega$  and  $51\Omega$  resistors),  $IC_{1B}$  samples the output via the 10:1 divider. Both  $IC_{1A}$  and  $IC_{1B}$  have local roll-off, attenuating their response to high frequencies. Casual consideration of  $IC_{1A}$ 's and  $IC_{1B}$ 's operation might raise concern about interaction, but detailed analysis shows that the offset and quiescent-current loops do not influence each other's operation.

#### -3-dB bandwidth extends beyond 110 MHz

When this circuit is constructed using high-frequency layout techniques and a ground plane, the performance is quite impressive. For gains ranging from 1 to 20, the



**Fig 9—Composite amplifiers aren't limited** to combinations of low-offset and high-speed stages. This circuit (a) offers low noise performance (b) as well as low drift.

You can build a circuit that uses a composite of paralleled buffers to create a simple high-current stage.

full-power bandwidth remains at 25 MHz, and the -3-dB point extends beyond 110 MHz. The slew rate exceeds 3000V/ $\mu$ sec. The use of RF transistors can improve these specs, although the transistors shown are inexpensive. Fig 8b shows the circuit's  $\pm 12$ V output (trace B) in response to a pulse input (trace A) for a circuit gain of 10. The delay is about 6 nsec; the rise time is limited by the input pulse generator. The 10-pF trimmer at the  $Q_5$ - $Q_6$  connection optimizes damping.

To use this circuit, adjust the  $I_Q$  level to 80 mA immediately after turn-on. Next, set  $IC_{1B}$ 's input resistor divider to a ratio appropriate to the closed-loop circuit gain. Finally, adjust the 10-pF trimmer for the best response. Note that, in the interest of achieving high speeds, this circuit has no output protection.

#### Composites cut drift and noise

Although improvement in speed and offset specs constitutes the most common reason for employing composite techniques, you can also build composite

circuits that excel in other areas. For example, Fig 9 shows a combination of a low-drift chopper-stabilized amplifier and an ultralow-noise bipolar amplifier. In the circuit, the LTC1052 measures the dc error at the LT1028's input terminals and biases its offset pins to force the offset to a few microvolts. The IN758 zener diodes allow the LTC1052 to function from  $\pm 15$ V rails. The offset-pin biasing at the LT1028 is arranged so that the LTC1052 will always be able to find a servo point. The 0.01- $\mu$ F capacitor rolls off the LTC1052 at a low frequency, and the LT1028 handles the high-frequency signals. The combined characteristics of the amplifiers yield the following performance:

- Offset voltage = 5  $\mu$ V max
- Offset drift = 50 nV/ $^{\circ}$ C max
- Noise = 1.1 nV/ $\sqrt{\text{Hz}}$  max.

Fig 9b plots the noise amplitude over time within a 0.1- to 10-Hz bandwidth.

Fig 10 uses multiple LT1028 low-noise amplifiers to implement a statistical noise-reduction technique. The

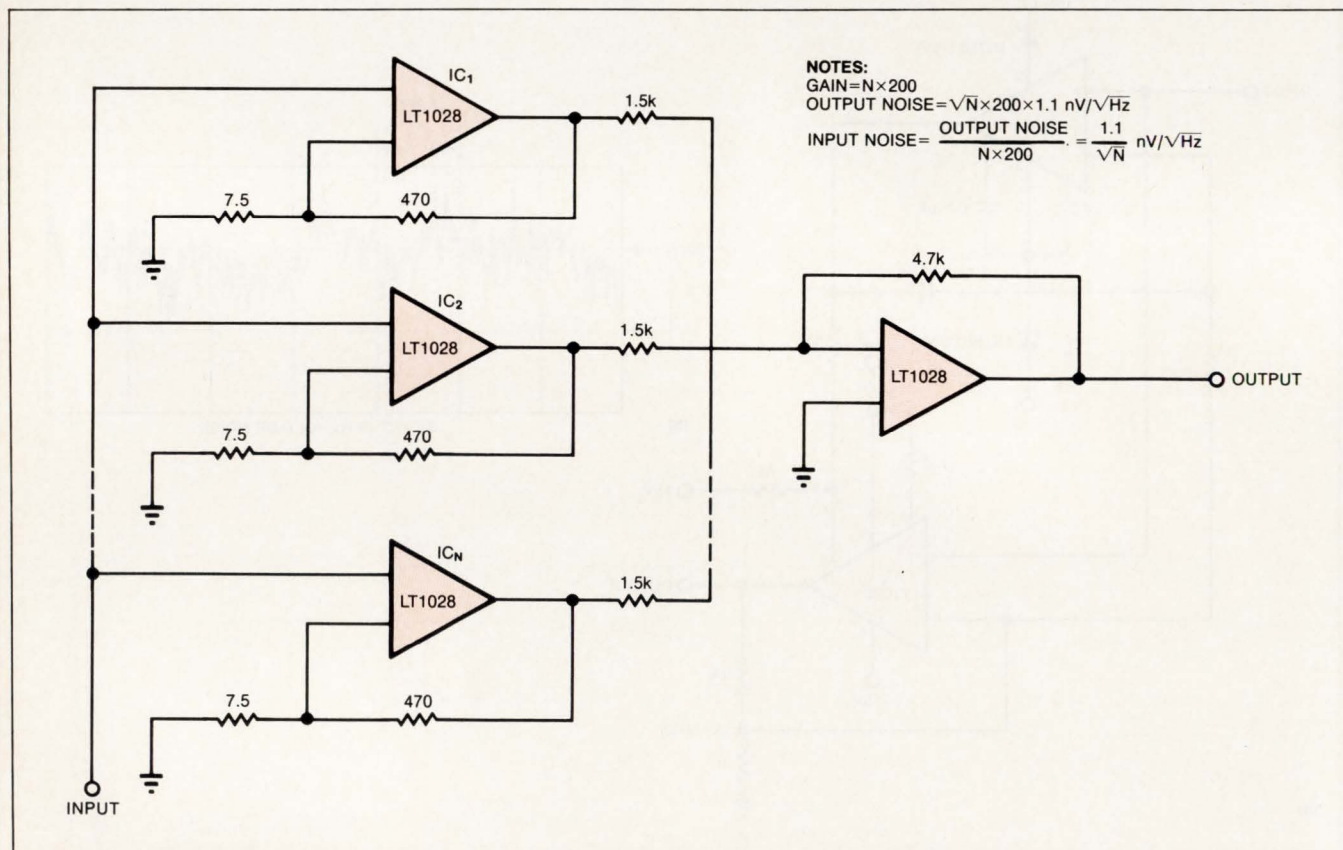
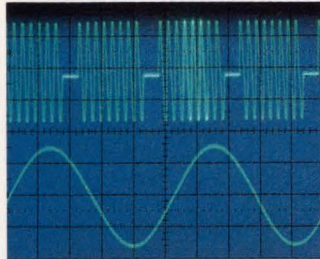
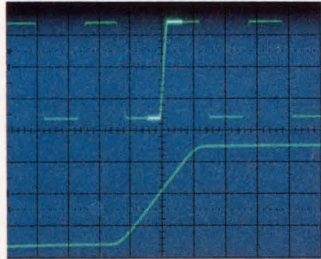


Fig 10—This multiple-amplifier design makes use of a statistical technique to reduce noise. The decrease in noise is proportional to the  $\sqrt{N}$ , where  $N$  is the number of devices in parallel.

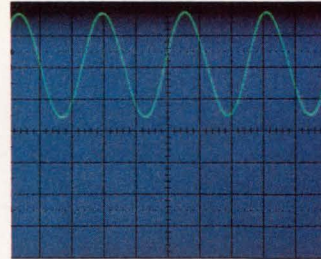
# NOW GET SCOPE, COUNTER AND DMM INPUT ALL AT ONCE THROUGH ONE PROBE!



**Gated frequency measurement.** B sweep triggering during the intensified portion of the A sweep. Intensified portion frequency is measured with the counter/timer/DMM.



**Delay time measurement.** Delay time from the start of A sweep to the start of the B sweep is measured with crystal accuracy.



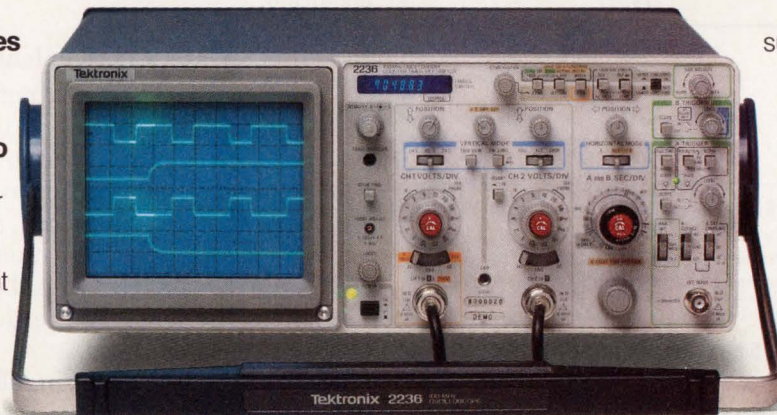
**Channel 1 dc volts measurement.** The average dc component of a waveform is measured directly through channel 1 with direct digital fluorescent readout.

The Tek 2236 combines 100 MHz, dual timebase scope capability with counter/timer/DMM functions integrated into its vertical, horizontal and trigger systems. For the same effort it takes to display a waveform you can obtain digital readout of frequency, period, width, totalized events, delay time and  $\Delta$ -time to accuracies of 0.001%.

The same probe is used to provide input for the CRT display and the digital measurement system, resulting in easy set-up, greater measurement confidence and reduced circuit loading. Probe tip volts can also be measured through the Ch 1 input.

### Precision measurements at the touch of a button.

Auto-ranging frequency, period, width and gated measurements are push-button-simple. And the 2236 offers an independent floating 5000 count, auto-ranging multimeter with side inputs for DC voltage mea-



surements to 0.1%.

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**The 2236: scope, counter, timer, DMM plus a 3-year warranty —all for just \$2,650.**

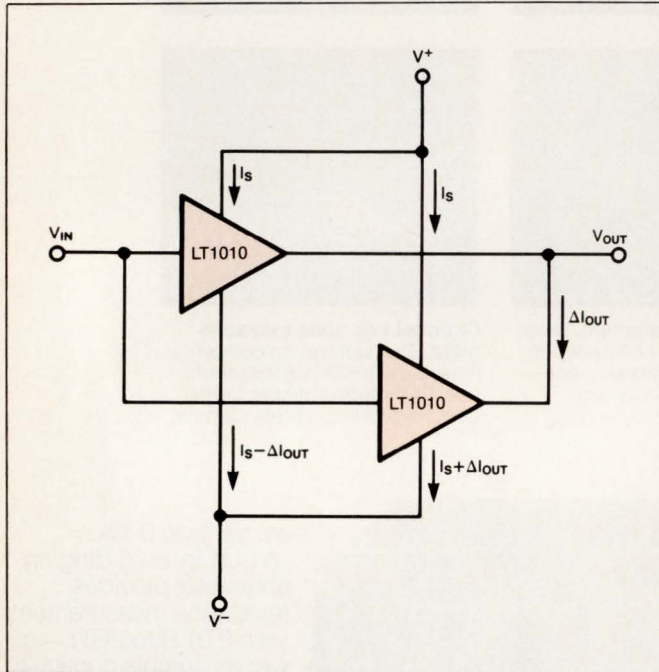
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Bandwidth	100 MHz
No of Channels	2 + Trig. View
Max. Sweep Speed	5 ns/div
Digital Readout Features	Direct Ch 1 Voltage Meas. 0.5% DC; 2.0% AC RMS Resistance: .01 $\Omega$ to 200 Meg $\Omega$ Continuity/Temp: Audible/C $^{\circ}$ or F $^{\circ}$ Totalizing Counter: — 1 counts to 8,000,000 Direct Freq. Meas: 100 MHz to 0.001% acc. Period, Width Meas: 10 ns with 10 ps max. resolution
Timing Meas. Accuracy	.001% (delay and $\Delta$ -time with readout)
Trigger Modes	P-P Auto, Norm, TV Field, TV Line, Single Sweep
Weight	7.3 kg (16.2 lb)
Price	\$2650
Warranty	3-year including CRT (plus optional service plans to 5 years)

*Parallel connection might require some increased attention to heat sinking.*



**Fig 11—Paralleled LT1010 buffers** create a simple high-current stage. You can parallel any number of LT1010s as long as you take into account the increased dissipation within individual units that results from mismatches in output resistance and offset voltage.

circuit is based on the fact that noise changes in inverse proportion to the  $\sqrt{N}$ , where  $N$  is the number of devices in parallel. For example, for nine amplifiers in parallel, the noise would decrease by a factor of three, to about 0.33 nV/ $\sqrt{\text{Hz}}$  at 1 kHz. A potential difficulty is that, with such a configuration, the input-current noise increases with  $\sqrt{N}$ .

#### Paralleled buffers increase drive

A final circuit, shown in Fig 11, uses a composite of paralleled LT1010 buffers to create a simple, high-current stage. Parallel operation provides reduced output impedance, more drive capability, and improved frequency response under load. You can directly parallel any number of LT1010s as long as you take into account the increased dissipation in individual units caused by mismatches of output resistance and offset voltage.

When the inputs and outputs of two buffers are connected together, a current ( $\Delta I_{\text{OUT}}$ ) flows between the outputs:

$$\Delta I_{\text{OUT}} = \frac{V_{\text{OS1}} - V_{\text{OS2}}}{R_{\text{OUT1}} + R_{\text{OUT2}}}$$

where  $V_{\text{OS}}$  and  $R_{\text{OUT}}$  are the offset voltages and output resistances of the respective buffers.

Normally, the negative supply current of one unit will increase and that of the other unit will decrease, with the positive supply current staying the same. You may assume that the worst-case increase in standby dissipation (that is, when  $V_{\text{IN}}$  approaches  $V^+$ ) is  $\Delta I_{\text{OUT}} V_T$ , where  $V_T$  is the total supply voltage.

The offset voltage for LT1010s is specified for the worst case over a range of supply voltages, input voltage, and temperature. It would be unrealistic to use these worst-case numbers for the Fig 11 circuit, because the paralleled units are operating under identical conditions. The offset voltage specified for  $V_S = \pm 15\text{V}$ ,  $V_{\text{IN}} = 0\text{V}$ , and  $T_A = 25^\circ\text{C}$  will suffice for a worst-case condition.

#### Use 25°C for worst-case calculations

The circuit divides the output load current according to the output resistance of the individual buffers. Therefore, the available output current will not quite be doubled unless the output resistances are matched. As for the offset voltage above, you should use the 25°C limits for worst-case calculations. Parallel operation is not thermally unstable. Should one unit get hotter than its mates, its share of the output and its standby dissipation will decrease.

As a practical matter, parallel connection requires only some increased attention to heat sinking. In some applications, a few ohms of equalization resistance in each output might be wise. Only the most demanding applications require matching, and then just of output resistance at 25°C.

**EDN**

#### Author's biography

*Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at MIT. Jim is a former student of psychology at Wayne State University, and he enjoys tennis, art, and collecting antique scientific instruments.*

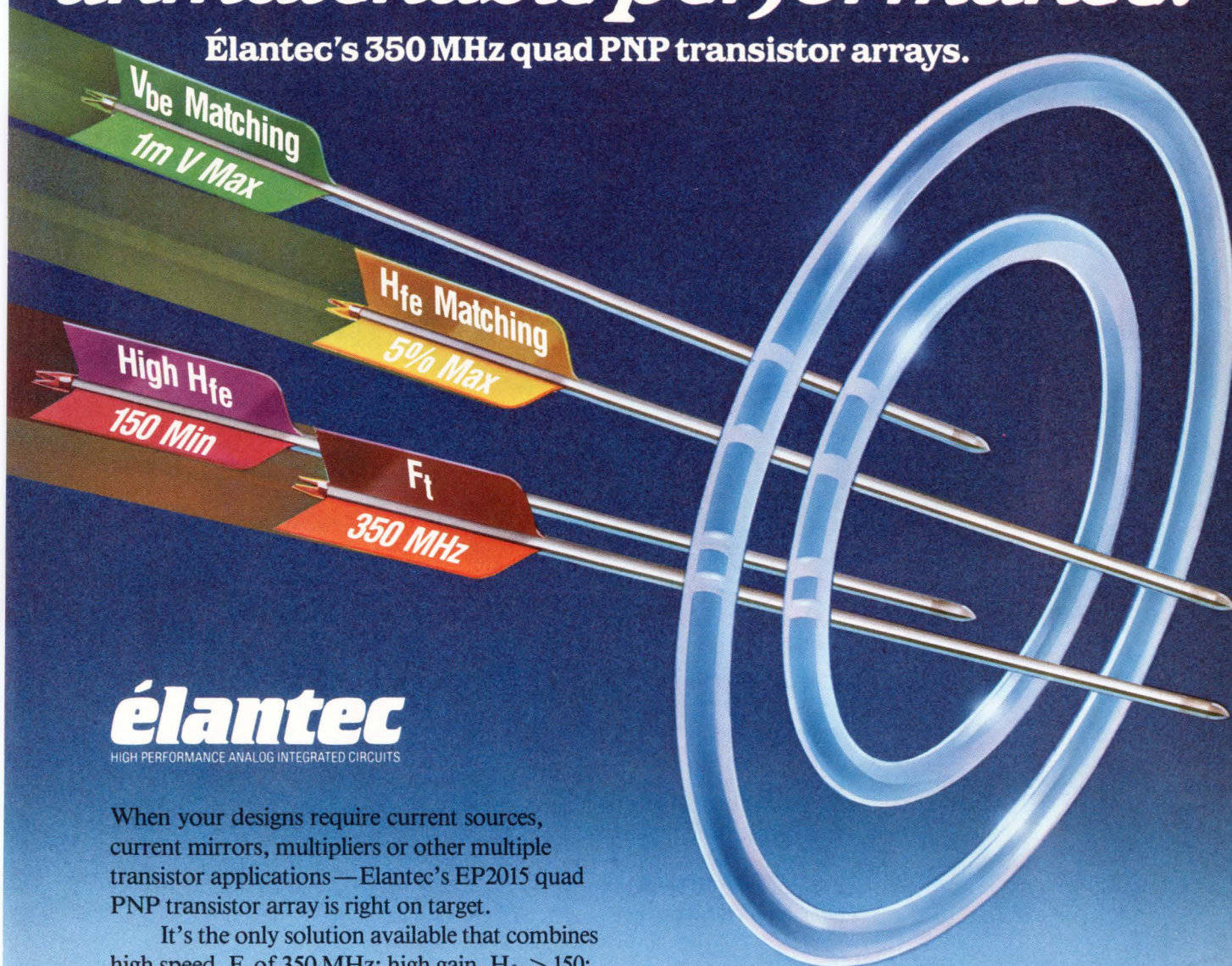
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CIRCLE NO 83

# EDIF format brings uniformity to CAE/CAD data

*The existence of a standard data format would help design engineers transfer data easily between CAE/CAD systems, or to and from a device manufacturer. The Electronic Design Interchange Format (EDIF) proposes to be such a standard. This article, the first of a series, presents the basic EDIF syntax and structure. Subsequent articles will take you through the creation of EDIF libraries, test patterns, and interfaces.*

Esther Marx, Hart Switzer, and Mike Waters,  
*Motorola Inc*

The Electronic Design Interchange Format (EDIF) is a public-domain data format that presents and orders schematics, symbolic and physical layouts, interconnections, and textual information pertaining to the design of digital and analog circuits. By using a standard data format like EDIF, you can transfer design data among incompatible CAE/CAD systems. You can also receive designs from and transfer data to ASIC foundries and pc-board fabricators.

Assuming the popularity of EDIF gains momentum, it can prevent a CAE vendor from locking you into its system; using EDIF, you can transfer your database to any CAE/CAD system that accepts this format. ASIC manufacturers will be able to use EDIF to supply libraries of their components to a variety of CAE packages.

The format lets you transfer all levels of electronic-design information. As Fig 1 shows, EDIF is the only electronic-design format that can transfer information about libraries, schematic capture, behavior, functional

and logical structure, circuits, geometric layout, and test definition, generation, and simulation.

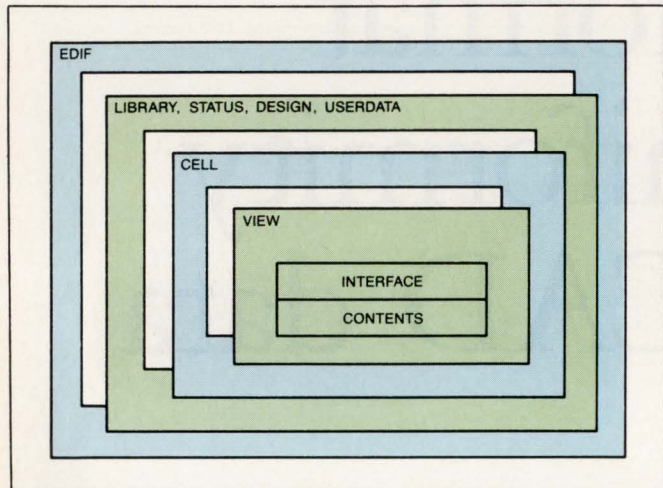
EDIF allows you to describe library and cell organizations, cell interfaces, cell details, and processing technologies. The cell-interface description includes logic symbols, ports, parameters, boundaries, port-to-port timing, feedthroughs, and functional-test patterns, and it tells you whether you can permute logical ports. The cell-detail description includes net lists, schematic diagrams, geometric layouts, gate arrays, logic models, symbolic layouts, and simulation parameters. The processing-technology description includes layer definitions, device-size scaling information, and simulation values.

To use EDIF, you must understand its structure and syntax. You can't execute EDIF as you would a pro-

	MOTOROLA MENTOR	TEXAS INSTRUMENTS	NATIONAL SEMICONDUCTOR	DAISY SYSTEMS	CALMA	OTHERS	EDIF
LIBRARIES	TDF (PHYSICAL)		CIDF (SCHEMATIC)		GAIL (PHYSICAL)		E D I F
SCHEMATIC							
BEHAVIOR				DABL		HELIX I	
STRUCTURE	SNET-WORK	TIDAL		GAIL	TEGAS		
TEST	SPAT-TERN						
CIRCUIT						SPICE	
GEOMETRY	FIX/AUX	TIDAL	CIDF	GAIL	STREAM	CIF	

Fig 1—Although CAE/CAD vendors have developed a number of data formats, only EDIF lets you transfer every aspect of a design.

*EDIF provides a standard format that lets you transfer all levels of electronic-design information.*



**Fig 2**—The hierarchical structure of EDIF reflects the natural structure of design data, from the cell library down to the devices and interconnections within each cell.

gram. It is neither a programming language nor a database system. An EDIF file is a character stream.

The hierarchy of EDIF files is based on the structure of the Lisp programming language. To write EDIF files, you don't need to be a Lisp programmer, but you do need to understand the structure of EDIF.

EDIF, like Lisp, has a tree-like structure. The fundamental objects in an EDIF file are called atoms. Groups of zero or more atoms form lists, which are separated by parentheses. Groups of lists form high-level lists, which ultimately form a file. An EDIF file, then, is a list that comprises several sublists. For example, the list (A,(B,C,B),( ),C) contains four elements (that is, atoms and sublists): the atom A; the list (B,C,B); an empty list; and the atom C.

To access and manipulate an EDIF file, you must develop a list handler. Depending on your application, you need a reader, a writer, or both. The reader must be able to access and retrieve lists. The writer must include such list-building features as creation, insertion, and concatenation.

#### Any language can handle EDIF files

You can use the list-processing features of Lisp to create and to gain access to data in an EDIF file. Remember, however, that even though EDIF has a Lisp-like structure, any programming language can manipulate EDIF files. Even if you use Lisp, you need only the data-manipulation functions; you don't carry out any computations.

The recursion features of computer languages like

Lisp, C, and Pascal make these languages particularly suitable for developing EDIF software. However, you can write list handlers in a language that lacks recursive capabilities. A Fortran G program, for example, can read and write EDIF files.

The first element of any EDIF list is a keyword, which functions as an atom in an EDIF list, along with other EDIF-specific words and your own data. **Fig 2** shows how these keywords define the hierarchy of an EDIF file.

The topmost level of an EDIF file ("EDIF" in the figure) simply identifies the file. The next level consists of four sections. The keywords that describe these sections are "status," "design," "library," and "user-data."

The status section controls your use of a file. This section includes such information as the name of the person who created the data, the name of the program that translates the data, the site where the data was created, the program version, and the version number of the data. The status section is particularly important when you are working with libraries that you didn't create, where you need to keep track of new revisions as simply as possible.

The design section is the starting point of an EDIF description. This section provides a pointer to the initial cell or design within a particular library. The library section consists of one technology section and one or more cell sections. Because this section requires only one entry for a characteristic that is common to all the cells in a library, it uses less disk space than a flat library, which repeats the common characteristic in every cell description. The userdata section lets you add extensions to the standard EDIF specification. You can also use this section to experiment with forms that will appear in later releases of EDIF.

The most important part of an EDIF file is the library section, which contains cell descriptions. A cell in a library can contain zero or more "views," and each view describes a different aspect of the cell. EDIF currently offers seven types of view, called "masklayout," "schematic," "symbolic," "netlist," "behavior," "document," and "stranger."

The masklayout view describes such physical data as mask layers and colors for plots. This view can, for example, contain descriptions of geometric figures for mask layouts. In addition to EDIF, the masklayout view accepts the public-domain California Intermediate Format (CIF).

The schematic view describes logic diagrams. This

view defines interconnections and logical elements. The symbolic view describes symbolic layouts for placing and routing a design. You can specify such data as protection frames and layout interconnections.

The netlist view lists interconnections among the components of a design. In EDIF, net lists are net oriented. In a net-oriented file, each net contains the parts that are attached to that net. In contrast, a part-oriented Spice file lists a part and then gives the nets that are connected to that part. Fortunately, the conversion between part-oriented and net-oriented files is easy and fast.

The behavior view provides basic models of simulator primitives. This view also describes cells in terms of their logic values. The behavioral descriptions let you define logical cells such as inverters and latches. The behavior view also includes a list of the logic states that you are using. For example, to use the behavior view, you need to specify how your design arbitrates wired functions and the value you wish to assign to any unconnected ports.

The document view contains diagrams and text for your design. EDIF lets you add headings, illustrations, and other documents to your text. Finally, the stranger

**TABLE 1—LEGAL CONSTRUCTS FOR EDIF VIEWS**

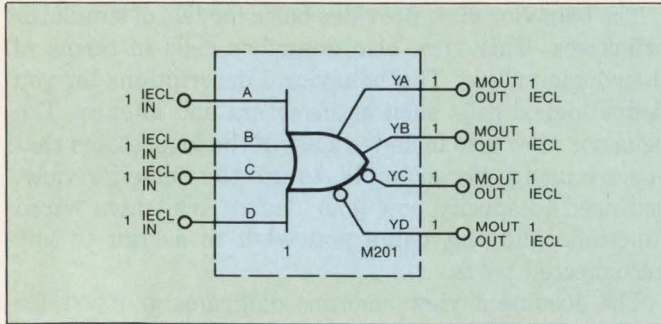
**INTERFACE SECTION**

	NETLIST	SCHEMATIC	SYMBOLIC	MASKLAYOUT	BEHAVIOR	DOCUMENT	STRANGER
PORTIMPLEMENTATION	•	•	•	•	•		•
UNUSED	•	•	•	•	•		•
BODY	•	•	•	•	•		•
ARRAYRELATEDINFO			•	•			•
JOINED	•	•	•	•	•		•
MUSTJOIN	•	•	•	•	•		•
WEAKJOINED	•	•	•	•	•		•
PERMUTABLE	•	•	•	•	•		•
DEFINE	•	•	•	•	•		•
TIMING	•	•	•	•	•		•
SIMULATE	•	•	•	•	•		•
COMMENT	•	•	•	•	•	•	•
USERDATA	•	•	•	•	•	•	•

**CONTENTS SECTION**

DEFINE	•	•	•	•	•		•
UNUSED	•	•	•	•			•
GLOBAL	•	•	•	•			•
INSTANCE	•	•	•	•		•	•
FIGUREGROUP				•			•
JOINED	•	•	•	•			•
MUSTJOIN	•	•	•	•			•
ANNOTATE		•	•				•
WIRE		•	•				•
SECTION						•	•
CRITICALSIGNAL	•	•	•				•
REQUIRED	•	•	•				•
MEASURED	•	•	•				•
LOGICMODEL					•		•
COMMENT	•	•	•	•	•	•	•
USERDATA	•	•	•	•	•	•	•

*EDIF is neither a programming language nor a database system. An EDIF file is a character stream.*



**Fig 3**—Even describing a component as simple as this 4-input OR/NOR macrocell isn't easy. **Listing 3** is only part of the EDIF listing that describes this cell.

view handles cells that don't fit into the current EDIF specification. You can transfer a stranger view file to another EDIF user only if you make prior arrangements with that user.

At the cell level, cell views relate to one another by means of "instances" or "viewmaps." Instances associate several cells or cell views that have something in common. **Listing 1** shows how to use an instance to express the relationship between a symbolic view and a masklayout view (the listings begin on page 157). A viewmap expresses the relationships among objects of the same type in different views of a cell.

In a viewmap, you can use "portmaps" and "instancemaps." A portmap lets you associate ports in different cell views. The association can be a one-to-one or a one-to-many relationship. An instancemap identifies instances in different views that describe the same object. **Listing 2** shows the use of a viewmap to describe the relationship between port A in a schematic view and ports A\_top\_of\_cell and A\_bottom\_of\_cell in a symbolic view.

### Maintain several versions of a cell

Each view has its own name, and you can create several versions of a view. For example, you can create separate military and industrial specification versions of a cell. Each view also contains "interface" and "contents" sections. The interface describes the external characteristics of a cell. It details, for example, which ports of a cell are connected within the cell and which ports are designated as interchangeable. The contents section of each cell view simply tells what devices and connections are in the cell.

You must use several keywords to define the interface and the contents of each cell. However, not all of these keywords are legal for every view type. **Table 1** lists the

keywords that are legal in the interface and contents sections of each EDIF view type.

Using these EDIF keywords, you can describe discrete devices or components in ASIC libraries. For example, you can use EDIF to create a model of the M201 bipolar 4-input OR/NOR macrocell in **Fig 3**.

**Listing 3** lists a part of the macrocell's EDIF file. (Ellipses mark missing portions of the file.) This file describes the schematic view for the cell. An interface section defines the external symbol, and a contents section describes the internal behavior of the macrocell. The file also includes a status section, which gives the originator and the time of origination of the cell.

The remaining articles in this series will show you how to create component libraries, how to create and transfer test patterns, and how to develop EDIF interfaces for your own CAD operation. In the meantime, if you want more information about EDIF or copies of the specification, contact the EDIF User Group, 2222 S Dobson Rd, Bldg 5, Mesa, AZ 85202. **EDN**

### Authors' biographies

*Esther Marx is a senior software engineer in Motorola Semiconductor Product Sector's ASIC Division (Mesa, AZ). She received an MS from George Washington University and a BA from Oberlin College. Before joining Motorola, Esther served five years in the Air Force. She enjoys writing science fiction and collecting Star Trek memorabilia.*



*Hart Switzer is a software engineer with Motorola Semiconductor Products, where she designs and implements EDIF software. She received a BS from Stanford University. Hart enjoys gardening and collecting antiques.*



*Mike Waters is a principal engineer and EDIF project manager at Motorola Semiconductor Products. He received a BS in computer science from Regent's College in New York. Mike likes to exchange ideas with other EDN readers via his ham radio (license AA4MW) or his amateur packet radio.*



Article Interest Quotient (Circle One)  
High 473 Medium 474 Low 475

### LISTING 1—EDIF INSTANCE

```
(CELL EXAMPLE_CELL_1
  (VIEW MASKLAYOUT EXAMPLE1
    (COMMENT "RELATING TWO VIEWS TOGETHER"))))
(CELL EXAMPLE_CELL_2
  (VIEW SYMBOLIC EXAMPLE2
    (COMMENT "INSTANTIATING MASKLAYOUT VIEW IN CELL EXAMPLE_CELL_1")
    (CONTENTS
      (INSTANCE EXAMPLE_CELL_1 EXAMPLE1 ID1))))
```

### LISTING 2—EDIF VIEW MAP

```
(CELL EXAMPLE_CELL
  (VIEWMAP
    (PORTMAP
      (QUALIFY SYMBOLICLAYOUT A_TOP_OF_CELL)
      (QUALIFY SYMBOLICLAYOUT A_BOTTOM_OF_CELL)
      (QUALIFY SCHEMATIC_REP A)))
    (VIEW SCHEMATIC SCHEMATIC_REP
      (INTERFACE
        (DEFINE INPUT PORT A)))
    (VIEW SYMBOLIC SYMBOLICLAYOUT
      (INTERFACE
        (DEFINE INPUT PORT
          (MULTIPLE A_TOP_OF_CELL A_BOTTOM_OF_CELL))
        (PORTIMPLEMENTATION A_TOP_OF_CELL
          (FIGUREGROUP METAL
            (RECTANGLE
              (POINT 10 11)
              (POINT 11 12))))
        (PORTIMPLEMENTATION A_BOTTOM_OF_CELL
          (FIGUREGROUP METAL
            (RECTANGLE
              (POINT 10 0)
              (POINT 11 1))))
        (JOINED A_TOP_OF_CELL A_BOTTOM_OF_CELL))))))
```

### LISTING 3—EDIF FILE FOR M201 MACROCELL

```
(EDIF M2500_SYMBOL_LIBRARY
  (STATUS (EDIFVERSION 1 0 0)(EDIFLEVEL 0)
    (WRITTEN (TIMESTAMP 1986 4 14 23 15 32)))
  (LIBRARY M2500_ECL
    (TECHNOLOGY M2500_ECL
      (NUMBERDEFINITION ENGLISH (SCALE DISTANCE 1 (E 1 - 4)))
      (COMMENT "EDIF UNIT IS ONE TENTH OF A MIL")
      (NUMBERDEFINITION SI
        (USERDATA POWERDEFINITION (SCALE POWER 1 (E 1 - 3))))
      (COMMENT "EDIF UNIT IS ONE MILLIWATT"))
    (CELL M201
      (STATUS (EDIFVERSION 1 0 0)(EDIFLEVEL 0)
        (WRITTEN (TIMESTAMP 1986 4 11 15 49 54 46)
          (ACCOUNTING PROGRAM "SYM2EDIF V2.00")
          (ACCOUNTING AUTHOR "MOTOROLA SEMI-CUSTOM")))
      (VIEW SCHEMATIC MACRO_SCHEMATIC
        (INTERFACE
          (USERDATA PAGESIZE (POINT - 125000 - 125000)(POINT 125000 125000))
          (USERDATA PINSPACING 2500)(DEFINE UNSPECIFIED PORT YD)
          (PORTIMPLEMENTATION YD
            (FIGUREGROUP SYMBOL_PIN (DOT (POINT 20000 0)))
            (USERDATA ATTRIBUTE
              (PROPERTY MAMP 1
                (PROPERTY DISPLAYAT (POINT 18250 500)(POINT 19500 1750))
                (PROPERTY JUSTIFY LOWERLEFT))))))
```

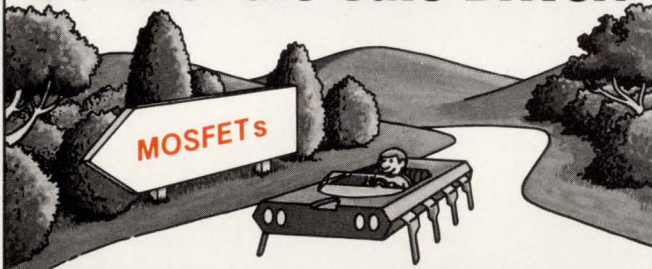
Listing continued on pg 158

**LISTING 3—EDIF FILE FOR M201 MACROCELL** (Continued)

```

(USERDATA ATTRIBUTE
  (PROPERTY OUTPUTTYPE "MOUT" (PROPERTY VISIBLE FALSE)
    (PROPERTY DISPLAY AT (POINT 21250 750)(POINT 23250 1250))
    (PROPERTY JUSTIFY LOWERLEFT)))
(USERDATA ATTRIBUTE
  (PROPERTY PINNAME "YD"
    (PROPERTY DISPLAY AT (POINT 15750 500)(POINT 18750 2000))
    (PROPERTY JUSTIFY LOWERRIGHT)))(DEFINE OUTPUT PORT YC)
(PORTIMPLEMENTATION YC . . . )(DEFINE OUTPUT PORT YB)
(PORTIMPLEMENTATION YB . . . )(DEFINE OUTPUT PORT YA)
(PORTIMPLEMENTATION YA . . . )(DEFINE INPUT PORT D)
(PORTIMPLEMENTATION D . . . )(DEFINE INPUT PORT C)
(PORTIMPLEMENTATION C . . . )(DEFINE INPUT PORT B)
(PORTIMPLEMENTATION B . . . )(DEFINE INPUT PORT A)
(PORTIMPLEMENTATION A . . . )
(BODY
  (FIGUREGROUP SCHEMATIC__SYMBOL (FILLPATTERN 1 1 "0")
    (SHAPE
      (ARC (POINT 6750 2000)(POINT 7500 3750)(POINT 6750 5500)))
      (PATH (POINT 6750 2000)(POINT 9000 2000))
      (PATH (POINT 9000 5500)(POINT 6750 5500)) . . . )
    (USERDATA BORDER MACRO_BORDER
      (FIGUREGROUP BORDER (BORDERPATTERN 6 "001111")
        (RECTANGLE (POINT 2500 -2500)(POINT 17500 10000))))
    (USERDATA ATTRIBUTE
      (PROPERTY COMPSIZE 1
        (PROPERTY DISPLAY AT (POINT 7500 -2000)(POINT 9000 -500))
        (PROPERTY JUSTIFY LOWERLEFT)))
    (USERDATA ATTRIBUTE
      (PROPERTY MACRONAME "M201"
        (PROPERTY DISPLAY AT (POINT 16750 -2000)(POINT 22750 -500))
        (PROPERTY JUSTIFY LOWERRIGHT))))))
  
```

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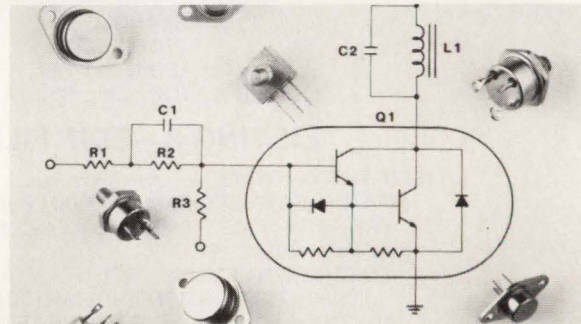
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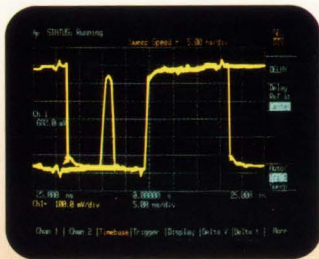
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## Floppy Disk

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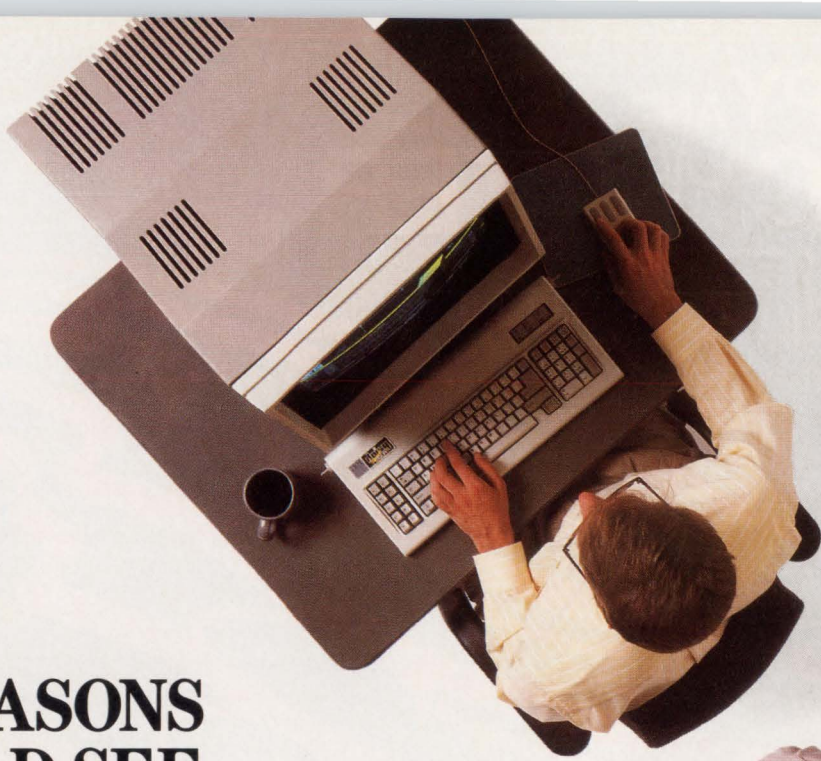
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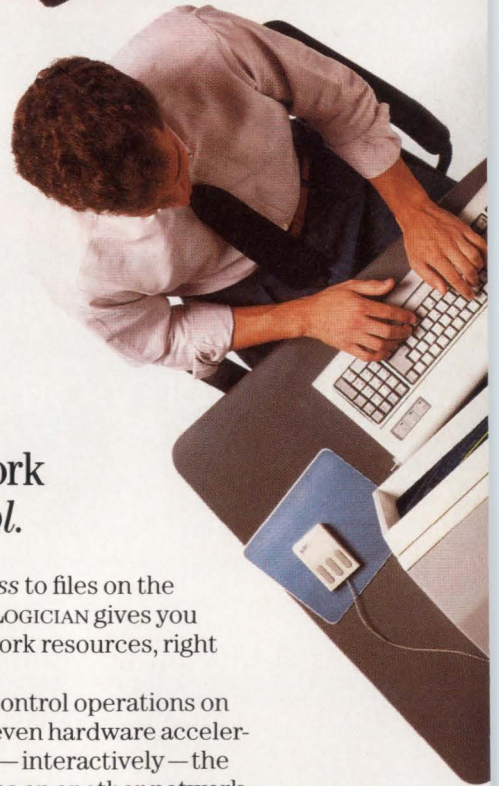
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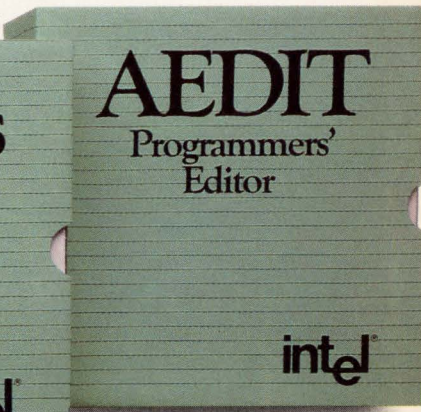
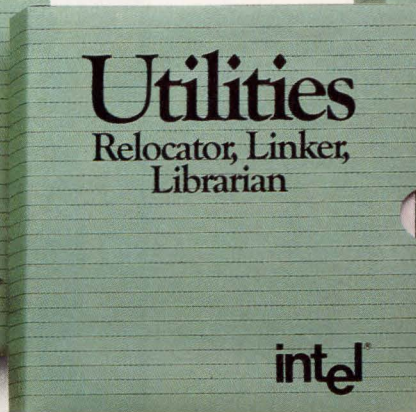
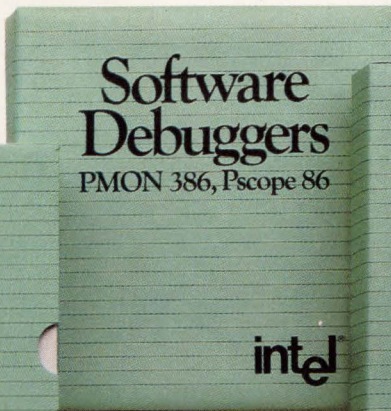
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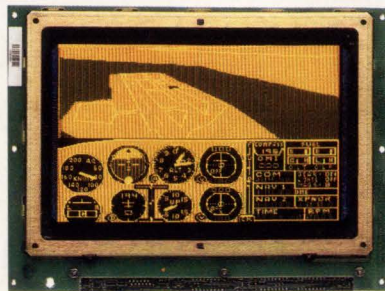


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# ISDN terminals simplify data transmissions

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*The Integrated Services Digital Network (ISDN) digitizes voice signals to provide a complete digital link from end user to end user. The result is a common communication link—the telephone system—that provides access to all forms of communication. A recently introduced IC set can simplify the implementation of ISDN terminals.*

---

Tony O'Toole, *Advanced Micro Devices*

Converting digital data to an analog signal is an inefficient and expensive proposition. The conversion often garbles the data, and because it limits transfer speed, it always increases telephone charges. The increased use of computer-based systems has compounded the problem by increasing the amount of data being transferred over long distances.

The solution to this problem is the Integrated Services Digital Network (ISDN), a technique for using phone lines to transmit digital data instead of the analog data they transmit now. The ISDN will also digitize voice signals, so that the same lines will carry voice, facsimile, data, and telex-type transmissions. Furthermore, because this technique doesn't require

you to convert your data transmission to analog signals to send it over the phone lines, your transmission will be faster. You can configure an ISDN terminal by using a recently introduced chip set that contains most of the functional blocks required for implementing the ISDN protocols.

Before designing an ISDN terminal, however, you must understand the electrical, data-interchange, and call-rate control protocols recommended by the CCITT (International Consultative Committee for Telegraphy and Telephony) for ISDN devices. These protocols will allow independently designed ISDN devices to communicate with one another.

The basic access interface is the connection point on the ISDN for user terminals. **Fig 1** shows a functional model of the elements forming this interface. The S interface supports terminal connections in either a point-to-point (for maximum range) or a point-to-multipoint environment. ISDN terminal equipment (TE1) connects to the S interface to form the user's access point. Non-ISDN terminal equipment (TE2) connects to an R interface first, and then to the S interface through a terminal adapter (TA). The R interface can accommodate any communication protocol (RS-232C, X.21, etc), but the TA must convert these protocols so that they're compatible with the S interface. The network termination (NT2) converts the point-to-multipoint S interface to a point-to-point T interface.

The 2-wire U interface can extend the range of the

*The Integrated Services Digital Network (ISDN) is a technique for using phone lines to transmit digital data instead of the analog data they transmit now.*

basic access interface in a point-to-point configuration. Unfortunately, no international standard exists for implementing a U interface, so the companies that produce ISDN products each have different versions of it. The exchange termination (ET) forms the interface between the local exchange and the basic access interface. Its function depends on the architecture of individual exchanges.

In an ISDN network, the basic access information rate for terminal equipment in each transmit and receive direction is 144k bps. Each user-designated B data channel (B1 and B2) requires 64k bps, and the D channel uses the remaining 16k bps to carry signaling information for B-channel call control. You can also use the D channel for a packet-switched data connection, or for maintenance purposes.

The S interface provides a 4-wire connection between the TE and the NT2. Data transfers every 250  $\mu$ sec in 48-bit frames (Fig 2). The data rate in both directions is 192k bps: 144k bps for the B and D channels and 48k bps for framing control, dc balancing, and the D-channel access protocol.

The CCITT recommendations for terminal-to-network signaling communication are based on layered protocol levels specified by the International Standards Organization (ISO). The use of a layered protocol divides the communication operation into separate functions. Each protocol layer in a terminal performs its intended function by interacting with its peer in the network via a virtual connection (Fig 3). Sets of primitives that allow adjacent layers in the protocol to

communicate with each other maintain the virtual connections. Keeping these primitives simple ensures that boundaries between layers are well defined, and these established boundaries allow the layers to function independently.

**Special considerations in terminal design**

The intelligence requirement for a basic call is the major difference between a conventional phone and an ISDN terminal. The conventional phone merely translates a given key operation into a line signal. The ISDN terminal must interpret inputs, basing its interpretation on the current progress state of a given call. For example, the terminal may have to generate a message and invoke the level 2 procedure to ensure correct transfer to the exchange. To do so, it must first handle incoming messages at level 2, use their level 3 content to provide feedback to the user, and change the current call status.

Traditional phones are line-powered devices, so they can work when local power is lost and the exchange is operating on a backup supply. It's relatively simple for the conventional phone to function on backup power, because the phone's circuitry is not very complex and its power drain is minimal. The power drain of an ISDN terminal is much higher; an ISDN terminal requires additional circuitry to digitize the voice channel and handle the signaling protocol.

Most ISDN terminals incorporate a display that provides the extensive call information (the calling number, call state, etc) that an ISDN user needs. ISDN

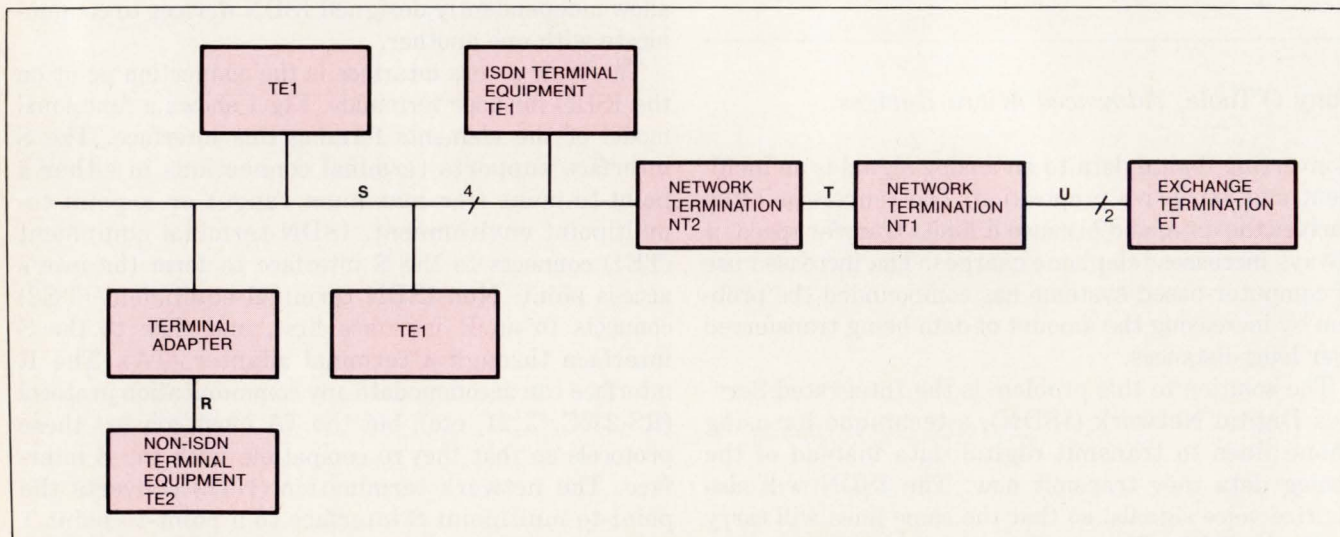


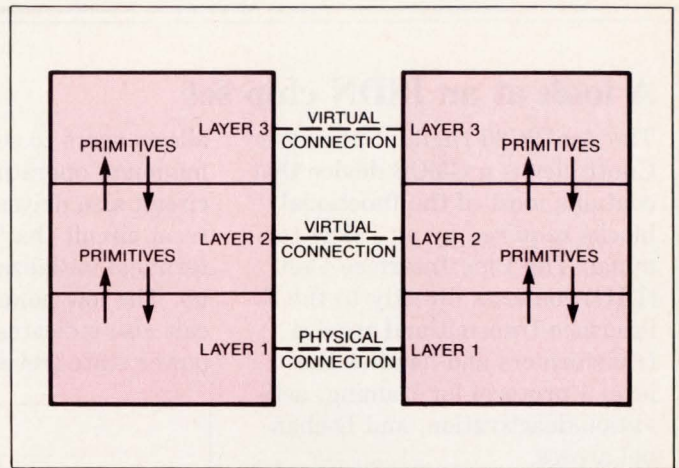
Fig 1—The connection point on the ISDN for user terminals is the basic access interface.

terminals must also provide the user with the ring signal and with call-progress tones that are not necessarily available from the network. Furthermore, no ringing voltage can be present on the digital interface; the terminal must provide an alert tone via a loud-speaker.

Your terminal should also allow you to alter the volume, pitch, and pattern of the tones to indicate different incoming-call conditions—internal/external call, emergency call, etc. Call-progress tones, which are normally provided by the network, may not necessarily be available either to the local exchange or to an ISDN terminal; to carry a call-progress tone, both these systems would need to have a B channel allocated. If the local exchange and terminal can carry a call-progress tone, the local exchange may specify the actual frequency and cadence of the tones, so the terminal must have software control over the tone generation.

When an ISDN network makes a call to a conventional network, the ISDN terminal may have to provide DTMF tones. Existing analog services such as home banking rely on the user to provide DTMF tones during the data-transfer phase of a call, so any ISDN terminal you build now will have to provide these DTMF tones to maintain compatibility with the conventional equipment. Providing these tones will ensure that existing user services are maintained while the communications networks make the transition to a complete digital system.

The two 64k-bit B channels on the S interface are not dedicated to a particular function—you can use them



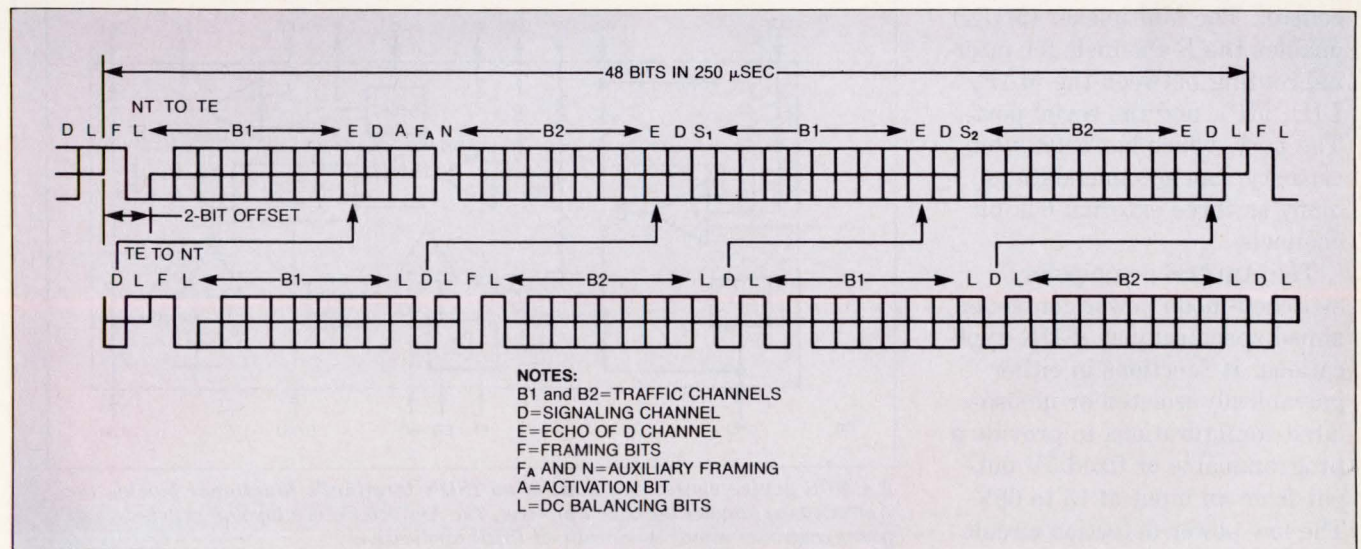
**Fig 3**—To perform its intended function, a layer in the terminal interacts with its peer in the network via a virtual connection. Sets of primitives maintain the virtual connections.

for voice or data. Therefore, the terminal must be able to route each B channel to either its voice or its data endpoint.

### ICs simplify terminal design

**Fig 4** illustrates an ISDN terminal design based on the Am79C30 digital subscriber controller (DSC) and the Am7936 subscriber power controller (SPC). An 80C51 microcontroller, configured in the expanded mode to accommodate an external EPROM/ROM for continued program-memory expansion, controls the terminal. The external RAM stores data, and the liquid-crystal display, keypad, and telephone handset form the user interface. The Am79C30 connects the handset to the S interface. The 80C51 accesses the Am79C30, keypad, and display as external memory; port 1 of the 80C51 provides display reset and keypad scanning functions. The Am79C30 is transformer coupled (in both the transmit and receive directions) to the S interface, so it provides access for all information transfer.

The Am79C30 is mapped into eight bytes of the



**Fig 2**—The S interface provides a 4-wire connection between the TE and the NT. Data transfers every 250  $\mu$ sec in 48-bit frames.

## A look at an ISDN chip set

The Am79C30 Digital Subscriber Controller is a CMOS device that contains most of the functional blocks required by an ISDN terminal. The Line Interface Unit (LIU) connects directly to the S-interface transmit and receive transformers and handles the level 1 protocol for framing, activation/deactivation, and D-channel access.

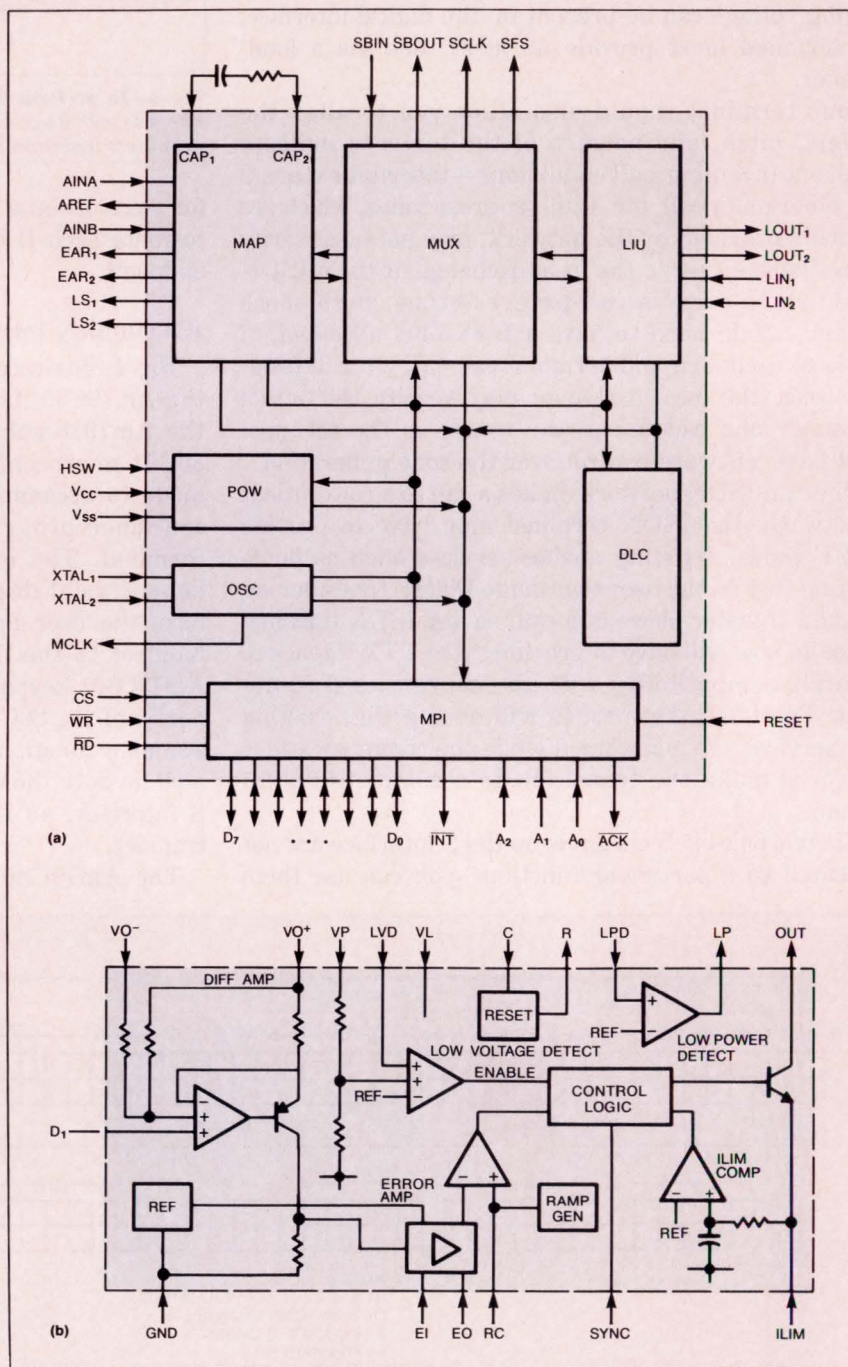
The Main Audio Processor (MAP) connects to two sets of audio transducers. It uses digital signal processing to perform all the normal codec filter functions, and it provides transmit and receive gain and response adjustments, as well as side-tone control. The MAP also contains two tone generators that users can configure three different ways to produce call-progress tones, a ringing tone, and multifrequency (MF) tones.

The Data Link Controller (DLC) processes the D channel as far as an intermediate stage of the LAPD protocol, performing flag insertion and deletion, zero insertion and deletion, CRC generation and checking, address recognition, and message-length checking. The 8-bit Microprocessor Interface (MPI), which allows external control of all the internal blocks, maintains control. The Multiplexer (MUX) enables the B channels for internal routing between the MAP, LIU, MPI, and the serial port. The port, which has a 192k-bit capacity, can accommodate as many as three external 64k-bit channels.

The Am7936 is a bipolar switched-mode power controller aimed specifically at ISDN applications. It functions in either galvanically isolated or nonisolated configurations to provide a programmable or fixed 5V output from an input of 15 to 65V. The low-power-detection circuit

allows users to select a variable minimum operating voltage. The circuit also drives an on-chip reset circuit that's suitable for terminal initialization at power up. The low-power-detection circuit also indicates the emergency power state (reverse voltage on

the S interface). To accommodate the presence of analog circuitry in the terminal, a sync input allows you to synchronize the Am7936 to the analog processing circuit, thereby reducing the effects of supply interference on signal-to-noise performance.



A CMOS device containing most of an ISDN terminal's functional blocks, the Am79C30 (a) handles the level 1 protocol. The Am7936 (b) is a bipolar switched-mode power controller aimed specifically at ISDN applications.

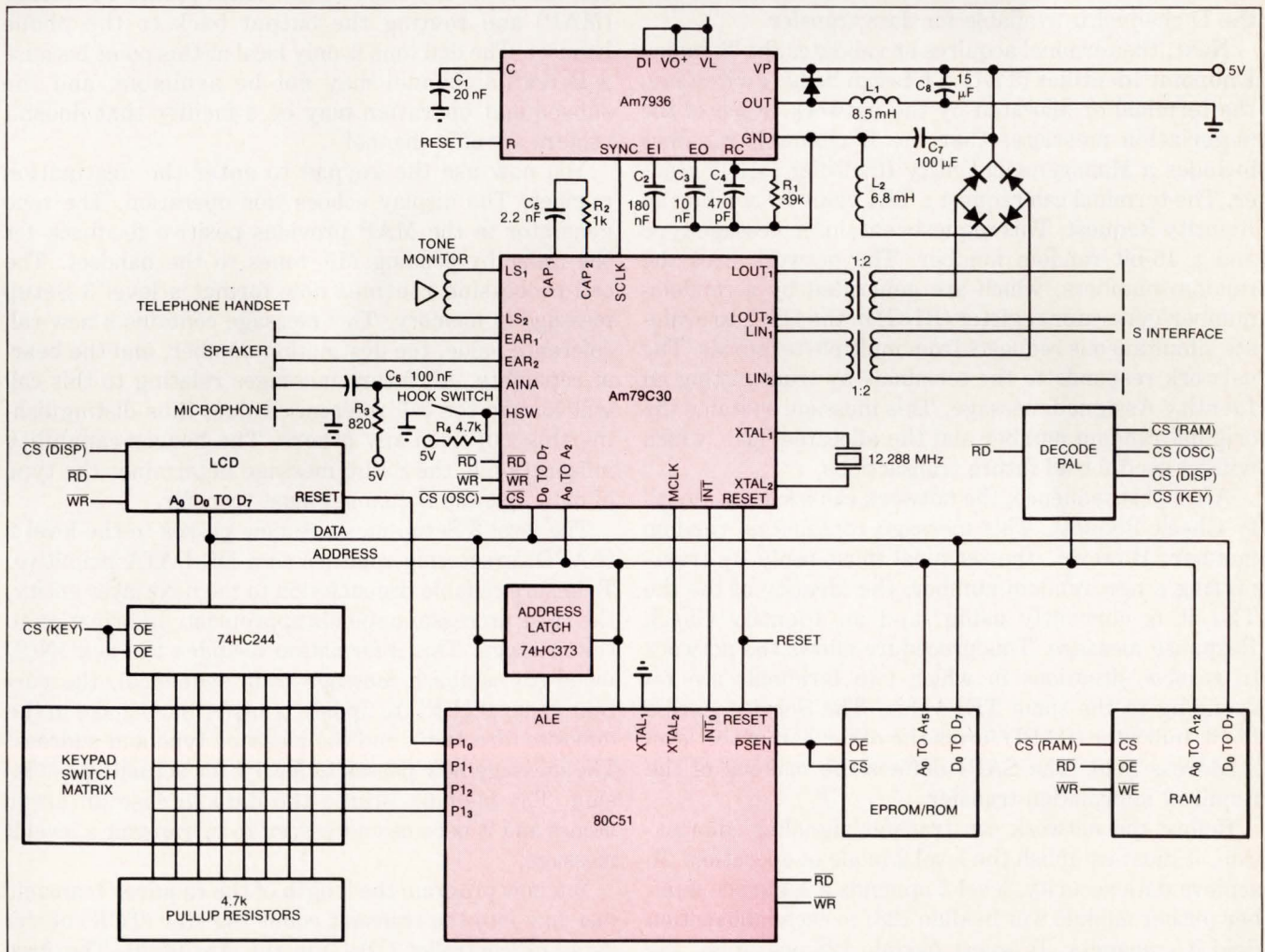
*To keep all the data between a terminal and exchange in digital form, the terminal must digitize voice signals before they get to the exchange.*

80C51's external memory space. The 80C51 accesses the Am79C30's most frequently used registers directly and uses the Am79C30's register-pointer mechanism to access the less frequently used registers. The MCLK output of the Am79C30, derived from a crystal oscillator circuit, supplies the system clock to the 80C51. In normal operation, a single interrupt connection between the Am79C30 and the 80C51 is activated by a change of state in the D channel, in hookswitch operation, or in the S-channel protocol.

The LCD displays call-progress and user-to-user information. The 80C51 accesses the display as two bytes of external memory—one for command inputs, such as cursor control, and one as an ASCII data input. The keypad consists of a simple switch matrix that's

read via an octal buffer and scanned via a series of I/O pins on the 80C51. As each I/O line is successively strobed, the 80C51 reads the buffer to determine whether any key is depressed.

The Am7936 SPC—a switched-mode power converter compatible with the S-interface requirements—supplies power to the terminal circuits. Here, the SPC is configured as a step-down converter that supplies a regulated 5V output from an input of 15 to 65V. A diode bridge ensures that the terminal will operate during emergency power conditions, under which the power-feed polarity is reversed to deactivate nonessential equipment. Connecting the serial clock from the Am79C30 to the Sync pin of the SPC synchronizes the converter. This scheme minimizes noise caused by



**Fig 4**—To simplify the implementation of an ISDN terminal, you can combine the 79C30 digital subscriber controller with the Am7936 subscriber power controller. An 80C51 controls the terminal.

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*Before the network can transfer signaling information, it must establish the level 2 mode of operation.*

---

power-supply ripple on the analog voice channel.

The 80C51 scans the keypad, displays information, and controls channel B in the Am79C30. It also has routines for performing the level 2 and level 3 protocols on the D channel. The 80C51's timers provide a real-time clock for scheduling the above tasks and a cadence control for tone generation.

On power up, the reset output from the Am7936 initializes the terminal. The terminal must now negotiate several logical states before it can generate calls. Under the control of the 80C51, the Line Interface Unit (LIU) in the Am79C30 connects the terminal to the interface. If no signal is present on the network side, the LIU signals an activation request by transmitting the INFO1 signal. Once the terminal detects an activation frame (INFO2), it enters the activated state and the D channel is available for data transfer.

Next, the terminal acquires or validates the Terminal Endpoint Identifier (TEI). TEIs can be hardwired into the terminal or allocated by the network. Each of the negotiation messages that the D channel transfers includes a Management Entity Identifier (MEI) header. The terminal can request a TEI value by sending an Identity Request. This request contains a message type and a 16-bit random number. The network uses the random numbers, which are generated by a random-number-generator register (RNG) in the DSC, to evaluate simultaneous requests from multiple terminals. The network responds to the terminals by transmitting an Identity Assigned message. This message contains the original random number and the allocated TEI, which will be used for all future transactions.

After this sequence, the network can issue an Identify Check Request. This message contains no random number. However, the terminal must reply by transmitting a new random number, the identity of the TEI it is currently using, and an Identify Check Response message. This procedure allows the network to resolve situations in which two terminals are responding to the same TEI value. The Service Access Point Indicator (SAPI) forms the other half of the level 2 address field. The SAPI defines the makeup of the required information transfer.

Before the network can transfer signaling information, it must establish the level 2 mode of operation. To achieve data security, level 2 appends a sequence number (either modulo 8 or modulo 128) to each information field it transmits. To select modulo 128 operation, the terminal sends a Set Asynchronous Balance Mode Extended (SABME) signal to the connecting level 2 inter-

face. If the interface can support modulo 128 operation, it returns an Unnumbered Acknowledgment (UA) frame to the terminal. To select modulo 8 operation, the terminal sends a Set Asynchronous Balance Mode (SABM) signal and receives a UA frame. Regardless of the operating mode, the level 2 variables are initialized, and secure data transfer can proceed.

To understand how the terminal implements the protocol to establish communication links, consider the progress of a simple voice call. You initiate a call by taking the terminal off hook. The Am79C30 detects this action and interrupts the 80C51, which interprets the off-hook as a request for service and generates a local dial tone. The 80C51 generates this tone by setting the required frequency register (FTG) and amplitude register (ATG) in the Am79C30's Main Audio Processor (MAP) and routing the output back to the phone handset. The dial tone is only local at this point because a B traffic channel may not be available, and the subsequent operation may be a facility that doesn't require a traffic channel.

You now use the keypad to enter the destination number. The display echoes this operation. The tone generator in the MAP provides positive feedback for the caller by sending MF tones to the handset. The call-processing routines now format a level 3 Setup message in memory. This message contains a new-call reference value, the destination number, and the bearer capability. All future messages relating to this call will contain the call reference value, thus distinguishing this call from any others. The bearer-capability information in the Setup message determines the type of data that the B channel must transfer.

The level 3 Setup message now passes to the level 2 (LAPD) processing routines as a DL-DATA primitive. To ensure reliable transmission to the next layer entity, the layer processor appends appropriate information to the message. This information includes the next N(S) value (to establish message-train sequence), the current value of N(R) (to update transfer handshake in the opposite direction), and the message type and address. The message now passes to level 1 for actual transmission. The memory stores the data in case an error occurs and it becomes necessary to retransmit a level 2 message.

You now program the length of the required transmit message into the transmit count register (TCR) of the data-link controller (DLC) in the Am79C30. The first byte transfers to the transmit data register (TDR), enabling transmission. Once the D channel has been

## Basic ISDN operation

To understand ISDN message-transfer techniques, consider a simple call from one terminal to another in the same exchange. A terminal initiates a call when the user takes the terminal off hook and keys in digits via a keypad. To initiate a call, level 3 in the terminal always generates a Setup message. The terminal selects a call-reference value and uses this value in all subsequent messages relating to this call between the originating terminal and the exchange.

The Setup message must contain the bearer capability—information that details the type of data to be transmitted on the traffic channel. For this sample call, a normal off-hook condition indicates a voice connection coded in A or  $\mu$  law. For a data call, the Setup message would indicate the format and data rate. The keyed digits form the destination-address field. If any digits are unknown at the start of the sequence, the terminal supplies them in subsequent Information messages.

When the exchange receives the Setup message, it replies with a Setup Acknowledge, designating the traffic channel (B1 or B2) to be used for the call. The exchange then routes the call and designates a call reference value for all message transfers to and from the destination terminal. Next, the exchange sends a Setup message to the destination terminal. This message contains the originating bearer capabilities, the traffic-channel information, and the

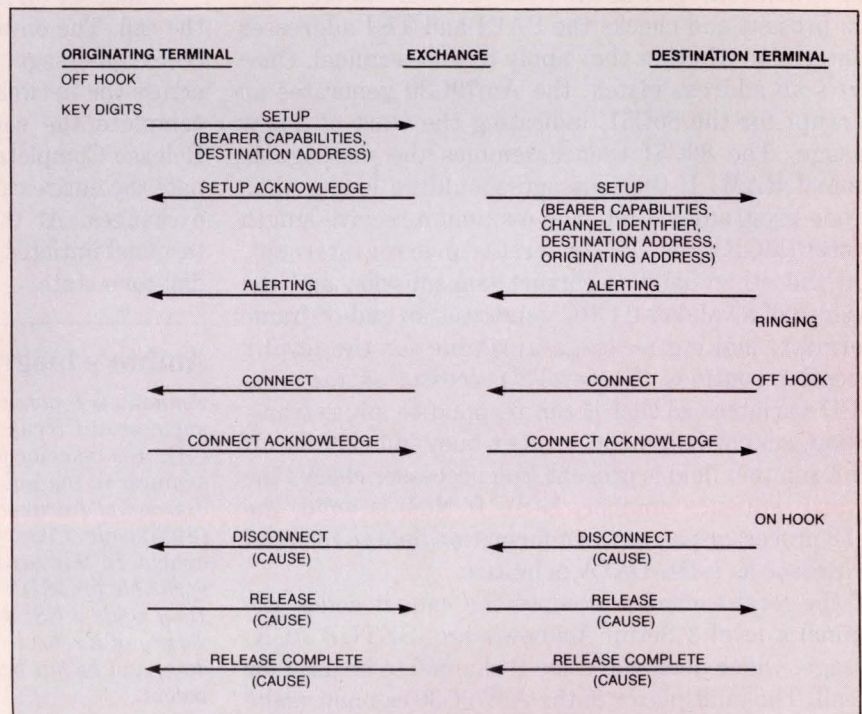
destination and origination addresses. The destination address is not redundant information, because a terminal may have several addresses in a network, or the exchange may have rerouted the call.

The destination terminal checks the validity of the bearer capability and replies with an Alerting message if the bearer capability is valid. The destination terminal then alerts its user to the incoming call by generating a ring signal. When the destination terminal goes off hook, it sends a Connect message through the exchange to the originating terminal. The call is now in the voice-transfer state.

Either user can terminate the

call by putting the terminal on hook. This action generates a Disconnect message, which breaks down the call in the exchange and then gets passed to the other terminal. Note that a normal termination, such as this, is not the only cause of a Disconnect. A Disconnect could also be the result of network congestion, incompatible bearer capabilities, or other problems.

After the Disconnect, the Release and Release Complete sequence completes the call-teardown procedure between each terminal and the exchange. The exchange then releases the call reference values associated with the call on both data links.



*For a call within the same exchange, an ISDN terminal initiates a call when the user takes it off hook and keys in digits via a keypad.*

---

*Once the exchange signals that it has received a suitable level 2 response, the terminal's memory can discard the transmitted message.*

---

idle for the appropriate number of bits, transmission starts, and the DLC generates an opening flag. Transmission then continues; the Am79C30 generates interrupts to the 80C51 as new bytes are required. When the required number of bytes has been transmitted, the DLC appends a cyclic redundancy check (CRC) and a closing flag to the outgoing message.

If the DLC does not receive the appropriate number of bytes, it generates a transmit-underrun error and does not append a CRC to the frame. If a conflict should occur on the D channel, the E channel echoes the data that has been accepted. The LIU in the Am79C30 monitors the E channel. If it detects an error, it aborts transmission and generates an interrupt for the 80C51. When the D channel is free, the transmit process must begin again from the start of the message. Because the E channel's abort mechanism produces an immediate response, one terminal's data will always transfer correctly when a conflict occurs.

Once the exchange signals that it has received a suitable level 2 response, the terminal's memory can discard the transmitted message. If the exchange doesn't signal a response, the terminal retransmits the message after a level 2 timeout. When a message from the D channel arrives at the DLC, the DLC detects any flags present and checks the SAPI and TEI addresses to determine whether they apply to this terminal. Once there's an address match, the Am79C30 generates an interrupt for the 80C51, indicating the start of a new message. The 80C51 then assembles the message in terminal RAM. If the message should be longer than the one programmed into the maximum-receive-length register (MCR), the DSC generates an error interrupt.

On the other hand, a correct transmission and the presence of a validated CRC generates an end-of-frame interrupt, making message available for the level 2 processing routines. The level 2 processor extracts the LAPD variables so that it can respond to any retransmission, acknowledgment, or peer-busy information. If an information field is present, the processor checks the forward sequence number, N(S). If N(S) is valid, the level 2 processor passes the information field to the level 3 processor as a DL-DATA primitive.

If the local exchange accepts the call, it sends the terminal a level 3 Setup Acknowledge (SETUP ACK) message, which designates the B channel to be used for the call. The multiplexer in the Am79C30 can now make the appropriate connection, on the Line Interface Unit (LIU), between the MAP and the selected B channel.

The local exchange also forwards a SETUP message

to the destination terminal. If the destination terminal is deactivated, the network must first activate it by sending INFO2 frames, which are level 2 parameters that must be negotiated. The level 2 parameters at each terminal don't have to be identical. Nor does the SETUP message received by the destination terminal have to match the originating message—parameters such as the selected B channel are unique to the local interface. If the originating terminal receives no response to the initial SETUP message, it will make another attempt to initiate the call.

If the destination terminal is free, it responds to the SETUP message with a Call Proceeding (CALL PRO) message. The called terminal then generates local ringing to its loudspeaker, and displays an incoming-call message that includes the number of the originating terminal. The calling terminal generates distant ringing to its handset. The local Am79C30's tone generators produce both of these ring tones.

A handset-off-hook condition at the called terminal stops the generation of the local tone and sends a Connect (CONN) message. When the originating terminal receives the CONN message, remote ring-tone generation stops; the call is now in the connect phase.

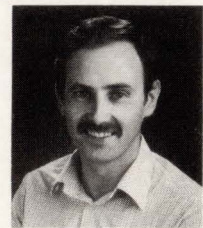
A handset-on-hook condition at either terminal ends the call. The on-hook condition generates a Disconnect (DISC) message, which in turn deletes the connection across the network. The terminals and local exchanges complete the sequence with a Release (REL) and Release Complete (REL COM) message, which terminate the entire call procedure in the terminals and local exchanges. At this point, any off-hook condition at a terminal initiates a new call, and the system enters the dial-tone state.

**EDN**

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### Author's biography

*Anthony O'Toole, now a senior design engineer at Cirrus Logic (Milpitas, CA), was a senior product-planning engineer in the Voice Communications division of Advanced Micro Devices (Sunnyvale, CA) when he wrote this article. In this capacity, he was responsible for ISDN product planning. Tony holds a BSc degree from the University of Exeter in the United Kingdom, and he has been granted one patent.*



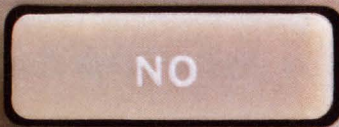
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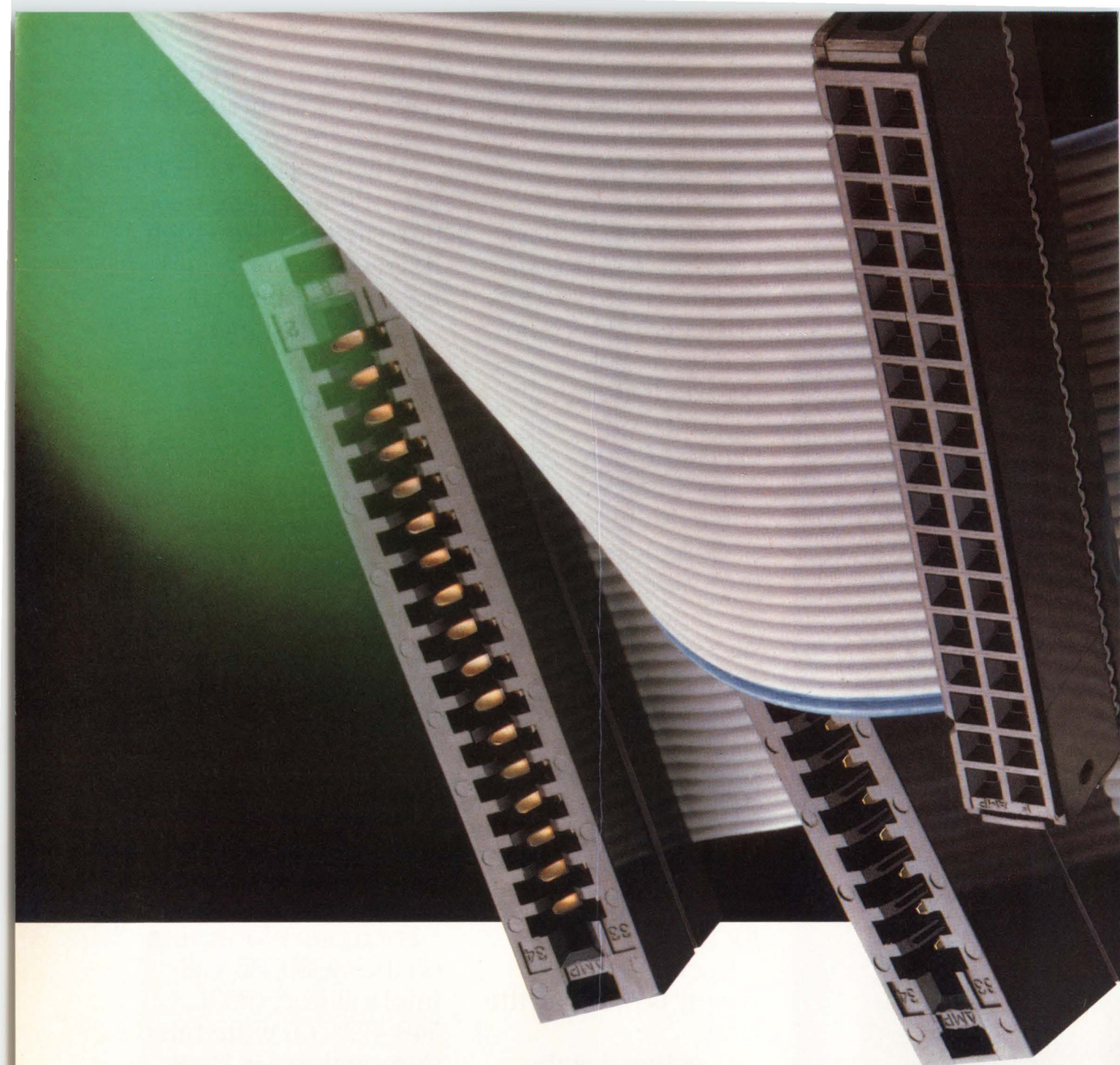
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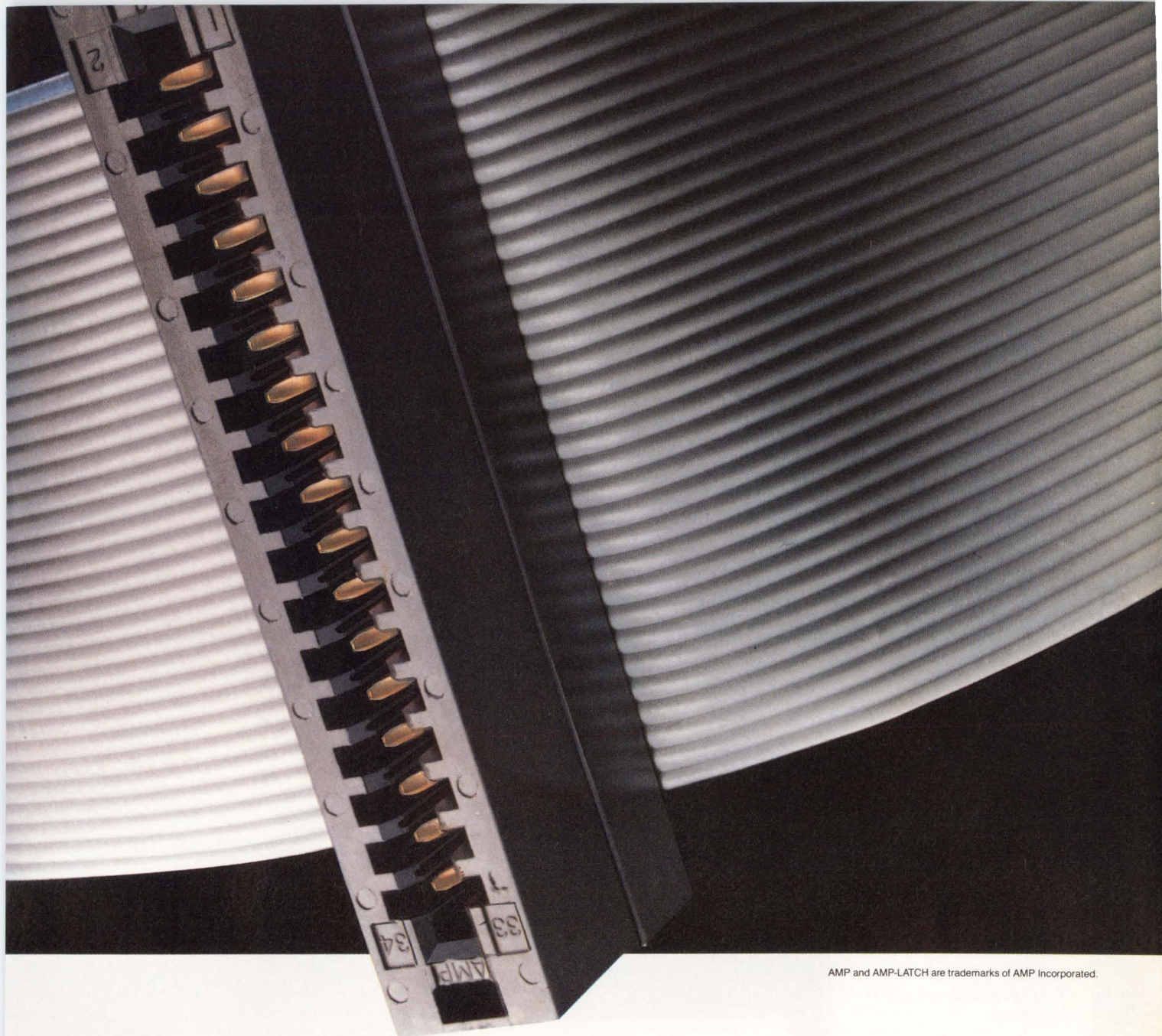
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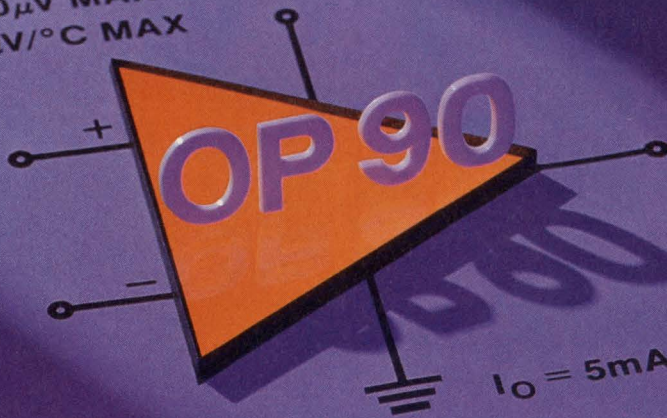
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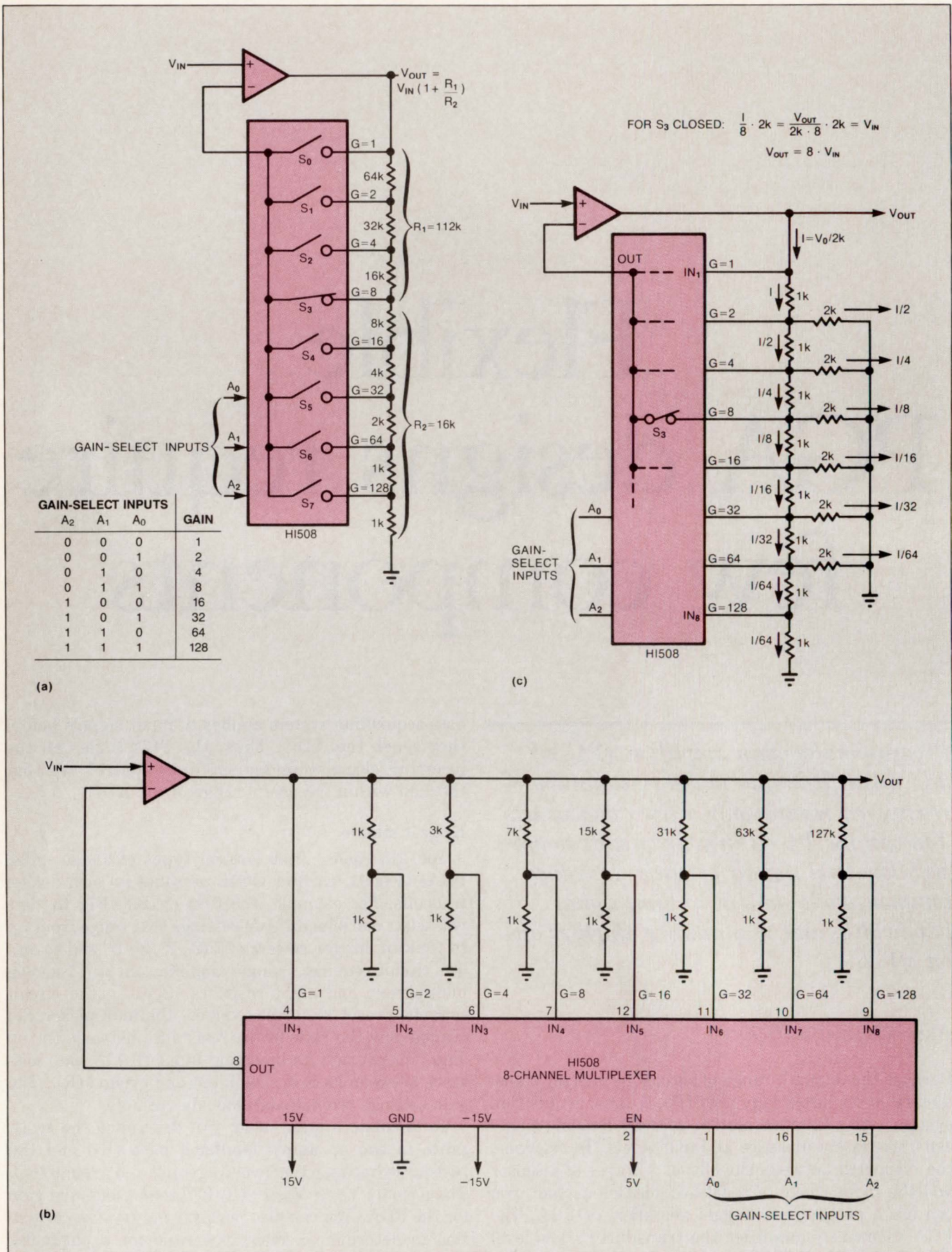
Because the dynamic range of signals from many transducers is so large (say, 80 dB), a data-acquisition system with a 12-bit resolution (a 72-dB dynamic range) can't accurately measure all input levels. To overcome the mismatch between the output voltages of a sensor and the input range of a data-acquisition system, you can use a programmable-gain amplifier, or PGA. The PGA accurately amplifies the transducer's low-level output signals so that a modest A/D converter can measure them with reasonable accuracy. A PGA with TTL- or CMOS-compatible control inputs lets you use your computer system to select the gain that the

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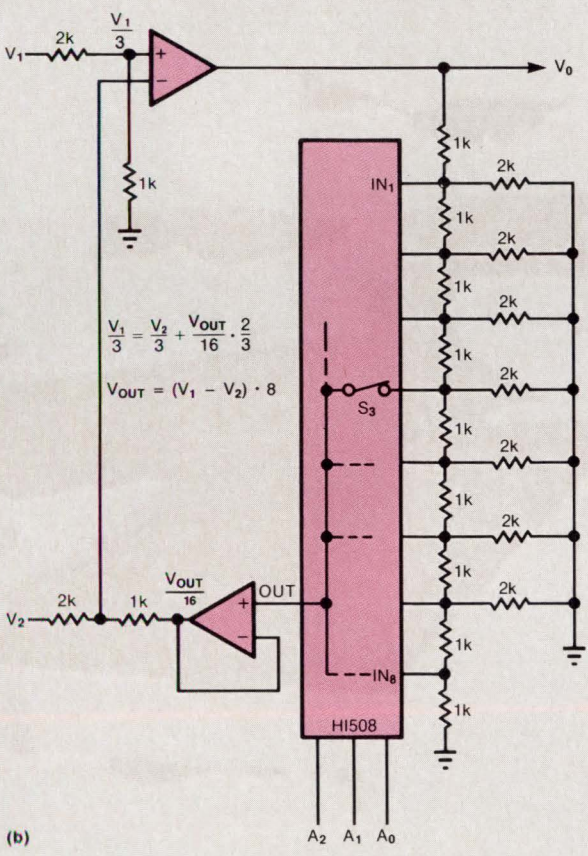
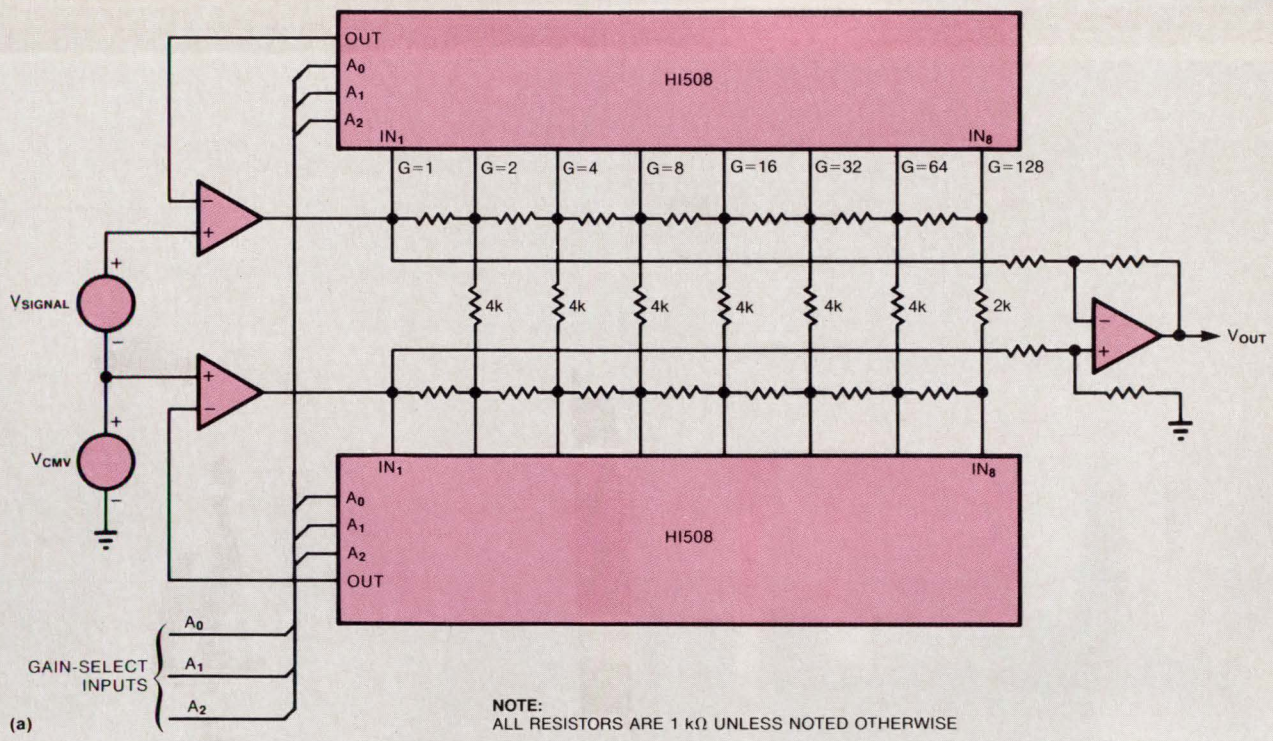
You can choose from several types of single-ended PGAs (Fig 1), each of which presents its own design tradeoffs. For example, the first circuit (Fig 1a) lets you select one of eight gain settings that range from  $1\times$  to  $128\times$  in integer powers of 2 ( $2^0$ ,  $2^1$ ,  $2^2$ ,  $2^3$ , and so on). The circuit requires a single amplifier, an 8-to-1 analog multiplexer, and eight resistors. Because the circuit contains preset resistance values, the multiplexer can change only the ratio of the resistance between the op amp's output and its inverting input ( $R_1$ ) to the resistance between its inverting input and ground ( $R_2$ ). The gain settings are not continuously variable.

To calculate a gain value, you determine the resistance in the op amp's feedback path ( $R_1$ ) and the resistance between the inverting input and ground ( $R_2$ ). The formula  $V_{OUT} = V_{IN}[1 + (R_1/R_2)]$  then yields the gain for the PGA. You can also perform the reverse calculation to determine a resistance ratio for a particular gain. In the example in Fig 1a,  $R_1$  equals 112 k $\Omega$  and  $R_2$  equals 16 k $\Omega$ . The gain for the PGA is 8, therefore. Because the analog multiplexer's switch is in series with the op amp's high-impedance noninverting input,



**Fig 1—Single-ended programmable-gain amplifiers (PGAs) require an op amp, an analog multiplexer, and resistors. The simplest PGA (a) supplies a feedback resistor and a resistor between the amplifier's output and ground. A second circuit (b) supplies individual resistor networks that minimize the effects of leakage currents in the multiplexer. An R-2R resistor ladder (c) minimizes both resistor errors and temperature-tracking effects.**





**Fig 2**—A differential PGA amplifies low-level signals while rejecting common-mode voltage and noise. You have a choice between two circuits that perform the same function. The first circuit (a) requires more components than does the second (b).

the switch's impedance doesn't affect the PGA's net gain.

The leakage current through each switch can induce significant errors in the amplifier's output, however. Such errors arise because the leakage path through an open switch completes a high-impedance connection to ground through the resistor network. A second single-ended PGA (**Fig 1b**) uses almost twice as many resistors as the first PGA circuit does. However, the overall circuit is less affected by the leakage current in the multiplexer's switches. In the second circuit, the leakage takes place through a much lower impedance, namely the 1-kΩ resistor in each pair that goes to ground. Leakage current in the analog multiplexer is approximately 300 pA at room temperature.

Both circuits suffer from having high resistance ratios (127k:1k, or 127:1) in their gain-determining networks. Higher gain settings would require an even larger range of resistor values—for example, 1024:1. You could use discrete resistors, but poor temperature tracking and parasitic impedances become problems in gain-determining networks that employ high resistance ratios. Such large resistance ratios are impractical for thin- or thick-film networks in hybrid circuits.

A third single-ended PGA (**Fig 1c**) also requires a 14-resistor network. However, instead of specifying a wide range of resistance values, you can construct a ladder network from a set of resistors that maintain a 2:1 resistance ratio. The use of resistors with R and 2R values in a ladder configuration improves the temperature-tracking characteristics of the network. Such precision resistor networks are readily available and are



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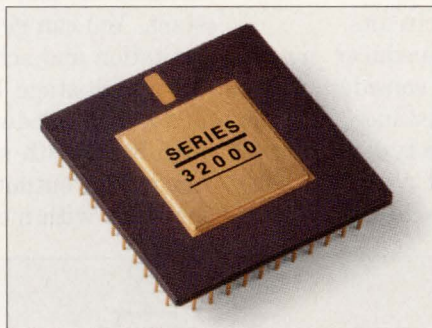
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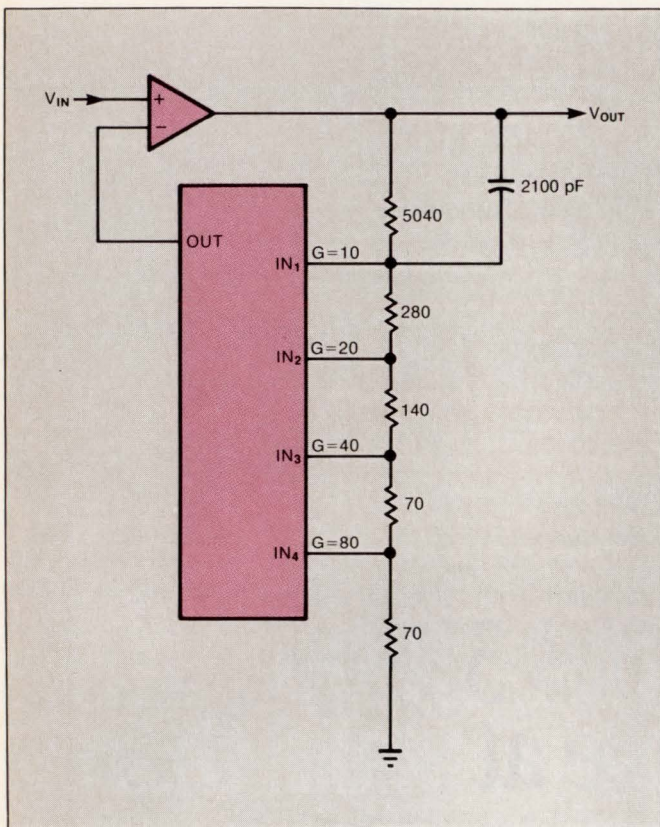
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**Fig 3**—A constant-bandwidth PGA lets you attenuate high-frequency signals that might add aliasing errors to your sampled signals. The amplifier above offers gains of 10, 20, 40, or 80.

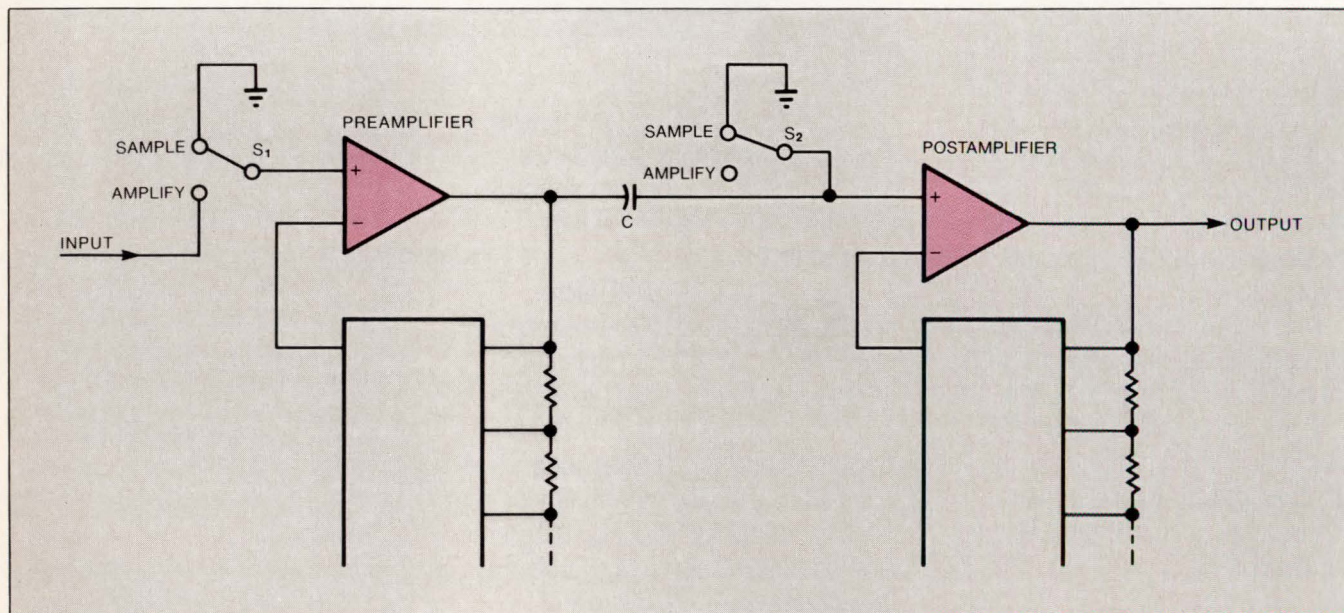
routinely fabricated for use in hybrid circuits.

In situations in which low-level transducer signals contain common-mode voltage or noise, consider using a differential-input PGA (Fig 2). For instance, you can use such a PGA with an iron constantan type-J thermocouple that generates only 95  $\mu\text{V}/^\circ\text{F}$  at room temperature. Before such a low-level signal reaches your data-

acquisition system, a differential PGA helps eliminate the common-mode voltage and noise that have become part of the thermocouple output.

If you add a PGA to a data-conversion system, remember that you can recover an original signal from a sampled signal as long as the sampling rate is at least  $2f$  samples/sec and the original signal contains no frequency component above  $f$  Hz. If the signal contains frequency components above the  $f$ -Hz limit, you may observe aliasing errors. To eliminate aliasing errors, therefore, the PGA must attenuate signals above the  $f$ -Hz limit for all its gain settings. For example, if the ADC operates at 30k samples/sec, the PGA that precedes it must maintain a constant 15-kHz bandwidth for all gain settings (Fig 3).

You can configure a single amplifier as a constant-bandwidth PGA as long as gain and bandwidth are relatively low. However, if you continue to increase a circuit's gain, you will ultimately reduce its bandwidth because the amplifier's gain-bandwidth product is constant. You can get around the gain-bandwidth product limitation and achieve a higher bandwidth by employing a multistage PGA. Each stage provides a low gain and a high bandwidth. By combining the low-gain and high-bandwidth stages, you obtain a high-gain, high-bandwidth output. The overall bandwidth ( $f_{\text{H}}^*$ ) for an amplifier with  $n$  equivalent stages is



**Fig 4**—By adding a capacitor between the stages of a multistage PGA, you can form a sample/hold circuit. The capacitor stores the offset voltage from the input amplifier and automatically sets it to zero when switches  $S_1$  and  $S_2$  are in their amplify positions, thus preventing the offset voltage of the preceding amplifier from saturating the following amplifier.

---

---

*A basic programmable-gain amplifier requires only an op amp, an analog multiplexer, and resistors.*

---

$$\text{OVERALL BANDWIDTH } (f^*_H) = \\ \text{SINGLE-STAGE BANDWIDTH } (f_H) \cdot \sqrt{2^n - 1},$$

where  $n$  is the number of amplifier stages.

In a multistage PGA, however, you can set a different gain, and thus a different bandwidth, for each stage. To compute the overall bandwidth for an amplifier with nonequivalent stages requires a more complex equation. The equation requires that you supply the single-stage bandwidth value for each amplifier:

$$\frac{1}{\sqrt{1 + (f^*_H/f_{H1})^2}} \cdot \frac{1}{\sqrt{1 + (f^*_H/f_{H2})^2}} \dots \\ \frac{1}{\sqrt{1 + (f^*_H/f_{Hn})^2}} = \frac{1}{\sqrt{2}}.$$

### Reduce offset voltage

Multistage PGAs have a drawback: The offset voltage of a preceding amplifier might saturate the amplifier that follows it. By inserting a capacitor between the stages (Fig 4), you form a sample/hold (S/H) stage. By periodically activating grounding switches  $S_1$  and  $S_2$ , the S/H circuit cancels the first amp's offset voltage.

To optimize the performance of the S/H circuit, you must use a good-quality capacitor with a Teflon, a polystyrene, or a polypropylene dielectric, all of which minimize dielectric absorption effects. A low-bias-current amplifier as well as low-leakage switches and a low-leakage capacitor minimize voltage droop in the S/H circuit. Proper circuit compensation and a good DMOS switch, such as the SD210, will minimize the charge transferred from the switch's gate to the hold capacitor. Keep in mind that the sample time must be sufficiently long to acquire the offset voltage.

### Consider using hybrid PGAs

Hybrid-circuit technology excels in the production of accurate and stable PGAs. To make such a PGA, a manufacturer assembles and interconnects an accurate R-2R resistor network, a CMOS multiplexer, an op amp, and discrete components on an alumina substrate. Because you select the circuit elements separately in this process, you can choose the best element for each intended function. For example, the resistor network can be either a thick- or a thin-film configuration that has been laser-trimmed so that it achieves 0.01% accuracy and a gain drift of  $<1$  ppm/ $^{\circ}$ C. Such a hybrid-

circuit configuration also lets you trim the op amp's input offset voltage and common-mode rejection ratio (CMRR) to produce a PGA that needs no adjustment.

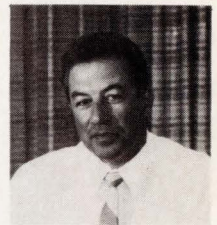
Finally, note that a CMOS analog multiplexer for use in a PGA must provide switches that have low leakage currents in both their on and off states. In general, CMOS switches change channels smoothly and thus shorten the settling time associated with each gain-switching operation.

**EDN**

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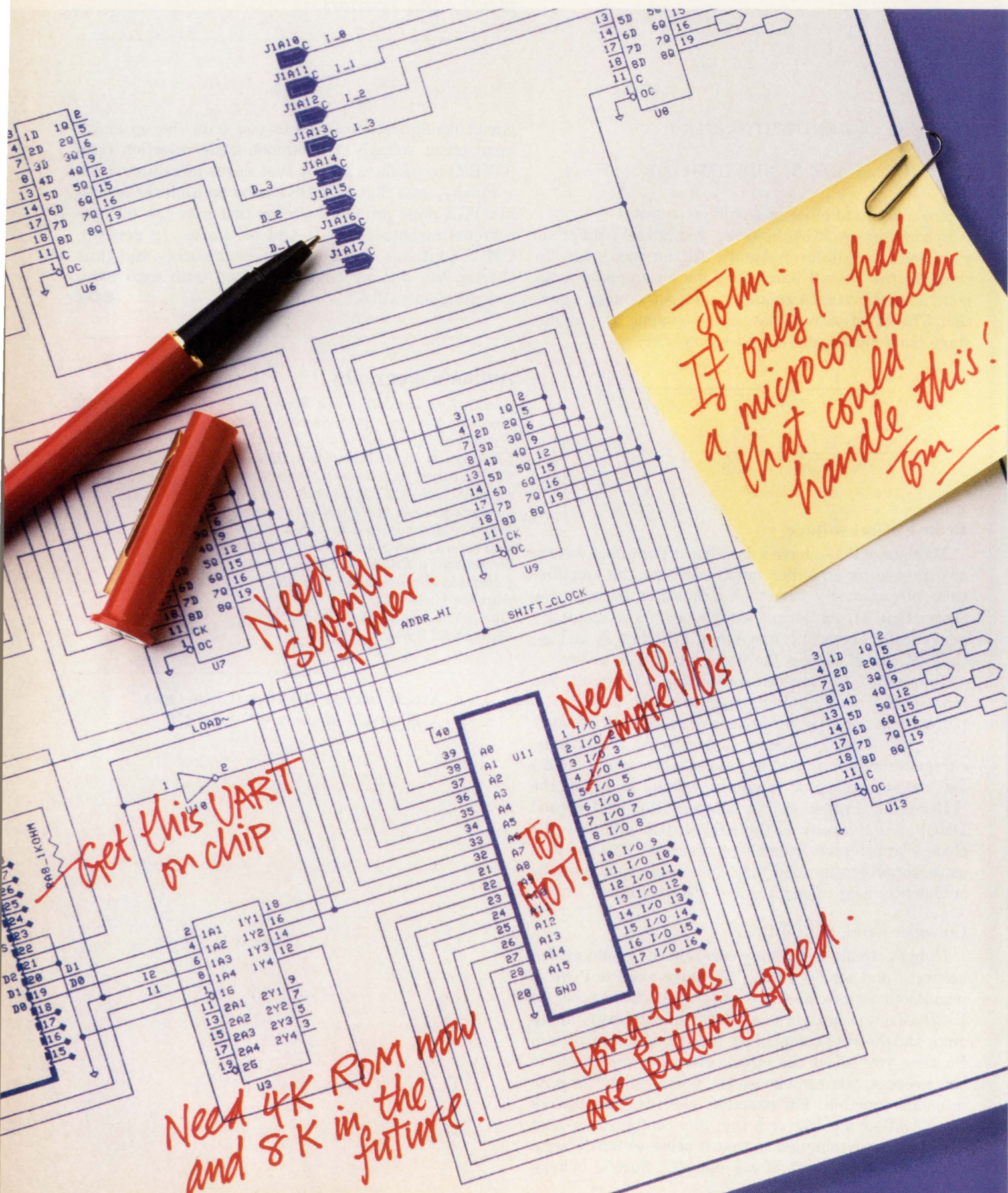
### Author's biography

*Akavia Kaniel worked as a design engineering manager at the microcircuits division of Intech Inc (Santa Clara, CA) when he wrote this article. His work involved supervising the development of electronic components and subsystems. Aki is the author of many technical articles, and he has a patent that covers analog measuring systems. He received a BSEE and MSEE from Columbia University and an MBA from the University of Santa Clara. During his leisure time, he enjoys sailing and flying.*



---

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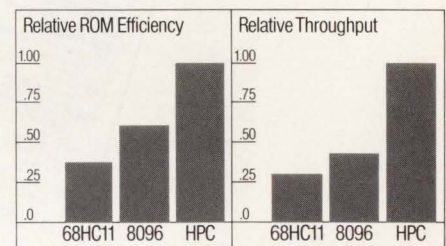
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# Product News

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### Enclosure makers respond to system-packaging needs

Doona Coos, Assistant Editor

Advances in the electronic industry have trickled down to affect every market, and slowly in company after company, the industry is responding with appropriate products in which enclosure packaging is a key element.

Technology Update

CMOS the choice for multiplying D/A converters

Tammi Harber, Staff Editor

Recent product introductions illustrate that CMOS has become the technology of choice for multiplying D/A converters (DACs). Demand for the propagation delay, low power to allow 4-out, low power to allow 4-out, as well as the ability to

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## EDN

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For Engineers' Professional Growth and Development

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COVER GALLERY ..... 1

**Seminar Service Helps EEs Cope With Technology Explosion**

By Michelle Cobb

Keeping abreast of the newest developments in technology is vital to an engineer's ability to survive in an increasingly competitive job market. Such knowledge shows that technical skills, particularly among engineers, becomes obsolete within five years. Ironically, two of the factors that contribute to that erosion—specialization and rapid technological advancement—characterize the high-tech industry.


First Seminar Service helps engineers find the appropriate courses to keep their technical courses to date. The service's database contains thousands of engineering seminars run by some of the most familiar education sources in the electrical engineering profession, including Worcester Polytechnic Institute, the Software Institute of America, the Institute for Advanced Technology, and the Center for Professional Development.

**Knowledge Network**

Founded by John Tammishele, a former Prime Computer training director, First Seminar Service has been in full operation for about one year. According to Tammishele, the service was created to serve as a network through which professionals could satisfy their continuing need for new knowledge. "An engineer's lifeblood is to know what the next best thing will be," he says. "Everything is constantly changing. How does an engineer keep up?"

**Riding the Fast-Growth Express**

By Kate Colburn



Engineers who work for fast-growing companies face considerable pressure, but many say the rewards are worth it.

"The biggest thrill is to be the only engineer on a project," says Scott McMurrow, manager of memory marketing and applications for Lattice Semiconductor in Ioverton, Ore. "I can't describe the high when you see the results of your efforts," says Laurie Lauchlin, senior development engineer for Integrated Device Technology, a semiconductor manufacturer in Santa Clara, Calif. These sentiments are echoed by engineers in a variety of companies. For hardware and software people, managers and recently hired graduates, interviewing, re-engineering department determine a company's ability to stay competitive in the marketplace." As Burroughs Corp., Detroit, Mich., director of employment Howard Owens explains, "Although business success is important, it's absolutely critical to company growth." Product cycle times are shortening, and there's tremendous pressure on product improvement built in hardware and software development," Owens states.

Regardless of size or age, all electronics companies must find ways to attract high-quality engineers and motivate and maintain them once they are on board.

**Creative Work Environment**


Assuring that salary and benefits packages are competitive, one of the most attractive qualities a company can boast is a creative work environment that allows and encourages engineers to take risks. Such an

**Engineers' Satisfaction a Key to Company Success**

By Marjorie Stender-Costanzo

Motivating engineers is vital for the health of any high-tech organization. Companies are finding more creative ways to attract and hold on to valuable EEs.

Top companies in the electronics industry are engineering talent as the key factor in maintaining their competitive edge. Says Roger Brown, vice president of industrial relations at Sanders Associates of Nashua, N.H., "The developments that come out of a progressive and innovative engi-





# IN ONE HOT NEWSPAPER... EDN NEWS

In January, EDN Product News and EDN Career News, EDN's two tabloid editions, merge to form EDN News... bringing you all the hottest news of products, technology, and careers.

## HOT NEWS OF PRODUCTS

The focus of EDN News is on hot products that will have the most powerful impact on the way you do your job. EDN News will cover the best products on the market, how they evolved, and why. Plus, it will now cover industry events (news of business, finance, economics) that drive product technology and hence product introductions.

## HOT NEWS OF CAREERS

In a separate section, EDN News will keep you abreast of professional developments and job openings in the electronics field. It will carry editorial aimed at your career and professional growth. Editorial that will help you find a job and keep it. Watch for your copy of EDN News arriving in the mail soon!

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News of Products, Technology and Careers for Engineers and Engineering Managers

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**DSP Board Fits IBM PC**

GE/Intersil's EVK-128 combines A/D conversion and FIR filtering

JEFF HAIGHT  
GE/Intersil, Inc.

As digital signal processing becomes simpler, cheaper, and more pervasive, the boundaries between design ideas and way for a more integrated approach to system development. Intersil's EVK-128 board, which occupies one slot in an IBM PC, incorporates analog processing techniques. The board works in such applications as PC-based analog or digital data-acquisition and digital filtering systems, finite-impulse-response (FIR) filter design and development systems, or as part of an FIR filter processor for off-line or non-real-time data. The system (Fig. 1, below) offers an active antialiasing filter, power-supply circuitry, A/D and D/A converters, and digital interfacing and control circuitry. The board also has FIR filtering circuitry and software plotting, and control. Documentation includes itemized parts lists, schematics, timing

The EVK-128 provides signal processing hardware and FIR filter design and modification software. You can copy all or part of the system for use in your own signal processor.

**Power MOSFET Makers Boost Electrical Specs**

Manufacturers improve electrical characteristics and offer a host of package types

TAMMI HARBERT  
Staff Editor

Recent power-MOSFET introductions offer lower on-resistance, higher voltage, factor switching, and innovations in onboard intelligence. Packaging improvements include greater electrical isolation and an increased availability of plastic and surface-mount parts.

Among the manufacturers of low-on-resistance devices are some companies well known in the power-MOSFET industry: Siliconix, Fairchild, International Rectifier, and General Instruments. New manufacturers—IXYS, for example, have also entered the arena.

**Low-on-resistance parts**

Made for applications requiring low on-resistance, Siliconix's SMM70N05 is built using the company's MOSPower-6 technology, which produces a chip density of 1.6M transistors/in<sup>2</sup>. The device has an 18-mΩ on-resistance with a 70A. The 50V SMM70N05, which follows on to the company's SMP6N05 and SMM60N05, is available in TO-3 packaging for \$10.11 (1000).

Like the SMM70N05, the SMP and SMM60N05 are 50V MOSPower-6 devices. Unlike the newer device, however, these parts offer current and on-resistance of 60A and 21 mΩ respectively. Another device

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**CAREERS**

### The Temptations of Tempering

Once confined to the clerical realm, tempering grows in popularity among EEs.

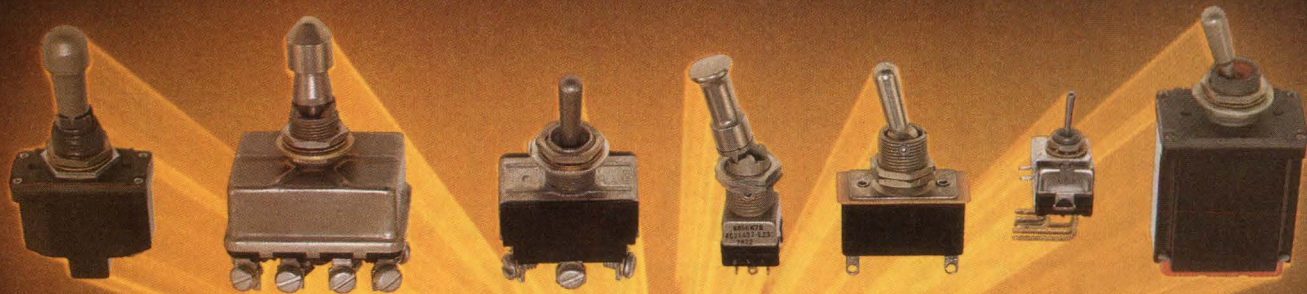
RUTH CLOOSTON

Chris Clark, a 30-year-old programming consultant from Hopkinton, MA, has worked as a contractor for six months. He started tempering because he wanted freedom and independence—he is developing his own software and needs to avoid the conflicts of interest

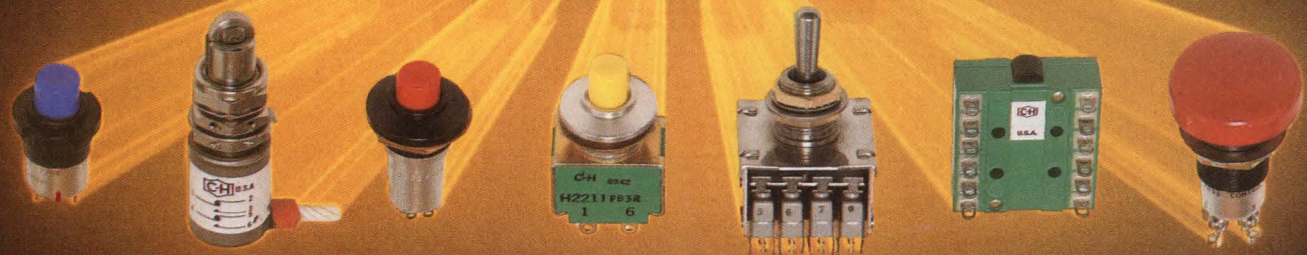
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**COMPANIES WITH EXPANDED OPTIONS**

EEs are increasingly being drawn toward tempering.



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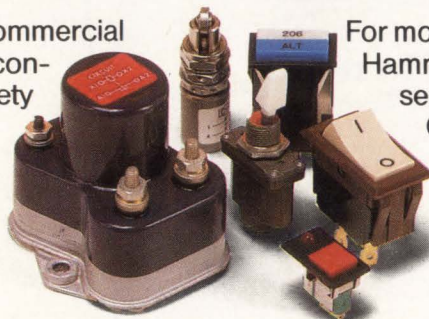
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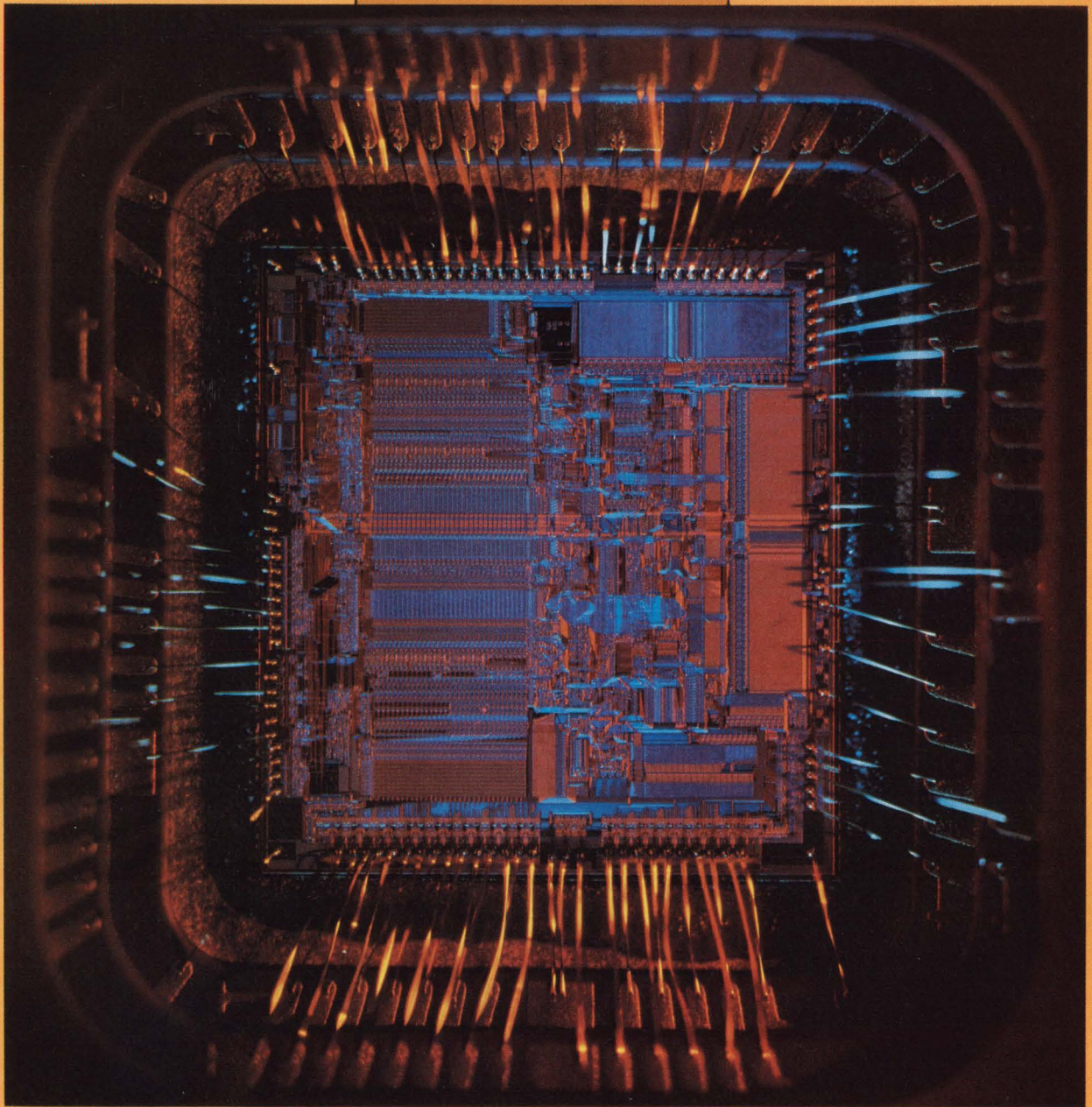
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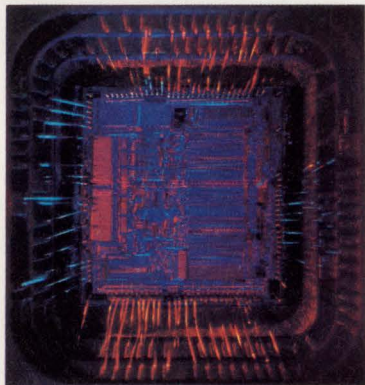
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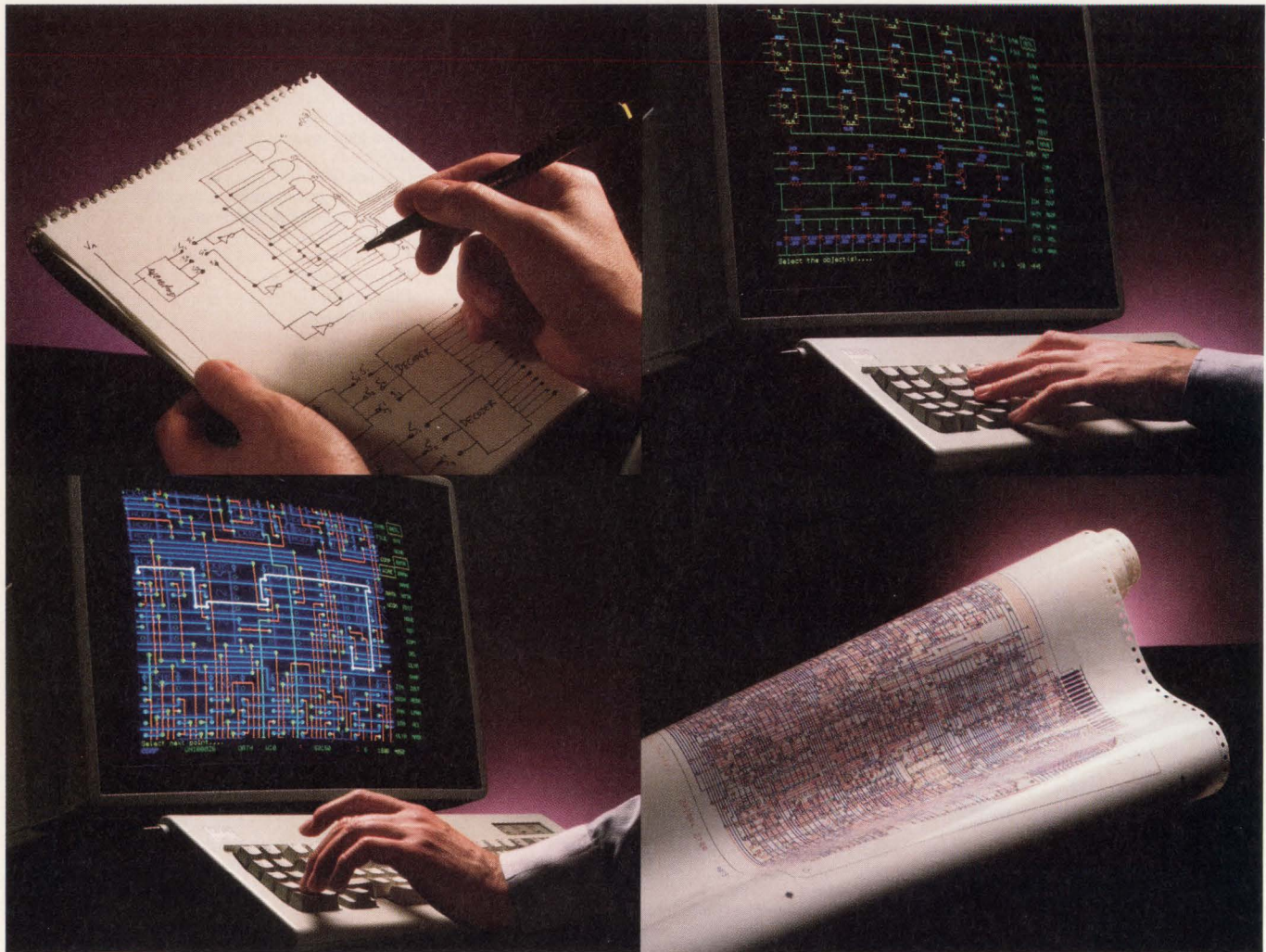
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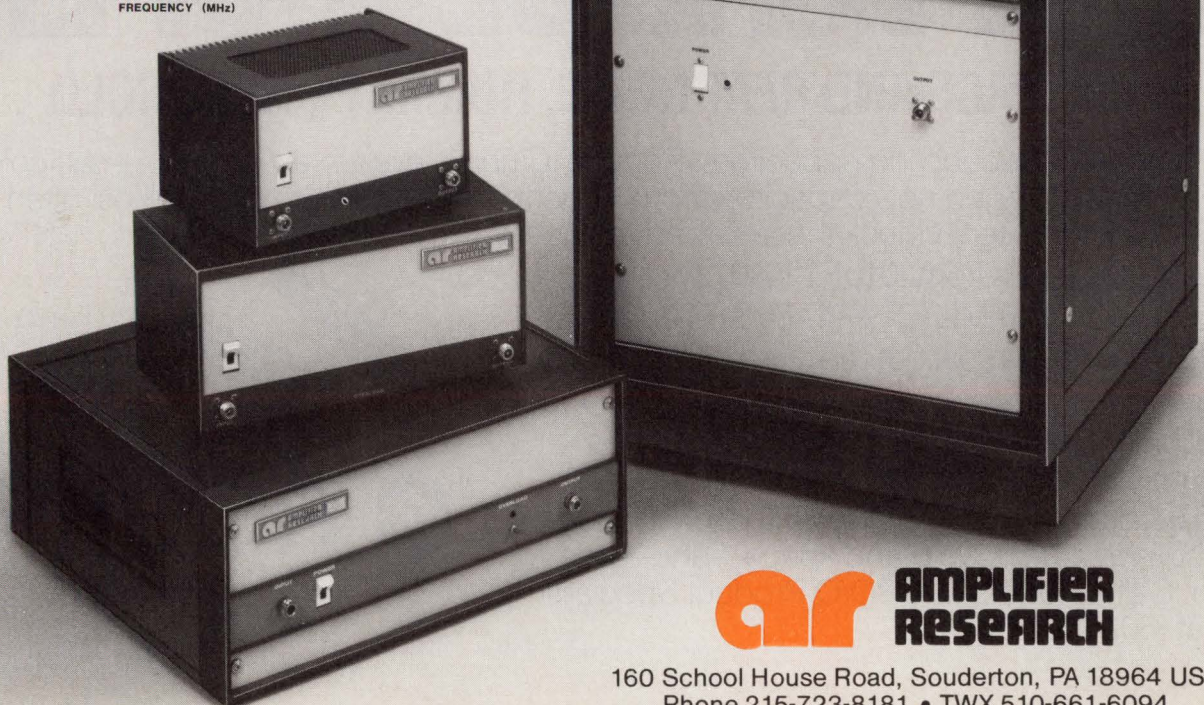
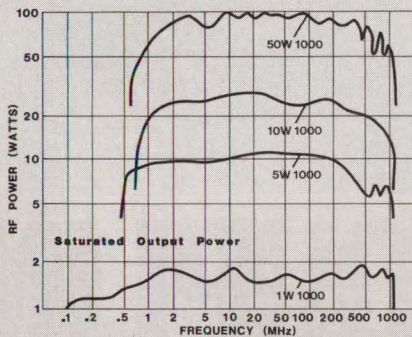
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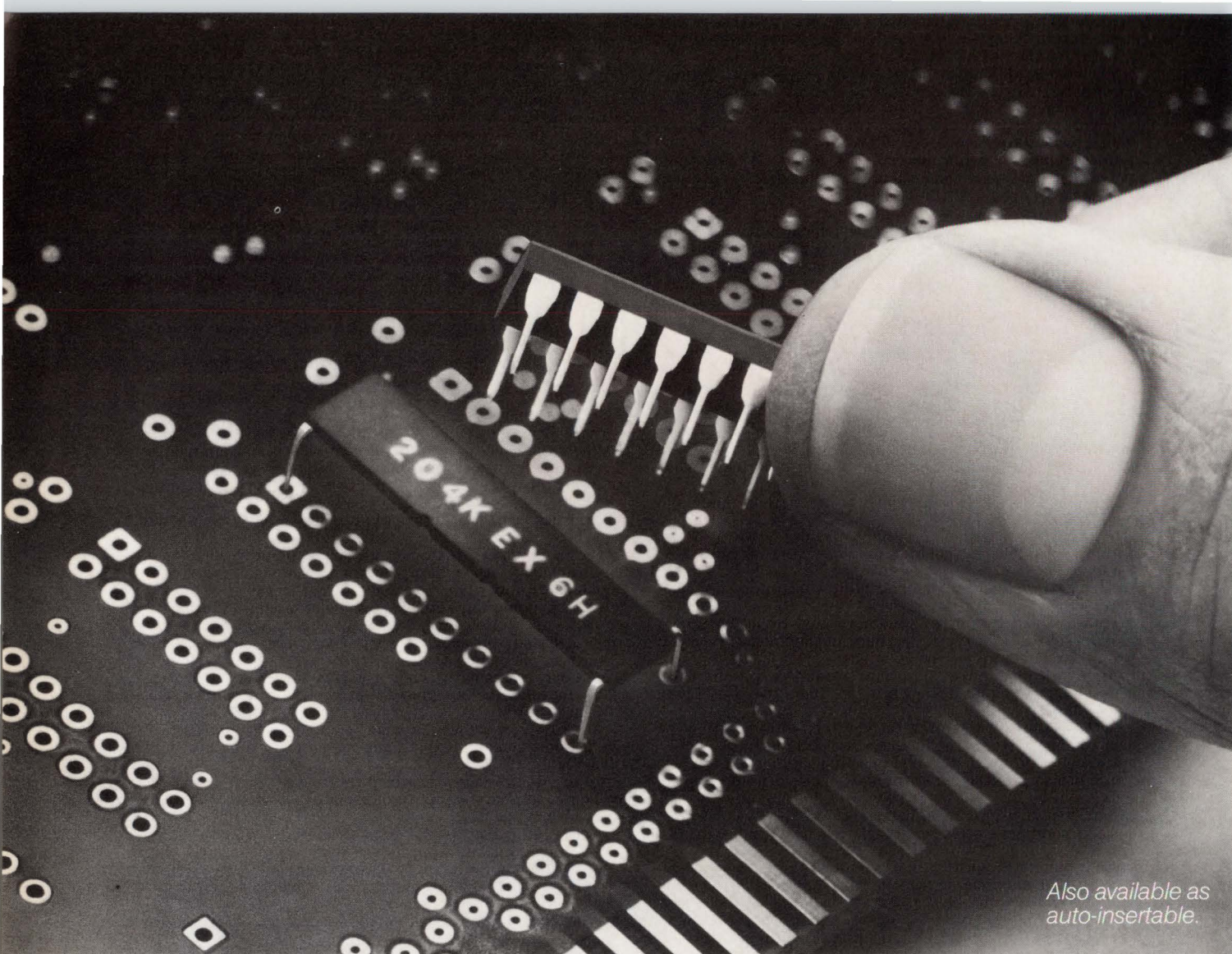
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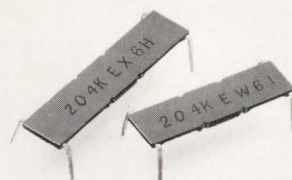
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- Powerful Unix-based workstations take on minicomputers, mainframes. *Weiss, Ray, Field Editor; Electronic Design, 05/15/86, pg 75, 4.5 pgs.*
- Task partitioning eases concurrent programming. *Brubaker, David, Brubaker Elec Consultants; Case, Don, Dest; Computer Design, 09/15/86, pg 83, 5 pgs.*
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- UNIX V gets locking, streams. *Meng, Brita, Technical Editor; Digital Design, 08/86, pg 29, 1.5 pgs.*
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- Computer security & crime**
- A new way to tighten security in PC networks. *Lineback, J Robert, Dallas Editor; Electronics, 10/30/86, pg 32, 1 pg.*
- Bootlegging on satellites turns out to be real problem. *Barney, Clifford, San Mateo Editor; Electronics, 05/05/86, pg 14, 1.5 pgs.*
- Computer software, application generator**
- The case for CASE. *Meng, Brita, Technical Editor; Digital Design, 06/86, pg 77, 4 pgs.*
- Computer software, communications/networking**
- Software makes nets transparent to users. *Rosenberg, Robert, Communications Editor; Electronics, 10/30/86, pg 36, 1 pg.*
- Computer software, data/file management**
- Second-generation CAE tools learn to share one data base. *Sullivan, Jerry S, Tektronix; Rummier, David C, Tektronix; Electronic Design, 07/10/86, pg 121, 5 pgs.*
- Computer software, design applications**
- A modular approach to real-time software. *Chao, Alfred, Software Components Grp; Computer Design, 10/01/86, pg 85, 4 pgs.*
- Analog-I/O boards and software for IBM PCs. *Conner, Margery S, Regional Editor; EDN, 06/12/86, pg 116, 16 pgs.*
- Automating logic design with Socrates. *Gregory, David, Calma; et al, Digital Design, 10/86, pg 44, 3 pgs.*
- Autorouters use sophisticated algorithms to lay out complex, multilayer pc boards. *Freeman, Eva, Associate Editor; EDN, 08/07/86, pg 67, 6 pgs.*
- Basic program eases analysis of phase-locked loops. *Rippy, Ron, EDN, 06/26/86, pg 157, 6 pgs.*
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- IBM PC-based software for CAE and CAD. *Freeman, Eva, Associate Editor; EDN, 09/18/86, pg 162, 12.5 pgs.*
- Low-cost PCs and software analyze analog circuits. *Travis, Bill, Senior Editor; EDN, 10/02/86, pg 163, 13 pgs.*
- Optimizing and verifying software in embedded systems. *Gary, Ted, Northwest Instrument Systems; Digital Design, 08/86, pg 58, 4 pgs.*
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- Pictures propel programming to a new plane. *Schindler, Max, Technology Editor; Electronic Design, 08/21/86, pg 94, 8 pgs.*
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- Programmable logic devices. *Smith, David, Associate Editor; EDN, 05/15/86, pg 94, 13 pgs.*
- Saber cuts spice out of analog simulation. *Staff; Electronics, 10/30/86, pg 80, 3 pgs.*
- Safeguarding analog designs against disaster. *Crosby, Brian C, Analog Design Tools; Wong, Ken, Analog Design Tools; Electronic Products, 06/16/86, pg 39, 6 pgs.*
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- Software packs power designs into analog CAE tool set. *Crosby, Brian C, Analog Design Tools; Tabrizi, Mehrdad, Analog Design Tools; Electronic Design, 09/04/86, pg 133, 3.5 pgs.*
- Spice improvements ease analog simulation. *LeBrun, Jean-Noel, Daisy Systems; Goshen, Raffy, Daisy Systems; Computer Design, 08/01/86, pg 97, 5 pgs.*
- Tester mockups and device libraries bring CAE to analog pc-board design. *Freeman, Eva, Associate Editor; EDN, 05/29/86, pg 49, 5 pgs.*
- The case for CASE. *Meng, Brita, Technical Editor; Digital Design, 06/86, pg 77, 4 pgs.*
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- Tools provide integration, measure performance. *Aseo, Joseph, West Coast Technical Editor; Digital Design, 09/86, pg 61, 2 pgs.*

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- Large-kernel convolutions in image processing. *Hall, Gene, Datacube; Digital Design, 08/86, pg 46, 3 pgs.*
- PC imaging software packs floating-point punch. *Molinari, John, Data Translation; Mulligan, John, Data Translation; Digital Design, 07/86, pg 50, 4.5 pgs.*
- Software is the challenge now in better graphics. *Manuel, Tom, Managing Editor; Electronics, 09/04/86, pg 95, 4 pgs.*
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- Pictures propel programming to a new plane. *Schindler, Max, Technology Editor; Electronic Design, 08/21/86, pg 94, 8 pgs.*
- Software. *Wolfe, Alexander, Software/Microsystems Editor; Electronics, 10/16/86, pg 74, 2 pgs.*

## Computer software, performance measurement

- Reliability and data management top SDI software concerns. *Hindin, Harvey, Special Features Editor; Computer Design, 07/86, pg 128, 1 pg.*
- Test hardware helps pinpoint software bugs. *Blakeslee, Thomas R, Orion Instruments; James, John S, Orion Instruments; EDN, 09/04/86, pg 169, 7 pgs.*

## Computer software, program development

- C compilers speed single-chip- $\mu$ P development. *Satten, Corey, John Fluke Manufacturing; EDN, 06/26/86, pg 213, 9.5 pgs.*
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- Software productivity moves upstream. *Wolfe, Alexander, Software/Microsystems Editor; Electronics, 07/10/86, pg 80, 7 pgs.*

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- Algorithm generates a list of combinations. *Capps, Charles P, General Motors; EDN, 05/15/86, pg 184, 0.5 pgs.*
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- Software provides indirect call for  $\mu$ C. *Moore, Allen, Sunstrand Data Control; EDN, 05/15/86, pg 188, 0.5 pgs.*
- Software provides rapid parity check. *Thompson, Jerold R, Sperry; EDN, 09/18/86, pg 316, 1 pg.*
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## Computer subsystems/peripherals, other

- Clock/calendar chips add system features; hybrid versions vie for memory sockets. *Leibson, Steven H, Regional Editor; EDN, 06/12/86, pg 73, 5 pgs.*

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- Computers. *Manuel, Tom, Managing Editor; Electronics, 10/16/86, pg 68, 4 pgs.*

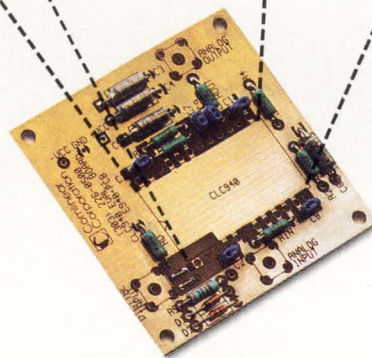
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- CAD tools detect EM emissions and heat. *Wilson, Dave, Executive Editor; Digital Design, 06/86, pg 19, 1 pg.*
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- Can Intergraph catch IBM in CAD/CAM market? *Leopold, George, Government & Military Editor; Electronics, 05/05/86, pg 48, 1.5 pgs.*
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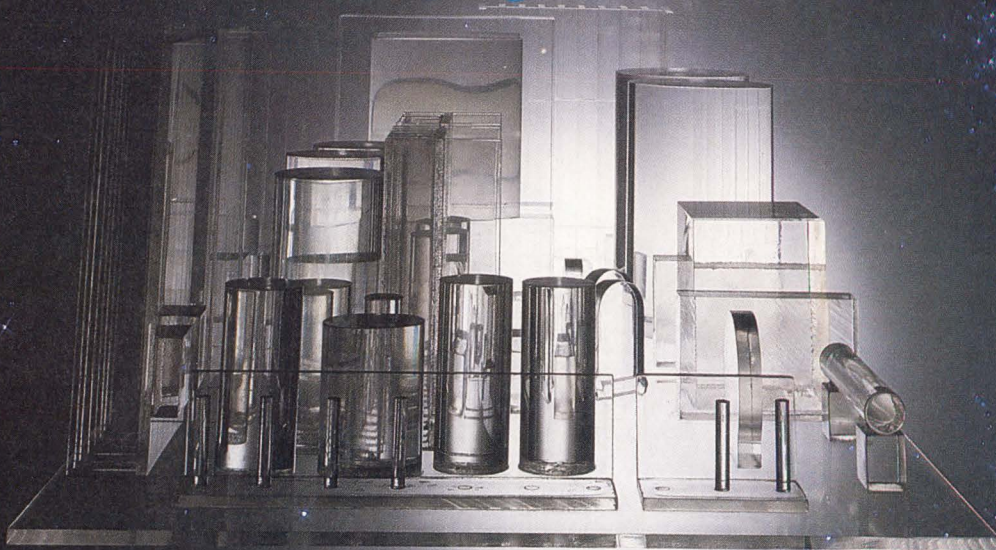
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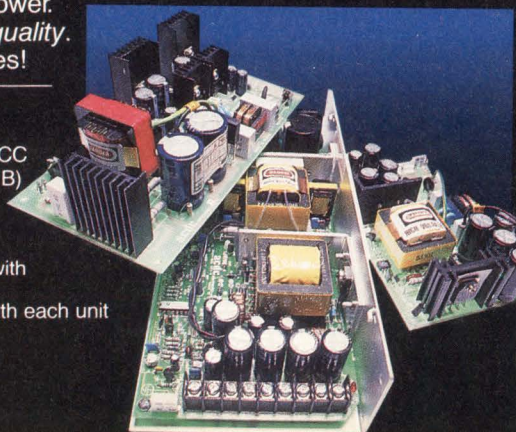
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RBO131	135W	+5V 15A	+12V 4A	-12V 0.7A	-5V 0.7A	(L)	5.0x10.5x2.5
RBO132	135W	+5V 15A	+15V 3.2A	-15V 0.7A	-5V 0.7A	(L)	5.0x10.5x2.5
RBO133	135W	+5V 15A	+12V 3A	-12V 0.7A	+24V 1.5A	(L)	5.0x10.5x2.5
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- Integrating CAE, CAD and CASE. *Marshall, John, Hewlett-Packard; Van Dyne, Denese, Hewlett-Packard; Digital Design, 06/86, pg 40, 4.5 pgs.*
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In 1,500 centuries, this clock will lose 1 second. *Gosch, John, Frankfurt Editor; Electronics, 10/30/86, pg 38, 1 pg.*  
Plessey chips will run wristwatch pager. *Waller, Larry, Los Angeles Editor; Electronics, 09/18/86, pg 42, 0.5 pgs.*  
The fight over formats will be fierce at CES. *Iversen, Wesley, Industrial & Consumer Editor; Electronics, 06/02/86, pg 44, 2 pgs.*  
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Zenith TV sounds better with folded waveguide. *Rosenberg, Robert, Communications Editor; Electronics, 08/21/86, pg 40, 1 pg.*

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AMD trims sails as slump hits home. *Barney, Clifford, San Mateo Editor; Electronics, 08/21/86, pg 31, 1 pg.*  
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Can Intergraph catch IBM in CAD/CAM market? *Leopold, George, Government & Military Editor; Electronics, 05/05/86, pg 48, 1.5 pgs.*  
Can Japan catch up in 32-bit microprocessors? *Cole, Bernard C, Semiconductors Editor; Cohen, Charles L, Tokyo Editor; Electronics, 05/12/86, pg 41, 5 pgs.*  
Can Toshiba make it big in information systems? *Berger, Michael, World News Chief; Electronics, 07/24/86, pg 109, 4 pgs.*  
Can Zilog-AT&T team score in the 32-bit race? *Erikson, Arthur L, Executive Editor; Electronics, 05/19/86, pg 19, 1 pg.*  
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DOD spurs VHSIC efforts with 'advance agreements.' *Waller, Larry, Los Angeles Editor; Electronics, 09/04/86, pg 29, 1.5 pgs.*  
First it was the Yugo, now it's the Iskra VME. *Rosenberg, Robert, Communications Editor; Electronics, 05/05/86, pg 49, 0.5 pgs.*  
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Industry splits on what Computer III adds up to. *Leopold, George, Government & Military Editor; Electronics, 05/26/86, pg 18, 1 pg.*  
Intel pumps new life into Multibus I line. *Rose, Craig, Boston Editor; McLeod, Jonah, Managing Editor; Electronics, 10/16/86, pg 34, 0.5 pgs.*  
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The toughest fight yet for Monolithic Memories. *Kozma, Robert J, Business Editor; Electronics, 05/19/86, pg 68, 1 pg.*  
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## Current sources

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# D

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## Data-communications systems/techniques

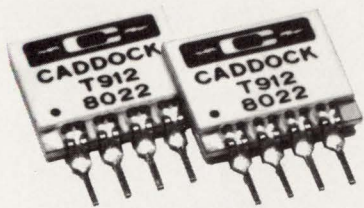
Board-level modems boast higher speeds, more features and lower cost. *Cashen, Frank, Contributing Editor; Computer Design, 07/86, pg 40, 4.5 pgs.*  
Communications board speeds network integration. *Lafreniere, Bernard, Systech; Computer Design, 05/01/86, pg 89, 4.5 pgs.*  
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VMEbus boards handle X.25-based packet-switched communications. *Mitch Beedie, Field Editor; Electronic Design, 06/12/86, pg 57, 4 pgs.*

## Data converters

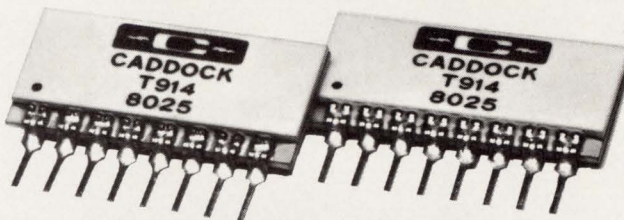
ADC chips leap ahead both in speed and accuracy. *Goodenough, Frank, Senior Editor; Electronic Design, 09/04/86, pg 90, 8 pgs.*  
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Synchronous V/F converter aids linearity in data acquisition. *DeVito, Larry, Analog Devices Semiconductor; EDN, 10/16/86, pg 183, 6 pgs.*



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Type T912 Ultra-Precision Resistor Network 'Pairs'

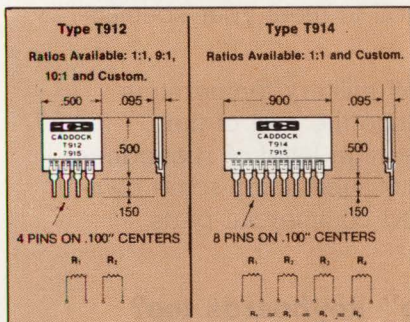


Type T914 Ultra-Precision Resistor Network 'Quads'

**Type T912 / T914 Ultra-Precision Resistor Networks are constructed with Caddock's Tetrinox™ resistance films to achieve all of these high performance characteristics:**

- **Absolute Tolerance:** 0.1% for all resistors.
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- **Shelf Life Stability of Ratio for Six Months:** Within ±0.005%.

This exceptional combination of performance specifications – and the compact, plug-in configuration of the Type T912/T914 precision resistor 'pairs' and 'quads' – provide the single-package

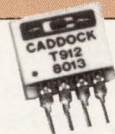
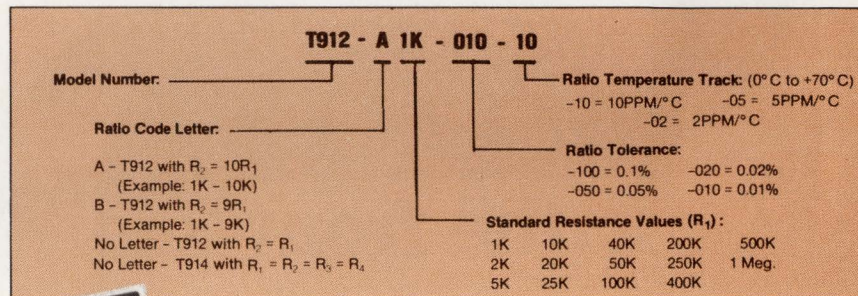


matched resistor characteristics and stability required by high-accuracy analog circuits, including –

- Precision analog amplifiers.
- Voltage reference circuits.
- Instrumentation bridge circuits.
- Voltage and current comparison circuits.

**Standard models of Type T912 / T914 precision resistor 'pairs' and 'quads' include 14 off-the-shelf resistor values with a wide choice of Ratio Tolerances, Ratio TCs and Resistance Ratios:**

This standard part number provides a selection of over 500 in-production models of Type T912/T914 precision resistor 'pairs' and 'quads':

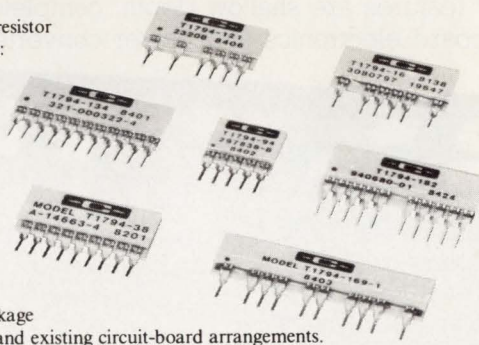


As an example of the price/performance advantages of this advanced resistor technology, the Model T912-A1K-010-10 shown here provides a 1K-10K resistor 'pair' with a ratio tolerance of ±0.01% and a ratio temperature coefficient of 10 PPM/°C at a 1000-lot unit price under \$2.66. The same resistor 'pair' with a ratio tolerance of ±0.1% delivers at a 1000-lot unit price under \$1.52!

## Type T1794 Custom Precision Resistor Networks meet special circuit and packaging requirements:

The Type T1794 custom precision resistor networks provide a unique range of flexibility:

- From 2 to 15 resistors per assembly.
- Absolute tolerances from 1.0% to 0.05%.
- Custom voltage and power ratings.
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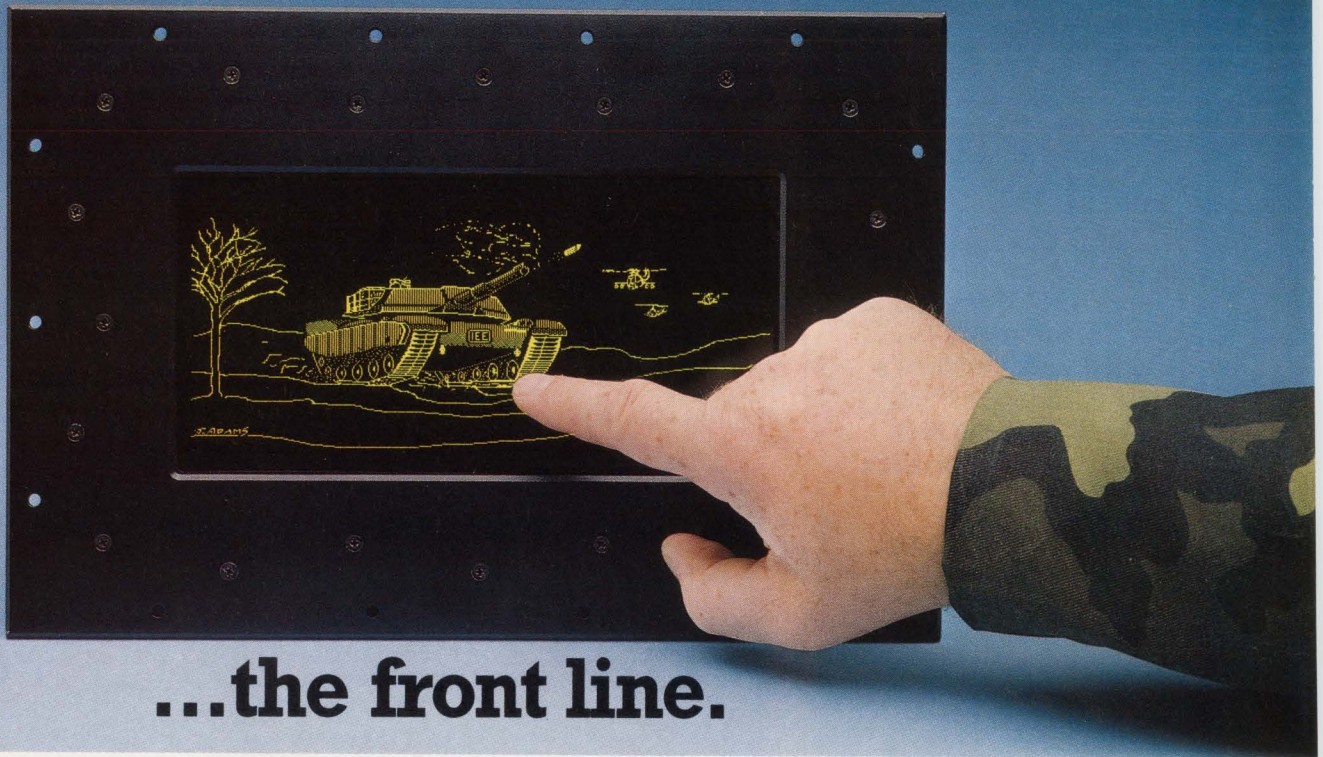
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## Fiber optics

A low-cost way to build a fiber-optic local-area net. *Staff; Electronics, 06/02/86, pg 36, 2 pgs.*

Fiber optics. *Biancomano, Vincent, Technology Editor; Electronic Design, 07/10/86, pg 74, 5.5 pgs.*

Fiber optics points way to speed divergent networks. *Mokhoff, Nicolas, Senior Editor; Computer Design, 08/01/86, pg 48, 2 pgs.*

French find easier way to build fast photodiode. *Gallagher, Robert T, Paris Editor; Electronics, 06/02/86, pg 15, 0.5 pgs.*

High-performance chips drive optical fibers to their limit. *Spadaro, Joseph J, Associate Editor; Electronic Products, 06/02/86, pg 63, 4 pgs.*

The next step for MAP: fiber-optic networks. *Iversen, Wesley R, Industrial & Consumer Editor; Electronics, 10/02/86, pg 36, 0.5 pgs.*

Time-domain reflectometers tackle fiber-optic cabling. *Michaels, Ian, Electronic Design, 08/07/86, pg 59, 3 pgs.*

## Filter circuits

A/Ds and D/As team to make adaptive filters. *Byrne, Mike, Analog Devices; Minogue, Paschal, Analog Devices; Electronic Products, 09/02/86, pg 53, 5.5 pgs.*

Analog filters come as gate arrays or standard ICs. *Roche, Jean-Pierre, Thomson Semiconducteurs; Caillon, Christian, Thomson Semiconducteurs; Electronic Design, 10/16/86, pg 143, 5 pgs.*

Chopper amp provides low-offset filter. *Hoskins, Kevin, National Semiconductor; EDN, 08/07/86, pg 204, 1 pg.*

Controller chip builds flexible FIR filters. *Bursky, Dave, Associate Managing Editor; Electronic Design, 09/18/86, pg 61, 3 pgs.*

DSP-filter software offers design help to novices. *Cushman, Robert H, Special Features Editor; EDN, 07/10/86, pg 152, 11 pgs.*

Filter IC performs signal demultiplexing. *Denton, Smaragda, National Semiconductor; EDN, 10/16/86, pg 226, 1 pg.*

Programmable filter chip and its PC-based tools offer new analog solutions. *Dille, Thomas, Crystal Semiconductor, et al; Electronic Design, 05/29/86, pg 147, 5.5 pgs.*

Programmable switched-capacitor filter ICs cut component count in many filter types. *Cormier, Denny, Regional Editor; EDN, 06/26/86, pg 71, 6 pgs.*

## Finance

Despite doubts, industry backs Senate tax bill. *Leopold, George, Government & Military Editor; Electronics, 05/19/86, pg 19, .5 pgs.*

U.S. midyear market report. *Barney, Clifford, San Mateo Editor, et al; Electronics, 07/10/86, pg 105, 7 pgs.*

## Flip flops

IC forms an edge-sensitive R-S flip-flop. *Murugesan, S, ISRO Satellite Ctr; EDN, 10/02/86, pg 204, 0.5 pgs.*

## Floppy-disk drives

Analog testing and PC hosts boost the capabilities of Winchester disk testers. *Leibson, Steven H, Southwestern Editor; EDN, 05/01/86, pg 71, 4.5 pgs.*

Half-height rigid disk drives fill the void. *Aseo, Joseph, West Coast Technical Editor; Digital Design, 09/86, pg 20, 1 pg.*

IBM lights a fire under the 3½-in. disk. *Naegele, Tobias, New York Editor; Electronics, 05/05/86, pg 15, 0.5 pgs.*

## Function generators/generation

Use a PC to generate analog output signals. *Croteau, John, Analog Devices; Grant, Doug, Analog Devices; EDN, 05/15/86, pg 131, 10 pgs.*

## Fuses

AC circuit breaker has adjustable threshold. *French, Kurt, C F Electronics; EDN, 06/12/86, pg 211, 1 pg.*

# G

## GPIB instruments

Lab/benchtop power supplies offer a wide range of functions. *Text continued on pg 215*

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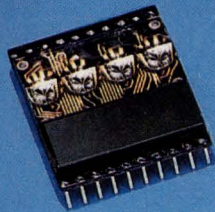
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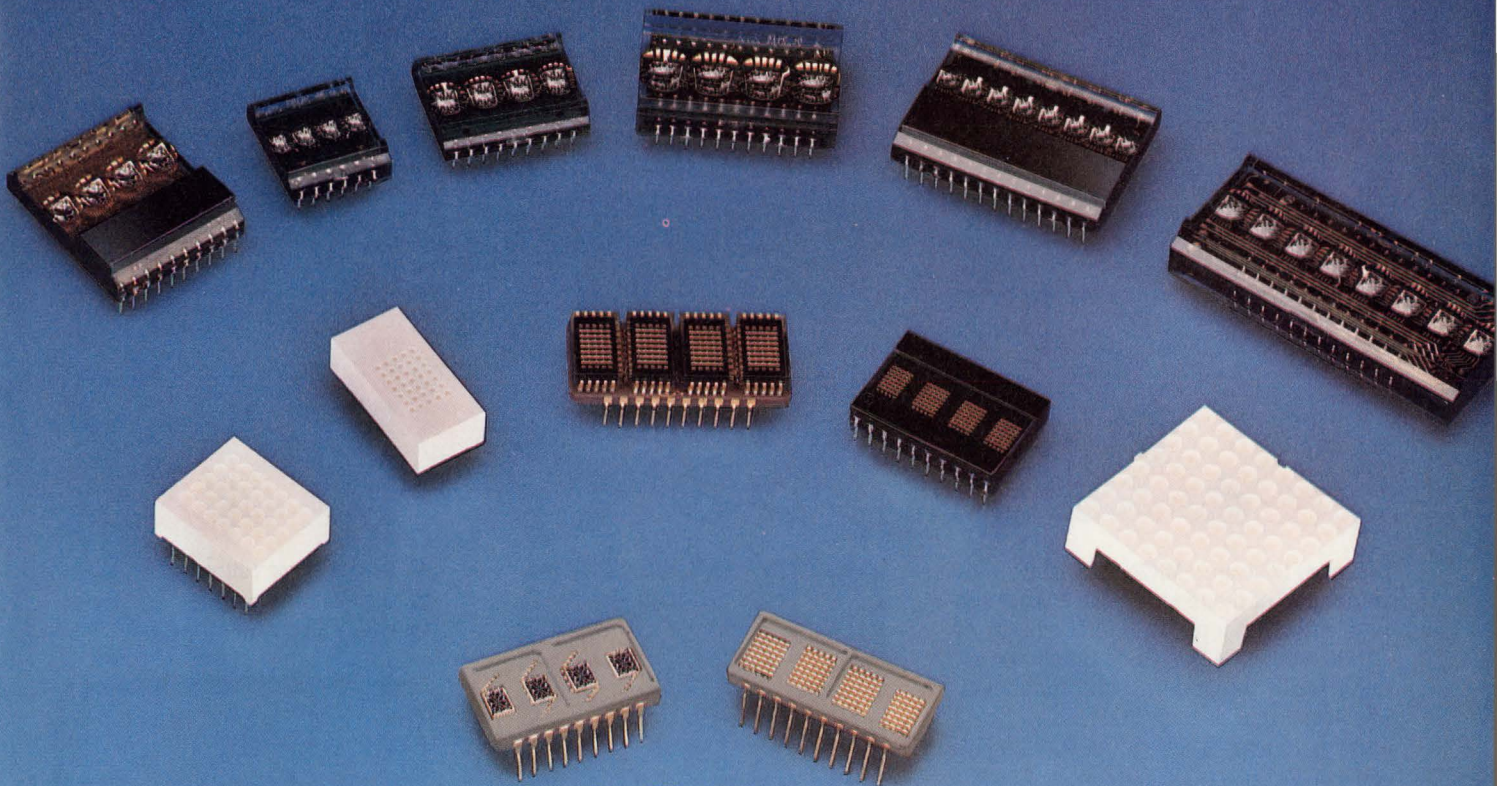
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1987

	Siemens ("us")	"them"
10 years experience	YES	not even close
Continual product refinement and evolution	YES	NO
Over 10 million unit hours of testing	YES	NO
100% burn-in (standard)	YES	NO
Choice of 32 different devices	YES	Only 3 types
Dot matrix font	YES	NO
Choice of colors	YES	NO
History of volume on-time deliveries	YES	NO
New software-programmable displays	YES	NO
Custom capabilities	YES	Limited

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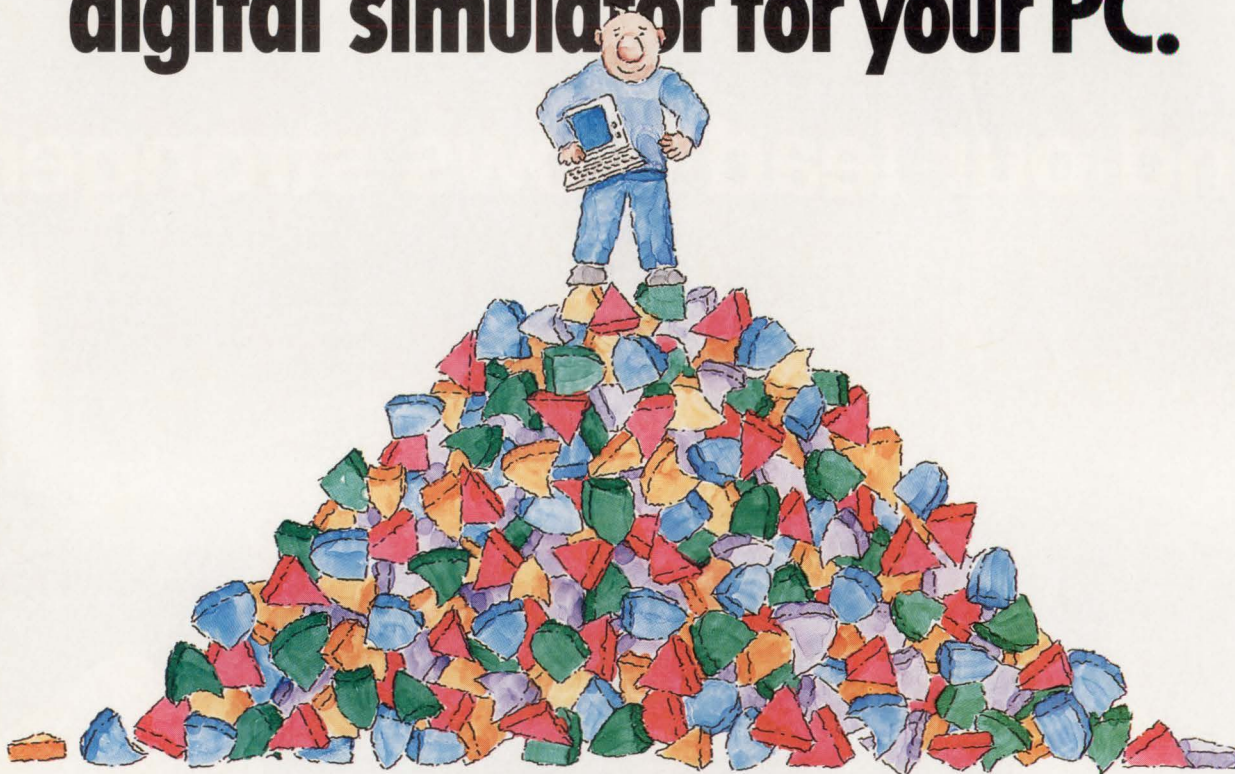
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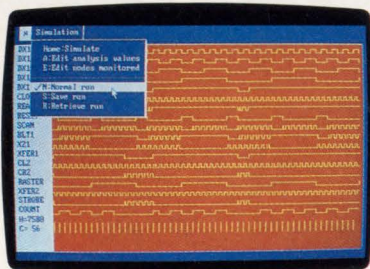
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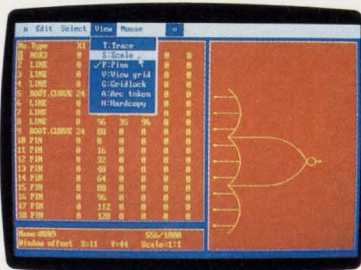
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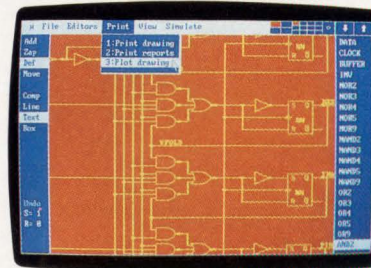
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# EDN TECHNICAL-ARTICLE DATABASE

Mosley, J D, Regional Editor; EDN, 07/10/86, pg 186, 8 pgs.

## GaAs technology

Bit-slice ICs kick off era of commercial GaAs LSI. Staff; *Electronics*, 09/18/86, pg 61, 4 pgs.

Controllers turn to GaAs for 2048x2048 displays. Wilson, Andrew, Senior Technical Editor; *Digital Design*, 09/86, pg 23, 1 pg.

Examine and verify GaAs IC performance. Pengue, Louis, *TriQuint Semiconductor*; Walters, Eldon, *Tektronix*; EDN, 08/21/86, pg 127, 9.5 pgs.

GaAs LSI goes commercial. Cole, Bernard C, Managing Editor; *Electronics*, 09/18/86, pg 57, 4 pgs.

GaAs RISC processor is in the works. Lineback, J Robert, Dallas Editor; *Electronics*, 06/09/86, pg 21, 1.5 pgs.

GaAs gains ground against CMOS and bipolar techniques. Marrin, Ken, Senior Editor; *Computer Design*, 07/86, pg 131, 3.5 pgs.

GaAs pushes bit slice to new performance levels. Kates, Geoffrey, Contributing Editor; *Computer Design*, 08/15/86, pg 26, 2 pgs.

Gallium Arsenide—a semicustom approach. Wilson, David, Executive Editor; *Digital Design*, 06/86, pg 89, 3 pgs.

High-speed logic ICs. Cormier, Denny, Regional Editor; EDN, 08/21/86, pg 112, 9 pgs.

Microwave and digital circuits are combined on one GaAs chip. Waller, Larry, Los Angeles Editor; *Electronics*, 10/02/86, pg 31, 1 pg.

Subnanosecond silicon ECL gate arrays face challenge from GaAs and CMOS. Bursky, Dave, Associate Managing Editor; *Electronic Design*, 06/12/86, pg 74, 8 pgs.

TI builds 1-K static ram in GaAs-on-silicon. Lineback, J Robert, Dallas Editor; *Electronics*, 09/18/86, pg 31, 1.5 pgs.

The race is on to develop microwave GaAs ICs for DOD. Waller, Larry, Los Angeles Editor; *Electronics*, 10/30/86, pg 29, 1 pg.

## Gate arrays

A bipolar gate array that runs fast on low power. Staff; *Electronics*, 10/02/86, pg 68, 4 pgs.

A new, easy way to design ASICs. Staff; *Electronics*, 10/16/86, pg 53, 5 pgs.

Checking out VLSI with standard test gear. Staff; *Electronics*, 05/26/86, pg 33, 3 pgs.

Customizing a gate array, Part 2: verifying and laying out the design. Gabay, Jon, Associate Editor; *Electronic Products*, 06/02/86, pg 50, 9 pgs.

Customizing a gate array, Part 3: along the road to final silicon. Gabay, Jon, Associate Editor; *Electronic Products*, 07/15/86, pg 52, 5 pgs.

Digital analysis system wears many hats. Bennett, David L, *Tektronix*; *Electronic Products*, 07/15/86, pg 58, 8 pgs.

ECL gate arrays emerge as speed and density contenders. Marrin, Ken, Senior Editor; *Computer Design*, 10/15/86, pg 31, 7 pgs.

From testable, soft macrocells springs an 8000-gate array. Wick, David G, Honeywell Digital Products Center, et al; *Electronic Design*, 10/16/86, pg 155, 3.5 pgs.

Gate arrays make an end run around military red tape. Waller, Larry, Los Angeles Editor; *Electronics*, 10/16/86, pg 31, 1 pg.

Gate-array compiler cuts big designs down to size. Well, Steven, FutureNet Division, Data I/O, et al; *Electronic Design*, 06/26/86, pg 101, 5.5 pgs.

How designers can save time in laying out a sea of gates. Staff; *Electronics*, 10/30/86, pg 77, 3 pgs.

How Motorola moved BiMOS up to VLSI levels. Staff; *Electronics*, 07/10/86, pg 67, 4 pgs.

IC emulates many types of logic gates. Christner, Kurt W, EDN, 09/04/86, pg 212, 1.5 pgs.

Laser-customized gate arrays in 24 hours. Collett, Ronald E, Senior Technical Editor; *Digital Design*, 05/86, pg 24, 2 pgs.

Linear and digital ASICs converge on same silicon chips. Leonard, Milt, Northwestern Editor; *Electronic Products*, 05/01/86, pg 50, 5 pgs.

New test tools help solve prototype verification problems. Goering, Richard, Senior Editor; *Computer Design*, 10/15/86, pg 61, 13 pgs.

Novel architectures give these chips new speed and capacity. Panasuk, Curtis, Field Editor; *Electronic Design*, 10/16/86, pg 94, 6 pgs.

PAL devices help smooth design of gate array's macrocells. Jaeger, Kent, *Monolithic Memories*; *Electronic Design*, 10/16/86, pg 123, 4.5 pgs.

Sea-of-gates array puts 75% of its gates to use. Cole, Bernard,

Managing Editor; *Electronics*, 10/16/86, pg 38, 0.5 pgs.

Sierra's new simulator speeds up ASIC design. Staff; *Electronics*, 10/16/86, pg 60, 3 pgs.

Standard-cell libraries expand. Winard, Harold, *Electronic Design*, 09/11/86, pg 179, 6 pgs.

Stretching the limits of ASIC software. Cole, Bernard C, *Semiconductors Editor*; *Electronics*, 06/23/86, pg 34, 5 pgs.

Subnanosecond silicon ECL gate arrays face challenge from GaAs and CMOS. Bursky, Dave, Associate Managing Editor; *Electronic Design*, 06/12/86, pg 74, 8 pgs.

Timing verification predicts performance of logic arrays. Franz, Michael, *Applied Micro Circuits*; EDN, 06/12/86, pg 161, 8.5 pgs.

Vendors stock standard-cell libraries with linear and LSI-level functions. Smith, David, Associate Editor; EDN, 10/02/86, pg 63, 7.5 pgs.

Why silicon compilers are starting to take off. McLeod, Jonah, Managing Editor; *Electronics*, 07/24/86, pg 72, 6 pgs.

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Scots, Irish no longer court just any firm. Waller, Larry, Los Angeles Editor; *Electronics*, 05/05/86, pg 24, 1 pg.

Trade pact hits fast as prices soar on some Japanese ICs. Barney, Clifford, San Mateo Editor; Berger, Michael, World News Chief; *Electronics*, 08/21/86, pg 79, 2 pgs.

## Graphics boards

Boards that meet EGA spec bring flexible graphics capability to IBM PC workstations. Conner, Margery S, Regional Editor; EDN, 09/18/86, pg 75, 6 pgs.

CRT display circuit eliminates need for controller chip. Davidian, David, NEC Electronics; EDN, 06/26/86, pg 185, 11.5 pgs.

IBM graphics add-ons—emulating aameleon. Wilson, Andrew, Senior Technical Editor; *Digital Design*, 07/86, pg 27, 2 pgs.

Image-processing boards boost real-time performance. Molinari, John, Data Translation; Dizenzo, Anthony, Data Translation; *Computer Design*, 05/15/86, pg 75, 5 pgs.

Livelier graphics—the bit-slice bonus. Kondraske, George V, University of Texas at Arlington, et al; *Electronic Products*, 09/16/86, pg 54, 8 pgs.

## Graphics circuits

CRT display circuit eliminates need for controller chip. Davidian, David, NEC Electronics; EDN, 06/26/86, pg 185, 11.5 pgs.

Graphics IC simplifies design, boosts performance. Randall, Martin, Intel; *Computer Design*, 06/01/86, pg 73, 4.5 pgs.

Graphics coprocessor chip gives small systems a look at the big picture. Randall, Martin, Intel; Johary, Arun, Intel; *Electronic Design*, 05/29/86, pg 159, 6 pgs.

How silicon ICs are reshaping the graphics picture. Ohr, Stephan, Technology Editor; *Electronic Design*, 06/26/86, pg 72, 6 pgs.

Intel designs a graphics chip for both CAD and business use. Staff; *Electronics*, 05/19/86, pg 57, 4 pgs.

Livelier graphics—the bit-slice bonus. Kondraske, George V, University of Texas at Arlington, et al; *Electronic Products*, 09/16/86, pg 54, 8 pgs.

NCR aims its graphics chips at PC instead of work station. Staff; *Electronics*, 05/19/86, pg 61, 3 pgs.

Powerful support chips simplify graphics design. Raghavan, Mike, Hitachi America; Wheeler, P Kim, Hitachi America; *Electronic Design*, 08/21/86, pg 123, 5 pgs.

Racehorse RAM spurs sharper color graphics. Teza, Jeff, Brooktree; Plummer Sr, Wylie, Brooktree; *Electronic Products*, 09/16/86, pg 68, 5 pgs.

Super chips bring unprecedented power to graphics display control. Williams, Tom, Western Managing Editor; *Computer Design*, 05/01/86, pg 65, 13 pgs.

The scramble to win in graphics chips. Lineback, J Robert, Dallas Editor; *Electronics*, 05/19/86, pg 64, 2 pgs.

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Advances in flat-panel-display technology improve display features and cut prices. Mosley, J D, Regional Editor; EDN, 09/04/86, pg 79, 5 pgs.

Boards that meet EGA spec bring flexible graphics capability to IBM PC workstations. Conner, Margery S, Regional Editor; EDN, 09/18/86, pg 75, 6 pgs.

Compressing data conserves memory in bit-mapped displays. Fuchs, Peter M, *Advanced Micro Devices*; EDN, 10/30/86, pg 173, 7 pgs.

Designers want realism and real-time interactivity in graphics systems. Williams, Tom, Western Managing Editor; *Computer Design*, 07/86, pg 62, 2 pgs.

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Frame-grabber boards acquire and process images in real time. *Preston, Craig, Data Translation; Molinari, John, Data Translation; EDN, 09/18/86, pg 273, 6 pgs.*

Graphics pixel processing sizzles with smart frame buffer. *Williams, Tom, Western Managing Editor; Computer Design, 10/01/86, pg 46, 1.5 pgs.*

PC onslaught leads to lower-cost graphics. *Wilson, Andrew, Senior Technical Editor; Digital Design, 10/86, pg 21, 1 pg.*

PC-based graphics take on work stations. *Rubinger, David, Electronics, 07/24/86, pg 38, 1 pg.*

Pixel-plane machine debuts at SIGGRAPH. *Wilson, Andrew, Senior Technical Editor; Digital Design, 09/86, pg 24, 2 pgs.*

Smart buffer speeds 3-d graphics. *Rose, Craig D, Boston Editor; Electronics, 08/21/86, pg 36, 1 pg.*

Versatile add-in boards acquire and process video images and graphics in real time. *Titus, Jon, Senior Editor; EDN, 08/07/86, pg 103, 6 pgs.*

What's new in imaging at EI '86. *Wilson, Andrew C, Senior Technical Editor; Digital Design, 10/86, pg 57, 3 pgs.*

## H

### Heat sinks/cooling devices

Tiny channels take heat from multichip modules. *Lyman, Jerry, Packaging/Production Editor; Electronics, 05/12/86, pg 28, 0.5 pgs.*

### Hybrid circuits

Careful design takes the heat out of hybrid power op amps. *Scofield, Granger, Apex Microtechnology; Electronic Design, 09/11/86, pg 115, 5 pgs.*

High-power hybrid op amp dissipates up to 500 W and guards against burnout. *Scofield, Granger, Apex Microtechnology; Electronic Design, 05/15/86, pg 129, 5 pgs.*

Hybrid IC operational amplifiers achieve higher power, voltage, and speed. *Fleming, Tarlton, Associate Editor; EDN, 09/18/86, pg 59, 7 pgs.*

Hybrid circuits: meeting tough challenges in tough environments. *Mennie, Don, Electronic Design, 06/19/86, pg 64, 8 pgs.*

Hybrid makers balk at MIL-STD obstacle course. *Dixon, Thomas, Midwestern Editor; Electronic Products, 10/15/86, pg 68, 5 pgs.*

Isolation amplifiers get better as their sizes and costs shrink. *Heftman, Gene, Electronic Design, 05/01/86, pg 101, 4.5 pgs.*

Motorola makes a run at the hybrid market. *Iversen, Wesley R, Industrial & Consumer Editor; Electronics, 10/16/86, pg 34, 1 pg.*

Synchro/resolver converters bring low cost and small size to motion-control systems. *Fleming, Tarlton, Associate Editor; EDN, 10/30/86, pg 61, 6 pgs.*

Thick and thin films battle for growing hybrid market. *Lyman, Jerry, Packaging/Production Editor; Electronics, 08/07/86, pg 88, 5 pgs.*

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### Inductors

Lack of standards breeds diversity in SMD inductors. *Leibson, Steven H, Regional Editor; EDN, 07/24/86, pg 189, 6 pgs.*

### Industrial electronics

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### Inspection

CAD data makes inspection flexible. *Rose, Craig D, Boston Editor; Electronics, 06/16/86, pg 27, 0.5 pgs.*

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Increased use of radiation-hardened ICs calls for more careful interpretation of test claims. *Bloom, Michael, Contributing Editor; Computer Design, 07/86, pg 26, 5 pgs.*

Test & measurement. *McLeod, Jonah, Managing Editor; Elec-*

*tronics, 10/16/86, pg 98, 2 pgs.*

Tester guarantees ASIC performance. *Lindsay, Ken, Integrated Measurement Systems; Miller, John, Integrated Measurement Systems; Digital Design, 05/86, pg 73, 4 pgs.*

Time-domain reflectometers tackle fiber-optic cabling. *Michaels, Ian, Electronic Design, 08/07/86, pg 59, 3 pgs.*

### Insurance

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### Integrated circuits/semiconductor devices/circuit design, other

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Fairchild's radical process for building bipolar VLSI. *Staff; Electronics, 09/04/86, pg 55, 5 pgs.*

ICs outspeed software in doing text searches. *Manuel, Tom, Managing Editor; Electronics, 07/24/86, pg 32, 1 pg.*

Methodology speeds VLSI circuit design cycles. *Feller, Albert, RCA, Aerospace & Defense Division; EDN, 05/15/86, pg 151, 7.5 pgs.*

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Revived transistor structure lowers cost of bipolar VLSI. *Gosch, John, Frankfurt Editor; Electronics, 07/24/86, pg 29, 1 pg.*

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High-level software simplifies use of PC-based instrument modules and systems. *Everett, Chris, Regional Editor; EDN, 10/16/86, pg 61, 5.5 pgs.*

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Professional wire-wrapping services ease prototype-circuit assembly tasks. *Ormond, Tom, Senior Editor; EDN, 09/18/86, pg 115, 5 pgs.*

## K

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## L

### Leadless chip carriers

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*Waltersdorf, Harvey R, Thomas & Betts; Electronic Design, 06/19/86, pg 107, 4.5 pgs.*

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Digital gain control streamlines signal-acquisition systems. *Graeme, Jerald, Burr-Brown; EDN, 05/29/86, pg 171, 9 pgs.*

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- High-power op amp provides diverse circuit functions. *Widlar, Robert, National Semiconductor; Yamatake, Mineo, National Semiconductor; EDN, 05/29/86, pg 185, 13 pgs.*
- High-precision CMOS op amps accommodate  $\pm 15V$  supplies. *Sherman, Leonard, Maxim Integrated Products; EDN, 05/29/86, pg 149, 9 pgs.*
- High-voltage circuits use mixed processes, fulfill diverse roles. *Travis, Bill, Senior Editor; EDN, 07/10/86, pg 74, 10 pgs.*
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- Local-area network architecture/design/design standards**
- A low-cost way to build a fiber-optic local-area net. *Staff; Electronics, 06/02/86, pg 36, 2 pgs.*
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- LAN standards breed a multitude of smart boards. *Mokhoff, Nicolas, Senior Editor; Computer Design, 05/15/86, pg 34, 3 pgs.*
- Low-speed LANs check in at \$100 per connection. *Barney, Clifford, San Mateo Editor; Electronics, 07/10/86, pg 29, 1 pg.*
- MAP: Blueprint for a new industrial revolution. *Dixon, Tom, Mfg. Automation Editor; Electronic Products, 08/15/86, pg 46, 8 pgs.*
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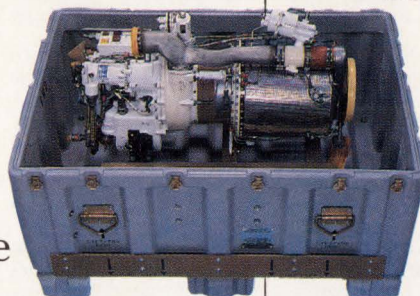
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CIRCLE NO 133

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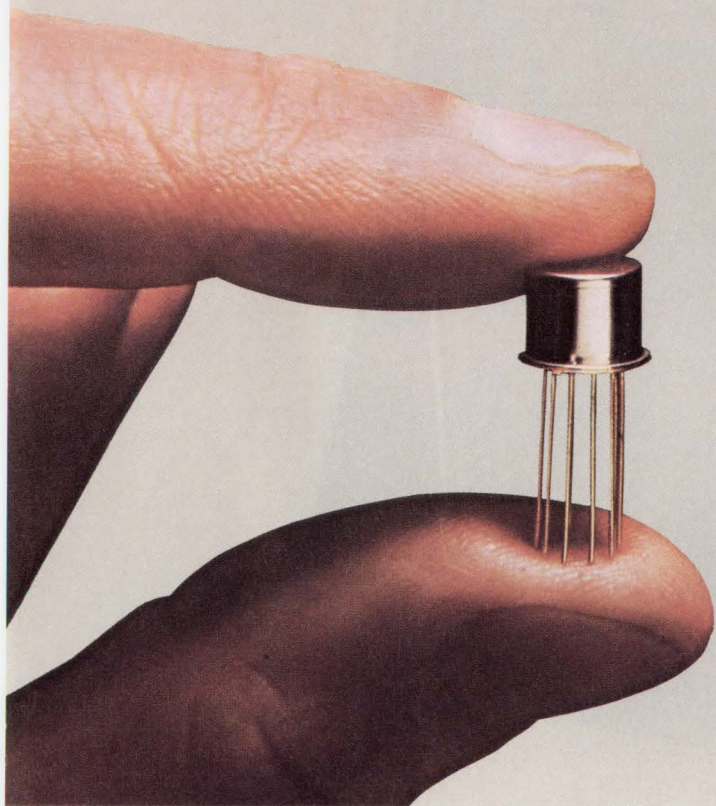
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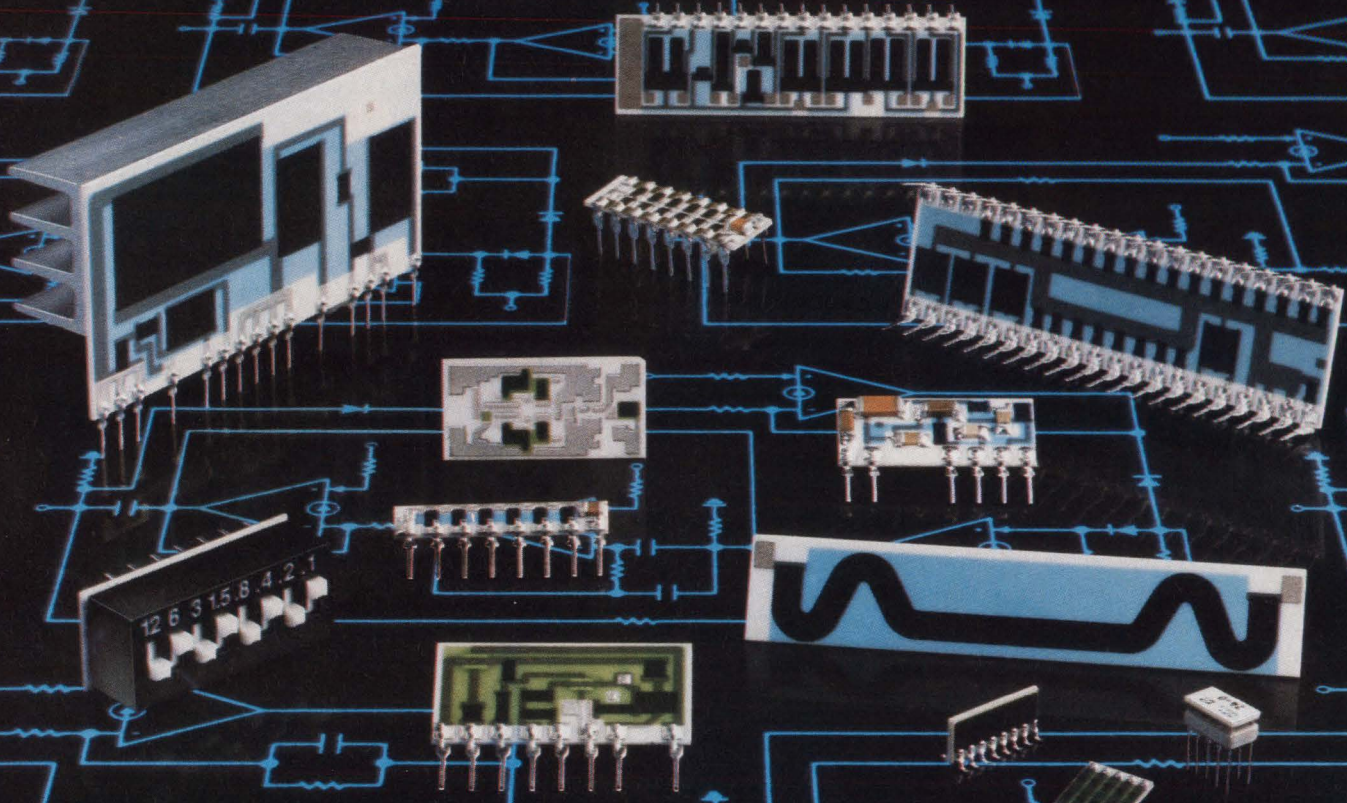
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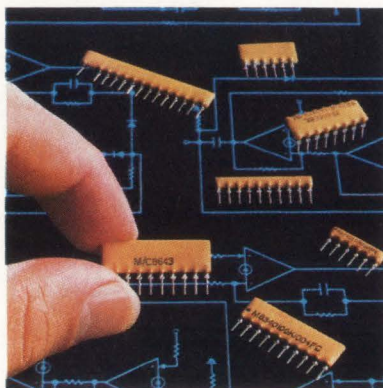


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# P

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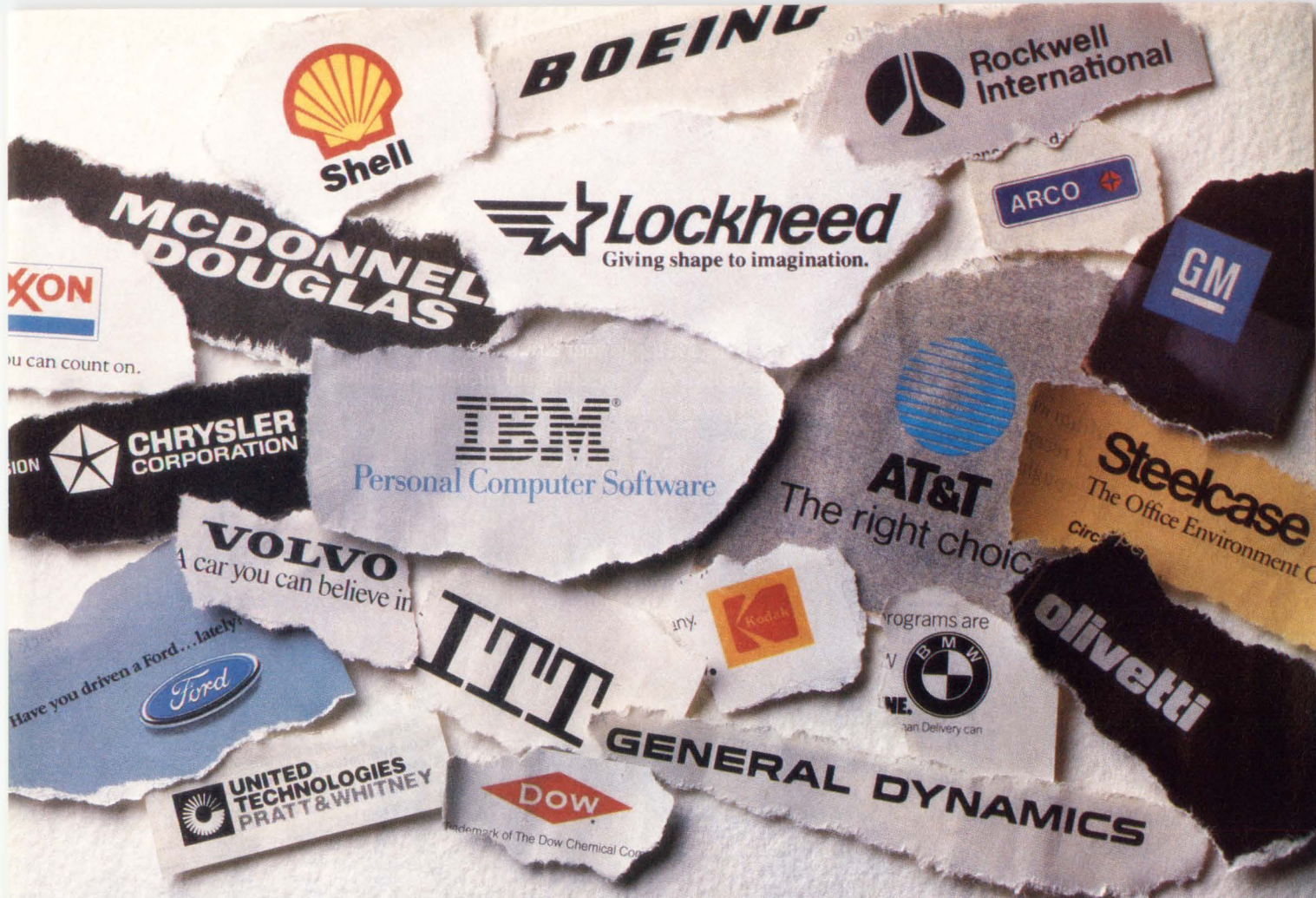
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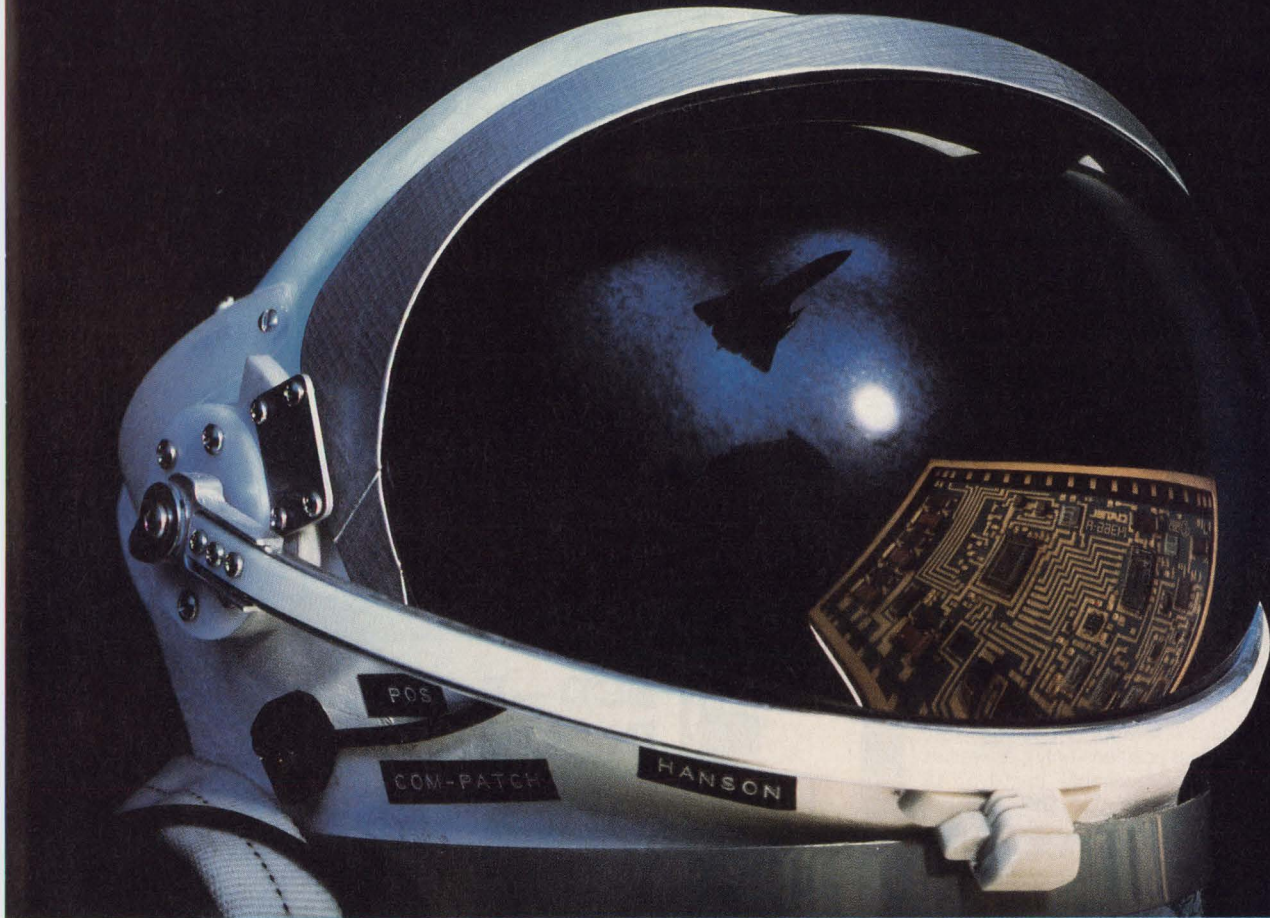
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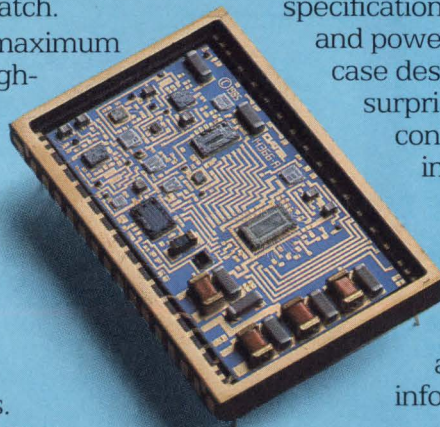
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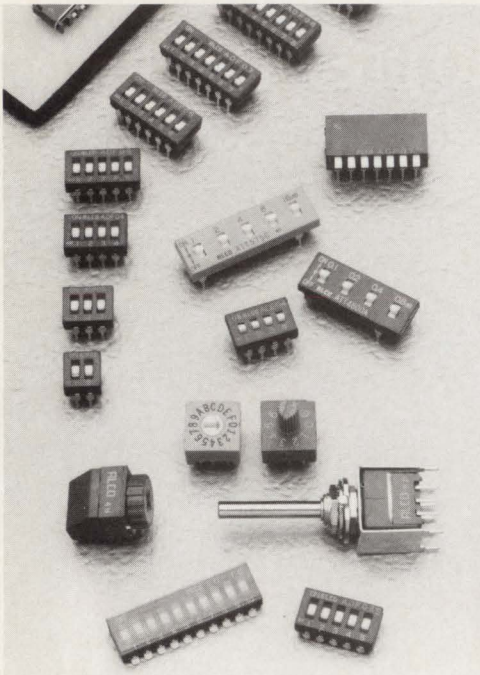
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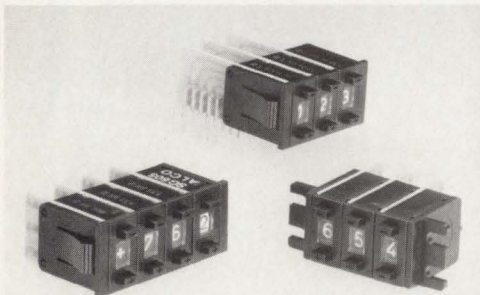
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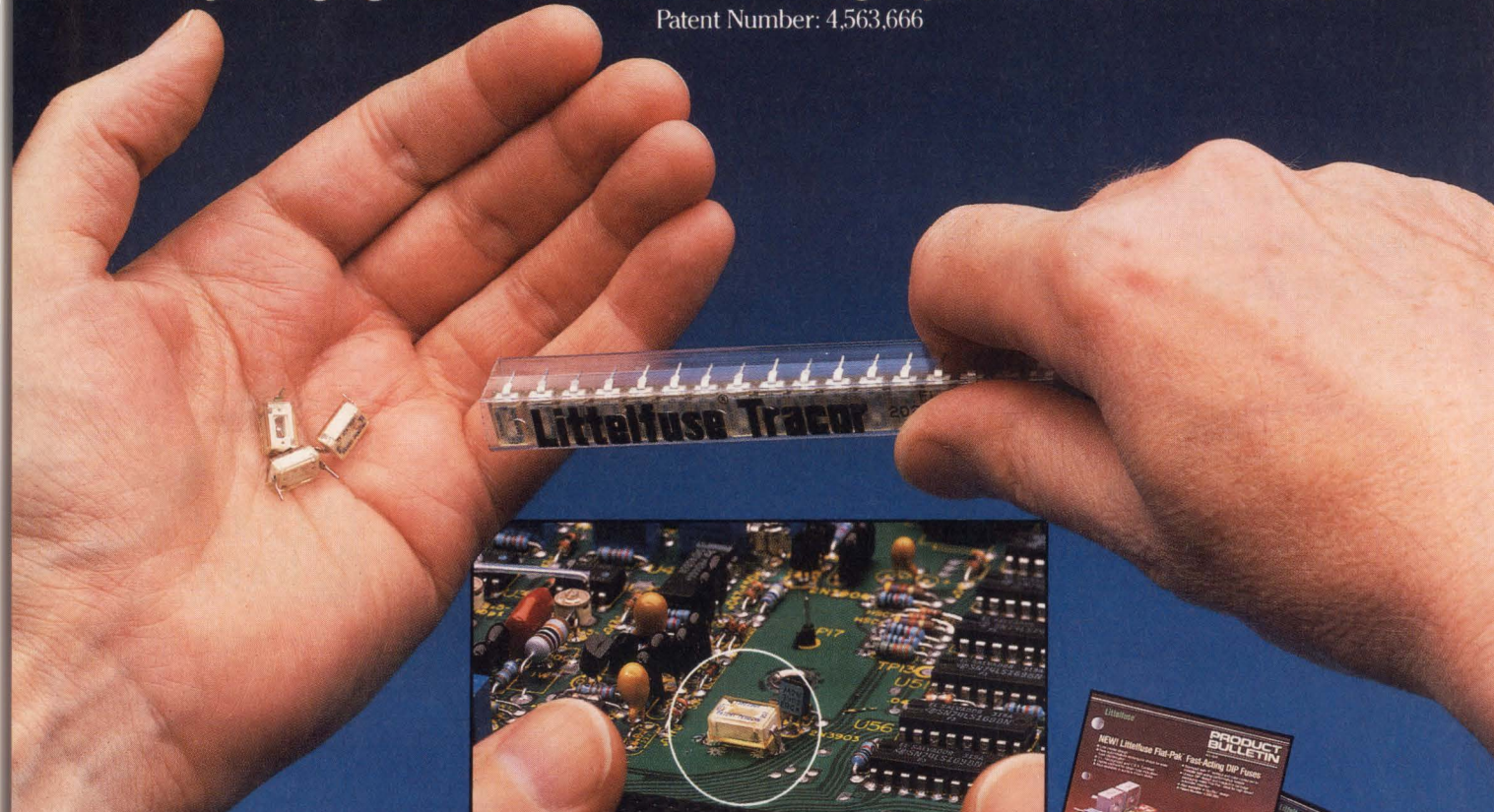
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Module adds smarts to Minitel terminal. *Schenker, Jennifer L, Electronics, 09/04/86, pg 44, 0.5 pgs.*

New standards, silicon chips nudge ISDNs closer to reality. *Allan, Roger, Associate Managing Editor; Electronic Design, 07/24/86, pg 88, 7 pgs.*

Packet-switched communications extend multiprocessor's range. *Marrin, Ken, Senior Editor; Computer Design, 09/01/86, pg 20, 4 pgs.*

Production deficiencies may slow East Germans. *Gosch, John, Frankfurt Editor; Electronics, 05/05/86, pg 22, 1 pg.*

Quality speech rides 8-kb/s channel. *Rose, Craig D, Boston Editor; Electronics, 08/07/86, pg 36, 1 pg.*

Satellite system to cut marine telecom costs. *Staff; Electronics, 09/18/86, pg 38, 2 pgs.*

Telecommunications. *Rosenberg, Robert, Communications Editor; Electronics, 10/16/86, pg 85, 3 pgs.*

The digital phone net finally starts taking off. *Rosenberg, Robert, Communications Editor; Electronics, 08/21/86, pg 57, 5 pgs.*

The French move to open telecom market. *Gallagher, Robert T, Paris Editor; Electronics, 05/26/86, pg 19, 1 pg.*

## Temperature measurement

Temperature measurements gain from advances in high-precision op amps. *Wong, James, Precision Monolithics; Electronic Design, 05/15/86, pg 167, 4 pgs.*

## Terminal controllers

High-density chip set trims PC AT for industrial tasks. *Owen, Jeff, Chips & Technologies; Electronic Design, 10/02/86, pg 131, 5 pgs.*

Terminal controllers cut UNIX host interruptions. *Aseo, Joseph, West Coast Technical Editor; Digital Design, 05/86, pg 27, 1 pg.*

Terminals add PC features to fulfill multiuser system demands. *Killmon, Peg, Senior Editor; Computer Design, 05/01/86, pg 46, 1.5 pgs.*

## Terminals

Advances in flat-panel-display technology improve display features and cut prices. *Mosley, J D, Regional Editor; EDN, 09/04/86, pg 79, 5 pgs.*

## Test fixtures/probes

How Genrad's new tester copes with VHSIC chips. *Staff; Electronics, 05/19/86, pg 49, 4 pgs.*

## Thin-film equipment, chemical vapor deposition

Tools make thin films predictable. *Rose, Craig D, Boston Editor; Electronics, 05/26/86, pg 16, 1 pg.*

## Thyristors

Transistor provides thyristor control. *Zannis, James, Renishaw Metrology Ltd; EDN, 06/26/86, pg 233, 1 pg.*

## Timer ICs/circuits

Digital-delay circuit is programmable. *Embler, Gary, Tall Tree*

# EDN TECHNICAL-ARTICLE DATABASE

*Systems; EDN, 09/04/86, pg 214, 1.5 pgs.*  
PLD provides chip select and wait states. *Dujari, Vineet, Advanced Micro Devices; EDN, 08/21/86, pg 184, 2 pgs.*  
Programmable event generator conquers timing restraints. *Threewitt, Bruce, Advanced Micro Devices; Electronic Products, 07/01/86, pg 60, 5 pgs.*  
Sequential timer uses three chips. *Kuber, V B, Motwane Mfg Co Private Ltd; EDN, 09/18/86, pg 318, 1 pg.*  
Timer IC provides low-power voltage monitor. *O'Farrell, John J, Tran-Trol; EDN, 07/10/86, pg 262, 1.5 pgs.*

## Touch-screen devices

A new cost contender in touch-sensitive screens. *Rose, Craig D, Boston Editor; Electronics, 07/24/86, pg 38, 1 pg.*  
Can touch-screen technology move beyond special uses? *Naegele, Tobias, New York Editor; Electronics, 05/05/86, pg 42, 2 pgs.*  
Touchscreen displays suit multifarious applications. *Javetski, John, EDN, 10/16/86, pg 195, 8 pgs.*  
Touch-screen scopes ease complex measurements. *Rogers, Greg, Tektronix, et al; Electronic Design, 10/16/86, pg 109, 6.5 pgs.*

## Training

EE students learn the newest technologies but some are opting for non-design jobs. *Asbrand, Deborah, Staff Editor; EDN, 10/02/86, pg 285, 2.5 pgs.*  
To Bales, training is the way to beat Japanese. *Iversen, Wesley R, Industrial & Consumer Editor; Electronics, 05/12/86, pg 58, 0.5 pgs.*

## Transmitter/receiver circuits

CMOS RS-232-C interface chip packs in three driver/receivers. *Tussing, Tanya, Motorola; Bauer, Valerie, Motorola; Electronic Products, 05/01/86, pg 81, 5 pgs.*

## Transmitters/receivers

At last, it's easy to design RS-232-C modems. *Staff; Electronics, 07/24/86, pg 89, 4 pgs.*  
Dual op amp forms RS-232C driver/receiver. *Lambrechts, Jean-Paul, National Semiconductor; EDN, 05/15/86, pg 182, 1 pg.*

## Trigger circuits

Programmable event generator conquers timing restraints. *Threewitt, Bruce, Advanced Micro Devices; Electronic Products, 07/01/86, pg 60, 5 pgs.*

# V

## Video

AT&T makes the right choice for imaging support. *Wilson, Andrew C, Senior Technical Editor; Digital Design, 09/86, pg 40, 2.5 pgs.*  
Disputes may stall HDTV standard for two years. *Leopold, George, Government & Military Editor; Gallagher, Robert, Paris Editor; Electronics, 05/12/86, pg 19, 1 pg.*  
Frame memory adds new TV features. *Cohen, Charles L, Tokyo Editor; Electronics, 06/02/86, pg 24, 1 pg.*  
How image enhancement is taking a giant leap. *Waller, Larry, Los Angeles Editor; Electronics, 07/24/86, pg 30, 0.5 pgs.*  
Image sensors reach megapixel mark. *Wilson, Andrew, Senior Technical Editor; Digital Design, 07/86, pg 25, 1 pg.*  
Large-screen displays get bigger and brighter. *Leaf, Jesse J, News Editor; Electronics, 05/12/86, pg 46, 2 pgs.*  
Now 3-d CAD images can be moved in real time. *Staff; Electronics, 08/07/86, pg 97, 4 pgs.*  
Scanner handles text, images simultaneously. *Barney, Clifford, San Mateo Editor; Electronics, 05/19/86, pg 18, 1 pg.*  
Siemens fits digital TV into 2-Mb/s data stream. *Gosch, John, Frankfurt Editor; Electronics, 10/02/86, pg 40, 1 pg.*  
Solid-state area-scan image sensors vie for machine-vision applications. *Harold, Peter, European Editor; EDN, 05/15/86, pg 55, 6 pgs.*  
The fight over formats will be fierce at CES. *Iversen, Wesley, Industrial & Consumer Editor; Electronics, 06/02/86, pg 44, 2 pgs.*  
The move to PC-based image storage. *Rose, Craig D, Boston Editor; Electronics, 05/12/86, pg 19, 1 pg.*  
Video buffer amplifiers get faster and lower in distortion. *Panasuk, Curtis, Field Editor; Electronic Design, 05/29/86, pg 89, 4.5 pgs.*

## Vision systems

A new way to probe submicron details. *Staff; Electronics, 09/04/86, pg 88, 3 pgs.*

AT&T makes the right choice for imaging support. *Wilson, Andrew C, Senior Technical Editor; Digital Design, 09/86, pg 40, 2.5 pgs.*

Board-level image processors enter desktop arena. *Williams, Tom, Western Managing Editor; Computer Design, 06/01/86, pg 25, 4 pgs.*

CCD cameras reflect emphasis on size and sharpness. *Shapiro, Sydney F, Managing Editor; Computer Design, 06/01/86, pg 41, 3 pgs.*

Fault imaging moves from lab to fab. *Barney, Clifford, San Mateo Editor; Electronics, 10/02/86, pg 37, 1 pg.*

Frame-grabber boards acquire and process images in real time. *Preston, Craig, Data Translation; Molinari, John, Data Translation; EDN, 09/18/86, pg 273, 6 pgs.*

Holographic filter spots images from any angle. *Barney, Clifford, San Mateo Editor; Electronics, 09/04/86, pg 37, 1 pg.*

Image sensors reach megapixel mark. *Wilson, Andrew, Senior Technical Editor; Digital Design, 07/86, pg 25, 1 pg.*

Image-processing boards boost real-time performance. *Molinari, John, Data Translation; Dizenzo, Anthony, Data Translation; Computer Design, 05/15/86, pg 75, 5 pgs.*

Machine vision guides robots and inspection. *Williams, Tom, Western Managing Editor; Computer Design, 07/86, pg 92, 2 pgs.*

Military imaging systems find new targets. *Wilson, Andrew, Senior Technical Editor; Digital Design, 06/86, pg 25, 1 pg.*

Pyramid processing redefines machine vision. *Davis, Andrew W, Recognition Technology; Khan, Imran, Recognition Technology; Digital Design, 05/86, pg 34, 5 pgs.*

Solid-state area-scan image sensors vie for machine-vision applications. *Harold, Peter, European Editor; EDN, 05/15/86, pg 55, 6 pgs.*

Standalone imagers focus on workstation segment. *Wilson, Andrew, Senior Technical Editor; Digital Design, 05/86, pg 17, 2 pgs.*

Uncooled IR sensors shrink scopes. *Leopold, George, Government & Military Editor; Electronics, 05/19/86, pg 21, 0.5 pgs.*

VME imaging boards target machine vision. *Birenbaum, Robert I, Imaging Technology; King, David R, Imaging Technology; Digital Design, 05/86, pg 28, 4 pgs.*

## Voltage converters

Focus on dc-dc converters. *Newhart, Milton, Electronic Design, 09/11/86, pg 169, 4.5 pgs.*

# W

## Waveform analyzers/analysis

Use a PC to generate analog output signals. *Croteau, John, Analog Devices; Grant, Doug, Analog Devices; EDN, 05/15/86, pg 131, 10 pgs.*

# DESIGN IDEAS

EDITED BY TARLTON FLEMING

## Heater controller uses inexpensive parts

Thomas George Barnett  
The London Hospital Medical College,  
London, UK

The heater-control circuit of **Fig 1** operates from 32 to 42°C and delivers as much as 18W to the heating element. Moreover, the circuit controls temperature within  $\pm 0.2^\circ\text{C}$  and is simple to calibrate and use.

For temperature sensing, it uses a half-bridge consisting of a 7-k $\Omega$  resistor and a UUA41J1 thermistor, energized by a 1.26V bandgap reference (IC<sub>2</sub>). Op amps IC<sub>1A</sub> and IC<sub>1B</sub> form a high-input-impedance differential amplifier with a gain of 9.2 that amplifies the bridge output and drives the 20V digital panel meter (DPM).

To calibrate the DPM, substitute a decade resistance box for the thermistor and simulate temperatures of 32, 37, and 42°C by setting the box to 7403, 6017, and 4917 $\Omega$ , respectively. (Corresponding DPM input voltages will be 3.2, 3.7, and 4.2V. See the Fenwal data sheet for full details.) Adjust R<sub>1</sub> so that the DPM reads these temperatures correctly; you can use the meter's gain control for fine adjustment. All the resistors in this part of the circuit should have tight tolerance and low

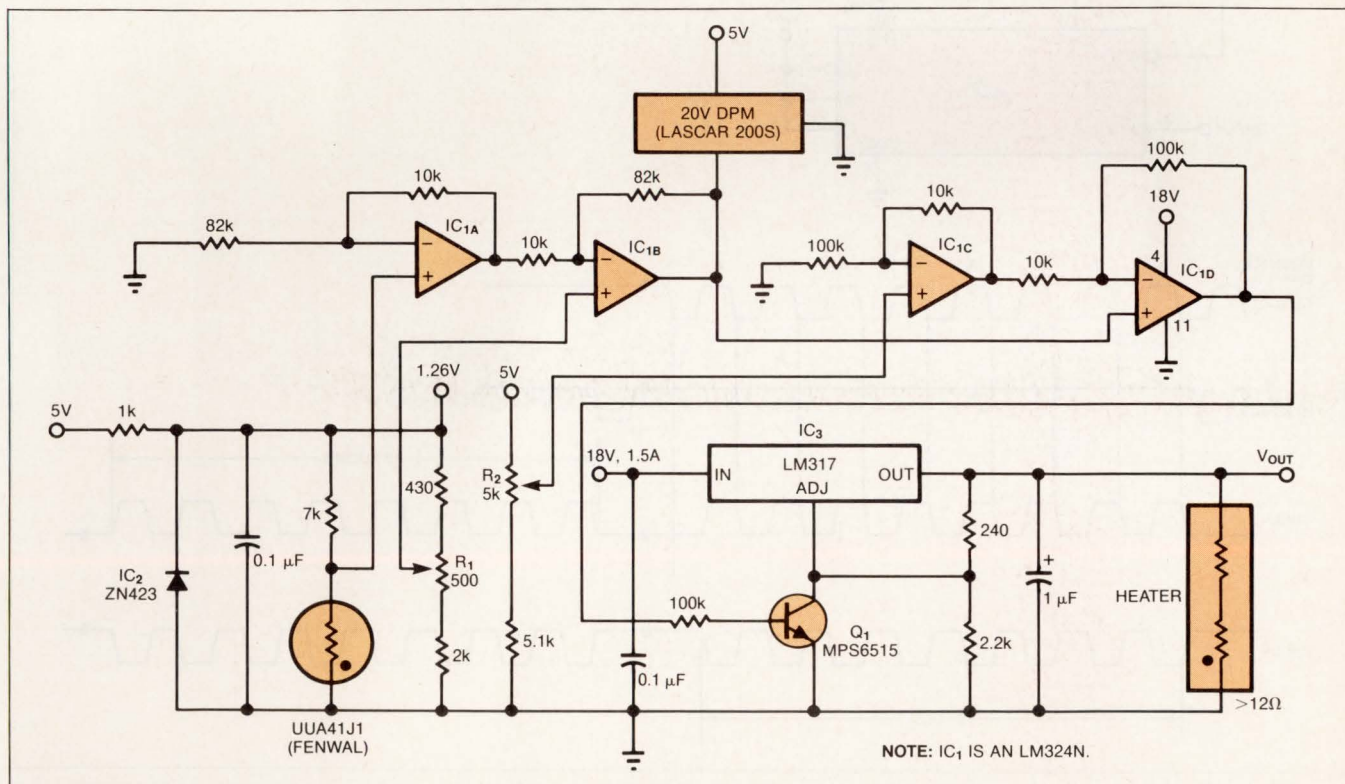
TC to maintain measurement accuracy.

Op amps IC<sub>1C</sub> and IC<sub>1D</sub> form a second high-input-impedance differential amplifier with a gain of 11 that drives transistor Q<sub>1</sub> through a 100-k $\Omega$  resistor. This action controls the voltage output of the positive, variable-voltage regulator (IC<sub>3</sub>) by lowering resistance between the regulator's adjust pin and ground. The regulator can supply as much as 1.5A to the heater.

You can change the circuit's damping as required by varying the IC<sub>1C</sub>-IC<sub>1D</sub> amplifier's gain and Q<sub>1</sub>'s base resistor value. Because the thermistor has a time constant of several seconds, however, this circuit is adequately damped using the component values shown; it does not operate in the bang-bang mode.

R<sub>2</sub> is the set-point potentiometer. To calibrate, note the temperature achieved at different settings and mark the dial accordingly, allowing time for stabilization at each setting. The 5V supply must be well stabilized; other supply voltages are less critical. **EDN**

To Vote For This Design, Circle No 750



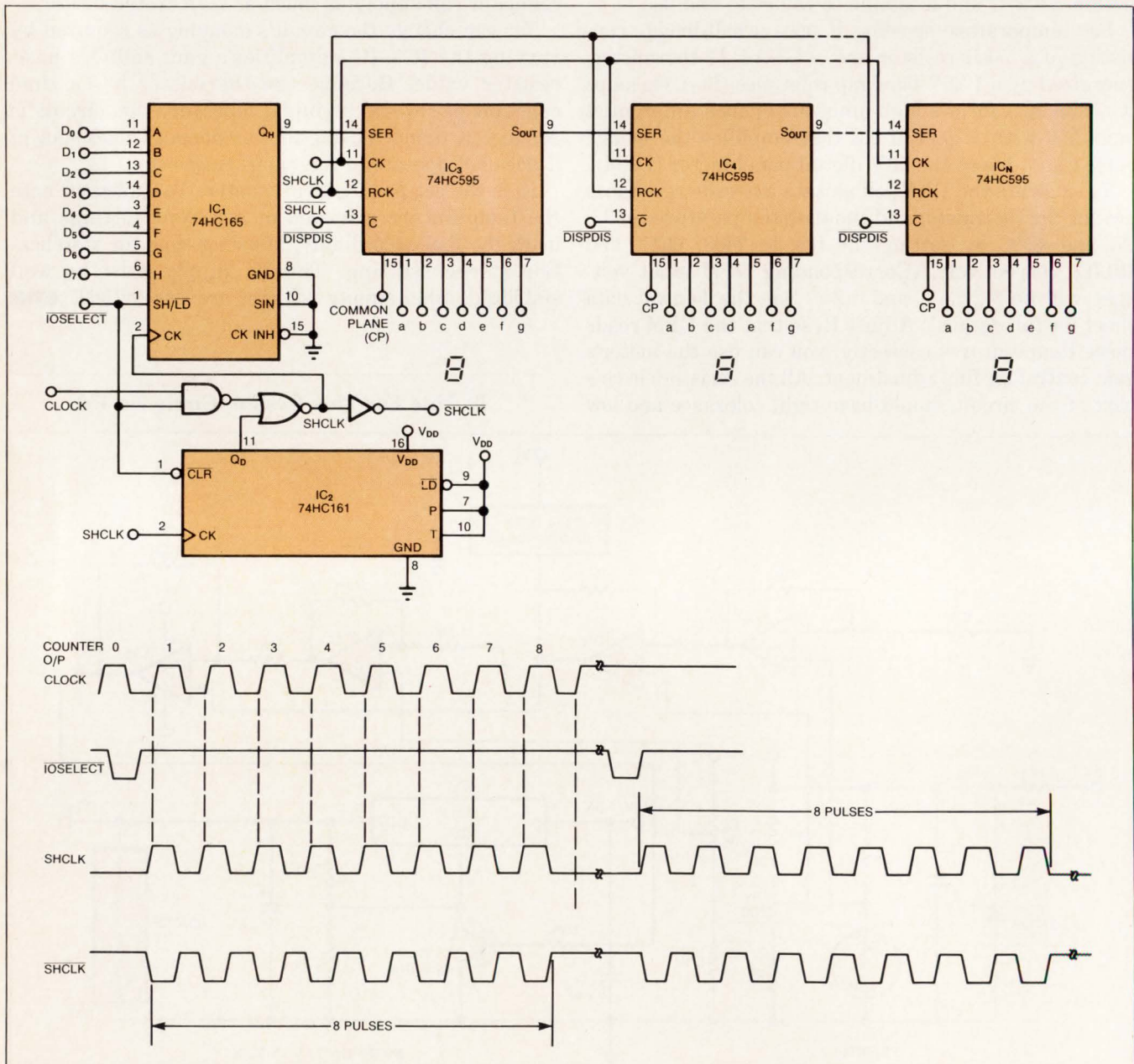
**Fig 1**—This simple, low-power heater controller maintains temperature within  $\pm 0.2^\circ\text{C}$  from 32 to 42°C.

## LCD drivers minimize component space

Ravindra Karnad and Nimisha Mahuvakar  
*Centre for Development of Telematics,  
 Bangalore, India*

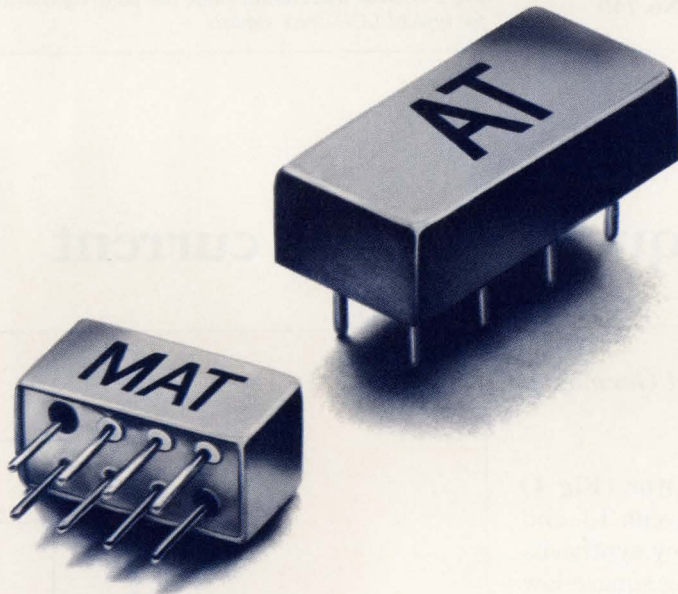
Although you can obtain multicharacter IC drivers for LCDs, an alternative circuit (**Fig 1**) offers advantages. The circuit uses processor time in lieu of external

hardware for timing and decoding. The  $\mu\text{P}$  spends only 100  $\mu\text{sec}$  or so out of every 15 msec to update the display, issuing approximately one data byte per displayed character. To display more information, you add one 16-pin DIP per additional character. Furthermore, the wiring between the display and processor boards comprises just six wires, including  $V_{\text{CC}}$  and ground.



**Fig 1**—This interface circuit between a  $\mu\text{P}$  and an LCD display lets you tailor the parts count to the number of characters in the display.

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AT-5	MAT-5	5
AT-6	MAT-6	6
†† AT-6-75*		6
AT-7	MAT-7	7
AT-8	MAT-8	8
AT-9	MAT-9	9
AT-10	MAT-10	10
†† AT-10-75*		10
AT-12	MAT-12	12
AT-15	MAT-15	15
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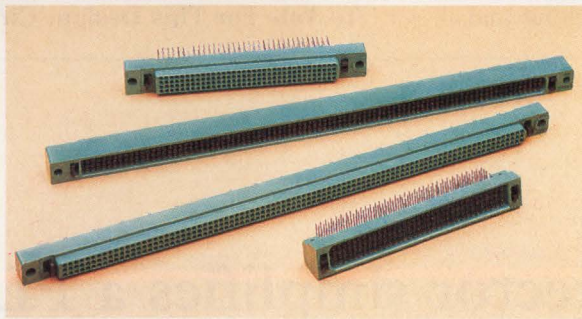


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# DESIGN IDEAS

$$\frac{I_3}{I_1} = e^{\frac{q(V_{BE3} - V_{BE1})}{KT}}, \quad (2)$$

where  $I_S$ =saturation current,  $q$ =electron charge,  $K$ =Boltzmann's constant,  $T$ =absolute temperature, and  $V_{BE1}$  and  $V_{BE3}$  are the base-emitter voltages for transistors  $Q_1$  and  $Q_3$ .

Because  $V_{BE3} = V_{BE1} + R_1(I_1 + I_2)$ , you can write Eq 2 as

$$I_3 = I_1 e^{\frac{q(I_1 + I_2)R_1}{KT}}.$$

Substituting  $I_{IN}$  from Eq 1 yields

$$I_3 = I_{IN} e^{\frac{2qI_{IN}R_1}{KT}}.$$

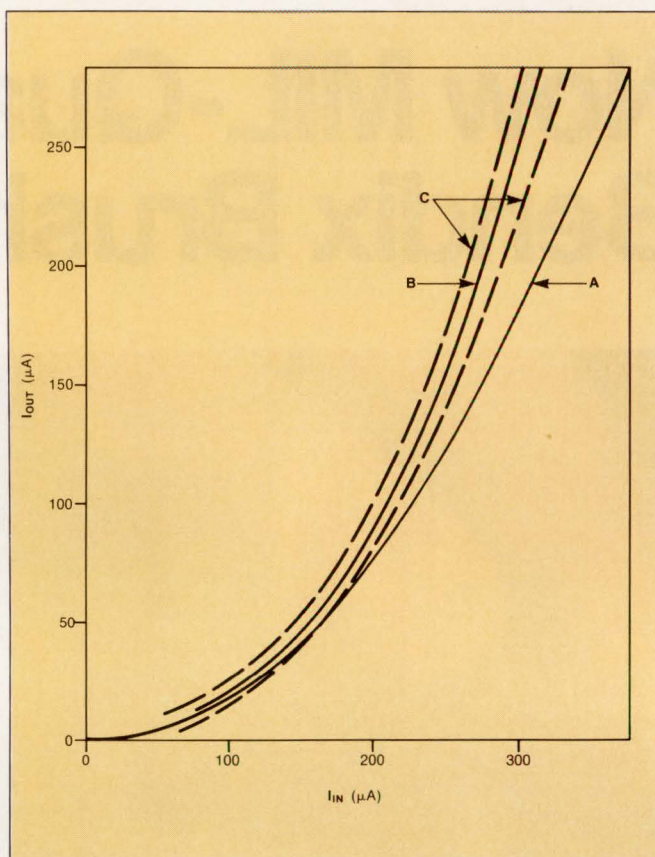
Thus, transistor  $Q_3$  provides an exponential function that you can expand as a power series in the form of  $e^x = 1 + x/1! + x^2/2! + x^3/3! + \dots$  to yield

$$I_3 = I_{IN} \left[ 1 + \frac{2qI_{IN}R_1}{KT} + \left( \frac{2qI_{IN}R_1}{KT} \right)^2 / 2 + \left( \frac{2qI_{IN}R_1}{KT} \right)^3 / 6 + \dots \right]. \quad (3)$$

The output current is  $I_{OUT} = I_3 - I_5 = I_3 - I_{IN}$ . Substituting for  $I_3$  (Eq 3) eliminates the linear term, so the series begins with the quadratic term:

$$I_{OUT} = \left( \frac{2qR_1}{KT} \right) I_{IN}^2 + \left( \frac{2qR_1}{KT} \right)^2 I_{IN}^3 / 2 + \left( \frac{2qR_1}{KT} \right)^3 I_{IN}^4 / 6 + \dots$$

In short, the circuit produces a useful squaring characteristic for low  $2qR_1/KT$  ratios and low input currents. Fig 2 shows the measured and calculated results for a CA3096 transistor array and a  $27\Omega$  resistor. You can extend the 20:1 output-current range by using transistor pairs with tighter  $V_{BE}$  matching and



**Fig 2**—These curves illustrate the performance of Fig 1's circuit. The curve labeled A represents the ideal squaring function, the curve labeled B shows the calculated function, and the two curves labeled C form an envelope for the results obtained using five different CA3096 arrays.

higher betas. If desired, you can reverse the output-current polarity by inserting a resistor with a value  $2R_1$  in the emitter of  $Q_4$  (remove the  $Q_1$ - $Q_2$  emitter resistor in this case). **EDN**

To Vote For This Design, Circle No 746

## Sampling phase detector simplifies a PLL

Russell Kautz  
Texas Instruments, Plano, TX

Phase-locked loops can include an analog frequency-mixing circuit (Fig 1a) or a digital divider (Fig 1b) to

accomplish synchronous down-conversion of the reference and input frequencies. An alternative, the sampling system in Fig 1c, reduces parts count and cost by a factor of eight. Moreover, the sampling approach removes frequency-conversion circuitry from the signal



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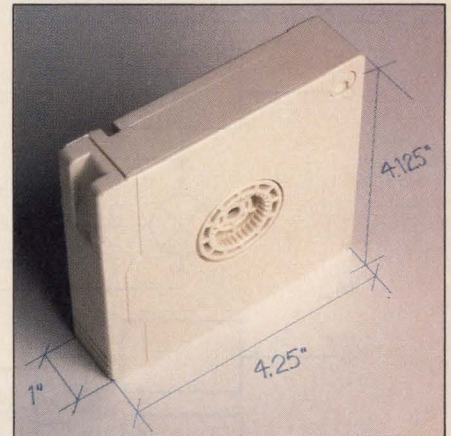
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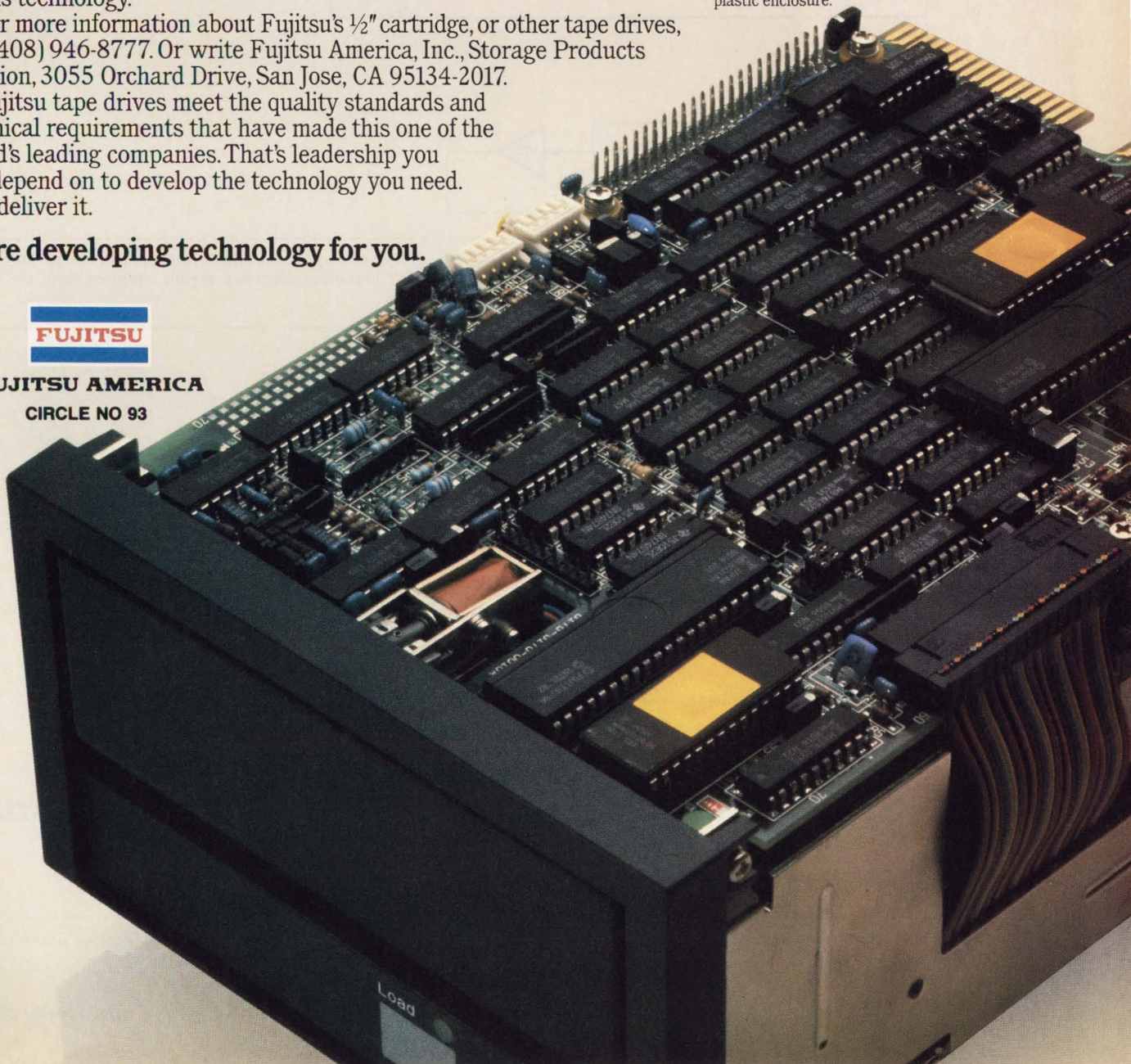
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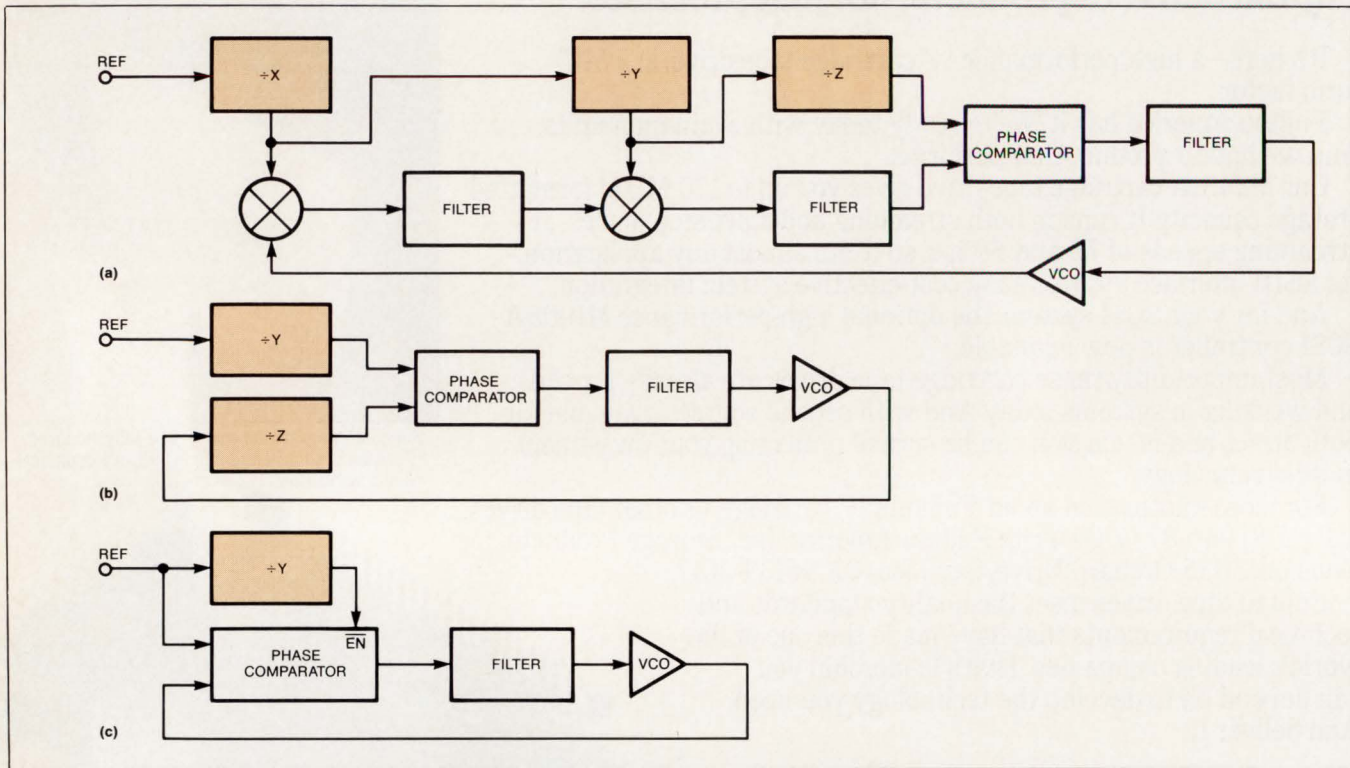
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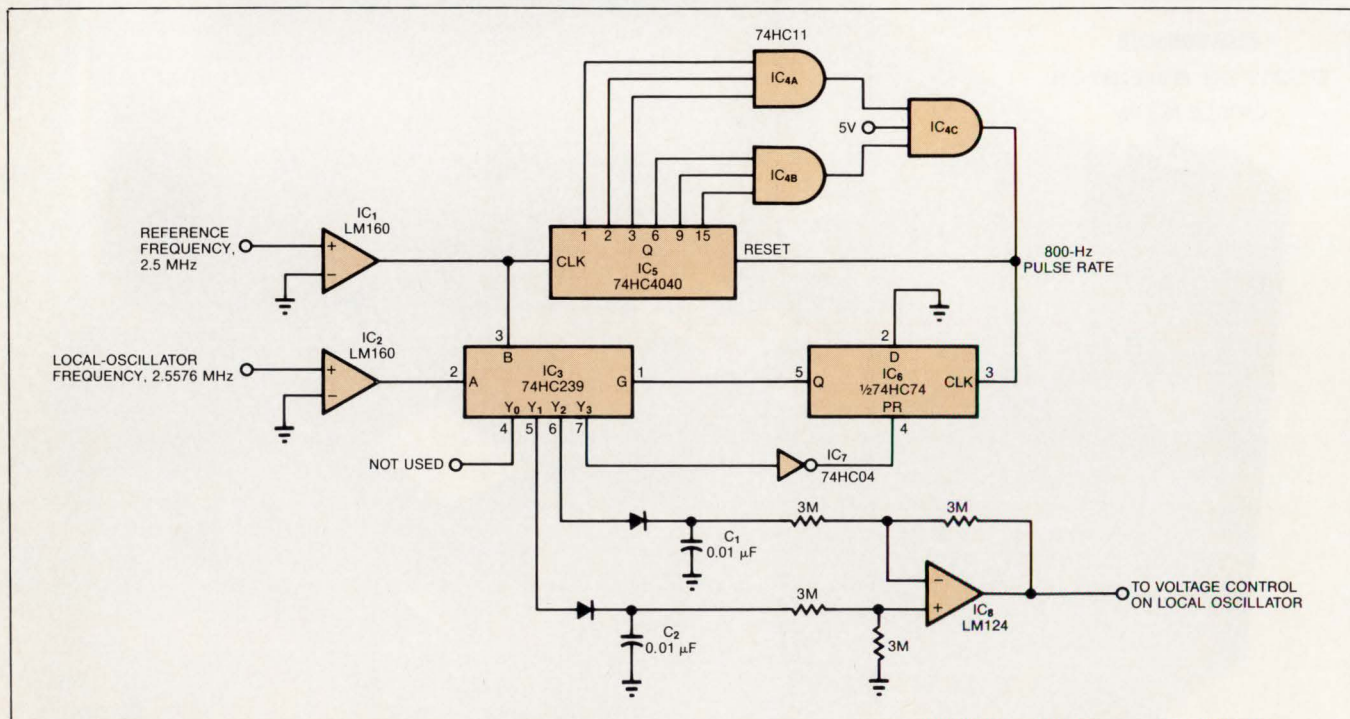
# DESIGN IDEAS

path, which provides improved short-term stability for the local oscillator, excellent temperature stability, and a thirtyfold decrease in lock-in time.

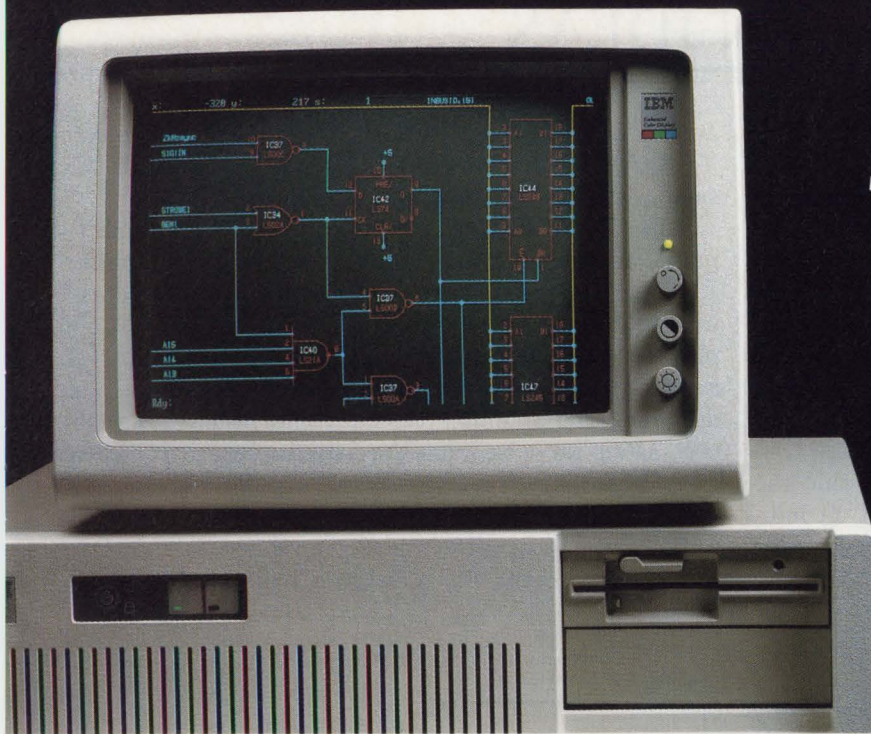
Fig 2 demonstrates a sampling phase-detector loop that locks the output of a crystal oscillator to that of a rubidium standard. First, the zero-crossing detectors



**Fig 1**—Some phase-locked loops use analog frequency-mixing techniques (a), and some divide both inputs to the phase comparator using digital dividers (b). The sampling phase comparator (c) achieves advantages by eliminating down-conversion circuitry from the signal paths.



**Fig 2**—This sampling phase-locked loop generates a voltage output whose polarity and magnitude represent the local oscillator's phase error.



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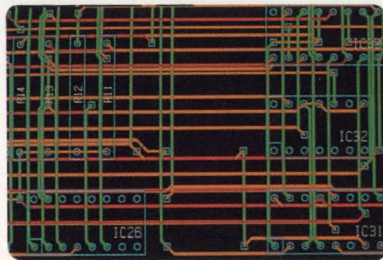
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# DESIGN IDEAS

IC<sub>1</sub> and IC<sub>2</sub> convert the reference and local-oscillator (LO) frequencies to digital signals. The 2-to-4-line demultiplexer IC<sub>3</sub> then samples these frequencies at 800 Hz (every 1.25 msec). The reference and LO frequencies may differ, but each must be an integral multiple of the sampling rate if the system is to achieve lock.

To set the sampling period, IC<sub>4A</sub> and IC<sub>4B</sub> wait for the output 110000110101 (count of 3125) from the 12-bit counter IC<sub>5</sub>. When that output occurs, IC<sub>4C</sub> issues a brief positive pulse that resets the counter and toggles the flip-flop IC<sub>6</sub>.

Fig 3 illustrates the digital phase detection that the IC<sub>3</sub> demultiplexer performs. The presence of Y<sub>1</sub> indicates a phase lead between the LO and reference frequencies, and the duration of Y<sub>1</sub> indicates the

amount of phase lead. Similarly, Y<sub>2</sub> indicates phase lag. Y<sub>3</sub> goes high when both inputs are high, which ends the sample period by setting the flip-flop.

Note that in Fig 2 C<sub>1</sub> and C<sub>2</sub> convert the Y<sub>1</sub> and Y<sub>2</sub> pulses to voltage inputs for the differential amplifier IC<sub>8</sub>. The amplifier in turn produces a dc voltage representing polarity and magnitude of the local oscillator's phase error. When locked, the loop produces narrow Y<sub>1</sub> and Y<sub>2</sub> pulses (less than 1 nsec) of equal magnitude and duration. The amplifier rejects common-mode signals such as digital noise from the demultiplexer. **EDN**

To Vote For This Design, Circle No 747

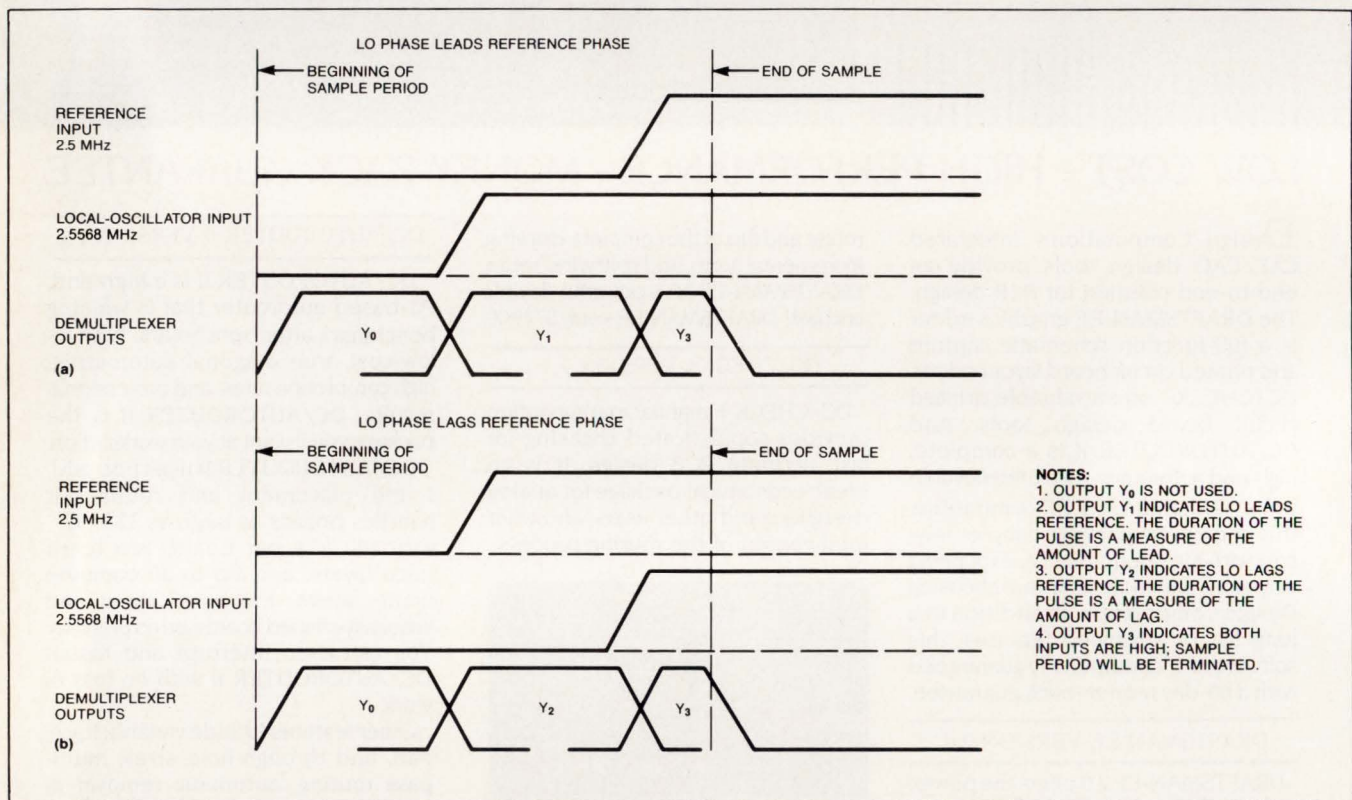


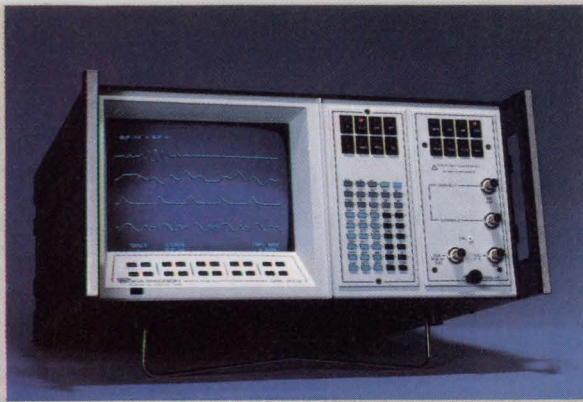
Fig 3—These waveforms depict Fig 2's operation for the cases of leading phase (a) and lagging phase (b).

## Programmable integrator has 6-decade range

Mike Chang  
Amber Electro Design Inc,  
Montreal, Quebec, Canada

The voltage-controlled integrator of Fig 1 provides a programmable time constant for use in applications

such as programmable oscillators and programmable filters. Compared with designs based on OTAs (operational transconductance amplifiers) and monolithic multipliers, this circuit offers lower distortion, lower noise gain vs frequency, and better dynamic range. Furthermore, the circuit provides continuous remote tuning



DATA 6000 Waveform Analyzer



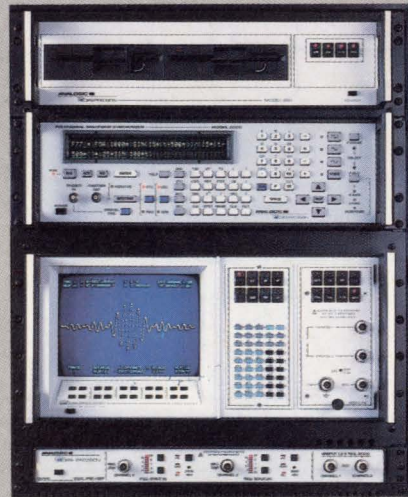
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- Companion Model 681 Flexible Disk Drive for waveform and program storage.
- Full Programmability for ATE via IEEE-488 or RS-232 interface.



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\* Patents pending

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Circle 191 for Additional Information

Circle 152 for Demonstration

251

# DESIGN IDEAS

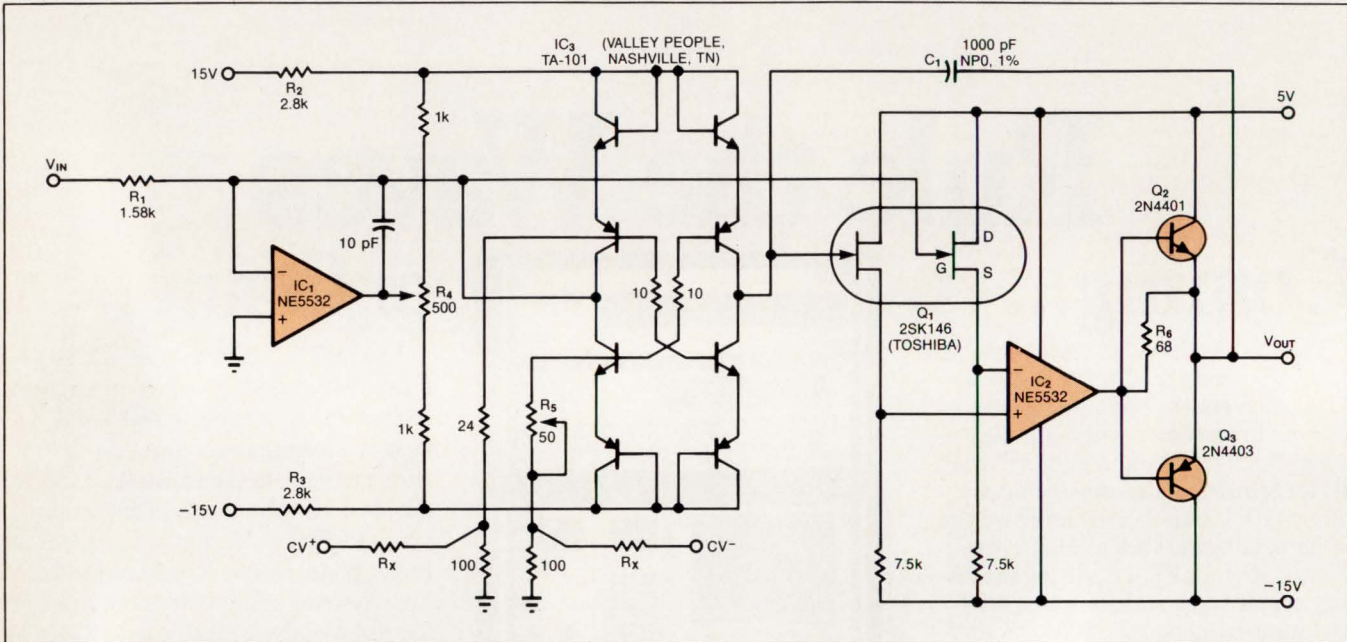
and incurs minimal noise-gain problems during tuning. A 1- to 100-kHz oscillator based on state-variable-filter topology, for example, produces -80 dB of distortion at 100 kHz and -95 dB at 1 kHz (THD plus wideband noise).

The differential control voltage CV sets the time constant of this noninverting integrator. The resulting output is

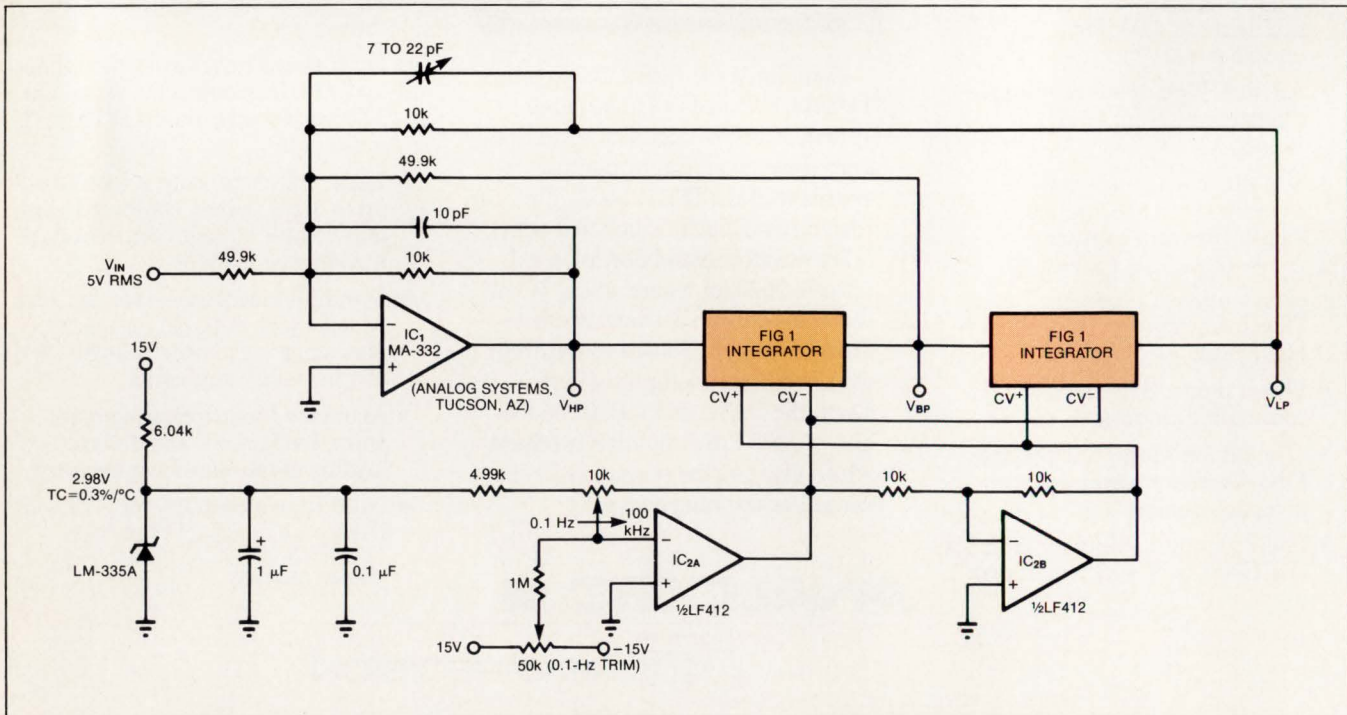
$$V_{OUT} = \int_0^t V_{IN} dt [\log^{-1}(\log V_{IN} + V_C)],$$

where

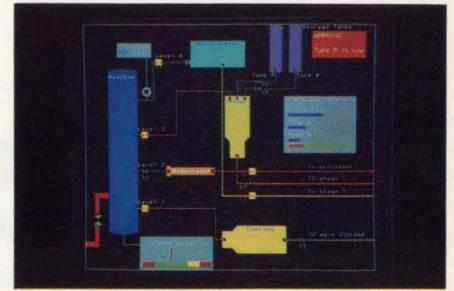
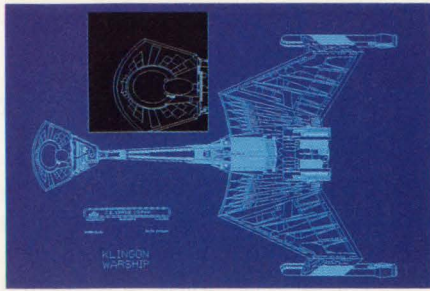
$$V_C = \frac{200CV^+}{R_X + 100}.$$



**Fig 1—This noninverting integrator** has a voltage-programmable time constant that you can adjust over six decades by varying the differential control voltage CV.



**Fig 2—This 0.1- to 100-kHz filter** uses two of Fig 1's integrator circuits and includes an LM-335A temperature sensor to compensate for the transistor array's 3300-ppm/°C temperature coefficient. You set the filter's cutoff frequency by adjusting the 10-kΩ potentiometer.



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The integrator includes an 8-transistor array connected as a complementary, cross-balanced, log-antilog multiplier. Resistors  $R_2$  and  $R_3$  set a 4-mA bias for the multiplier that allows low-distortion operation for inputs as high as 5V rms and 100 kHz. You trim the circuit for minimum second-harmonic distortion by adjusting  $R_5$  at the highest operating frequency ( $CV=0V$ ). Then, use  $R_4$  to adjust for minimum distortion at the lowest operating frequency.

You scale the differential control voltage  $CV^+/CV^-$  by selecting  $R_X$  (two resistors) to provide the desired internal voltage range (a differential of 120 mV at the top of the 100 $\Omega$  resistors causes one decade of frequency change).  $CV=0V$  produces the highest operating frequency allowed by the integrator components  $R_1$  and  $C_1$ , which is 100 kHz for this circuit.

The matched pair of JFET source followers ( $Q_1$ ) buffers the input bias currents of op amp  $IC_2$  and reduces output noise within the integrator's 120-dB operating range.  $Q_2$ ,  $Q_3$ , and  $R_6$  buffer  $IC_2$ 's output, allowing the integrator to maintain low distortion while driving capacitor  $C_1$  and the output load.

Feedforward compensation (the connection from  $Q_1$  to the virtual ground of  $IC_1$ ) achieves a threefold increase in  $Q$  as compared to that of a simple Miller integrator. In addition, feedforward compensation counters the unwelcome  $Q$  enhancement that would otherwise occur in this circuit when used in topologies such as state-variable filters.

The transistor array exhibits a TC of 3300 ppm/ $^{\circ}C$ , for which a thermistor (for example, Tel Labs' Q-81 or EQ) usually provides compensation. However, the thermistor's nonlinear TC and the difficulty of achieving tight thermal coupling between the thermistor and the array make the use of a thermistor troublesome. You can achieve more precise compensation by using an LM-335A temperature sensor as shown in Fig 2. The sensor's 2-mA bias generates the same self-heating effect as that experienced by the array. Compensation is quite effective if you protect the sensor from air currents and provide good thermal contact between the sensor and the array.

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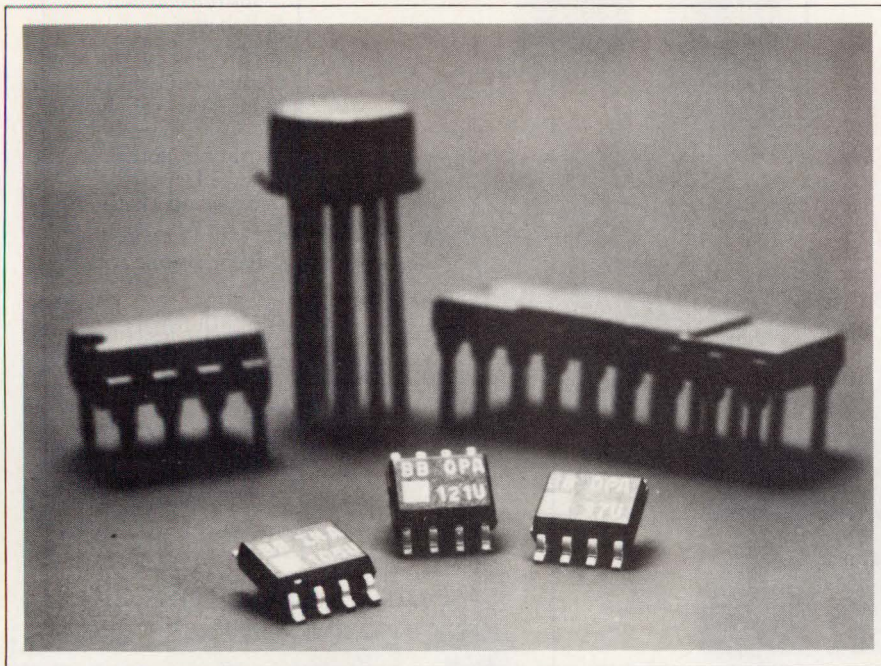
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CIRCLE NO 111

# NEW PRODUCTS

## INTEGRATED CIRCUITS



### OP AMPS

- Available in small-outline packages
- Cut required board space by 50%

Models OPA121U, OPA27/37U, and INA105U amplifiers are small-outline (SO) versions of the manufacturer's DIP-encased devices of the same part numbers (less the U suffix). The ICs measure approximately 0.2×0.15×0.1 in., depending on the model, and have eight 50-mil-center leads having a gull-wing configuration. The OPA121U is a FET-input unit that specs 10-pA max bias

current, 3-mV max offset voltage, and 3- $\mu$ V/ $^{\circ}$ C drift. Models OPA27U and OPA37U are the SO versions of the manufacturer's low-noise 3.2 nV/ $\sqrt{\text{Hz}}$  at 1 kHz op amps. Model INA105U is a unity-gain differential amplifier that specs 0.001% max nonlinearity, 0.025% max gain error, and 72-dB min common-mode rejection over temperature. OPA121U, \$3.05; OPA27/37U, \$3.25; INA105U, \$3.80 (100).

**Burr-Brown Corp.**, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TWX 910-952-1111.

Circle No 351

### POWER-MONITOR IC

- Monitors four supply voltages simultaneously
- Detects overvoltage and undervoltage faults

A quad power-fault monitor, Model SG1548J, keeps watch on as many as four dc-supply voltages simultaneously. The device includes a 2.5V,  $\pm 1\%$  reference; an external divider network connected to the reference allows you to program fault-toler-

ance windows from  $\pm 5$  to  $\pm 40\%$ . An external capacitor sets the fault-indication delay, thereby eliminating false outputs that could arise from switching noise, logic-transition current spikes, and short-term ac-line interruptions. An additional comparator that uses the 2.5V reference allows you to monitor the ac line for undervoltage conditions or for generating a clock. The device is available in a 16-pin plastic or ceramic DIP, or in a 16-pin SO pack-

age. \$2.05 (1000).

**Silicon General**, 11861 Western Ave, Garden Grove, CA 92641. Phone (714) 898-8121. TWX 910-596-1804.

Circle No 352

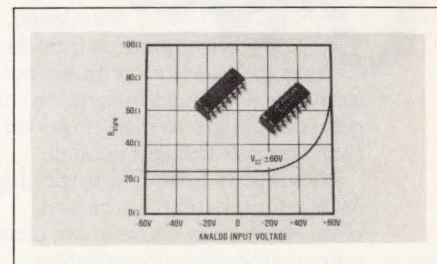
### PC/AT CHIP SET

- Replaces  $> \frac{1}{2}$  of mother board's devices
- Uses 1.8- $\mu$ m standard cells

A 2-chip set called Poach (PC on a chip) replaces more than half the devices found on a PC/AT's mother board. Nine of the replaced devices are major 80286-family peripheral ICs. The two 1.8- $\mu$ m CMOS chips are housed in 84-pin PLCCs. Using readily available 120-nsec RAMs, the chip set can achieve no-wait-state operation at a 10-MHz clock rate. The chip set costs \$45 (OEM qty); for demonstration as a design aid, the company also offers a PC/AT mother board that incorporates the chip set.

**Zymos Corp.**, 477 N Mathilda Ave, Sunnyvale, CA 94086. Phone (408) 730-5400.

Circle No 353



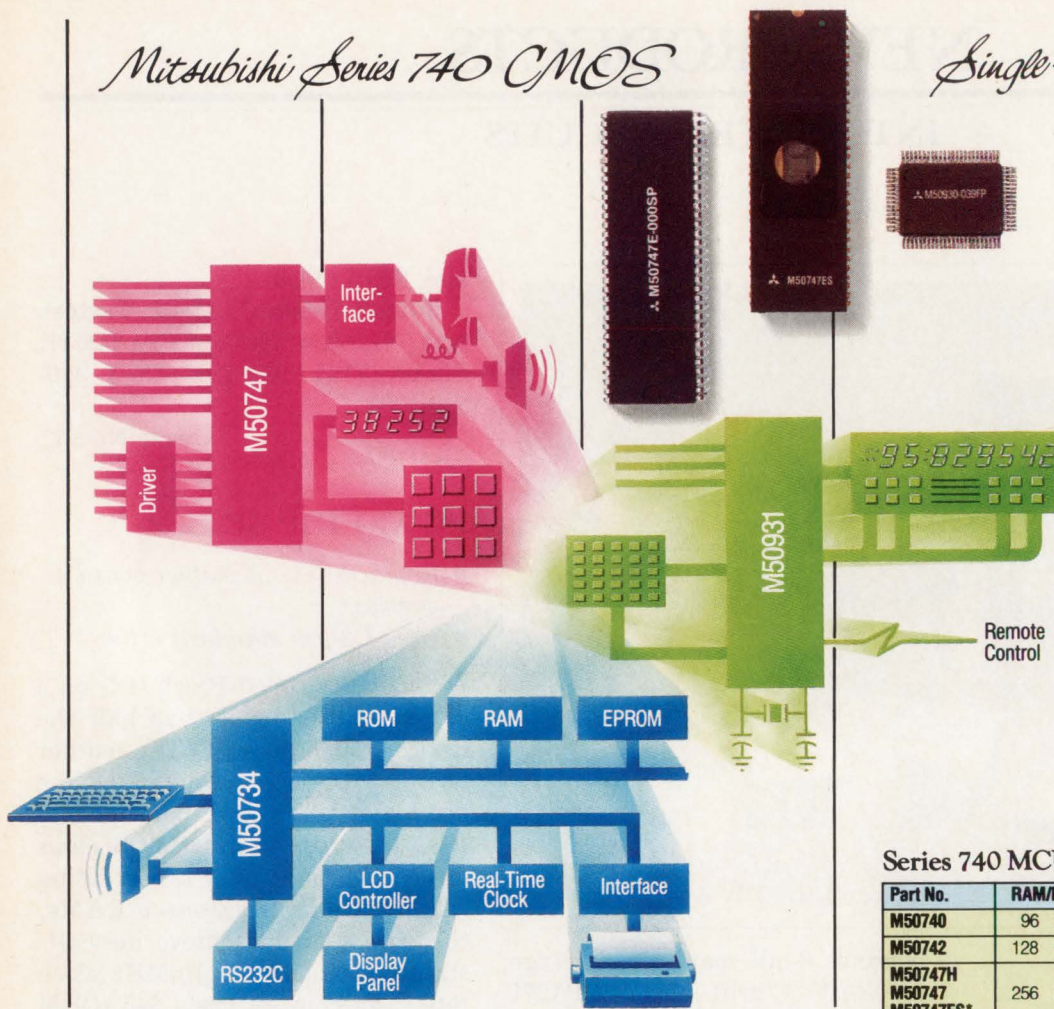
### ANALOG SWITCHES

- Offer  $\pm 50$ V operation, low on-resistance
- Guarantee latch-up-free operation

A family of high-voltage CMOS/DMOS analog switches operates from split supplies of  $\pm 20$  to  $\pm 50$ V or a single supply of 20 to 60V.

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  - CATV Decoders
- Consumer**
  - Security Systems
  - Smart Audio Systems
  - Toys

## Series 740 MCU's (Partial Listing)

Part No.	RAM/ROM	I/O Lines	Key Features
M50740	96 3K	32	
M50742	128 4K	56	SERIAL I/O
M50747H M50747 M50747ES* M50747ESP**	256 8K	56	UART, SERIAL I/O
M50746 M50746ES*	144 6K	53	A/D, D/A
M50734	EXTERNAL	32, plus address and data bus	UART, A/D, STEPPER-MOTOR CONTROLLER.
M50930 M50931	128 4K 512 4K	32, plus 32 LCD segments	LCD CONTROLLER

\*ES: EPROM version \*\*ESP: One-time-programmable (OTP) version

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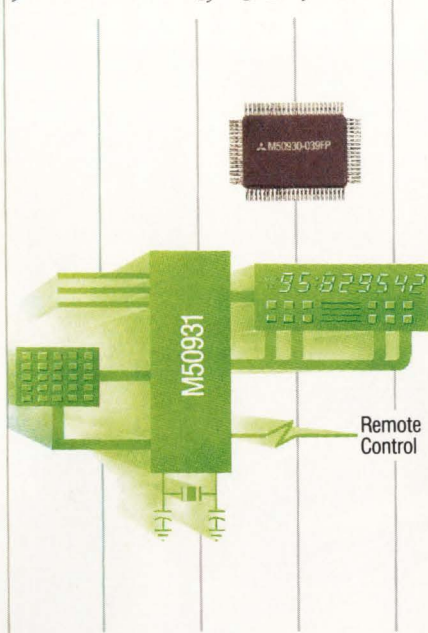
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RAM (bytes)	128	512	
Memory Limit	16K x 8		
I/O Ports	32, plus 32 LCD segments		
Minimum Instruction	2 $\mu$ sec		

\*Under development

For single-chip solutions, call or write Mitsubishi Electronics America, Inc., Semiconductor Division, 1050 E. Arques Avenue, Sunnyvale, CA 94086. (408) 730-5900, Ext. 2314.

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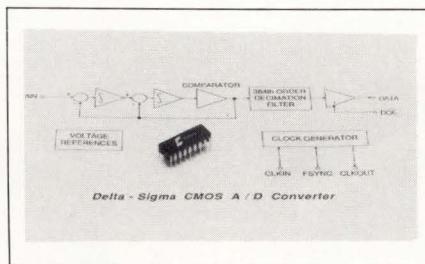
**MITSUBISHI  
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CIRCLE NO 15

## INTEGRATED CIRCUITS

Models MAX341/343/345 have an on-resistance of 80 $\Omega$  typ, 110 $\Omega$  max; MAX348 specs an on-resistance of 35 $\Omega$  typ, 55 $\Omega$  max. Drawing less than 20-mW of operating power, the switches offer operation that's latch-up free. You can cascade the devices to switch currents as high as 500 mA. The switches' control input accepts 15V CMOS or other high-level drive signals. The ICs' specs guarantee make-before-break operation. Turn-on and -off times are 1  $\mu$ sec max and 750 nsec max, respectively. Models MAX341 and MAX348 are dual spst devices; the MAX343 is a dual spdt unit, and the MAX345 is a dual dpst switch. All models are available in commercial, industrial, and military temperature ranges. Prices for the MAX341, MAX343/345, and the MAX348 start at \$5.95, \$9.95, and \$8.95 (100), respectively.

**Maxim Integrated Products**, 510 N Pastoria Ave, Sunnyvale, CA 94086. Phone (408) 737-7600.

Circle No 354



### A/D CONVERTER

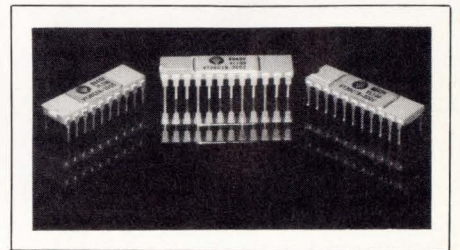
- Uses delta-sigma modulation
- Has 16-bit resolution, 84-dB dynamic range

Using an oversampling technique called delta-sigma modulation, Model CS5316 A/D converter provides 16-bit resolution, 84-dB dynamic range, and full-scale signal-to-total harmonic distortion exceeding -72 dB. The converter samples input signals at a 2-MHz rate to digitize signals whose frequencies range from 0 to 4 kHz. A delta-sigma modulation loop then processes the resulting input samples to obtain a 1-bit digital-data

stream. An internal linear-phase digital filter refines the 2-MHz data stream. The resulting 16-kHz data stream of 16-bit words then emerges from the IC through a codec-like serial interface. The converter operates from 5V power supplies and dissipates less than 200 mW. Housed in an 18-pin plastic DIP, the CS5316 costs \$30 (1000).

**Crystal Semiconductor Corp.**, Box 17847, Austin, TX 78760. Phone (512) 445-7222. TLX 910-874-1352.

Circle No 355

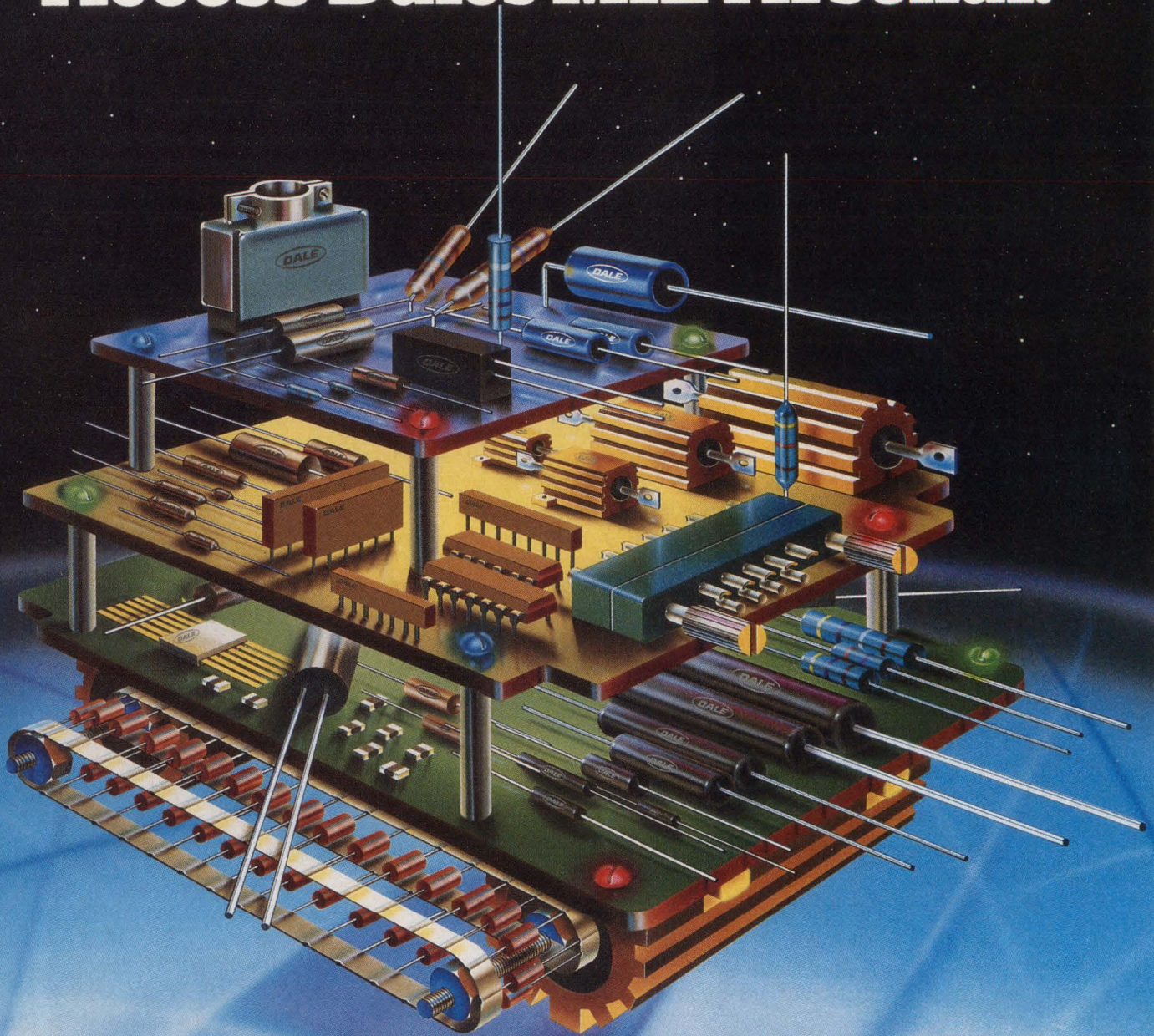


### STATIC RAMs

- Have access and cycle times as low as 20 nsec
- Available in 2k x 8- and 4k x 4-bit versions

These six CMOS-processed, 16k-bit static RAMs spec access and cycle times as low as 20 nsec. Models VT20C18 and VT20C19 are organized as 2048 x 8 bits; Models VT20C68/69/78/79 are organized as 4096 x 4 bits. In addition to their 20-nsec access and cycle times, models VT20C19/69/79 have a fast-chip-enable option that provides data access in as little as 10 nsec. Models VT20C18/19/78/79 also have a fast-output-enable control function. Active power consumption is typically 550 mW; models VT20C18/68/78 reduce power consumption further by providing an automatic power-down feature that reduces standby power consumption to 35 mW in the presence of TTL inputs. For CMOS inputs, standby current consumption is 10 nA max. Models VT20C18/19 come in 24-pin, side-braced ceramic DIPs; the VT20C68/69, in 20-pin, side-braced DIPs; and the

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##### MIL-R-122

##### MIL-R-10509

- RN50, RN55, RN60
- RN65, RN70, RN75

#### MIL-R-22684

- RL07, RL20

#### MIL-R-39017

- RLR05, RLR07, RLR20

#### MIL-R-55182

- RNR55, RNR60, RNR65
- RNC50, RNC55, RNC60
- RNC65, RNC70

#### WIREWOUND RESISTORS

Phone 402-564-3131

##### MIL-R-26

- RW67, RW68, RW69
- RW70, RW74, RW78, RW79
- RW80, RW81

##### MIL-R-18546

- RE60, RE65, RE70
- RE75, RE77, RE80

#### MIL-R-39007

- RWR71, RWR74, RWR78
- RWR80, RWR81, RWR82
- RWR84, RWR89

#### MIL-R-39009

- RER40, RER45, RER50
- RER55, RER60, RER65
- RER70, RER75

#### INDUCTORS

Phone 605-665-9301

##### MIL-C-15305

- MS75087, MS75088, MS75089
- MS75083, MS75084, MS75085
- MS14046, MS18130, MS90538

#### CONNECTORS

Phone 605-665-9301

##### MIL-C-28748/7,8

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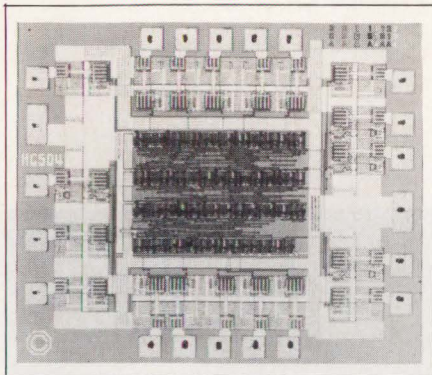
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## INTEGRATED CIRCUITS

VT20C78/79 in 22-pin, side-brazed DIPs. The 20-nsec versions of the VT20C18/19, \$21.24; of the VT20C68/69/78/79, \$14.28 (1000).

**VLSI Technology Inc**, 1109 McKay Dr, San Jose, CA 95131. Phone (408) 434-3000. TLX 278807.

Circle No 356



### SAR CHIP

- Directly replaces 2504 and 25L04 bipolar ICs
- Consumes <4 mA at 25 MHz

This CMOS-processed, high-speed successive-approximation register, Model Zy25HCT04, is a direct replacement for 2504 and 25L04 bipolar devices. The device draws less than 4 mA of supply current at its guaranteed maximum operating frequency of 25 MHz. At a 1-MHz clock rate, the IC draws less than 100  $\mu$ A from its 5V supply. The device is fabricated with a 1.5- $\mu$ m, n-well CMOS process and is available in chip form or in a plastic DIP. Chips, \$4.80; DIP units, \$5.50 (100).

**Zyrel Inc**, 1900 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 433-0488.

Circle No 357

### SINGLE-CHIP $\mu$ Cs

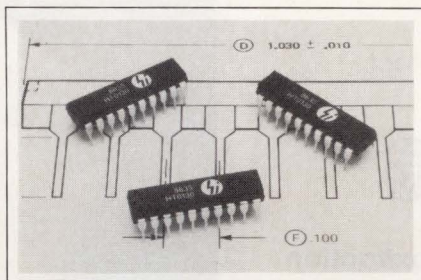
- Software compatible with the 8086 and 8088
- Reduce power requirements

Two CMOS-processed 1-chip microcomputers combine 8086/8088 compatibility with internal peripheral features. The  $\mu$ PD70320 and

$\mu$ PD70322, members of the manufacturer's V25 Series, provide serial and parallel I/O ports, a comparator, timers, a DMA controller, and 256 bytes of RAM. These peripheral functions previously required chips external to the 8086/8088  $\mu$ P. Other features include a 16/32-bit temporary register/shifter, a 16-bit loop counter, a program counter and pre-fetch pointer, and a dual data bus that allows fetching two operands simultaneously. The  $\mu$ PD70322 differs from the  $\mu$ PD70320 in that it contains 16k bytes of mask-programmable ROM. In 80-pin plastic miniflat packages or 84-pin plastic LCCs, each device costs \$25 (OEM qty).

**NEC Electronics Inc**, Literature-MS4580, 401 Ellis St, Mountain View, CA 94039. Phone (415) 965-6144. TWX 910-379-6985.

Circle No 358



### LEVEL TRANSLATOR

- A 1-chip low-to-high-voltage translator
- Drives n- and p-channel push-pull outputs

Claimed by its manufacturer to be the industry's first monolithic low-to-high-voltage translator, Model HT01 is an 8-channel device that provides 0 to 300V outputs. This high-voltage capability allows the device to drive n- and p-channel complementary-output devices connected in a push-pull configuration. Containing eight channels that have separate inputs and outputs, the HT01 has output-source and -sink capabilities of 200 and 100  $\mu$ A, respectively. Logic inputs to the device can range from 5 to 15V. The

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CIRCLE NO 16

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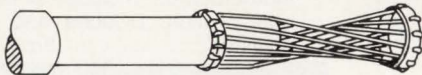
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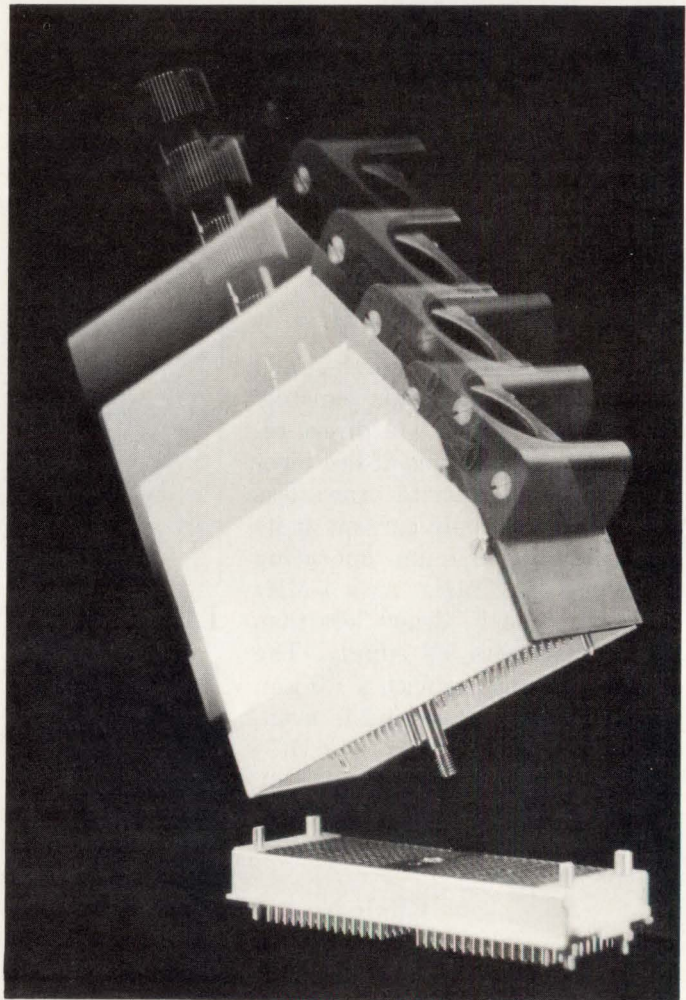
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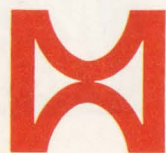


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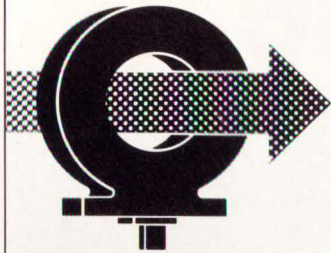


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CIRCLE NO 17

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## INTEGRATED CIRCUITS

high-voltage-referenced logic outputs swing to 14V less than the high-voltage rail. Housed in a 20-pin plastic DIP, the HT01 costs \$3.42 (1000).

Supertex Inc, Box 3607, Sunnyvale, CA 94089. Phone (408) 744-0100. TLX 6839143.

Circle No 359

## ANALOG SWITCH

- Improves on dc parameters and speed
- Many previously untestable specs 100% tested

Model DPG201A quad spst analog switch specs source and drain leakage currents of 250 pA at 25°C and 1 nA over -40 to +85°C, a supply range of 10.8 to 22V, a tested charge transfer of 50 pC, and guaranteed maximum variations in on-resistance and switching times between any two channels. Available in plastic and ceramic 16-pin DIPs as well as a 16-pin narrow-body plastic small-outline package, the device comes in models that operate over the military or industrial ranges. \$4.74 to \$17.51 (100).

Siliconix Inc, 2201 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 970-2045.

Circle No 360

## BUFFER AMP

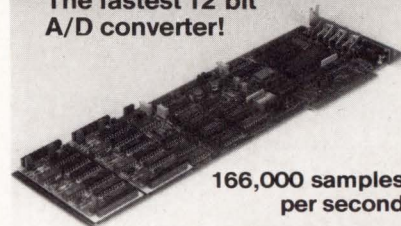
- Has matched vertical pnp and npn transistors
- Draws 10 mA from  $\pm 15V$  supplies

Drop-in-compatible with models HA3-5033-5 and HA3-5002-5, the EL2033CN is a high-speed, unity-gain buffer amplifier that uses the dielectric-isolation process to produce vertical pnp and npn transistors having virtually identical ac and dc characteristics. The device draws only 10 mA typ from its  $\pm 15V$  supplies, as compared with the 21 mA typ drawn by the HA3-

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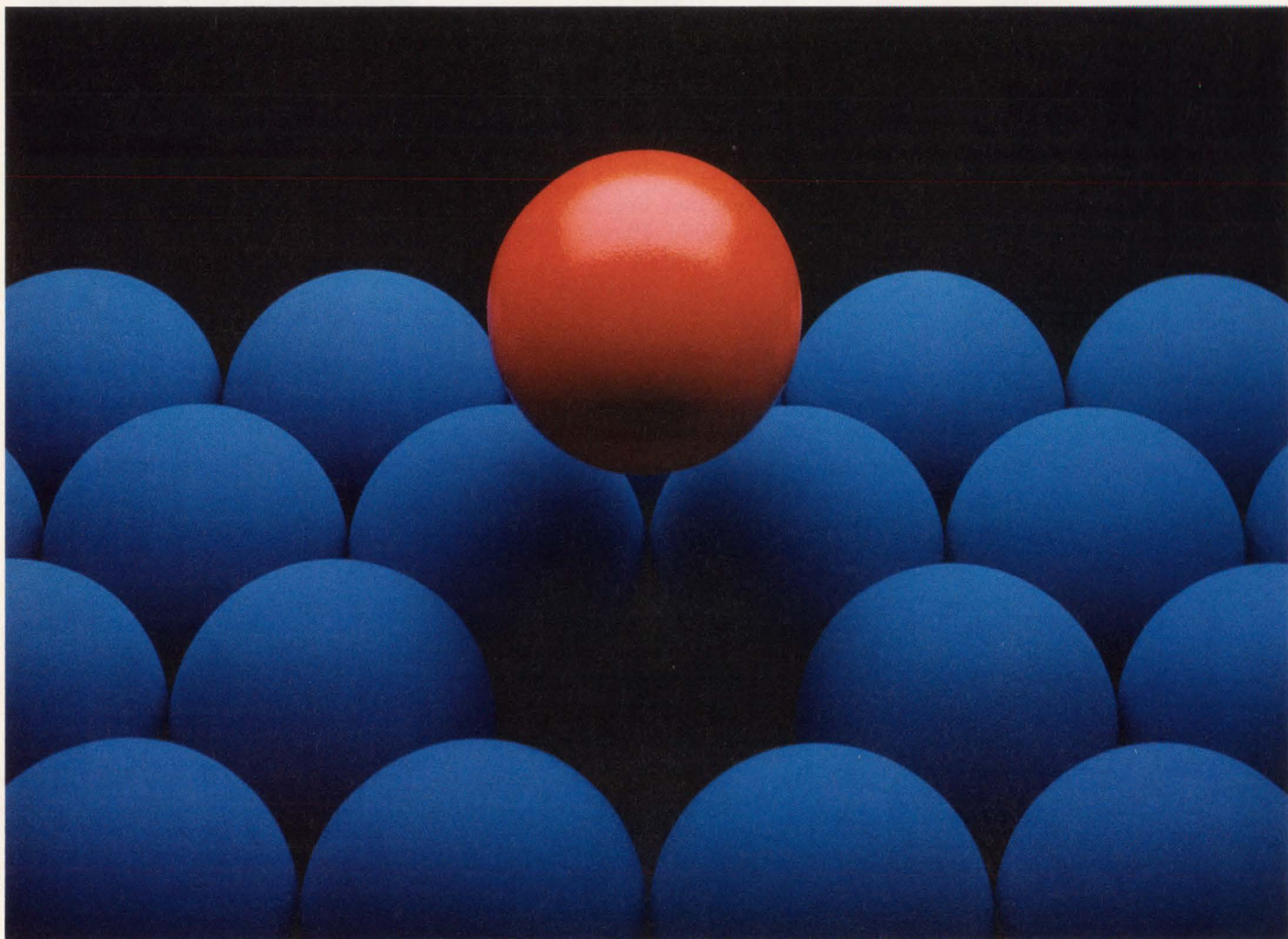
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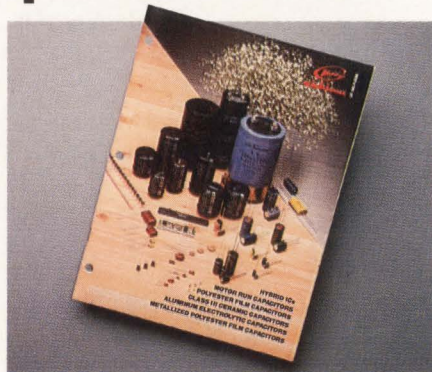


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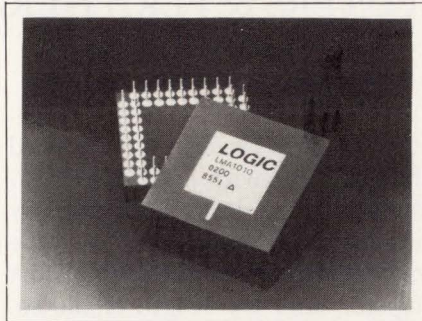
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## INTEGRATED CIRCUITS

5033-5. The EL2033CN operates over  $-25$  to  $+85^{\circ}\text{C}$  and offers short-circuit protection. The IC has a 100-MHz bandwidth and provides at least 100 mA of output current. \$5 (100).

**Elantec Inc.**, 1996 Tarob Court, Milpitas, CA 95035. Phone (408) 945-1323.

Circle No 361



### STEPPER-MOTOR ICs

- Sense and control current in motors
- Operate in tandem with a power stage

Models L6505 and L6506 operate in combination with such power stages as the L293, L298, or L7180 to provide a constant-current drive for inductive loads. Each combination also performs all interface functions, from the control logic through the power stage. The two ICs differ only in the logic used to implement the chopping for the current load. Model L6505 includes exclusive-OR gates in the chopping section, and you can use it with the L298 for 2-phase bipolar motors, in either full- or half-step drives. Model L6506 uses AND gates in the chopping control; you can use the IC in either 2-phase bipolar or 4-phase unipolar configurations. The TTL devices are rated at 10V; they have a 1W power-dissipation capability. \$1.41 (1000).

**SGS Semiconductor Corp.**, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. TLX 249976.

Circle No 362

### 16×16-BIT MACs

- Breaks the \$10 price barrier
- Offered in 45-nsec version

These 16×16-bit multiplier/accumulator ICs come in two versions: Model LMA1010PC breaks the traditional \$10 price barrier for 16×16-bit devices; Model LMA1010PC-45 features 45-nsec operation time. Pin

and function compatible with TMC2010 and Am29510 MACs, both devices perform  $16 \times 16$ -bit multiplication and 35-bit accumulation, as well as subtraction and rounding, using 2s-complement and unsigned-magnitude operands. Available with MIL-STD screening, the MACs come in ceramic DIPs, pin-grid arrays, and plastic LCCs. LMA1010PC, \$9.95; LMA1010PC-45, \$17.93 (1000).

**Logic Devices Inc.**, 628 E Evelyn Ave, Sunnyvale, CA 94086. Phone (408) 720-8630.

Circle No 363

### CMOS PLDs

- First MIL-STD, CMOS 20-nsec reprogrammable PLD
- Saves >60% power vs bipolar designs

A family of 20-pin reprogrammable CMOS PLDs meets MIL-STD-883 and specs 20-nsec propagation delays. Models PALC16L8/R8/R6/R4 use a floating-gate EPROM technology. Specs include 20-nsec propagation delay and setup time, 15-nsec clock-to-output time, 28.5-MHz operating frequency, and 70-mA active current. The units accommodate CUPL and ABEL programming software. Prices for MIL-grade, 20-nsec versions in opaque DIPs, windowed DIPs, and LCCs are \$15, \$27, and \$48 (100), respectively.

**Cypress Semiconductor Corp.**, 3901 N First St, San Jose, CA 95134. Phone (408) 943-2666.

Circle No 364

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80287-6	6 MHz	<b>\$199</b>
80287-8	8 MHz	<b>\$259</b>
80287-10	10 MHz	<b>\$395</b>
NEC V20-8	8 MHz	<b>\$16</b>
NEC V30-10	10 MHz	<b>\$30</b>
64K RAM set	150 ns	<b>\$10</b>
256K RAM set	150 ns	<b>\$27</b>
256K RAM set	120 ns	<b>\$39</b>
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**87 BASIC™** A patch to the IBM Basic or MS QuickBASIC compiler that provides fast, USER TRANS-PARENT 8087 support..... **\$150**

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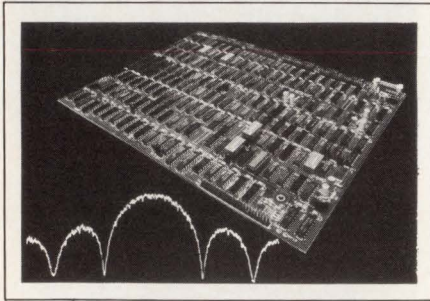
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CIRCLE NO 94

# NEW PRODUCTS

## COMPUTERS & PERIPHERALS



### SEQUENCE GENERATOR

- Features parallel interface to drive frequency hopper
- Includes pseudonoise generator

The PNG-100 is a pseudorandom sequence generator on a 12x9.5-in. pc board. It is designed for use in the development and test of both spread-spectrum and conventional data-communication systems. The board includes a pseudonoise gener-

ator, which is basically a high-speed shift register with linear feedback. You select the desired sequence by setting the feedback pattern, the initial contents of the 16-bit shift register, and the length of the sequence. You can also alter these three parameters on the fly and thus generate highly complex sequences. You can also generate linear recursive sequences by using the board's built-in XOR feedback logic or by inserting your own custom feedback logic. The maximum clock rate is 25 MHz. The board operates in burst, staggered, BPSK, QPSK, or GOLD/JPL modes. You control the generator via clock, data, and start/stop signals. Outputs include a buffered clock, sequence strobes, I and Q direct sequences, and a parallel in-

terface to drive a frequency hopper. \$3500. Delivery, stock to 60 days.

**New Wave Instruments**, 3760 Masters Ct, San Jose, CA 95111. Phone (408) 629-3105.

Circle No 365

### PUBLISHING CARD

- Desktop publishing board for the IBM PC/AT
- Doubles the resolution of some laser printers

The Conovision 2800 board for the IBM PC/XT and PC/AT features a high-resolution monochrome graphics adapter and is optionally available with a raster image processor. The combination doubles the resolution of laser printers that use the Canon LPB-CX engine. For exam-

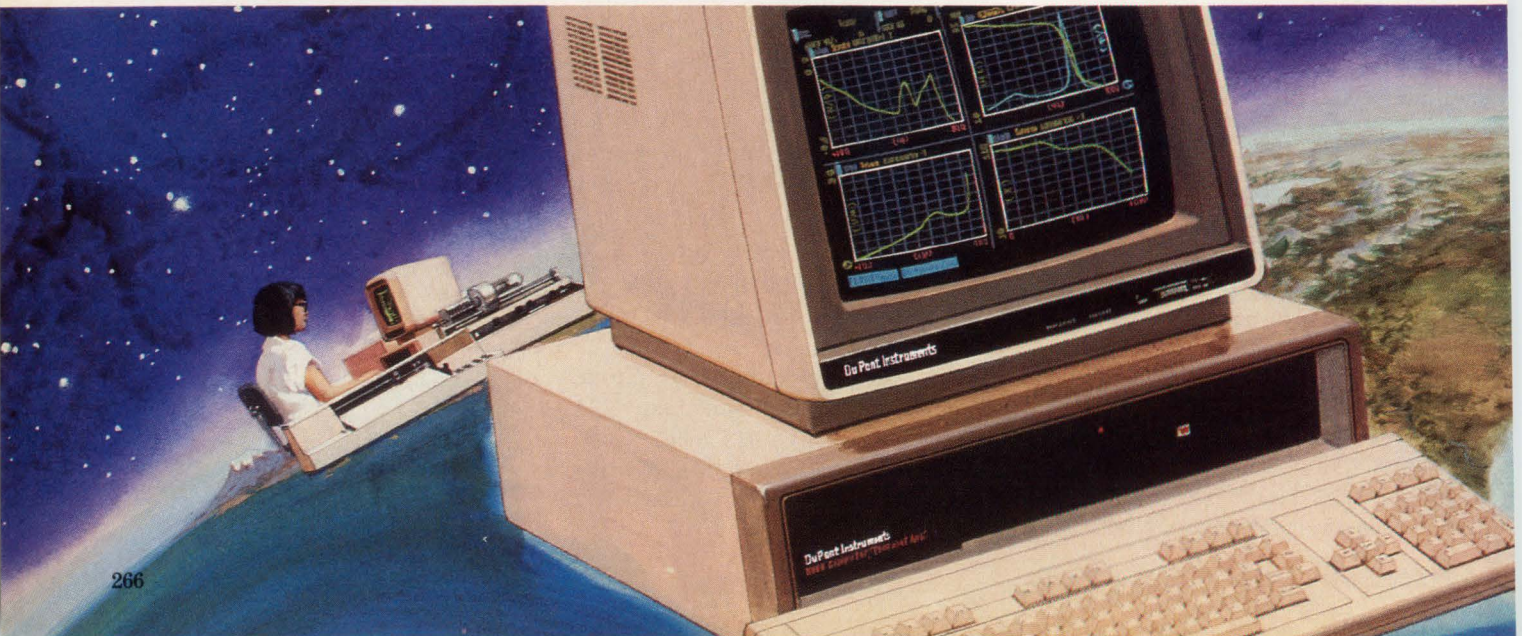
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ple, the board increases the resolution of the HP Laserjet printer to 600x300 dpi. The 2880x1024-pixel resolution of the graphics adapter delivers the WYSIWYG (what you see is what you get) capability essential to desktop publishing. A preview capability details graphics and actual typefaces at small point sizes. Screen drivers enable any software that runs under Microsoft Windows to run with this board. Hardware is included for pan and zoom. The optional raster image processor prints a formatted page at the rate of 8

sec/page. Using your application software, you can select between this Conovision image processor and the printer's native image processor. The board boots up in a Hercules-compatible mode. \$1985, including the raster image processor; without image processor, \$1325.

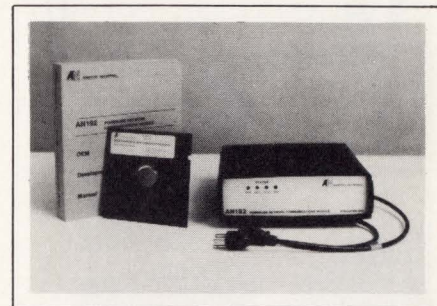
**Conographic Corp**, 17841 Fitch, Irvine, CA 92714. Phone (714) 474-1188. TLX 755453.

Circle No 366

### POWER-LINE LAN

- Delivers data at 19.2k bps
- Can support 255 master and slave units

The AN192 power-line network communications module provides LAN communications at 19.2k bps over a building's power lines. It uses modulation, demodulation, and error-control coding methods de-



signed specifically for power lines, where noise and signal distortion demand less traditional techniques for data communication. The device supports as many as 255 master and slave units; all master and slave units use identical AN192 modules. The module allows you to configure a LAN as a bus equipped with one or more central controller master units and with or without token passing. \$97 (1000).

**Adaptive Networks Inc**, Box 1020, Cambridge, MA 02142. Phone (617) 497-5150.

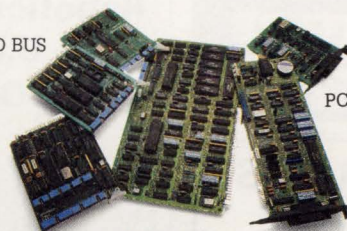
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Illustration of Dupont 9900 Thermal Analysis systems. Dupont Company, Instrument Systems Division, Wilmington, Delaware



**VIDEO DIGITIZER**

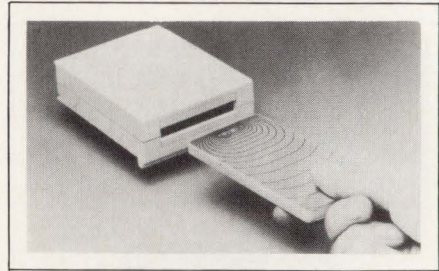
- Designed for IBM PC
- Provides 256 gray levels

The PCVisionplus frame grabber occupies a single slot in an IBM PC or compatible computer and provides 8-bit A/D conversion, which translates into 256 gray levels per pixel. The frame grabber's use of a phase-locked loop guarantees stable synchronization with VCRs, according to the manufacturer. The digitizer's offset and gain are program-

mable, and the 1024x512x8-bit memory can store multiple images. Pan, zoom, and scroll are implemented in hardware. You can write-protect each of the eight bit planes individually. The video interface accepts RS-170-, RS-330-, NTSC- (luminance only), and CCIR-formatted signals. You can access the frame memory in Z-mode (all eight bits of each pixel), X-mode (eight horizontally adjacent pixels within a single bit plane), or block-move mode (which transfers eight 8-bit pixels in a single host operation). Twelve 8-bit registers, which are mapped into the PC's I/O space, control all the functions of the board. The frame memory is mapped into the PC's memory space in 64k-byte blocks. \$1995.

**Imaging Technology Inc.**, 600 W Cummings Park, Woburn, MA 01801. Phone (800) 532-3500; in MA, (617) 938-8444. TLX 948263.

Circle No 368



**SMART CARD**

- Cards come with 64k, 256k, or 1M bits of memory
- No exposed electrical contacts

The LSI Card is an external memory card that features noncontact data transfer at a rate of 500k bps. The card and its associated reader work with programmable controllers in computer timesharing and access-control applications. The card comes with either 64k, 256k, or 1M bits of CMOS static RAM and is powered by a lithium battery. The method of data transfer is magnetic coupling. The card is about the size

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Manufactured by Liaisons Electroniques Mecaniques, SA., Switzerland.

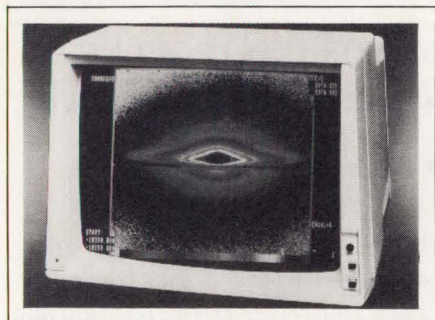
**REKCO**  
 INCORPORATED  
 P.O. Box 162  
 New Berlin, Wisconsin 53151  
 414/784-3430 • TWX 910-262-3005

CIRCLE NO 33

of a credit card; the nonvolatile RAM and the read/write coils inside the card are resistant to moisture, dirt, and oils because they are embedded in plastic. An evaluation kit with two 16k-bit memory cards, card-reader board, and documentation costs \$995.

**Orientation Inc.**, 101 Coolidge St, Hudson, MA 01749. Phone (617) 568-0509.

Circle No 369



**COLOR DISPLAY**

- High-resolution color monitor
- Offers variable scan rates

The 7241 19-in. in-line CRT offers 1080x1024-pixel resolution and a 0.31-dot pitch. The color monitor provides a 40-MHz video bandwidth, user-selected scan rates that range from 15.75 to 45 kHz, and an autoscans option. It is compatible with the IBM professional graphics adapter (PGA) and is available in cabinet, chassis, and rack-mount configurations. \$2995.

**Conrac Display Products Group**, 600 N Rimsdale Ave, Covina, CA 91722. Phone (818) 966-3511.

Circle No 370

**HARD-DISK DRIVE**

- Version offers as much as 235M bytes of storage
- For the Macintosh Plus and Macintosh 512K E

The MagicDrive hard-disk drive for the Macintosh Plus and the Macintosh 512K E is available in 20M-, 30M-, 65M-, and 235M-byte versions. Features include automatic

error detection and correction, automatic head parking, print spooling, password security, and backup utilities. The drives are equipped with the Small Computer Systems Interface, and you can daisy-chain as many as seven other SCSI devices. The drives operate under Apple's hierarchical file system (HFS) and have a data-transfer rate of 5M

bps. The operating temperature spans -40 to +140°F. The package measures 14.5x9.75x3.5 in. and weighs 11.5 lbs. Magic20, \$699; Magic30, \$899; Magic65, \$1299; Magic235, \$3399.

**Rabbit Industries**, 4505 Spice-wood Springs Rd, Suite 304, Austin, TX 78759. Phone (512) 343-0781.

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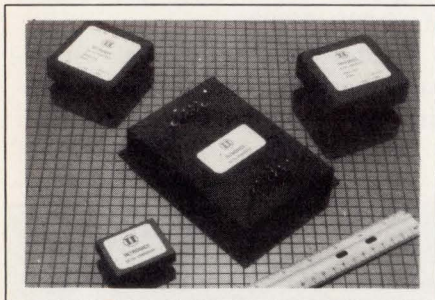
**FOR MORE INFORMATION CALL:**  
 VME Microsystems International Corp.  
 12021-N South Memorial Parkway  
 Huntsville, Alabama 35803  
 (205) 880-0444 - Telex-593128

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Photo courtesy of NASA

# NEW PRODUCTS

## COMPONENTS & POWER SUPPLIES



### CONVERTERS

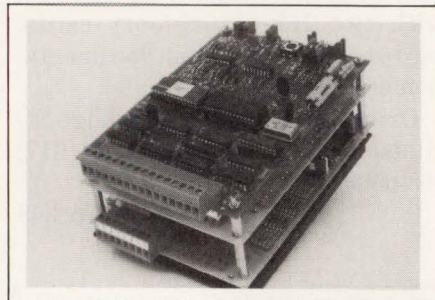
- Available as single- or triple-output modules
- All units feature 2% line and load regulation

PC-board-mountable and available as single- or triple-output modules, the KZ-100, -200, -300 and -400 are rated at 15, 25, 40, and 100W, respectively. All four power ranges

are available as a 5V dc output, or as 5, 12, and -12V dc outputs. In addition, the KZ-200C offers 5, 15, and -15V dc outputs. All units are fully isolated, protected against a variety of faults, feature 2% line/load regulation, and have efficiencies of 75% min at full load. The KZ-400 employs a 6-sided, aluminum enclosure, which serves as an RFI shield, and also an integral, large-surface heat sink. Standard units are specified for a nominal 48V dc input, but versions are available that accept 24 or 12V dc as an option. \$54 to \$150 (100). Delivery, four to six weeks ARO.

**Intronics Inc.**, 57 Chapel St., Newton, MA 02158. Phone (617) 964-4000. TWX 710-335-6835.

Circle No 372



### MOTOR CONTROLLER

- Controls both the position and velocity of dc motors
- Resonance-free operation at speeds to 600,000 pulses/sec

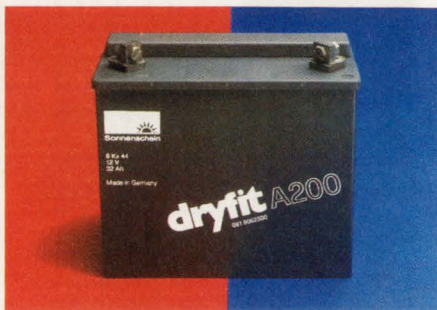
Using incremental-encoder feedback, the PIC-850 Series controller/driver controls both the position and velocity of a dc motor. It sends motion commands to the controller



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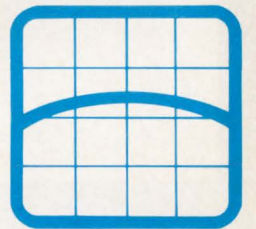
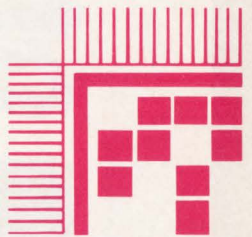
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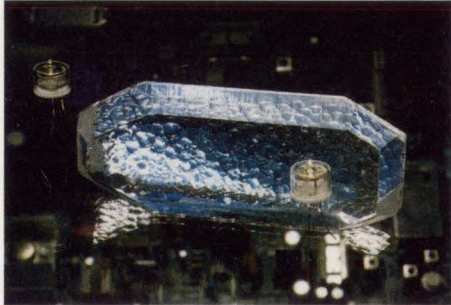
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CIRCLE NO 22

## DID YOU KNOW?

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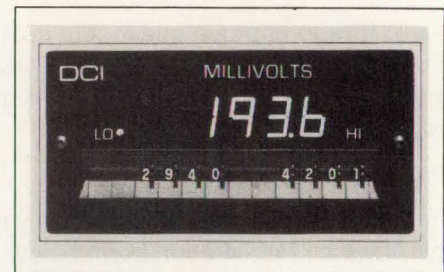
# EDN

## COMPONENTS & POWER SUPPLIES

in the form of pulses; a separate direction line controls the direction of motion. By varying the input-pulse frequency, the unit can specify the motor velocity and produce complex velocity profiles. It can control motors with a rating as high as 3 hp. Other features include resonance-free operation at speeds from 0 to 600,000 pulses per second, tolerance of position errors ranging to 32,767 counts, and an onboard 13-bit D/A converter. \$995 to \$1550.

**Galil Motion Control**, 1928-A Old Middlefield Way, Mountain View, CA 94043. Phone (415) 964-6494. TLX 171409.

Circle No 373



### CONTROLLER

- Reads out voltages in engineering units
- Either 4 or 4½ digits of LED display, readable at 30 ft

By varying the reference voltage, you can scale the display of the Series 200B panel-mounted voltmeter controller to read out a voltage in engineering units. It has dual-alarm setpoints and either 4 or 4½ digits of display with polarity. The unit has a front-panel status indicator to let you know if the parameter being monitored is below, between, or above the alarm setpoints. Standard input-voltage ranges are 0 to 200 mV and 0 to 10V. Outputs include form-C relay closure for each limit, logic-level outputs for Low, In, and High, and optional optically isolated BCD lines. The display features 0.6-in., high-efficiency-red LEDs with sculptured corners for easy reading at 30 ft. Designed for

## COMPONENTS & POWER SUPPLIES

industrial environments, the unit has a heavy-duty aluminum case, UL-listed pc-board materials, and gold-plated I/O contacts for high reliability. From \$299. Delivery, four to six weeks ARO.

**DCI Inc**, Box 215, Olathe, KS 66061. Phone (913) 782-5672.

Circle No 374



### FILTER

- Rejects second harmonic of land mobile transmitters
- Power handling specs at 375W

The Model 5201 lowpass filter's 147- to 174-MHz passband rejects the second harmonic of land mobile transmitters to eliminate interference with other off-air systems. Maximum loss and VSWR spec at 0.5 dB and 1.5:1, respectively. The harmonic rejection over a 294- to 1000-MHz range specs at 50 dB min, and power-handling capability measures 375W. The filter measures 1.6x2.05x5.75 in., has a 50Ω impedance, and comes with type-N female connectors. \$160.

**Microwave Filter Co Inc**, 6743 Kinne St, East Syracuse, NY 13057. Phone (800) 448-1666; in NY, HI, AK, and Canada, collect (315) 437-3953.

Circle No 375

### OPTOCOUPLEDERS

- Operate over a -55 to +125°C range
- Accommodate supply voltages of 4.5 to 20V

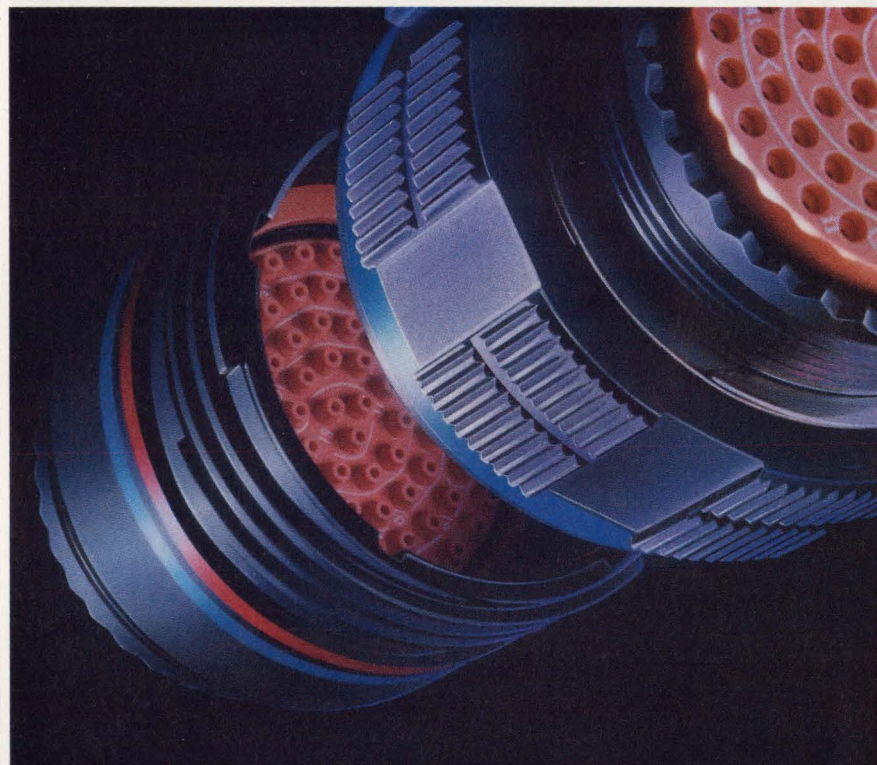
HCPL-52XX Series logic-gate optocouplers are available in single-channel (HCPL-5200) and dual-channel (HCPL-5230) designs, as well as versions tested for MIL-

STD-883 Class B compliance (HCPL-5201 and -5231). All can operate over a -55 to +125°C range. These hermetically sealed units accommodate supply voltages of 4.5 to 20V. They have low supply-current requirements of 6 mA at 5V to 7.5 mA at 20V. The HCPL-5200 and -5230 devices exhibit a guaranteed CMR of 1000V/μsec at 25°C. The

HCPL-5200 and -5230 also have a guaranteed propagation delay of 300 nsec over the full operating temperature range. All four units are housed in 8-pin DIPs. \$33.30 to \$82.95 (100).

**Hewlett-Packard Co**, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 376



These days,  
our MIL-C-38999  
can do about  
anything.

If this connector doesn't look like your typical MIL-C-38999 Series III, it isn't.

This is an ITT Cannon 38999 Special whose modified shell has been finished in conductive black cadmium over nickel. It was specifically designed for a unique aerial/ground camera application.

Future possibilities are endless. If you have a custom application for the MIL-C-38999 connector, we're the Specials expert. The complete lines of our standard Series I, II and III are also available by calling Cannon direct.

Contact ITT Cannon Military/Aerospace, a unit of ITT Corporation, 666 E. Dyer Road, Santa Ana, CA 92702. Or call 714/557-4700.

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CIRCLE NO 23

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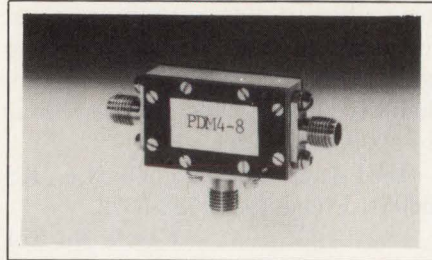
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### EDN

## COMPONENTS & POWER SUPPLIES



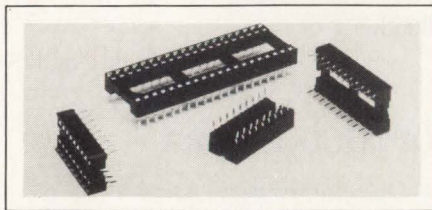
### PHASE DETECTOR

- Frequency range of 4 to 8 GHz
- Has removable connectors for drop-in applications

The PDM4-8 double-balanced phase detector provides a dc output voltage that is proportional to the phase and amplitude differences of the RF inputs. Typical specifications for the detector are a 4- to 8-GHz frequency range, an 8-dB nominal conversion loss, and a -1-dB output response of dc to 300 MHz. The output voltage with 0° and 180° inputs into a 50Ω load equals ±0.6, ±60, and ±110 mV for both RF input signals of -10, 0, and +3 dBm, respectively. With a 1-kΩ load, respective outputs measure ±28, ±150, and ±180 mV. Removable connectors allow you to use the device in drop-in applications. The device operates over -30 to +70°C. \$850. Delivery, 150 days ARO.

**RHG Electronics Laboratory Inc.**, 161 E Industry Ct, Deer Park, NY 11729. Phone (516) 242-1100. TWX 510-227-6083.

Circle No 377



### DIP SOCKETS

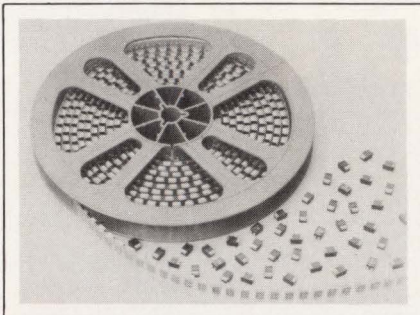
- Feature dual-face-wipe contact design for high reliability
- Crimped-tail design holds socket during soldering

Series 812 dual-beam DIP sockets are available in 8- to 48-position

versions. They feature crimped tails that hold the sockets in place during the soldering process. The dual-face-wipe contact design provides two points of contact with the IC lead. A 43° target angle allows easy, damage-free entry of device leads. The bottom of the socket is closed to eliminate solder wicking. A variety of contact materials and platings are available to meet specific application needs. A 16-position socket with phosphor-bronze, tin-plated contacts, \$0.068 (OEM qty).

**Wells Electronics Inc.**, 1701 S Main, South Bend, IN 46613. Phone (219) 287-5941.

Circle No 378



for devices having standard capacitance values. The capacitors are available in four package sizes. Voltage ratings range from 4 to 50 WV dc, and capacitance values span a 0.01 to 100  $\mu$ F range. Operation spans -55 to +85°C with no derating (to +125°C with derating). The capacitors come taped on 8- or 12-mm reels, per EIA 481A, for use

### OSCILLATOR

- Specifications guaranteed over -54 to +85°C
- 10-dBm min output power

The LNO-550 varactor-tuned oscillator is designed specifically for low-noise performance in the 550- to 775-MHz frequency range. Typical phase noise specs -112 dBc/Hz at 10 kHz from the carrier and -128 dBc/Hz at 1 MHz from the carrier. Minimum output power specs at 10 dBm. The oscillator requires only 50 mA at 12V dc and is packaged in a hermetically sealed TO-8V transistor case. All specifications are guaranteed over a -54 to +85°C range. \$325.

**Avantek Inc.**, 3175 Bowers Ave, Santa Clara, CA 95054. Phone (408) 970-2583.

Circle No 379

### CHIP CAPACITORS

- Operate over -55 to +85°C range
- Conform to IEC QC300801/001 specification

Designed for surface-mount applications, Type 293D molded-case, solid-electrolyte Tantalex chip capacitors conform to IEC QC300801/001, the new EIA industry specification



These days, our MIL-C-38999 can do about anything.

If this connector doesn't look like your typical MIL-C-38999 Series III, it isn't.

This is an ITT Cannon 38999 Special whose shell has been modified to accept printed circuit board contacts for computer system and black box applications.

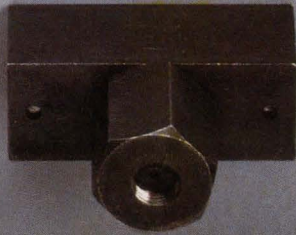
Future possibilities are endless. If you have a custom application for the MIL-C-38999 connector, we're the Specials expert. The complete lines of our standard Series I, II and III are also available by calling Cannon direct.

Contact ITT Cannon Military/Aerospace, a unit of ITT Corporation, 666 E. Dyer Road, Santa Ana, CA 92702. Or call 714/557-4700.

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with automatic placement equipment. \$0.21 (1000) for a 35V,  $\pm 20\%$ -tolerance 1- $\mu$ F unit. Delivery, 8 to 12 weeks ARO.

**Sprague Electric Co**, Box 9102, Mansfield, MA 02048. Phone (603) 224-1961.

Circle No 380

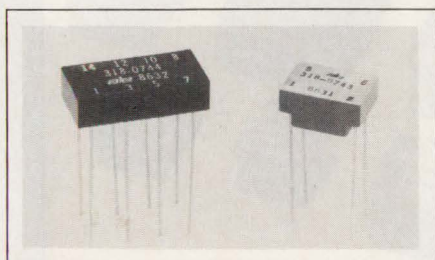
### VFD BAR GRAPHS

- Spec 1% accuracy
- Offer two optional setpoints

The 9280 Verigraph Series of bar graphs includes 100-segment vacuum-fluorescent displays that feature 1% accuracy. The 9280 is a single-display element offering two optional setpoints (either high/low, high/high, or low/low). Model 9281 offers 9280 capability plus a 3-digit, built-in display to provide 0.1% digital accuracy and full bar-graph/alarm capability. The 9282 comprises two 9280s in a single package. Each has its own display and its own input; optional alarm circuitry is available. From \$250.

**International Instruments**, Box 185, North Branford, CT 06471. Phone (203) 481-3450.

Circle No 381



### TRANSFORMERS

- Couple any Manchester-encoded data transmission
- Unaffected by electromagnetic interference

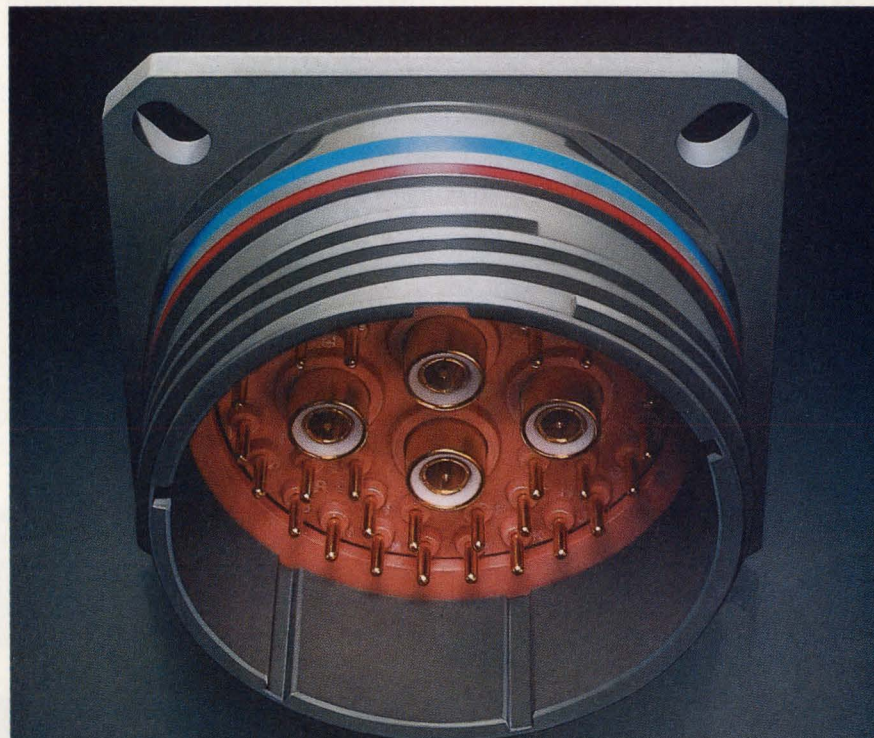
These StarLAN local-area network transformers, the 8631 and 8632, are for coupling Manchester-encoded data at 1-MHz data rates to a 92 $\Omega$  twisted-pair bus conforming to the IEEE 802.3 1BASE5 standard for LANs. Available in single- and

dual-transformer versions, the devices will handle loads of approximately 100 $\Omega$  over a range of 250 kHz to 2 MHz. In the transmitting mode, an RS-485 driver, which has pulse shaping to reduce the rise and fall times, drives the transformer so that the transmitted pulse approximates a sine wave. In the receive circuit, the limited bandwidth of the

transformer helps reduce high-frequency noise. The transformers are unaffected by interference from adjacent transformers or other sources. Dual and single versions, \$5.85 and \$3.25 (1000), respectively.

**AIE Magnetics**, 701 Murfreesboro Rd, Nashville, TN 37210. Phone (615) 244-9024.

Circle No 382



These days, our MIL-C-38999 can do about anything.

If this connector doesn't look like your typical MIL-C-38999 Series III, it isn't.

This is an ITT Cannon 38999 Special which has been modified to accept twin-ax contacts for MIL-STD-1553 data buss connector applications.

Future possibilities are endless. If you have a custom application for the MIL-C-38999 connector, we're the Specials expert. The complete lines of our standard Series I, II and III are also available by calling Cannon direct.

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# NEW PRODUCTS

## TEST & MEASUREMENT INSTRUMENTS



### PHASE STANDARD

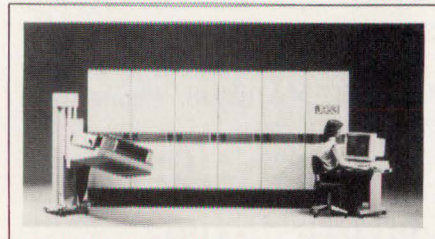
- Provides two synthesized sine waves
- Phase-angle resolution specs 1 millidegree

The Model 5000 phase-angle standard provides two digitally synthesized sine waves whose phase you can control from  $-999.999$  to  $+999.999^\circ$ . The instrument's phase-angle resolution is 1 millidegree over its frequency range of 1 Hz to 100 kHz. Each sine wave is individually adjustable from 100 mV to

11.9V. Phase accuracy from 1 Hz to 1 kHz is  $\pm 0.003^\circ$  typ, decreasing to  $\pm 0.05^\circ$  at higher frequencies. The unit is fully programmable over the IEEE-488 bus. The sine-wave outputs have  $-74$ -dB max total distortion. \$9400.

**Clarke-Hess Communication Research Corp.**, 220 W 19th St, New York, NY 10011. Phone (212) 255-2940.

Circle No 383



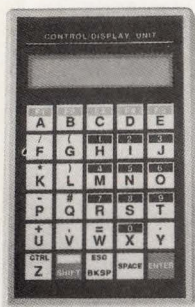
### VLSI DEVICE ATE

- Operates two test heads simultaneously
- Each I/O channel has a test vector and a timing generator

The J953 VSLI tester can test two devices at 50-MHz rates (100-MHz

multiplexed). Its pattern generator backs up each test channel with 4M bytes of test-vector memory. Each of the tester's two test heads includes 256 I/O channels and has its own parametric measurement unit (PMU). Each pin also has a timing generator that can generate 5-nsec pulses having 100-psec timing resolution. Each  $50\Omega$  channel has 30 pF of capacitance. The tester's waveform-edge placement accuracy is  $\pm 250$  psec max. You program the tester with the company's proprietary, C-based language. \$1,100,000

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to \$2,500,000. Delivery, 32 to 36 weeks ARO.

**Teradyne Inc**, Inquiry Systems, 25 Drydock Ave, Boston, MA 02210. Phone (818) 888-4850.

Circle No 384



**OPTICAL METER**

- Measures power of both long and short wavelengths
- Portable unit runs from battery or ac

The AQ-2101 optical-power meter consists of a main unit and one of three sensors. The AQ-2703 sensor, for large-diameter cable, covers wavelengths from 0.8 to 1.7  $\mu\text{m}$ ; the AQ-2702, for connector inputs, and the AQ-2704, for nonconnector applications, measure 0.4- to 1.1- $\mu\text{m}$  wavelengths. The main unit's 4-digit LCD shows readings in dB, dBm, mW,  $\mu\text{W}$ , and nW. Depending on the sensor used, the instrument can measure optical power from 1 nW to 100 mW without an attenuator. The 5-oz unit measures 6 $\times$ 3 $\times$ 0.4 in. AQ-2101, \$480; AQ-2702 sensor, \$260; AQ-2703 sensor, \$1830; AQ-2704 sensor, \$340.

**Ando Corp**, 7617 Standish Pl, Rockville, MD 20855. Phone (301) 294-3365.

Circle No 385

**MIXED ATE**

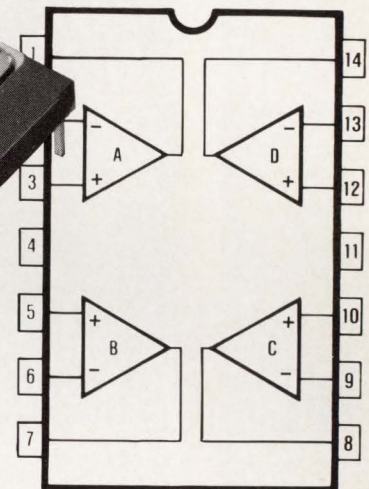
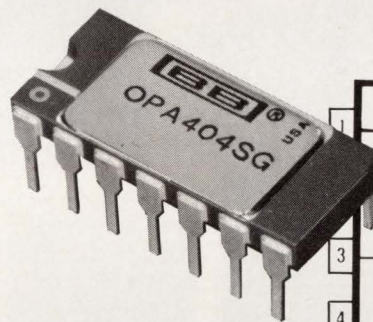
- Handles chips that have both analog and digital functions
- Runs at 128M samples/sec with a 128-MHz analog bandwidth

The HP 9480 mixed-signal IC ATE handles such devices as a flash converter, a DAC, and DSP chips. The 128-pin tester supplies eight chan-



nels of dc stimulus from 100  $\mu\text{V}$  to 100V at 1 pA to 100 mA. The ac waveform generator supplies 128-MHz sine waves or 32-MHz arbitrary waveforms. The tester's waveform digitizer samples to 16 bits at 1 MHz and to 12 bits at 20 MHz. Its digital pattern generator and pattern analyzer both have 16k sample memories and run at 128M samples/

# Fast Quad FET Op Amp Settles to 0.01% In 1.5 $\mu\text{s}$



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- Offset voltage .....  $\pm 750\mu\text{V}$  max
- Bias current .....  $\pm 4\text{pA}$  max
- Noise at 10kHz ..... 12nV/ $\sqrt{\text{Hz}}$
- Price ... from \$8.95 U.S. (100s)

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Improving Analog Productivity

## INSTRUMENTS

sec. The tester runs Unix System V with real-time extensions. You program it in a proprietary language that the company claims is somewhat like Pascal. Approximately \$650,000. Delivery, 14 weeks ARO.

**Hewlett-Packard Co.**, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 386

### INTERFACES

- Provide a variety of control lines for BCD instruments
- Available as either RS-232C or IEEE-488 interfaces

The Digital232 and Digital488 interface boxes provide RS-232C and IEEE-488 interfaces, respectively, to 40 TTL-level I/O lines. The 40



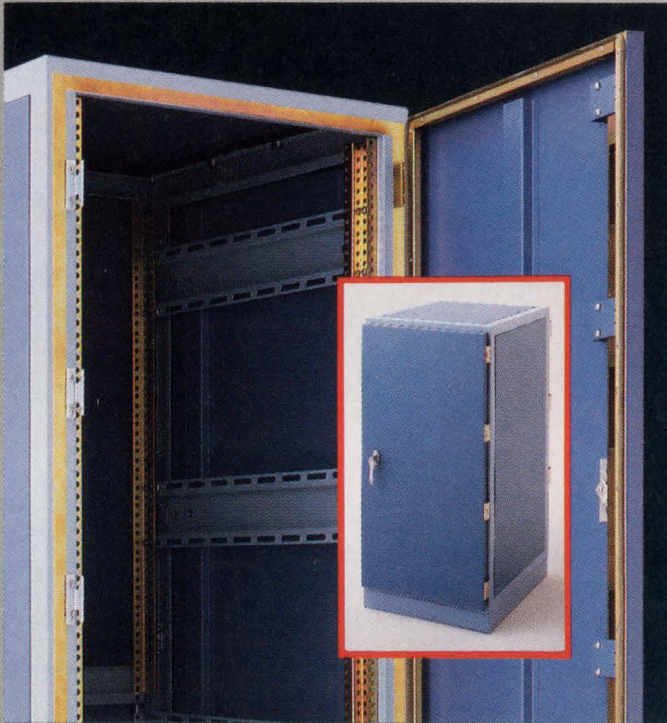
lines divide into five 8-bit ports. You can set up each line as an input or an output under computer control. In addition, the interfaces have handshake and control lines that can interface with a variety of digital and BCD devices. These lines provide trigger, clear, inhibit, latch, and service-request functions. Each model costs \$595.

**Iotech Inc.**, 23400 Aurora Rd, Cleveland, OH 44146. Phone (216) 439-4091.

Circle No 387

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Available for FCC and military shielding requirements



  
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Emcor Products

Emcor offers two levels of standard catalog EMI/RFI shielded enclosures: one to meet FCC requirements and another to meet levels of attenuation required by the military. Both product lines have been tested to MIL STD 285. Emcor also has the capability to provide custom requirements not covered by standard catalog items.

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1600 Fourth Avenue N.W., Rochester, Minnesota 55901 (507) 289-3371

### WORD GENERATOR

- Executes algorithmic patterns
- Has 40-MHz clock rate

The PG4064 digital word generator works with the company's logic analyzers. The unit generates data words that are as much as 64 channels wide and 4k words deep, or as little as 2 channels wide by 128k words deep in the serial mode. It supports algorithmic pattern generation in accordance with data tables and 3-level-deep nested loops. It has a 40-MHz (max) clock rate and generates 25-nsec pulses. \$19,100. Delivery, 60 days ARO.

**Gould Design & Test Systems Div.**, 19050 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 538-9320; in CA, (408) 988-6800. TWX 910-338-0509.

Circle No 388

### BENCHTOP ATE

- Has as many as 1000 analog or 320 digital test points
- Fits in the space of an office copier

The Checkmate benchtop ATE system performs digital and analog

For winning 8051 family designs that meet your time-to-market deadline and engineering budget—you'll need development tools, particularly In-Circuit Emulation.

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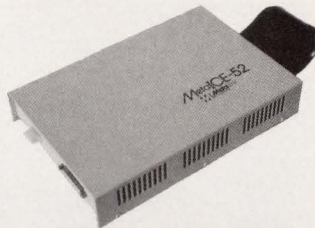
With our MetaICE-52 tool for example, you can add real time, transparent 8052-family In-Circuit Emulation to your lab PC for \$3,295—a fraction of the cost of large, dedicated development stations.

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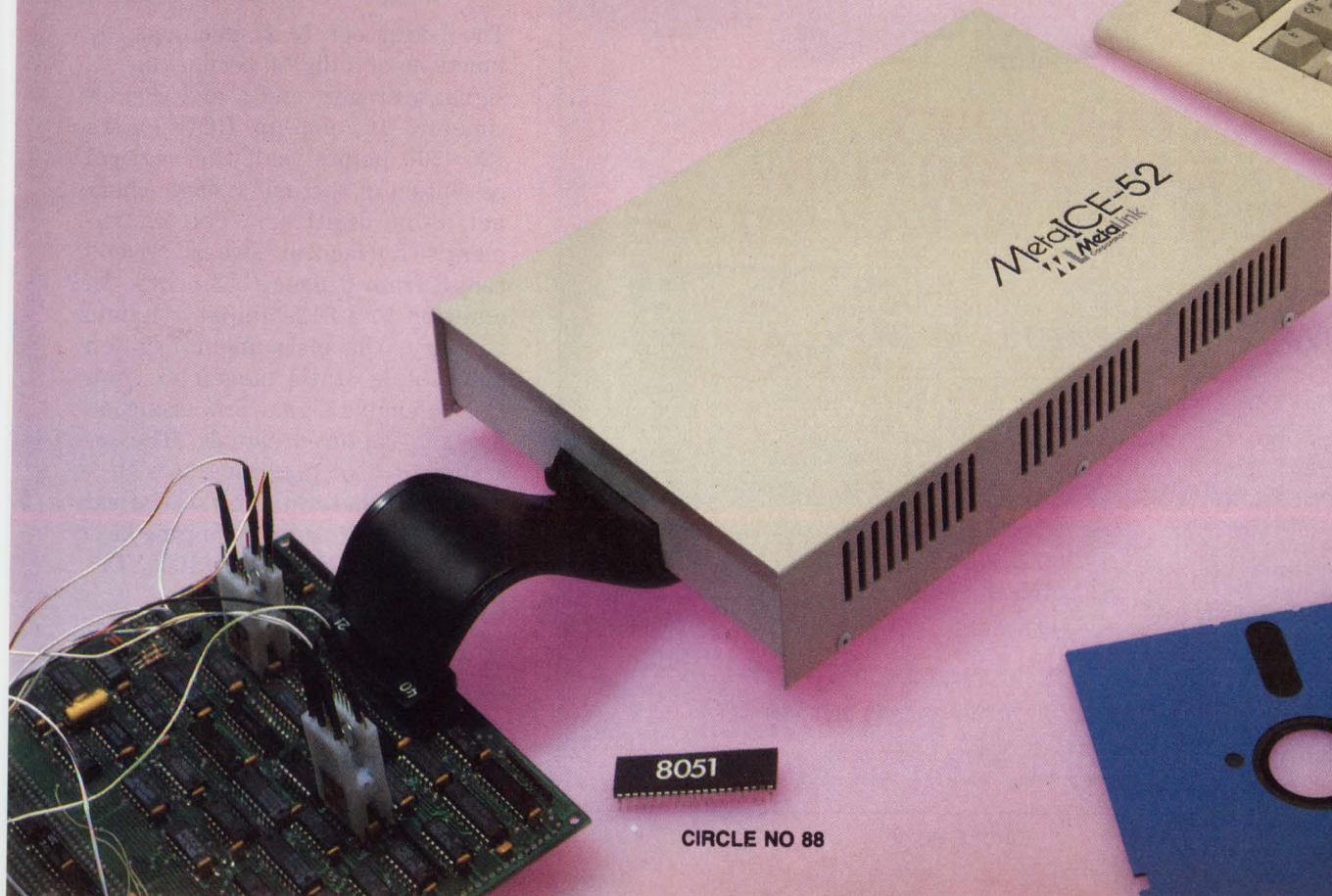
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# PC-hosted 8052 ICE for under \$3500!



CIRCLE NO 88

functional tests as well as in-circuit tests. It fits into the space needed for the average office copier. The instrument accepts as many as 21 measurement or function pc boards: a counter/timer, function generator, digital multimeter, logic analyzer,  $\mu$ P emulator, voltage source, general-purpose I/O board, and IEEE-488 interface. For digital tests, you



can equip the unit with 320 input channels and 20 output channels, or you can equip it as a 64-channel, 100-MHz logic analyzer. You can measure digital parameters with 25-nsec accuracy and 5-nsec resolution. For analog tests, the unit offers 6-wire, guarded measurements and can have as many as 1000 test points. It includes a color monitor and two 3½-in. floppy disks. \$25,000 to \$50,000.

**Marconi Instruments**, 3 Pearl Ct, Allendale, NJ 07401. Phone (800) 233-2955; in NJ, (201) 934-9050.

Circle No 389



**LCD SCOPE/METER**

- Combines digital scope and multimeter
- Folds up into carrying case

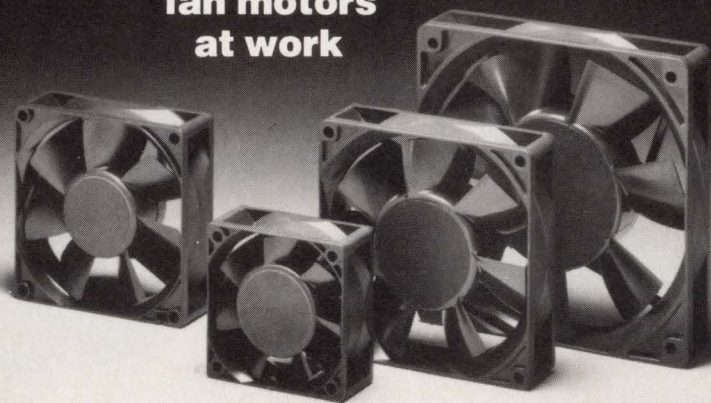
The Iskrascope LCD combines the functions of a digital oscilloscope, a signal averager, and a digital multimeter. Its pop-up LCD shows 120×200 points (half the vertical resolution of the unit's single-channel, 8-bit digitizer). The instrument's horizontal sweep speeds range from 5  $\mu$ sec to 3.5 hrs. In addition to a 512-sample dynamic memory, the instrument has ten 200-sample static memories. You can do simple signal processing on live and captured signals. The instrument also functions as a 3½-digit multimeter having statistical capabilities. It has a membrane keyboard and weighs 8 lbs. \$1500. Delivery, 12 to 14 weeks ARO.

**Iskra**, 222 Sherwood Ave, Farmingdale, NY 11735. Phone (800) 862-2101; in NY, (516) 753-0400. TLX 221257.

Circle No 390

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## CAE & SOFTWARE DEVELOPMENT TOOLS

### MATH LIBRARY

- Contains more than 400 routines
- Optimized for use with 8087 and 80287 math coprocessors

Optimized for use with the 8087 and 80287 math coprocessors in IBM PC, PC/XT, PC/AT, and compatible machines, Mathpac is a library of more than 400 routines that are written in ANSI 77 Fortran and assembly language. All the routines perform their computations with extended 80-bit precision and make their results available, with either 32-bit or 64-bit precision, in IEEE-standard floating-point format. The routines can operate on both real and complex numbers. You can link these routines to application programs involving computer graphics,

scientific computing, numerical analysis, statistical analysis, signal processing, image processing, process control, and simulation. You can plot as many as 16 variables on the same graph, and you can choose monochrome or color graphics. The routines include vector operations, matrix operations, FFTs, 2D and 3D image rotation, predictor-corrector and integration operations, and various forms of numerical optimization. Because the calling sequences are standardized, you can add your own routines to the library. \$495.

**Systolic Systems Inc**, 1065 E Brokaw Rd, San Jose, CA 95131. Phone (408) 286-0421. TWX 910-338-2290.

Circle No 391



### DATA ACQUISITION

- Features menu selection of setup and sampling functions
- Provides sampling rates as high as 62,000 samples/sec

Stream-16 is a software routine that lets you store A/D conversions, ac-



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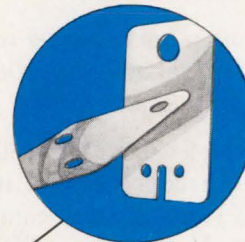
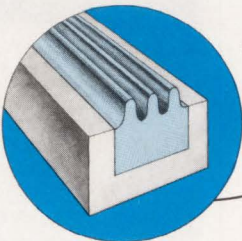
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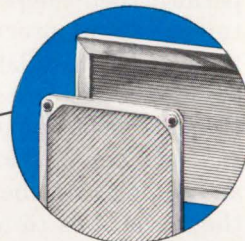
Our *Molded-in-place EMI/EMP cover seals* combine design freedom with serviceability and cost effectiveness.



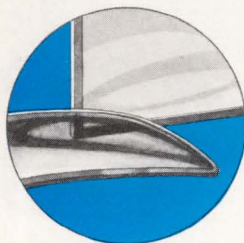
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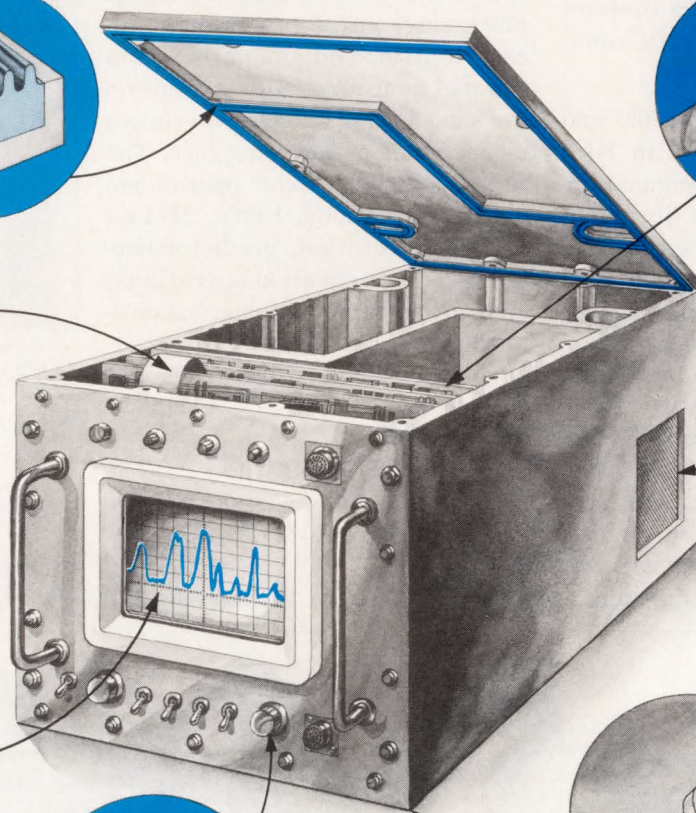
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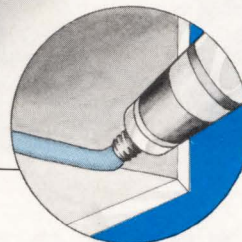
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quired from the vendor's DAS-16 or DAS-16F boards, to a hard-disk file at sampling rates as high as 62,000 samples/sec. Using the DAS-16's DMA feature, the program transfers the samples initially to a circular memory buffer. As soon as data enters the buffer, the program starts writing it to the disk. Pointers keep track of the as-yet-unwritten data. The program is menu driven; from the menu, you can select the channels to scan, the trigger mode, the sampling rate, the file name, and other options. Comprehensive error-checking routines warn you of probable errors in the data stream. The vendor's DAS-16 and DAS-16F boards (formerly called DASH-16 and DASH-16F) can scan eight differential or 16 single-ended analog channels and provide 12-bit A/D conversions at rates as high as 50,000 samples/sec (DAS-16) and 100,000 samples/sec (DAS-16F). Stream-16, \$250.

**Metrabyte Corp.**, 440 Myles Standish Blvd, Taunton, MA 02780. Phone (617) 880-3000. TLX 503989. **Circle No 392**

**ADA FOR 1750A  $\mu$ Ps**

- Lets you develop Ada software for MIL-STD-1750A machines
- Provides Ada Programming Support Environment (Apse)

Running on a VAX/VMS host, the Telegen2 1750A development system lets you develop software targeted for embedded computers based on the MIL-STD-1750A architecture. The development system includes an Ada cross-compiler and a set of object tools consisting of an Ada linker, a library manager, a library tool set, and an Ada runtime library. The cross-compiler comes with a number of tools, including a source-level debugger and

language tools. The combination of this software and the VAX/VMS operating system provides programmers with an Ada Programming Support Environment (Apse). The package complies fully with MIL-STD-1815A specifications and will be submitted for validation in the first quarter of 1987. License fees, \$17,000 to \$86,000, depending on the hardware configuration and the number of tools licensed.

**Telesoft**, 10639 Roselle St, San Diego, CA 92121. Phone (619) 457-2700. TLX 855300.

**Circle No 393**

**ASIC SIMULATOR**

- Runs on the IBM PC/AT and compatibles
- Simulates networks of standard cells

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PC/AT and compatible machines. Its simulations of standard-cell networks take into consideration some characteristics of actual cell performance. By specifying the upper and lower limits of circuit operating conditions, you can adjust the timing within the cell modules for voltage, temperature, and processing effects. The simulator obtains its cell

models from the vendor's standard-cell libraries and allows you to use the same regular, analog, cluster, and telescoping macros that you would use on the mainframe version (which runs on Prime computers). You specify the network, the cell list, the number of cells in the design, and the process technology to be used for fabrication, and the sim-

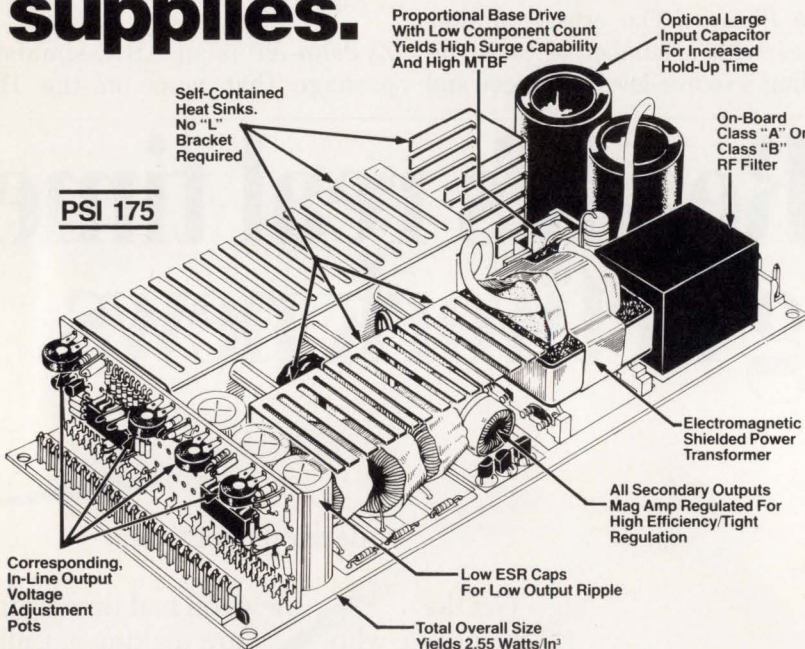
ulator then predicts the final die size of your ASIC chip. Because of the memory limitations of the PC/AT, you may have to divide a complex chip into sections and perform a preliminary simulation of each one separately. However, you can upload the sections to the vendor's mainframe to recombine the sections and perform a full simulation. \$2500.

**ZyMOS Corp**, 477 N Mathilda Ave, Sunnyvale, CA 94086. Phone (408) 730-5400.

Circle No 394

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### COMPILER

- Translates ISO data structures to C structures
- Facilitates upgrading of MAP/ TOP systems

The ASN.1 compiler is based on CCITT standard X.409; it accepts protocol data units (PDUs) defined in ASN.1 (Abstract Syntax Notation One) and generates the corresponding C language structures for manipulation by upper-layer protocols. Thus, in developing an application program, you don't have to re-code the PDUs manually from the complex ASN.1 syntax. The compiler is particularly valuable when you're upgrading ISO application- and presentation-layer protocols to conform to the MAP (manufacturing automation protocol) 3.0 and TOP (technical and office protocol) 3.0 standards. The compiler is available only as part of the vendor's ISO Upper Layer Protocol Package, which includes C source code for the File Transfer and Management and Common Application Services Elements kernel application-layer protocols. License fee, \$19,750; per-copy royalties are additional; current licensees of either package will receive the compiler at no charge.

**Communication Machinery Corp**, 1421 State St, Santa Barbara, CA 93101. Phone (805) 963-9471.

Circle No 395

CIRCLE NO 31



**CAD FILE TRANSFER**

- *Transfers drawings from PC-based station to CAD system*
- *Can transfer plot files to any PCI-format plotter on a network*

Cadvance 25, version 2.0, now lets you transfer 2-dimensional drawings generated on a PC-based workstation to the vendor's System 25 high-end CAD system. The program is menu-driven and allows use of mice and digitizers. It also lets you use nested commands and macros, and it provides facilities for extracting symbols from a database. Status prompts and case-sensitive on-line help screens aid the user in the creation of drawings. Included in the enhancements is a translator that converts the drawing files to a format that can be read by the vendor's System 25 multiuser computer. A LAN version allows you to transfer converted files directly to the host computer over the network.

Cadvance 25, \$500; LAN version, \$1500; telecommunications package, \$500.

CalComp, 2411 W La Palma Ave, Anaheim, CA 92801. Phone (714) 821-2142.

Circle No 396

**C LIBRARY**

- *Provides all C functions needed for measurement and control*
- *Lets you use an IBM PC for program development*

The AD1836 run-time library of C routines allows you to program the vendor's  $\mu$ MAC-5000 measurement and control system in C. The library includes program-development tools; real-time interrupt-service routines; analog and digital I/O routines; and routines for counting, communications timing, and failure detection. If you use an IBM PC as a development system, you can use a

library routine to download the executable code to the  $\mu$ MAC-5000. You should use the Aztec C compiler (versions 3.2D and 3.2E only) from Manx Software Systems (Shrewsbury, NJ). \$495 for the PROM containing the AD1836 library, an IBM PC-compatible disk containing an I/O library, a public-domain file transfer program to work with the downloading routines in the PROM, and a manual.

Analog Devices, Literature Ctr, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 329-4700.

Circle No 397

**TEST SOFTWARE**

- *For vector-network-analyzer data*
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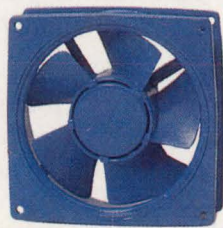
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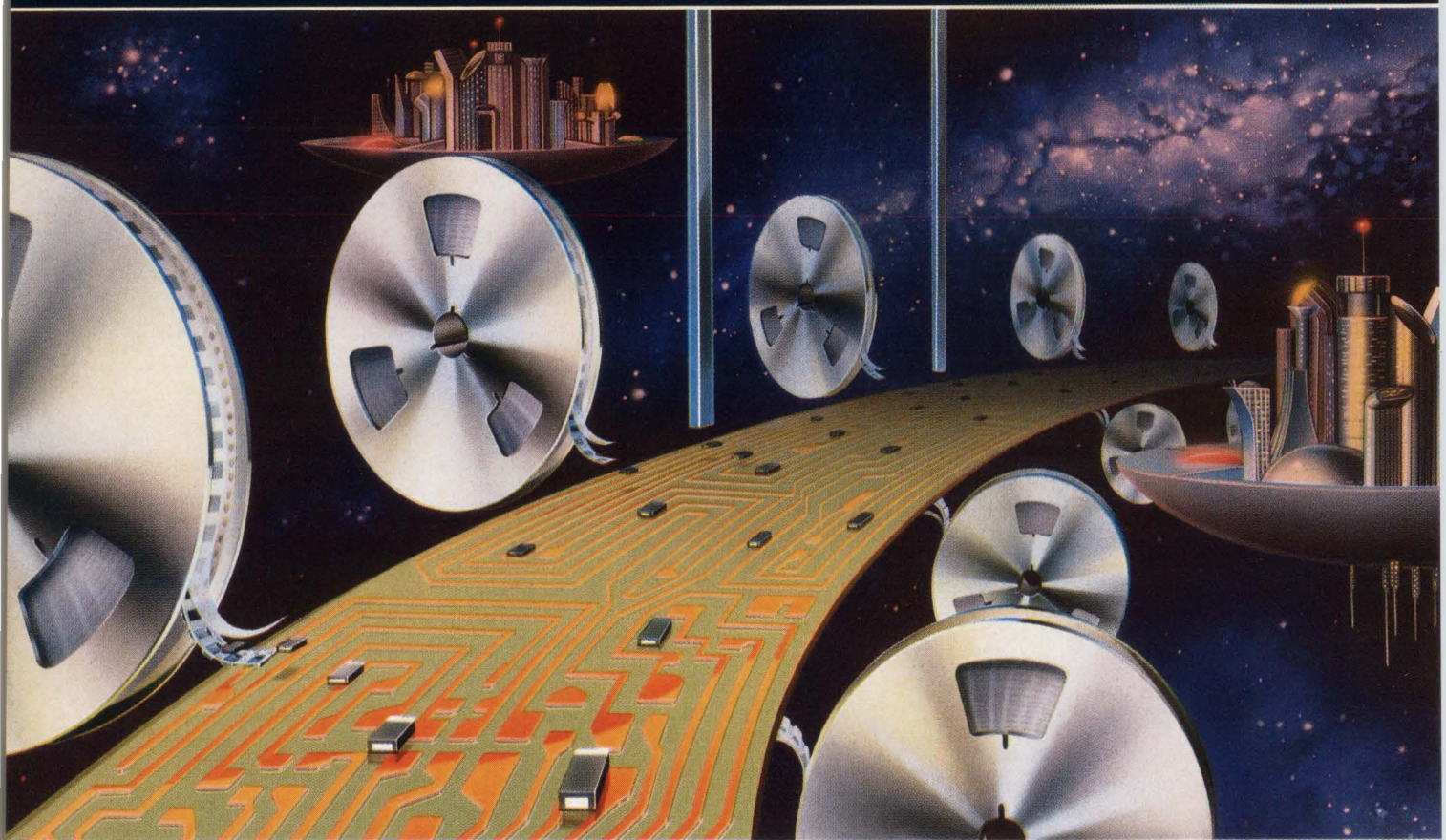
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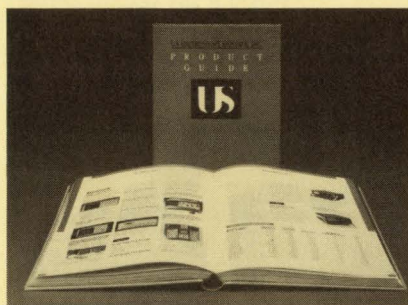
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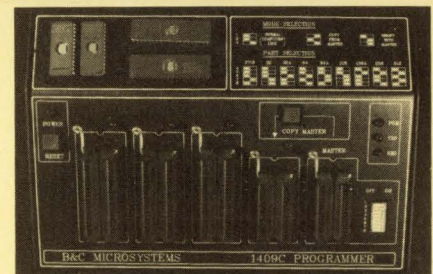
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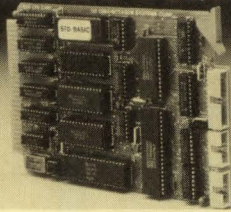
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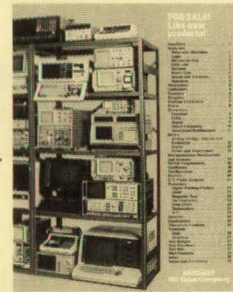
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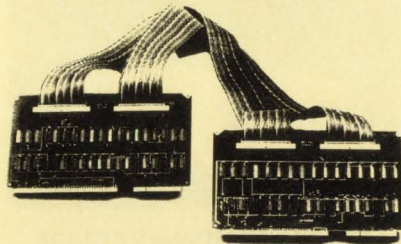
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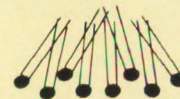
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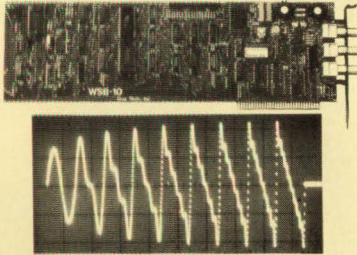
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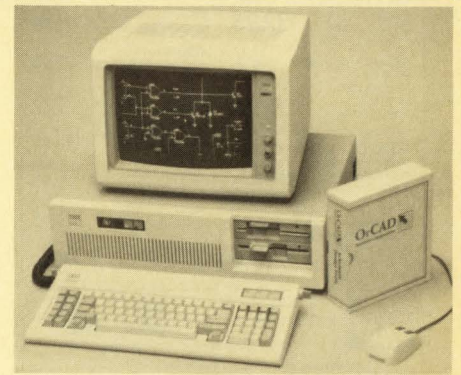
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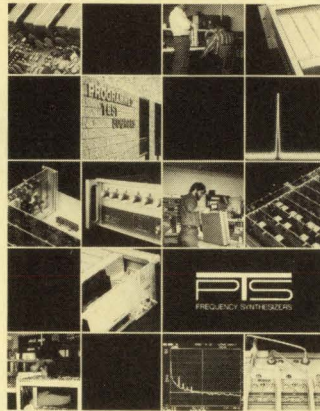


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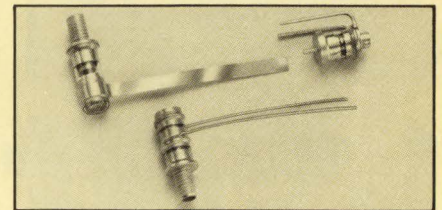
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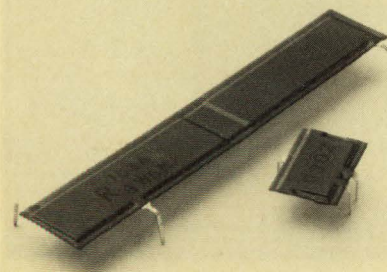
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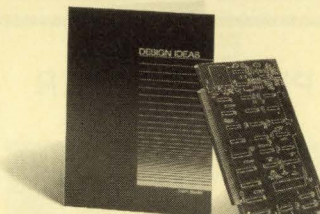
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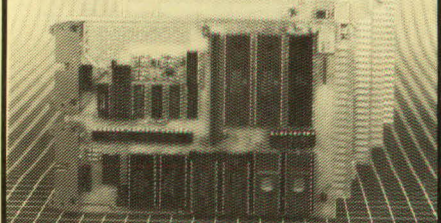
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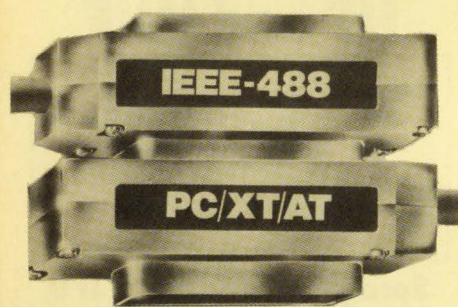
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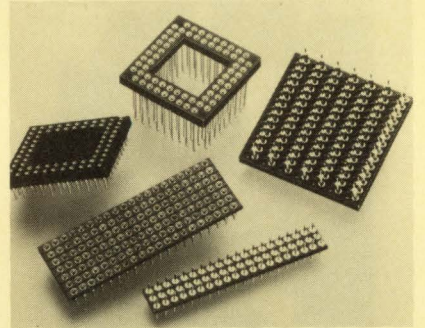


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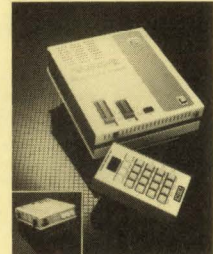
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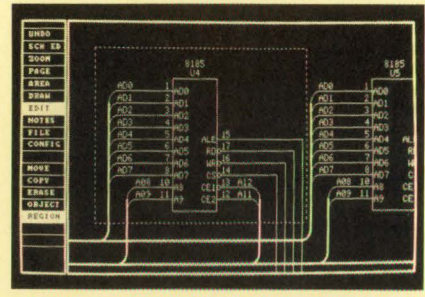


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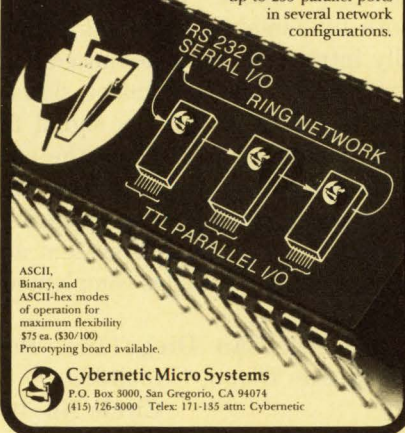
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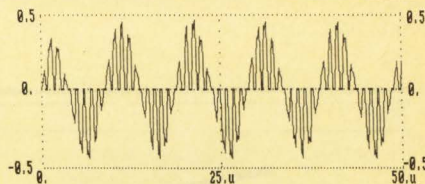


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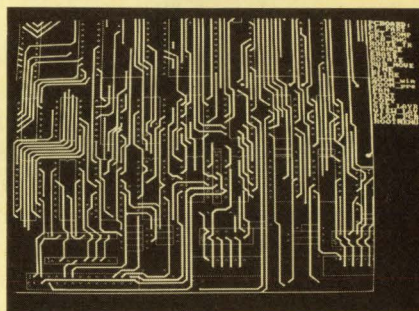
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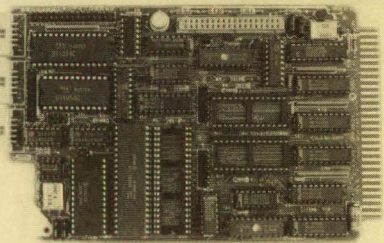
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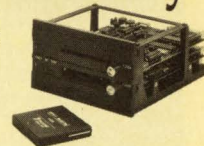
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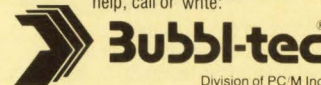
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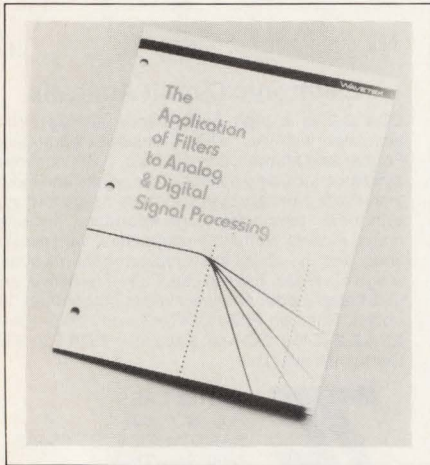


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CIRCLE NO 234



**Handbook is source of data on signal filtering**

*The Application of Filters to Analog & Digital Signal Processing* is a design handbook for both inexperienced and seasoned engineers. It's a useful primer for those unfamiliar with the concepts and applications of filters in signal-processing systems, and it's a solution-oriented technical reference for signal-pro-

cessing problems. The book begins with fundamental ideas and gradually introduces more-advanced concepts. Topics include analog signals and their spectra; noise; signal filtering at the input and at the output; sampling signals; and types and characteristics of filters, programmable filters, and ATE system applications. Illustrations complement the text.

**Wavetek San Diego Inc**, Box 85265, San Diego, CA 92138.

**Circle No 400**

new sections: listings that cross-reference vendors' and manufacturers' product lines; and charts that tell which companies offer which business-communication systems according to line size. It also includes product guides to PBX and key systems and related business-equipment technologies, as well as narrative reviews of industry trends. The 413-pg book costs \$45 for NATA members; \$75 for nonmembers.

**North American Telecommunications Association**, 2000 M St NW, Suite 550, Washington, DC 20036.

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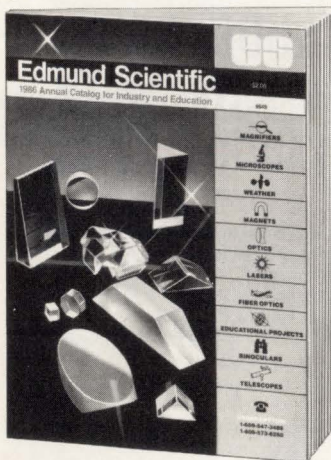
This year's edition of the North American Telecommunications Association's source book includes, as usual, a directory, a buyer's guide, and market overviews on telecommunications services and products. This year, the book contains several

**App note addresses amplifier measurements**

This application note (345-1) describes gain, gain-compression, isolation, and return-loss and SWR measurements using the HP 8757A scalar network analyzer and the HP

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## LITERATURE

8350B sweep oscillator. The 16-pg document also includes definitions of those five parameters, as well as measurement sequences for each. The 3-hole-punched note concludes with two appendixes: one addressing the choice of detection modes available for the scalar network analyzer, and the other describing the sweep oscillator. A list of references is also included.

Hewlett-Packard, Box 10301, Palo Alto, CA 94303.

Circle No 402



### Library of handbooks

This company's 1987 technical library of process-measurement handbooks consists of five books that address pressure, strain, and force; temperature; flow and level; pH and conductivity; and test instrumentation and tools. Each book contains specification information, reference sources, technical guidance, and pricing.

Omega Engineering Inc, Box 4047, Stamford, CT 06907.

Circle No 403

### Guide helps when selecting CAE/CAD for PCs

Organized into 13 categories relevant to the selection of a PC-based CAD/CAE system, this buyer's guide poses questions you should ask yourself when considering such a system. The 13 categories are hardware configuration, software maturity, schematic capture, schematic libraries, schematic design tools, output-file utilities, pc-board design, pc-board libraries, pc-board design tools, manufacturing-data output, database management, support and maintenance, and price.

EDN January 22, 1987

Aptos Systems, 4113 Scotts Valley Dr, Scotts Valley, CA 95066.

Circle No 404

### App note demonstrates A/D conversion scheme

This application note, *Analog-to-Digital Conversion Using Voltage-to-Frequency Converters*, demon-



strates several methods of using V/F converters as building blocks in an A/D conversion scheme. For instance, the document diagrams and discusses pulse-counting and period-timing techniques for interfacing with a 1-chip microcomputer. It also suggests possible sources of errors and solutions. Illustrations include the AD651 as a 16-bit-resolution

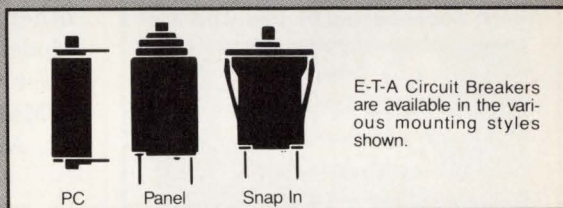
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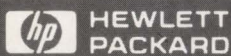
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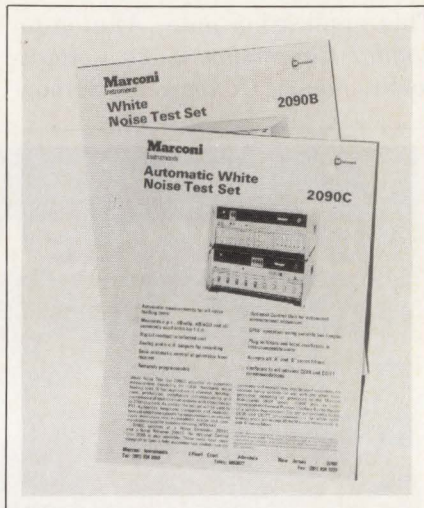
6557 N. Lincoln Ave., Chicago, IL 60645  
312-677-7660

## LITERATURE

A/D system.

Analog Devices, Literature Ctr,  
70 Shawmut Rd, Canton, MA  
02021.

Circle No 405



### Brochures characterize white-noise test sets

These two brochures present information on the manufacturer's two white-noise test sets. One of the brochures, consisting of eight pages, describes Model 2090B, which measures noise and intermodulation on wideband, multichannel telecommunications systems. The other brochure provides details, block diagrams, and specifications. The other, a 12-pg pamphlet, details Model 2090C, an automatic white-noise test set.

Marconi Instruments, 3 Pearl Ct, Allendale, NJ 07401.

Circle No 406

### Catalog presents coaxial products

This 25-pg catalog (#187) contains pricing information on the company's coaxial adapters, connectors, attenuators, and terminations as well as its coaxial cable assemblies (flexible and semirigid). In addition, the catalog covers twin-axial adapters and connectors.

Pasternack Enterprises, Box 16759, Irvine, CA 92713.

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CIRCLE NO 39

# NEW BOOKS

**Standard Handbook for Electrical Engineers**, edited by Donald G Fink and H Wayne Beaty. 2248 pgs; \$72.50 until January 31; \$86.50 after that date; McGraw-Hill Book Co, New York, NY, 1986.

This book is the twelfth edition of a standard reference created by over 100 experts who have contributed material on their engineering specialties. The book devotes full coverage to the generation, transmission, distribution, control, conservation, and application of electric power. Included are discussions of the impact on nuclear energy caused by the Three Mile Island nuclear plant accident, as well as the growing importance of alternative energy sources such as wind power, solar power, and magnetohydrodynamics. A list of standards completes the treatment.

**Transducers in Mechanical and Electronic Design**, by Harry L Trietley. 392 pgs; \$59.75; Marcel Dekker Inc, New York, NY, 1986.

This book provides detailed information on the operation, features, circuits, and applications of a variety of transducers, including resistive, magnetic, capacitive, self-generating, electrochemical, and semiconductor transducers, as well as potentiometers and variable-resistance sensors. Measurement applications include temperature, pressure, position, flow, vibration, shock, acceleration, conductivity, pH, and more. For each, typical circuitry is discussed. The book focuses on how to select the right sensor for your application.

**What Every Engineer Should Know About Engineering Workstations**, by Justin E Harlow III. 147 pgs; \$24.75; Marcel Dekker Inc, New York, NY, 1986.

The purpose of this book is to survey the types of hardware and software that characterize engi-

neering workstations and that differentiate them from traditional CAD/CAM systems. It identifies the appropriate applications for engineering workstations as well as points out some applications for which engineering workstations may well be the wrong answer. It explains some justifications for buying a workstation.

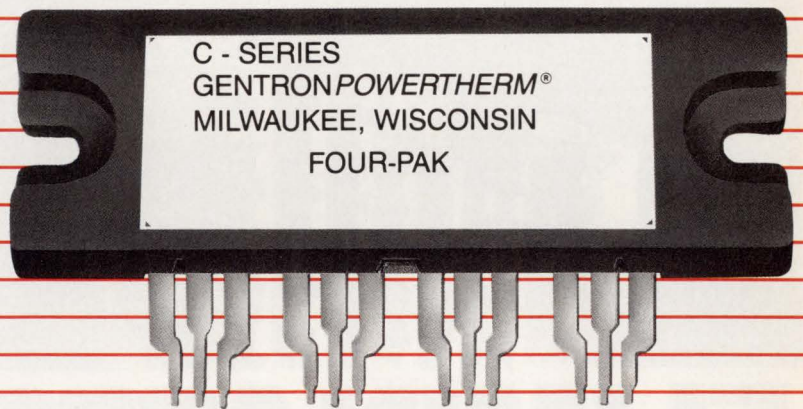
**Low-Temperature Electronics**, edited by Randall K Kirschman. 491 pgs; \$63.50; IEEE Press, New York, NY, 1986.

This book provides a survey of the characteristics and applications of electronic devices at low temperatures for both digital and analog uses. The book includes 72 reprinted papers on materials, sys-

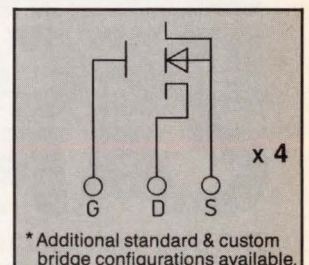
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**Random Signals Estimation and Identification**, by Nirode Mohanty. 626 pgs; \$59.95; Van Nostrand Reinhold, New York, NY, 1986.

Covering both analog and digital signal processing, this book offers a computational approach to estimation, detection, spectrum estimation, recursive filtering, smoothing, prediction, and identification. Two hundred and fifty examples illustrate how to apply these methods in such fields as communications, radar and electro-optical engineering, and physical science. Among the topics the book examines are linear-systems analysis; ergodicity and entropy; and band-limited, nonlinear, and adaptive systems.

**The Effects of Radiation on Electronic Systems**, by George C Messenger and Milton S Ash. 587 pgs; \$54.95; Van Nostrand Reinhold, New York, NY, 1986.

This book, written by radiation-effects specialists, describes the pertinent radiation types and the corresponding damage to electronic components, circuits, and systems. It covers such topics as radiation-susceptible physical and electrical properties of semiconductors; nuclear radiation environments and corresponding modern simulation sources; new radiation-hard systems; modern dosimetric methods; statistical analysis for hardness design; and hardness assurance. It explains how to incorporate rad-hard systems into all phases of construction of electronic systems, as well as how to implant them into systems already built. Other topics include post-radiation annealing of semiconductors, single-event upset, electro-

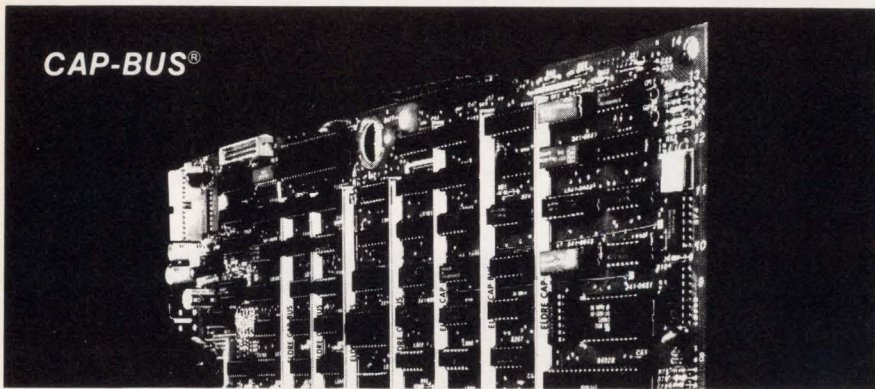
magnetic pulse, and gallium arsenide and new radiation-resistant devices. Charts, graphs, and tables are included showing damage to modern semiconductor types caused by various kinds of radiation.

**Undersea Lightwave Communications**, edited by Peter K Runge and Patrick R Trischitta. 621 pgs; \$60.80; IEEE Press, New York, NY, 1986.

This book describes recent progress in undersea light-wave technology for transoceanic communications systems. It contains 43 chapters, grouped into 10 parts; each part begins with background information about previous undersea systems and ends with a look at the technological options for the next generation of undersea light-wave systems.

**Software Portability**, by Olivier Lecarme and Mireille Pellissier Gart. 219 pgs; \$29.95; McGraw-Hill Book Co, New York, NY, 1986.

The essential techniques that are necessary to understand and achieve software portability are presented in this book. The authors explain how to develop a program that will not only meet current job requirements, but that can be transported to a different system for future projects. A series of case studies about language processors and operating and programming systems demonstrates portability in specific situations. The manual discusses the major problems in software portability, the software tools of transport, the linguistic means of transport, and language-implementation methods. It also explains how to cut the cost of software development and increase the life span of a program's effectiveness and how to produce software that is more efficient and more broadly applicable.



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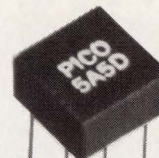
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MSA-0370	4.5	12.5	5.5	10.0	A	16.10
MSA-0420	3.5	8.5	7.0	15.0	C	18.45
MSA-0685	4.0	16.5	3.0	1.5	D	1.30
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# PROFESSIONAL ISSUES



## Laid-off engineers find the experience painful but survivable

Deborah Asbrand, *Associate Editor*

In 1985, Steven Soltz knew that his employer, Foxboro Co, was going through difficult financial times. Among the company's products were process-control systems for oil refineries, and when falling oil prices disrupted business for the company's Saudi Arabian clients, Foxboro felt the pinch, too. For the previous two years, the company had been regularly laying off employees. Rumors usually circulated about which employees would be the next to go, but Soltz didn't initially take them seriously: He thought that his five years with the company provided him an extra measure of security.

In the summer of 1985, though, Soltz began hearing his own name among those rumored to be laid off next. In December, the 29-year-old systems engineer received the news: "My boss told me in a

backhanded way, 'you'd better start looking for work.'"

Soltz is among thousands of electronics-industry employees who have lost their jobs to layoffs and plant closings. The exact number is unknown because until this year the US Bureau of Labor Statistics (BLS), the national keeper of unemployment statistics, hasn't kept track of the number of Americans who are unemployed because of layoffs. This year, however, Title 3 of the Job Training Partnership Act will require the government to initiate a program to compile layoff statistics, and beginning in April, the BLS will issue regular reports on national layoff and plant-closing figures.

Some states, however, do track the number of laid-off individuals among their unemployed, and the

Illustration by Michael Young

numbers do not bode well for the electronics sector. For example, in Massachusetts in 1985, a year in which that state's healthy economy kept its unemployment rate at 3.9%, more than 18,000 workers were laid off. The American Electronics Association (AEA) estimates that 12,000 of those jobs were cut from the electronics sector. The AEA also reports that 20,000 electronics jobs in California were eliminated in 1985. Layoffs continued in 1986, as employees at such companies as Tektronix, Texas Instruments, and AMD received pink slips.

For whatever reasons they are let go, however, employees are left with the same array of aftereffects: emotions that include anger, embarrassment, fear, and self-doubt; concern about their personal finances; hours of unfilled time; and, most important, the search for a new job.

### Receiving the news

For some engineers, like Soltz, being laid off caps several months of speculation about their futures with their present employers. "After a while it became a joke," Soltz recalls. "During the summer, a bunch of us started making plans to do things together because we'd heard there was a layoff coming up and we were part of it."

For others, job termination comes swiftly and unexpectedly. Product-support engineer Les Davis had been working for NCR in San Diego, CA, when a recruiter contacted him about an opening at nearby Metacomp, a maker of intelligent I/O controllers. After 10 years of work for such large employers as E-Systems, Texas Instruments, and NCR, Davis decided to interview for the position and was offered the job. Six months after joining the company, Davis was among 25 employees who were called into the cafeteria and informed that they were being let go as of that day. "I was in shock," he says. "I couldn't believe the way

they handled it." He received one week's salary as severance pay.

William Cain remembers his first reaction when his boss at GE-Datel (Mansfield, MA) told him he would be laid off in April of last year. "I was livid," the 46-year-old instrumentation engineer remembers. "I knew the [profitable] circumstances under which my group was operating. It took me a couple of days to cool down and realize it was a business decision." GE-Datel had decided to cut back on development of the small-size limit controllers on which Cain was working.

Even more powerful than the sense of anger that a dismissed employee feels, however, can be the sense of embarrassment, especially for those working with classified or proprietary materials. Employers "aren't going to ask you to be out in an hour, but they want you out as soon as possible," Cain says. "That's part of the trauma. Someone who's been a trusted employee suddenly comes under suspicion. Cleaning out your desk is done under guard and you walk out under scrutiny. It's



Michael Young

embarrassing. But you learn to be stoic." Cain speaks from experience: The layoff from GE-Datel was his second. In 1971, he was laid off from an engineering position at RCA.

Laid-off employees say that the extra time they have to themselves can be a mixed blessing. "You can use the time to get close to your family and catch up on things," Cain says. "I was able to exercise more regularly, watch my diet better, and get my garden in early." Davis, laid off in October, chose to wait until after the Thanksgiving and Christmas holidays to begin looking for a new job. Among the first decisions he and his wife made was to take their 3-year-old son out of the day-care center in which he was enrolled. "One occupational hazard for men," Davis says, "is that as fathers they don't get to know their kids." Over the next six months, Davis cared for their son while his wife went to her job as a program analyst at NCR.

Although the extra time allows laid-off employees to catch up on family matters and household projects, it can also become an enemy—sometimes there's too much time in which to contemplate financial strain, loss of self-esteem, and lingering self-doubt.

Rick Aseltine's layoff in June 1986, couldn't have come at a worse time for him. Aseltine, a medical-instrumentation engineer, and his wife were in the process of applying for a mortgage for the 7-room house they planned to build. Aseltine's biggest fear was that his layoff would jeopardize the couple's chance to obtain the loan and maybe even cost them the deposit they had put on the house. But assisted by an understanding loan officer, they got the loan and moved into their house later that summer.

Even Aseltine, busy as he was meeting bank appointments and packing his family's possessions for the move, found he had extra time on his hands. With his wife gone to work and his son at a day-care cen-

ter, the 33-year-old engineer found the days became long. "There were times when I had nothing to do all day," he recalls.

During his first few months of unemployment, Dan Hagget, a 32-year-old hardware engineer, devoted his time to volunteer work and to helping his family sell a hotel they owned in northern Maine. But as his months of unemployment stretched into a year, he began running out of projects—and money. Having spent most of his personal savings, Hagget went to work part time for a friend who owned a commercial-cleaning business. "At least you could see your accomplishments," he says wryly.

In fact, the long stretches of time away from work can deliver a damaging blow to a dismissed employee's often already fragile self-esteem. The laid-off employee must work hard to keep the potentially serious consequences of a layoff at bay. "I've seen friends completely devastated," Davis says. "I've seen marriages break up over it." Says Soltz: "The first conversation you have when you meet someone is usually 'what do you do?' When I told people I was laid off, they gave me a funny look."

Davis believes he weathered unemployment better than some people because his family, not his job, is the center of his life. "You can't blame the industry for your situation. If a company's profits are going downhill and they're not making money, you should expect you're going to have a good chance of being laid off. Their number one goal is to make a profit." Yet even he admits that he had to battle to maintain his self-esteem.

Overriding any concerns about personal finances and the struggle to maintain a positive self-image is an engineer's need to find a new job. Some companies give laid-off employees a hand in finding new employment. They allow ex-employees to use their telephones and typing services. Other employers hire job-

placement specialists to assist their laid-off employees in securing new jobs. Most ex-employees, however, find that unemployment means a lone campaign of sending out scores of résumés, placing telephone calls to prospective employers, attending job fairs, and going on interviews.

A job hunt that stretches over several months can be one of the

500 résumés, he remembers. Companies might interview more than 100 applicants for a single job. "There were so many engineers out of work, it was a struggle. I was considering leaving the profession. I even took salesmen's exams with insurance companies. That was the most desperate time for me."

Making Cain's 1971 job hunt more

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*"Cleaning out your desk is done under guard and you walk out under scrutiny. It's embarrassing. But you learn to be stoic."*

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most depressing work-related experiences. Davis, who had moved to Massachusetts with his family, says he went on 25 interviews and discovered that in more than a few cases, the companies did not have actual openings but had called him in for an "informational" interview. Job fairs, too, were depressing, he says. Many of those in attendance had been out of work for a long time, and many company representatives were there more to collect résumés than to interview for actual jobs. "If you're unemployed and have the time, it's worth a try," says Cain. "But I went to two or three and always went in and out in 15 minutes."

Cain viewed his earlier layoff as an advantage in handling the experience this time. Having learned that the experience was difficult but survivable, he had an added degree of confidence when he looked for work this time.

In fact, looking for an engineering job in Massachusetts in 1971 was much more difficult than his most recent job search, Cain says. "Back in the 1970s, everyone was touched by layoffs in some way. Those were bad times when a lot of engineers got out of the business. It was a very low ebb for the profession." An advertised position in the Route 128 area's largest newspaper, *The Boston Globe*, might draw more than

frustrating was the fact that, at RCA, he had worked as a manufacturing engineer. His engineering experience prior to that had been in design. But when he interviewed for design positions after his layoff, he found that interviewers reacted coolly to his time in manufacturing. "The perception in industry was that I had abdicated my design role," he says. Cain considers that premise to be unfounded. "It's absurd when you look back. Design skills don't dissolve in two years. But I've been leery of taking a manufacturing job ever since."

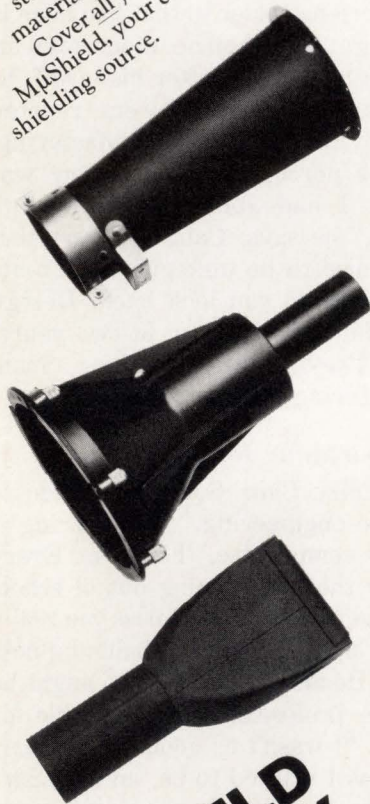
## Opportunity for change

Unlike Cain, Soltz did decide to leave engineering. "Engineering is very competitive," he says. "Every year the kids coming out of school are getting better. Unless you really stay up on it, you fall behind quickly." He also felt that there might be other professions more suitable for him. "I wasn't as good at engineering as I wanted to be, and I wasn't really interested enough to invest the time to get better."

He had always been interested in sales, however, so he decided to apply for sales positions. He sent hundreds of inquiries—and got hundreds of rejection letters. Self-doubt began to gnaw at him. After two months of unemployment, job interviewers began asking Soltz why he

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## PROFESSIONAL ISSUES

had been out of work for so long. His disposition changed, and he became morose and ill-tempered. "It was a depressing time," he remembers. "You start thinking, 'I'm no good, no one wants me.'" At one point, he threw a party to pick up his spirits, and, in a lighthearted moment, burned all of his rejection letters.

"When I was going through my most depressing time, I wasn't that excited about going back to work," says Soltz, who eventually got a job as a salesman for Astromed, a West Warwick, RI, maker of recorders for the aerospace and medical industries. "You get into a routine, and you don't want to break it." Happily, he found that once he went back to work, he felt as though he'd never been away.

Luck was an integral factor in helping Rick Aseltine obtain his job as engineering manager for C R Bard's Instrumentation Division in Danvers, MA. Anxious to secure a job and increase his chances of getting a mortgage, Aseltine was close to accepting a job that would mean a round-trip daily commute of more than two hours. But before accepting the offer, he decided to interview for one more job—a quality-analysis position that would have been an unusual choice for someone with his medical-instrumentation background. After reviewing his résumé, his interviewer turned to him and asked him flatly, "Why are you here?" Aseltine admitted the financial bind he was in. The interviewer knew of an opening for an engineering manager at the company and suggested that Aseltine interview for it. He did, and later was offered the job.

William Cain now works as director of engineering at LFE Corp's Instruments Div in Clinton, MA, where he supervises the design and development of single-loop PID (proportional-integral-differential) controllers. Like other engineers who have been laid off, he says the experience has permanently affected his attitude toward his em-

ployer. "It was a hardening experience to me. It taught me that no matter what level of engineering or management you're at, you never want to give up your basic design skills . . . Even though I'm director of engineering, I still spend a portion of my day with engineers to make darn sure I stay technical. If

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*Engineers who have been laid off say the experience permanently affects their attitudes toward their employers.*

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you've been laid off, you develop a mild paranoia."

Aseltine, too, sees changes in the way he views his employer. "It affects the way I look at things around me." He now feels much more protective of his career. "I'm much more cautious now about decisions I make," he says. Davis, now a systems support specialist for Apollo Computer (Chelmsford, MA), says the lesson he learned is "don't be confident in hiring on with a company that is doing well. You could be here today and gone tomorrow. That's not sarcasm. It's a realistic point of view."

For some, the aftereffects of a layoff include a continuing sense of loss about the potential that a former job held. Aseltine says he has watched the market grow for the emergency-communication device he worked on for his former employer. "Being laid off is more discouraging now because the product I was working on is finding more interest. . . . I knew this was an area we should pursue. Looking at the interest in the product now, [I realize] we could've been on the leading edge."

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# CAREER OPPORTUNITIES

## 1987 Editorial Calendar and Planning Guide

**EDN**  
Editorial Emphasis

EDN News

Issue Date	Recruitment Deadline	Editorial Emphasis	EDN News
Feb. 19	Jan. 29	Analog IC s; Artificial Intelligence; CAE	Closing: Feb. 4 Mailing: Feb. 20
Mar. 4	Feb. 12	Computer Graphics; Communications ICs; Test & Measurement	Closing: Feb. 20 Mailing: Mar. 16
Mar. 18	Feb. 26	CAE; ASICs; Electro '87; Show & Product Preview	
Mar. 31	Mar. 10	Electro '87 Show Issue; Design & Development Tools; ICs & Semiconductors	
Apr. 15	Mar. 26	Microprocessor Technology; Software Development; Digital ICs	Closing: Apr. 2 Mailing: Apr. 23
Apr. 30	Apr. 9	Communications Special Issue; ASICs; Test & Measurement	
May 14	Apr. 23	Analog Technology Special Issue; ICs; Test & Measurement	Closing: Apr. 30 Mailing: May 21
May 28	May 7	Computer Peripherals; Software; Power Sources/Devices	
June 11	May 21	Math ICs; CAE; Computers	Closing: May 28 Mailing: June 18
June 25	June 4	ASIC (Semcustom ICs) Directory; Analog ICs; Surface-Mount Technology	
July 9	June 18	Product Showcase-Volume I; ICs & Semiconductors; Software	
July 23	July 2	Product Showcase-Volume II; Computers & Peripherals; Test & Measurement Instruments	Closing: June 25 Mailing: July 16

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**AMERICAN COMMUNICATIONS COMPANY:** Participates in major installations for telecommunications

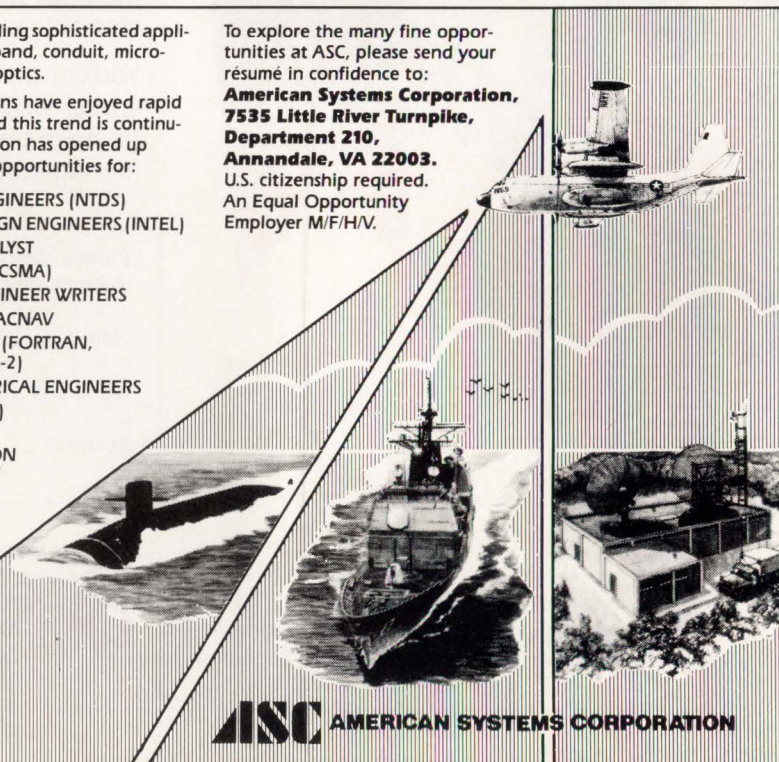
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To explore the many fine opportunities at ASC, please send your résumé in confidence to:

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Requires degree in EE, CS, Math or Physics and design experience including Digital Systems hardware and software architecture, redundancy management, and system integration and test. AFCS background needed.

## **ENGINEERING PROJECT MANAGER**

Will direct military avionic hardware development, to include overseeing design team, handling budget and scheduling responsibilities, and coordinating manufacturing and quality functions. Requires BSEE and 7-10 years military electronics experience, preferably to include flight control systems.

## **MARKETING MANAGER**

Will be responsible for new product marketing. Requires 5 years experience with DoD acquisition procedures in avionic electronic systems.

## **RADAR SYSTEMS DESIGN ENGINEERS**

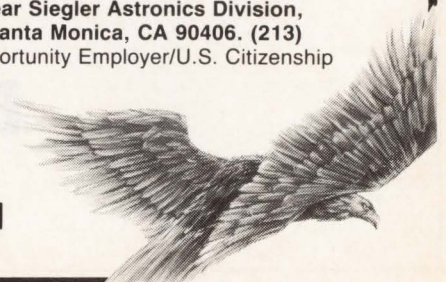
Will define systems requirements for new ground-based radar technologies, interface with Army development labs and provide technical support. Will also apply ECM/ECCM and high speed digital signal processing techniques for radar systems design, simulation and analysis. Requires BSEE and 5+ years relevant experience.

## **REAL-TIME SOFTWARE ENGINEERS**

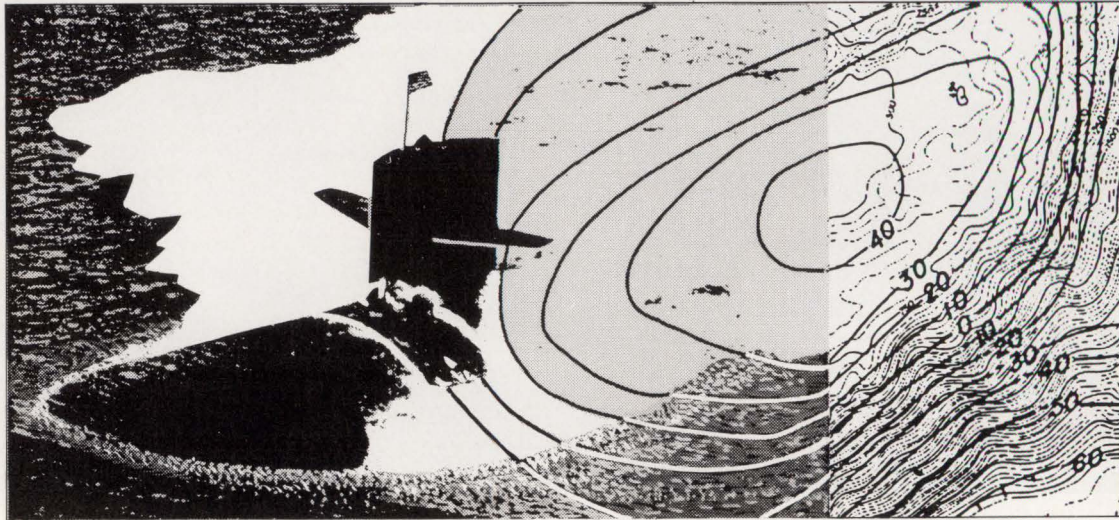
Requires BS in EE, CS or Math and 3+ years in avionics software including Minicomputer/Microprocessor Systems, Real-time and Assembly/higher languages for military applications.

In addition to a competitive compensation package, LSI Astronics offers an attractive Southern California location and professional relocation assistance. For consideration, send resume and salary history to: **Chuck Doyle, Dept. F04, Lear Siegler Astronics Division, 3400 Airport Ave., Santa Monica, CA 90406. (213) 452-6745.** Equal Opportunity Employer/U.S. Citizenship Required.

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### ELECTRONICS DESIGNERS

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—Military Electronics

### Another Surprise... Buffalo

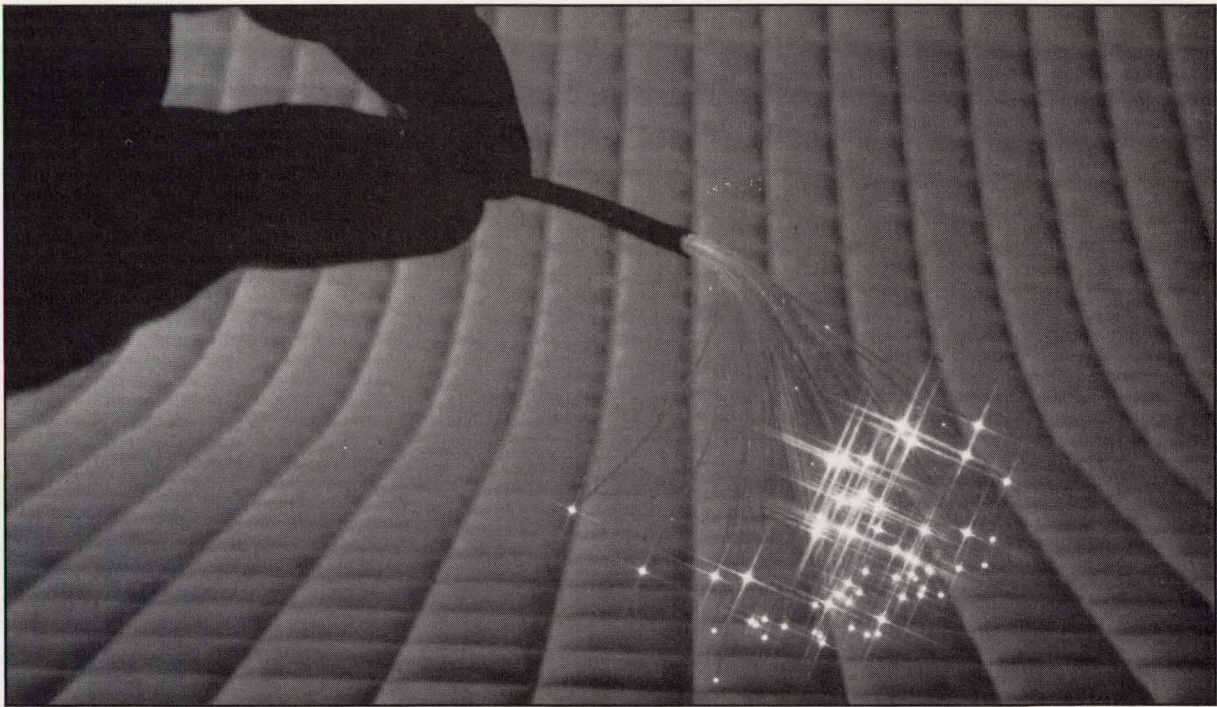
The Niagara Frontier is one of the great places to live in the U.S., rated in the top 15 areas in Rand McNally's "Places Rated Almanac." Housing costs are very reasonable, well below those of most comparable areas. Along with SUNY Buffalo, the largest educational facility in New York State, there are 17 colleges and universities and excellent elementary and secondary school systems. You'll find extensive medical facilities and health care costs are lower than any other metro area in the U.S. And there's lots to do. Enough restaurants to keep you visiting a new one every night for the next five years; plenty of major league and college action for sports fans; over 500 parks, playgrounds and 20 skiing areas within a 90 mile radius; and the Niagara River has more species of fresh water fish than any other in the U.S. The area is known for its excellent recreational activities.

We offer competitive salaries and generous benefits that include stock savings, health insurance, retirement program, liberal vacations and scholastic assistance. Get in touch with us, we have a great many pleasant surprises in store for you. Send your resume in confidence to: **D.W. Pearl, Dept. EDN-M-122, Bell Aerospace Textron, P.O. Box One, Buffalo, NY 14240.**

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- Digital Systems Design
- Real-Time Software Systems Design
- Guidance and Control Design
- Test Systems Design
- Radar Systems
- Reliability/Quality Assurance
- Electro-Optics Design
- Missile Guidance Design

Engineering positions require a minimum BS degree in Electrical or Computer Engineering, Physics or Mathematics and at least 3–5 years' experience with real-time command and control systems, radars, missile guidance and digital equipment.

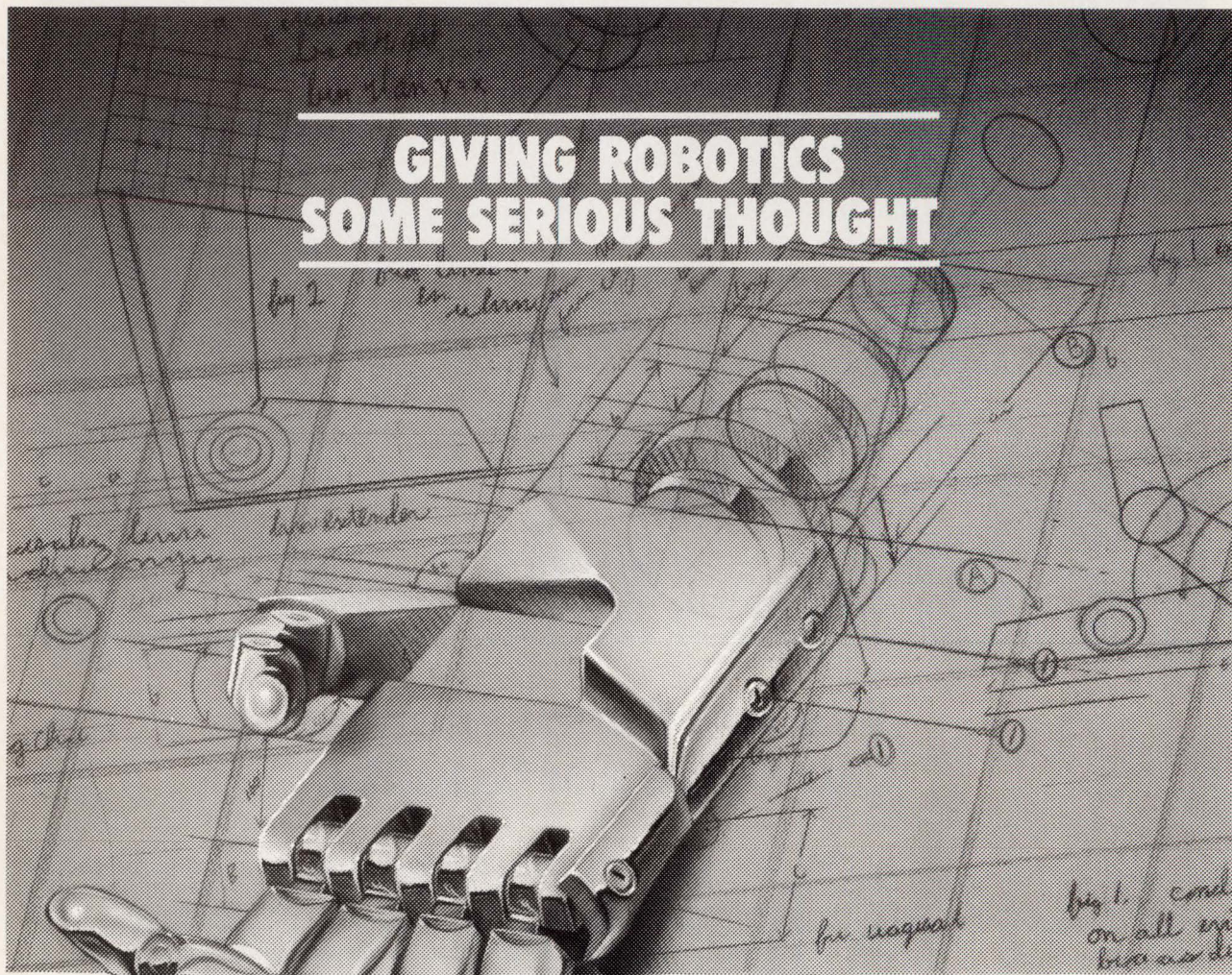
Raytheon offers excellent salaries and many company-paid benefits as well as Stock Ownership and Savings and Investment Plans and liberal relocation assistance. Please send resume with salary requirements to:

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# Raytheon

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## GIVING ROBOTICS SOME SERIOUS THOUGHT



management and C<sup>3</sup>I systems, and real-time displays for command and control systems.

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We invite you to be a part of this effort. If you have experience in robotics or artificial intelligence, give some serious thought to a career at Martin Marietta Aerospace. We have opportunities available in the following areas:

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- **Real-Time Computer Graphics for Animation**
- **AI Programming**
- **Operation Analysis**
- **C<sup>3</sup>I**
- **Biomedical Engineering**

If interested please send your resume to: Martin Marietta Baltimore Aerospace, Employment Dept. EDN187, 103 Chesapeake Park Plaza, Baltimore, Maryland 21220. U.S. Citizenship Required. An Equal Opportunity Employer m/f/h/v.

Imagine a robotic device that will allow the operator to see and feel what the robot is seeing and feeling. A device controlled easily and reliably, in much the same way as a human hand. This is "telepresence." And it's a technology being advanced at Martin Marietta Baltimore Aerospace.

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# New 1987 Survey explores the latest trends in engineering salaries, technology and career opportunities

**Y**ou know how quickly technology can change. But, do you know how much salaries change...or how much difference there is in compensation levels for engineering professionals who perform comparable functions...or how much salaries vary by industry or geographic location?

## Comprehensive review of salaries, trends and demand

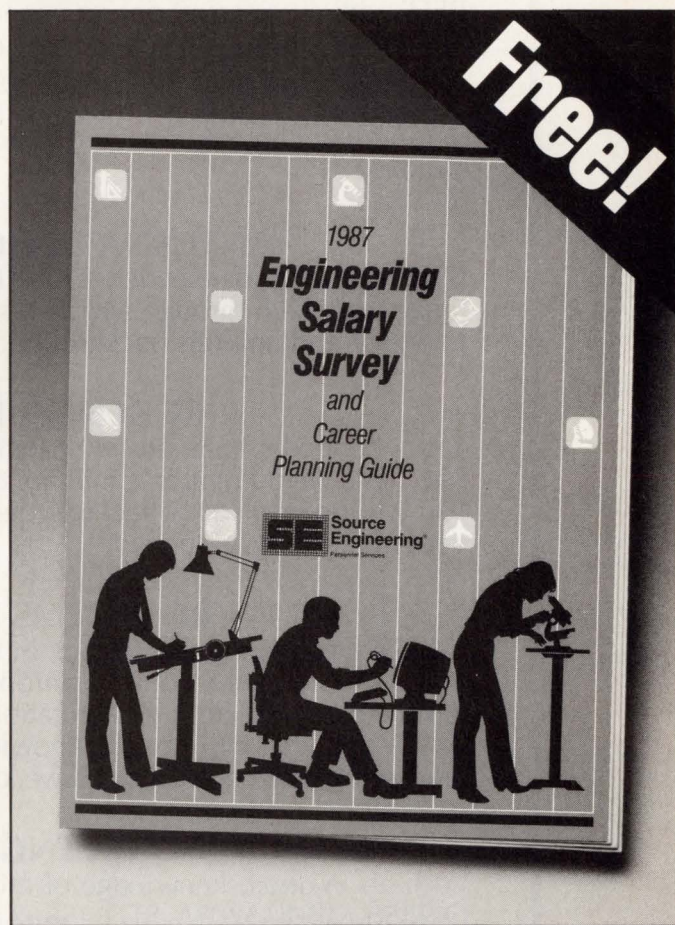
The new **1987 Engineering Salary Survey and Career Planning Guide** is based on information from thousands of engineers and firms that hire them from coast to coast. Salaries for twenty-seven position titles are reviewed including those in design and development, manufacturing, test, quality control, technical support and engineering sales and marketing. You'll learn if your compensation is keeping pace with your peers and what you can expect to earn as you advance in your career.

## Charts, exhibits and graphs to assess your progress

Included in the new Survey are a series of charts, exhibits and graphs to help you get a clearer picture of the profession and how to advance. Proven methods for setting your career objectives, implementing strategies, monitoring your progress and then taking corrective action (when and if needed) are defined. Five documented case studies on professional growth are also provided to point out typical mistakes so that you can avoid them to stay in the mainstream of your career.

## Free to engineering professionals

This valuable 16-page Survey is available without charge. You owe it to yourself to be informed. Call us today.



## Call the office nearest you today

To get your free copy of the **1987 Engineering Salary Survey and Career Planning Guide**, call the Source Engineering office nearest you. We'll mail you a copy in strict confidence and without obligation.

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EDN January 22, 1987

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### New Hampshire

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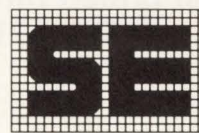
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BSEE with 4+ years of design experience required. Will be involved in the design, development and manufacturing of HF/VHF/UHF microwave receiver and transmitter equipment. Candidates should have design experience with tunable filters, VCO's, synthesizers, demodulator and modulator (PSK, QAM, etc.). IF circuitry and audio circuitry.

## **ANTENNA DESIGN ENGINEER**

BSEE with 2+ years experience in all types of antenna design, frequency range from VLF through MW. Must have both hands-on design experience and analysis background.

## **RF DESIGN ENGINEER**

You will need a BSEE plus 4 years RF design experience, leading to product development in a military defense electronics environment. You will be involved in receiver design, frequency synthesizers and demodulator development.

## **RF SYSTEMS ENGINEER**

A BSEE plus 5 years experience in receiver design and analysis in a military defense electronics environment are required. You will work it the conceptual design, fabrication and testing of receiver systems for EW applications. Working knowledge of system architecture signal processing, intercept, compressive, channelized techniques desirable.

## **QA ENGINEER**

With an in-depth knowledge of military specifications, particularly Q-9858, MIL-1-45208A, STD-45662 and STD-105D along with a working knowledge of manufacturing processes associated with printed circuit board assembly.

## **Xetron Corporation**

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We're state-of-the-art and world class." Ralph Love

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The professionals of Motorola's **Government Electronics Group** (GEG) have much to say about their company because GEG is a place where innovative ideas are put into action. The result is leadership in the research, development and manufacture of electronic hardware for our country's defense, national security and space programs. If you have the imagination and skill required to extend our technical frontiers, consider the opportunities now available.

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Responsible for maintaining, modifying and executing high level language computer simulation models of advanced missile system. Will also conduct parametric studies of factors related to accuracy. Must be able to interface internally with system engineers, subsystem designers and externally with customer representatives. Programming experience related to missile systems, antennas and guidance systems required. Prefer BSEE and 9-11 years experience. Contact Tony Benavidez.

### System Program Managers

Seeking individuals with demonstrated knowledge of production program management in a DoD related electronics environment. The successful candidate's background will include experience in manufacturing, project leadership and familiarity with the government acquisition process. Prefer a technical BS and 10 years related work experience. Contact Tony Benavidez.

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Positions require individuals whose backgrounds include experience with the following technologies: doppler ranging and FM-CW doppler ranging radars, analog and digital radar signal processing, proposal preparation and customer briefings. Requires the ability to provide technical direction to engineers and technicians. Experience with missile fuzing is highly desirable. Prefer BSEE and 7 years related experience. Contact Tony Benavidez.

### C<sup>3</sup>I Systems Engineers

Perform operational analysis, requirements analysis, architectural studies and top-level H/W and S/W designs. Experience in AI, image processing or top-down S/W design preferred. May assist in new business acquisition. Contact Jerry Chadwick.

### QA Test Engineers

Monitor the QA and reliability aspects of production testing and inspection performance. Responsible for failure data collection, analysis of trends and predictions, formal report writing and project coordination of Failure Review Boards. Responsibilities include supervision of technical personnel, project scheduling and budgeting. Previous experience with statistical analysis software is desirable. Prefer BSEE with 7 years experience. Contact Bob Eddy.

### Reliability & Components Engineers

Current experience in maintainability design, analysis modeling and prediction, bit and self-test effectivity/efficiency analysis, system safety/hazard analysis, safety fault free analysis and FMEA. Sneak circuit analysis, plus automated production experience highly desirable. Prefer BSEE with 7 years experience in maintainability and safety engineering. Contact Bob Eddy.

### Senior Engineering Writers

Develop depot-level maintenance manuals on computer-controlled satellite and ground-based digital communications systems. Will write and produce technical manuals on equipment. The writer will perform in an R&D environment. Requires strong analytical and communications skills to develop theory and maintenance procedures to the piece-part level using commercial and unique computerized setup equipment. Prefer an active secret clearance. Contact Bob Eddy.

Join the people of Motorola's **Government Electronics Group**. The benefits are many, including sunny Arizona — a land as beautiful as it is abundant with recreation and culture.

For prompt consideration, forward your resume in confidence to the appropriate technical recruiter at Motorola Government Electronics Group, 8201 E. McDowell Rd., Dept. B755, Scottsdale, AZ 85252; (602) 949-3759. An Equal Opportunity/Affirmative Action Employer. U.S. Citizenship Required.

*The Mind to Imagine*  
**THE SKILL TO DO**



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Advanced electronics for a more productive world.

# Capture the future at SRL

Systems Research Laboratories Inc., is a growing high technology, engineering research and development company. Because of our continued expansion into new areas of technology, we have the following career opportunities available at our Dayton, Ohio, headquarters:

## Software Development Manager

Must have experience with operational flight programs for airborne systems. Requires programming experience in J-73 or Pascal plus ability to analyze software and appropriate documentation. Supervise staff of software engineers during program development phase. BSCS or BSEE and 5-8 years experience with MIL-STD-1750A required.

## Environmental Test Manager

Responsible for setup and management of new environmental test facility for engineering assessment testing, qualification testing and environmental stress screening. Advise design groups, prepare environmental test procedures and plan, schedule

and manage environmental testing for military projects. BSME, 3-5 years environmental testing experience and familiarity with MIL-STD-810 required. Additional requirements include vibration structure design analysis skills, familiarity with environmental design and test specifications and knowledge of computer-controlled environmental test chambers and fixtures.

## Quality Assurance Engineer — Software

Responsible for development, implementation and maintenance of quality assurance plans for electronic graphic display products. BSEE and 3 or more years experience developing and monitoring quality programs in high technology product development environment required. Direct product development, design experience and knowledge of appropriate MIL-SPECS preferred.

## Senior Digital Systems Engineer — Avionics

Responsible for digital hardware development and systems integration for military avionics, EW and display systems. BSEE and 5-10 years experience in digital hardware development required.

## Programmer/Analyst

Design and develop real-time software for scientific applications in human/machine integration. Requires BSCS with 2 or more years experience in FORTRAN, BASIC and C, using UNIX-based systems on variety of computers such as VAX/VMS, PDP-11 systems, 1750A/1533 bus system.

## Systems Analyst

Design, plan and develop real-time software from top-down systems description for advanced generic crew station simulator. Lead software team. Requires BSCS with 5-8 years experience in a VAX/VMS environment and working knowledge of UNIX, C, FORTRAN, Ethernet and computer graphics software. Experience with aircraft dynamics and flight simulation desired.

SRL offers an excellent compensation and benefits package and a working atmosphere that encourages personal career growth. Qualified candidates should send their resume in confidence to Dept. 12, Systems Research Laboratories, Inc.

EOE/MFHV  
Principals only



U.S. Citizenship required

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## EDN CAREER OPPORTUNITIES

# EDN



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We have long been involved with the entire space program. Missiles. Satellites. Space Shuttle. You name it. Depending on orientation, you'll be seeing, and contributing to, the last word in radar, optical instrumentation, telemetry, communications, data handling, C<sup>2</sup>, statistical data reduction, meteorology, timing/firing, frequency control, shipboard instrumentation . . . and related technologies.

## The third range is choice

Following is a diverse array of engineering opportunities. Each requires an appropriate degree and at least 5 years relevant experience.

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Will accomplish design, acquisition, installation and evaluation of antennas, preamplifiers, mixers, down-converters, filters, demodulators, demultiplexers and computer interfaces for large aperture S-band telemetry antenna systems. Must perform hardware design and system analysis.

### DATA SYSTEMS ENGINEER

Will accomplish design, acquisition, installation and evaluation of data acquisition, transmission, processing and display systems for distributed instrumentation complexes. Must have substantial experience in system/subsystem design, test and evaluation.

### RADAR SYSTEMS ENGINEER

Will perform design, acquisition, installation and evaluation of high power transmitters, solid-state receivers, and digital range machines, and preparation of specifications for new land and shipboard radar used in tracking and signature



data collection. Must be experienced in system/subsystem design, test and evaluation.

### OPTICAL SYSTEMS ENGINEER

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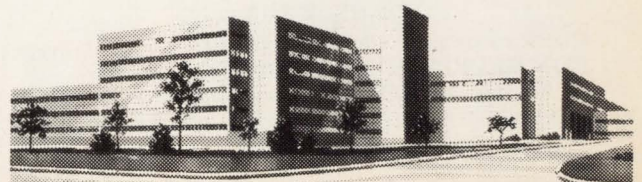
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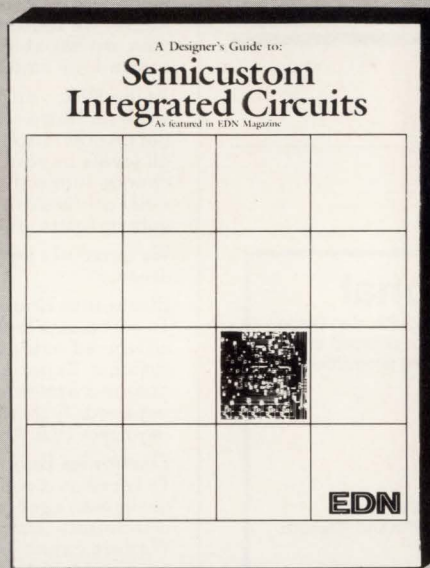
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# LOOKING AHEAD

EDITED BY GEORGE STUBBS

## TIMETABLE FOR PROGRESS IN OPTICAL-COMPUTING RESEARCH

1986	PROTOTYPE OF GENERAL-PURPOSE OPTICAL COMPUTER
1987	PROTOTYPE OF OPTICAL SUPERCOMPUTER, WITH SPECIFICATIONS EXCEEDING THOSE OF ELECTRONIC SUPERCOMPUTERS
1988	INEXPENSIVE OPTICAL MEMORY; CASCADED, PROGRAMMABLE, OPTICALLY ADDRESSED DIGITAL OPTICAL LOGIC ARRAYS
1989	FAST, HIGH-RESOLUTION, COMMERCIAL-QUALITY SPATIAL LIGHT MODULATOR
1990	INTEGRATION OF BISTABLE DEVICES ON CHIP; OPTICAL ASSOCIATIVE MEMORY; COMMERCIAL OPTICAL ARRAY PROCESOR AND HYBRID ELECTRICAL/OPTICAL COMPUTER
1991	PRACTICAL OPTICAL INTERCONNECTS FOR SILICON CHIPS
1995	THE FIRST FULLY OPTICAL COMPUTER; COMMERCIAL OPTICAL BISTABLE DEVICES; COMMERCIAL OPTICAL ASSOCIATIVE MEMORIES

(SOURCE: SEAI TECHNICAL PUBLICATIONS)

### Market for optical computers to be worth \$1B by 2000

Even as university and corporate researchers plumb the limits of parallel processing and supercomputing, others are exploring the next step beyond—optical computers. According to SEAI Technical Publications, a Madison, GA-based publisher of technical reports, computers that process information encoded in the form of light beams will make steady advances over the next 10 to 15 years, surpass the current perceivable limits of electronic computing, and constitute a \$1 billion market by the year 2000.

There are several types of optical computers, reports SEAI. Digital optical computers use nonlinear or bistable optical materials in a manner similar to the use of the transistor in an electronic computer. The analog optical computer applies the ability of a lens to perform a Fourier transform, and of a convolution to perform advanced mathematical operations, such as matrix-to-matrix multiplication in linear algebra. Some designs use systolic arrays to allow analog processing of digital data. Optical pattern-recognition systems also employ the inherent ability of optical systems to perform transforms.

The advantages of optical computing go beyond the familiar virtue

of great speed that lightwave technology affords. Optical lenses can perform mathematical calculations that are very difficult to perform using digital circuitry. Also, optical holography will be able to achieve high-density, 3-D information storage. Finally, says SEAI, optical technology confers space advantages and eliminates the clock skew of circuit-wire interconnections.

SEAI believes that, within a few years, an electronic computer with an optical array processor will equal today's supercomputers in speed for selected operations, while offering vast improvements in cost, size, weight, power consumption, and reliability. It is almost certain, says SEAI, that algebraic optical computers will be successful technically and commercially, and that they will be a driving force in the much-needed improvements of optoelectronic components and devices.

A number of companies and organizations are pursuing research into optical computers. The Optical Circuit Cooperative at the University of Arizona has a number of companies as members. A major research program is underway at Bell Laboratories, and the Defense Advanced Research Projects Agency (Darpa) has made a major commitment to the development of optical computers, optical interconnects in VLSI, and

high-performance spatial light modulators. Companies like Texas Instruments, Harris Corp, Hughes, Honeywell, Westinghouse, Grumman, and General Dynamics are reported to have begun significant research into optical computing.

### AI reaches factory floor: Market to top \$1.7B by '90

If computers were smart, they'd get into management. So say analysts at the market-research company Frost & Sullivan Inc (New York, NY), who note that computers are doing just that—finding their way to the factory floor and helping to make complex, management-like decisions. These artificial-intelligence (AI) systems, say F&S researchers, will form a \$1.7 billion commercial market in 1990, of which \$700 million will be devoted to software and hardware used in factories.

F&S estimates the dollar value of in-place factory AI systems at \$145 million for 1986. Such systems include Westinghouse's ISIS-II, a work-order system that produces prioritized schedules, computes permissible worker overtime, and performs other functions. Another AI system, Digital Equipment Corp's ZCON, generates plans for combining the components for customized superminicomputers; the system reportedly can make substitutions or additions of components while ensuring the lowest possible cost to the customer.

For the \$425 million 1986 market for AI goods to make its predicted fourfold increase by 1990, F&S admits, some technological advances must occur. In 1990, factory purchases of AI systems and equipment will be greatest for unbundled software, symbolic computers, engineering workstations, and expert-system development tools and applications.

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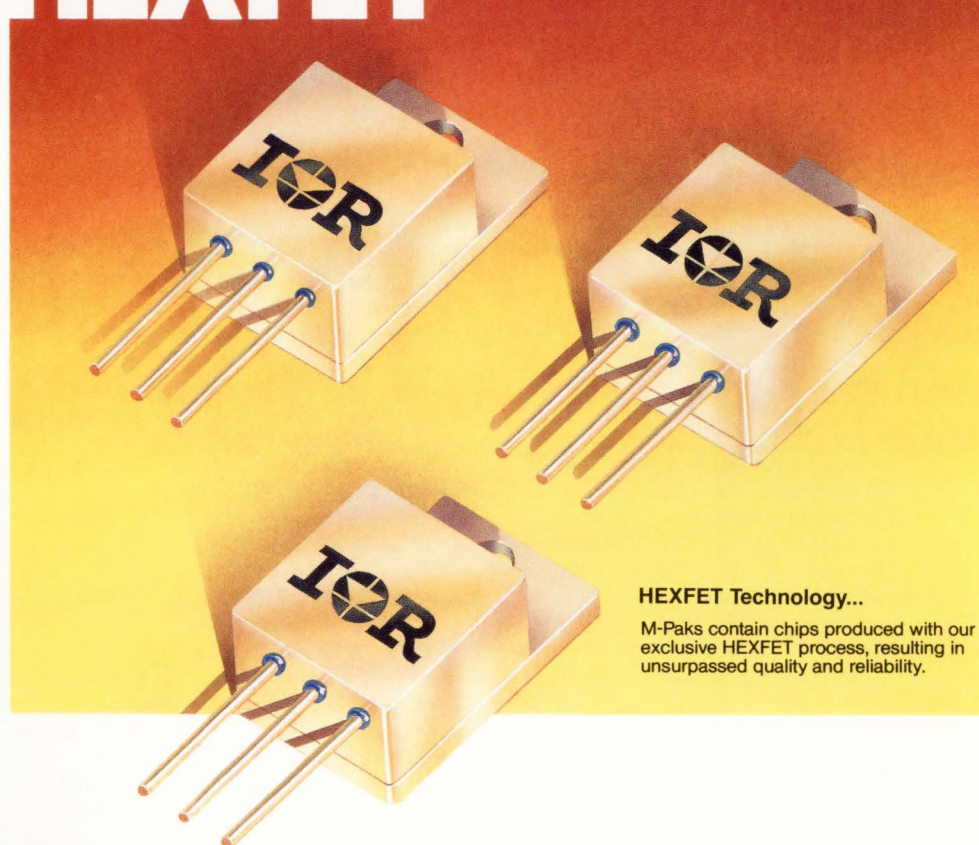
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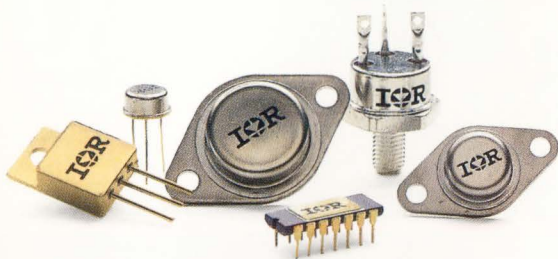
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