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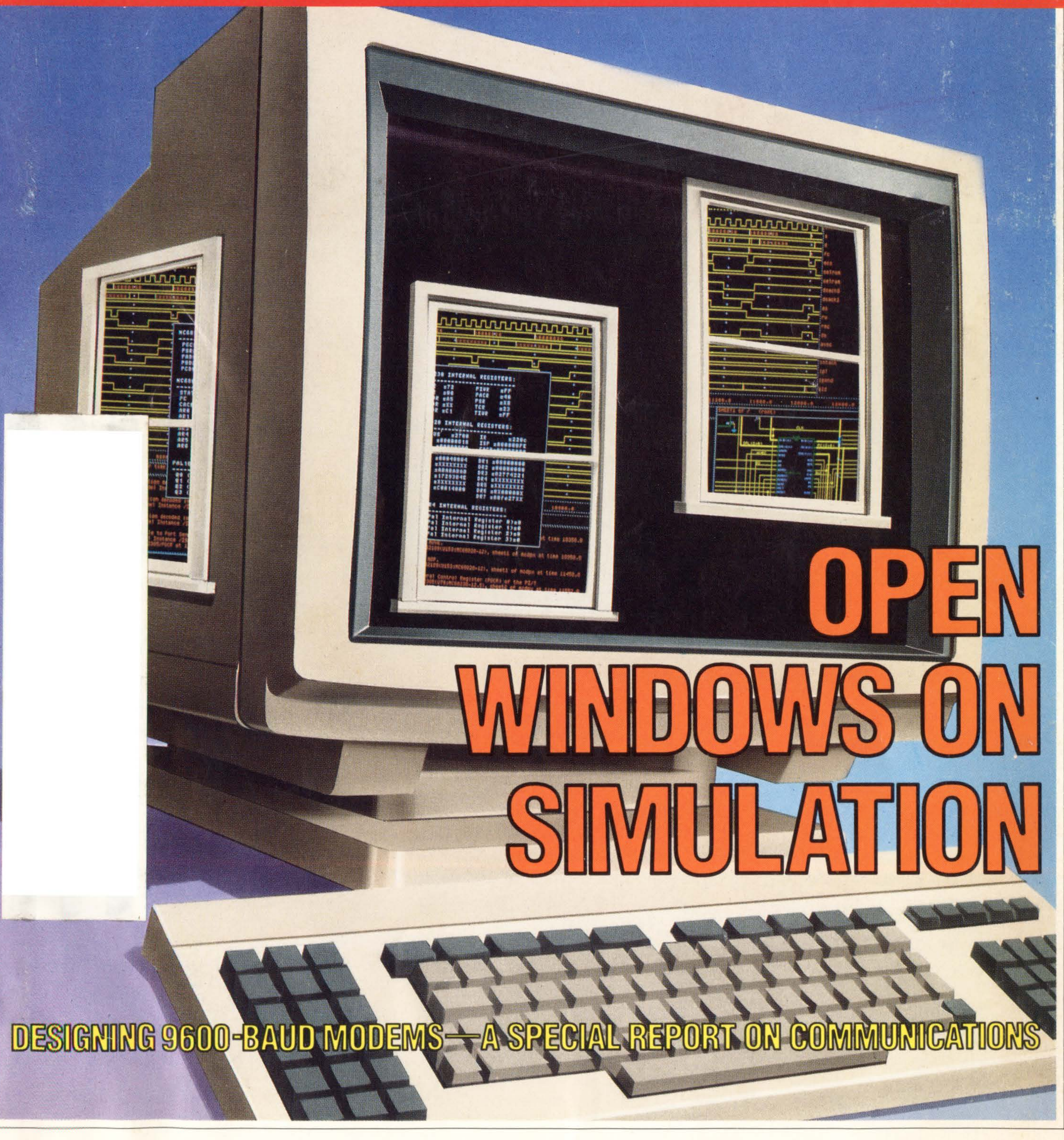

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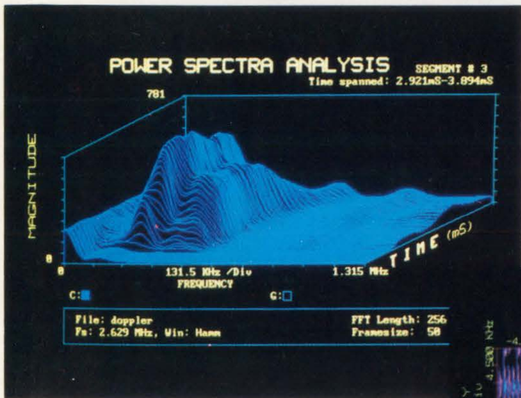

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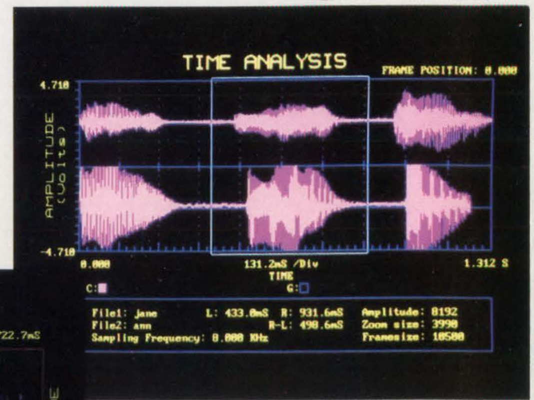

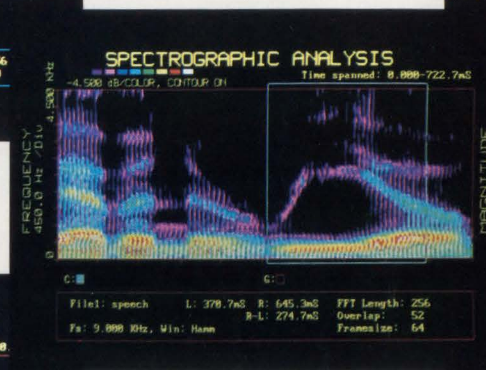

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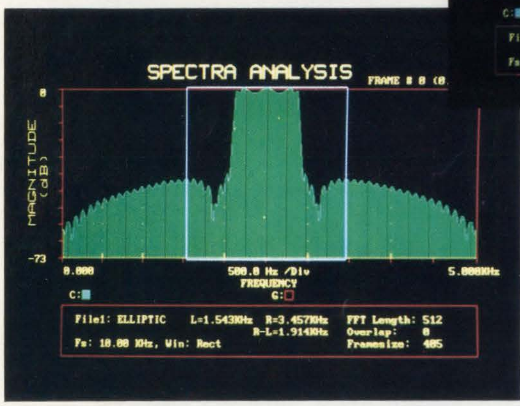

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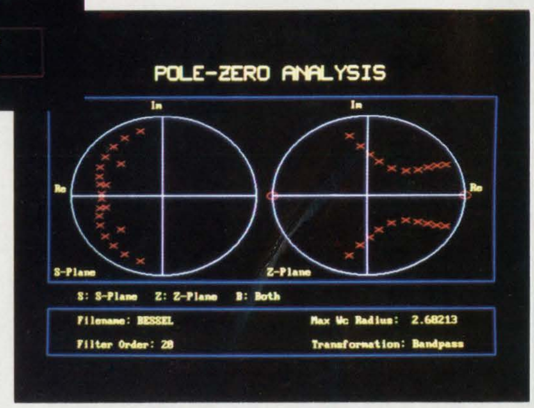

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CIRCLE 131

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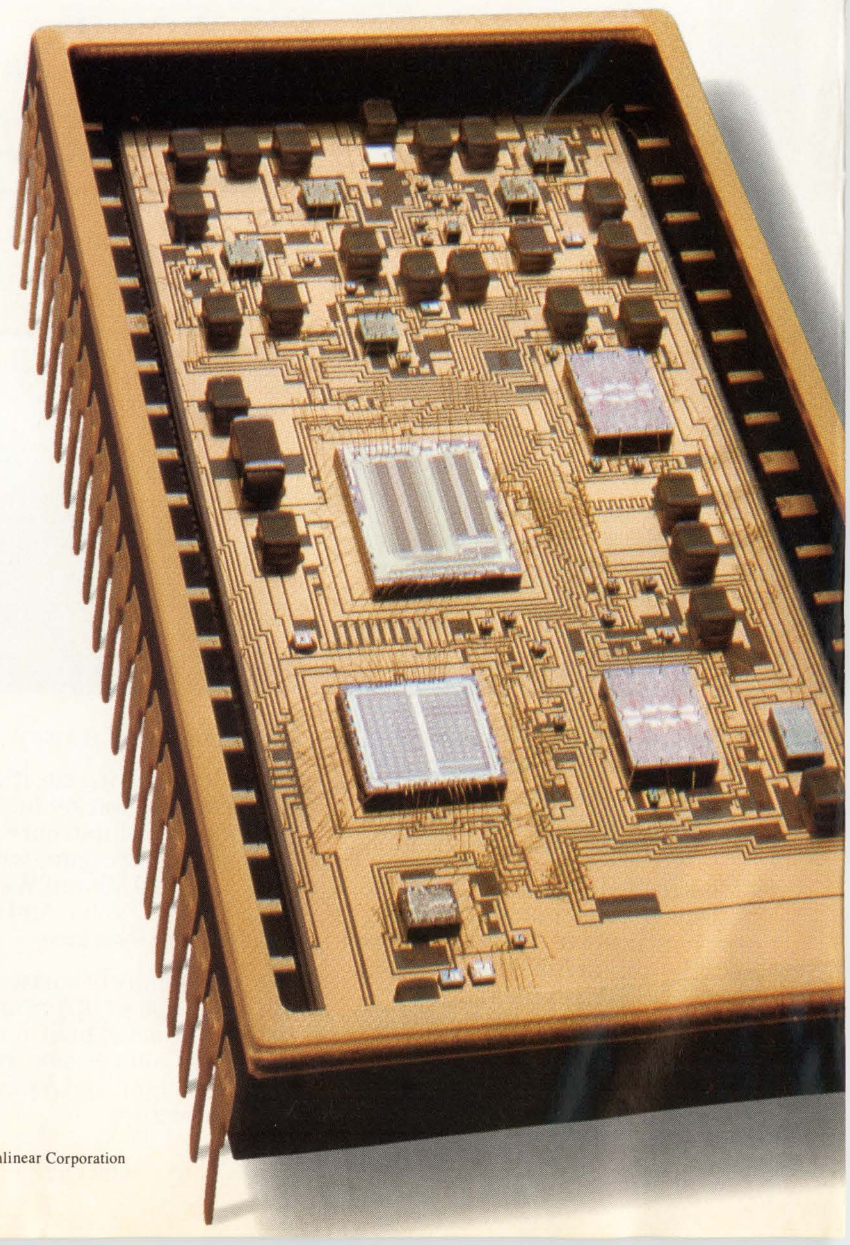

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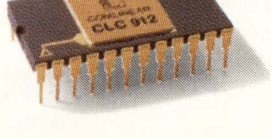

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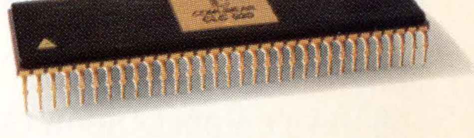

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CLC925

CIRCLE 3

MARCH 9, 1989 VOL. 37, NO. 5

ELECTRONIC DESIGN

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AMERICAN EXPRESS

CIRCLE 6

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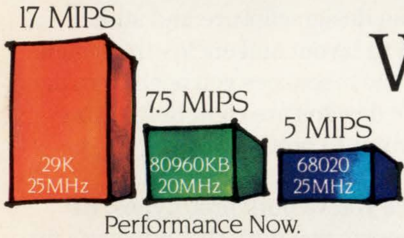

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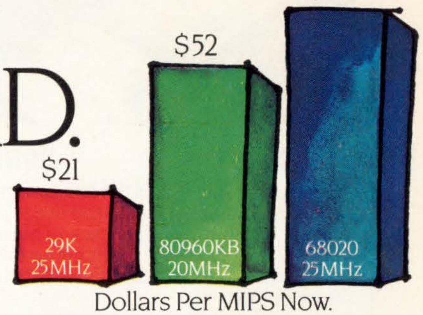

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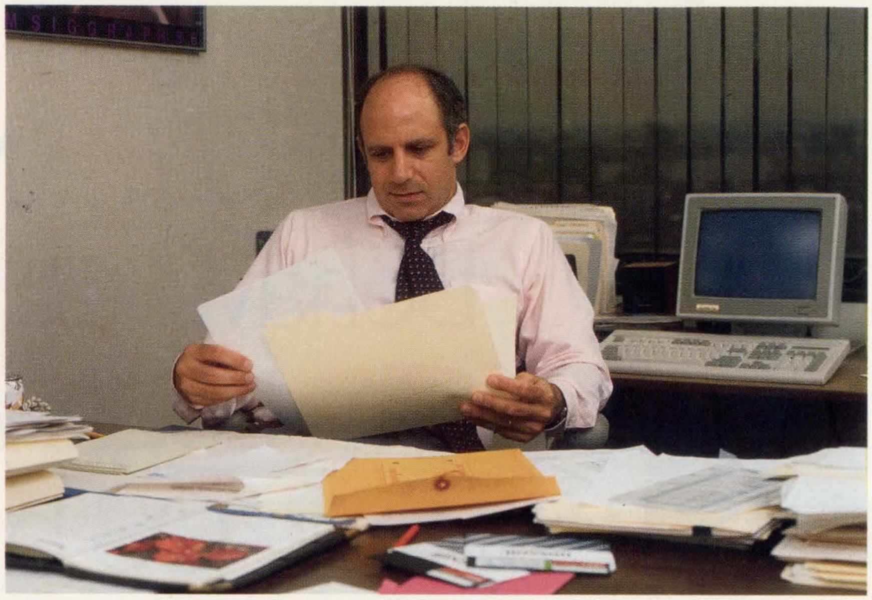
EDITORIAL



MOMENT OF TRUTH

THIS IS WHAT YOU WANTED TO BE AN ENGINEER FOR, announced the billboard on 101 North in Santa Clara. In the sign's lower right-hand corner was a silver-capped pin-grid array marked 29K.

Was this why I wanted to become an engineer? I remember winning a prize in a high-school science fair for modifying and building a cardiac-monitor circuit I found in *Popular Electronics*. Winning the prize wasn't nearly as exciting as that moment when, in my attic workshop in the middle of the night, I inserted the batteries in the amplifier, taped the electrodes to my forearms, and watched the meter needle slam over with each beat of my heart. "It works!" I screamed, waking up everyone in the house.

Like most engineers, the job I do now is quite different from the work I thought I would be doing when I first considered becoming an engineer. These days, I worry about the RISC vs. CISC competition, about the Japanese domination of the memory business, about the prospects for ASIC suppliers with their unmentionable NRE costs. I'm hounded by deadlines, budgets, and other mundane problems. All this is a far cry from the pure excitement I felt as a teenager, borrowing circuits from magazines and seeing if I could get them to work.

Just the other day, I escaped from a taxing business meeting, emotionally drained and exhausted. I beat a path to my office and sank into my chair. On my desk was a letter from an old friend, Walt Jung, who does applications work for Linear Technology Corp. He included an audio preamp circuit and a fistful of parts. "You probably don't have time for this stuff anymore," he apologized, "but if you try this circuit . . . it'll knock your socks off."

As frustrating as it may sometimes seem, our work does have its moments.

Steve Ohr

Stephan Ohr
Editor-in-Chief

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HIGH PASS Model *HP-		50	100	150	200	250	300	400	500	600	700	800	900	1000
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	end, min.	200	400	600	800	1200	1200	1600	1600	1600	1800	2000	2100	2200
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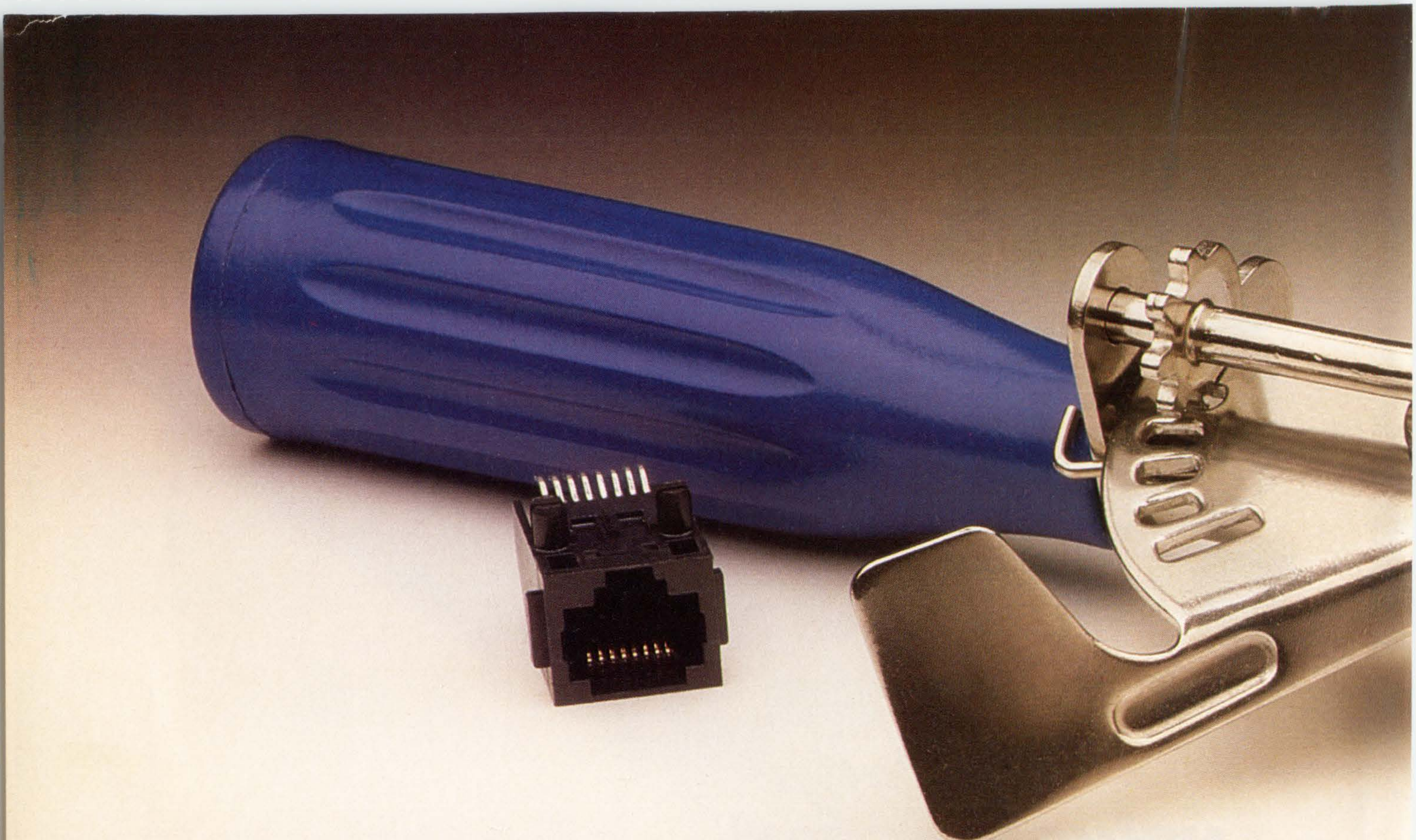
*Prefix P for pins, B for BNC, N for Type N, S for SMA   *example:* **PLP-10.7**

CIRCLE 10

C105 REV. E



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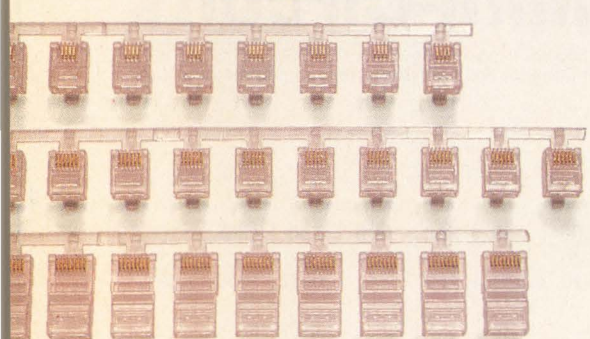

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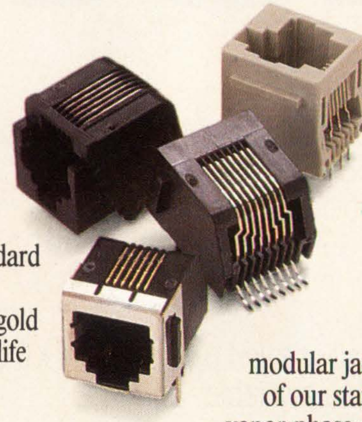

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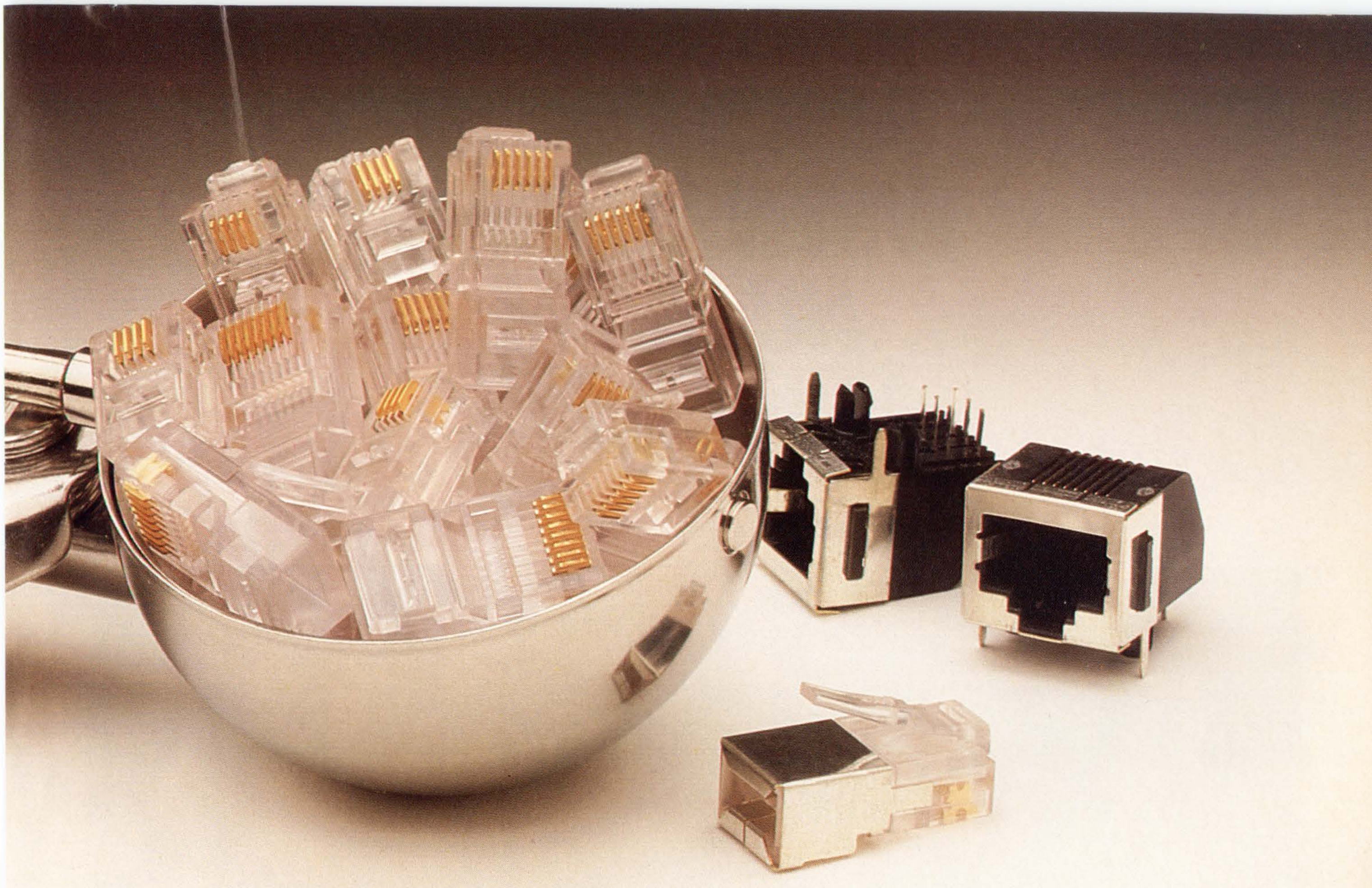

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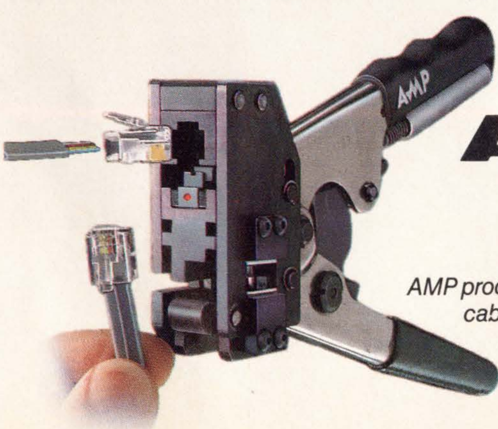
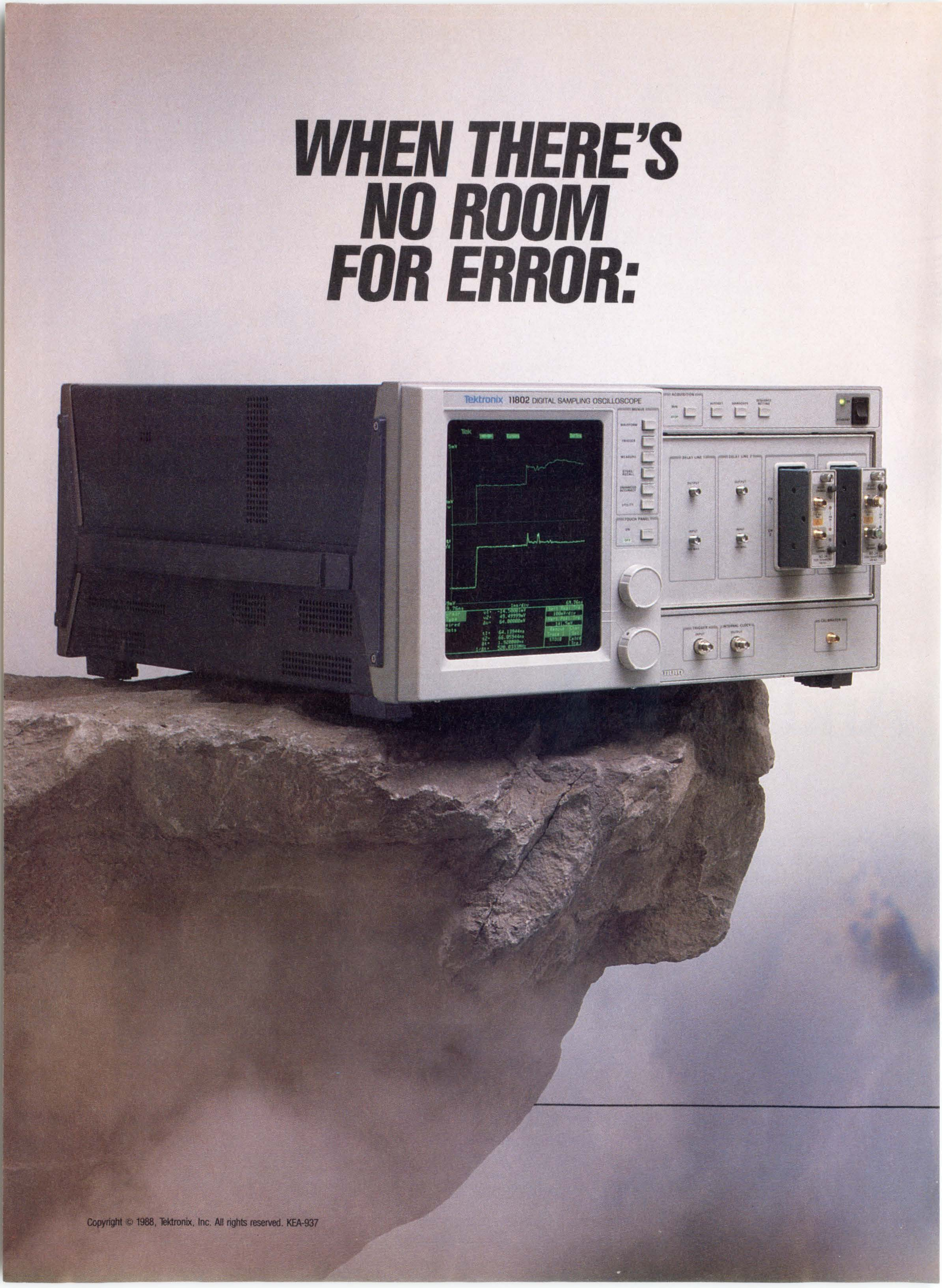


AMP production hand tool cuts cable, strips cable jacket, and mass terminates loose-piece plugs.

AMP Interconnecting ideas

CIRCLE 28


WHEN THERE'S NO ROOM FOR ERROR:
Tektronix 11802 DIGITAL SAMPLING OSCILLOSCOPE

EISA VS. MCA: A SPLIT DECISION

LISA GUNN

Which will be the next industry standard, the Micro Channel Architecture (MCA) or the Extended Industry Standard Architecture (EISA) bus? Because the two 32-bit buses are so similar, this is a difficult question without a clear-cut answer. If it's customer support that makes an architecture succeed, then the Micro Channel, with 1.5 million already sold, is far ahead of EISA. If, however, it's vendor support that is key, it looks as if this fight might end up in a split decision.

The EISA bus specifications were finalized around the end of January. Intel is seeing a lot of interest in the EISA chip set it will be shipping second quarter. The Gang of Nine all stated their intentions to do EISA systems, and over 100 other system and board companies have publicly said they would be doing EISA products. The first rollout of products is expected by the end of the year. On the other hand, there are currently over 700 cards available for the Micro Channel from third-party manufacturers, and over 1800 ID numbers are assigned for companies who intend to develop them.

With so much support on both sides, the industry might end up with two standard buses. After all, the PC industry has been big enough to support both the IBM and Apple standards. Why not one more variation? Some companies are pledging support to both sides. Tandy and Olivetti, for instance, are among the nine PC companies working on the EISA project while also manufacturing PS/2-clone machines. Ed Juge, director of market planning for Tandy, believes that both buses have a strong hold on the market already. "Both buses are good, and both have a place in today's PC market. Many people are saying that the EISA bus is too late. Everbody seems to forget that it is just an extension of the PC AT bus. Therefore anyone using a PC AT computer today is using the EISA bus."

Intel, as it turns out, produces silicon for both the MCA and EISA. Rajiv Sachdeva, Micro Channel product line manager for Intel, thinks that the two bus structures "can definitely coexist. We certainly see the market being big enough for two bus structures."

Is the industry big enough to support two buses? Scott Brooks, a spokesman for IBM, states, "The customers will decide that, but I don't think that the industry needs a second 32-bit bus. One of them has been out there for almost two years now, with well over a million and a half shipped. I think that there already is a standard." If the industry needs only one standard, why all the support for the emerging EISA bus? "It doesn't really cost anything to support EISA at this time, because they don't have a product. If you went out today and bought a 386-based machine from another manufacturer, and at some point you decide you need an extended 32-bit bus, you have to go out and buy a new computer. There's only one company making 32-bit buses now, and that's IBM."

If the PC industry does end up with both architectures, what factors will make consumers pick one bus architecture over the other? After all, the EISA bus looks pretty attractive, but many customers have a strong desire to stick with IBM. They might have a lot invested in an IBM mainframe and need the consistency that IBM offers. "From an end-user standpoint, the two buses are very similar. Boards are available for both, and software is compatible with both. So a big part of the decision is who you want to buy the computer from. People who need complete IBM compatibility will buy the Micro Channel," says Brian Ekiss, EISA product line manager for Intel. "The other part of the decision is whether PC AT-bus compatibility is important to you. With the strength of the companies that are behind each bus structure, they both have an excellent chance of success."

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CIRCLE 19

IMAGE-PROCESSING ICS RIP THROUGH DATA

With 30-MHz throughput, a pair of digital circuits aimed at image-processing applications ease the filtering and mixing aspects of image manipulation. Developed by TRW LSI Products Inc., of La Jolla, Calif., the 1-μm CMOS circuits contain multiple arithmetic blocks and data paths that accelerate processing. One of the chips, the TMC2249, packs a pair of 12-by-12-bit multipliers, an adder, and a cascadable accumulator to perform tasks such as simple image mixing and switching. It can also implement finite-impulse-response filters, digital quadrature mixers, modulators, and vector arithmetic functions. The chip offers a unique feature: For each of its 12-bit multiplier inputs, users can program a pipeline delay of up to 16 clocks. By using the delay registers as pipelined storage banks in digital filtering applications, the chip holds up to 32 coefficient and data-word pairs, split into even and odd halves. As a result, it calculates two taps of a filter every clock cycle. The other new chip, the TMC2246 image-filter convolutional array, readily performs pixel interpolation in image manipulation and filtering applications. It boasts four on-chip 11-by-10-bit registered multipliers, plus a summer and an accumulator. Off-chip data buses can directly feed the chip all eight of its multiplier inputs. The accumulator delivers a 16-bit sum output. DB

AN X-RAY SYSTEM FOR MAKING SEMICONDUCTORS

A new means of generating, detecting, and processing X rays could lead to better and less expensive X-ray microlithography systems. Researchers at Quantum Diagnostics Ltd., of Hauppauge, N.Y., are working on a stimulated X-ray emitter (SXE) that creates tightly collimated, nearly monochromatic beams to supply the high-resolution, high-intensity rays needed for microlithography. Conventional microlithography uses synchrotrons to obtain X rays of the needed intensity, but synchrotrons are expensive—in the $10 million range—and can expose only small portions of the semiconductor wafer at a time. With the SXE, large portions of the wafer can be exposed to X rays at least as intense as those generated with synchrotrons. Quantum Diagnostics is also developing an optically based image detector and an optical image-processing computer to handle real-time image processing of X rays. The entire system—SXE, detector, and image processor—is intended for medical diagnostic systems, but may serve in other areas as well. JT

ADA DEVELOPMENT TOOLS FOR SPARC PROCESSORS

Designers of real-time embedded controllers can now develop Ada software for Sparc-based systems. Four companies—Mizar Inc., of Carrollton, Texas, Sun Microsystems, of Mountain View, Calif., Verdix Corp., of Chantilly, Va., and Wind River Systems, of Emeryville, Calif.—have pooled their resources to create VADSWorks, an Ada development package that includes compilers, debuggers, and a real-time operating system. Programmers can write code under the SunOS Unix system on either a Sun workstation or a Mizar Hybrid Ada Development System. Code is downloaded to target systems, where the Ada programs run under the VxWorks real-time operating system. The growing availability of Ada development tools for RISC processors signals a turning point in embedded-system design. Although most embedded controllers are 8- or 16-bit complex-instruction-set computer (CISC) chips and most control code is written in C, both Ada and RISC processors are beginning to carve inroads into the embedded-controller arena. JT

LASER CUTS INTO TAB BONDING TIMES

Designers can now attach ICs to TAB tapes with a new laser-bonding system that performs 5 to 50 times faster than conventional systems. A product of Microelectronics and Computer Technology Corp.'s packaging and interconnection research program, the system incorporates an yttrium-aluminum-garnet (YAG) laser to quickly and precisely bond the leads from TAB tape to chip without damaging the chip, even if the chip's bonding pads are located over active circuitry. The bonder is a flexible, low-cost, nondamaging bonding technology, which can be applied in a production environment. The Austin, Texas, company has licensed Electro Scientific Industries (ESI), of Portland, Ore., to manufacture the system, at first for MCC and its shareholders, then for general use. JL

NATIONAL'S 32532 POWERS NEW ENCORE COMPUTERS

One of the first applications of National Semiconductor Corp.'s 30-MHz, 32-bit NS32532 microprocessor comes from Encore Computer Corp., of Marlborough, Mass., in its new family of Unix-based, parallel-processing superminicomputers. The Multimax 500 family accommodates up to 10 processor boards in its most powerful version, which executes 170 million instructions per second. That's more than four times as fast as Encore's earlier Multimax 300 family, which uses the 15-MHz NS32332 microprocessor to execute 40 MIPS in a 10-board configuration. Two NS32532 processors on each

Multimax 500 board execute 8.5 MIPS. That translates into 17 MIPS for a one-board, entry-level Multimax 510, which sells for $159,000. A similarly priced Digital Equipment Corp. VAX 6300 system delivers about 5 MIPS. Encore expects the 500 family to find use in both technical and commercial computing applications, ranging from software development and simulation to database management and on-line transaction processing. LC

DATA GENERAL BUILDS ON MOTOROLA'S RISC

The first evidence of Data General Corp.'s commitment to RISC technology surfaced in late February when the Westboro, Mass., computer maker unveiled four workstations and a server built around the Motorola 88000 CMOS RISC microprocessor and DG/UX, Data General's symmetric multiprocessing version of Unix. The move marks the company's first venture outside its proprietary MV/Eclipse computers, most of which run DG's AOS operating system. The lowest-priced workstation, a diskless model with 4 Mbytes of memory and a 20-in. monochrome display, comes in at well under $10,000 and performs 17 MIPS with a 16.7-MHz version of the 88000. That compares with 14 MIPS at $11,900 for Digital Equipment Corp.'s recently announced entry-level RISC workstation, the DECstation 3100, built around a MIPS Computer System's R2000 RISC CPU. Two other Data General models incorporate a 20-MHz 88000 that executes 20 MIPS. LC

A VAST, INEXPENSIVE TECHNICAL LIBRARY

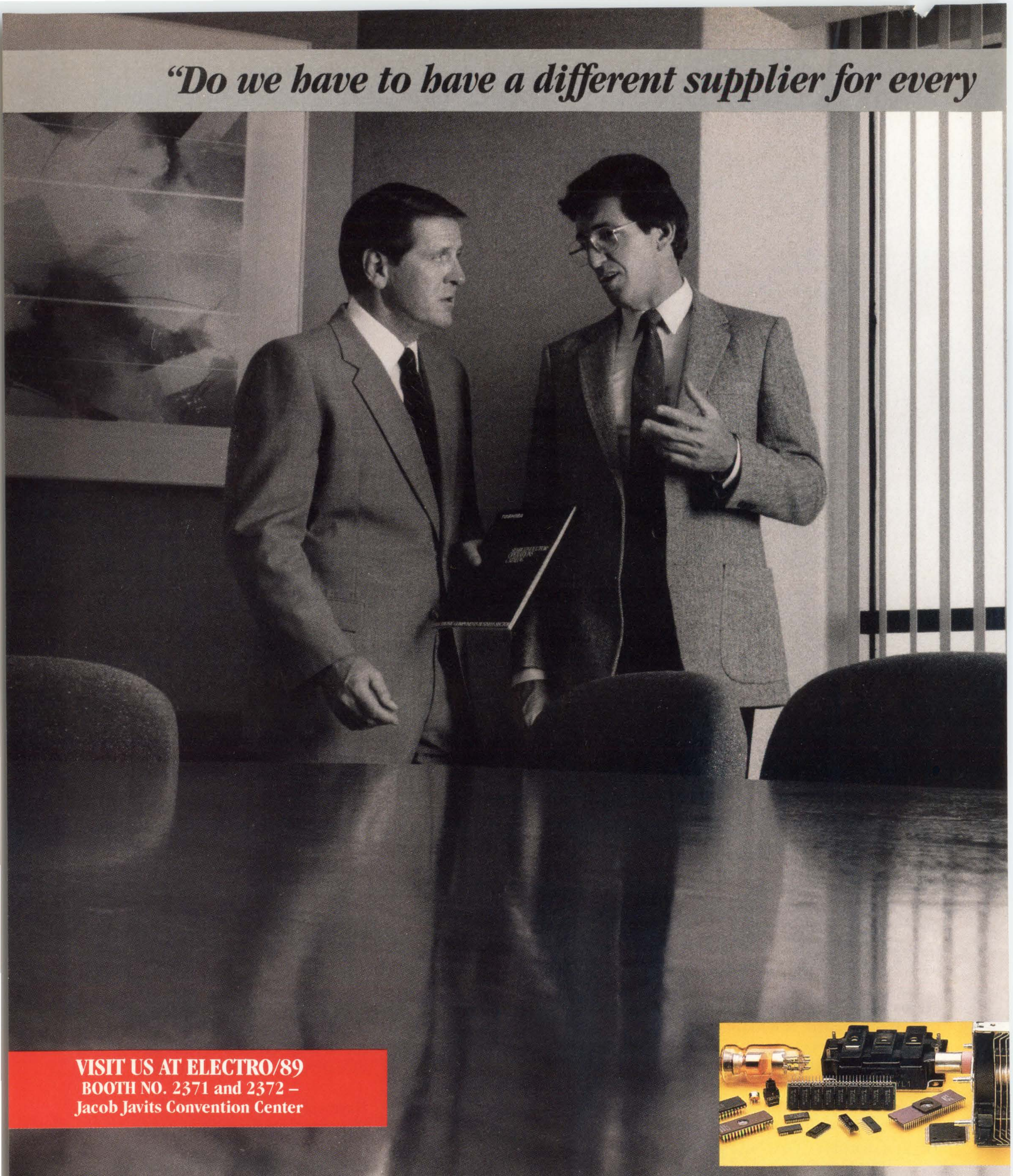
Just as movable type spread printed material to the general population, two new classes of membership will give the design community access to a large technical library on the West Coast. Until now, the library and database offered by Lucid Information Services Inc., of Santa Clara, Calif., was open to corporate sponsors, which each paid a minimum of $35,000 per year. For that tidy sum, they could access more than 480 technical publications and journals and various database search-and-information services. But now individual subscribers can access the library for a nominal minimum service fee—just $250 per quarter, plus copywrite payments for any literature copied. The individual membership lets you drop in and review periodicals, conference proceedings, reference books, and databases and request copies of desired documents. A second individual membership class, a subscriber account, has a minimum service fee of $600 per quarter. Subscribers get individual-account privileges, plus regular delivery of the tables of contents of up to 10 journals to expedite their literature searches. Members can ask for literature in person, by telephone, facsimile, or letter. Requests are usually filled within 24 hours. DB

LANGUAGE PROCESSOR SPEEDS CODE EXECUTION

Software written in Forth, Fortran, C, and other languages can now run faster, thanks to a custom language-processor CPU architecture developed by the Applied Physics Laboratory of Johns Hopkins University. The architecture has been implemented as a 32-bit custom processor chip, the SC32, by Silicon Composers Inc., of Palo Alto, Calif. That chip, in turn, powers a single-board computer produced by SCI. The SC32, which will be offered commercially, promises to accelerate real-time control tasks by virtue of its 10-MIPS throughput when running at 10 MHz. At that speed, the chip can execute the popular sieve-of-Eratosthenes and Fibonacci benchmarks in 2.3 and 7.0 s, respectively. In comparison, an 80386/387 combination running at 20 MHz takes 23.18 and 42.48 s to do the same calculations. Unlike conventional processors, which are optimized for straight-line code execution, the SC32 processor was optimized to handle subroutine calls and returns—one-cycle calls and zero-cycle subroutine returns are possible. The SC/FOX32, a development board that plugs into an IBM PC XT, AT, or compatibles, contains the SC32 processor and the SC/Forth32 software development environment for writing Forth programs. DB

FAULT GRADER SPEEDS TEST-VECTOR CREATION

Designers can quickly develop and measure the effectiveness of circuit test vectors with a forthcoming statistical fault-grading tool from Mentor Graphics Corp., of Beaverton, Ore. Because QuickGrade is integrated with Mentor's Idea Series design tools, fault flags can be directly displayed on a circuit schematic, graphically pinpointing the location of untested or untestable circuitry. QuickGrade users can also display signal waveforms and a list of circuit activity. In this way, they can quickly relate the fault coverage back to the circuit and stimuli that created the faults. The $11,900 package analyzes circuits created with any combination of Mentor's modeling approaches. Designers thus can model in the most efficient form—behavioral, switch-level, gate-level, levelized compiled code, hardware models, and third-party behavioral models. DB



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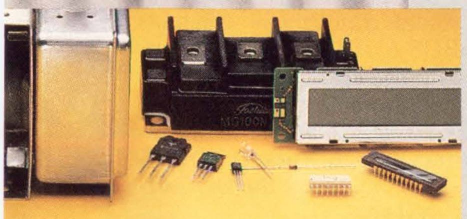

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CIRCLE 15

NEWS

DDC

MARCH 1989

ILC DATA DEVICE CORPORATION

ABOUT SYNCHRO-CONVERSION • A/D & D/A CONVERSION • 1553 BUS DEVICES • POWER & CUSTOM HYBRIDS

NOW AVAILABLE . . . 1553 AIM HY
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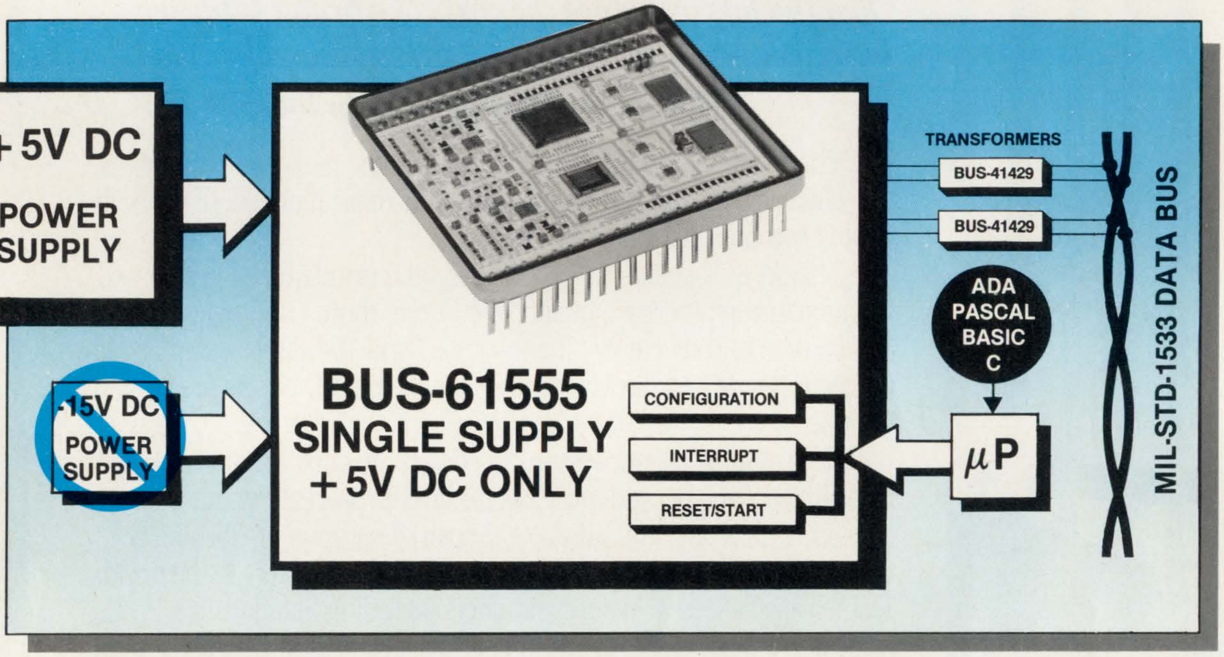

DDC's BUS-61553, THE SMALLEST, MOST INTEGRATED MIL-STD-1553 BC/RT/MT INTERFACE IS NOW AVAILABLE AS A +5V DC ONLY UNIT DESIGNATED BUS-61555. The BUS-61555 is pin compatible with the popular BUS-61553 (which requires -15V DC and +5V DC) except that the bus transformers required for the BUS-61555 are different (require BUS-41429 transformers.)

Using the BUS-61555 in a system might allow for the complete elimination of a power supply since no -15V DC is required for the 1553 function.

This Advanced Integrated MUX (AIM) HYbrid replaced earlier board level solutions with a single 2.1" x 1.9" hybrid package. Dubbed the "AIM HY", the BUS-61555 contains a low power +5V only Dual Transceiver, complete Bus Controller (BC), Remote Terminal (RT), and Bus Monitor Terminal (MT) protocol, a powerful Memory Management/Host Interface IC and 8 x 16 bits of low power CMOS static RAM. This internal memory can be expanded to 64K x 16 bits by adding up to 56K x 16 bits of Static RAM external to the hybrid by properly using the control signals available from the hybrid. The internal RAM need not be utilized at all.

By incorporating proven DDC components, the AIM HYbrid represents a risk-free, flexible MIL-STD-1553 *solution* with a host of support tools already available. The BUS-61555 is ideal for applications requiring a powerful, inexpensive, low power component that minimizes precious PC-board real estate usage while providing maximum flexibility and inherent reliability.

Other model numbers in the "AIM-HY" Family:

BUS-61553—15V Unit in a Plug-in-Package.

BUS-61554—12V Unit in a Plug-in-Package.

BUS-65163—15V Unit in a Flat-Pack (for Surface Mount Applications.)

BUS-61564—12V Unit in a Flat-Pack.

BUS-61556—is a unit that does not contain any transceivers which can be used with external sinusoidal transceivers (such as the BUS-63102) for McAIR applications.

For additional information call Mike Glass at 516-563-5545 or toll-free (outside New York State) 800-DDC-1772 or contact the DDC office nearest you. □

CIRCLE 26 FOR SALES CONTACT

DDC

CIRCLE 27 FOR LITERATURE

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RISC Processor Combines Integer, FP, And Graphics

Just released, the iAPX-80860 reduced instruction-set processor packs all the computation-intensive resources to construct a 3D graphics workstation using the fewest chips. The processor also marks a new path for Intel in making chips for general-purpose computing platforms. By integrating over 1 million transistors on a 1-by-1.5-cm CMOS chip, designers at the Santa Clara, Calif., company combined a 32-bit RISC CPU for integer processing, a floating-point unit for 32- or 64-bit numeric calculations, a 3D graphics processor, and 12 kbytes of cache memory—in short, all the key blocks to accelerate future workstations.

The combination of the floating-point and 3D hardware lets the 80860 perform over 500,000 transforms/s, including 4-by-4 3D matrices, clipping tests, and calculations for perspective. Shading hardware can also process images at up to 50,000 triangles/s, where the 100-pixel triangles are Gouraud shaded, transformed, Z-buffered, and include one light source.

The first versions of the chip will run at 33 or 40 MHz, but at last month's International Solid State Circuits Conference, the company showed it could build a 50-MHz version. The integer block and the floating-point section can operate in parallel. Thus, at 33 MHz, the integer processor can deliver a throughput of 33 million instructions per second, while the floating-point multiplier and floating-point accumulator each operate at 33 MFLOPS. Excluding the operations performed by the graphics unit, the total computational power of the chip adds up to 99 million operations per second, a new peak in throughput for a CMOS CPU. And, at 40 MHz, the peak throughput hits 120 MOPS. As a benchmark, the chip runs over 90,000 dhrystones/s when clocked at 40 MHz and can deliver the equivalent throughput of a DEC VAX system running at 33 MIPS—all for $750 apiece in quantities of 1000.

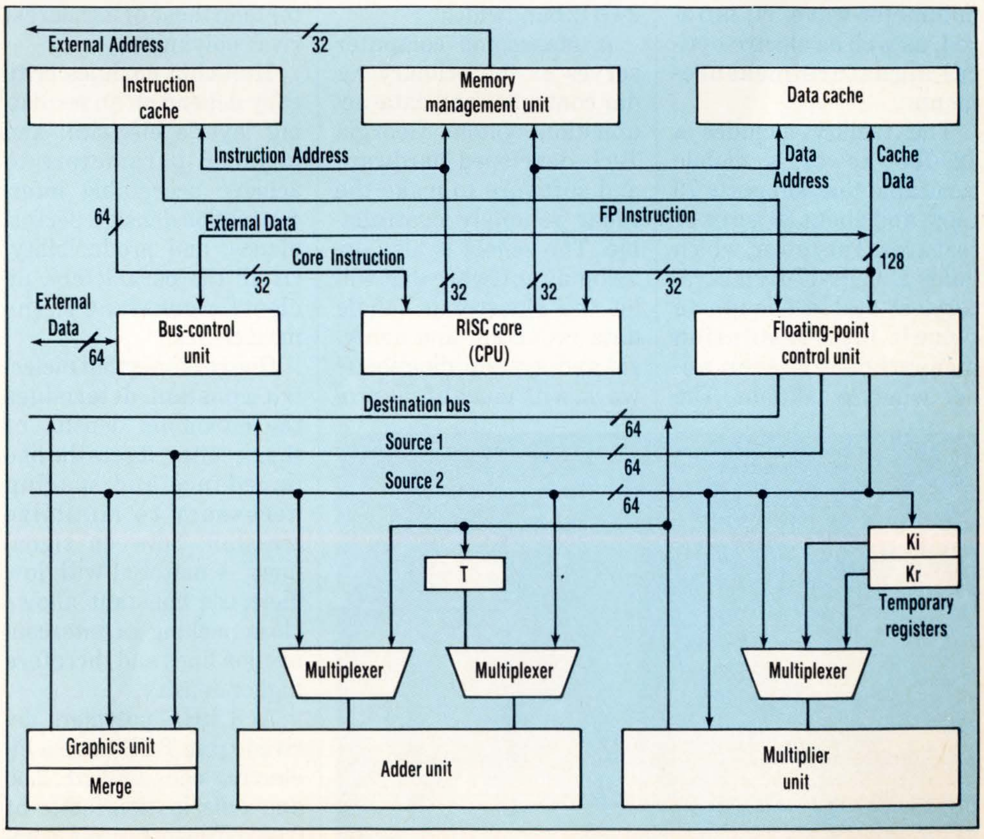
To achieve parallel operation among the chip's sections, more than half of the million transistors serve in cache memories and small register files that feed the integer and math units. The 12 kbytes of cache are divided into two sections: 8 kbytes for the data memory and 4 kbytes for instruction storage. Both cache sections are two-way set associative, and the cache manager employs a 32-byte line to maximize cache reloading efficiency. A 64-entry, four-way associative translation look-aside buffer memory works in tandem with the on-chip memory-management unit.

A 32-word by 32-bit triple-ported register file is used by the integer processor, and a five-ported register file is available to the floating-point math section. That math register file can be software controlled to appear as an 8-word-by-128-bit, a 16-word-by-64-bit, or a 32-word-by-32-bit storage area, depending on the resolution of the math operations.

Beside the integer processor, the CPU block includes a memory-paging unit and a bus controller. Data can be moved quickly on or off the chip, thanks to a 64-bit-wide data bus and a pipelined loading feature that allows various on-chip memories to be loaded from external memory at the full bus bandwidth. On the chip, multiple 128-bit data buses hasten data movement, and a 64-bit instruction bus permits two commands to start every clock cycle.

Supporting the RISC processor are C and Fortran compilers, as well as a Fortran code vectorizer. In development is Unix System V, release 4. Also available are a simulator and an assembler for cross-software development.

DAVE BURSKY



95-GHz Radar Will Teach The Army About Target Resolution

To learn more about resolution in millimeter-wavelength radars, the U.S. Army Missile Command and the Georgia Institute of Technology are installing a 95-GHz research radar at the Redstone Arsenal in Huntsville, Ala.

The system, known as HIPCOR (for high-power, coherent radar), will help the Missile Command answer questions about the resolution needed to differentiate targets, the best waveforms to use, and how target and clutter scattering characteristics differ at millimeter wavelengths. The radar is part of the Target Seekers Measurement Facility, where the Missile Command evaluates seeker technology and makes millimeter-wave, rf, infrared, as well as electro-optical signature measurements.

The facility includes a 329-foot tower, a mobile turntable that supports 70 tons, and about 30 acres of test area. The tower, which holds a 32-by-17-ft. laboratory, is stable enough to permit high-resolution measurements, even under windy conditions. The turntable will rotate a target and move it into different types of backgrounds so that scattering comparisons can be made. An elevator in the tower permits measurements at different angles.

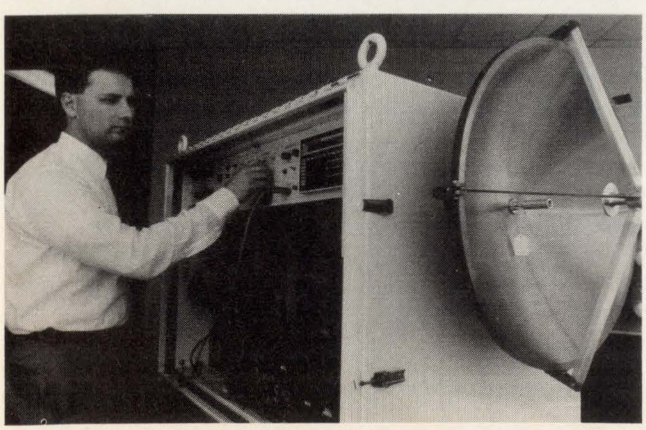
Researchers can vary several system parameters, including polarization, bandwidth, frequency step size, and pulses. As a result, HIPCOR is unusually flexible for a coherent radar of its size, according to Ted Lane, senior research scientist in Georgia Tech's Radar and Instrumentation Laboratory.

The radar permits pulse-to-pulse frequency agility in either a high-power mode, 2000 W with a 350-MHz bandwidth, or medium-power mode, 100 W at a 2-GHz bandwidth.

A Masscomp computer serves as the primary radar controller and data-acquisition system. Georgia Tech developed hardware and software to make the radar remotely controllable. The school is also developing software that will let the Masscomp handle data reduction and analysis and system diagnostic work, with much of the processing in real time.

"HIPCOR's step frequency approach will allow the Army to investigate how much resolution it really needs to try to detect different kinds of targets with various background conditions," says Lane. The general scenario, according to Lane, is an airborne radar looking down at the ground trying to discriminate tactical vehicles from natural and man-made clutter. The idea is to develop fine-grain target signatures that can differentiate a tank, for instance, from less important targets or even clutter.

JOHN NOVELLINO



Polymer Meets Needs Of Multichip Modules

A new class of polymeric materials called benzocyclobutenes, or BCBs, from Dow Chemical Co., Midland, Mich., seems poised to challenge existing polymers for a critical job, that of an insulating film in multilayered, thin-film, multichip modules (MCMs). The electrical and mechanical characteristics of the BCBs are considerably better than those of its nearest rival, polyimide.

Multichip modules critically depend on an insulating layer's electrical and physical parameters to achieve acceptable interconnection density, performance, and producibility. Of all the parameters, dielectric constant is the most critical.

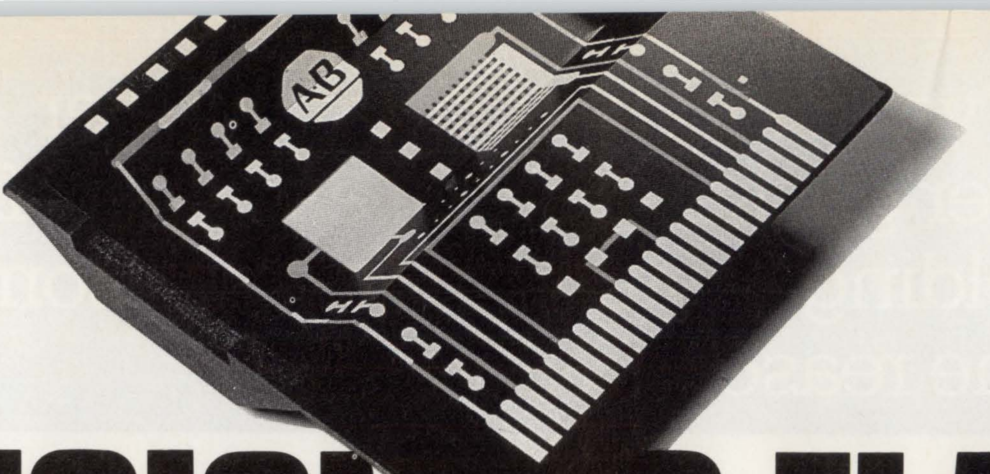
One reason is that dielectric constant determines the maximum density of the circuitry; it sets the line impedance and spacing necessary to minimize crosstalk between signal lines. A material with low dielectric constant allows close packing of interconnection lines and therefore higher density.

At 1 kHz, polymers derived from BCB have a dielectric constant of 2.66 and a dissipation factor of 0.001. These figures compare favorably with polyimide's dielectric constant of 3.2 to 3.5 and dissipation factor of 0.002. Also, water absorption by dielectric films can drastically increase their dielectric constants, degrading the electrical characteristics of the interconnections. BCB absorbs only 0.5% of water (by weight) after a 24-hour immersion at 100°C. Under the same conditions, polyimide absorbs 2 to 3% of its weight in water.

The new polymers can be easily processed using standard thin-film fabrication techniques to build high-density interconnection structures. To prove the concept, Dow produced a functional three-metal-layer test structure with aluminum conductors and BCB as the interlevel dielectric.

After the structure was thermally cycled, resistance measurements of its daisy-chained conductor patterns indicated good continuity and reliability between metal layers. Such results imply that the thermal stresses resulting from mismatches in moduli and coefficients of thermal expansion were not sufficient to crack the test structure's conductors.

JERRY LYMAN



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CIRCLE 20

MULTICHIP MODULES AIM AT NEXT-GENERATION VLSI

ADVANCED PACKAGES MIX IC AND THIN-FILM PROCESSES TO REACH NEW HIGHS IN PACKAGING DENSITY AND SPEED.

JERRY LYMAN

After several false starts, wafer-scale integration, the holy grail of packaging, still remains a paper concept. But the multichip module (MCM), a hybrid version of WSI, is coming on strong, with at least 50 companies worldwide actively working on it. Evidencing the importance of MCM, three technical sessions with a total of 14 papers cover all phases of the new packaging method at this week's National Electronic Packaging and Production Conference (Nepcon West, '89) in Anaheim, Calif.

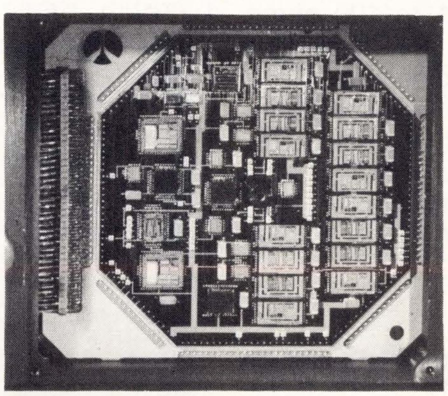
Major efforts are being made to develop MCMs because conventional interconnection and IC packaging technologies cannot meet the challenge of current and future VLSI superchips. Production-level IC chips are now at the 1-μm feature level, and 0.5-μm chips should arrive in two to four years. By the late 1990s, promises of 0.3-μm IC families could come true. At these levels, multilayer pc boards or thick-film hybrids simply won't allow the new VLSI to perform at full capability.

The MCM, on the other hand, with its low-dielectric-constant polymeric materials (such as polyimide with a dielectric constant K of 3.4, or benzocyclobutene with a K of 2.66) and with extremely short chip-to-chip wiring, provides a substrate enviroment suitable for fast chips. And, equally important, the IC-like features of the substrate's interconnection make possible wiring densities at least two to three orders of magnitude higher than do comparable pc or thick-film hybrid interconnections *(see the table)*.

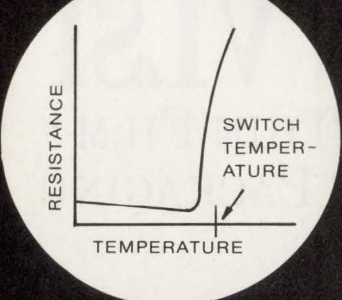
Many of today's MCMs are thin-film multilayer hybrids with metal conductors and polymeric insulating layers built on ceramic, silicon, or metal substrates. Alternatively, an MCM can also be a silicon substrate multilayered and patterned using conventional IC processing.

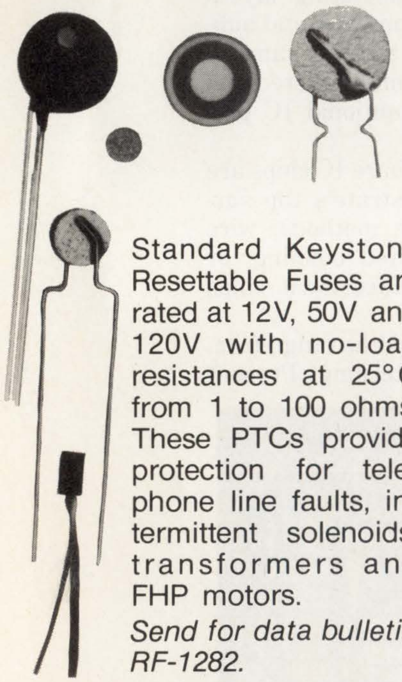
In either approach, bare IC chips are connected to the substrate's top surface by one of three methods: wire bonding, tape-automated bonding, or with solder-bumped face-down chips (flip-chips).

Module conductor widths range from 75 to 5 μm (IC-type patterning). Present



1. TWO 1750A PROCESSORS and support chips consisting of 140 components and 1080 connections are incorporated on one 2.5-in.^{2} silicon substrate. This multichip module from Rockwell International uses a thin-film aluminum/polyimide structure.





PROPERTIES OF INTERCONNECTION TECHNOLOGIES

	Chip density (Chips/in²) MSI	VLSI*	Wiring density (Lines/in./layer)	Thermal conductivity (W/cm/°K)	Mechanical strength (bending moment)	Signal speed (ns/in.)
Printed-wiring boards	2	0.5	20	0.02	Low	0.15
Multilayer ceramics	20 ‡	4	200	0.08	Medium	0.50
Copper polymide	20 ‡	4	500	0.20	Medium	0.40
Silicon wafers	36 ‡	9	1250	1.48	High	0.30

* 20 Kgates/cm² chip ‡ Bare chips Source: Mosaic Systems Inc.

thin-film MCMs typically have five conductive layers composed of power and ground planes, orthogonal X and Y wiring planes, and a top layer composed of IC pads and extra pads for engineering changes.

But before plunging headlong into this technology, a potential developer should consider the range of skills needed to design and make a module of this type. These include circuit design (more akin to system design), thin-film assembly, IC processing, transmission-line techniques, thermal management, packaging, and selecting a mechanical interface to the next level of interconnection.

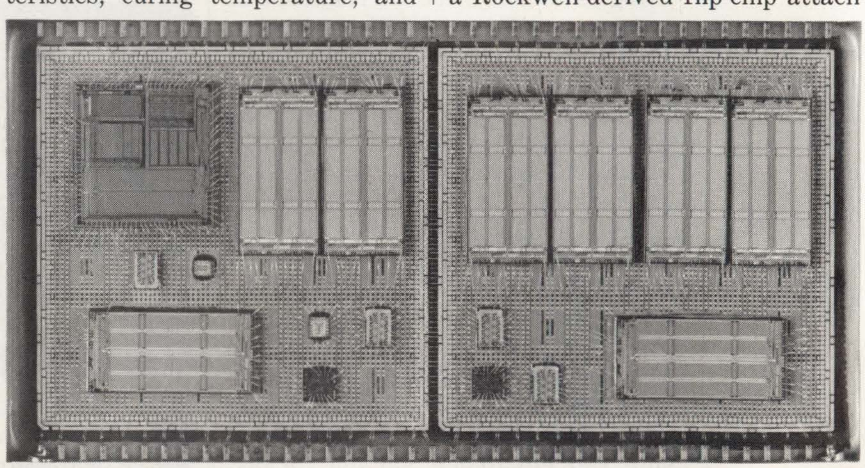
The designer must also pay close attention to the thermal, mechanical, and electrical properties of all the materials used. For example, the substrate material's temperature coefficient of expansion must nearly match that of silicon. The other critical material is the insulating polymer. Here, the polymer's dielectric constant, water-absorption characteristics, curing temperature, and etching method affect the module's eventual yield and performance.

One of the more recent examples of MCM technology is a fast dual 1750A CPU developed and tested by the Autonetics Sensors and Aircraft Systems Division of Rockwell International Corp., Anaheim, Calif. The MCM was built by Rockwell's Collins Avionic Group in Cedar Rapids, Iowa.

DUAL PROCESSORS

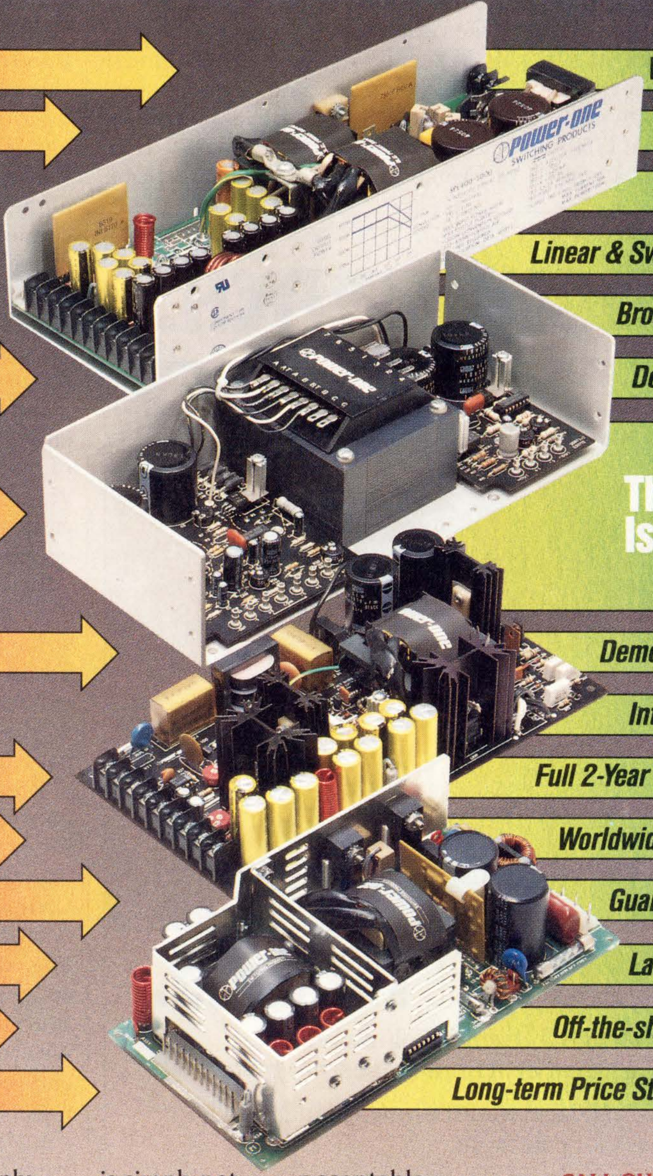
The module crams two 1750A processors, a memory-management unit, 16 kbytes of EEPROM, 512 kbytes of static RAM, and a system interface chip onto a 2.5-by-2.5-in. silicon substrate *(Fig. 1)*.

The silicon substrate has four metal layers with 1-mil conductors on 2-mil spaces deposited on alternating polymeric layers. Chips are wire-bonded. According to James Spear, manager of advanced design and packaging for the company's Sensors and Aircraft Systems Division, a Rockwell-derived flip-chip attach-



2. THE EQUIVALENT OF A ONE-BOARD COMPUTER is compressed into a 1.4-by-2.6-in. package by Mosaic Systems' all-silicon hybrid. The two small modules contain an INMOS transputer, 1 Mbyte of dynamic RAM, and memory interface logic.

Power-One Has Good News And Great News



- Incomparable Power-One Quality
- Exacting Workmanship Standards
- Tough Double Test & Burn-in
- CAE/CAD Designs
- Extensive R&D Investment
- Thick Film Hybrid Technology

The Good News Is What We Put Into Our Power Supplies

- Large Volume Production
- Advanced Circuit Technology
- Proprietary Production Processes
- Total Vertical Integration
- MIL-I-45208A Inspection Program
- MIL-Q-9858A Quality Program
- Statistical Process Control
- Experience — Over 5 Million Sold

- Value... Service... Economy
- Trouble-free Performance
- Worldwide Product Acceptance
- Linear & Switching Technologies
- Broadest Standard Product Line
- Dependable Factory Support

The Great News Is What You Get Out

- Demonstrated High Reliability
- International Safety Approvals
- Full 2-Year Warranty
- Worldwide Distribution
- Guaranteed Customer Satisfaction
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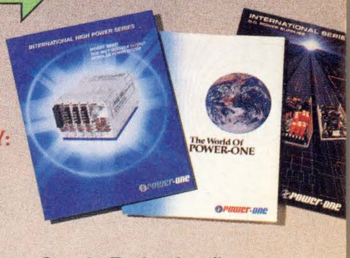

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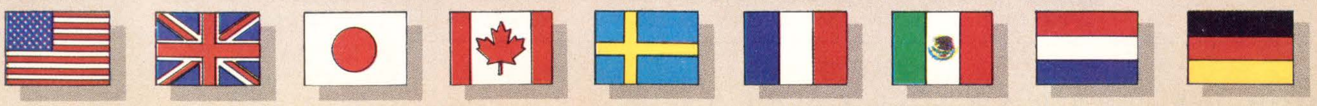

CIRCLE 22

ment method will be used on future MCM designs.

The module has been run at 30 MHz, but Rockwell designers believe it can be made to operate at up to 40 MHz. In comparison, the 1750A chip set used in the MCM runs at only 20 MHz in its normal IC package.

Designers who don't have an MCM facility at their disposal must go outside for their custom substrate. In the U.S., designers have four sources: Mosaic Systems Inc., of Fremont, Calif., with an all-silicon structure; Polycon, of Ventura, Calif., with an aluminum/polymer thin-film substrate; Rogers Corp., of Chandler, Ariz., with a copper-polyimide substrate; and Advanced Packaging Systems, a Raychem/Corning Venture in San Jose, Calif., with an aluminum/polyimide thin-film interconnection on either a silicon or ceramic substrate. Outside the U.S., companies in Japan, the United Kingdom, and France have MCM facilities. But these are for in-house use only.

Mosaic features an off-the-shelf silicon substrate with a built-in grid of metal lines and amorphous silicon vias. The lines and vias can be electrically programmed to connect bare chips wire-bonded to the substrate.

In a recent application of this all-silicon hybrid, two 0.933-by-0.957-in. substrates containing an INMOS T4414 transputer, 1 Mbyte of dynamic RAM, and memory interface logic were crammed into a 1.4-by-2.6-in. package *(Fig. 2)*.

Present-day MCM technology is impressive enough, but what might be on the way is mind-boggling. For example, the Microelectronics and Computer Technology Corp. (MCC), Austin Texas, has a long-term objective to package a 10-million-gate computer with a 3-ns cycle time in four multichip modules, each containing 25 to 36 chips—all for $9000, chip cost not included. This would mean cutting the present cost of a copper/polyimide interconnection from $\$40/ft^2$ to $\$10/ft^2$.

The Microelectronic Center of North Carolina, Research Triangle Park, North Carolina, plans to eventually put the equivalent of the largest serial computer on a 4-by-4-in. MCM. Every module will contain 25 0.5-μm chips, each composed of 330,000 gates. Because of this theoretical system's high power dissipation, MCNC is developing a silicon carbide substrate and investigating liquid cooling. □

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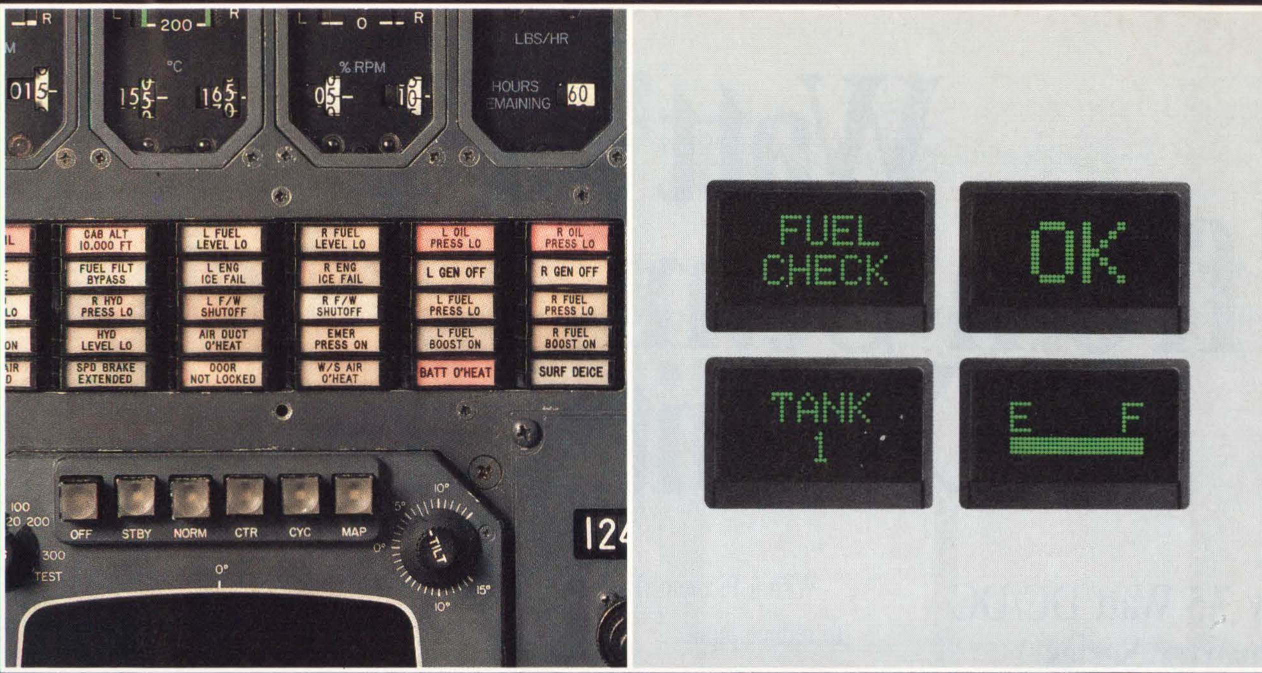

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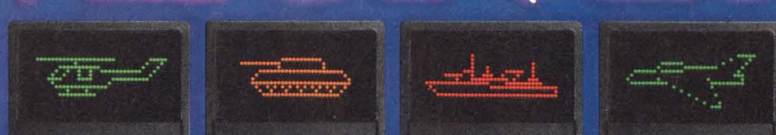

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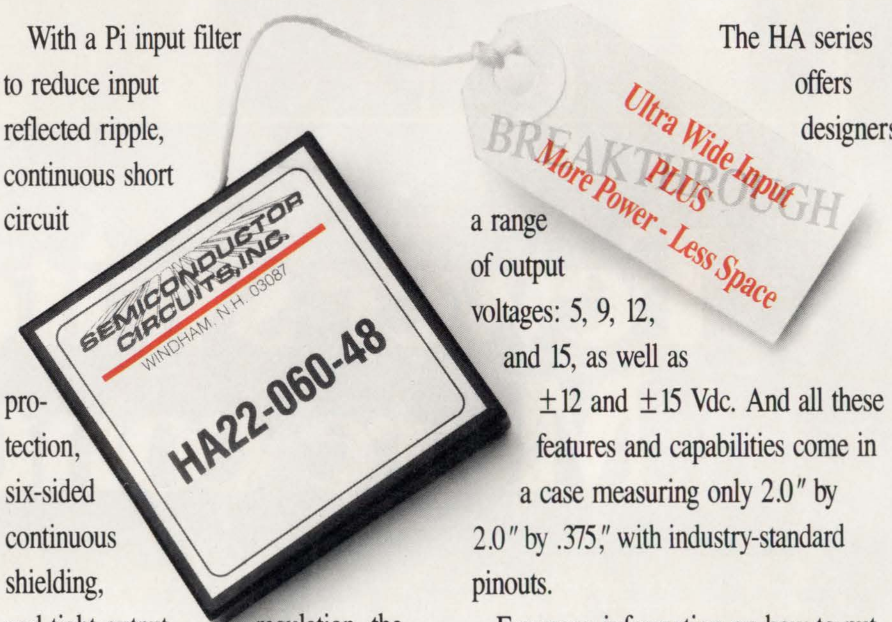

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CIRCLE 18

Behavioral Models Open Windows On Complex Integrated Circuits For Effective System-Level Debugging.

Device Models Show Chip Operation

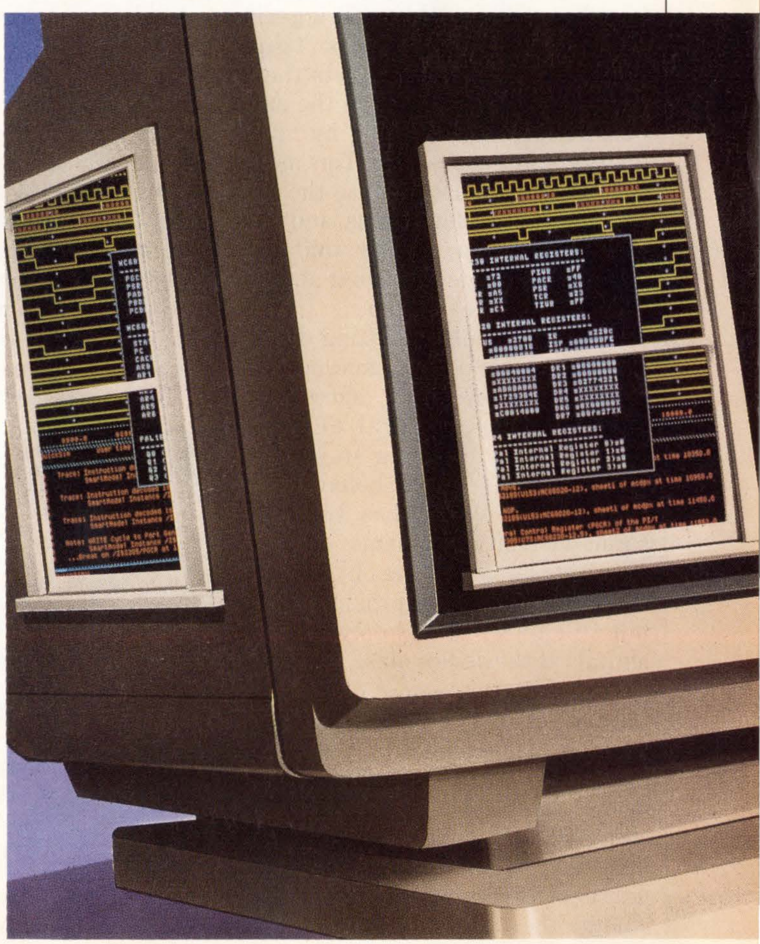
Bob Milne

Engineers who must verify system-level designs got a break a few years ago when Logic Automation Inc. came out with its SmartModels behavioral-simulation models. Now comes the icing on the cake—SmartModel Windows lets designers see the internal workings of the device being simulated. In effect, this modeling technique acts like an emulator for an entire circuit board.

With these models, a designer running a simulation can not only look inside the registers of all the devices on his board, but also change their contents. For consistency and ease of use, the Windows feature uses the simulator's standard user interface. Users can examine processors, peripherals, programmable logic devices, and memories. They can set breakpoints, including word-specific breakpoints, single-step through instructions, and change register values. They can even set breakpoints to span combinations of register values across multiple devices on a board.

At introduction, SmartModel Windows will be available for Motorola processors and peripherals, plus a broad range of programmable logic devices. The Motorola devices include the MC680X0 processor family, along with MC68230, MC68440, MC68442, MC68452, MC68851, MC68881, and MC68HC11 devices. PLDs include a full range of products from Advanced Micro Devices, Altera, Lattice Semiconductor, Monolithic Memories, and Texas Instruments. In July, Intel devices will be available, and by the end of the year all devices in the SmartModel library will have Windows.

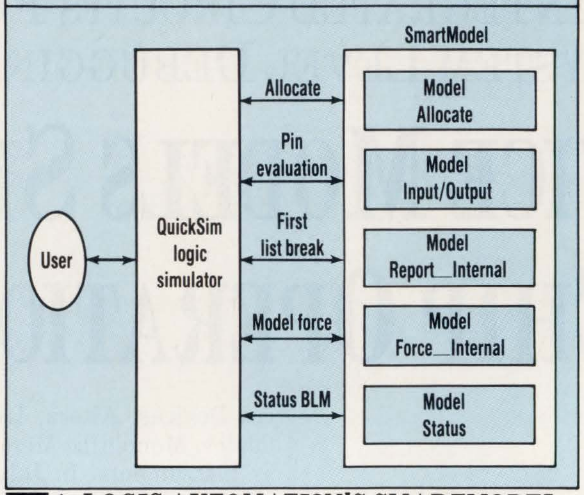
SmartModel Windows will initially be released for Mentor Graphics' QuickSim logic simulator. Meanwhile, work is under way to add it to Hewlett-Pack-



ard's design-automation system.

Never easy, verifying designs has become almost an ordeal. A designer developing a board based on a 68020, for example, faces 89 internal registers in the processor alone. Besides, the associated floating-point unit has 8 32-bit registers and 8 80-bit registers, and the control logic typically consists of PLDs with 10 to 40 buried states. To debug such a circuit board, the designer must determine what's going on inside each of these devices. With conventional verification tools, he must troubleshoot by looking at the signals on a device's I/O pins. Then he must try to divine the inner workings of the internal registers.

SMARTMODEL WINDOWS INTERFACE

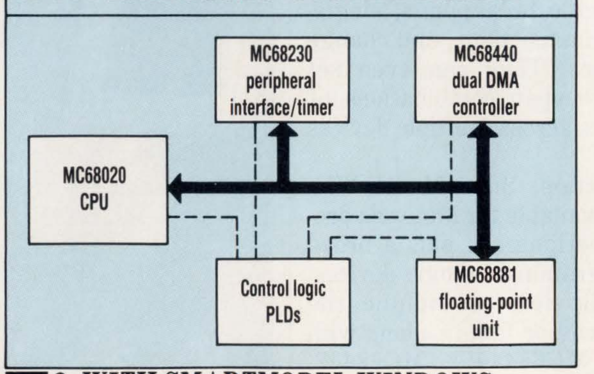


1. LOGIC AUTOMATION'S SMARTMODEL Windows links with Mentor Graphics' QuickSim logic simulator at five major points. The allocate and pin evaluation points are found in all behavioral models. The remaining three are unique to the special Windows models.

Even with instrumentation that's made faster and deeper to handle more complex devices, triggering is still a major problem. Triggering on a word, for example, doesn't guarantee that the designer gets the information he needs, since the same outputs can be produced by vastly different internal states. This means the designer must analyze the data collected at the device pins, and from the progression of how that data changes try to deduce what actually happened inside the chip.

Emulators help by letting designers look inside popular microprocessors. But they don't address the problem of peripheral devices. Simulation using standard models—either behavioral or gate-level—has the same visibility problems. It eliminates many of the physical problems, such as probing, but still allows access only to signals at the device pins.

A TYPICAL 68020 SYSTEM BOARD



2. WITH SMARTMODEL WINDOWS, a designer can simulate this 68020-based design and view the internal register operation of all the devices.

SEE INSIDE REGISTERS

With SmartModel Windows, the picture changes dramatically. Access to on-chip registers yields two main benefits: visibility into internal registers and the ability to change their contents. Of the two, visibility is by far the most important asset, because it gives the designer a more complete understanding of chip and system operation.

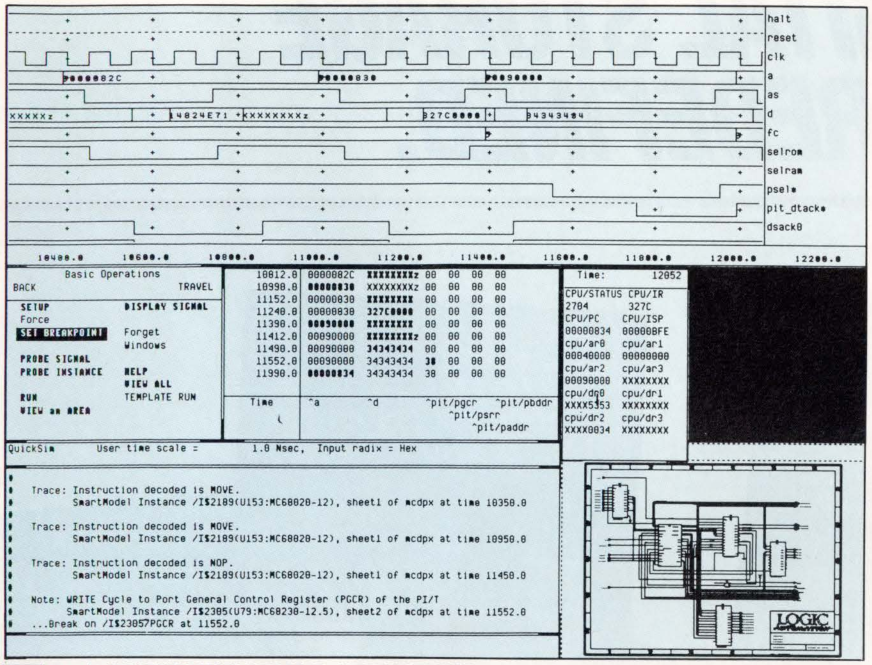
The ability to change the contents of registers during simulation can be a mixed blessing, though. The good news is that it lets the designer confirm the results of such changes right away. He can find out whether a particular change solves his problem, and if it does, he can go back to the processor source code and/or schematic and make the change.

There is a need for caution, however. With today's complex devices and systems, all the side effects of changing register contents might not be apparent until much later in the simulation run. At this point, the engineer may have forgotten which registers were changed, at what time, and so on.

SmartModel Windows are implemented by tightly coupling the SmartModel directly to the simulator's existing user interface. The user can therefore work with the model's internal registers in the same way that he works with the design's external nets (signals). In other words, the designer can simulate, trace, or break on internal registers exactly as he does with nets. He doesn't have to learn any new interface commands, and on-line aids help him identify internal registers and determine how they're used.

Consider, for example, Mentor Graphics' QuickSim logic simulator. The commands that control QuickSim's operation are Force, to apply stimulus; List, to generate tabular listings of stimulus-and-response patterns; Trace, to create stimulus-and-and response waveforms; and Break, to stop execution of the simulator when a specified condition is met. Each of these commands applies equally to any net in a design and to a SmartModel's internal registers. Users can get on-line help with the Status BLM command.

SmartModel Windows and QuickSim have five major interface points between model and simulator (*Fig. 1)*. The top two points exist in all behavioral models. These supply the basic initialization, input, and output (from nets to pins) interaction with the simulator. The Force Internal and Report Internal points are specialized simulator hooks that let the SmartModel communicate with the simulator outside the normal net-pin in-



3. A QUICKSIM SIMULATION RUN using SmartModel Windows gives a designer much more than a conventional waveform display. The listing in the middle of the screen shows 68020 processor address and data buses, along with peripheral interface/timer register contents.

teraction. The Status interface gives access to the on-line help specific to that SmartModel.

To get a feel for how you can use SmartModel Windows, consider a microprocessor system *(Fig. 2)*. This 68020-based system board has RAM, ROM, some control logic implemented in PLDs, and several support chips. The PLDs supply interrupt and bus-arbitration logic, as well as address decoding. The peripheral chips include an MC68440 dual-DMA controller, an MC68230 parallel interface/timer, and an MC68881 floating-point unit.

To access these chips' complex internal states, the designer typically changes his machine code to read the registers through their data ports and back to the processor. But changing source code to read from peripheral chips can be time-consuming. It's also prone to the same errors designers face in trying to write to the chips. If the data he reads back is incorrect, the question becomes, "Did the write to the chip fail, or did the system read it incorrectly?" SmartModel Windows avoids this quandary by letting the designer actually see the write data being loaded into the peripheral chip's register.

For example, consider a QuickSim screen display of a write cycle to the MC68230 PIT parallel interface/timer chip. The traces at the top show a write to address 90000 hexadecimal, which is the memory-mapped address of the port general-control register (PCGR). The data the processor is writing is 34 hexadecimal, which configures the MC68230's parallel port into the unidirectional 8-bit mode.

The designer can also set a breakpoint inside the MC68230 to break when the PGCR register changes. This action can be seen in the transcript window at the bottom left of the screen *(Fig. 3)*. Notice also in this window the debugging messages that have been printed. The processor tells what instruction is executing, and the PIT prints out a message when a write cycle has occurred—in this case just before the breakpoint. A listing in the screen's center shows the processor address and data buses, along with register values inside the PIT.

Finding The Problem

To the right of the list window, another window shows the current values of some of the MC68020 processor registers. The write address just used is ar0 and the data just written to the PIT is dr1. This confirms that the designer's machine code did load the correct address and data values to write to the peripheral. Back in the list window, notice that the PIT/PCGR register just changed from 00 to 38 hexadecimal. This is a problem because the processor just wrote a 34 to the PIT, but 38 is what got written.

A design error was the culprit. Data-bus bits 2 and 3 were connected backward to the MC68230, causing the write cycle to incorrectly initialize the parallel port. If the designer wasn't able to look into the MC68230 as the write cycle occurred, this error would have been much more costly, as it would have to be caught farther downstream.

The SmartWindows user is doubly blessed, because he can instantaneously correct the problem by typing the QuickSim command "force pit/pgcr 34." This command loads the correct value into the PGCR, allowing the designer to continue debugging without quitting the simulation. Thus, he can continue simulating a correct design, even though he must make some changes to the schematic later.□

Price And Availability

Containing over 4000 devices, the SmartModel library is available as a subscription service in one-year increments for $7900 per workstation. The SmartModel Windows option costs an additional $4000. The first SmartModel Windows will be available in April.

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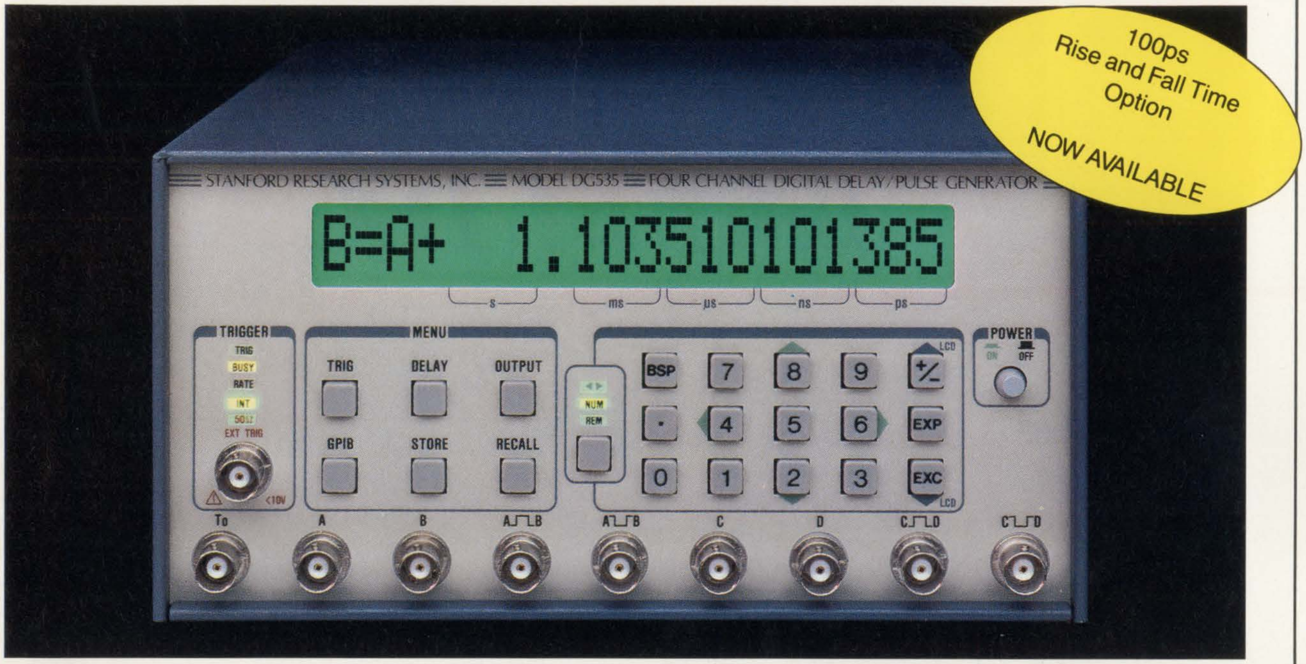

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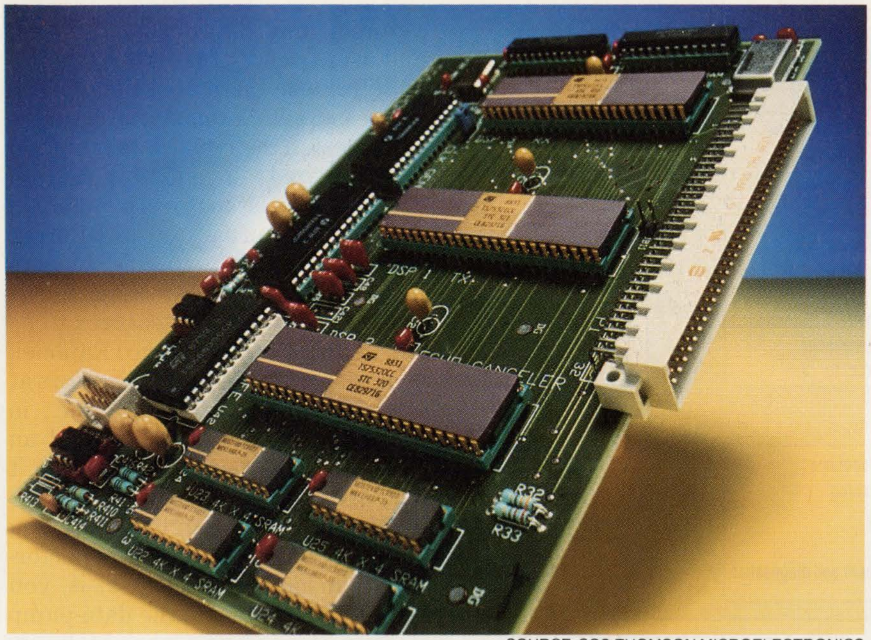


SOURCE: SGS-THOMSON MICROELECTRONICS

BLACK MAGIC: BUILDING A V.32 MODEM

PUTTING A 96,000-BIT/S MODEM TOGETHER IS PART SCIENCE, PART ART.

JOHNA TILL

Designing a high-speed dial-up modem is a lot like devising a Ferrari Testa Rossa: At high speeds, new problems appear and old ones are exacerbated. Just as Ferrari designers have to cope with increased cooling requirements, streamlining, and aerodynamic stability, high-speed modem designers must deal with echo cancellation, error-correction encoding, and tighter requirements for analog components. In a similar vein, the design of the modem's "engine"—the data pump—is critical to the unit's performance.

Although it's possible to go faster with complex data-compression algorithms, the fastest standard dial-up modem is defined by the CCITT Recommendation V.32. At 9600 bits/s, full duplex, this is truly the Ferrari of modems.

"It's certainly the most exciting standard from a technology standpoint," says Dudley Westlake, modem marketing manager at Rockwell International Corp.'s Newport Beach, Calif., division. No other modem packs adaptive equalization, echo cancellation, and trellis coding along with options for backward error correction and data compression.

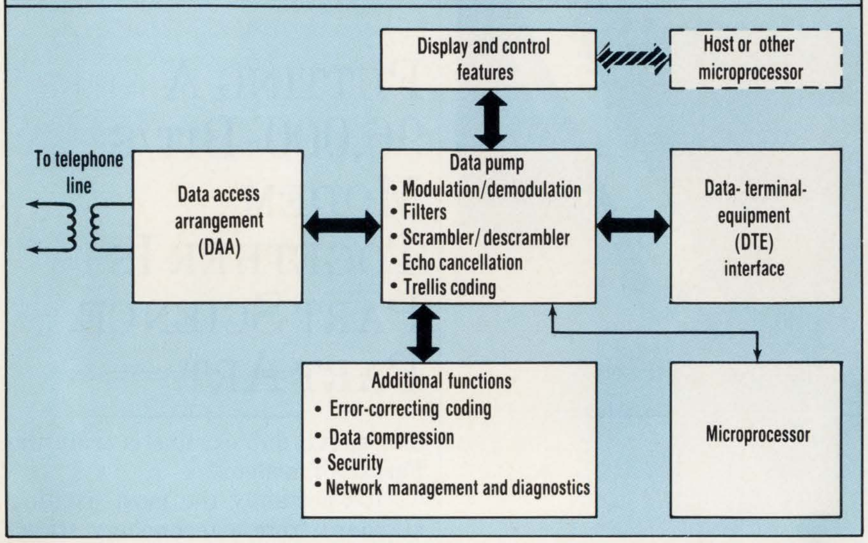
Designing such a powerhouse can be a daunting task. As you begin to design a V.32 modem—whether as part of your next system or to enter the high-speed modem marketplace—you might wonder where to begin. For starters, take a brief look at the modem's engine.

The heart of a V.32 system—as in any modem—is the data pump, which handles the modulation and demodulation of the signal. In a V.32 modem, the data pump also handles forward error-correction encoding, filtering, equalization, scrambling and descrambling, and echo cancellation.

Most often, the data pump's design is part analog and part digital. The analog section takes care of various front-end jobs, including analog-to-digital and digital-to-analog conversion. It also deals with near-end echo cancellation. The digital part consists of some digital signal processors, which perform the trellis coding, adaptive equalization, and filtering for far-end echo cancellation.

Though V.32-data-pump design

FUNCTIONS SPLIT INTO SIX PARTS



1. A V.32 CAN BE THOUGHT OF as dividing functionally into six blocks. These blocks can be designed separately, but work together in a complete modem.

sounds straightforward enough, it's usually described by experts as a "black art." As with the temperamental Ferrari, careful tuning and tweaking is necessary to achieve optimum performance. Consequently, one of the first design issues in building a V.32 machine is deciding how much of the data pump to build yourself. Designers often turn to a predesigned chip set or module for the data pump and turn their energies toward the modem's other features. To better understand these design options, it helps to examine the rest of a V.32 modem.

Functionally, the modem can be divided into six parts. Besides the data pump, there's the data-access-arrangement (DAA) circuit, the data-terminal-equipment (DTE) interface, control and display functions, the microprocessor, and other "value-added" functions, such as backward error-correction and data compression *(Fig. 1)*.

The DAA is the interface between the modem and the telephone lines. Though it can be tricky to design—especially in the case of the V.32—it often comes as part of a chip set, requiring only a transformer and resistor. The specifications for some components—the transformer, in particular—are quite stringent because the transformer's linearity directly affects how well the echo-cancellation algorithm works. If you've designed a DAA before, though, making one for a V.32 modem shouldn't present a tremendous obstacle.

Similarly, interfacing to the DTE should be easy. Electronic Industry Association standard 232-D and the CCITT recommendation V.32 govern the connectors, cable, and lead use. The main problem here is inside the DTE. Small computers often can't handle a full-duplex 9600-bit/s rate, and there can be buffer overload problems.

Designing the control and display circuitry and choosing the microprocessor depend on what added functions the modem will need. If you want to use complex data-compression algorithms, for instance, you'll have to ensure that the host processor can handle the computation. You may, in fact, want to use an auxiliary processor just for data compression.

USER-FRIENDLY FEATURES

Choosing and designing the modem's special features can constitute the whole of the design. On top of data compression and backward error-correction, you can add security features, such as encryption, passwords, and callback; network management and diagnostic abilities; and user-friendly features like autodial. Because there are so many other areas to work on, manufacturers often design their own data pumps in order to avoid reinventing the wheel. They work on either offering more in the total modem package or tailoring the modem to fit specific system needs. "A merchant modem needs most of the standard features to be competitive," says Howard Raphael, chairman of the board of directors at Cermetek Microelectronics Inc., in Sunnyvale, Calif. "Designers of an OEM modem, though, can groom it for specific system needs."

Of course, you might decide you want to build an optimum-performance modem as well. That is, you might want to tackle the data-pump design. If so, you should know what's involved.

A V.32 data pump includes adaptive equalization, echo cancellation, and trellis coding. Both echo cancellation and trellis coding are relatively new techniques, and both seem fairly straightforward in theory. The real world, however, is not as simple. Echo cancellation, in particular, is much harder to do in practice.

An echo canceler does just what its name implies—it cancels echoes. These echoes arise from signal reflection at impedance mismatches at the two- to four-wire hybrids. There are several different kinds of echo, and all must be canceled.

Listener echo appears when a modem's receiver first hears a signal and then hears its echo. The echo results from making an extra trip across either the two- or four-wire connection *(Fig. 2)*. Because the echo is usually much weaker than the original signal, listener echo isn't a problem. Generally, listener echo is stripped out during adaptive equalization.

Talker echo is far more troublesome. It results from the reflection of a modem's transmitted signal back into its receiver. Near-end echo arises when the reflection is at the two-wire-to-four-wire interface, and far-end echo comes from the four-wire-to-two-wire hybrid *(Fig. 3)*. Because the echo is that of the transmitted signal, it's much larger than the received signal. This is because the received signal might have traversed as much as thousands of miles of cable.

Canceling this type of echo can be very tricky. Often, the near-end echo is canceled at the modem's analog front end, so digital signal processing can be done on a signal with less dynamic range. Because the received signal is so small—with an average attenuation of 33 dB—the a-d converter might not have enough bits to handle both types of echoes with sufficient accuracy. Deciding where to cancel the near-end echo, in fact, is an important factor in the modem's design.

Once you've stripped out the near-end echo, the far-end echo cancellation begins. The transmitted signal is fed to an echo emulator, which emulates the changes that the transmitted signal has presumably undergone during its far-end reflection—chiefly delay.

SHAKING HANDS

The delays are calculated during the initial handshaking part of the V.32 protocol, in which each modem sends a signal (half-duplex) down the line to find the line's echo characteristics. This information then sets the taps in the echo emulator's digital filters. The presumed echo (transmitted signal after filtering) is subtracted from the total received signal, and the result is checked for correlation with the transmitted signal using a decision-feedback-equalizer type of algorithm. If there's correlation between the received signal and the transmitted signal, the echo emulator is modified to try to cancel it. When the transmitted signal and the received signal show no correlation, the echo has been successfully removed *(Fig. 4)*.

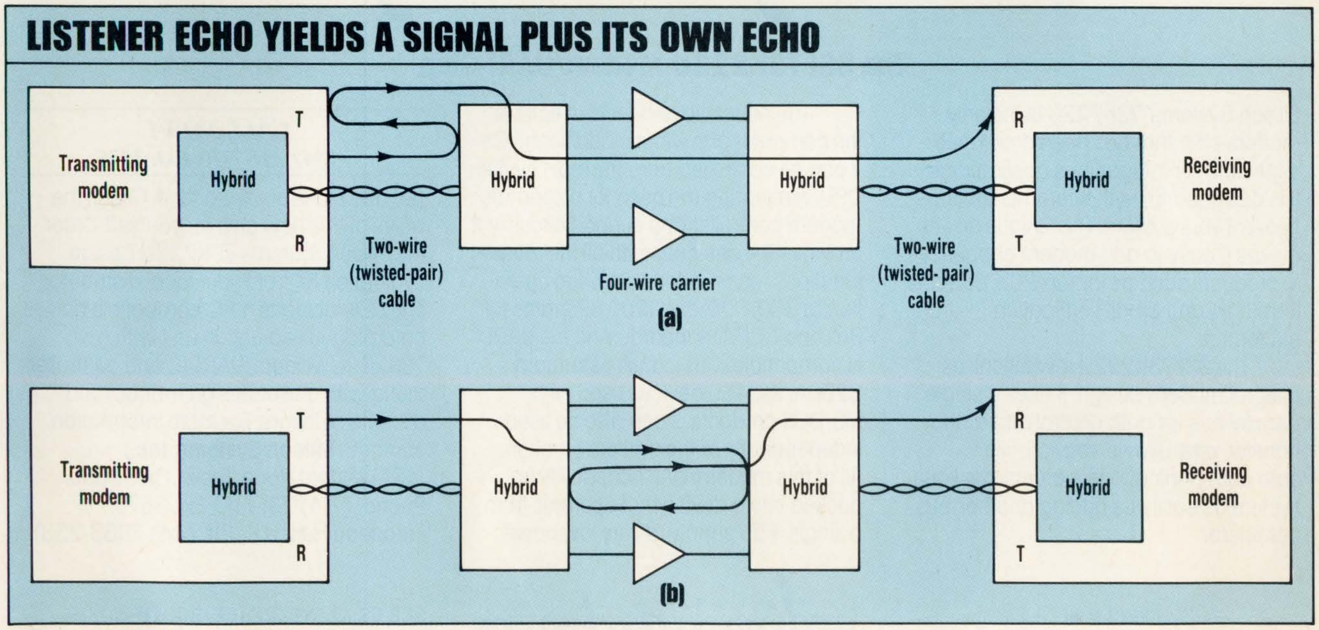
All this takes place in real time, with limited signal-processing resources. Not only is there a finite number of filter taps for what might be an infinite situation, but also the algorithm for setting them must be fast, accurate, and robust.

One solution to the problem of canceling echoes is to buy a pre-programmed echo-cancellation DSP chip, such as SGS-Thompson's TS75320 CP echo-cancellation IC. You could then design the data pump around it. But even this doesn't get you out of the woods, because other aspects of the pump design can get hairy. These include the timing and carrier recovery, the trellis-coding algorithm, and subtle problems like phase roll and ground noise.

The timing in a V.32 modem is determined by the transmitter. A crystal-based clock in the data pump sets the time for the transmitted signal, but the modem has to lock the received signal to the transmitted data. It does that at a rate determined by the transmit clock. Because crystals in the two modems aren't matched exactly, what tends to happen is that the received signal slowly precesses with respect to the transmitted signal. This problem can be difficult to solve.

PHASE ROLL

Sometimes, thanks to phase roll—another unexpected difficulty—signals change rapidly with respect to each other. Especially on international lines, the far-end echo can include a frequency shift. A signal that goes out at 1.8 kHz, for instance, can come back at 1.801 kHz. This is because as the signal travels along the trunk line, it undergoes a slight frequency shift. If it returns on the same trunk line, the shift is canceled out. If not, phase roll could occur. In this case, "There's an awful lot of black magic involved, because people don't agree on the characteristics of the far-end echo and the phase roll," warns John Bingham, a data-transmission consultant from Palo



2. LISTENER ECHO is when a signal reflects across the two-wire line (a) or the four-wire line (b), so that the receiver picks up an echo. It's not a critical issue in modem design.

Alto, Calif.

Trellis coding is another design that's simple on paper but difficult to make work accurately. It isn't unusually tough to implement, but the catch is finding an algorithm that's robust enough to stand up to real-life line requirements, yet compact enough to execute quickly. Telephone-line situations are often much worse than you would suspect, and your algorithms must be particularly durable.

The basic idea behind V.32 trellis coding is that four bits are encoded as five, increasing the number of points in the point-constellation signal space from 16 (2^4) *(Fig. 5a)* to 32 *(Fig. 5b)*. The minimum distance between points also increases, making their detection less ambiguous. Trellis coding—also called forward error correcting—is really a way to minimize, rather than correct, errors. It works best with predominantly white noise, rather than burst noise. Backward error-correcting encoding works better in situations in which there's a lot of burst noise. In many cases, you need both kinds of coding.

The big trade-off with trellis coding is between the amount of data you save for encoding and the amount of processing you must do. Finding a balance between the two is necessary for a robust algorithm.

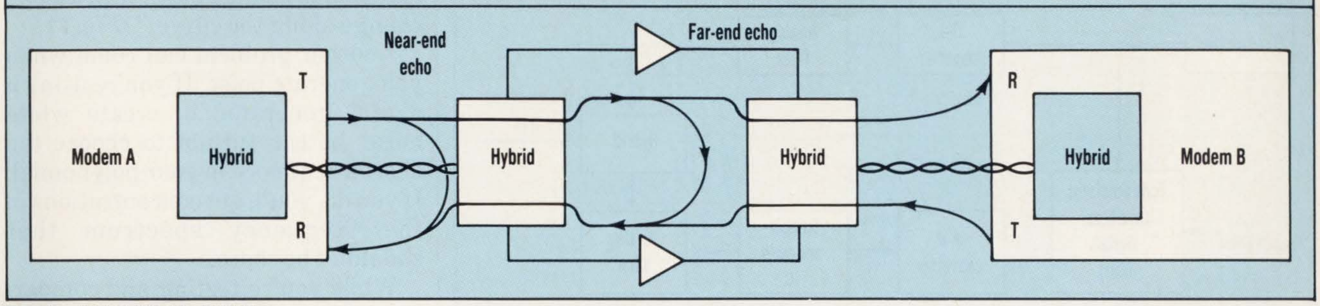
With timing and coding difficulties, the problem is that when a V.32 modem realizes it's no longer receiving correct data, it "retrains" or reinitializes. While not a problem in slower modems—some can retrain in under a second—retraining in a V.32 can take up to 10 to 12 seconds. If a modem has to retrain too often, its throughput degrades considerably. If your timing solutions and trellis algorithms aren't carefully thought out, your modem will perform poorly.

Circuit layout can also cause problems. If you use switched-capacitor circuitry, you get noise when the frequency at which the FETs are switched beats with timing frequencies. Other noise difficulties arise when the noise floor from the analog front end gets too high. In this case, when you lower the received signal level, but maintain the same signal-to-noise ratio, you'll find that you can't pick up the signal because of the internal noise. To avoid these problems, you must take extreme care when routing your digital lines to be sure that they're properly isolated from the analog lines. Solid separate grounding is a must.

Modem Gurus

It takes experienced modem designers to foresee these problems, and most design teams talk about having a "modem guru," as well as a signal processing expert, on board.

TALKER ECHO ADDS THE TRANSMITTED TO THE RECEIVED SIGNAL

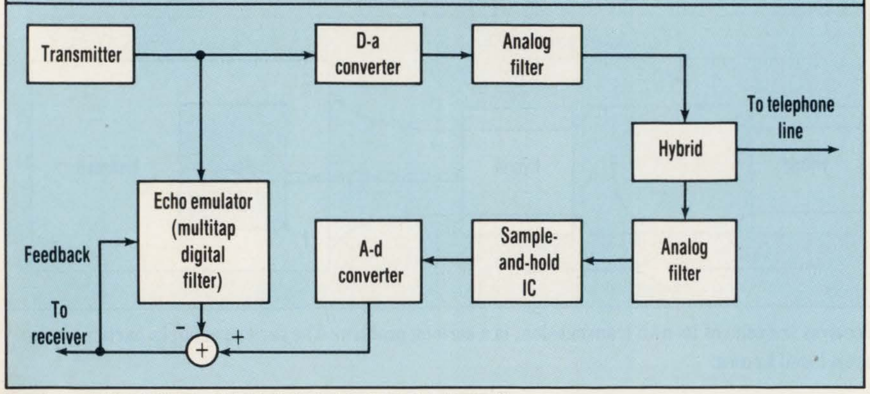


3. TALKER ECHO, in which a modem receives the echo of its own transmission, is a serious problem. The far-end echo, in particular, is difficult to cancel because its characteristics aren't well known.

These engineers can also be helpful in yet another way: interpreting the standards. "Because standards like the V.32 were written by people with a knowledge of the art and science of modem design, they are written in a sort of shorthand," says William Berger, a group leader in modem applications at Rockwell. "Inexperienced designers may underestimate, or miss entirely, the significance of a deceptively simple statement."

Clearly, the first design issue you'll face is whether to buy or build the data pump. If your design team has high-speed experience, you can afford to take the extra time—as long as an extra year—to get the modem to market. And if your company has the resources, building your own might make sense. You can use either general-purpose digital signal processors—many engineers recommend TI's TMS320 DSP series—or custom or semi-custom parts. Though it would take longer, your own design might be more economi-

ECHO EMULATOR CANCELS ECHOES



4. AN ECHO CANCELER OPERATES by simulating the transmitter echo and subtracting it from the received signal. If the resulting signal has no correlation with the transmitted signal, it's the true received signal.

cal and perform better. This depends, of course, on how good your design is and how many V.32 modems you plan to build.

On the other hand, if you need a V.32 modem as part of a system, must get to market quickly, and aren't making an overwhelming number of modems, your best bet might be to go with a predesigned data pump. Several good V.32 data-pump chip sets and modules are available, including a module from Rockwell and chip sets from Phylon, SGS-Thompson, and Universal Data Systems.

Each Pump Is Different

Because every pump's characteristics are different, you'll want to take a few months to test different pumps before deciding on one. You should design a test bed, simulate telephone lines, and check out bit-error-rate (BER) versus signal-to-noise ratio. Also, look carefully at things like the data pump's phase jitter and noise level *(Fig. 6)*. Measure the amount of phase roll it can handle. See how many times the pump must retrain over different telephone lines. After all, "Not all data pumps are created equal," warns Ken Miller, chief technology officer at Concord Data Systems Inc. in Marlborough, Mass. Sam Deus, V.32 project leader and senior electronics engineer at NEC America Inc. in San Jose, Calif., concurs. "Performance evaluation of the data pump is the most critical aspect of the design," he says.

Also, be aware of what is and isn't included on the data-pump chip set or module. Some data pumps have extra features, such as dialing commands. Check to see which diagnostics are present: Is there a full suite of test functions? Some chip sets don't include remote digital loopback abilities (CCITT Recommendation V.54, loop 2). Others don't include the Viterbi decoding algorithm, so you'll have to add your own. This algorithm might add another 25% to the amount of processing, so you might consider adding another DSP chip or using a bigger processor. Again, some chip sets don't include scramblers and de-scramblers.

Modem testing is an art in itself, especially when it comes to engine performance. For this reason, some manufacturers limit themselves to data-rate, compatibility, and throughput measurements. If you want to get deeply involved in performance issues, though, there are a few items to watch out for. One is to be sure that you're only varying what you think you are. "Repeatability of test results is a problem," says William Berger of Rockwell. "Analog test equipment with manual dials makes it easy to make a slight change in setting, with a big change in the modem's results. For instance, waterfall curves—BER versus signal-to-noise ratio—are very steep, and a small change may mean a large change along the curve." *(Fig. 7)*

Another problem can come when you generate noise. If you're using a digital generator to create white noise, be careful not to choose too short a sequence in your polynomial. If you do, you'll get concentrations in the frequency spectrum that shouldn't be there.

While you're testing and comparing data pumps, you can be working on the DAA, controlling processor, extra features, and user interface (if there is one). Critical to the success of your design at this point is "a dedicated team—one that works well together," according to NEC's Sam Deus. He further notes, "Your hardware designer doing the DAA and EIA interface must work closely with the designer doing the controlling code."

Component Engineering

On the DAA side, most of the design revolves around choosing the parts correctly. "Component engineering is even more important in a V.32 modem than in other modem designs," says Darryl Sell, vice president of engineering at Racal-Vadic, in Milpitas, Calif. This is particularly true when dealing with the transformer at the telephone-line interface. Finding a transformer that's highly linear, but in which the primary coil is conducting perhaps 100 mA of dc current, is no easy task. "Your transformer must have at least –65 dB and preferably –70 dB of harmonic distortion," Sell points out. John Bingham warns, "One way to get burned building V.32s is to cut pennies on the transformer."

Depending on the data pump you've chosen, choosing the transformer might be all the analog designing you do. If not, the choice of an a-d converter is important. "If you want to be classical about it, just taking the incoming signal and digitizing it, you need a 14-to-15-bit converter," says Sell.

Other issues crop up when you design the architecture of the modem's processing and control section. A

critical decision is which microprocessor to use. The conventional choice for modem control is a Z80, but many designers warn that this won't be powerful enough for a V.32. "If you're upgrading from a Z80, a good choice is the 64180, so you can use the same code," says Concord Data's Ken Miller. "It has direct memory access, paging, and other good features. Some high-end designers even go to the 68000 series for CPU-intensive tasks."

Another crucial decision is which functions to implement in the controlling processor and which to do in other hardware. An example is controlling serial communications. If you do it with the microprocessor, you can save the cost (and space) of an extra piece of hardware. Pack too many functions on your processor, though, and you'll need to choose a more powerful, expensive design to keep the system's real-time performance acceptable.

There's a similar problem with memory. If you write your control code in a high-level language, it will be portable and easier to design and debug. On the other hand, it takes up more memory. To save the cost of memory, you might end up writing it in assembly language.

FOR MORE INFORMATION

A good source for readers wishing to learn more about V.32 modem design is *The Theory And Practice Of Modem Design*, by John A.C. Bingham, John Wiley and Sons, 605 Third Ave., New York, NY 10158; (212)-850-6497.

An interesting part of the V.32 modem design is adding the extra functions. These differentiate one V.32 modem from the next, and it's with these that designers target their modems to end users or tailor them for integration into a specific system. As in most aspects of the design, standards are important here. "Make a list of your requirements, then look at the relevant international standards," says Howard Raphael of Cermetek.

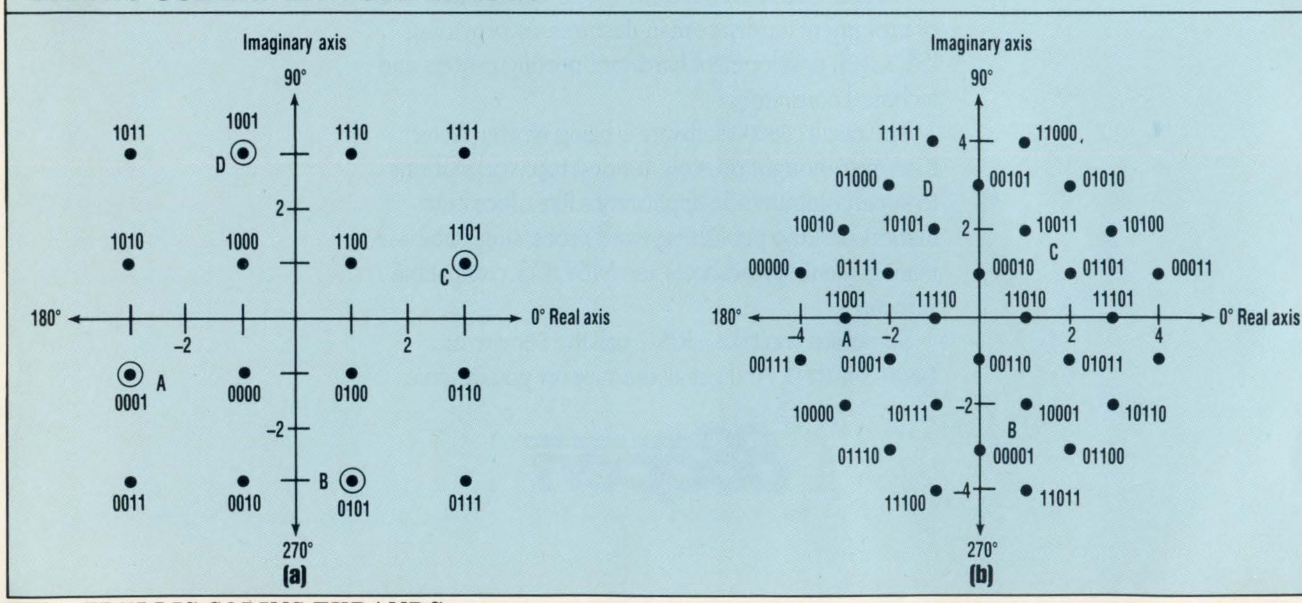
One of the most likely candidates for inclusion here is a backward error-correction protocol. While the V.32 recommendation already specifies one error-correction protocol (trellis coding) just to attain its 9600-bit/s data rate, adding another ensures that the data delivered by the modem is correct.

Backward error-correction is basically error-correction by retransmission. Data is packaged into packets, then framed by framing, control, and addressing bits. Some form of cyclic redundancy check is added to the packet, and then it's transmitted. The modem at the other end checks each packet for data integrity. If the packet is error-free, the receiving modem informs the transmitting modem with an acknowledge signal. If there are errors, the receiving modem sends back the packet address with an error signal, and the packet is retransmitted.

COMPLY OR CONFORM

Two common protocols for this type of error-correction are the Microcom Network Protocol (MNP), level 4, and the Link Access Protocol D (LAPD). The two are not compatible. The CCITT recently decided upon a compromise between them in its V.42 recommendation: Rather than choose one protocol over the other, V.42-compliant modems will include LAPM, a protocol similar to LAPD, and MNP-4 (LAPM and LAPD, while similar, aren't identical). A V.42 modem will determine which protocol its connecting modem uses. If both use LAPM, the link will follow that protocol. If not, the link

TRELLIS CODING REDUCES ERRORS



5. TRELLIS CODING EXPANDS the number of points in signal space for a 4-bit sequence from 16 (a) to 32 (b). In signal space, the y-axis is amplitude and the angle is phase.

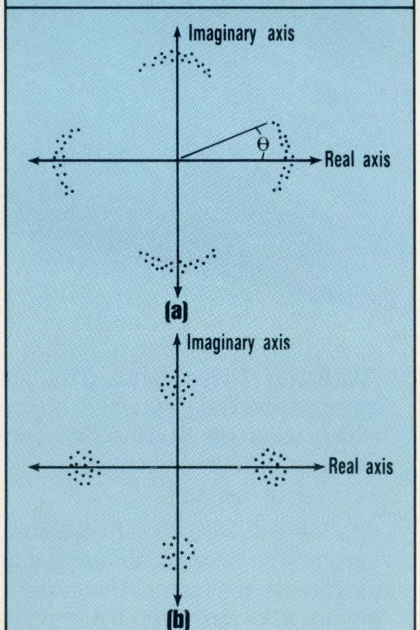
will be made using the MNP level 4 protocol.

"Key here is the word *compliant*," says Dave McNamara, a senior product planning manager at Codex Corp. in Mansfield, Mass. "A modem that supports just MNP-4 is *compatible* with the V.42 recommendation, as is one that supports just LAPM—but neither of them are compliant with V.42."

V.32 designers must choose one or the other—or both—of the protocols for their applications. One factor to keep in mind is that the MNP-4 is a proprietary protocol (developed by Microcom), and it requires licensing fees. Of course, designers could also develop their own error-correction protocols. This strategy would make the most sense if the modems were designed for a closed environment—say, a factory floor.

Data compression is another option for V.32 designers. With a 2:1 data-compression ratio, the 9600-bit/s rate jumps to 19.2 kbits/s; with a 3:1 algorithm, the rate rises to 38.6 kbits/s. One of the most widely implemented data-compression algorithms is included in the MNP level 5 protocol suite. Because it's the first broadly implemented compression algorithm, MNP-5 has become something of a defacto standard.

PHASE JITTER AND NOISE



6. PHASE JITTER can be seen when the points don't change amplitude much (y-axis coordinate) but vary in theta, the phase (a). It's distinct from white noise, in which the amplitude and phase change randomly (b).

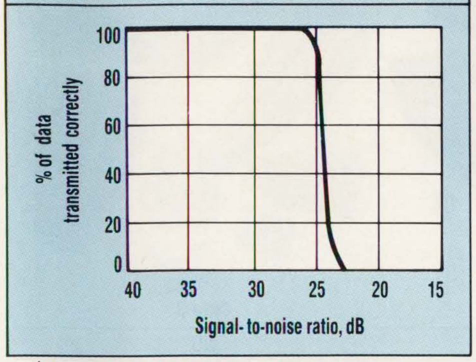
However, the CCITT is in the process of deciding upon a recommendation governing data compression. This recommendation will probably be known as V.42 bis, and the algorithm under consideration is one developed by British Telecom. MNP-5 isn't being considered, in part because the MNP protocols violate the OSI 7-layer model for communication protocols. Consequently, designers who want their modems to comply with a future standard for data compression would do well to conform to the V.42 bis.

The V.42 bis data-compression algorithm is an example of a smart data-compression algorithm, one which adapts the compression to the type of data. In the V.42 bis approach, the encoder (compressor) and decoder (decompressor) maintain identical dictionaries of strings. The encoder accepts characters and matches them to the longest string in the dictionary. It then sends the index of the string to the decoder, which reconstructs the string from its own dictionary. The key is that the dictionaries are adaptive—the encoder builds the dictionary by observing the input characters. Because the decoder must maintain an identical dictionary, error-free communication between the two is vital.

WRITE, FARM, OR BUY?

Another feature to think about carefully is the modem's command set. If you're designing for the European community, you'll probably want to go with the CCITT V.25 bis recommendation. If it's for the American PC marketplace, however, you'll most likely want to choose the Hayes AT command set. And if the modem is to be integrated into a system as a PC card, you have a choice between writing your own software drivers, farming the task out to a software company, or buying prefabricated drivers.

A TYPICAL WATERFALL CURVE



7. A SLIGHT CHANGE in the signal-to-noise ratio causes a dramatic increase in the bit-error rate.

Other features to consider are security, diagnostics, and network management. The type of security capabilities you choose will depend on how secure the communications must be. A fairly simple form of security is password security, in which the modem doesn't grant access without the correct password. Another is automatic dialback, in which the user gives the modem an I.D. or password, and the modem calls back to a prestored number. A user that's not at that number clearly won't get access to the modem.

CRYPTIC MODEMSPEAK

A more comprehensive form of modem security is encryption, in which the data itself is encrypted. Users decode the data with a system of keys, and key management becomes an important issue. Security and network management are thus closely linked.

Diagnostics and network management are also linked. One of the more useful purposes of a network management system is the ability to discern the type and cause of a modem failure and decide on the appropriate action. This could be dispatching a technician to the modem site, for instance.

More basic forms of diagnostics are covered in the CCITT recommendation V.54, which describes two kinds of loop-back testing appropriate for modems. Loop 3 is a local analog loop-back ability. It basically involves hooking the transmitter to the receiver, although the situation in V.32 is more complex, thanks to the echo cancellation. Loop 2 is a remote loop-back test. In this mode, one modem sends a test pattern to a remote modem, which returns it.

Both loops are usually included as part of the engine. If they aren't, it might be wise to include them, either alone or as part of a more comprehensive network-management package.

After you've designed or chosen your data pump, picked your processor, and agreed on the features to include, it's time to think about one of the more subtle aspects of modem design: meeting Federal Communications Commission (FCC) and Electronic Industry Association (EIA) specifications. In the U.S., these bodies govern things like radiation emission and lead functions in connectors. If a modem is to operate in the U.S., it must be FCC-certified. Particularly troublesome to modem designers is part 68 of the FCC rules, which defines the DAA circuitry, and parts 15a and 15b, which regulate the radiation of industrial and commercial equipment.

"Some designers don't think about these things until the last minute," says Deus. "Then they must rely on Band-Aid fixes. It's better to design carefully from the beginning." Another FCC regulation to keep an eye on is the "drop test"—any hand-held device must be able to withstand a drop of a certain distance.

One piece of advice that's echoed by most modem manufacturers is to find out what you're getting into with a V.32 design. "Do your homework," says Dave McNamara of Codex. "Don't underestimate the complexity. Collect every piece of information available," Deus agrees. Miller says, "Be careful, because this is a very sophisticated technology—much more so than other modems."□

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CIRCLE 35

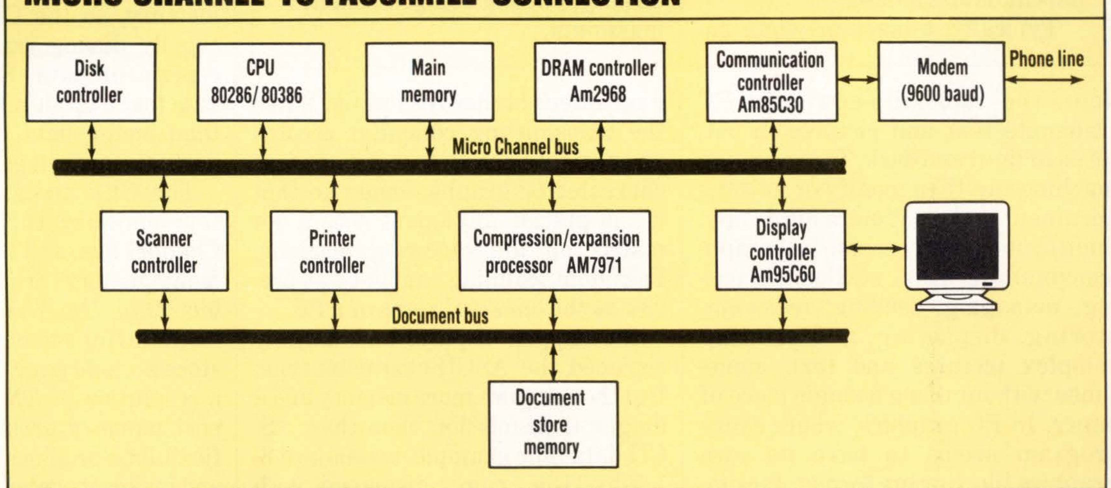
A Compression And Expansion Processor Squeezes More Data Into Less PC Memory And Speeds Up Fax-Like Transmissions.

PC Facsimile Transfer Steps Up

PC-facsimile transmission becomes faster and takes up less space in your PC's memory with a dedicated hardware chip that compresses and expands software-generated data. One such chip, the Am7971A Compression/Expansion Processor (CEP) from Advanced Micro Devices, compresses a bit-mapped image in a PC system as much as 50 times, in accordance with international CCITT standards. The compressed data not only occupies less memory space, but takes less time to send over regular phone lines. The chip also makes it possible for PCs to receive fax transmissions over phone lines and to display the expanded image on a display terminal.

Instead of transmitting text in alphanumeric bytes through a traditional mo-

MICRO CHANNEL TO FACSIMILE CONNECTION



1. THE CEP GATHERS DATA from an input device through the Micro Channel bus and sends it to the document memory through the document bus.

GOVIND KAMATH
Advanced Micro Devices, 5900 E. Ben White Blvd., Austin, TX 78741; (512) 462-5817.

THE CEP: AN EXPANDED LOOK

The CEP (Compression/Expansion Processor) is a high-performance peripheral that compresses and expands two one-bit mapped images in accordance with internationally accepted standards. The chip supports Modified Huffman (MH) run-length coding as well as Modified Read (MR) and Modified-Modified Read (MMR) coding, as recommended by CCITT T.4 and T.6 for Group 3 and Group 4 compatible equipment. MH coding is a one-dimensional technique that identifies and codes run lengths of black or white pixels.

MR coding compresses a single scan line using MH coding, followed by K–1 scan lines (two-dimensional), coded in reference to the previous line. MMR coding is a full two-dimensional type that uses an all-white imaginary reference line when coding the first scan line.

All lines on the page are coded two-dimensionally. The compressor and expander operate not only in full-duplex mode, but each processor can be independently programmed for one-dimensional encoding/decoding, two-dimensional encoding/decoding, or transparent data transfer.

Typically, a black or white image will yield compression ratios ranging from 5:1 to 50:1. A gray-scale image may yield negative compression, producing a "compressed" file larger than the original. In such cases, the CEP passes data through without modification. The CEP has an on-chip error-detection mechanism that detects data corruptions by checking for illegal codes, negative run lengths, and incorrect line lengths. The architecture allows for error recovery with minimal intervention from the CPU.

Document page width is programmable for up to 16,000 pixels. A programmable frame width makes windowing possible, and programmable top, left, and right margins allow image boundaries to be left blank. An optional express mode skips one line after a predetermined number of lines, accelerating compression.

On the expansion side, the granularity option lets the processor duplicate every one to seven lines. In the two-dimensional mode, the programmable K-parameter defines the number of lines to be encoded in a 2D coding sequence before a 1D line is inserted. For error-free environments, K is set to infinity, putting compression at a maximum.

dem, the facsimile-equipped PC transmits text and pictures in patterns of light and dark. The receiving machine can then modify or edit the document and print out a hard copy. Such systems can become full graphics-communication stations, creating, managing, sending, receiving, storing, displaying, and printing complex pictures and text, sometimes without using a single piece of paper. In PC graphics, where every program seems to have its own graphics file-storage format, facsimile could deliver the blessings of standardization.

Digitizing images by bit-mapping, as a PC does, rather than by scanning, as a facsimile machine does, guarantees higher resolution. When the transmitting computer creates an image, it lines up each dot of a text character or graphic image so that it's in precise alignment with a dot matrix on the receiving machine. Facsimile scanning cannot be as precise as the ones and zeros of a PC.

Bit-mapped displays have largely replaced the ASCII-character type. But they require more memory and a longer transmission time than ASCII data. For example, a standard 8-1/2-by-11-in. page, displayed with 300 lines per in., requires about 1 Mbyte of bit-mapped memory versus 4 kbytes of alphanumeric characters. Software compression and expansion is 10 to 20 times slower than hardware compression, because standard microprocessors aren't suited for the algorithmic and bit-intensive operations needed in compression techniques. Special-purpose hardware, such as the CEP, gives designers a dedicated processing solution.

CEP ARCHITECTURE

For maximum performance, the CEP contains two separate buses: the system bus and the document bus. Data transfers between the CEP and main memory take place on the system bus; those between the CEP and the document memory take place on the document bus. One DMA controller on the CEP chip serves both, but DMA transfers cannot take place on both buses at the same time. Slave transfers, however, can occur on the system bus while a DMA transfer is taking place on the document bus *(see "The CEP: An expanded look")*.

The CEP processes two types of data: uncompressed, or image, data and compressed, or coded, data. Both types have their own external storage buffers. The image buffer is usually stored in document memory because of its high data rate. For maximum performance, this buffer should be large enough to store one uncompressed document. The code buffer is usually stored in main memory, so the CPU can access it rapidly during transmission or reception of data. Since compressed data takes up significantly less room than image data, it does not slow down the overall performance.

The CEP accesses the main-system memory through the Micro Channel bus, and the on-board document memory through the document bus *(Fig. 1)*. The on-board, document-buffer memory (1 Mbyte) can store a whole page of bit images with a resolution of 300 dots/in. A dual-port memory architecture provides flexibility in allocating buffer sizes and makes it easier to access the document bus, Micro Channel bus, or the CPU. For compression, the system loads the bit image into the document memory and initializes the CEP registers. During this procedure, the

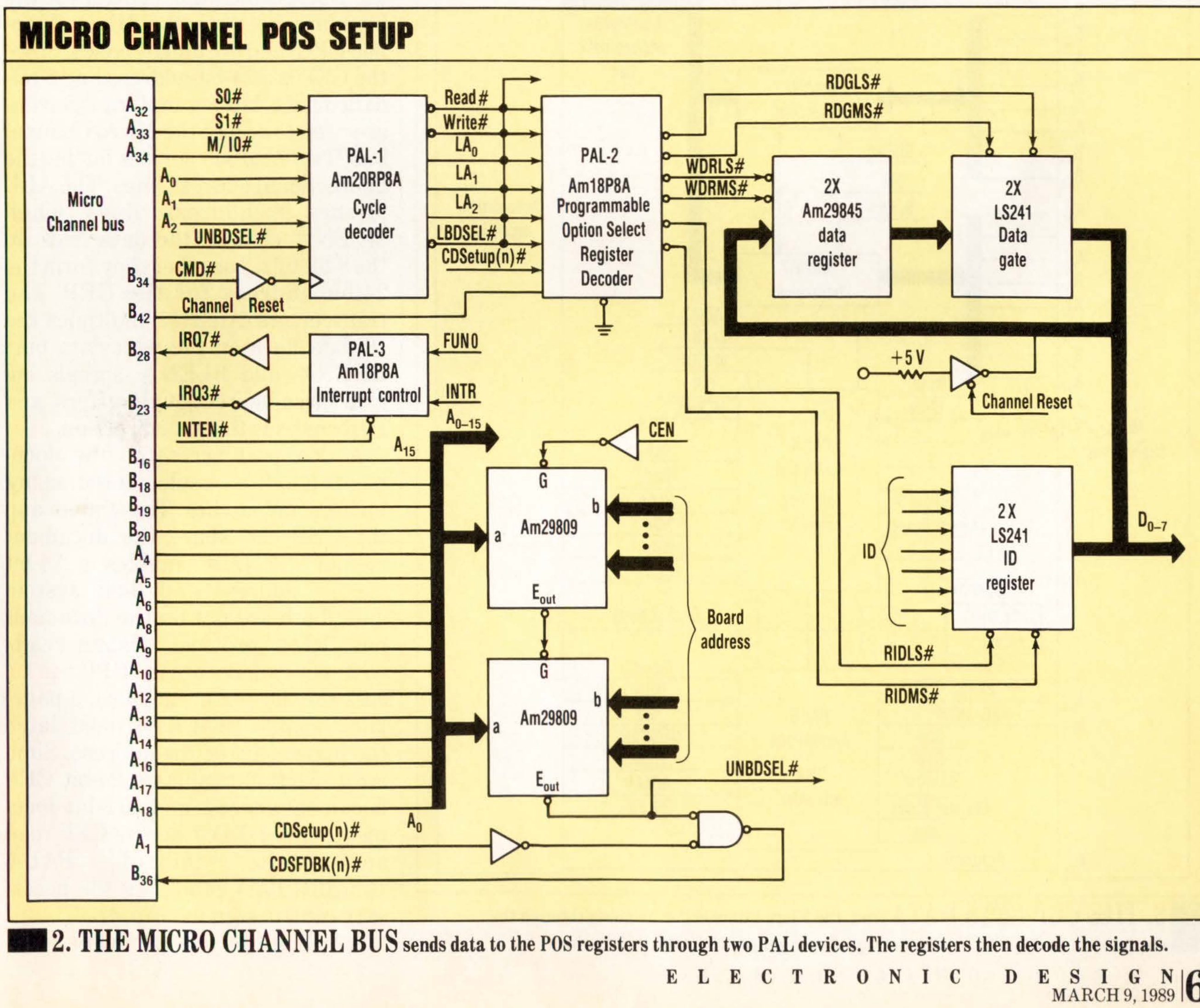
CEP transfers the compressed data back into the document memory. The CEP then transfers this data to the main memory or to a mass-storage device using on-chip DMA. Next, the data is sent out through a serial-communication device and a modem to another fax system.

During expansion, the compressed data is first loaded into the system's main memory and then sent to the CEP for processing. The expanded data is then stored in the document memory, to be sent to a laser printer or to a display terminal for further editing and processing. Both the compression and expansion logic are completely independent and can operate simultaneously. In principle, the compression and expansion work with any image resolution. In practice, however, if resolution is too low, the compression ratio becomes insignificant. For images such as halftones, the compressed data may even be larger than the original. In this situation, the CEP alerts the CPU by setting an interrupt and a status bit. A transparent mode is enabled, thus bypassing compression.

The Micro Channel system has two modes of operation: board setup and board command/data transfer. It implements a board setup and selects a programmable option select (POS) algorithm that identifies the presence of I/O boards in a system. An ID number, read by the system, identifies these boards. Then it writes the selected options to the POS latches. System information is kept in nonvolatile RAM and is available to the setup algorithm at each power-up.

Each slot in the system has a separate CDSetup(n)# line that is used for board setup. The POS registers are decoded, and the read and write signals are generated by two PAL devices (Am20RP8A and Am18P8A) from the bus signals S0#, S1#, M/IO#, and address lines A0, A1, and A2, and latched by a CMD# signal *(Fig. 2)*. Upon system request, the signals RIDLS# (lower or LS byte) and RIDMS# (upper or MS byte) enable the board ID. If the system identifies an approved ID, it writes option bits into data registers using the signals WDRLS# and WDRMS#. These registers contain information such as board address, board enable, arbitration level, and special-function selects. The system can read these option bits from the data gates, using signals RDGLS# and RDGMS#.

During normal operation, the system sends out a 16-bit I/O address to read or write to the registers on the



2. THE MICRO CHANNEL BUS sends data to the POS registers through two PAL devices. The registers then decode the signals.

CEP board. Two comparator chips decode the unlatched 16-bit address and option bits IA0 to IA2; the unlatched decoded board select (UNBDSEL#) signal enables the dedicated-slot feedback signal (CDSFDBK[n]#). The system uses this signal to verify the board's availability. It is restrained, however, during the setup cycle when CDSetup(n)# is active. The latched board select (LBDSEL#) and latched address (LA0) generate a valid CEP-select signal (CS) using PAL-4 *(Fig. 3)*.

All control signals are synchronized to the CEP clock, in this case 8 MHz. PAL-1 decodes read and write signals using the bus signals S0#, S1#, and M/IO#. PAL-4 (Am22V10A), which includes the board-select signal (LBDSEL#), generates synchronized read and write signals to the CEP. A Ready signal from the CEP is gated to ensure that the CEP completes the previous operation. The CEP's ALE generates MCEN# and ADRC signals to latch the necessary addresses from the Micro Channel bus. A CHReset signal from the Micro Channel generates a Reset using PAL-5 *(Fig. 3, again)*.

PAL-4 also generates the I/O ready command (CDCHRDY[n]#). This input on the Micro Channel bus must not be inactive (low) for more than 3 μs. An active CS# signal makes CDCHRDY# inactive. This keeps the host CPU in a wait state until a valid read or write signal is available.

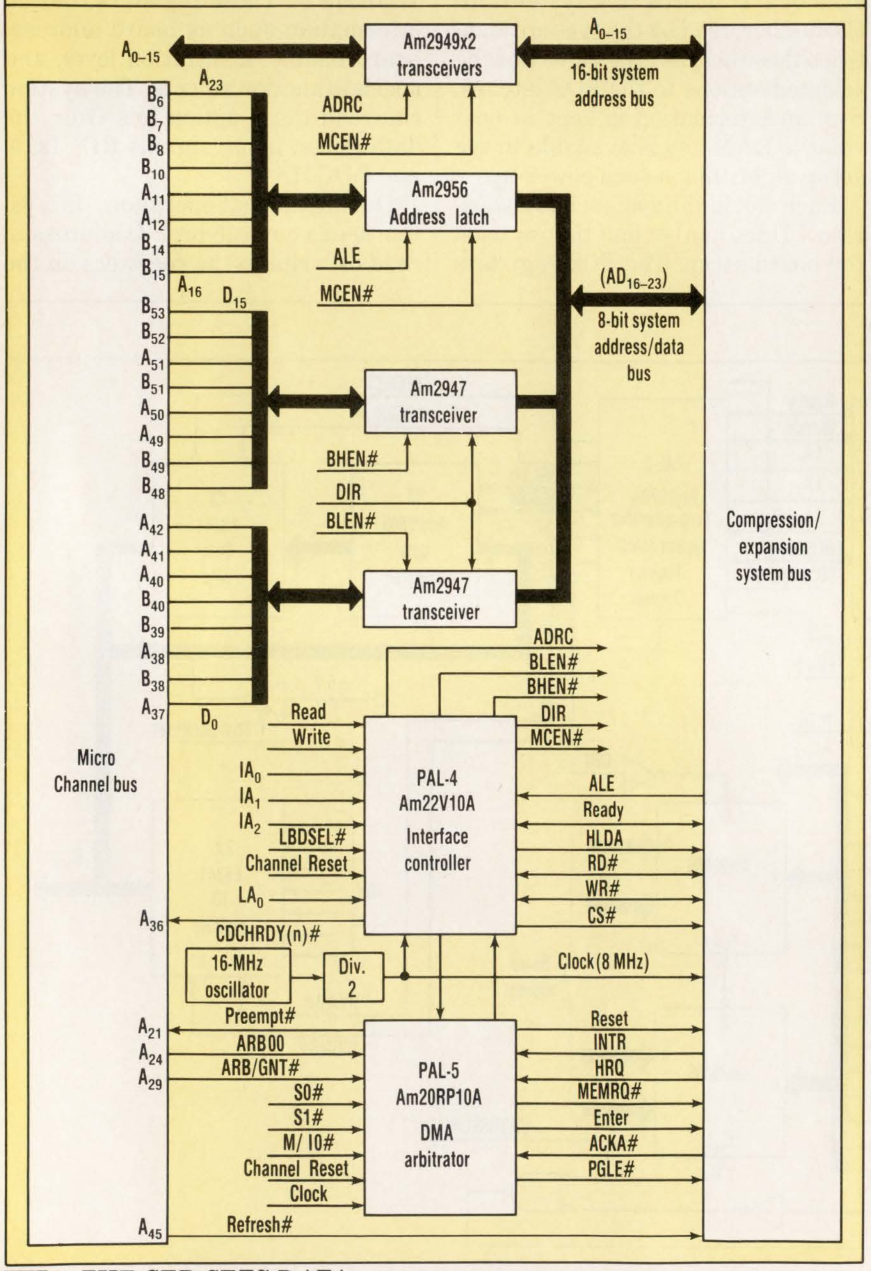
CEP To Micro Channel

PAL-4 provides the timing control, and PAL-5 (Am20RP10A) supplies the DMA-arbitration control for the interface between the Micro Channel, CPU, and document buses. Since the CEP is a 24-bit-address and 8-bit-data device, latches and transceivers are used to access the Micro Channel bus. Two Am2949 devices buffer the bidirectional address lines. The ALE latches 8 address lines when MCEN# enables the data lines on the 8-bit bus. Together they form the 24-bit address for the CEP. The transceivers (Am2947) multiplex the 16 data lines on the 8-bit data bus. BHEN# and BLEN# signals enable these bidirectional buffers, and DIR controls the data direction.

A dual-port access to the document RAM is implemented using buffers and latches. The system and the CEP can share the document memory. ENA# enables a 24-bit system address and 8-bit system data; both are put on the document bus. RD# provides system read/write control. Before the CPU can access the document memory, a page-latch enable (PGLE#) must latch the upper part of the address. Similarly, ENB# enables a 24-bit CEP document address and an 8-bit document data. DRD# issues CEP read and write control. PAL-6 (Am20RP10A) generates the necessary control signals *(Fig. 4)*.

A 1-Mbyte document memory uses

MICRO CHANNEL INTERFACE TO CEP SYSTEM



3. THE CEP GETS DATA from the Micro Channel bus by going through the document memory. The valid-select signals are generated by the PAL devices.

four banks of eight 256-kbyte-by-1-bit DRAM chips, held in check by a DRAM controller (Am2968). This controller supplies the necessary row and column addresses and appropriate control lines. PAL-6 puts in all the control signals needed to implement dual-port access to the DRAM controller.

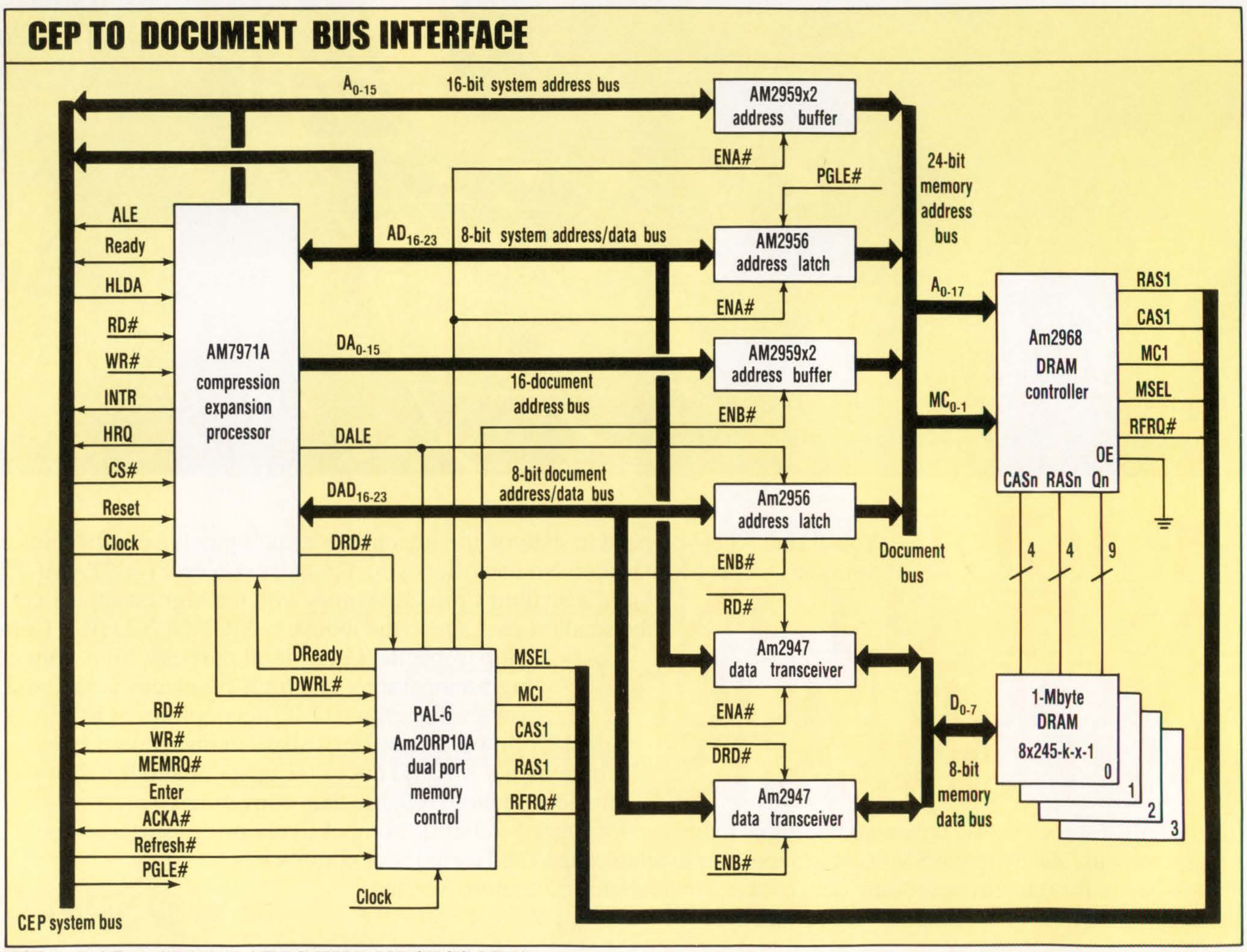
The CEP's 8-bit data bus is multiplexed with the upper eight address lines of the Micro Channel bus, which are latched, in turn, by the ALE to the main-memory bus. RD# and WR# indicate the read and write accesses of the CEP. Any number of wait states can be inserted into a CEP-memory access by keeping the Ready signal low; with no wait states, memory access takes three clock cycles.

The system interface works with a simple arbitration scheme, using signals HRQ (Hold Request) and HLDA (Hold Acknowledge). In the Master mode, HRQ is used when the CEP performs an independent master-DMA access on the system bus. This request is granted by an active HLDA. The CEP performs one memory-access cycle for each bus-arbitration cycle. While the CEP is compressing or expanding a picture, internal registers can be accessed. This is known as the Slave mode.

The CEP has 46 registers for address pointers, parameters, and status information, offering flexibility in memory management and format control. They are initialized before an expansion or compression begins. All registers are directly addressed through lines A1 to A7; data transfer to and from the registers is sent on lines AD16 to AD23.

Since the system interface is used for master-DMA accesses as well as slave accesses to the registers, several control signals are bidirectional. These I/O signals are put in a three-state mode by the CEP when it is not in master mode. The CEP recognizes a register request when the CS# line is activated. CS# is kept low for consecutive slave accesses. After data is available from or successfully written to the registers, the CEP responds by making the Ready line high. It should be noted that Ready can be suppressed between 4 and 20 clock cycles if the CEP is idle and up to 50 clock cycles if it is busy.

If the host CPU aborts the slave-access mode before the CEP responds with an active Ready signal, the CEP ignores the slave access and no register contents are changed. The master-status register supplies the CPU with the current status of



4. PAL-6 GENERATES THE NECESSARY control signals to enable the address buffers and latches.

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CIRCLE 37

the expansion/compression operation. This register is accessible to the CPU without delay (4 clock cycles).

There are two modes the CEP can use to access the system bus. In both, data can be transferred during DMA operation. While the CEP is in idle mode, access to the CEP bus is simple, since no collision is expected. However, when the CEP is busy compressing or expanding data, arbitration, mediated by HRQ and HLDA signals, makes sure that only one device accesses this bus.

The CEP sends a request to the system bus, which asserts a Preempt# signal to the Micro Channel through PAL-5 *(Fig. 3, again)*. The channel then responds by driving the arbitration-grant (ARB/GNT#) line high. During this cycle, the CEP system is at the arbitration level. The changeover is granted by sending the ARB/GNT# line low. The CEP system can now use the bus until the ARB/GNT# signal goes high again. Asserting the HLDA# signal indicates bus acknowledgement to the CEP. Transactions can now proceed without bus contention. A new arbitration cycle is repeated, if necessary. All drivers are disabled, giving the CEP free access to the host memory and I/O devices.

Error Detection

Data is vulnerable to transmission error. When erroneous data is expanded, the resulting image is very different from the original. The CEP checks the expanded line for the number of picture elements within a specified width. If there is a discrepancy, an interrupt alerts the CPU.

The CEP sends an interrupt-request signal (INTR) that is high under special conditions, such as end of operation, buffer overflow, or data error. This action generates a system interrupt. The host CPU then reads the master status register to get the particulars. The interrupt-level selection can be programmed in option-select register bit FUN0. PAL-3 implements this logic.□

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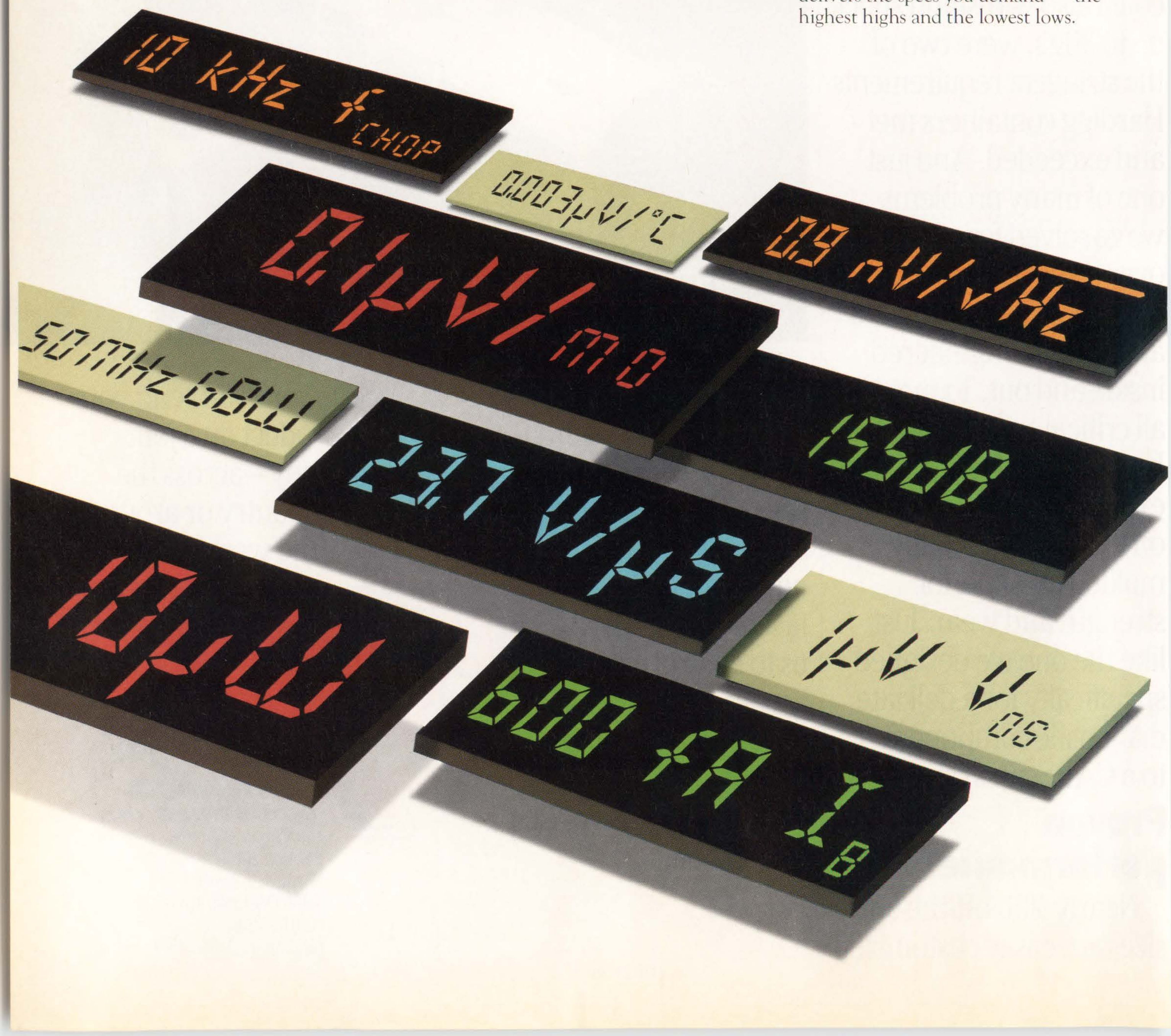

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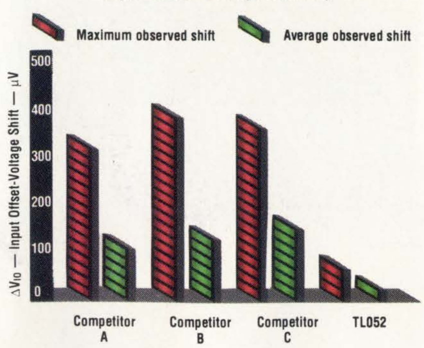

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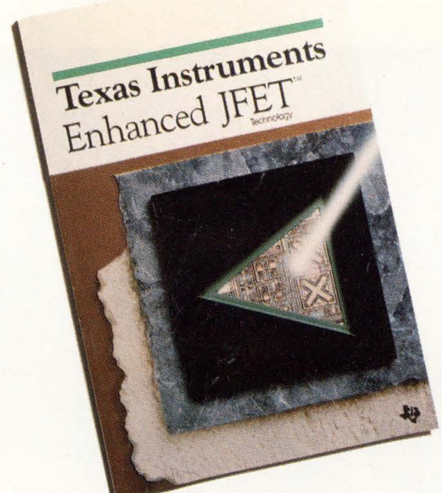

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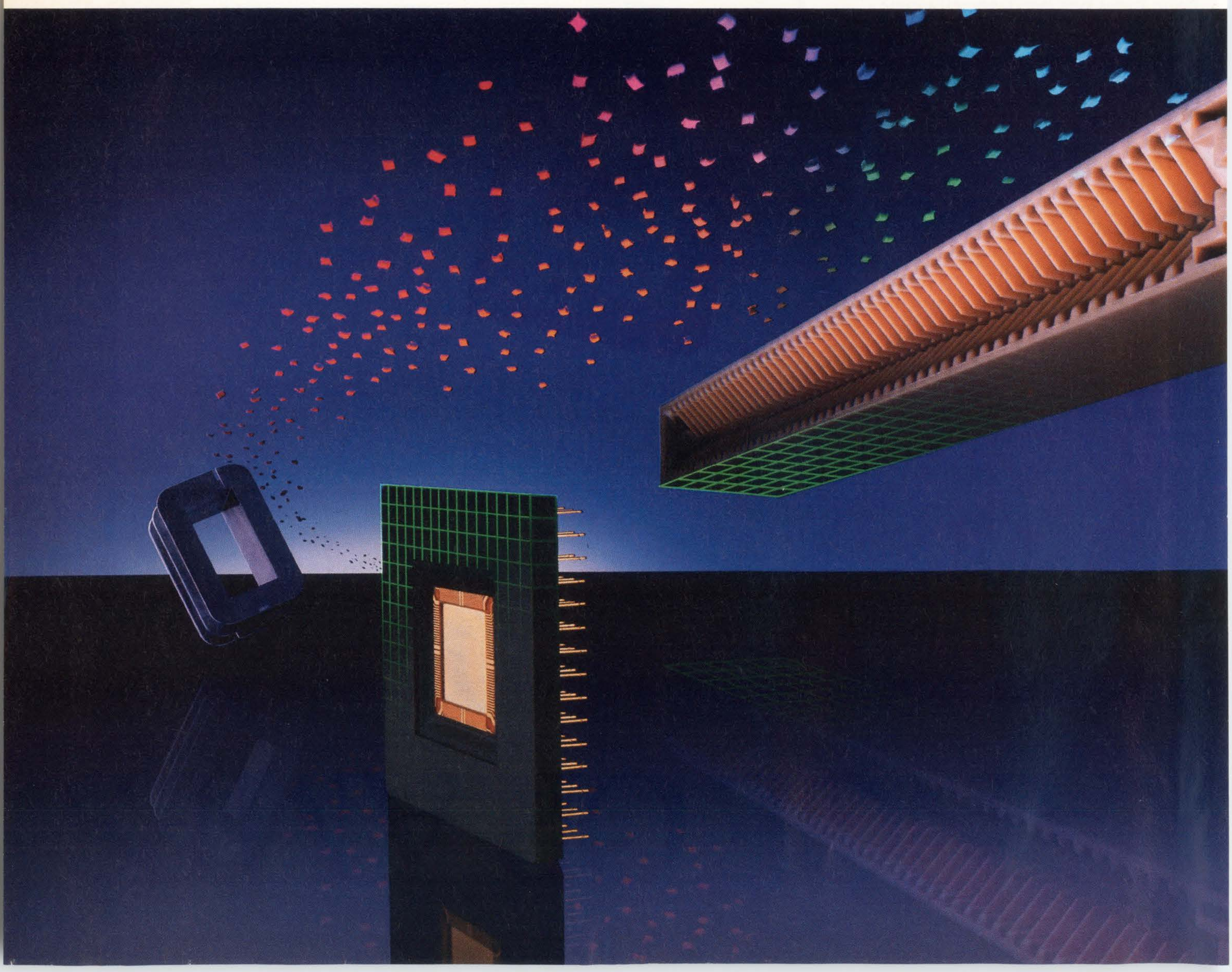

GaAs Cuts Power/Space In Fiber-Optic Networks

Pairing GaAs And CMOS Replaces ECL Decoders And Obtains Data Rates Up To 416 Mbits/s.

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The use of ECL in a fiber-optic data network, such as the 100-Mbit/s Star*Bus, isn't without its problems. Notably, one decoder board alone dissipates 13 W—a high power level for any circuit board for use in a space application where power is crucial. (Star*Bus was developed for space applications for NASA's Goddard Space Flight Center.) Also, the board has the high IC count of 35 ECL chips, and the interconnection scheme for the ECL circuits requires a complex, eight-layer stripline board design.

However, a GaAs LSI array with CMOS logic ICs in this crucial decoder section of the network's bus-interface unit (BIU) cuts power dissipation by about 90% and reduces the IC count to eight. Moreover, the tested speed of the network increases to more than 325 MBits/s, with a theoretically attainable speed of 416 Mbits/s. Accordingly, GaAs processing technology is no longer "five years down the road—and always will be," as the saying goes.

In this GaAs-CMOS circuit, the Transmitter Control block of the BIU subsystem controls the transmission of data packets over the network. The Decoder block receives the packets and stores them for processing by the system's front-end processor *(Fig. 1a)*. The data packet includes a 56-bit preamble, an 8-bit start flag, a 48-bit header, as many as 16,384 bits of data, a 16-bit cyclic-redundancy-check (CRC) error code, and an 8-bit end flag *(Fig. 1b)*. When the network transmits, it stuffs bits into the header, data, and CRC field. Upon receiving the packet, the network strips these inserted bits.

The Decoder block employs two cards: Decoder A and Decoder B. A portion of Decoder A, implemented with GaAs circuits, performs the needed high-speed processing, including flag detection, bit stuffing, CRC verification, and serial-to-parallel conversion *(Fig. 2)*. Decoder B, a CMOS gate array, performs lower-speed, parallel-processing tasks.

Decoder A receives nonreturn-to-zero (NRZ) formatted data from the system. Accordingly, a change to another bit-encoding method (the system presently uses the Manchester format) to minimize clock speeds and optical-receiver and -transceiver bandwidth requirements would not require a decoder redesign. This is noteworthy because the Manchester format has disadvantages at data-transfer rates exceeding 100 Mbit/s.

Inside The Array

The GaAs portion of Decoder A consists of a TQ3000 GaAs gate array. For Decoder A, the TQ3000 directly accepts ECL-level inputs and delivers CMOS-level outputs. This configuration not only reduces the need for ECL-to-CMOS converters, but also eliminates 2.3 W of power from the total circuit (0.4 W in the GaAs array and 1.9 W in external ECL-to-CMOS converters).

This array, on a 160-mil-square die, has a 3000-gate-equivalent capacity with 64 I/O connections for ECL, CMOS, or TTL lines. Its enhancement and depletion-mode FETs use 1-μm gate geometries and two-layer metal interconnects that have a minimum metal pitch of 5.0-μm. The second metal layer is an air bridge supported by posts that also serve as electrical connections. Capacitance of the air bridge is 70 pF/mm, which makes possible clock rates as high as 700 MHz. Each gate dissipates 800 μW plus I/O power—6 mW for the

CMOS outputs.

The array comes in a 132-pin, surface-mounted multilayer-ceramic (MLC) package and is specifically designed for use with the GaAs die. Carrying leads on 25-mil centers, the package measures 0.97 in.^{2}. Transmission-line I/O techniques minimize reflections and optimize rise and fall times. Internal power and ground planes, as well as the provision for on-board high-frequency decoupling capacitors, ensure that the array receives clean voltages.

There are 1088 cells in the array, which divide into two blocks: 1024 core cells surrounded by 64 I/O cells. The core cells, arranged in horizontal pairs, form six 36-pair vertical columns and nine 37-pair vertical columns. The 64 I/O cells inhabit the perimeter of the array, 16 cells to each side of the die. Air-bridge metal forms 19 channels between columns. Two of the channels supply power buses, and the remaining 17 supply conductor routing.

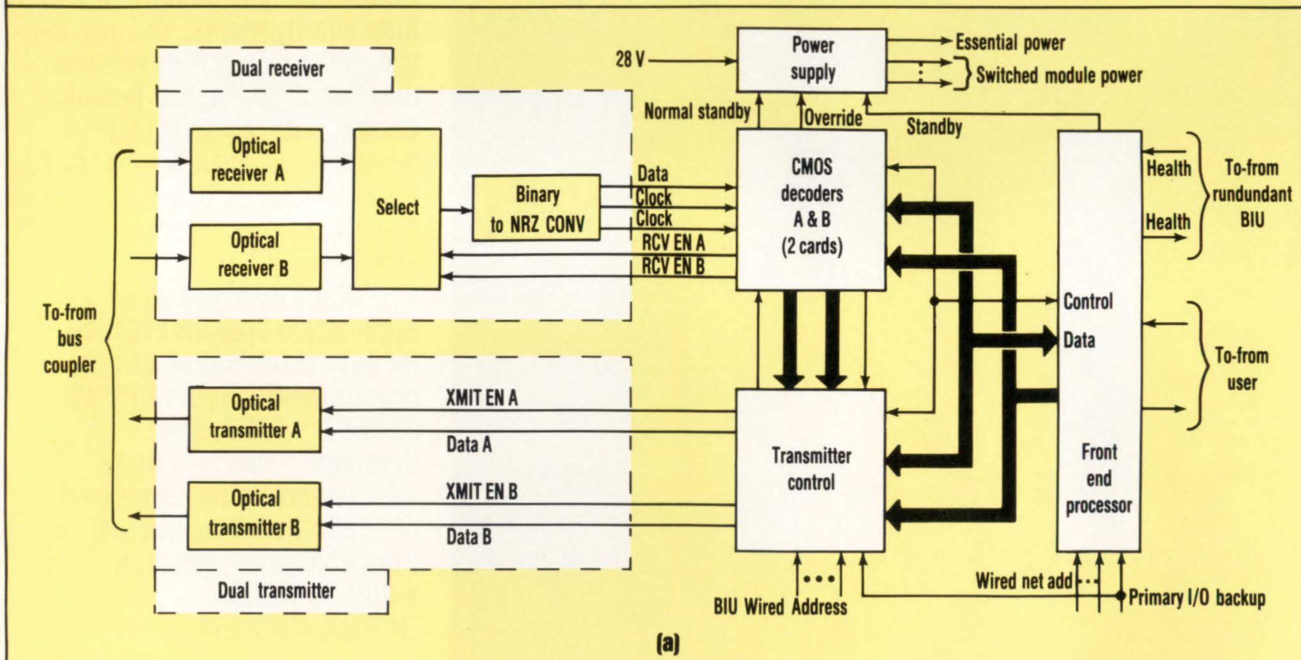
Each cell pair has 14 horizontal channels that serve either as crossovers between vertical routing channels, as macro interconnects, or as I/O-cell access lines. In Decoder A1, the V_{SS} pads in the center of each side supply the –2.6 V needed by the core cells and the ECL inputs. Two of the I/O pads on the perimeter of the chip carry the 5-V supply voltage for the CMOS outputs. Connected to the corner pads and to another four pins on each side, V_{DD} forms the ground line.

The core cells in the array use a buffered-FET-logic (BFL) architecture, optimum for speed, noise margin, and processing yield in GaAs technology. Twelve FETs supply two three-input NOR functions. Each NOR gate includes an enhancement-mode FET driver, a depletion-mode FET load, and an enhancement-mode FET buffer that has a depletion-mode pull-down current source. For each cell assigned a macro function, a diode connects from each NOR-gate pair to V_{SSP}, the internal voltage reference for all cell inputs.

Intercell delays are 41 ps/mm of metal and 19.5 ps/load. These figures result in a NOR-gate (plus cell-to-cell) delay of 120 ps unloaded, and 285 ps with three loads and 3 mm of metal (in this case, 75% of the die width). Note that almost 60% of the loaded delay is attributable to the load and the metal interconnect.

Besides the GaAs array, the decoder A also includes input OR gate, an ECL-to-CMOS level shifter, a –2.6-V regulator, CMOS output buffers, and power-strobe circuitry. The use of power strobing—shutting down power when no data is pre-

STAR*BUS BLOCK DIAGRAM



Preamble	Flag	BIU ADDR	Source BIU	Command control	End destination address	Data	CRC	Flag	Postamble
56	8	8	8	16	16	0 to 16384	16	8	8

(b)

1. IN THE CMOS-GaAs circuit (a), the transmitter control block of the bus-interface unit subsystem controls the transmission of data packets over the network, and the Decoder block receives the packets and stores them for processing by the system's front-end processor. The data packet (b) includes a 56-bit preamble, an 8-bit start flag, a 48-bit header, as many as 16,384 bits of data, a 16-bit cyclic-redundancy-check (CRC) error code, and an 8-bit end flag.

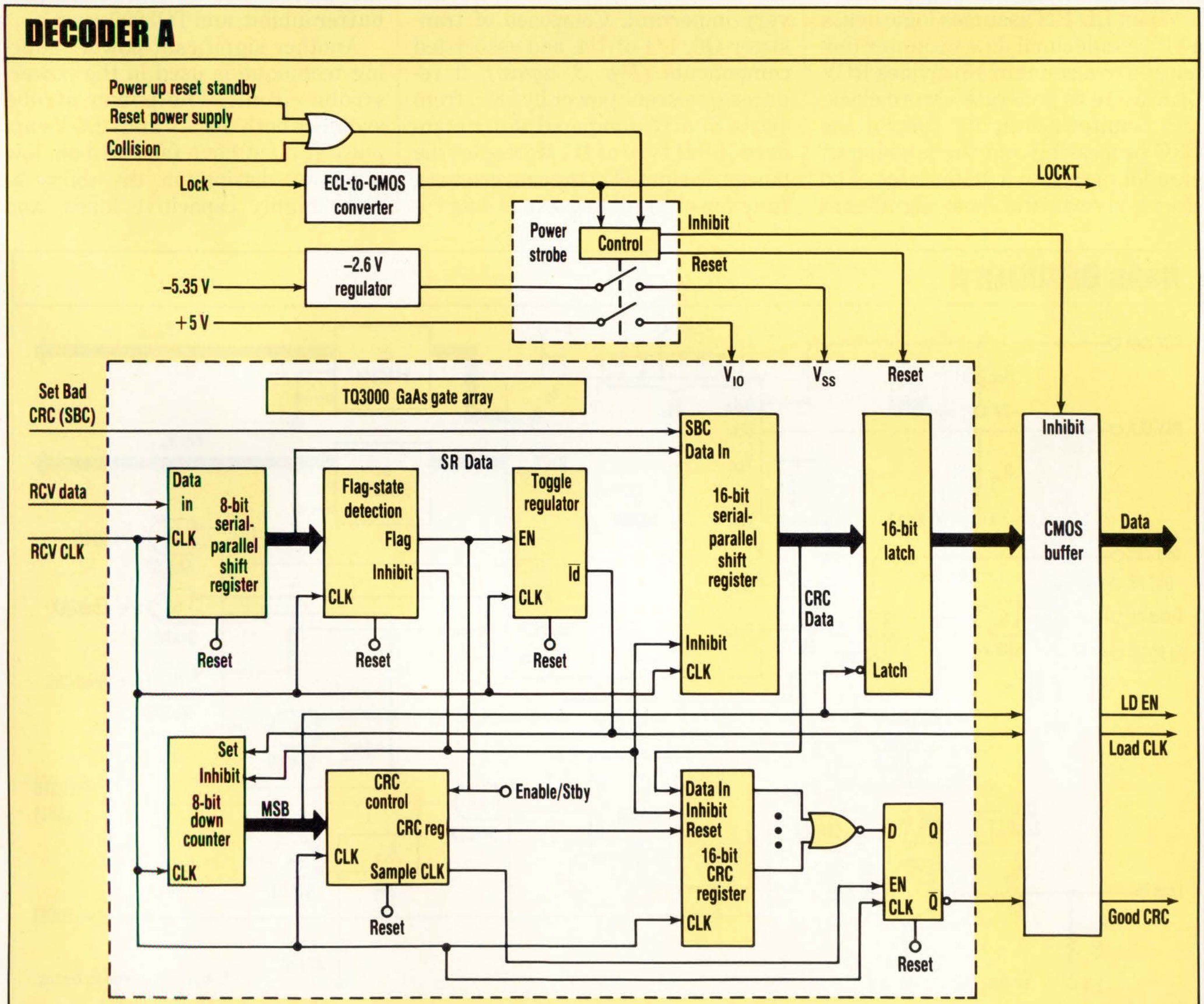
sent—with GaAs technology minimizes power consumption.

To accommodate the GaAs circuitry, the board's new design uses 50-Ω microstrip for high-speed ECL interconnection. It is also designed to minimize inductance in the power-strobe outputs, which eliminates ringing during power-up. A socket for the GaAs array enables one board to serve for chip testing or for insertion in the BIU.

The original 35 ECL ICs in Decoder A required numerous 50-Ω transmission lines, which entailed a complex eight-layer stripline board. The new GaAs decoder only needs a simpler four-layer board: two signal layers, a power plane, and a ground plane. Also, the circuit operates with just three high-speed, ECL-level signals—Lock, RCV Data, and RCV CLK. All other digital signals operate at CMOS levels.

Activating the Lock signal initiates the operation of the Decoder-A card *(Fig. 3)*. Lock is a logic one when optical power is present on the network and a logic zero when no power is present. When the Lock input is logic zero, the power strobe cuts off the V_{SS} and V_{IO} supplies to the TQ3000, minimizing power dissipation. Reset applied to the GaAs array and the CMOS output buffers ensures that the outputs are in a defined state, so spurious operation doesn't occur because of the power-off condition. After a short power-stabilizing delay, the assertion of Lock follows and Reset releases, allowing the reception and processing of data packets.

Under the control of RCV CLK, the packet shifts serially into the TQ3000 array. The array then performs flag detection, bit stripping, CRC-polynomial division and verification, word-clock generation, and serial-to-parallel conversion. The data packet shifts serially into an 8-bit serial-to-parallel shift register. Flag and strip-detection logic monitors the output of the shift register



2. A PORTION OF DECODER A, implemented with GaAs circuits, performs the needed high-speed processing, including flag detection, bit stuffing, CRC verification, and serial-to-parallel conversion.

on a bit-by-bit basis. The logic then looks for two different serial bit patterns. When the circuit detects a 01111110 flag pattern, the Flag signal goes high for one clock period.

Two flags accompany each packet. The first defines the beginning of the packet and sets LD EN to logic one; the second defines the end of the packet, resets LD EN, and samples the CRC result. To prevent a flag's inadvertent presence in the portion of the packet between the legal flags, the transmitter control inserts an extra logic zero into the serial data stream whenever it detects five ones in a row. Using the Strip signal, the TQ3000 then strips these inserted zeros from the incoming packet.

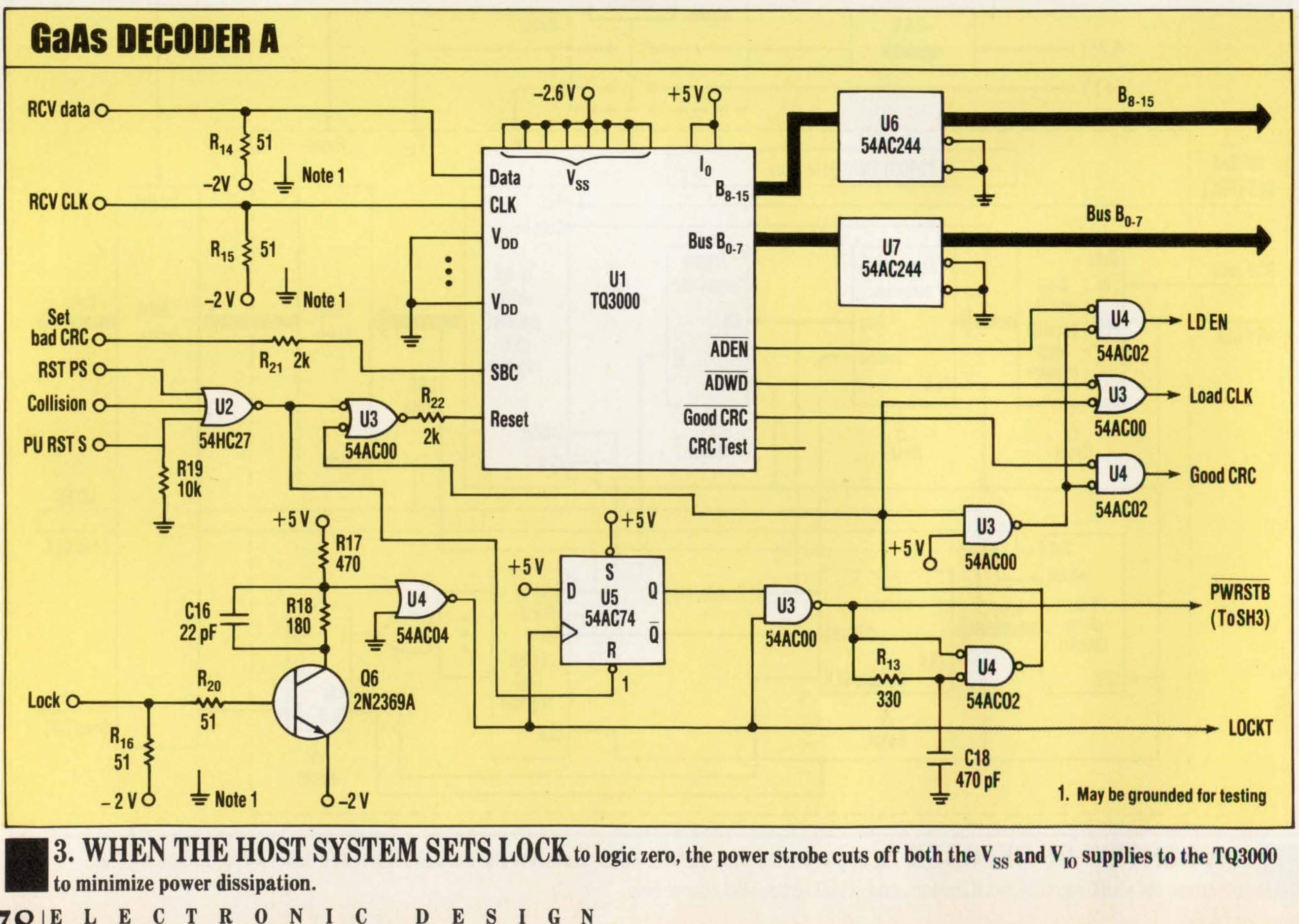
When LD EN assumes logic one, a 4-bit hexadecimal down counter (initialized to a count of 15) divides RCV CLK by 16 to generate a word clock. The counter's outputs control the CRC processing and the latching of parallel data into a 16-bit latch. The circuit inverts the most significant bit to supply the LOAD CLK signal.

CRC processing, implemented serially in the TQ3000 array, uses the standard CRC-CCITT generating polynomial. The transmitter control calculates and appends a 16-bit CRC field to the data polynomial to make it exactly divisible by the generating polynomial. If the division of received data by a CRC register in the TQ3000 array yields no remainder, it's assumed that the data has no errors. In the absence of errors, the CRC register output is all zeros, and the Good-CRC becomes a logic one.

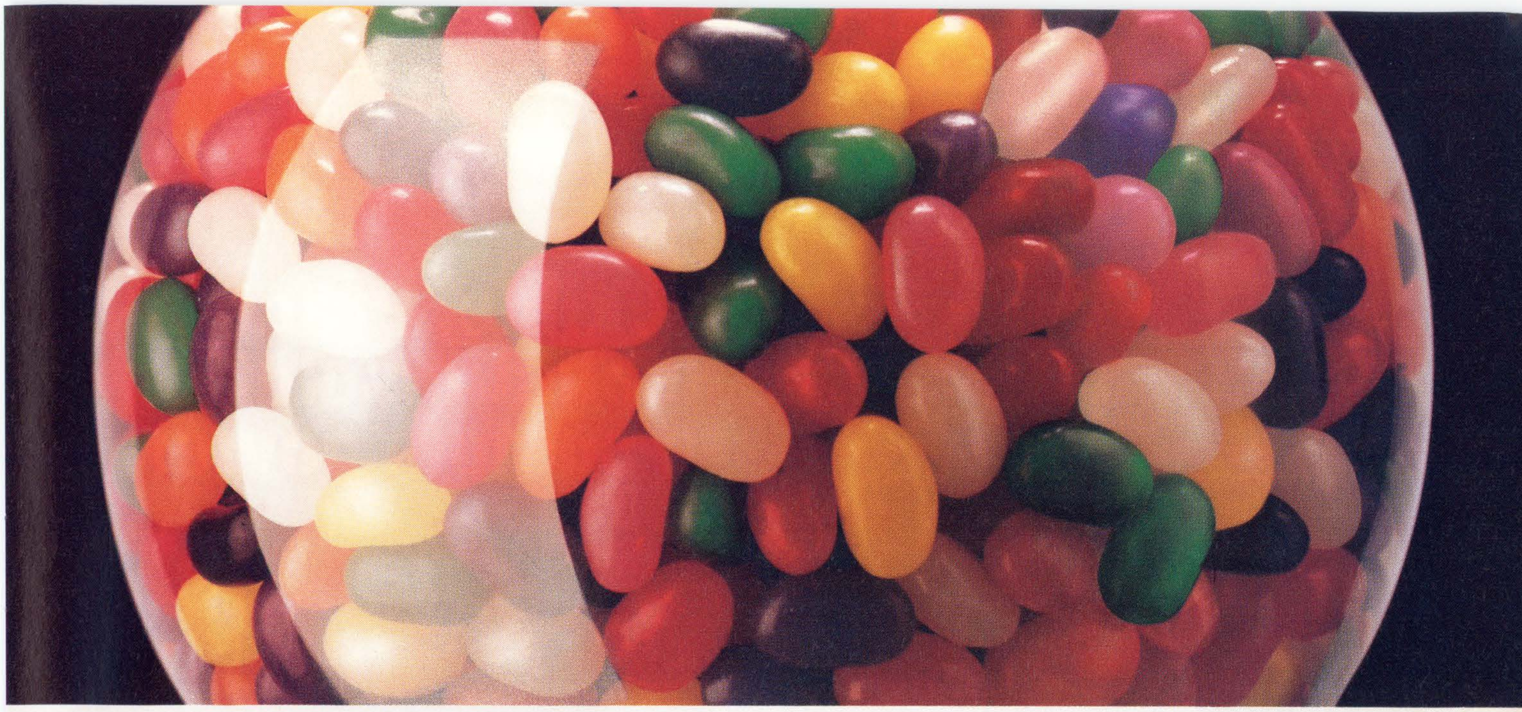
Especially for space applications, the power-reduction techniques in Decoder A, as used in the custom-designed ECL-to-CMOS converter, are very important. Composed of transistor Q6, 1/4 of U4, and associated components *(Fig. 3, again)*, it reduces quiescent power by 78%, from 400 to 87 mW, compared with a standard 10KH type of IC. Moreover, the power dissipated in the converter is a function of the data packet's duty cycle. When Lock is at a logic one, Q6 is off and power dissipation is virtually zero. The V_{BE} of Q6, with the –2-V power supply, defines the –1.3-V ECL input threshold; the V_{BE} of Q6, with the V_{SS} and the R_{17}/R_{18} voltage divider, determines the CMOS low threshold. The 5-V supply defines the high threshold.

The LOCKT signal output from the ECL-to-CMOS converter controls the TQ3000 reset and the inhibit function of the CMOS output buffers. Upon receiving a packet, LOCKT switches high and sets flip-flop U5 to logic one. U5's output, ANDed with LOCKT, generates $\overline{\text{PWR STB}}$, which directly controls the power strobe, CMOS output-buffer inhibit, and TQ3000 reset.

Another significant power reducing technique is used in the power-strobe circuit. The power strobe switches both the 5-V and –2.6-V supplies. It must have fast turn-on, low quiescent dissipation, the ability to drive highly capacitive loads, and



3. WHEN THE HOST SYSTEM SETS LOCK to logic zero, the power strobe cuts off both the V_{SS} and V_{IO} supplies to the TQ3000 to minimize power dissipation.



If this is how you see LEDs, the ad is over.

The popular myth goes something like this: "An LED, is an LED, is an LED." Or: "If you've seen one, you've seen them all." And of course: "LEDs? They're commodity products."

Notions we at Dialight, steadfastly reject. And once you're familiar with our products, you'll know why.

Take our Circuit Board Indicators. Single or multiple discretes aligned in a sturdy plastic housing, complete with their own current limiting resistor. The entire assembly polarity-keyed to guarantee correct insertion.

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All meticulously engineered with the understanding that the failure of a "jelly bean product" can cost thousands in end-user downtime, and who-knows-what in customer loyalty.

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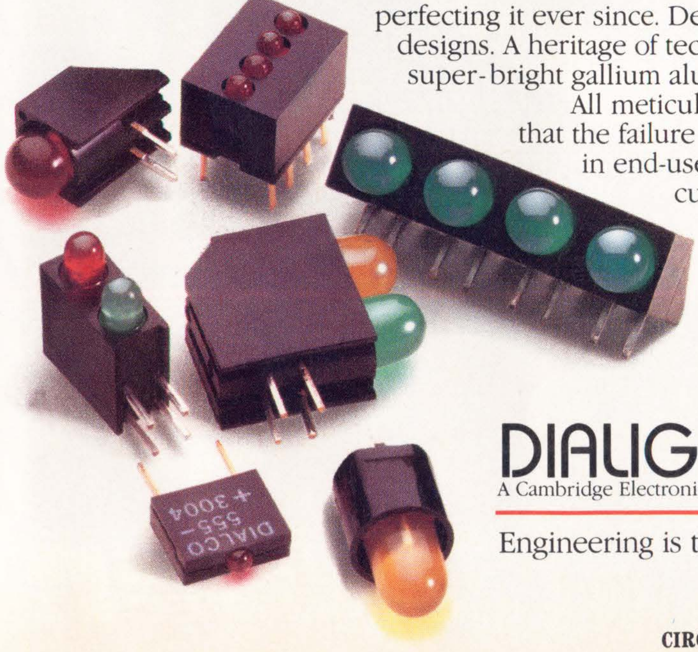

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CIRCLE 43

It seems that every custom power supply project starts with inflexible performance specifications, impractical space limitations, and unrealistic completion schedules.

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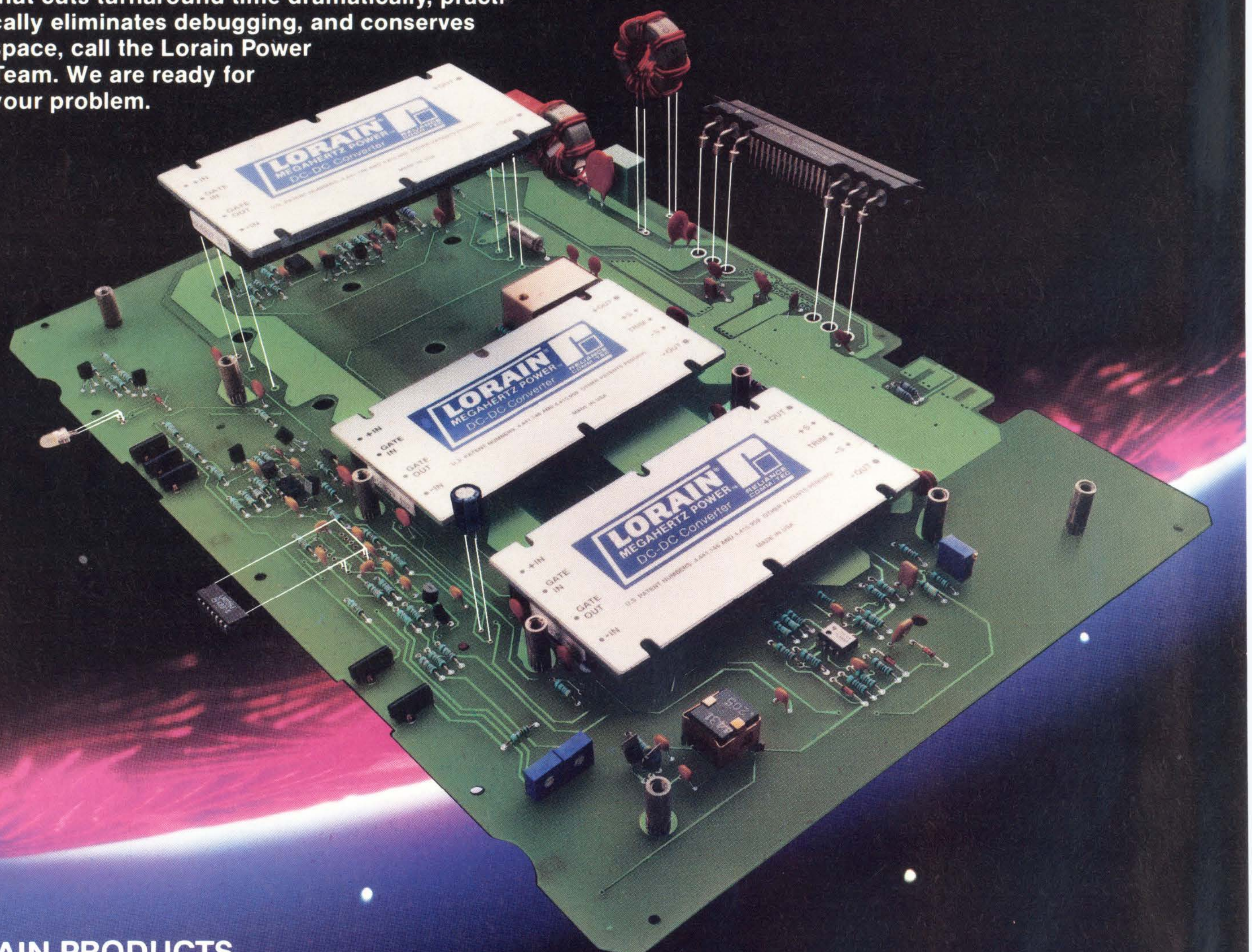

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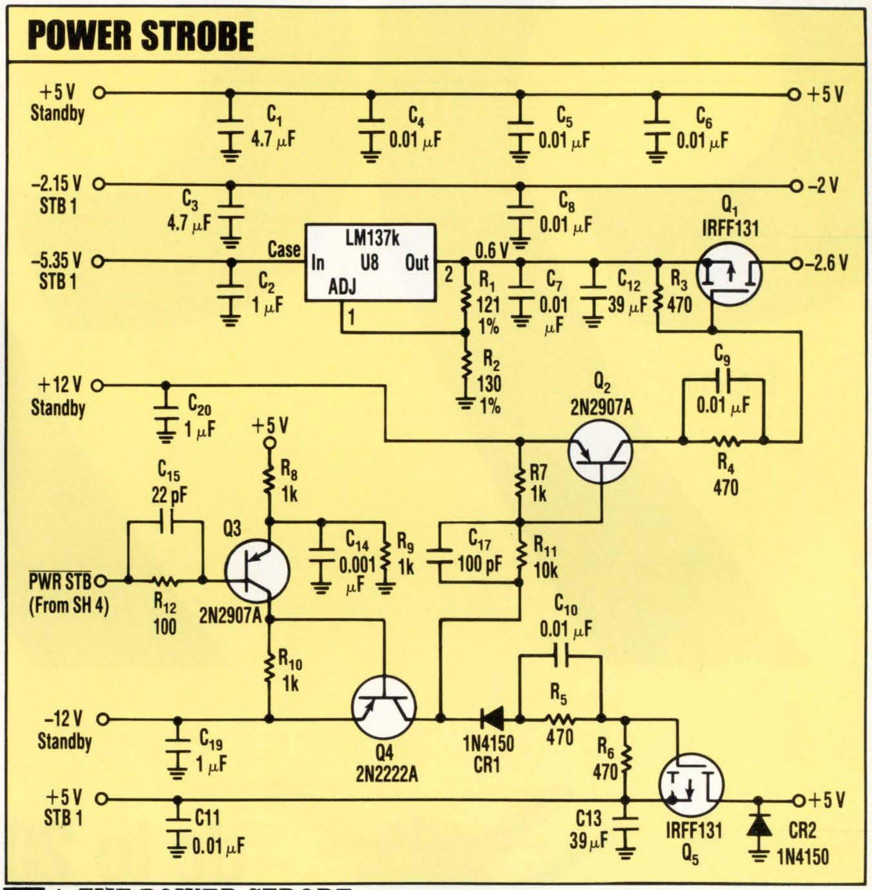
RELIANCE COMM/TEC

CIRCLE 51



4. THE POWER STROBE switches both the 5-V and -2.6-V supplies, based on the power-FET switches Q1 and Q5, and power-dump drivers to supply rapid turn-on.

low active power to ensure that strobing is, indeed, beneficial. Power-FET switches Q1 and Q5 *(Fig. 4)*, using power-dump drivers, supply rapid turn-on.

If Decoder B determines that the packet address is that of another BIU, the circuit asserts RST PS and the power strobe turns off. This feature conserves power if the packet is addressed to another BIU, by requiring the power to be applied only during the first part of the packet (the address header). Power reduction is significant, especially for long packets when the header represents less than 1% of the total packet length.

Because the new Decoder A dissipates so much less power than the ECL-based board, it's questionable whether or not power strobing is worth the effort. Indeed, the power-strobe circuit has a duty-cycle crossover point, beyond which it adds more power than it saves. Fortunately, the maximum operating duty cycle is substantially lower than where power strobing becomes a liability—even in the GaAs version.□

*John DeRuiter, a staff engineer with Honeywell's Satellite Systems Division, is the principal hardware designer of the Star*Bus network. Currently, he is working on a generic VHSIC spaceborn computer (GVSC).*

David Perkins, LSI product engineer at TriQuint, is responsible for customer ASIC development and product management. He earned a BA from Northwest Nazarene College and MSEE from Oregon State University.

HOW VALUABLE?	CIRCLE
HIGHLY	541
MODERATELY	542
SLIGHTLY	543

99¢

from

dc to 2000 MHz amplifier series

SPECIFICATIONS

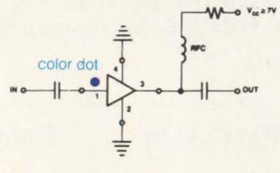
MODEL	FREQ. MHz	GAIN, dB 100 MHz	1000 MHz	2000 MHz	Min. (note)	• MAX. PWR. dBm	NF dB	PRICE $ Ea.	Qty.
MAR-1	DC-1000	18.5	15.5	—	13.0	0	5.0	0.99	(100)
MAR-2	DC-2000	13	12.5	11	8.5	+3	6.5	1.50	(25)
MAR-3	DC-2000	13	12.5	10.5	8.0	+8 □	6.0	1.70	(25)
MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.90	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)
MAR-8	DC-1000	33	23	—	19	+10	3.5	2.20	(25)

NOTE: Minimum gain at highest frequency point and over full temperature range.
• 1dB Gain Compression
□ +4dBm 1 to 2 GHz

designers amplifier kit, DAK-2

5 of each model, total 35 amplifiers

only $59.95



Unbelievable, until now... tiny monolithic wide-band amplifiers for as low as 99 cents. These rugged 0.085 in.diam.,plastic-packaged units are 50ohm* input/output impedance, unconditionally stable regardless of load*, and easily cascadable. Models in the MAR-series offer up to 33 dB gain, 0 to +11dBm output, noise figure as low as 2.8dB, and up to DC-2000MHz bandwidth.

*MAR-8, Input/Output Impedance is not 50ohms, see data sheet. Stable for source/load impedance VSWR less than 3:1

Also, for your design convenience, Mini-Circuits offers chip coupling capacitors at 12 cents each.†

Size (mils)	Tolerance	Temperature Characteristic	Value
80 × 50	5%	NPO	10, 22, 47, 68, 100, 470, 680, 1000 pf
80 × 50	10%	X7R	2200, 4700, 6800, 10,000 pf
120 × 60	10%	X7R	.022, .047. .068, .1µf

† Minimum Order 50 per Value

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CIRCLE 49

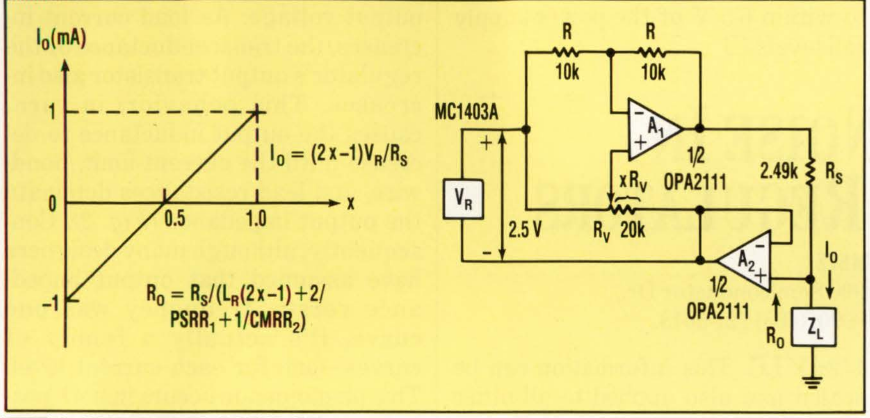
C113-Rev. D

CIRCLE 521

BIPOLAR SOURCE USES UNIPOLAR REFERENCE

JERALD GRAEME
Burr-Brown Corp., International Airport Industrial Pk., P. O. Box 11400, Tucson, AZ 85734; (602) 746-7412.

BIPOLAR REFERENCE SOURCE



A CURRENT SOURCE that has continuous control of the magnitude and polarity of its amplifier gain needs only one voltage reference.

Conventional bipolar current-source circuits have one or more of three general limitations: the need for a variable-polarity voltage reference, the presence of large errors around zero current, and the requirement of a floating load. However, switching the polarity control of the circuit from its reference to its output amplifier's gain directly removes the first limitation and avoids the other two as well.

Changing the polarity of the dc reference source is the more direct means for obtaining a bipolar capability in a current source. But such a conventional approach requires two voltage references. Unfortunately, the two references would supply counteracting effects that are difficult to balance around the zero-current output level. Instead, a current-source circuit that has continuous control of the magnitude and polarity of its output-amplifier gain would need only one voltage reference.

Such an improved current-source circuit includes a reference V_R, a voltage-amplifier circuit A1 with a gain-setting resistor R_S, and a bootstrap follower amplifier A2 *(see the figure)*. The bootstrapping converts the circuit to a current source and allows the load to be grounded. Any voltage developed across the load Z_L feeds back to the reference and voltage amplifier, making their functions immune to that voltage. Then the current-source circuitry floats instead of the load.

To understand how the circuit works, consider both the input and output of voltage follower A2 grounded—zero voltage is convenient for the basic analysis. The grounded input and output points thus share a common potential throughout the voltage-follower action. Now the reference V_R and the gain of the A1 circuit control both the voltage across R_S and the magnitude and polarity of the current in R_S. The result is precise R_S current.

Connecting the voltage reference to both the inverting and noninverting inputs of A1 provides a balanced combination of positive and negative gain. The inverting connection has equal feedback resistors R for a gain of -1, and the noninverting connection varies according to the fractional setting X of potentiometer R_V. Adjusting X controls the noninverting gain and counters the effect of some of the inverting gain. The value of X is the portion of R_V's resistance from the noninverting input of A1 to the temporarily grounded output of A2.

With the output of A2 grounded and X=0, the noninverting connection of A1 has no gain. The net gain V_R receives is the -1 of the inverting connection, and a voltage equal to $-V_R$ develops across sense resistor R_S, which develops an output current of -1 mA when V_R is 2.5 V.

At the other potentiometer extreme, when X=1, V_R connects to the noninverting input part of the A_1 circuit to produce a gain of +2. Combined with the -1 gain of the inverting connection, the result is a net +1 gain. The voltage developed across resistor R_S is equal to $+V_R$ for a +1-mA output to the load.

Between these potentiometer extremes, the current varies with X from -1 mA to +1 mA. The linearity and resolution are determined mostly by potentiometer errors. Simple multiturn potentiometers have errors around 1%; precision versions reduce the errors to about 0.1%. The tolerances and temperature coefficients of the fixed resistors and the voltage reference primarily determine gain errors. With an MC1403A reference and 1% metal-film resistors, the worst-case tolerance error is 4%. Trimming the inverting-gain part of the circuit with a 500-Ω poten-

IFD WINNERS

IFD Winner for November 10, 1988

Kamil Kraus, Ejpovice 96, 337 01 Rokycany, Czechoslavakia. His idea: *"Crossover Networks Are Phase Equalized."*

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tiometer inserted between the two R resistors and connecting the wiper to the –A1 input can reduce the gain error. This adjustment can achieve an error of less than 0.1% before temperature coefficients introduce diminishing returns.

Voltage compliance for a current source defines the range of voltage over which its load can vary without disturbing linear operation. With common-mode and supply-rejection ratios around 100,000 for the OPA2111 dual op amp, and a line regulation of 50 μV/V for the reference, the circuit develops an output resistance of 12,500 × R_S, or 31 MΩ. The result is a negligible 0.032-ppm output error for a full-scale output-current transition. Also, with the 2.5-V reference and the two OPA2111 amplifiers, normal operation is retained to within 6.5 V of the power-supply rail levels.□

CIRCLE 522

Reduce Noise In Voltage Regulators

ERROLL DIETZ
National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 95052-8090; (408) 721-5619.

Simply placing capacitors across the output and the adjust pins of three-terminal regulators is the usual approach to reducing regulator noise. On most regulators, though, the noise voltage over some narrow frequency ranges can peak—even though for typical values of output bypass capacitances, the overall noise voltage over a broad frequency range may drop. Also, the regulator's transient response can experience unexpected effects.

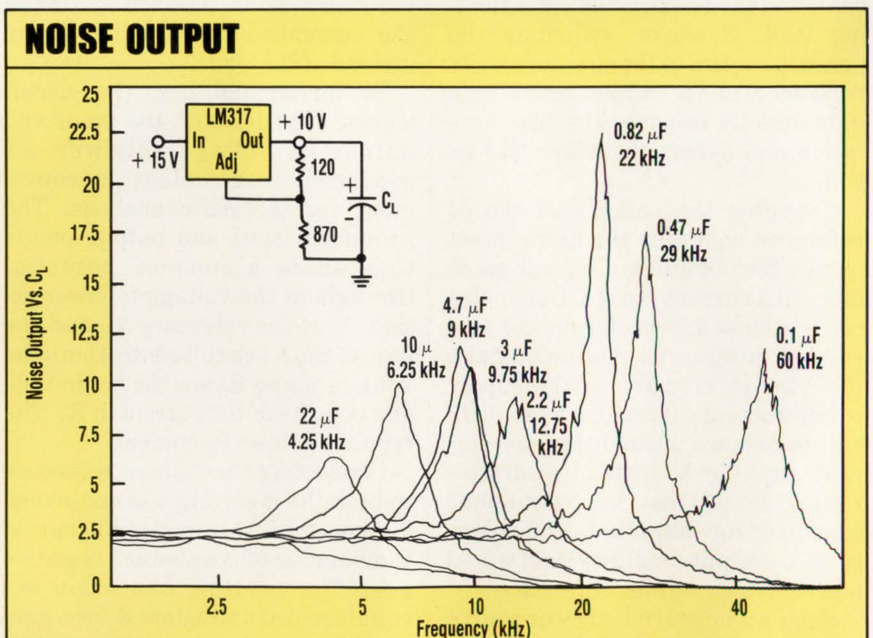
The output impedance of the LM317 voltage regulator, for example, over a 1-kHz to 1-MHz range, is inductive. This is not because of lead inductance, but rather because its internal gain roll-off is 6 dB/octave—just as for an op amp. This characteristic is typically unimportant to average users of IC regulator circuits. But when users shunt this inductive output impedance to ground with a capacitor, the combination can produce a noise peak at the resonant frequency of this inductance and added capacitance *(Fig. 1)*.

For an LM317 with various capacitive loads, the frequency range of the noise spike doesn't extend much above 100 kHz nor below 10 kHz. This is because of ohmic losses in the inductance of the regulator and in the added output capacitance. The frequency is predictable from $1/2\pi\sqrt{LC}$. This information can be scaled and also applied to all other three-terminal voltage regulators.

A noise spike's magnitude depends on the Q of the resonant circuit, which the series resistance of the output capacitor mainly dominates. For instance, a good 1-μF polypropylene capacitor with an equivalent series resistance (ESR) of 20 mΩ at 30 kHz produces a noise peak three times greater than that of the same value of tantalum capacitor with an ESR of 1 to 2 Ω. The noise peak also reflects back to the input of the regulator at about 20-dB down from the output.

A little known fact is that the output impedance of three-terminal regulators varies substantially with load current and the programmed output voltage. As load current increases, the transconductance of the regulator's output transistor also increases. This behavior, in turn, causes the output inductance to decrease until the current-limit, bond-wire, and lead resistances dominate the output impedance *(Fig. 2)*. Consequently, although many designers have assumed that output impedance versus frequency was one curve, it's actually a family of curves—one for each current level. This phenomenon occurs in both positive and negative regulator types (LM117 and LM137), in adjustable and fixed types (LM140 and LM120), and in high- and low-current regulators (LM138 and LM317LZ).

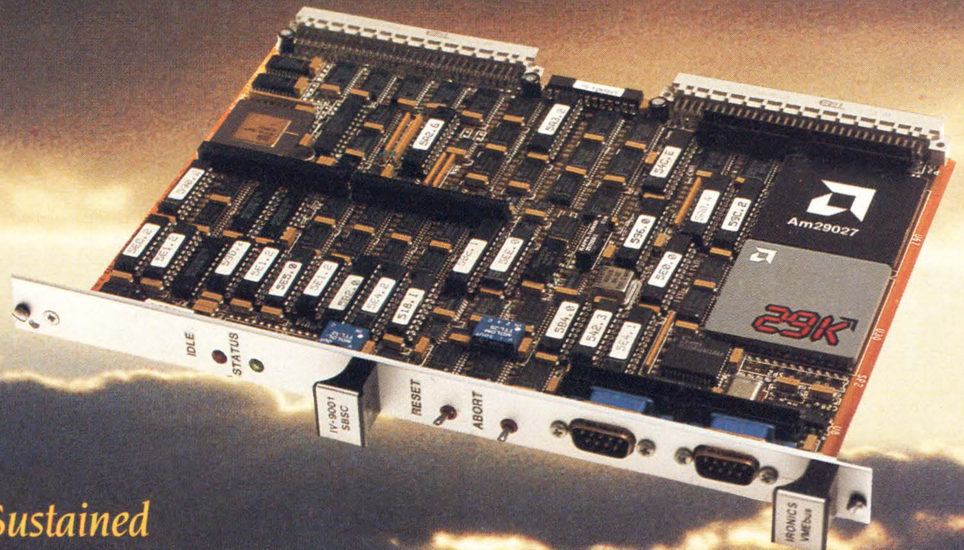
Fortunately, in most cases, several microvolts of power-supply noise peaking at 5 or 10 kHz won't cause problems. But if the application cir-



1. SHUNTING THE INDUCTIVE OUTPUT IMPEDANCE of a three-terminal regulator to ground with a capacitor can produce a noise peak at the resonant frequency of this inductance and added capacitance.

A New Age Is Dawning

Super Computer Performance on a Single Board



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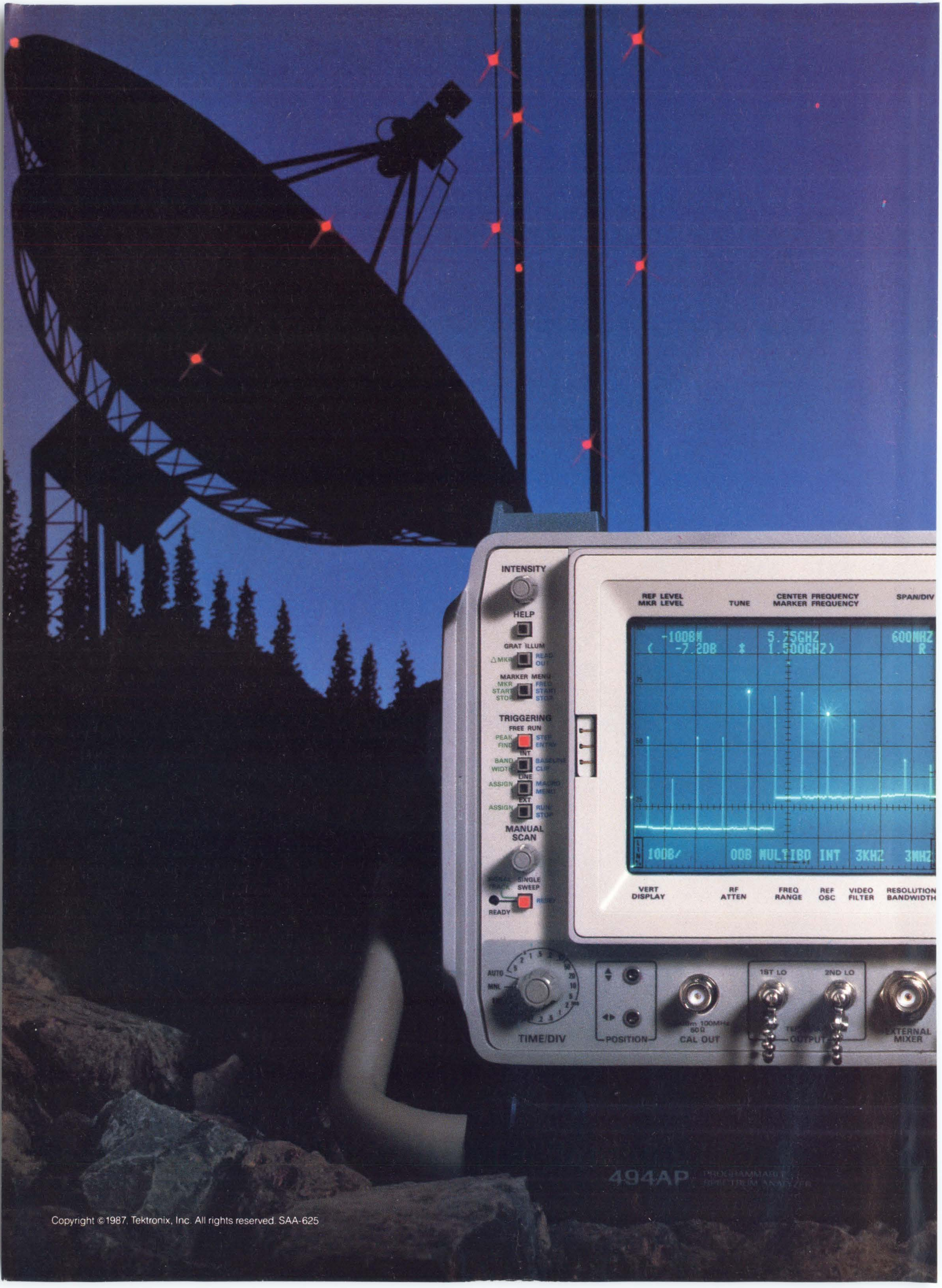
CIRCLE 47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HELP
GRAT ILLUM
MARKER MENU
TRIGGERING
FREE RUN
MANUAL SCAN
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REF LEVEL
MKR LEVEL
TUNE
CENTER FREQUENCY
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-7.2DB
5.75GHZ
1.500GHZ
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10DB/
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CIRCLE 48

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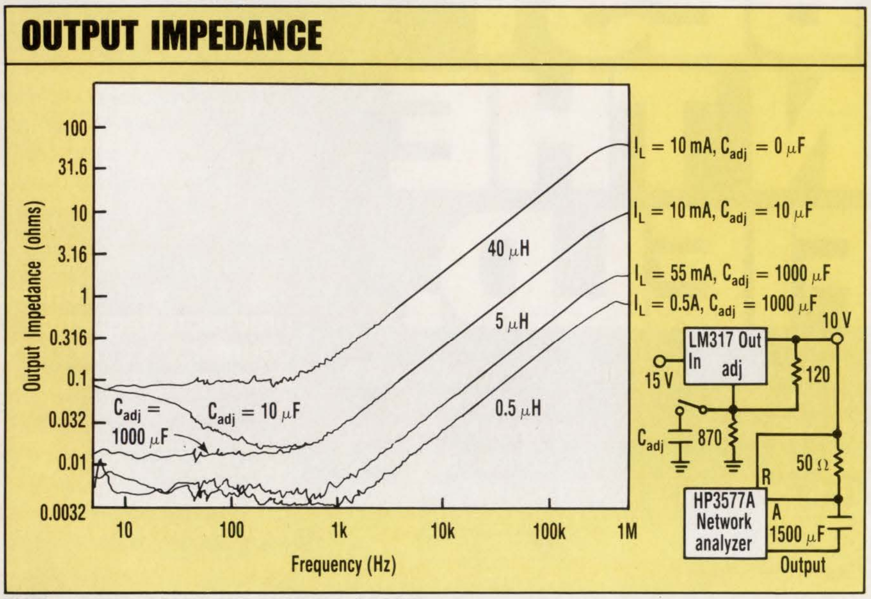


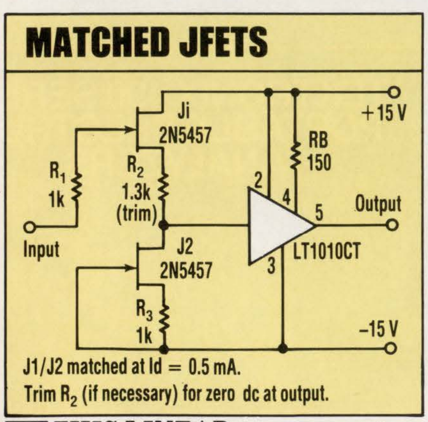
2. THE OUTPUT IMPEDANCE of three-terminal regulators versus frequency forms a family of curves, one for each current level, which changes the output inductance.

cuit is extremely sensitive to excess noise from the supply at a particular frequency, then users can easily engineer the regulator's circuit so that the noise peak falls outside the critical range. Capacitors between 0.1 to 20 μF, especially those with low ESR, should be avoided in low-noise applications. The most effective noise reduction occurs with electrolytic capacitor sizes of 50 μF or greater connected across the output and at least 1 μF connected from the adjust pin to ground.□

CIRCLE 523

Low Distortion Video Buffer

WALT JUNG and RICH MARKELL
Linear Technology Corp., 1630 McCarthy Blvd.,
Milpitas, CA 95035-7487; (408) 432-1900.



THIS LINEAR buffer amplifier's overall harmonic distortion is a low 0.01% or less at 3-Vrms output into a 500-Ω load with no overall feedback.

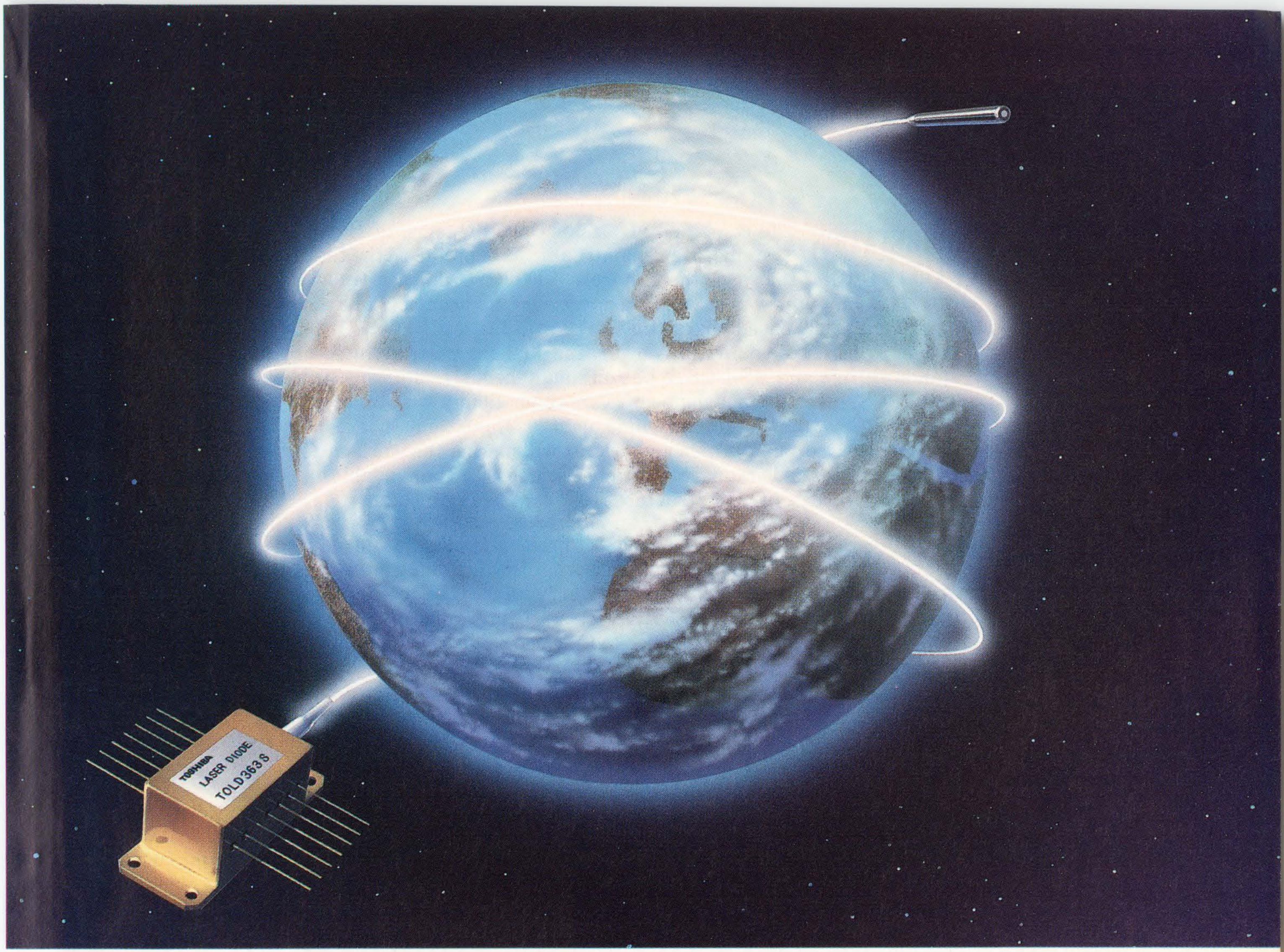
Wideband, unity-gain buffers are utilitarian elements for a broad spectrum of circuits, from dc to video frequencies. To execute a buffer, designers can use various approaches, employing one IC or a complex multitransistor discrete circuit. Of course, designers must typically trade-off in one or more areas, such as in dc offset, speed, linearity, and many other circuit parameters. Nevertheless, a buffer circuit using an LT1010CT video amplifier offers an interesting combination of high performance and relative simplicity.

The amplifier offers a 100-V/μs slew rate, a 20-MHz video bandwidth, and 100 mA of output. It has internal short-circuit protection and is relatively easy to use. For especially high-linearity applications, the amplifier can extend class-A operation by using a fifth biasing terminal. In Sallen-Key unity-gain types of active-filter, or even just for general audio use, this extended linearity can be very important.

One accommodation that designers must make, though, is to cancel the LT1010's nominal dc offset of approximately 60 mV. Also, its input impedance needs boosting. Accordingly, the LT1010 is primarily an inside-the-loop op-amp—not a pure standalone unity-gain buffer. Such accommodations make it possible to exploit the device's high output-drive and linearity virtues, and have a circuit with very high input impedance, low bias current, and low dc offset voltage.

In the circuit, a pair of JFETs, J1 and J2, are preselected for a nominal match at the bias level of the linearized source-follower input stage, at about 0.5 mA *(see the figure)*. The source-bias resistor, R_2, of J1 is somewhat larger than R_3 so that it can drop a larger voltage and cancel the LT1010CT's offset. In use, J1 and J2 provide an untrimmed dc offset of ±50 mV or less. Then swapping J1 and J2 or trimming the R_2 value can give a finer match. If resistors R_2 and R_3 were equal, as in the case of classic form of a zero-offset FET buffer, the LT1010CT's offset in the second-stage would still appear at the circuit's output.

The circuit's overall harmonic distortion is low—0.01% or less at 3-Vrms output into a 500-Ω load with no overall feedback. Even with no overall feedback, the circuit's response to a ±5-V, 10-kHz square wave input, band limited to 1 μs, has no overshoot. If needed, setting bias resistor R_B lower can accommodate even steeper input-signal slopes and drive lower impedance loads with high linearity. The main trade-off for both objectives is more power dissipation. A secondary trade-off is the need for retrimming the source-bias resistor R_2.□



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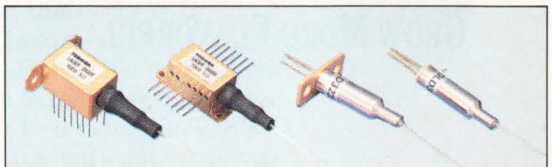

*DFB with Isolator	TOLD333S, TOLD383S
DFB LD	TOLD312S, TOLD313S, TOLD362S, TOLD363S
*Compact Module	TOLD321, TOLD323
Local Loop	TOLD320, TOLD322
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CIRCLE 46

88000-Based Workstation Debuts At UniForum

The combined efforts of Opus Systems, of Cupertino, Calif., and Everex Systems, of Fremont, Calif., have produced the first Unix-based workstation that uses the Motorola 88000 RISC chip set. Opus' Personal Mainframe Series 8000 computer was unveiled last week at UniForum in San Francisco. Opus Systems designed the 88000-based boards that work with Everex Systems' 386-based I/O subsystem to deliver 17 MIPS of computing power. The dual-processor architecture allows both industry-standard Unix and MS-DOS to be run simultaneously. Motorola's binary compatibility standard (BCS) gives this machine software compatibility with other 88000-based products supporting BCS. Other features include up to 20 Mbytes of on-board memory and a high-resolution graphics terminal. Opus and Everex will market the workstation separately. Opus Systems' prices for its Personal Mainframe Series 8000, to be available in the second quarter, start at $9995. Everex's pricing structure is as yet undetermined.LG **CIRCLE 301**

Daisy, Asix Systems Integrate Tools

Asix Systems Corp., of Fremont, Calif., has introduced its ASIX-VIP (verification/integration package), which integrates the ASIX-1 ASIC development/verification system with the CAE tools of Daisy Systems Corp., Mountain View, Calif. Basically, ASIX-VIP is a bidirectional tool set that lets ASIC designers complete all functional checks; look at the operation of a device under various power-supply conditions, input levels, and timings; emulate performance in a system; and check the effects of the manufacturing process range. These tasks can all be accomplished without leaving the Daisy design environment. Information in Daisy's design database is automatically translated into a test sequence for the ASIX-1 system. After the ASIC is tested, results are automatically translated back into the Daisy format.BM **CIRCLE 302**

Development System Gets 80386 Capability

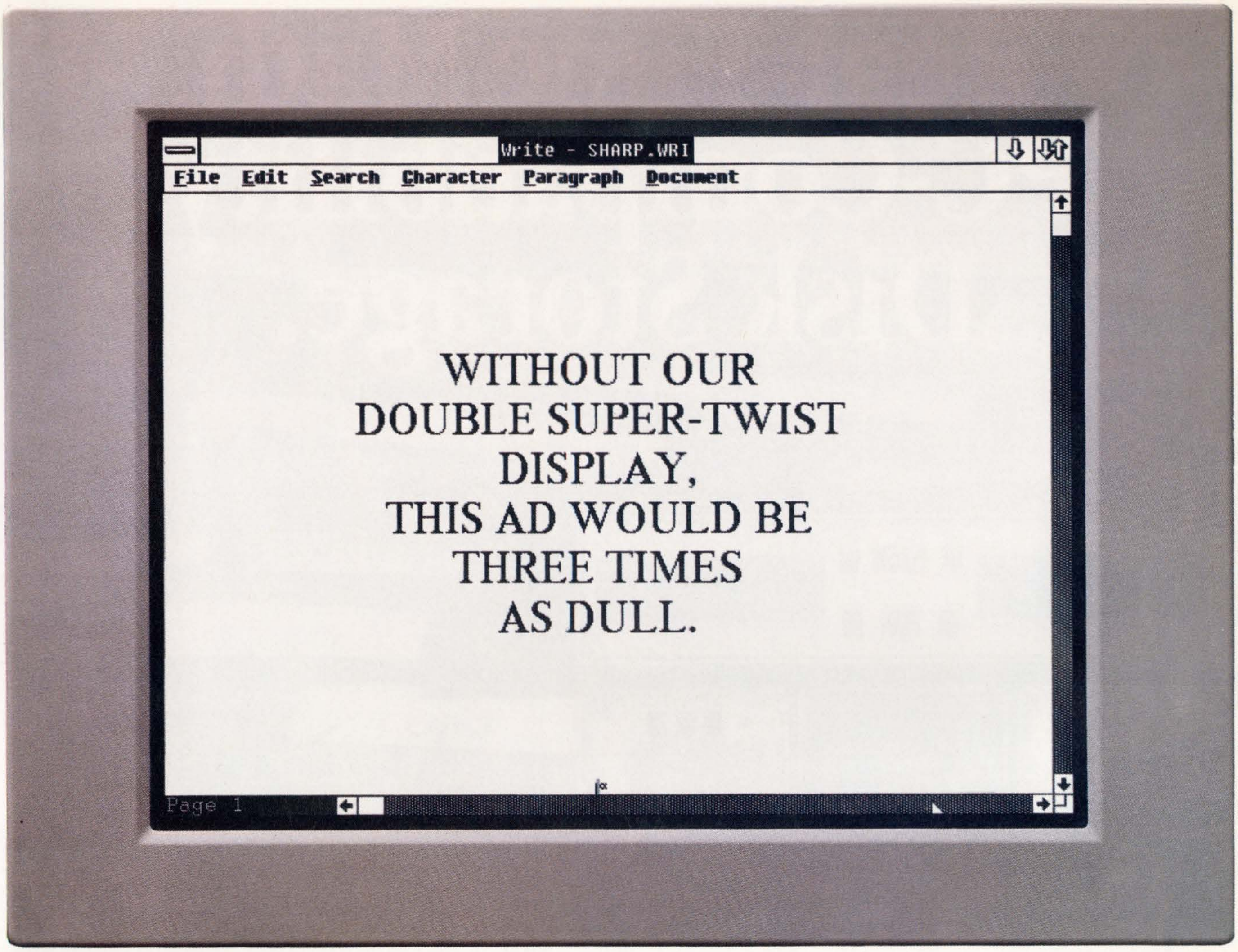
An emulator-analyzer combination adds the Intel 80386 to the list of more than 40 microprocessors served by Hewlett-Packard's HP 64000-UX universal development system. The HP 64420SA/SB emulator subsystem permits real-time execution with no wait states at up to 16 MHz using target or emulation memory. The SA version has 256 kbytes of dual-port emulation memory; the SB model offers 512 kbytes. The memory is mappable over the full 4-Gbyte address range of the 80386 with 256-byte resolution. Other features include single-step (op-code or bus-cycle) run-from and run-until directives; real-time analysis of bus-cycle activity for all address, data, and status lines; disassembly of 80386, 80287, and 80387 instruction sets; a 2048-state trace buffer; and software-performance measurements. The dual-port memory lets the designer display and modify data in emulation memory without halting the microprocessor. The HP 64420SA sells for $33,640, and the HP 64420SB goes for $35,640. Delivery is in two to four weeks.JN **CIRCLE 303**

Qbus-To-SCSI Adapters Grow More Flavorful

Thanks to two new SCSI host adapters from Emulex Corp., of Costa Mesa, Calif., system integrators can draw from about 80 different SCSI-compatible tape and disk drives for use with DEC's MicroVAX II computers. The $1600 UCL-7 single-board adapter and $2000 UCL-8 double-board adapter make the connection between any SCSI board and DEC's MSCP (mass-storage control port) architecture for disk or TMSCP architecture for tape. SCSI-side data rates for both boards are up to 2.9 Mbytes/s (asynchronous) and 4.0 Mbytes/s (synchronous) in the burst mode. The boards handle the full 3-Mbyte/s data rate on the Qbus side. Volume shipments with OEM discounts are scheduled for March.ML **CIRCLE 304**

PC Monitor, Board Aimed At CAE Needs

Directed at the PC-based CAD/CAE-system user, a new color monitor and graphics board from Compaq Computer Corp., of Houston, provides screen-resolution beyond that of VGA monitors. The Advanced Graphics 1024 board delivers 1024-by-768 resolution with 16 colors. An optional Advanced Graphics memory board furnishes 256 simultaneous on-screen colors for displaying shaded 3D renderings and images. Thanks to its Texas Instruments 34010 graphics processor, the 1024 board is five times as fast as a VGA board. The 16-in. color monitor offers precision equal to that of most 19-in. monitors. It displays graphics of 1024-by-768 resolution or full-screen 640-by-480 VGA resolution. The monitor uses signal pass-through from the VGA controller to display existing software on the entire screen. Prices for the Advanced Graphics monitor, 1024 board, and optional memory board are $1999, $1499, and $599, respectively.LG **CIRCLE 305**



If it weren't for Sharp's new technology, chances are you'd still be trying to read the headline above. That's because our display screen offers unsurpassed brightness and clarity, with three times the contrast of conventional LCDs. Along with an increased viewing angle, our double super-twist display provides an image quality which approaches that of a printed page.

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SHARP'S DOUBLE SUPER-TWIST DISPLAYS				
MODEL #	DOT FORMAT	OUTLINE DIMENSIONS WxHxD (mm)	VIEWING AREA WxH (mm)	DOT SIZE WxH
LM24010Z	240x128	176x96x22	134x76	0.49x0.49
LM64135Z	640x400	300x166x26	218x139	0.30x0.30
LM64148Z	640x480	280x180x25.5	205x155	0.28x0.28
LM64048Z	640x480	310x240x25	237x180	0.33x0.33
LM72060Z	720x400	320.4x170.4x34	260x147	0.32x0.32

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CIRCLE 50

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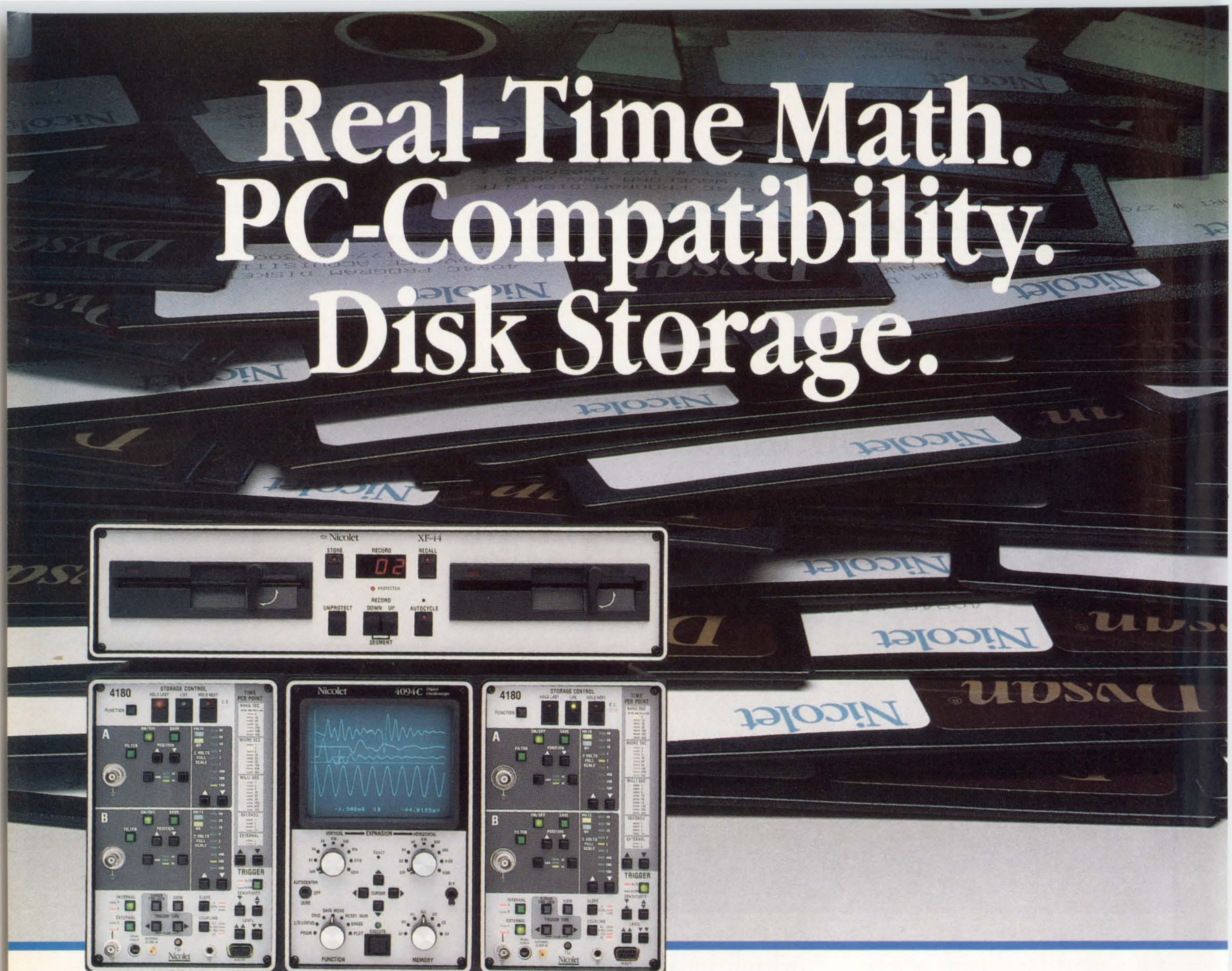

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INSTRUMENTS OF DISCOVERY

FOR MORE INFORMATION CIRCLE 44

BOARD LINKS VME HOSTS TO MILITARY COMPUTERS

AN OFF-THE-SHELF INTERFACE CONTROLLER CUTS DESIGN TIME AND COSTS OF VMEBUS COMPUTERS AND PERIPHERALS.

MILT LEONARD

An intelligent I/O VMEbus controller board from Rockwell International implements MIL-STD-1397A and Naval Tactical Data Systems (NTDS) protocols to ease the way toward using the bus in military applications. Thus far, implementing the VMEbus in equipment for military use has been anything but easy. One reason: U.S. Navy equipment must comply with MIL-STD-1397A, a de facto standard that defines the NTDS port. The standard specifies the protocols, driver and receiver circuits, and transmission-cable characteristics necessary for communication between different types of digital equipment from various vendors. To make matters worse, a Department of Defense mandate requires military systems to use standard components wherever possible to cut development time and cost. Both requirements impose tough challenges for any interface design—let alone the VMEbus.

Rockwell International's Intelligent I/O Controller (IIOC) board rises to the occasion, implementing MIL-STD-1397A, while complying with the Department of Defense mandate. The IIOC employs NTDS protocols, allowing designers of VMEbus-based equipment to include NTDS ports for communicating with standard Navy peripherals and computers without resorting to custom designs. The IIOC can be software configured to make its host act as a computer, a peripheral, or as a data-transfer device between computers.

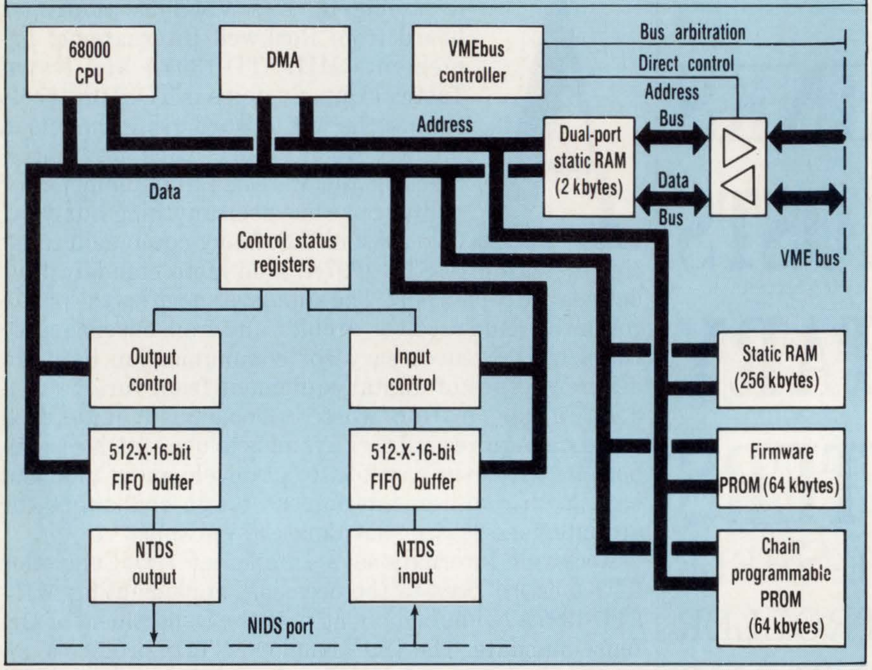
Electronic equipment built around the VMEbus presents an ideal platform for military applications. With its low-cost, high-performance open architecture that can link myriad devices with unusual bus interfaces, the VMEbus lets system designers draw from a broad selection of CPUs, memories, and peripherals. The bus also gives them the choice of special-purpose circuit cards for analog, control, and signal-processing functions. What's more, AT&T's Unix and Ada programming languages are ported to many VME CPUs, widening the selection of application software.

The controller architecture comprises 83 surface-mounted standard ICs and 40 discrete passive components configured for a high degree of user programmability *(see the figure)*. Controller intelligence is concentrated in a 10-MHz 68000 microprocessor, a 68450 DMA controller, and a 68172 VMEbus controller. Also on board are 256 kbytes of static RAM, 2 kbytes of dual-ported static RAM tied directly to the VMEbus, and 64 kbytes of EPROM.

The static RAM stores long command sequences and data strings. Rockwell's Mini-MOS operating system, which provides user-programmability for data handling and VME command-chain processing, is stored in the EPROM. The board has empty sockets for an additional 64 kbytes of EPROM for user-specified command chains. With a programmable configuration register, the controller works with 16- or 32-bit NTDS words and 16-bit

INTELLIGENT I/O CONTROLLER

VME-NTDS INTERFACE



AT THE HEART of Rockwell International's Intelligent I/O Controller are a 10-MHz 68000 CPU, a 68450 DMA controller, and a 68172 VMEbus controller. These combine to control data flow between NTDS input and output ports and the VMEbus. VMEbus-based equipment with NTDS ports can communicate with standard Navy computers.

VME words. Two VME interrupt vectors are also programmable.

The controller interfaces with NTDS equipment through an input and an output NTDS port, each connected to registers and FIFO memories. This architecture supplies each port with full-duplex operation for simultaneous data transmission and reception, up to the maximum NTDS data-transfer rate of 250 kwords/s. Each NTDS port is also associated with a programmable timer to allow user-specified time-out values for data transfers.

The VME system communicates with the IIOC by first loading a command chain into the dual-ported static RAM. The system then interrupts the board by writing an Execute Chain command to the appropriate VME mailbox location in the dual-ported static RAM. A command chain can be one command or several commands linked together. The microprocessor interprets these commands and sets up parameters in the control status registers for controlling the data that's moving between the VME and NTDS ports. The processor is now available for other tasks within the IIOC, and no further VME host intervention is necessary.

Each command block in a chain has several fields that specify the type of command to be executed, the address and word count, optional time-out value, a pointer indicating where the command status should be left, and a pointer to the next command in the chain. A parameter field specifies whether an interrupt should be generated upon completion or time-out, and which of the two VME interrupt vectors to use. The data source or destination can be host memory or local RAM on the IIOC.

The controller performs all NTDS data transfers, including forced functions, forced interrupts, and the full set of 16-bit VMEbus protocols (forced functions and interrupts are essentially priority commands from the host CPU). Besides NTDS I/O commands, Rockwell included commands that users can call to manipulate data fields for bit-masking and setting, logical operations, rotating and shifting, moving, comparison, and conditional jumps. With another command, users can call an application-specific subroutine, and can define custom commands not implemented in the IIOC instruction set.

Another command activates a self-test routine stored in the EPROM. This test is also executed whenever the SYS Reset VMEbus signal is detected or at the command of a reset switch mounted on the board.

Interface adapter modules, which plug into the IIOC motherboard, supply the data rates, voltage levels, drivers, and receivers required for specific NTDS port configurations, which are designated as Fast, Slow, and Anew. To maintain data integrity, even with long cable runs, differential receivers are used in the Fast and Anew modes, in compliance with MIL-STD-1397A.

Rockwell packed these functions onto a 6.375-by-9.25-in. multilayered motherboard with standard VME form-factor, card-cage, and connector configurations. The board fits a double-height VMEbus slot. Two VMEbus connectors and two NTDS port connectors are mounted on the board. The company is also developing ruggedized versions that will meet full military-temperature, shock and vibration, screening, and burn-in requirements. With these versions, users will carry one hardware and software design—from prototype through deployable equipment—for use in military systems.□

PRICE AND AVAILABILITY

The IIOC is priced at $5400 each, with OEM discounts available. Delivery is 30 days after receipt of order.

Rockwell International Corp., Interface Products Group, Autonetics Marine Systems Div., 3370 Miraloma Ave., Anaheim, CA 92803; (714) 762-1476. **CIRCLE 513**

HOW VALUABLE?	**CIRCLE**
HIGHLY	553
MODERATELY	554
SLIGHTLY	555

Vision System's Pad-To-Pad Matching Compensates For Bent Package Leads On Surface-Mounted ICs.

Software Puts Fine-Pitch Packages On Target

Jerry Lyman

A set of vision-software tools from Cognex aims at bull's-eye placement of fine-pitch, surface-mounted IC packages to matching pc-board pad patterns. The surface-mounted device (SMD) software also makes it possible to inspect the straightness of component leads. The software, plus the Cognex vision system, calculates the amount of error between ideal and actual lead patterns by finding the exact position of each lead. This information yields a unique benefit: the ability to correctly place fine-pitch IC packages with bent leads.

Other vision systems either reject units with bent leads or place them incorrectly. With the new software, Cognex vision systems can make the best match between the component's leads and corresponding pc-board pads. Furthermore, the tools adjust part placement so that bent leads make proper contact with their pads, while maintaining adequate coverage for other leads.

The software's advanced gray-scale image processing factors out changes in illumination that can interfere with performance. High-speed edge-finding algorithms allow the processor to locate each lead on the device before determining device position. This approach makes it possible to quickly and accurately place even devices with slightly bent leads.

The SMD tools are compatible with any Cognex one-board system and work with surface-mounted IC packages. The software/hardware combination particularly suits the new plastic quad flatpacks with lead pitches of 30 to 15 mils. These are hard to place and extremely susceptible to lead bending.

The SMD vision software consists of several modules that can be called from within a developer's C-language application program. The tools give the developer the flexibility to set new module parameters, replace modules, or add new modules to suit specific needs.

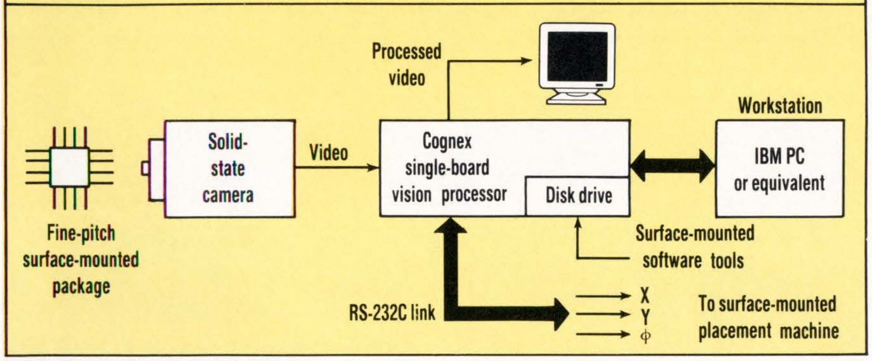
The present set of modules break down into setup or run-time functions. Setup functions give vision-system information about the optical configuration being used, such as magnification, camera field of view, camera alignment, and about the components that will be presented to the vision system.

An optical calibration module is one of the setup functions. It converts the vision system's pixel units into real-world units, so that the vision system can accept part descriptions and report results in real-world units. It also provides a basis for correcting camera nonlinearities. So the accuracy of the results doesn't depend on a perfect optical configuration.

Another setup module, the component training module, is critically important. It lets users describe each component type and its placement-site pad configuration to the system. Input to the module consists of parametric data, expressed in physical units such as number of leads, lead size and spacing, and so forth. No actual images of the components must be stored. With this module a library of thousands of component types can be built up.

SURFACE-MOUNTED PLACEMENT SOFTWARE

VISION SYSTEM FOR FINE-PITCH PACKAGES



USING AN IBM PC or compatible workstation, storage-module-device software tools allow a Cognex one-board vision system to produce xy and θ corrections to accurately match a fine-pitch package's leads to corresponding pads, even with bent leads.

After the setup functions are exercised, run-time functions, consisting of image-aquisition, part-location, lead-location, pad-to-pad matching, and reporting modules, are applied. The run-time functions return an xyθ correction that can be used to correctly place the packaged device on its corresponding solder pads. The functions also calculate values that can be used to reject parts with bent leads.

The image-acquisition module lets the system capture an appropriate image of a part. The next vision task is to find the part and its leads. The part-locating module determines the approximate xyθ position of the part under inspection to predict the lead positions. Then the lead-locating module determines the exact position of each lead.

Many vision systems stop at this point, using a weighted average of lead positions to guide SMD placement. The disadvantage of this technique is that a few bent leads will not significantly alter the results. Consequently, components may be placed so that bent leads don't achieve adequate pad coverage and may bridge adjacent pads. Alternatively, components with bent leads may be rejected as unplaceable.

The Cognex pad-to-pad matching module solves this problem by determining the part position that optimizes coverage for all leads, including bent ones. The module allows the part position to be adjusted so that bent leads are pulled onto their pads without sacrificing proper coverage by other leads. The developer can set thresholds for how far leads can be bent before the vision system will classify the device as a reject.

Lastly, the reporting module gives the xyθ correction a user's pick-and-place machine needs to correctly place packages in machine-compatible units. Users can obtain this information over an RS-232 link *(see the figure)*. They can also obtain raw data on lead and pad positions to create alternative part-to-pad matching algorithms.

For fine-pitch devices, the computed move will be accurate within at least ±1/2 mil. A sample cycle time for a 132-lead quad flatpack with leads on 25-mil centers—including image acquisition, vision processing, calculations, reporting, and other functions—is 500 ms on a Cognex 2000 vision processor.□

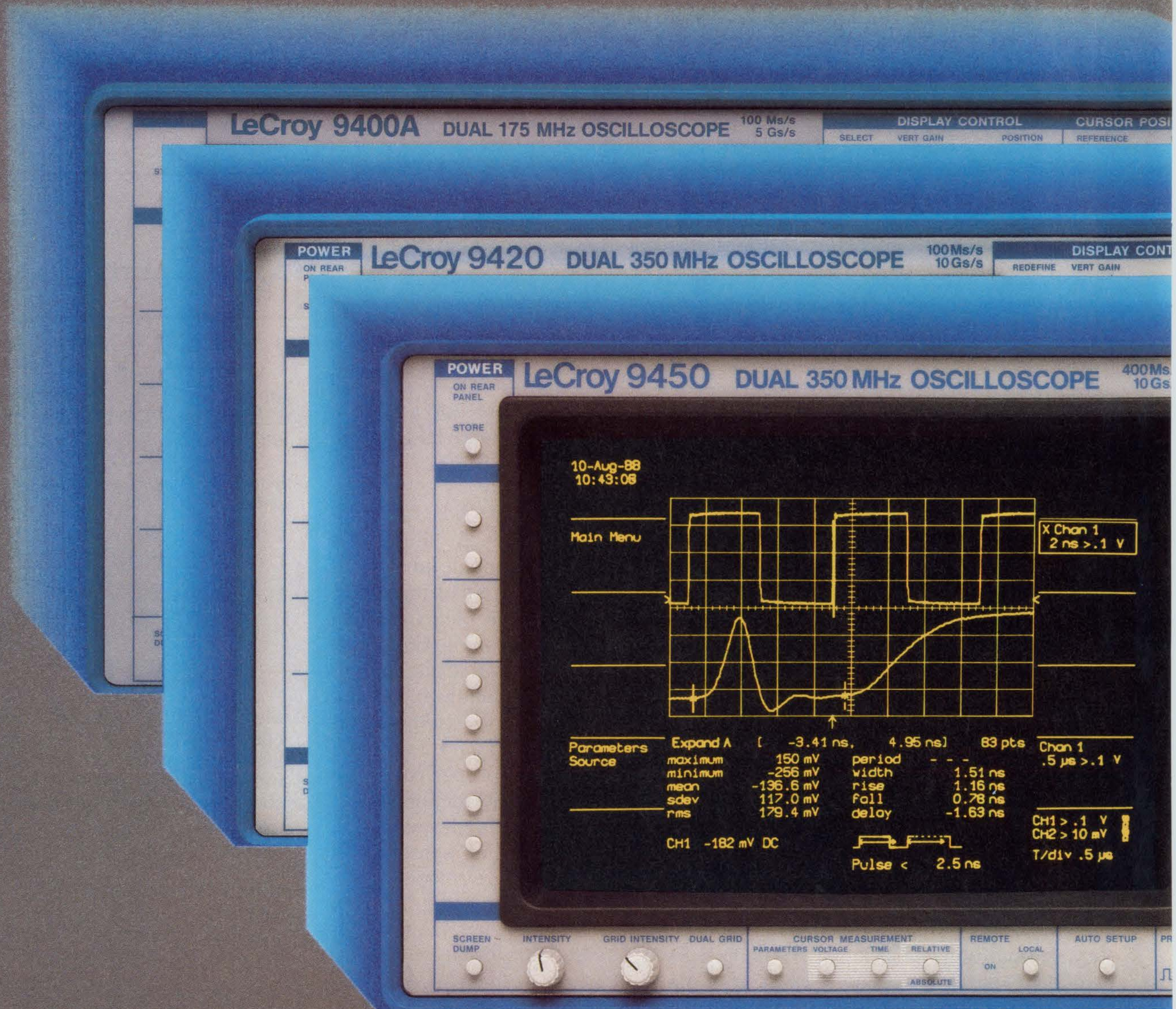
PRICE AND AVAILABILITY

The Cognex SMD tools, currently in beta-site testing, will be available in mid 1989 for $2000.

Cognex Corp., 72 River Park St., Needham, MA 02194; Judy Cobb, (617) 449-6030. **CIRCLE 515**

HOW VALUABLE?	CIRCLE
HIGHLY	559
MODERATELY	560
SLIGHTLY	561

Who do the Best



Model	Bandwidth (MHz)	Sampling Rate S.S. (Ms/s)	RIS (Gs/s)	Memory per Channel (kwords)	Vertical Resolution (bits)	FFT Spectral Analysis
9450	350	400	10	50	8†	yes
9420	350	100	10	50	8†	yes
9400A	175	100	5	32	8†	yes

† up to 12 bits with averaging

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CIRCLE 55

LOGIC ARRAY FAMILY BLENDS PGA AND PLD ATTRIBUTES

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DAVE BURSKY

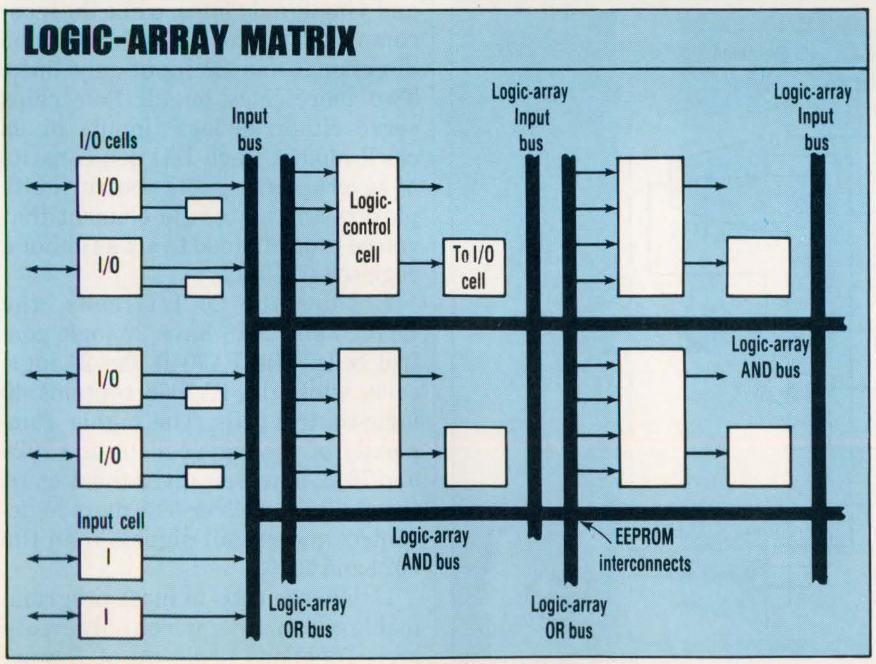
When designers are picking a programmable logic chip, they know that the more flexible the chip's architecture is, the better. Typically, this has meant choosing between the new high-density programmable gate arrays and the low-complexity programmable logic devices (PLDs). More flexibility allows chips to distinguish themselves in a crowded market of programmable ICs with propagation delays between 15 and 55 ns.

Flexibility is just what International CMOS Technology offers in its new family of electrically erasable, programmable logic circuits. The family solves some of the architectural limitations of past programmable chips by applying low-power CMOS circuitry and electrically erasable memory to a novel architecture.

The family comprises four arrays built in a 1-μm (drawn) CMOS process that combines aspects of both programmable-logic devices and field-programmable gate-array architecture to achieve approximate gate-replacement complexities of 1200 to 3000 gates. The architecture of ICT's Peel (programmable electrically erasable logic) Arrays probably seems familiar at first glance—it consists of an array of buried logic control cells surrounded by I/O output cells. Internal circuits operate at clock frequencies as high as 50 MHz, and the pin-to-pin propagation delay is 23 ns, maximum. (Pin-to-pin propagation is the delay of a signal going into an I/O buffer through one level of logic in the array and out through another I/O pin). Additional levels of logic can be added internally at a penalty of about 17 ns per level.

Unlike other arrays, though, which implement the logic function in the logic cells, the Peel Array architecture has its sum-of-products functions distributed in the programmable interconnection matrix *(Fig. 1)*. That distributed logic-array matrix consists of multiple buses that form the input lines (input bus), product terms (AND bus), and sum terms (OR bus). Thus, complete sum-of-product functions are available as inputs to each logic control cell. The control cell, in turn, would use the functions for various combinatorial and register-related purposes.

The flexibility of this dual architecture makes it possible for the PA7000 family to tackle a wide range



1. UNLIKE MOST PROGRAMMABLE ARRAYS, the Peel Array from International CMOS Technology has its combinatorial logic distributed in the X-Y interconnection channels.

of applications, from state machines to random logic. Like PLDs, the circuits can readily implement high-speed and wide-data-path sum-of-product functions, such as state machines, binary counters, clock dividers, address decoders or encoders, comparators, and so forth. And like programmable gate arrays, standard random-logic elements—such as a 74LS74 D flip-flop with independent Clock, Reset, and Preset, or Set-Reset and gated latches—can be readily programmed into the Peel Arrays.

The circuits are particularly well suited for high-speed state machines because both T and J-K type flip-flops can be configured, and extensive product-term sharing can be implemented to permit a large number of states and multiway branches to be set up. Buried state registers allow for both Mealy- and Moore-type state machines. And input latches can be set up for pipelining the state inputs.

There will be four versions of the array: the PA7024, 7028, 7040, and 7068. The first two to be sampled, the PA7024 and 7040, contain logic-control cells with four primary inputs and a general-purpose programmable register. The inputs are fed by sum terms from the OR bus *(Fig. 2)*. The cells contain three programmable signal-routing and control multiplexers, a register that can be configured as an asynchronous or synchronous D, T, or J-K flip-flop, and several EEPROM bits to hold the configuration data.

Sum term inputs can be used to control multiple functions. For example, SUM A can serve as the D, T, or J input of the register or combinatorial path. SUM B can serve as the K input or the preset to the register or a combinatorial path. SUM C can be the clock or the reset to the register or a combinatorial path. SUM D can be the clock to the register, the output enable for the connected I/O cell, and so forth. Unlike programmable logic chips that have simple product-term control for clocks, resets, presets, and output enable signals, the chips use complete sum-of-product functions and are thus more flexible.

Furthermore, the logic-control cells also have two primary outputs: One sends its signal to the input bus; the other can be connected to any I/O cell. The two logic-control cell outputs are completely independent of each other. Consequently, each cell can have two different outputs. That gives a chip like the PA7024 a total of 40 sum-of-products logic functions. In comparison, a popular PLD such as the 22V10 can deliver only 10 sum-of-product functions. Of the two logic-control cell outputs, one can be routed to an I/O cell and the associated I/O pin. The other output is "buried" and available for use within the distributed logic-array matrix. Up to 20 levels of buried logic are possible with the PA7024—enough for the circuit to implement a 20-bit binary counter without using any I/O pins.

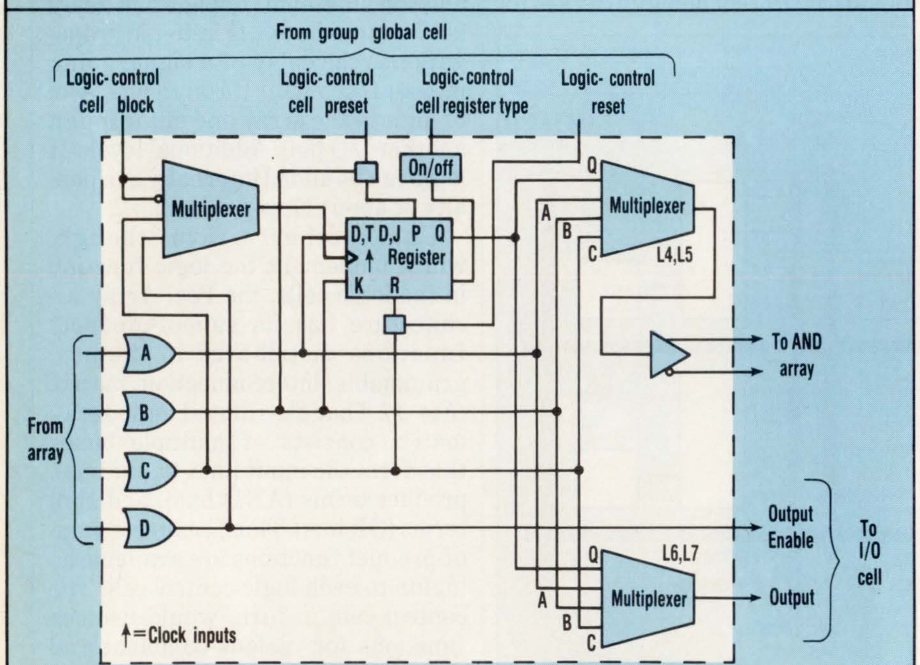
The other two chips, the PA7028 and 7068, have functionally enhanced cells with six sum inputs, dual multipurpose registers, and three outputs. The enhanced cells have more flexibility and make possible a higher degree of cell utilization.

The PA7024 and 7040 have I/O pin counts of 20 bidirectional lines (7024), and 24 bidirectional and 12 input-only lines (7040). The more complex PA7028 packs 20 bidirectional and 4 input-only lines, while the most complex chip, the PA7068, has 40 bidirectional and 22 input-only lines. Two more lines on all four chips serve either as logic inputs or as clock inputs. Each I/O cell consists of several routing and control multiplexers and a storage element that can be programmed to act as either a register or a latch.

Besides the 20 I/O cells, the PA7024 and 7028 have 20 logic control cells. The PA7040 has 24 logic cells, while the PA7068 contains 40 logic-control cells. The higher complexity of the logic cells in the 7028 and 7068, however, gives those chips the ability to deliver 50% more logic-control and output signals than the 7024 and 7040.

Unlike the cells in most programmable gate arrays, which only create logic functions made up of few inputs, the logic-control cells of the PA7000 family can have very wide sum-of-product functions. The wide

LOGIC CONTROL AND I/O CELLS



2. EACH LOGIC-CONTROL CELL in the PA7024 gets its four inputs from the distributed logic, sends one of its outputs back into the array, and sends the other output to one of the I/O cells.

FOR LAMBDA CIRCLE 56 ⟶

PRICE AND AVAILABILITY

Samples of the PA7024 will be available in the second quarter in either 24-pin 300-mil DIPs or 28-lead plastic leaded chip carriers. Samples of the other chips will be ready in the third quarter. The PA7040 will come in a 40-pin DIP or 44-lead PLCC; the PA7028, in a 28-lead 300-mil DIP or PLCC; and the PA7068, in a 68-lead PLCC. The initial price for the PA7024 in 100-unit quantities is $22.50.

International CMOS Technology Inc., 2125 Lundy Ave., San Jose, CA 95131; (408) 434-0678, Robin Jigour. **CIRCLE 512**

functions make it possible for the circuits to implement complex logic with a single-level propagation delay, rather than the multiple levels typically required in most programmable arrays.

Residing at the intersection of each bus within the distributed logic array are electrically erasable and reprogrammable memory cells that control the interconnectivity. With these memory cells, the input lines, product terms, and sum terms can be selectively connected to form complete sum-of-product functions. The end result is that each sum term feeding into a logic-control cell can have extensive product-term sharing, much as with programmable-logic-array architectures. The AND buses of the PA7024, for example, supply up to 80 product terms, while the 7040 supplies up to 120 terms.

Furthermore, because the array structure is very symmetrical, timing delays between I/O pins, I/O cells, and logic-control cells are completely uniform. The symmetry eliminates some of the complex routing and timing issues that high-complexity logic chips encounter.

To make the job of designing with these new chips easier, ICT has created the Arrays family of development tools, which run on IBM PC XTs, PC ATs, or compatible computers. Standard Boolean-logic design techniques can still be applied, but the system also offers schematic entry. The package includes an architectural editor and a logic compiler that creates a design environment amenable to both Boolean-logic entry and schematic descriptions. Once designs are captured, the compiler portion of the software performs syntax checking, logic transformation and reduction, simulation, documentation, and JEDEC-file creation for the programming hardware.□

HOW VALUABLE?	CIRCLE
HIGHLY	550
MODERATELY	551
SLIGHTLY	552

CIRCLE 57

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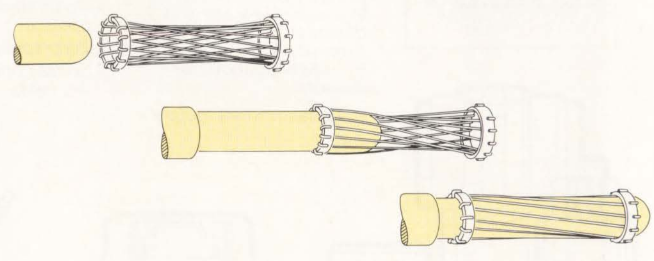

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CIRCLE 58

Improvements Help Double MFLOPS Rating.

VLIW Computers Shift Into High Gear

Lisa Gunn

On their way to forging the world's fastest super-minicomputers, companies like Alliant and Convex have taken the parallel processing route. But parallel processing has its limitations: Only portions of an application—mainly loops and vector calculations—can run in parallel. Conditional jumps and data precedence further limit the amount of code that can execute simultaneously.

Designers at Multiflow Computer, in Branford, Conn., tried a different concept. Using a very-long-instruction-word (VLIW) architecture, they developed a family of computers that run at between 23 and 120 MFLOPS. The Trace 300 series is the second-generation of Trace computers. The first units, the 7- and 14-word-wide Trace 200 introduced in April, 1987, do roughly 14 and 30 MFLOPS, respectively.

The Trace 300 family includes three virtual-memory, Unix-based systems. These faster machines owe their speed to improvements in the compiler technology, the CPU, and the I/O hardware. The family can handle 7-, 14-, and 28-word (1024-bit) widths. The Trace 28/300 system is the industry's first computer to handle 28 separate operations in one clock cycle.

According to company designers, who began work on the first machine in 1984, the VLIW architecture, combined with a compacting compiler, paves the road to fastest performance. The principle behind VLIW computing is similar to that of parallel computing—execute multiple instructions in one clock cycle. VLIW differs from other technologies in that all instructions are arranged as one word for one processor. Nonvectorizable code and conditional jumps don't inhibit the VLIW architecture's speed increases. The Multiflow architecture delivers unmatched performance on a broad range of applications, including but not limited to those programs containing vector computations.

Software Driven

The VLIW computer has a software-driven architecture. Its hardware was designed as a target for the Trace Scheduling compiler. Because there's just one CPU and one program counter, the design is very simple.

The Multiflow Trace Scheduling compiler is the heart of the machine: With software, it handles code compaction—the rearrangement of code for parallel execution. This was previously done with hardware. The compacting compiler takes ordinary sequential code and compresses it into very long instruction words that run on the Multiflow architecture.

Compilers designed to make program execution parallel look for pieces of software programs that can be executed simultaneously, while still maintaining correctness. Previous approaches to compacting compilation looked only at these basic blocks of code and were limited in the amount of overlap found.

Trace-Scheduling compacting compilers operate by predicting the fastest route, or trace, through a program. The compiler then compacts the entire trace, overcoming the traditional conditional-branch bottleneck to achieve large program speedups.

Code Compensation

Mistakes can occur, though, if the compaction causes something to happen before it should, or if it

VLIW COMPILER TECHNOLOGY

Sequential code:

```
LD A
LD B
t1 = A*2
T2 = B*3
t3 = t1 + t2
LD I
t4 = 2*I
C = t4*t3
ST C
LD J
t5 = I+J
t6 = 4*t5
t7 = A+B
t8 = C+t7
Q = t8 -t6
ST Q
```

(b)

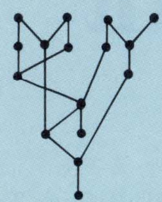
Fortran code:

C = (A*2 + B*3) *2*I

Q = (C + A + B) -4*(I+J)

(a)

Dependency graph



(c)

Wide instruction words:

LD 0	LD 1	INT 0	INT 1	FP 0	FP 1	Branch
LD A	LD B					
LD I	LD J			A*2	B*3	
		2*I	I+J	t1+t2	A+B	
		4*t5		t4*t3	C+t7	
ST C				t8-t6		
ST Q						

(d)

1. NEW COMPILER TECHNOLOGY offers further compaction of code for a faster run time. A simple Fortran program that computes two equations executes in 16 sequential operations (a, b). A graph illustrates which operations are dependent on the outcome of others (c). The 16 sequential operations are compiled into very-long-instruction words that compute the equations in only six clock cycles (d).

doesn't cause a necessary action to occur at all. Necessary corrections—predominantly the branch bottleneck—are handled automatically through compensation code. Compensation is generally small, and its execution time doesn't take away the speed increase that is gained the compaction.

A big advantage of the software-based approach to computing is the ease with which applications can be ported to it. The compiler runs any code written in standard Fortran or C to produce efficient object code. Lisp, Pascal, and Ada programs will also be supported.

Already over 100 third-party applications and hundreds of proprietary applications were ported to the Multiflow system. This opens doors to those who want the high performance of mini-supercomputers, but don't want to fiddle with code.

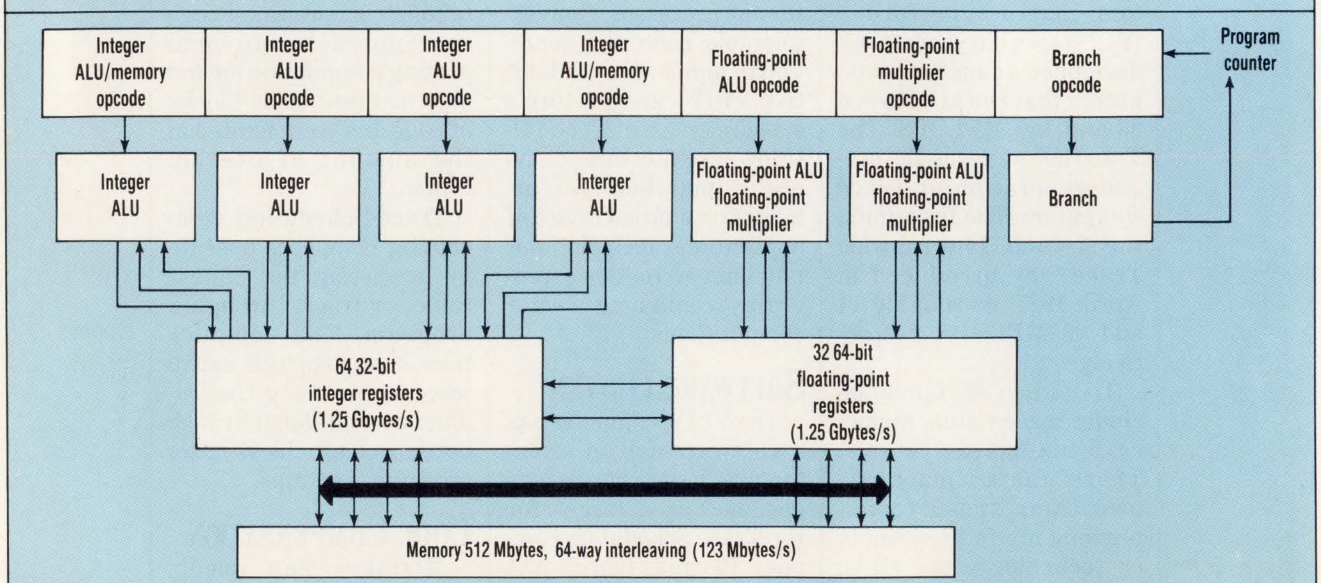
COMPILER TRANSPARENCY

It's this compiler transparency that makes Multiflow's mini-supercomputers valuable to those outside of the scientific community. "The VLIW architecture is less sensitive to coding style, making it easier to write code for it," says John O'Donnell, Multiflow's vice president of engineering. "The programmer can focus on the application problem, not the hardware."

Because Multiflow takes the software-based approach to computing, most improvements made for the second-generation model were to the machine's compiler. Compiler changes resulted in almost a three-times increase in program execution speed *(Fig. 1)*.

The compiler underwent three major modifications. The first was a new procedural linkage for call subroutines that's four times faster than the previous compiler's method. Also, the compiler has a new loop-optimization method and new register-

HARDWARE IMPROVEMENTS



2. HARDWARE CHANGES in the Trace 300 computer include a bigger I/O system and multifunctional math units. Implementing the floating-point units in ECL resulted in a substantial speed increase.

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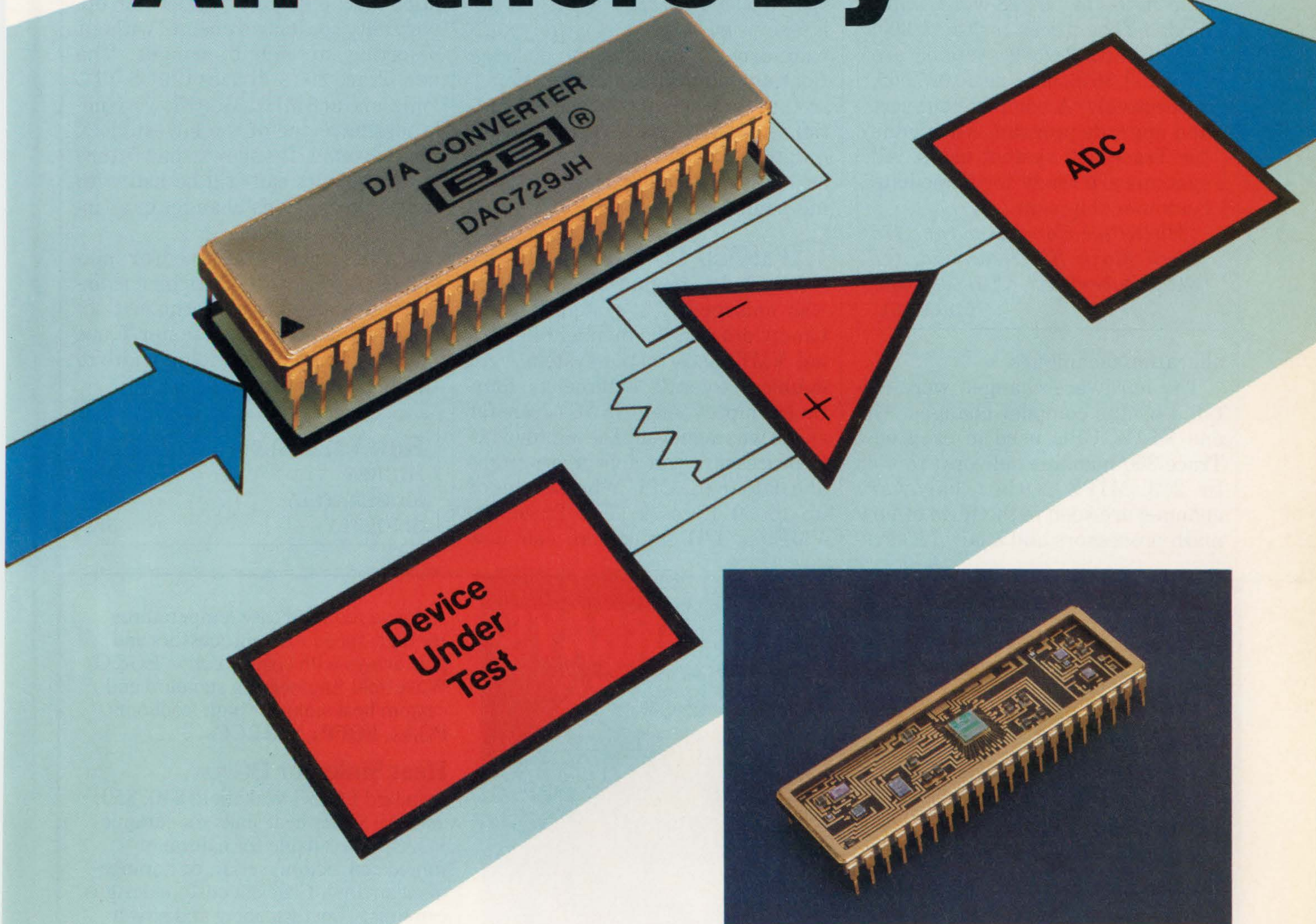

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PRICE AND AVAILABILITY

The Trace 300 computer is available in 7-, 14-, or 28-word width models. The prices for the 7/300, 14/300, and 28/300 systems are $514,300, $646,300, and $1,025,600, respectively. A complete support and upgrade program is available for Trace 200 system users. All systems are ready for immediate customer shipment.

Multiflow Computer Inc., 175 North Main St., Branford, CT 06405; Robert Nix, (203) 488-6090.

CIRCLE 511

allocation techniques.

The hardware changes were dictated by the compiler changes. The one VLIW CPU used in each new Trace 300 machine delivers from 53 to 213 MIPS. Other hardware changes are seen in the form of new math processors and a new I/O system *(Fig. 2)*.

Trace 300 computers have ECL floating-point units for improved speed. The ECL math units cut the latency time in half. A largely software-driven change was to make all floating-point units multifunctional, so that they can perform multiplications and additions. This leaves more opportunity for the compiler to schedule an instruction at any floating-point unit.

EXPANDED I/O BANDWIDTH

The Trace computer's I/O system was enlarged. It's system-memory bandwidth and the number of external VMEbuses to the system were doubled. Overall, a three- to four-times improvement in I/O transfer speed was achieved. The improved I/O processors can deliver programs and data to the CPU at burst rates of up to 60 Bytes/s. The Trace 300 VMEbus I/O processors can now support virtually any high-performance peripheral.

When designing its second generation machine, Multiflow saw an opportunity for improvements without resorting to circuit changes. The new Trace 300 still uses CMOS TTL logic, and at 8 MHz, Multiflow's computers have one of the lowest clock rates around. It follows that future improvements can still be had with process technology changes or an increased clock speed.

Unlike traditional vector machines, the Multiflow machine is linearly scalable in performance. In other words, building a faster Trace machine just entails adding width to the instruction word.☐

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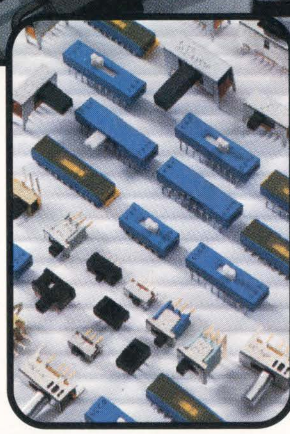

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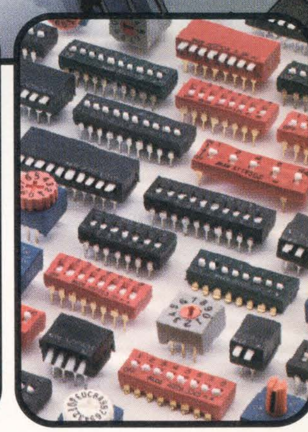

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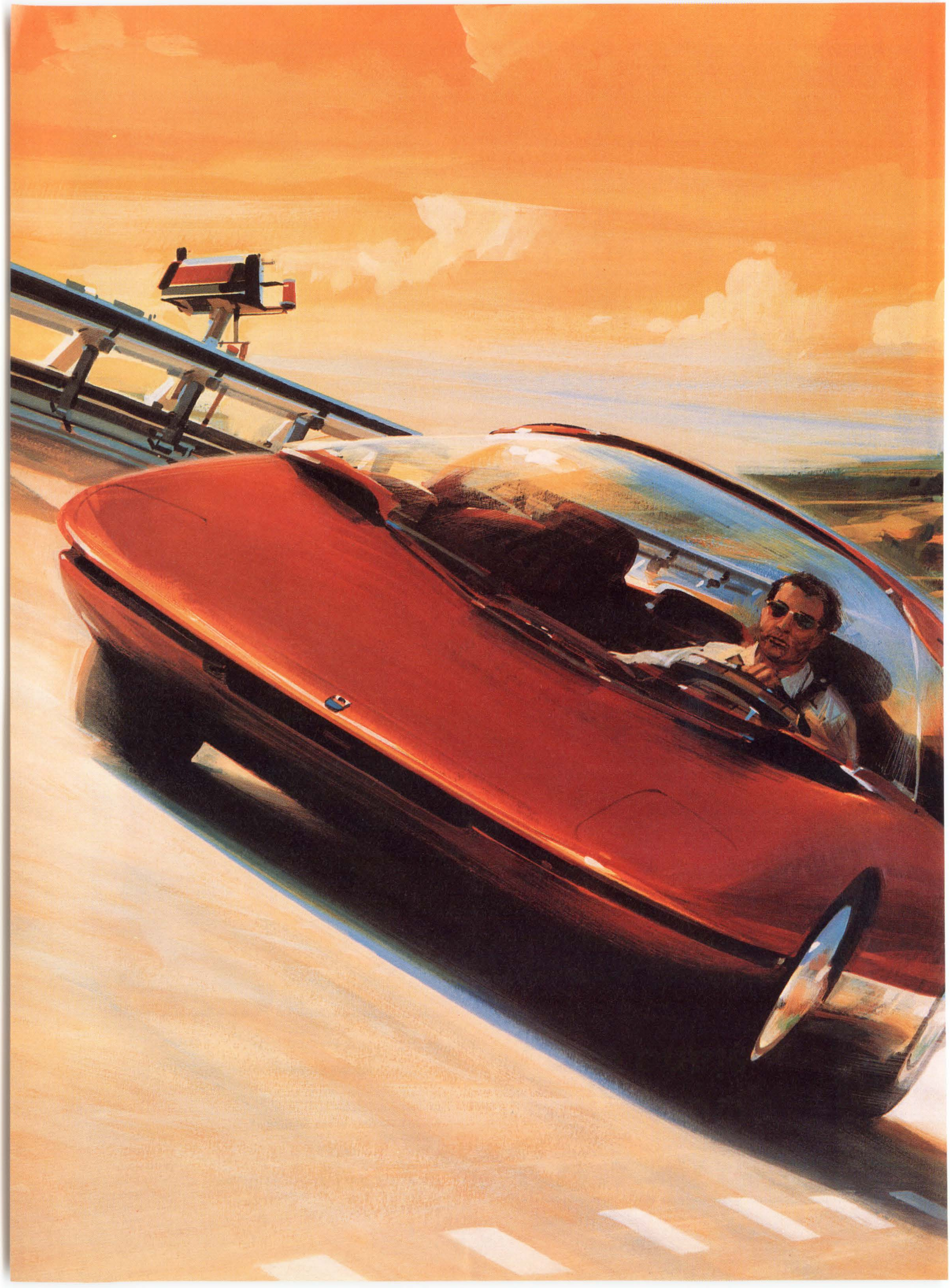

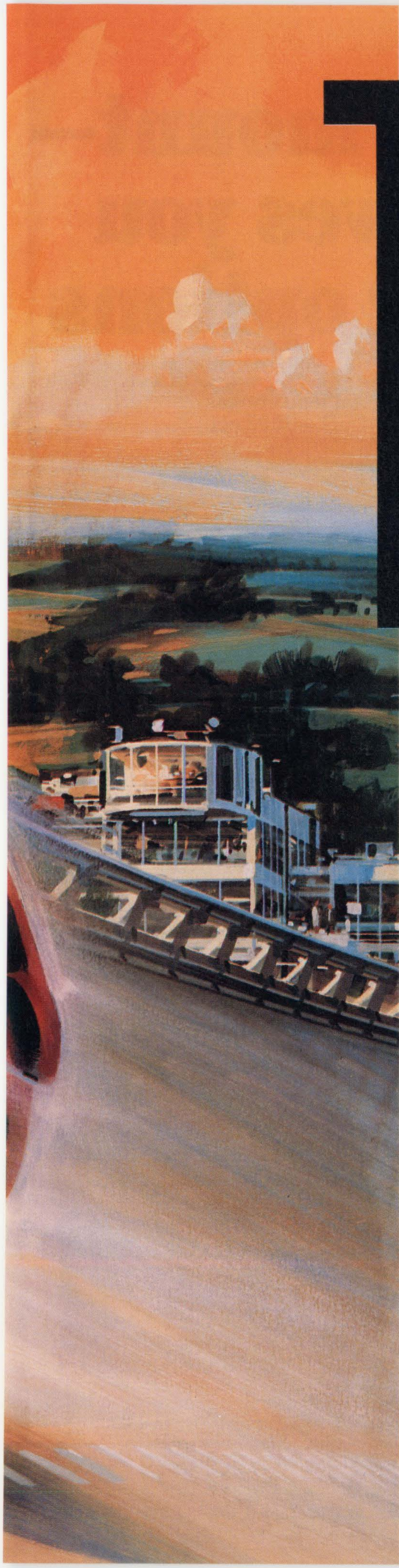

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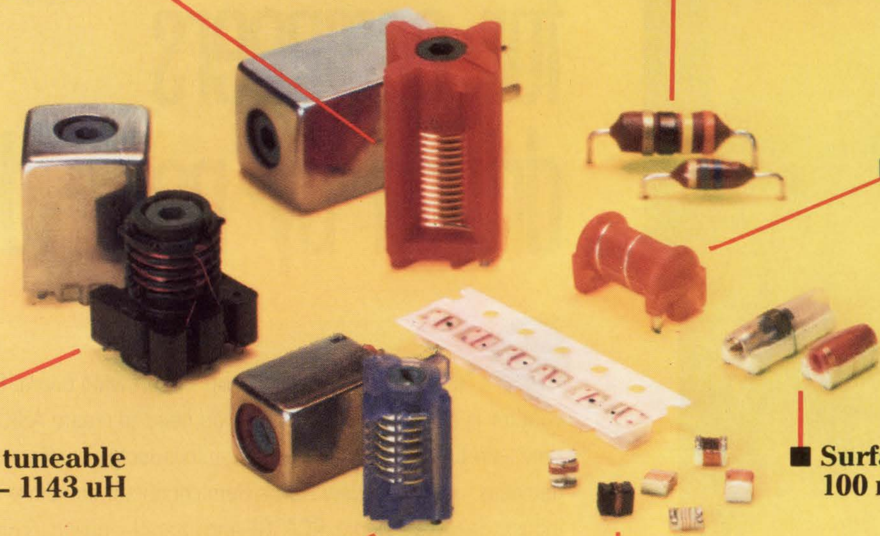

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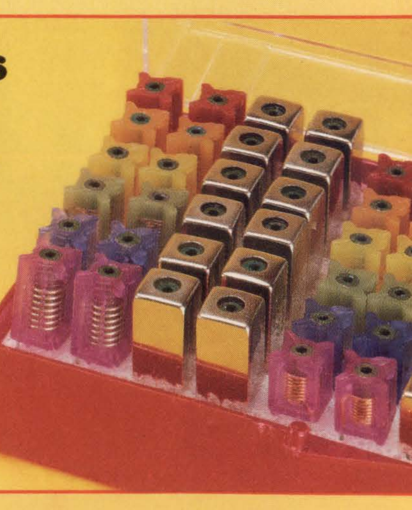

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Serial-Communications Controller Boasts 10-Mbit/s Transfer Rate

David Maliniak

Pressed by the demands of computer users, designers have searched for ways to increase the speed of network communications to take advantage of the burgeoning speed and power of today's processors. Zilog's Z16C30 universal serial controller (USC) chip is a step in that direction. With its 10-Mbit/s data-transfer rate, the CMOS chip is the fastest dual-channel, general-purpose controller available, according to the company.

The device's 10-protocol, general-purpose architecture enables designers to link their networks to a variety of systems, even as interconnection standards evolve. On top of that, the controller's programmability lets the single chip communicate with multiple systems, instead of using a dedicated controller for each protocol.

Communication-throughput gains and the related reductions in CPU overhead have been achieved through the incorporation of a 32-byte FIFO buffer on each transmit and receive line. A single burst access over one channel of the USC chip can thus move a 32-byte block of data, compared with multiple 3-byte transfers performed by conventional controllers.

The USC chip has two full-duplex channels, each supporting 10 different protocols and eight data-encoding formats. Some of these protocols include asynchronous, bit and byte synchronous, isochronous, Ethernet, and MIL-STD-1553B. Data-encoding formats include NRZ, NRZI, FM0, FM1, Manchester, and differential Manchester. Two independent baud-rate generators for each channel can be programmed to permit each channel's receiver and transmitter sections to operate at different rates. Each channel also includes a digital phase-locked loop and interrupt lines that implement a CPU-to-USC daisy-chain hierarchy.

Each receiver and transmitter is supported by a 32-byte-deep FIFO memory and a 16-bit message-length counter. All modes permit optional even, odd, mark, or space parity. Synchronous modes allow the choice of two 16-bit or one 32-bit cyclic-redundancy-check (CRC) polynomials. Selection of from 1 to 8 bits per character is available in both receiver and transmitter independently. Error and status conditions are carried with the data in the receive and transmit FIFO memories to greatly reduce the central processing unit's overhead required to send or receive a message.

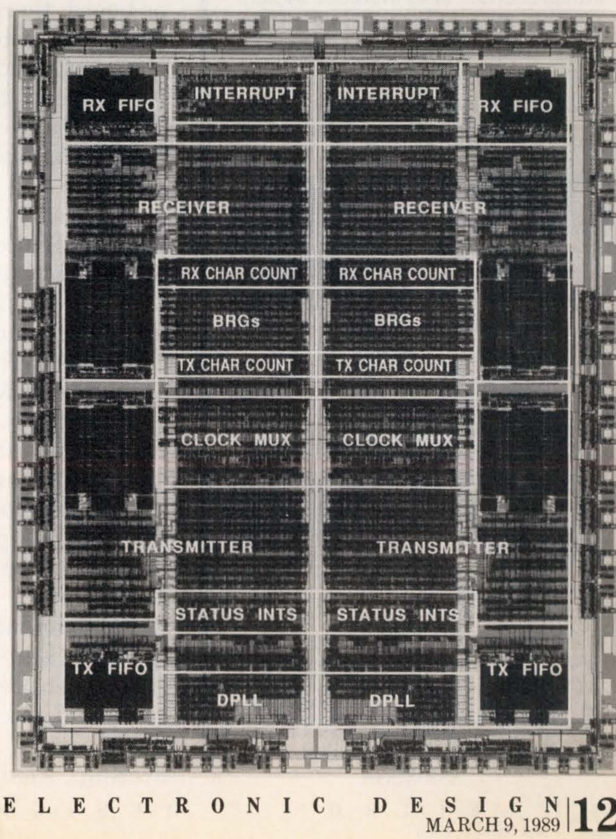
Specific, appropriately timed interrupts are available to signal such conditions as overrun, parity error, framing error, end-of-frame, idle line received, sync acquired, transmit underrun, CRC sent, closing sync/flag sent, abort sent, idle line sent, and preamble sent. In addition, several useful internal signals such as receive FIFO load, received sync, transmit FIFO read, and transmission complete may be sent to pins for use by external circuitry.

The device can generate and check CRC codes in any synchronous mode, and can be programmed to check data integrity in various modes. The controller also has facilities for modern controls in both channels. In applications where these controls are not necessary, the modern controls may be used for general-purpose I/O operations. The same is true for most of the other pins in each channel.

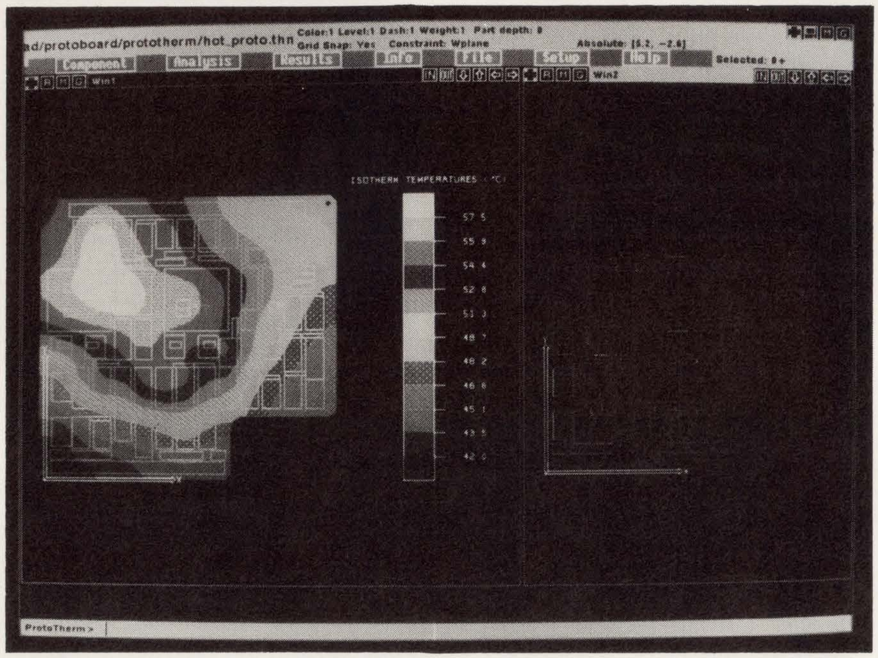
Reliability is enhanced by the device's bus-oriented testability. Dedicated registers buried in the device are accessible by means of the data bus through the regular register set. This permits users to test the controller's transmission reliability during system operation.

Because the controller's cores and cells are designed modularly, the company can easily increase or decrease functionality in subsequent versions that will appear in 1989. The Z16C30 universal serial controller chip comes in a 68-pin plastic leaded chip carrier. It operates from a 5-V supply and consumes 250 mW maximum. The initial sample price is $105 in quantities of 100. Volume pricing in lots of over 10,000 is expected to be under $30 within 12 months. Samples are delivered from stock.

Zilog Inc., 210 Hacienda Ave., Campbell, CA 95008; (408) 370-8000. **CIRCLE 306**



Additions To CAE Packages Ease Thermal-Analysis Tasks



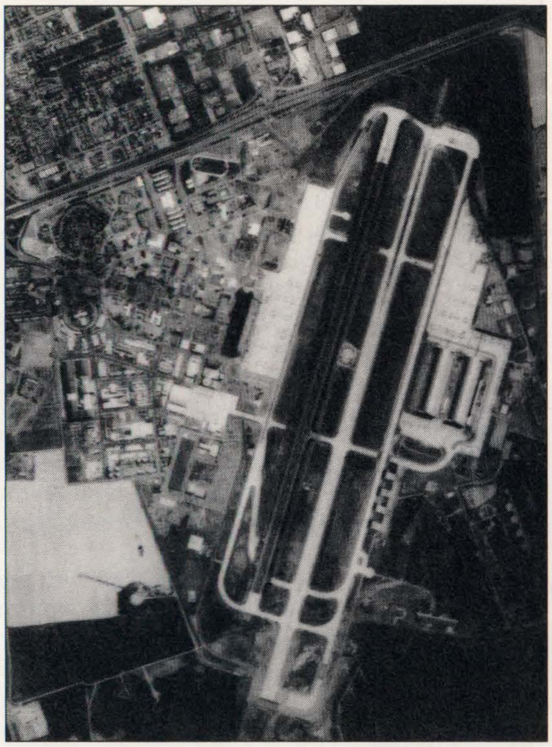
A pair of thermal-analysis tools and a solids-modeling capability strengthen Mentor Graphics' design-automation offerings. ProtoTherm is a pc-board thermal-analysis tool for designers who need a fast, easy means of evaluating the thermal performance of their designs early in the design cycle. For packaging engineers, airflow modeling has been added to the AutoTherm thermal-analysis software for the company's Package Station, while AutoSurface gives that system the ability to transform wireframe models into shaded images in minutes.

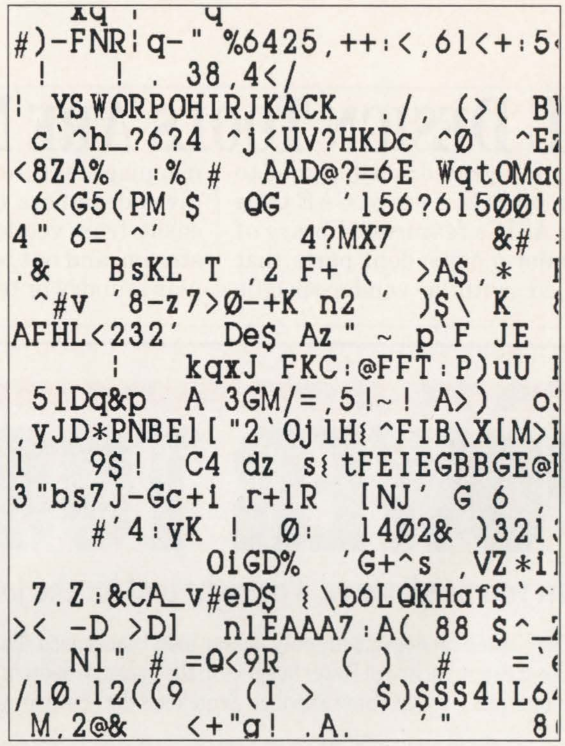
The ProtoTherm tool is offered as an option to Mentor's IDEA Series engineering workstations that include Idea Station schematic capture and simulation systems and Board Station pc-board layout systems. The tool can give users a complete analysis of the temperature distribution across a board in minutes. It models conduction, convection, and radiation heat-transfer mechanisms. Also, it can predict junction temperatures and potential thermal failures due to board and component overheating. Analysis results are presented in various graphic formats, including isotherm maps, temperature-profile graphs, junction-temperature maps, or tabular reports.

By adding airflow modeling to the AutoTherm thermal-analysis software, the package can now predict the velocity distribution and temperature of airflow within an electronic-package enclosure. With its flow solver, AutoTherm models forced convection by using an ideal flow to predict velocities at any point on a board. Users can specify flow boundaries, inlets and outlets, as well as inlet velocity to define the model. The AutoSurface capability for the Package Station automatically creates shaded images and models with hidden lines removed from wireframe models.

Until June 30, the ProtoTherm tool goes for $15,000 with first shipments in March. The AutoTherm software and AutoSurface capability are included in the company's Package Station. The AutoSurface can be added to 3D Design as an option for $7500. Both will ship in March.

Mentor Graphics Corp., 8500 S.W. Creekside Pl., Beaverton, OR 97005; (503) 626-7000. CIRCLE 307

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ASIC DESIGN TOOLS ARE NOT TIED TO FOUNDRY

Fully integrated and designed to run on PCs, a set of CAE tools for ASICs features a library of 1200 vendor-independent parts that is coupled with a vendor-specific mapping feature. The combination gives designers the ability to move easily from vendor to vendor in midstream, and not be tied to any particular foundry or technology.

With the tool set, designers can quickly develop prototypes with gate arrays to keep costs down, and then switch to another technology or vendor to get higher performance, lower piece prices, or to circumvent supplier problems. Circuit designs can easily be translated from one vendor's library to another's. In addition, the tools let users simulate the performance of candidate vendors and evaluate test vectors on a PC, instead of incurring high foundry costs.

The system begins with a generic schematic library and capture tool that offers some 1200 medium-scale-integration parts, including 236 flavors of flip-flops and many high-level devices like adders, comparators, and multiplexers. Users can design their schematics rapidly with a high-level pick-and-place technique that eliminates the need for assembly with low-level primitives. The resulting designs map into silicon with optimum efficiency.

ASIC designers then use a net-list translator which, with a vendor-mapping library and a simulator mapping feature, "compiles" the circuit schematic into a collection of vendor-specific cells and interconnections. If the selected vendor does not offer a particular high-level part, the translator automatically compiles it from the vendor's primitives. Vendor-mapping libraries are available for several ASIC vendors.

The system's gate-level simulator helps users verify their designs and make strategic tradeoffs among price, performance, vendors, and technologies. A given 5000-gate ASIC design tested with 2000 vectors benchmarks in 10 minutes on a 10-MHz PC AT.

The price for the schematic library, the simulator mapping library, and the net-list translator is $200. Each vendor-mapping library is an additional $200. The gate-level simulator goes for $950. All are delivered from stock.

Tanner Research Inc., 128 W. Del Mar Blvd., Pasadena, CA 91105; (818) 795-1696. **CIRCLE 308**

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CIRCLE 29

PC-BOARD SOFTWARE EASES PARTS PLACEMENT, ROUTING

Version 4 of DC/CAD adds automatic parts placement and a rip-up and retry autorouter to the schematic capture and printed-circuit board design software. Using a parts list generated at the netlist level, the autoplace facility accomplishes its task in three passes. The autorouter offers high completion rates for densely-populated or complex boards and has the ability to route around pads. And bidirectional file transfers let the software communicate with other CAD systems.

Cadet Inc., 36 Franklin Ave., Staten Island, NY 10301; (718) 442-1053. **CIRCLE 316**

TOOL SIMULATES NEURAL-NETWORKS

BrainMaker, a neural-network simulation tool, is a complete system for designing, building, training, testing, and running neural networks. It can run up to 500,000 neural connections/s. No programming is required; the software takes care of that. It is fully menu-driven and supports color monitors and mouse attachments. Special input and output

facilities are included for visual or symbolic data manipulation. The tool runs on an IBM PC XT, PC AT, or compatible, DOS 3.0 or higher, and one floppy-disk drive. A user's guide accompanies the software.

California Scientific Software, 160 E. Monecito #E, Sierra Madre, CA 91024; (818) 355-1094. $99.95. Available immediately.

CIRCLE 317

MEMORIES PROGRAMMED IN-CIRCUIT THROUGH PC

The Boardsite in-circuit programming systems make on-board programming of MOS and CMOS PROMs, EPROMs, EEPROMs, microcontrollers, microprocessors, and PLDs available to commercial users. Designers can program or reprogram devices that are already assembled on a board without removing them and without fear of damaging the surrounding logic devices. This reduces manufacturing and servicing costs. The model 4100 programs one board at a time, while the 4400 can program several boards simultaneously. Both are available in benchtop or portable versions.

Data I/O Corp., 10525 Willows Rd. N.E., Redmond, WA 98073; (206) 881-6444. $9500 (4100), $14,500 (4400). **CIRCLE 318**

DIFFERENTIAL EQUATIONS SOLVED AUTOMATICALLY

Simnon/PC Version 2.11, for MS-DOS or VAX computers, is an interactive tool that solves nonlinear differential and difference equations. All the user has to do is type in the equations. The program then automatically solves them using advanced numerical techniques and even plots the results. The progress of the solution can be monitored on-screen while the equations are being solved. All major graphics standards are supported. A math coprocessor chip is required.

Engineering Software Concepts Inc., 436 Palo Alto Ave., Palo Alto, CA 94301; (415) 325-4321. $695. Available immediately.

CIRCLE 319

CALCULATOR PERFORMS VARIED FUNCTIONS

A total of 254 functions, including 40 complex-number functions, are packed into an advanced scientific calculator from Texas Instruments. The TI-68 solves up to five simultaneous equations and has powerful formula-programming capabilities.

Taking the philosophy that engineers should only have to concentrate on problem-solving skills and not on programming intricacies, the calculator includes prompting, an alphanumeric display, straightforward number entry for complex numbers, and easy-to-use formula programming. As a result, the TI-68 performs complex activities, but is not complex to use.

In solving up to five simultaneous equations with real or complex coefficients, a plain-English prompting system guides users through each equation. Forty different complex-number functions are included from simple arithmetic to advanced trigonometry. Users can enter complex numbers just as they are written using either polar or rectangular coordinates. The display simultaneously shows both the real and the imaginary part of a complex number.

A last-equation feature recalls and replays the last equation calculated, enabling users to check entries and verify answers quickly and easily. Equations can be reviewed without having to be reentered, and changed if necessary.

Up to 36 memories are provided for user storage. Alphanumeric names can be given to each register.

The formula-program memory handles up to 440 steps and as many as 12 formulas. With the calculator's alphanumeric display, program writing and editing is fast and easy. Users can solve problems simply by entering values for the variables.

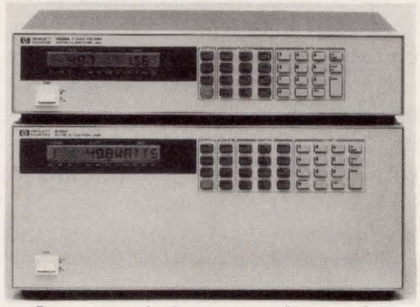
Other functions include integration using Simpson's rule; calculation of the real and complex roots of quadratic, cubic, and quartic equations; and one- and two-variable statistical functions including linear regression and trend analysis. Arithmetic can be done using decimal, hexadecimal, octal, and binary numbers. The calculator performs number-base conversions and Boolean-logic operations.

The TI-68 scientific calculator goes for a suggested retail price of $65 and will be available in the second quarter.

Texas Instruments Inc., Consumer Relations, P.O. Box 53, Lubbock, TX 79408; (806) 747-1882.

CIRCLE 309

DC ELECTRONIC LOADS EASE TESTING OF POWER SUPPLIES AND COMPONENTS



A set of features directed toward power-supply testing, battery-performance evaluation, and power-component testing, either in manual or automatic environments, is packed into a pair or HP-IB-controlled dc electronic loads from Hewlett-Packard. The HP 6050A and 6060A are designed for technical applications in research-and-development labs, incoming and production testing, and electronic-equipment servicing.

The HP 6060A is a 300-W, single-input unit, while the HP 6050A is an 1800-W, multiple-input mainframe device that can hold up to six individual plug-in load modules. A built-in HP-IB interface permits remote control and readback of all load functions. The single-package integrated design of the loads simplifies their integration into an automatic test system.

Applications include power-supply load-regulation tests, load-transient response tests, current/voltage/power crossover characterization, and start-up-delay measurements. Battery-capacity testing can be automated when the load is used with a suitable controller and characteristic curves are plotted. A variety of real-life battery-capacity tests can be simulated under user-programmed control.

The 1800-W HP 6050A is a multiple-input unit that goes for $1800. The 300-W HP 6060A, a single-input load, costs $1995. Delivery is estimated at 4 to 8 weeks.

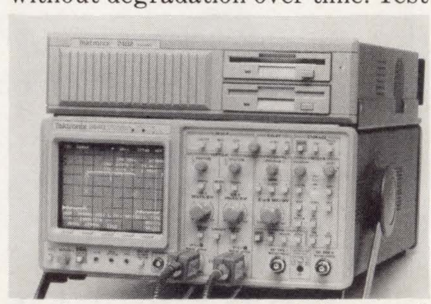
Hewlett-Packard Co., 1820 Embarcadero Rd., Palo Alto, CA 94303; call local Hewlett-Packard sales office. **CIRCLE 310**

WAVEFORM STORAGE, ANALYSIS, AND TRANSFER SYSTEM LINKS TO SCOPES

By linking with any Tektronix 2400 Series digital oscilloscope, the 2402 TekMate software and hardware product significantly extends the scopes' traditional capabilities. With TekMate, users can save up to 500 waveforms and perform sequences of measurements and advanced waveform analysis without the usual programming, time, and expense.

Users can make immediate waveform comparisons, view derived functions (such as fast Fourier transforms) on the scope screen, and capture large numbers of waveforms automatically, without operator attention.

As an integral part of a 2400 Series scope, the 2402 gives users more detailed information from their test results. Because the system stores over 500 waveforms on a single disk, all the raw data is always available without degradation over time. Test results are stamped with dates and times to end test-data confusion.



The 2402 system takes over tedious and time-consuming tasks to free users for more important work. It waits for and saves failures, allowing unattended operation. On top of that, it extends scope automation without adding a controller.

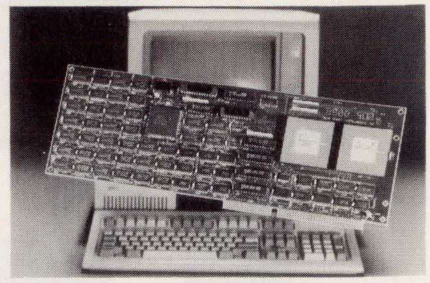
The system includes two 3.5-in., 720-kbyte floppy drives. It comes with GPIB interface and parallel and serial ports.

In a complete package with software, the 2402 TekMate goes for $2990. Delivery is in 2 weeks.

Tektronix Inc., Portable Instruments Division, P.O. Box 1700, Beaverton, OR 97075; (800) 426-2200. **CIRCLE 311**

NEW PRODUCTS
INSTRUMENTS

DESIGN KIT EASES 32-BIT PROCESSOR PROGRAMMING



Users of the SN74ACT8800 family of 32-bit building-block processors will find it easier to program and evaluate the processors using the '8800 Software Development Board (SDB) Design Kit. Consisting of hardware, software, and documentation, the kit lets the user download an application program and data from the host computer to the SBD, where it will be processed by the microprogrammed system. The computer can then read the results out of the SBD's local-data memory. The kit is designed for use with the IBM PC AT and compatibles and with 80386-based systems operating at clock frequencies of 20 MHz or less.

Texas Instruments Inc., Semiconductor Group, P.O. Box 809066, Dallas, TX 75380; (800) 232-3200 Ext. 700. $4000. **CIRCLE 320**

PORTABLE DISK-DRIVE TESTER GOES ANYWHERE

Conducting a full range of analog and digital parametric tests asynchronously, the FS3000 portable test system is compatible with all industry-standard interfaces. Any combination of 3.5- and 5.25-in. drives can be accommodated. The system is self-calibrating during operation. Applications include quality assurance, incoming inspections, manufacturing, and field operation for service organizations, value-added resellers, OEMs, and system integrators. The portable unit contains a 37-character keypad, an optional 80-column printer, and a liquid-crystal display with 640 by 200 resolution.

Flexstar Corp., 606 Valley Way, Milpitas, CA 95035; (408) 946-1445. $12,995. Availability is 30 days. **CIRCLE 321**

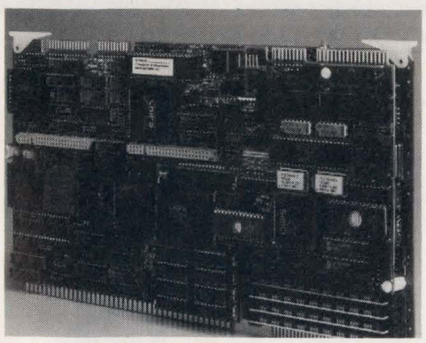
Single-Board Computer Brings AT Software To Multibus I Party

Multibus I, the most popular OEM bus, now can enjoy compatibility with the huge variety of IBM PC AT software thanks to a single-board computer from Single Board Solutions. The MAT286 board is meant for use by OEMs who are heavily invested in Multibus I and would like to branch out into PC-DOS-based applications.

The board combines all the functions of an AT motherboard with other functions usually residing on add-in cards. For example, serial and parallel I/O are included.

For assembly of a complete AT-compatible system, the company's MATxSYSIO board mounts 1/2-in. above and parallel with the MAT286 board in a Multibus I card cage. An EGA-compatible video controller, floppy-disk controller, and SCSI hard-disk interface are packed onto the piggyback card.

For main memory, the MAT286 board uses two or four 256-kword-by-9-bit or 1 Mword-by-9-bit SIMM



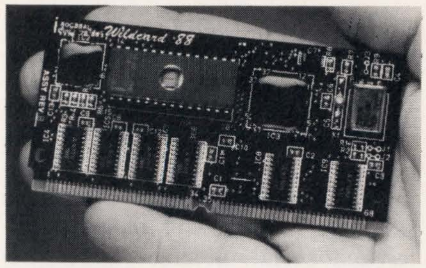
dynamic-RAM modules. This yields an on-board capacity of 512 kbytes, 1 Mbytes, 2 Mbytes, or 4 Mbytes of parity-checked, dual-ported RAM.

The MAT286 board ranges from $997 with no RAM to $3342 with 4 Mbytes. A fully configured MATx-SYSIO board goes for $598, with less capable versions available at lower cost. All prices are for single quantities. Small lots are available from stock.

Single Board Solutions Inc., 20045 Stevens Creek Blvd., Cupertino, CA 95014; (408) 253-0250.

CIRCLE 324

Tiny Board Adds IBM PC XT Functions



The Wildcard-88 is a complete IBM PC XT motherboard equivalent. The interesting feature about this board is its size–two by four inches. Because of this feature and its relatively low-cost, it is suitable for such applications as telephones, home banking systems, and portable instrumentation equipment. The board, which adds XT functionality to products that use embedded-control electronics, is built around a standard CHMOS 80C88 16-bit microprocessor. An EEPROM socket is provided on the board for storing the computer's BIOS program. An 8087 numeric-coprocessor socket is available as an option.

Intel Corp., 3065 Bowers Ave., P.O. Box 58065, Santa Clara, CA 95052. $50 in quantities of 1000.

CIRCLE 325

20-MHz Multibus Board Packs 8 Mbytes Of Memory

Operating at 20 MHz, the MPU-28 multibus single-board computer is designed for applications that require fast processing and large amounts of memory. The board can be used either as a stand-alone microcomputer, a single CPU/controller in a multibus system, or as one of multiple CPUs in a multiprocessor system. It can be configured with 1, 2, 4, or 8 Mbytes of on-board dual-ported DRAM. Other features include a SCSI interface, a 24-bit parallel port, and four 28-pin EPROM sockets. A 68881 or 68882 floating-point math coprocessor is available as an option.

SBE Inc., 2400 Bisso Lane, Concord, CA 94520; (415) 680-7722. From $2155. Avail. is 30 days.

CIRCLE 326

ACCESSORY BOARD FEATURES 10-μS AQUISITION TIME

Allowing the aquisition of data from 2, 3, or 4 channels with less than 40 ns of channel-to-channel sample time, the SSH-4 is a simultaneous sample-and-hold accessory board that may be daisy chained, letting up to 16 channels be sampled at the same time. Featuring a 10-μs aquisition time, each channel may be independently programmed for one of the nine selectable gains over a range of 1 to 800. Each input is fully differential and has its own gain control. Users can measure signals with full-scale ranges between ±5 V and ±6.25 mV. On-board screw terminals simplify field wiring and accept wire sizes from 12 to 22 awg.

Metra Byte Corp., 440 Myles Standish Blvd., Taunton, MA 02780; (508) 880-3000. $425. Available from stock. **CIRCLE 327**

DSP BOARD PERFORMS 1024 FFTS IN 5.7 MS

An IBM-PC compatible DSP board, the ZPB32-HS, is capable of performing a 1024-point fast Fourier transform in just 5.7 ms. And an FIR filter can be done in 160 ns per tap. The board features a high-speed floating-point processor to eliminate range and overflow problems, parallel and serial interface buses, 64-kbytes of RAM, and a comprehensive software-support package. Included in the software are a utilities debugging program and libraries to interface between the board and the PC. An assembler/linker/simulator package is available separately.

Burr-Brown Corp., International Airport Industrial Park, P.O. Box 11400, Tucson, AZ 85734; (602) 746-1111. $1495 with quantity discounts available. Availability is stock to four weeks. **CIRCLE 328**

CONVERTER CARD BOASTS ±1.3-ARC MINUTE ACCURACY

With an accuracy of ±1.3 arc minutes, the SDC-36015 resolver-to-digital and digital-to-resolver six-channel converter card is IBM PC compatible. Each of its six channels offers programmable resolution and bandwidth. Other features include high-quality velocity output, built-in test, loss of signal, and 4-bit turns counting. Output-angle information is provided to the host computer in two 8-bit words. All generated information is memory mapped into four RAM locations and is available through a read command. Demonstration software is available with the card. It can operate in temperatures from –55 to +125°C.

ILC Data Device Corp., 105 Wilbur Pl., Bohemia, NY 11716; (516) 567-5600. From $1095. Availability is stock to 12 weeks. **CIRCLE 329**

ONE SIP CONTAINS TWICE THE MOSFETS

Dual uncommitted power MOSFETs are offered in one hermetic single-in-line metal package (SIP). This lowers production cost, while at the same time reduces equipment size. The OM6201SS through OM6217SS series of n-channel devices is rated at 30 A, with voltages ranging from 100 to 1000 V. Internally-connected bilateral zener clamps protect the MOSFET gates. Applications include military equipment, switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high-energy pulse circuits.

Omnirel Corp., 205 Crawford St., Loeminster, MA 01453; (508) 534-5776. $90 in quantities of 100.
CIRCLE 330

RF AMPLIFIER COVERS 100-MHZ TO 1-GHZ RANGE

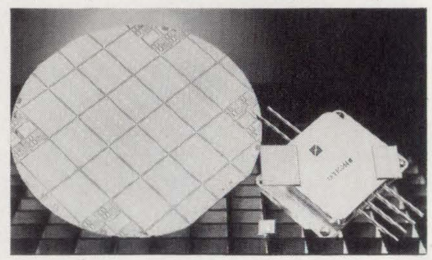
The Model 100W1000M7 broadband rf amplifier delivers a maximum of 180 W, and a minimum of 100 W of continuous-wave power for sweep-frequency testing, rfi-susceptibility testing, antenna and component testing, wattmeter calibration, and general laboratory work in the frequency band ranging from 100 MHz to 1 GHz. Its linear output at less than 1-dB gain compression is 70 W.

Amplifier Research, 160 School House Rd., Souderton, PA 18964; (215) 723-8181. $40,000. Availability is 90 days. **CIRCLE 331**

1000-V, 38-A MOSFET CAN SUPPLY 10 KW FOR MOTOR CONTROLS AND SUPPLIES

Five times the wattage of conventional MOSFETs—up to 10 kW through a single full-bridge configuration—is supplied by Advanced Power Technology's Monster MOS devices. With the devices, designers can build demonstrably more reliable, compact, powerful, and cost-efficient power systems.

A total of 10 devices are being added to the company's Power MOS IV line, extending from the APT10025FN, a 1000-V, 38-A device with a 0.25-Ω on resistance, to the APT4003FN, a 400-V, 100-A MOSFET with 0.035-Ω on resistance. The 12,600-pF maximum input capacitance on these MOSFETs gives them exceptional speed for devices of their power.



Now, designers of power supplies and motor controls can use MOSFETs to handle power levels that in the past were the sole domain of bipolar transistors and thyristors. When used in place of bipolar power transistors, the Monster MOS devices enable designers to simplify control schemes and reduce drive requirements. When used instead of thyristors, these fourth-generation MOSFETs free systems from costly, complex commutation circuits.

The line includes die and devices in TO-3, TO-247, TO-254, TO-257, and TO-258 packages, as well as the company's F-package for Mighty MOS and Monster MOS die with high-current capability. In quantities of 100, prices range from $85 to $130 for die and from $199 to $249 for F-packaged devices. Delivery is from 1 to 6 weeks.

Advanced Power Technology, 405 S.W. Columbia St., Bend, OR 97702; (800) 222-8278. **CIRCLE 332**

DC TO AC POWER INVERTER WEIGHS JUST 14 OZ

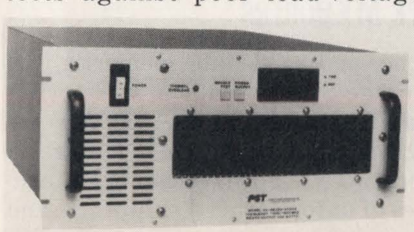
Occupying a space of just 19 in.^{3} and weighing only 14 oz., the Pocket Power Inverter takes an input voltage of 10 to 15 V dc and returns an output of 115 V ac ±5% at 60 Hz ±1%. The completely silent inverter

can be used to operate standard ac-powered electronic test equipment including oscilloscopes, spectrum analyzers, and chart recorders. Other features include a low-battery alarm and automatic cutoff, a high surge capability of up to 200 W, and an efficiency of 90%.

Statpower Technologies Corp., 170-717 Simundson Dr., Point Roberts, WA 98281; (604) 420-1585. $149.95. **CIRCLE 333**

HIGH-FREQUENCY LINEAR AMPLIFIER PUTS OUT 200 W

Covering the frequency range of 1400 to 1800 MHz, the BHC 148188-200 solid-state amplifier produces a 200-W rf output. The Class AB linear amplifier has a gain of 53 dB minimum, a pulse rise-and-fall time of 150 ns, and a instantaneous bandwidth of 400 MHz. A built-in circulator protects against poor load-voltage



standing-wave ratio. The amplifier and its power supply, which is contained in a 19-in. rack-mountable cabinet, operate at 220 V ac, 50 to 60 Hz. Its working temperature range is from 0 to +50°C.

Power Systems Technology Inc., 63 Oser Ave., Hauppague, NY 11788; (516) 435-8480. $42,900. Delivery takes four to five months. **CIRCLE 334**

BATTERIES WITHSTAND EXTREME TEMPERATURES

Ideal for military-communication applications, two lithium sulphur dioxide batteries are capable of withstanding temperatures from –55 to +70°C. The LX 2630 is a C-size cell in diameter, but is 25% shorter. The LX 1639 is a standard A-size battery. Both cells produce 3 V. A glass-to-metal seal prevents the electrolyte from leaking. Along with their exceptional shelf lives, the batteries have a service life more than four times than conventional batteries.

Saft America Inc., 711 Industrial Blvd., Valdosta, GA 31601; (912) 247-2331. **CIRCLE 335**

130- AND 150-W SUPPLIES ARE IBM PC COMPATIBLE

Two new series of switching power supplies are designed for use with IBM PC or compatible computers. The PA4131 series contains three models and achieves a 130-W output. Each model contains four output connectors. The PA4151 series supplies 150 W of power. It has four versions, each with six output connectors. All applicable safety standards are met. Both are equipped with short-circuit protection, incurring no damage when operated without a load. The 4131 is housed in a 150- by 100- (or 140, depending on the model) by 86-mm package. The 4151's casing is 210 by 140 by 118 mm or 150 by 140 by 86 mm.

Lite-On Inc., 726 S. Hillview Dr., Milpitas, CA 95035; (408) 946-4873. From $67.28. Availability is 30 days. **CIRCLE 336**

CUSTOMIZABLE TERMINALS LET INTEGRATORS CHOOSE FROM AMONG FEATURES

By basing the system around an external modular logic platform, Zentec Corp. has come up with a customizable terminal that lets value-added resellers and OEM system integrators cost-effectively select the exact features for any end-user application. The Genisys terminal is built around the Wedge, a wedge-shaped platform containing all 80188-based logic and firmware. Key to the platform's functionality is an internal architecture flexible enough to accept different microprocessors and logic cards.

Starting with the Wedge platform, OEMs select the emulation options, peripheral interfaces, keyboard layouts, and numerous other options that tailor the terminal to a given task. As a result, OEMs need no longer stock large, costly custom terminal systems. As off-the-shelf components, the family of keyboards, monitors, and logic modules that makes up the Genisys system are completely interchangeable.

Standard features of the Wedge platform include an interface for VGA standard monochrome or color monitors, a 60/70-Hz refresh rate, a 10-by-15-character cell, 8-by-11-dot characters, and 80- and 132-column display modes. In addition, the platform offers four ROM-based character fonts, two soft-character fonts, and international-character fonts. The system handles baud rates up to 38.4 Kbaud and can display a box, block, or underline cursor. Three RS-232 I/O ports serve peripherals.

Features for a given application can include touch screens, bar codes, cash drawers, swipe readers, light pens, integral modems, fiber optics, local-area network capabilities, and more. The terminals can be linked to multiple hosts and/or a PC concurrently.

Depending on volume, pricing to OEMs can be as low as $340 for the Wedge-based platform and up to $965 for a fully-configured Genisys with enhancements. Demonstration units are slated for first-quarter shipment.

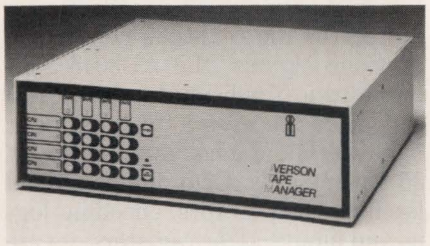
Zentec Corp., 2400 Walsh Ave., Santa Clara, CA 95051; (408) 727-7662. **CIRCLE 314**

SYSTEM COMBINES CACHE, DISK, SOLID-STATE MEMORIES

Combining disk, cache, and solid-state memories, the Model 9200 Mass Storage Subsystem is a high-performance plug-in compatible for the Unisys 1100/2200 Series system. This high-capacity storage unit features a dual-access controller, two to eight I/O-channel attachments, up to 32 Gbytes of unformatted disk storage, and up to 2.3 Gbytes of semiconductor memory for cache disk or solid-state disk operation. It is packaged in an attractive 2- by 3- by 5-ft. cabinet.

Amperif Corp., 9232 Eton Ave., Chatsworth, CA 91311; (818) 998-7666. From $175,000. Availability is 90 days. **CIRCLE 315**

DIGITAL SWITCH LETS CPUS SHARE TAPE DRIVES

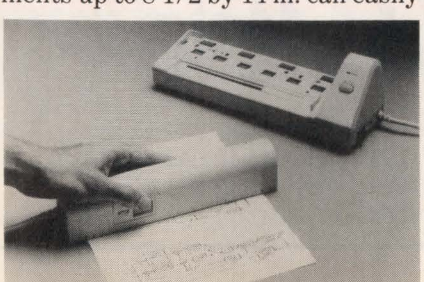


As a solution for the problems surrounding the multi-CPU environment, the Iverson Tape Manager (ITM) is an electronic digital switch that allows for the configuration of multiple tape drives between multivendor CPUs. By reducing the number of tape drives that are needed, efficiency and productivity are improved, while at the same time production cost is reduced. The ITM lets different CPU manufacturers, such as Sun, DEC, Data General, and IBM, share tape drives. Sixteen different configurations can handle up to eight CPUs and four tape drives. Upgrading the system means simply adding new boards.

Iverson Inc., One Saunders Ave., San Anselmo, CA 94960; (415) 459-5665. From $1950. **CIRCLE 353**

SCANNER CHANGES TEXT INTO MACHINE-READABLE DATA

A high-resolution, hand-held scanner lets users convert their source documents in the form of photographs, illustrations, graphics, and text into machine-readable data that can be manipulated by popular desktop-publishing programs running under MS-DOS-based systems. Called the Omniscan, the lightweight data-input device can read text at a rate of 10 seconds per page. Input resolution is 200 dots/in. Documents up to 8-1/2 by 14 in. can easily be handled. Two different modes accomodate either text or graphics. The scanner also accomodates most desktop publishing systems, including those that require a facsimile board.



NCL America Computer Products Inc., 1221 Innsbruck Dr., Sunnyvale, CA 94089; (408) 734-1006. $1290. Available immediately. **CIRCLE 354**

IBM-COMPATIBLE TRACK BALL REPLACES MOUSE

Designed specifically for use with IBM PCs, the RB2/CAD-6 Track Ball incorporates all the hardware and software that is needed to ensure compatibility with Microsoft mouse devices. The fixed-desk-position track ball needs a minimum amount of operating space, just 20% of the space that is required for a mouse. Interfacing with the PC's serial port, it gives the user total freedom for fast or slow operation, and has zero drift. The benefits can be seen in graphics programs, word processing, CAD/CAM and CAE, and menu-driven programs.

Marconi Electronic Devices Inc., 45 Davids Dr., Hauppauge, NY 11788; (516) 231-7710. From $198. Available from stock. **CIRCLE 355**

Fastest Monolithic Sample-and-Hold Amplifier Acquires Data in 1 μs

The speed and accuracy that today's data-acquisition systems demand is embodied in the AD684 monolithic quad sample-and-hold amplifier from Analog Devices. Sampling at rates near 100 ksamples/s with true 12-bit performance, each channel of the amplifier guarantees a maximum acquisition time for a 10-V step at 600 ns to within 0.1% and 1 μs to within 0.01%.

The four biMOS sampling channels, complete with internal hold capacitors, are independently controlled. Their key application is in multichannel data-acquisition systems using high-speed analog-to-digital converters. Motor-control and instrumentation applications will also gain from the amplifier's ability to operate in sequential, simultaneous, or random sampling modes.

Maximum nonlinearity of 0.005% full scale is up to 20 times better than that of existing quad sample-and-hold amplifiers with 10-bit performance at best. Besides saving space, the AD684 amplifier is up to three times faster, is more reliable, runs cooler, and has lower total harmonic distortion and a higher signal-to-noise ratio than roll-your-own solutions using four single amplifiers. For simultaneous sampling, because interchannel timing compensation is not needed, the AD684 amplifier's entire error budget is completely encompassed in a 300-ps guaranteed maximum aperture offset between channels.

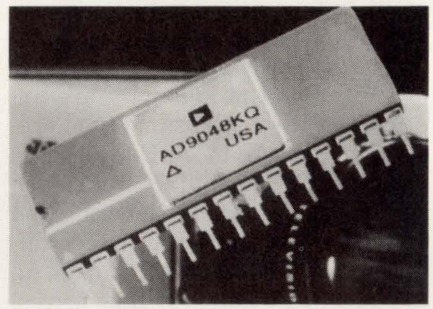
A proprietary error-correcting architecture compensates for hold mode errors and ensures accuracy and repeatability over temperature. Hold characteristics include a maximum 500-ns settling time and aperture uncertainty (jitter) of 200 ps.

The device comes in a 16-pin skinny DIP, operates from ±12-V supplies, and dissipates a maximum of 530 mW. Prices begin at $23.50 in quantities of 100, with sample quantities available from stock. Production quantities are delivered in 6 to 8 weeks.

Analog Devices Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106; (617) 329-4700. **CIRCLE 337**

Flash ADC Combines High Speed, Wide Bandwidth

Suited for the real-time conversion of video signals, the AD9048 8-bit monolithic flash analog-to-digital converter features a 10-MHz input bandwidth and a conversion rate of 35 Msamples/s. Containing strobed latching comparators, encoding logic, and input buffer registers, its applications include military instrumentation, and digital-radio, electro-optic, and medical equipment. The TTL-compatible device has a settling time to 8-bit accuracy of 20 ns after a



full-scale input. Many packaging options are available as well as different operating ranges and accuracy grades.

Analog Devices Inc., One Technology Way, Norwood, MA 02062; (617) 329-4700. From $20 in quantities of 100. Samples are available from stock. **CIRCLE 338**

CIRCLE 83

1-GHz GaAs Fiber-Optic Receiver Sports High Sensitivity, Linearity

A highly responsive 1300-nm photodetector and a monolithic gallium arsenide transimpedance amplifier with excellent sensitivity and linearity are featured in a fiber-optic analog receiver from Anadigics. The AAR10010 is a 10-kHz-to-1-GHz pigtailed receiver, and is the first of several hybrid integrated optoelectronic products featuring gallium arsenide ICs the company is planning.

The device offers a wide dynamic range, a 62-dB carrier/noise ratio, +18-dBm third-order intercept, and −75-dBc third-order harmonic distortion. The receiver can accept up to a −4-dBm input level and can operate in digital links up to 1.6 Gbits/s.

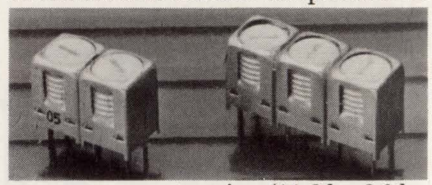
Typical applications for the part include CATV fdm/am and fdm/fm supertrunks and backbones. Other uses include telephone-company subscriber loops, supercomputer-peripheral links, clock-distribution networks, gigabit/second local-area networks, intracomputer links, radar-to-CPU links, high-resolution graphics, secure voice/video-communication links, test instruments, and radar/video remoting.

Future devices in the company's hybrid optoelectronic line will include digital receivers operating in excess of 1.6 Gbits/s, and models with clock and data-recovery capabilities. The AAR10010 fiber-optic receiver is available in a pigtailed 14-pin DIP with 50/125 multimode fiber and an ST connector. Other options are available. The device goes for $2500 in small quantities. Delivery is in 6 to 8 weeks.

Anadigics Inc., 35 Technology Dr., Warren, NJ 07060; (201) 668-5000. **CIRCLE 339**

Helical Filters Housed In Compact Case

Designed for communication devices operating in the frequency range of 350 MHz to 1.5 GHz, the 5HW double-tuned and 5HT triple-tuned helical filters are well-suited for paging receivers and cellular telephones. In

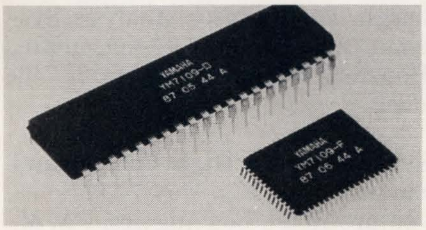


a very compact casing (11.2 by 6.0 by 9.5 mm), the filters feature an adjustable, screw-type core. They are designed to withstand vibration, shock, temperature change, and high humidity. Input impedence is 50 Ω.

Toko America Inc., 1250 Feehanville Dr., Mt. Prospect, IL 60056; (312)297-0070. From $6. Delivery takes four to six weeks. **CIRCLE 340**

SPEEDY SINGLE-CHIP MODEM OPERATES AT 9600 BITS/S

The YM7109 single-chip modem operates at 9600 bits/s. This low-cost CMOS device adheres to all industry standards. It runs off of a 5-V supply and consumes only 300 mW of power. The chip contains both serial- and parallel-port interfaces. Its features include a scrambler and descrambler, built-in programmable double-tone generation, programmable tone detection, and a transmission filter to reject out-of-band frequencies (0 to –15 dB). The chip is packaged in a 40-pin DIP or a 64-pin quad flatpack.



Yamaha Corp. of America, Systems Technology Div., 6600 Orangethorpe Ave., Buena Park, CA 90620; (714) 522-9223. $95 to $97 in quantities of 100. **CIRCLE 341**

DIGITAL TRANSMITTER ENHANCES AUDIO QUALITY

A 14-bit digital program channel sends high-quality audio signals over long-distance telephone lines. The DPC 15 converts the audio signal from analog into a digital form for transmission. This eliminates all the distortions and line losses associated with analog audio transmission. The system can also be connected in pairs to transmit audio signals in stereo form.

Coastcom, 2312 Stanwell Dr., Concord, CA 94527; (800) 433-3433 or (415) 825-7500. Available immediately. **CIRCLE 342**

HAYES-COMPATIBLE MODEM FITS IN YOUR POCKET

With the dimensions of 75 by 55 by 25 mm, the V22 Stradcom modem easily fits into your pocket. Powered by a single 9-V battery, the modem plugs directly into any standard 25-pin RS-232 connector. This makes it suitable for use with virtually any laptop or desktop computer. Despite its small size, it carries the same features as its slot-installed equivalent. It offers full Hayes compatibility and operates at baud rates of 1200 and 300 full duplex, and conforms with CCITT levels V22 and V21. Its features include auto-dial and answer and a built-in speaker used for call monitoring.

Dataflex Design Ltd., Merton Park House, 2 Jubilee Way, South Wimbledon, London, England SW19 3XD; 01-543 6417.

CIRCLE 343

UPCOMING MEETINGS

MARCH

Applied Power Electronics Conference and Exposition, March 13-17. Baltimore Convention Center, Baltimore, MD. APEC '89, 655 15th St., N.W., Ste. 300, Washington, DC 20005; (202) 639-4990.

Mid-lantic Electronics Show, March 21-22. Valley Forge Convention Center. Judith Ginsberg, Show Manager, 4113 Barberry Dr., Lafayette Hill, PA 19444; (215) 828-2271.

APRIL

InvenTech Expo Conference, April 2-4. Anaheim Convention Center, Anaheim, CA. Bailey Beeken, Edgell Expositions, 50 Washington St., Norwalk, CT 06854; (203) 853-0400.

Digital Signal Processing: Single-chip DSP Processors, Theory, Design, and Application, April 3-5. Massachusetts Institute of Technology, Cambridge, MA. Amnon Aliphas, DSP Associates, 18 Peregrine Rd., Newton, MA 02159; (617) 964-3817.

Commercially Available RISC Processors, April 5-7. Massachusetts Institute of Technology, Cambridge, MA. Amnon Aliphas, DSP Associates, 18 Peregrine Rd., Newton, MA 02159; (617) 964-3817.

Advanced Materials and Copper Conference, April 10-11. Orlando, FL. Nancy Binkley, International Society for Hybrid Microelectronics, P.O. Box 2698, Reston, VA 22090-2698; (703) 471-0066.

Electronic Imaging Conference West, April 10-13. Pasadena Convention Center, Pasadena, CA. MG Expositions Group, 1050 Commonwealth Ave., Boston, MA 002215; (617) 232-3976.

NCGA '89, April 17-20. Philadelphia Civic Center, Philadelphia, PA. National Computer Graphics Association, 2722 Merrilee Dr., Ste. 200, Fairfax, VA 22031; (703) 698-9600 or (800) 225-NCGA.

Southern California ISHM '89, April 18-19. Anaheim Marriott, Anaheim, CA. Nancy Binkley, International Society for Hybrid Microelectronics, P.O. Box 2698, Reston, VA 22090-2698; (703) 471-0066.

PCB Expo '89, April 26-27. Kenginston Close Hotel, London, England. Donna Esposito, PMSI, 1790 Hembree Rd., Alpharetta, GA 30201; (404) 475-1818.

MAY

International ANSYS® Conference and Exhibition 1989, May 2-4. Pittsburgh Hilton and Towers, Pittsburgh, PA. Swanson Analysis Systems, Inc., P.O. Box 65, Johnson Rd., Houston, PA 15342-0065; (412) 746-3304.

Symposium on High Voltage and Smart Power ICs, May 7-12. Bonaventure Hotel, Los Angeles, CA. M. Ayman Shibib, AT&T Bell Laboratories, P.O. Box 13566, Reading, PA 19612-3566; (215) 939-6576.

Parallel CFD Conference, May 8-9. Los Angeles, CA. Lynn McDaniel, AlTek, 8321 N. Woolsey, Portland, OR 97203; (503) 289-7735.

EuroBus/Germany, May 9-10. Munich Sheraton Hotel, Munich, Germany. Anne Weber, MultiDynamics, Inc., 13762 Newport Ave., Ste. 204, Tustin, CA 92680; (714) 669-1210.

DEXPO South '89, May 9-11. Atlanta Market Center, Atlanta, GA. Expoconsul International, Inc., 3 Independence Way, Princeton, NJ 08540; (609) 987-9400.

ISE '89, May 16-18. Convention Center, Albuquerque, NM. Vic Myers, Ideas in Science & Electronics Inc., 8100 Mountain Road NE, Ste. 207, Albuquerque, NM 87110-7822; (505) 262-1023.

Thermographic Applications, May 23-25. St. Louis, MS. JS&A, 17 First Ave., Montpelier, VT 05602; (802) 229-9820.

2,7 VS. 1,7 RLL CODE

Dear Editor,

It is a rare occasion when I read an article concerning disk drives in a general-purpose trade publication such as yours that doesn't contain one or more inaccuracies. Generally, I simply grimace and let it pass, but your product report on 5.25-in. drives *(November 10)* contained a statement that is so completely contrary to fact, I feel compelled to respond.

The article states that in converting from 2,7 RLL code to a 1,7 RLL code, data windows are expanded. Assuming capacity remains constant, this is true. The article then ascribes this sudden windfall to the fact that there is less intersymbol interference. In fact, greater intersymbol interference (a.k.a. pulse crowding) is the penalty that must be paid for the increased window size! An example will illustrate the point.

Assume a drive transfers 10 Mbits/s at the interface. A 1,7 encoder maps 2 data bits into 4 encoded bits, so data is written on the disk at a 20-MHz clock rate. The data window is thus 1/20 MHz = 50 ns. With a 2,7 code, there are at least 2 zeros between each one, so there are 150 ns between flux reversals. A 1,7 encoder maps 2 data bits into 3 encoded bits, so data is written on the disk at 15 MHz. The window size is 66.6 ns. In 1,7 code, there are as few as 1 zeros between ones, so flux reversals can be only two windows, or 133.3333 ns apart. The closer the peaks are spaced, the more they will interfere with each other.

The other misstatement in the article occurred in the same paragraph. The sentence seems to imply that signal/noise ratios are a consequence of intersymbol interference. This is not true. Noise-induced bit shift and bit shift induced by pulse crowding are two relatively independent causes of read-channel errors.

Other than this, you are to be congratulated for a thorough, informative article.

Robert Wickberg
Sr. Engineer
Miltape Corp.
Springfield, VT 05156

IBM SETS THINGS STRAIGHT

Dear Editor,

The article entitled "IBM to support open-token foundation" contained two errors. First, IBM has not made a decision at this time to join or support the Open Token Foundation. IBM is currently evaluating the opportunity to join the organization and will announce its decision soon.

Second, your statement "...until now the Armonk, N.Y., company has not participated in the process of setting the IEEE 802.5 standards, sharing research and development information, or projecting future direction for Token-Ring Networks" is completely inaccurate.

On the contrary, IBM has participated extensively in IEEE Project 802 since its inception. IBM has chaired the Token-Ring committee since its formation, contributing significantly to the 802.5 committee's standards-setting work. In addition, IBM has shared with the technical community and published extensive research and development information. Many computer-equipment companies have used the published specifications for IBM's Token-Ring adapter to build compatible products. And not only has IBM published specifications of at least five programming and hardware interfaces to it, but also conducted worldwide education courses on the Token-Ring hardware and software after its 1985 introduction.

Donald E. Frischmann
Director, Information
IBM Corp.

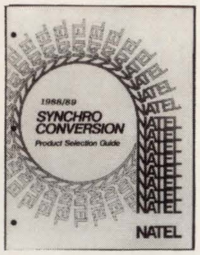
CREATIVE DISOBEDIENCE

Dear Editor,

This morning my supervisor distributed throughout our department a copy of your editorial *(Dec. 8, 1988)* entitled "Creative Disobedience." We have been in a similar situation for some time now. Our industrial business unit is only a small portion of our company. Therefore it seems as though our product ideas are not given priority by our management. We do have some mature and well-established products. However, until recently, custom engineering con-

(Continued on p. 158)

SYNCHRO-CONVERSION PRODUCTS CATALOG



In 24 pages and two colors, this catalog serves as a synchro-conversion products selection guide. The catalog covers synchro/resolver-to-digital converters, digital-to-synchro/resolver converters, and synchro/resolver components and instruments, including a synchro/resolver simulator.

Natel Engineering Co. Inc., 4550 Runway St., Simi Valley, CA 93063; (805) 581-3950. **CIRCLE 344**

COMPLETE LINE OF MILITARY PRODUCTS

Containing data sheets and other pertinent information on Teledyne Semiconductor's complete line of military products, the *Military Data & Design Handbook* lists all of the company's devices that comply with MIL-STD-883. These CMOS devices are the same as the standard commercial parts with the exception that they meet military specifications.

Teledyne Semiconductor, 1300 Terra Bella Ave., Mountain View, CA 94039; (415) 968-9241. **CIRCLE 345**

SOLUTIONS TO DATA-ACQUISITION PROBLEMS

Introducing new solutions to the problems in the areas of real-time data acquisition and control on the Macintosh, a 56-page color catalog gives designers numerous posibilities, using both hardware and software. Aside from product descriptions, the catalog includes technical specifications and application notes on the company's comprehensive MacADIOS family of data-acquisition and control hardware, software drivers, and applications software.

GW Instruments Inc., 35 Medford St., Somerville, MA 02143; (617) 625-4096. **CIRCLE 346**

COMPLETE LINES OF IC SOCKETS AND CONNECTORS

Containing everything the designer could need as far as IC sockets and connectors are concerned, this catalog features 63 pages of products. Most of the items contain precision machined pins and multifinger spring contact for highly reliable connections. Nearly all of the products shown in the catalog are manufactured domestically and are available from stock.

Mill-Max Mfg. Corp., 190 Pine Hollow Rd., Oyster Bay, NY 11771; (516) 922-6000. **CIRCLE 347**

Moving Up Without Changing Jobs Requires Enthusiasm And Time

Technical recruiter John Morganto calls them "tree-huggers"—the engineers who shun job hopping and actually enjoy their work. While many engineers perceive a job switch as the best way of getting attention and moving up in prestige and pay, this may not be necessary in a supportive company environment *(see "Are you a tree-hugger?" p. 158).* The tree-huggers are typically those who've found a company they like and want to invest their career in. On the other hand, they don't want to earn the same salary for the rest of their lives. What are the secrets to getting ahead in your own company?

If there's one fundamental, it's initiative. As one human-resources director phrased it, "The individual perceived as being enthusiastic and expert, who learns quickly, is potentially more likely to be recognized than someone perceived as a dull plodder."

"It takes initiative and intellectual capability," advises one Motorola engineer."You have to be able sort the good ideas from the not-so-good ideas, to be able to turn somebody's idea into a practical concept. It doesn't have to be your own idea, and it doesn't have to be a new idea. Most of the ideas in electronics were developed in the 1930s and 1940s, anyway. The whole industry—especially the microprocessor and digital fields—is driven by decreasing product cost over time. If you can figure out how to implement ideas, turn something that some professor has shown is possible into a practical product that will bolster your reputation."

But be aware: Any strides you take to get ahead are going to be on your own time. "You have to be aggressive enough to pursue it on your own dime," says Gary Lopes, an engineering manager. "I've always taken a personal interest in the business itself, to the point of taking on responsibility on my own, only to have it be recognized later by my supervisors." He continues, "The one thing that helped me was helping my supervisor with tasks he normally would be responsible for. Now that's what I look for in people who report to me. How much do I have to interface with someone on a particular task? Can I assign that task to someone who will literally disappear until it's done, correct, and complete?"

I HELPED MY SUPERVISOR WITH HIS TASKS. NOW THAT'S WHAT I LOOK FOR IN PEOPLE WHO REPORT TO ME...CAN I ASSIGN A TASK TO SOMEONE WHO WILL LITERALLY DISAPPEAR UNTIL IT'S DONE, CORRECT AND COMPLETE?

For better productivity when you're stuck on a problem, one engineer recommends asking someone to put you on the right track "rather than sitting around for two days trying to reinvent the wheel. Invent where it's necessary and make use of what's known when you can." Lopes agrees—to a point. "One thing that irritates me is when an engineer walks into my office with a problem and expects me to have some golden answer. I prefer an engineer to come in, acknowledge there's a problem, put forth a couple of options for solving it, and ask for my input. I manage a resource, and my resources are engineers. I treat each manager as his own separate manager of a group of tasks."

There are other ways to be visible, of course. Rob Gilmore was the ninth employee on the totem pole at Qualcomm, the San Diego firm where he's now engineering director. He'd worked with the founders for six years previously. He says, "The key to my getting ahead was being put to work on a group of proposals, which is very visible to upper management. If you win a few of those jobs, they regard you highly, because it's a combination of engineering and marketing skills." He adds, though, that to win such recognition is unfair in some cases. "To me, it's not necessarily the hardest work. Designing a circuit so you're going to build 10,000 of them and getting it to work is much harder than the Fantasyland of writing a proposal. You can make it sound great, but you don't have to build it."

It's just as important to be visible to coworkers. The word to remember is teamwork. As one engineer climbing a technical ladder within his company put it, "It's not only essential that I be innovative, but also that I'm perceived by my peers as an innovator—because progress on the technical ladder is governed by peer recommendations."

"It's a two-edged sword," acknowledges Qualcomm's Gilmore. "There are a lot of interruptions during the day," he laments, "and I find it hard to say no when people ask me to help. Also, you tend to learn from them when you help, so those interruptions can be good. But when people divert you to their projects—even though it may be more fun at the time—it can take time away from what you're focusing on."

Part of teamwork is having and exhibiting a positive attitude. "Say, you go into a meeting," explains Gary Lopes, "and half of the group says you can't do something because it's impossible or there's a technical problem or Joe Schmo's group won't help. If the other half of the group says that they'll find another way, that's impressive. Having the drive to work around issues

ARE YOU A TREE-HUGGER?

Before you decide whether or not your company is the one you want to stay with, you have to answer some questions. As Terrence Deal and Allan Kennedy ask in their book *Corporate Cultures*, "Who gets ahead? If all important positions are filled by ex-salespersons, then it's pretty clear what the culture believes in and values."

"Take stock and make sure you're in the right environment, that management philosophy is what you want it to be," suggests recruiter Ben Garfinkle. Recruiter Julie Kramer concurs, "It's always a good idea to know what one's strengths and limits are before deciding what to pursue. If what you really enjoy is getting down to bits and bytes, aspire to advance in the technical arena." She adds that, happily, it's not always necessary to join management to advance. "More companies are extending the career ladder in technology. There used to be an invisible barrier at $50,000. No matter what you're skills were, you couldn't go beyond it and stay technical. But companies are recognizing that certain technical skills are extremely valuable and hard to find, and they're willing to move the ladder up for technical people."

is important."

Personnel recruiter Julie Kramer echoes this sentiment: "Companies look for leadership skills, problem-solving skills, people skills. People skills might include either vendor relations or negotiating skills. In the interpersonal area, for instance, problems always crop up. It's the people who can solve those problems who tend to be recognized and thought of for advancement." Kramer tells how a departmental rivalry was quashed when a young staffer took someone from the other group out to lunch to get their side of the story. He went back to his own group and suggested a compromise that shortened the work schedule for both departments. Managers recognize that kind of skill.

Once you prove yourself to your coworkers—or, better yet, while you're doing so—make yourself known to other potential decision makers. Many companies post jobs. "If the process is not that overt," advises John Morganto, "you have to conduct an indirect sales process to make yourself known to people in other divisions. Network within the organization, whether for career planning or technical curiosity." Morganto also recommends outside activities to meet colleagues—professional societies like IEEE and ASME, continuing-education courses, user and hobby groups, for instance.

Cultivate the sales force. They're the ones who learn first what customers want and need. Keep track of what your competitors are doing, so you can suggest to your superiors that you do the same. Technical journals are a good way to do this.

As distasteful as it may sound, blowing your own horn is one of the keys to advancement. Recruiter Ben Garfinkle notes, "A salesman will come straight out and say, "Look, buddy, I brought you $6 million in contracts—what are you going to do for me?" Engineers haven't learned how to do that. They keep abreast of technology; they make valuable contributions; they're credited for patents; but they won't talk about it. You don't have to be arrogant. Something along the lines of 'I'm glad to have made this contribution, but I want to be recognized for it' will do."

"People who go the extra mile get promoted," says Kramer, "but people at the other extreme turn people off. A person who's nicely balanced is most impressive—someone who's willing to make the extra effort, to cooperate with people, to help figure out what their needs are and solve their problems."☐

HOWARD BALDWIN
VNU Publications

(Continued from p. 155)

tracts have been our department's main engineering concern. Now, due to our increasing overhead costs, we are trying to convince management to redirect our effort toward product design.

Unfortunately, our current "product" line had very small NRE (nonrecurring engineering) charges. As we try to expand our product line, we are expected to repeat history. That is not to say that our current products were not technically challenging. It's simply that they were designed and developed "underground" using a method similar to your "Creative Disobedience." Management has the attitude that since we did it then, surely we can do it now.

History here has also shown that this "underground" effort has been profitable, although not necessarily to the design engineering team. Our efforts, however noble, result in a 4% average increase in annual salary to the engineers. In addition to designing products on our time and at our expense, we are expected to meet schedules and be profitable for "approved" programs. This alone requires at least 40 hours per week of devoted effort. Those of us with family responsibilities find it difficult to justify this much dedication when we receive no additional compensation. Where is the incentive?

Unfortunately, your editorial supports my suspicion that this situation is becoming an industry trend. "Creative Disobedience" is not the answer. I will continue to search for a fair and viable compromise between engineering and management.

Anonymous

Editor's comment: We agree that management cannot expect extra-hours "underground" development efforts from engineers. The company cited in the editorial, for example, now has a bonafide standard-product program.

Although our policy is to not publish anonymous letters, the comments in this letter are important enough to all engineers' well-being to justify publication.

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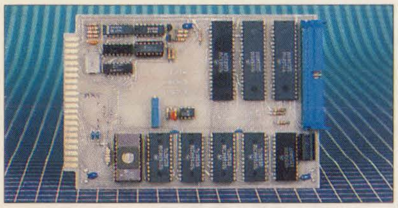

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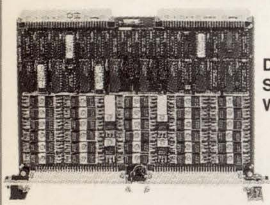

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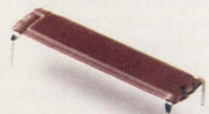

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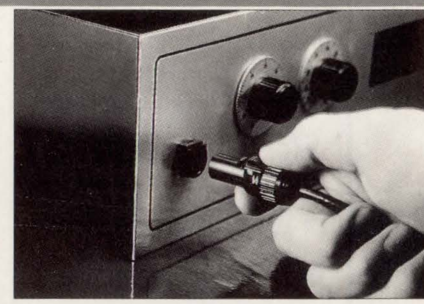

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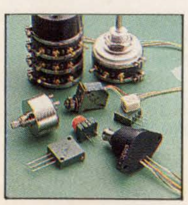

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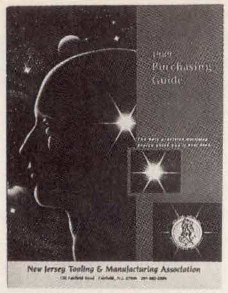

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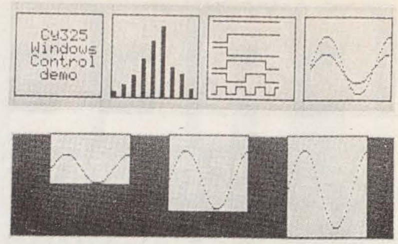

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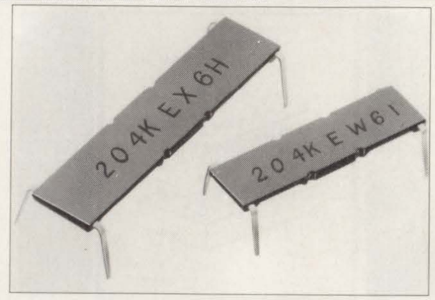

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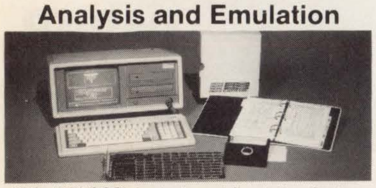

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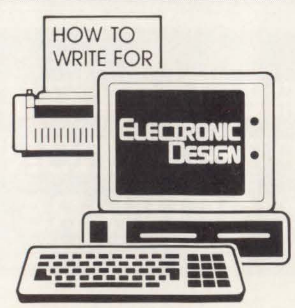

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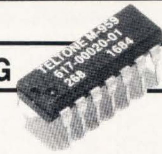

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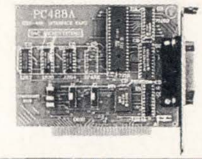

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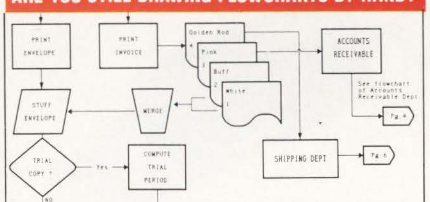

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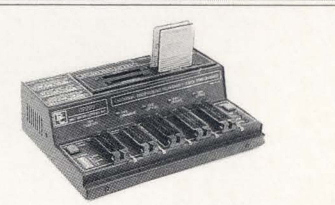

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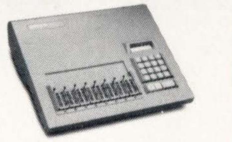

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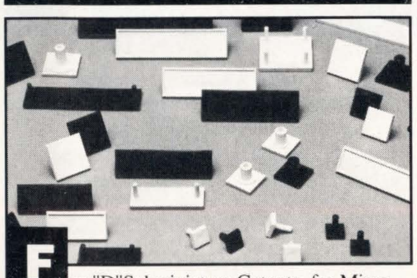

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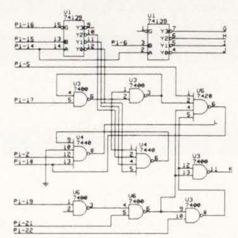

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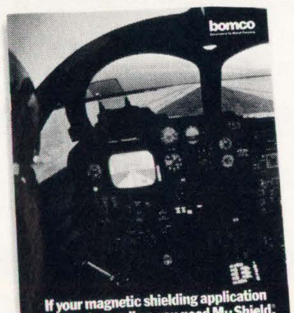

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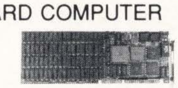

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