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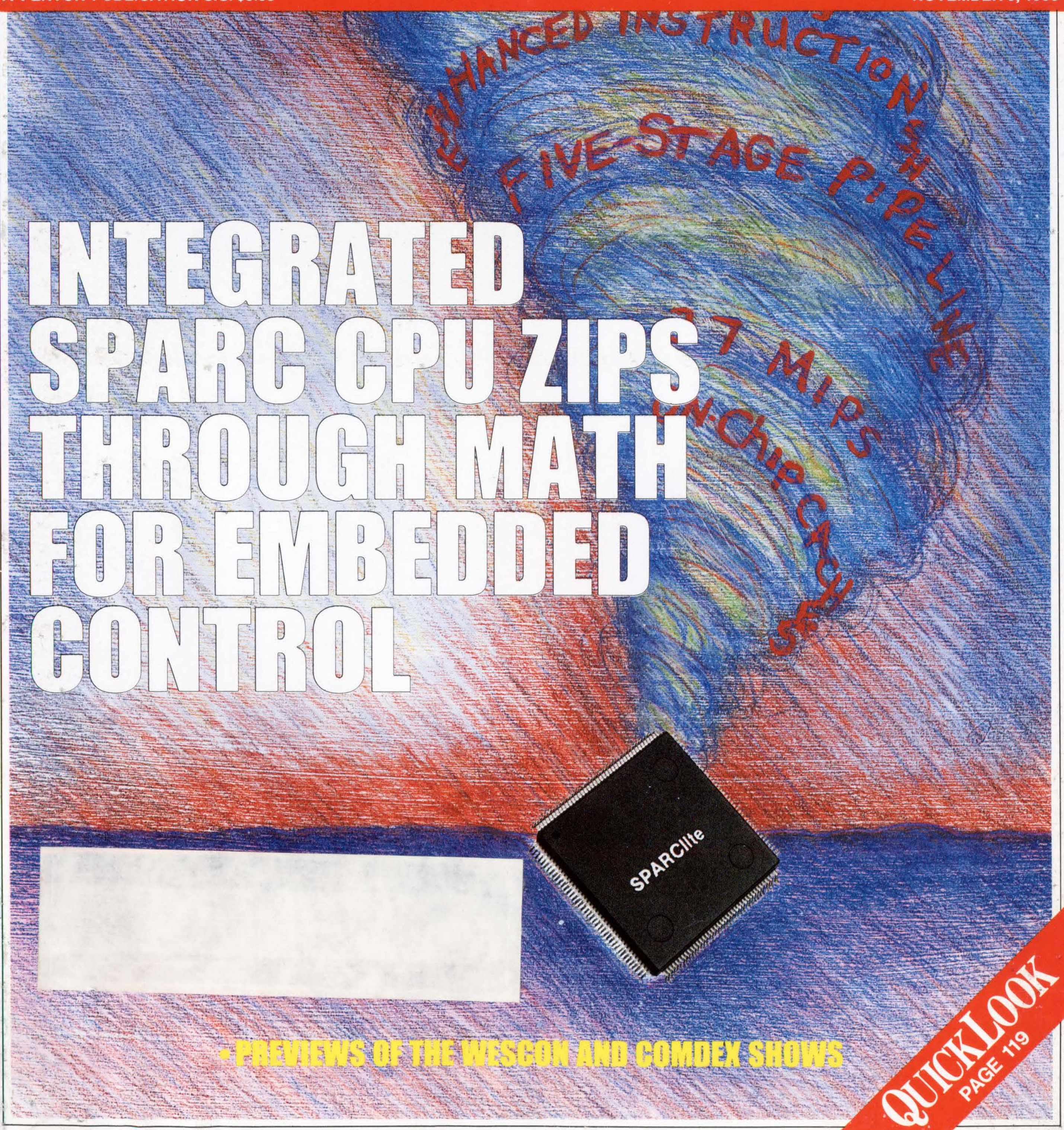

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QUICKLOOK PAGE 119

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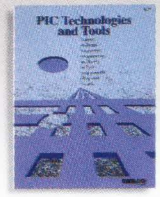

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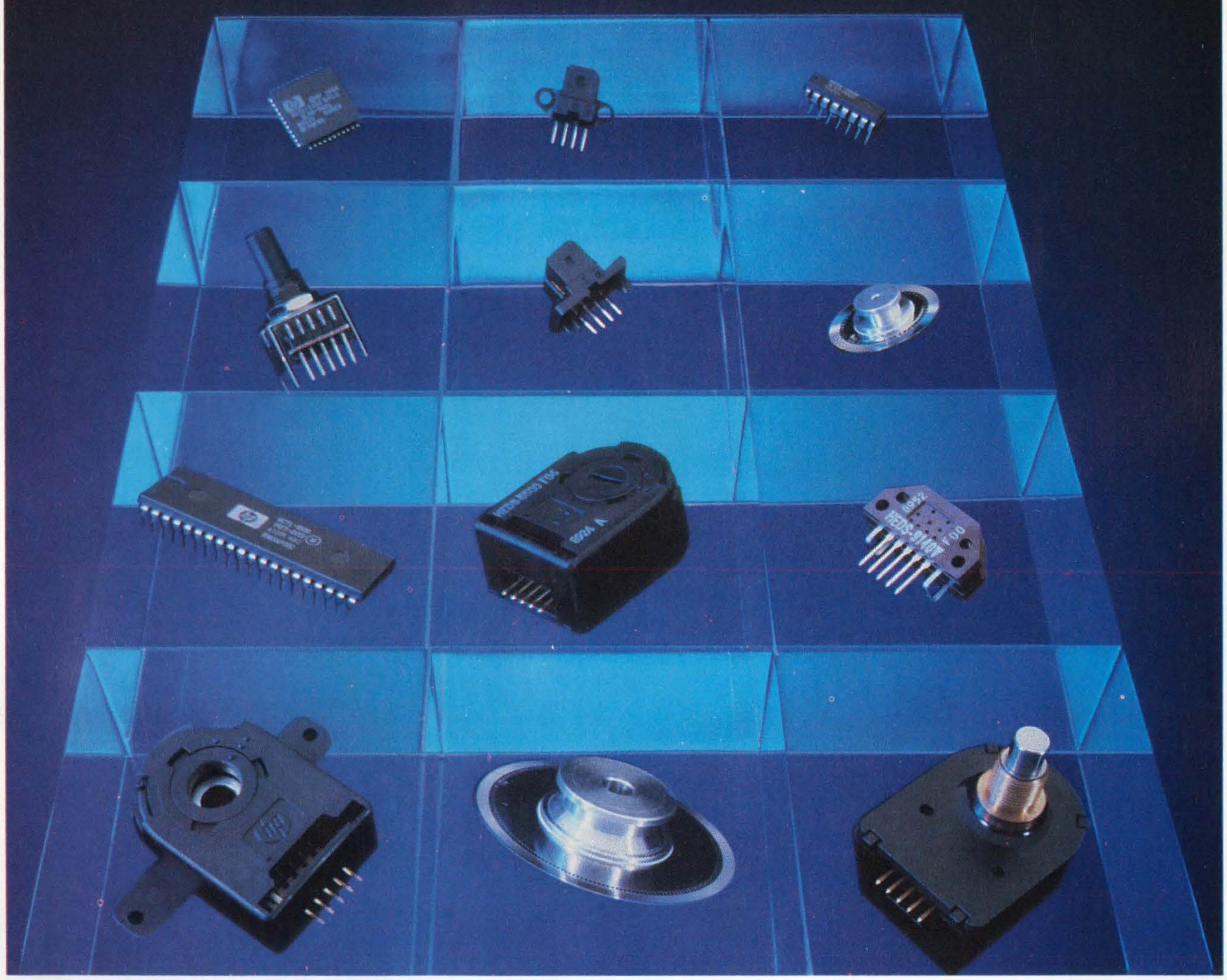
Control Tower



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NOVEMBER 8, 1990 VOL. 38, NO. 21

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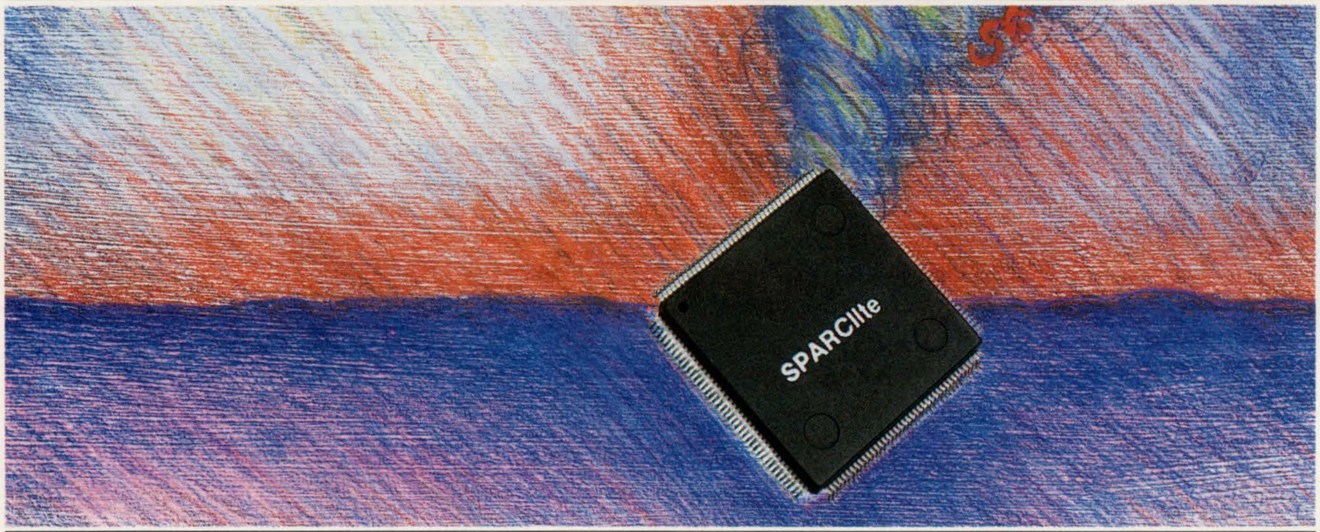

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- Special Report: Image processing—adapting PCs for multimedia applications
- A preview of semiconductor advances disclosed at the International Electron Devices Meeting
- First details on new CASE and simulation tools
- Building analog behavioral models in six easy steps
- Measure PLL open-loop response—with the loop closed
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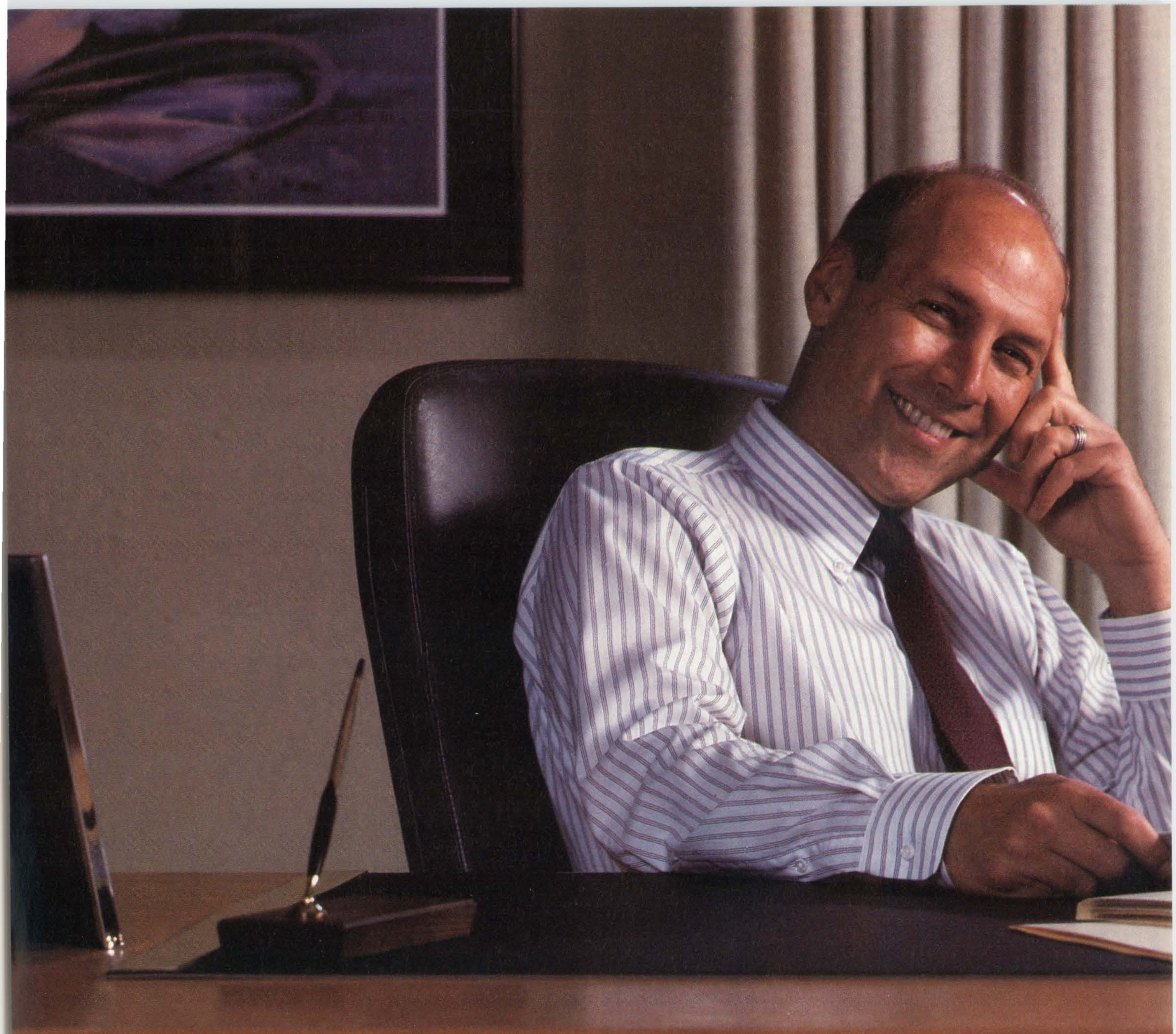
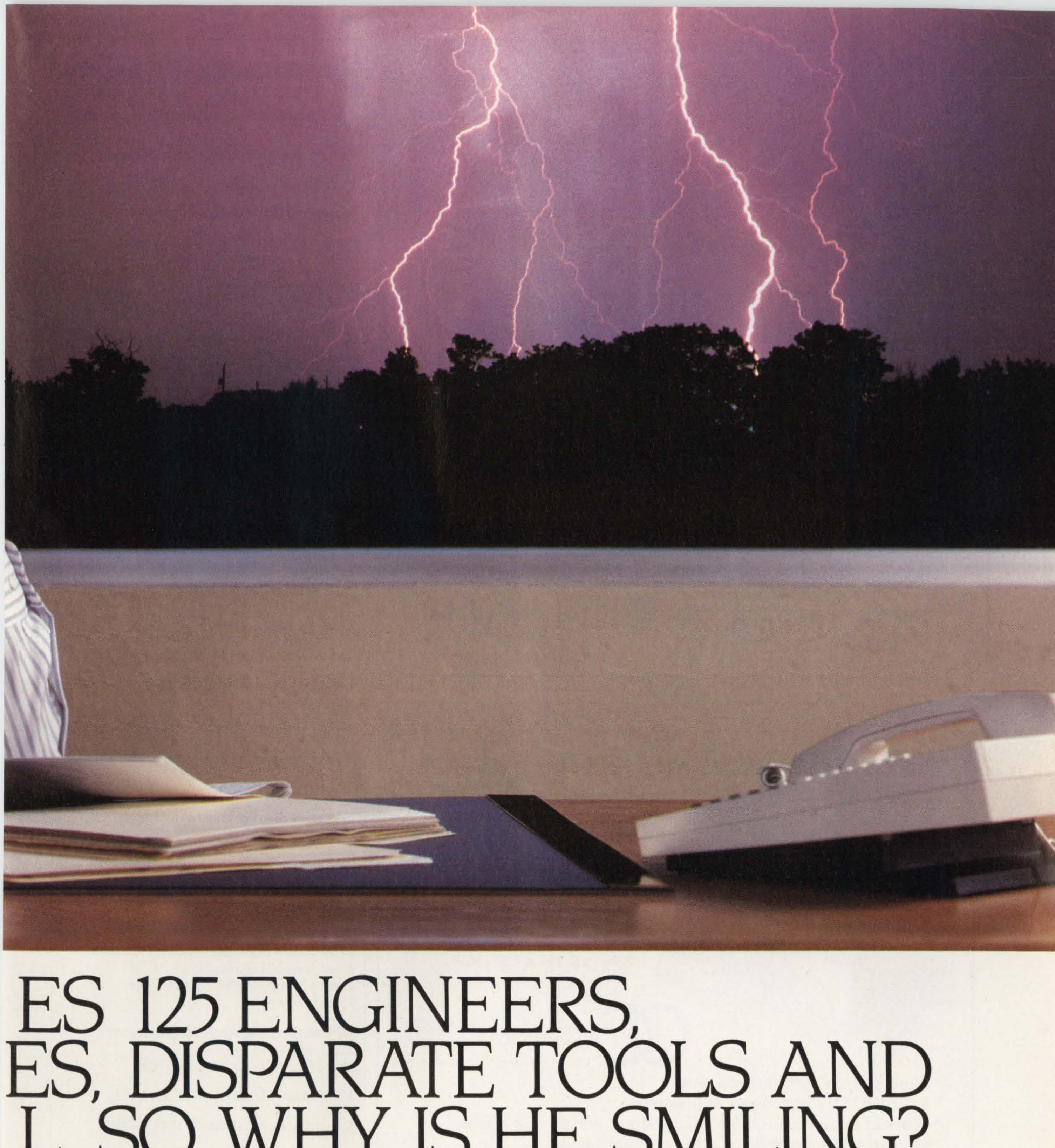


THIS MAN MANAG MULTIPLE DESIGN DISCIPLIN DEADLINES THAT COULD KIL

The dilemma rears its ugly head time and time again. Do the impossible. By tomorrow. Worse yet, do it with an intimidating hodge-podge of design automation tools and data formats. And while you're at it, make sure all these tools and data play together freely and efficiently. No problem. Right?

To avoid this kind of chaos, you need to consider a fundamental change in your engineering strategy. Which is why we now offer you our Concurrent Design Environment.™

Simply put, the Concurrent Design Environment allows tools from virtually any source to work together. Within it, our new Falcon Framework™ lets you assemble precisely the design automation environment your situation requires — without sacrificing the considerable benefits of integration. And our OpenDoor℠ program ensures that your choice of tools includes the best the entire industry has to offer.



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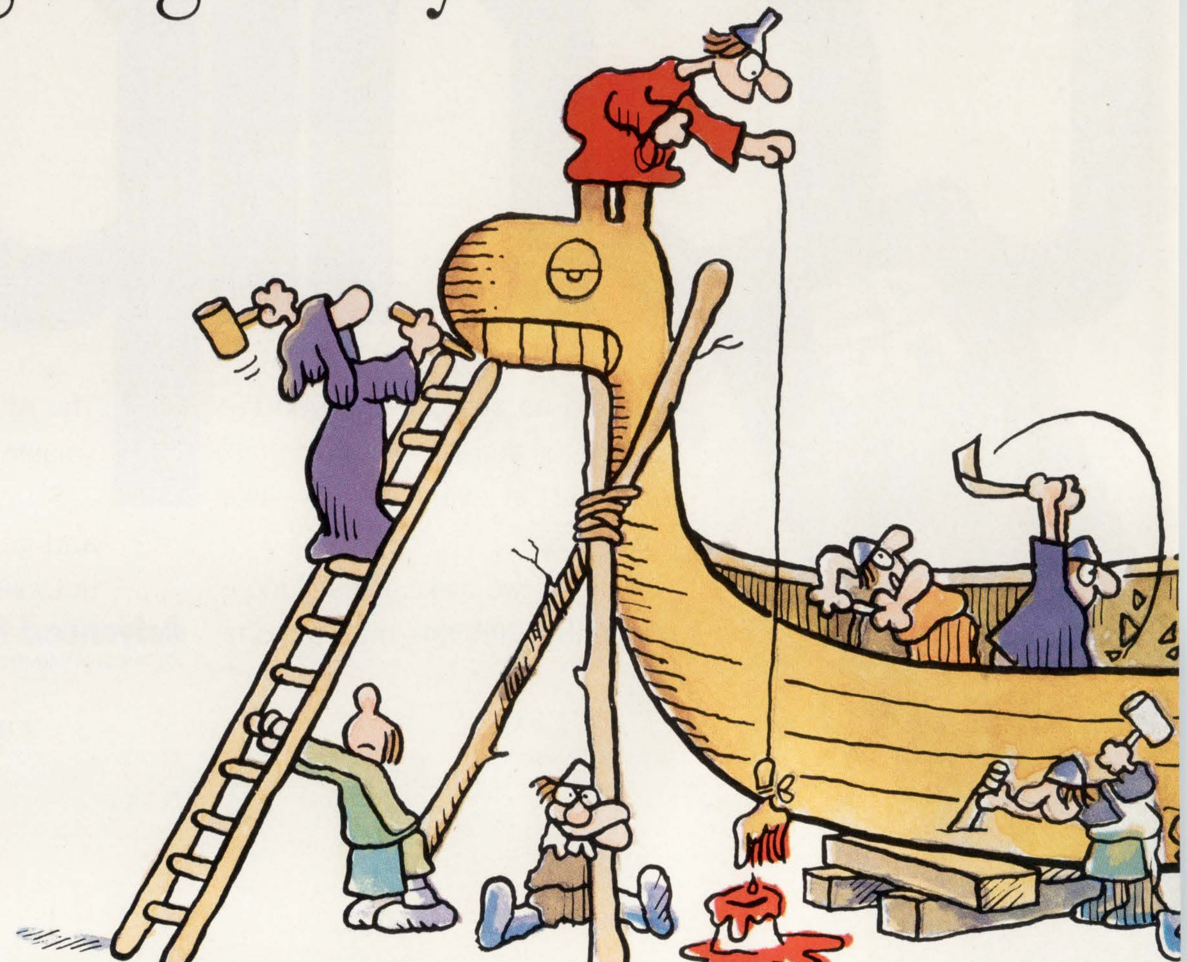
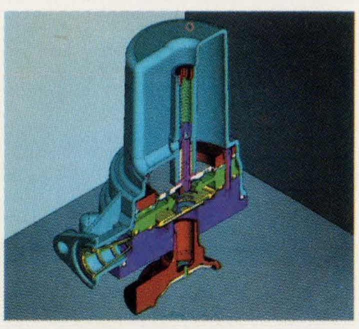
The IBM RISC System/
Designing on any other workstation



Whatever you're creating, you'll sail into a whole new age with any of the four POWERstations in the RISC System/6000 family. Because POWER (Performance Optimization With Enhanced RISC) processing can give you performance you've probably only dreamed about:



up to four instructions per machine cycle, 42 MIPS and 13 MFLOPS. Suddenly, complex designs don't take eons anymore.

The four RISC System/6000 POWERstations feature a range of graphics processors from grayscale to Supergraphics to satisfy any graphics demand. Great news for Power Seekers working on animation, scientific visualization, medical imaging and engineering solutions like CADAM,™ CAEDS™ and CATIA.™ And for electrical design automation, there's IBM's all new CBDS™ and an arsenal of over 60 EDA appli-

LOOKING AHEAD TO 1991

As the leaves begin to turn color, it signals that time when we must develop our editorial calendar for the coming year—special reports, conference and show previews, special sections, and so on. Of course, this does not fully cover all of our features for the year. In this fast-moving industry, it's impossible to foresee every emerging hot topic. However, the calendar is representative of the type of important technology material you will be seeing in ELECTRONIC DESIGN in 1991.

ELECTRONIC DESIGN 1991 EDITORIAL CALENDAR

Jan 10	Technology Forecast: Critical Issues for the Design Team; PC Design
Jan 31	PIPS: Power, Interconnections, Passives, Switches and Relays; Computer Systems: Boards/Buses/Peripherals
Feb 14	Advanced Semiconductors: ISSCC
Feb 28	CAE: Packaging Design Tools; Test & Measurement Update: VXI Bus Instruments
Mar 14	Digital Semiconductors: PLDs & FPGAs; PC Design
Mar 28	Communications ICs: Modems; Design Team Issues: System-Level Design; PIPS: Power, Interconnections, Passives, Switches and Relays
Apr 11	Analog Technology; CAD/Printed-Circuit Board Designers' Guide; Electro Preview
Apr 25	Digital Semiconductors: Memory ICs; Packaging & Materials Designers' Guide
May 9	PC Design: Personal Computers as Design Tools; ASICs
May 23	Image Processing; PIPS: Power, Interconnections, Passives, Switches and Relays
Jun 13	CAE: Simulation; DAC Preview; Careers Special: Reader Opinions Survey
Jun 27	Digital Semiconductors: Embedded Controllers: RISC + CISC; Design Team Issues: Design for Testability
Jul 11	Communications: Networks; PC Design; Test & Measurement Update: Digital Oscilloscopes
Jul 25	Analog Technology; PIPS: Power, Interconnections, Passives, Switches and Relays
Aug 8	Digital Semiconductors: Graphics ICs; Automotive Electronics Designer's Guide
Aug 22	CAE: Advanced Tools; Test & Measurement Update: Digital Multimeters
Sep 12	Analog Technology; PC Design; Computer Bus/Board Designers' Guide; Buscon Preview
Sep 26	Communications: Digital Speech Technology; Design Team Issues: Design for Manufacturability; PIPS: Power, Interconnections, Passives, Switches and Relays
Oct 10	Digital Semiconductors: Digital Signal Processing ICs; Careers Special: Reader Salary Survey
Oct 24	PC Design: PC Chip Sets Designers' Guide; ATE/VLSI Testing; Comdex Preview
Nov 7	CASE; Programmable Logic: Development Tools Designer's Guide
Nov 21	Analog and Mixed-Signal ASICs; PIPS: Power, Interconnections, Passives, Switches and Relays; Wescon Preview
Dec 5	CAE: VHDL; Advanced Semiconductors: IEDM; Test & Measurement Update: Communications Test Equipment
Dec 19	1991 Technology Review: Top 100 Products

SPDT switch dc to 5GHz with built-in driver

Truly incredible…a superfast 3nsec GaAs SPDT reflective switch with a built-in driver for only $19.95. So why bother designing and building a driver interface to further complicate your subsystem and take added space when you can specify Mini-Circuits' YSW-2-50DR?

Check the outstanding performance specs of the rugged device, housed in a tiny plastic case, over a -55° to +85° C span. Unit-to-unit repeatability for insertion loss is 3-sigma guaranteed, which means less than 15 of a 10,000-unit production run will come close to the spec limit. Available for immediate delivery in tape-and-reel format for automatic placement equipment.

SPECIFICATIONS YSW-2-50DR	dc-500MHz	500-2000MHz	2000-5000MHz
Insertion loss, typ (dB)	0.9	1.3	1.4
Isolation, typ(dB)*	50	40	28
1dB compression, typ (dBm @ in port)	20	20	24
RF input, max dBm (no damage)	22	22	26
VSWR (on), typ	———	1.4	———
Video breakthrough to RF, typ (mV p-p)	———	30	———
Rise/Fall time, typ (nsec)	———	3.0	———

*typ isolation at 5MHz is 80dB and decreases 5dB/octave from 5-1000 MHz

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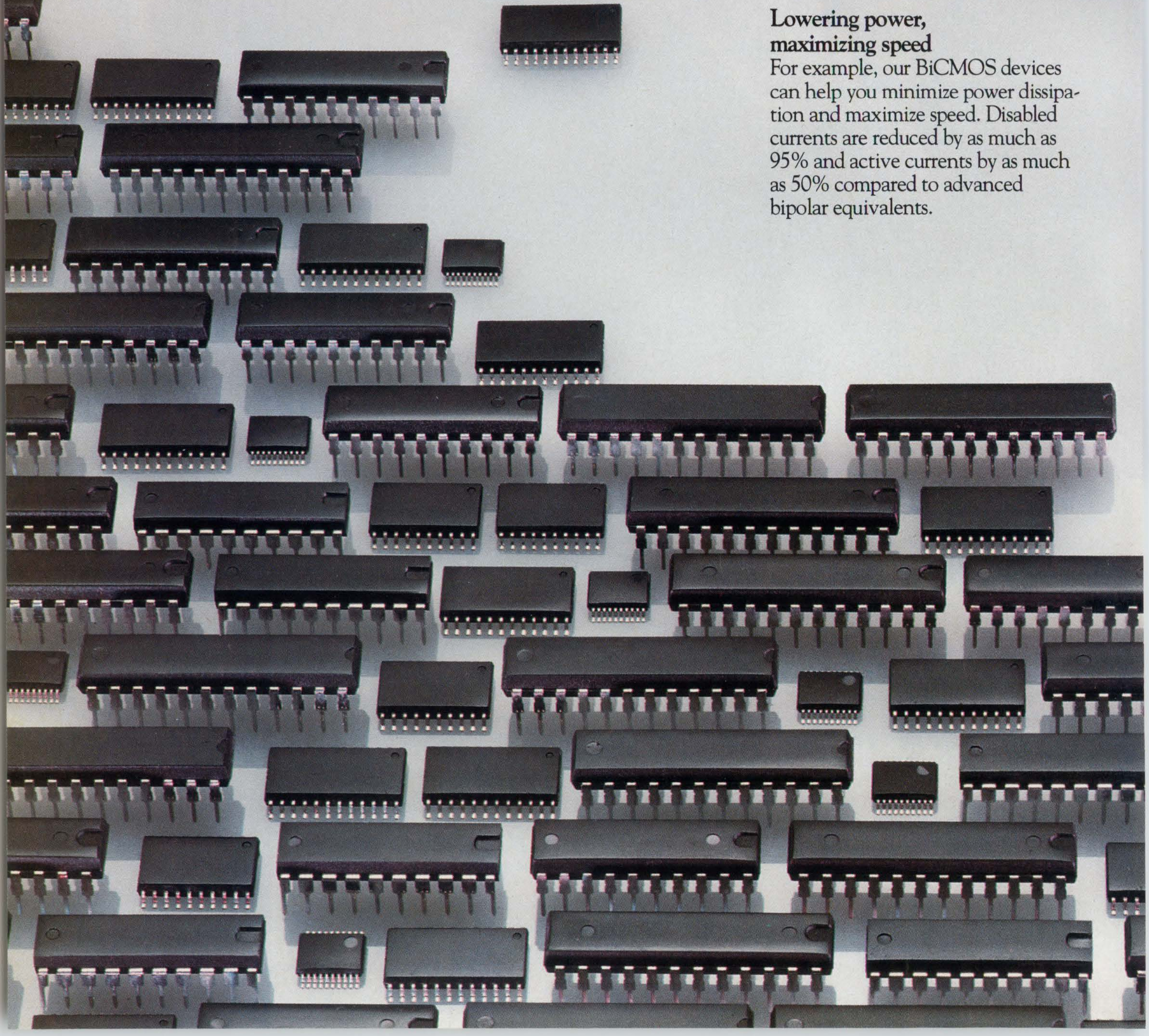


THE SOLID-STATE FLOPPY HAS ARRIVED

DAVE BURSKY
SEMICONDUCTORS

Advances in memory density and packaging technology over the past few years have led to practical-capacity memory cards that can store millions of bytes. Such densities make it possible for the cards to offer storage capacities that match, or even exceed, current-generation 3.5-in. floppy disks. Housed in a casing the size of a credit card with about five times the thickness, these cards promise to revolutionize the portable computing market if costs recede and a universal interface standard can be agreed on by all card makers.

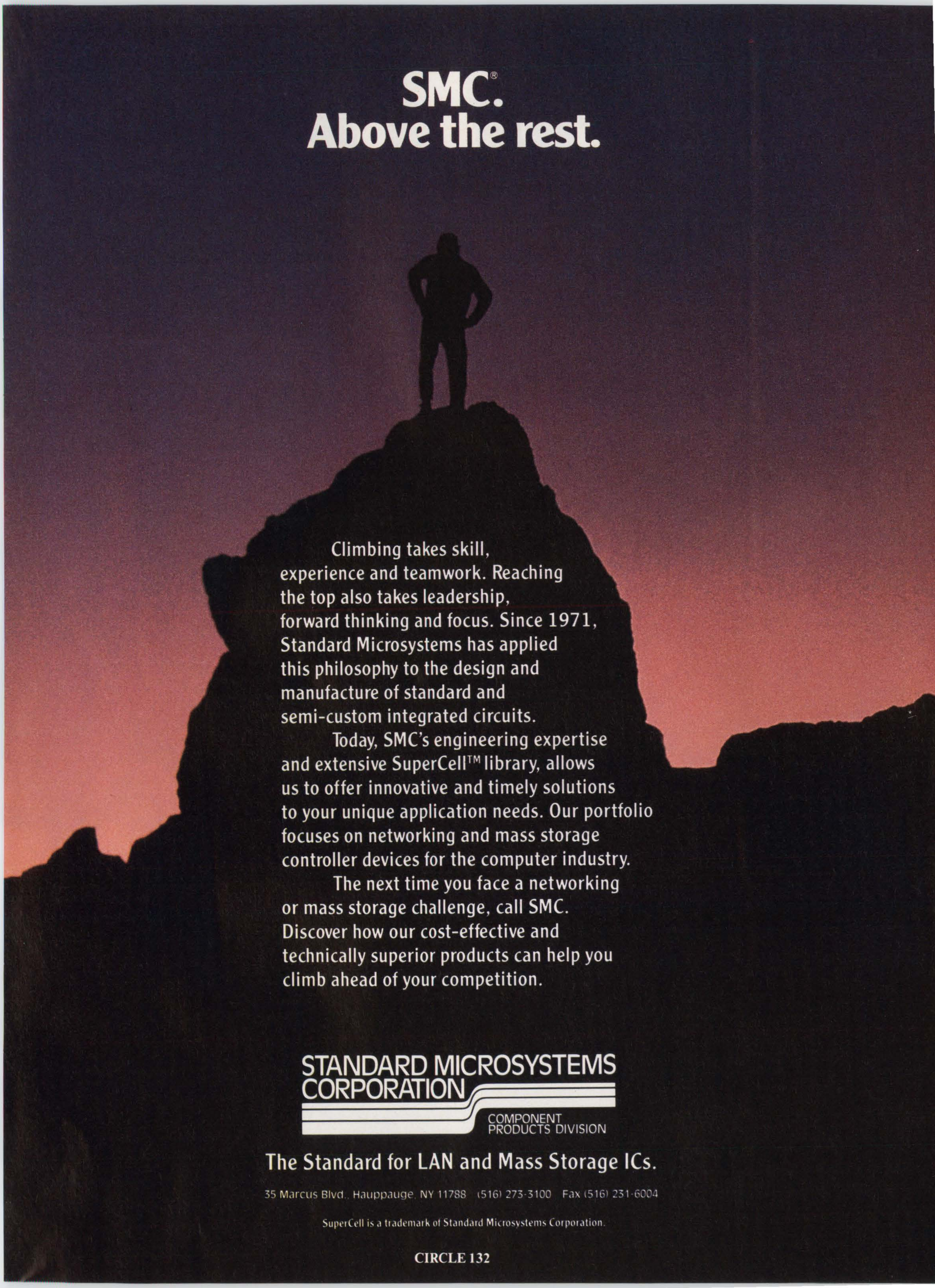
The latter is close to reality: The Personal Computer Memory Card International Association, with the Japan Electronic Industry Development Association, has developed a PC card standard. Currently in the form of Release 1.0, the standard defines the card's dimensions, the 68-contact connector format, the signal and electrical interface, the metaformat for the data storage, and other aspects.

The standard doesn't impose one philosophy on all applications, thus allowing very small memory cards to be used for such applications as appliance memory modules. The standard will also permit different data-storage (recording) formats so that the market can determine the preferred structure (to get a copy of the standard, contact Daniel Chen, the committee chairman, at Mitsubishi Electronics America, Sunnyvale, Calif., (408) 730-5900).

ROM cards, RAM cards (some with internal battery back-up), one-time programmable EPROM-based cards, and the recently released flash EPROM memory cards from Intel Corp., Folsom, Calif., are all available. Although most of these cards cost several orders of magnitude more than the $2 or so that the floppy disk sells for, they promise to eliminate the power-hungry disk drive and all of the reliability issues that the mechanical drive carries with it. Furthermore, because most cards permit random addressing of their contents, the host system will see a noticeable jump in apparent performance. Random accesses occur at sub-microsecond rates—about two or three orders of magnitude faster than the disk drive's access time.

The cost of the card-reader electronics must also come down. This is so that the card reader/programmer the card plugs into is priced comparably to a high-capacity floppy-disk drive. A few companies have started to offer "card drives," but the components used today aren't well integrated to reduce cost and board space. One such company, Databook Inc., Ithaca, N.Y., has developed drive replacements that contain all of the circuitry to both read data from, or store data in, the memory cards. The company is currently exploring ways to cost reduce the electronic drive through the use of ASICs. Software used by Databook to control the memory is the pre-release version of Microsoft Corp.'s flash file system. With that software, the memory card appears as if it were a fast disk drive. At least one portable computer maker, Poqet Computer Inc., Sunnyvale, Calif., incorporated the memory card standard and flash-file interface into its palm/pocket-sized personal computer.

With the prices of 4-Mbyte flash-based memory cards currently well over $1000, and CMOS static-RAM-based cards with 1 Mbyte of storage costing about half that, few users could afford the cost premium of the cards and the drive replacement. For now, most of that cost stems from the memory chips. However, chip costs should drop substantially over the next 6 to 12 months as manufacturing volumes ramp up. Studies done by several card makers suggest that by the middle of this decade, almost all of the portable computers expect to use memory cards rather than floppy-disk drives. This will save power, weight, mechanical wear and tear, and perhaps even more importantly, time. With solid-state memory, file loads and storage can run three to ten times faster than on a floppy drive.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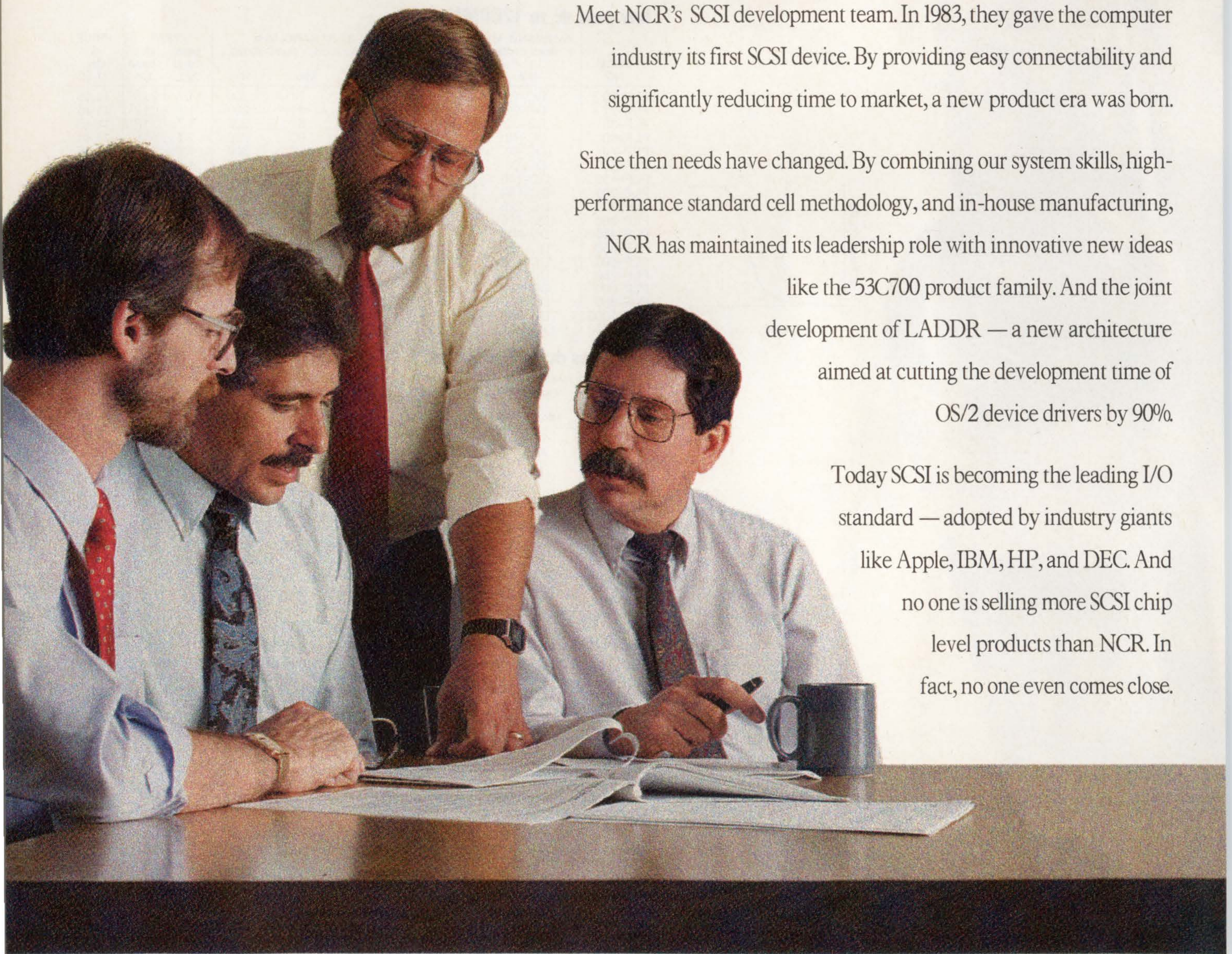
Here's one reason that over half of all SCSI devices sold are NCR.



We created the market... and we still lead the way.

Meet NCR's SCSI development team. In 1983, they gave the computer industry its first SCSI device. By providing easy connectability and significantly reducing time to market, a new product era was born.

Since then needs have changed. By combining our system skills, high-performance standard cell methodology, and in-house manufacturing, NCR has maintained its leadership role with innovative new ideas like the 53C700 product family. And the joint development of LADDR — a new architecture aimed at cutting the development time of OS/2 device drivers by 90%.

Today SCSI is becoming the leading I/O standard — adopted by industry giants like Apple, IBM, HP, and DEC. And no one is selling more SCSI chip level products than NCR. In fact, no one even comes close.

Part of the NCR SCSI Development Team: (left to right)
Jerry Armstrong, Sr.Software Engineer; **Harry Mason**, Strategic Marketing Manager; **John Lohmeyer**, NCR Sr. Consulting Engineer and Chairman of the ANSI X3T9.2 Committee and **Dave Skinner**, SCSI ProductManager.

North American Sales Headquarters
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Here's another.

The NCR 53C700 SCSI I/O Processor... So good, *Electronic Design* named it the product of the year.

"You can't tell a good SCSI chip just by looking at it... " and according to Electronic Design, NCR's 53C700 is the best there is.

The only third generation SCSI device on the market today, it concentrates all the functions of an intelligent SCSI adapter board on a single, smart and extremely fast, chip... for about 15% of the cost.

As the first SCSI I/O processor on a chip, the 53C700 allows your CPU to work at maximum speed while initiating I/O operations up to thousands of times faster than any non-intelligent host adapter. DMA controllers can burst data at speeds of up to 50 Mbytes/s. This new chip cuts down system time hookup to a fraction of what it has been.

Those are just a few of the reasons Electronic Design's "Best of the Digital IC's" award went to NCR's 53C700 last year.

And now the NCR 53C710!

For the complete story on the NCR SCSI product line featuring the new 53C710, as well as the upcoming SCSI seminars with the NCR SCSI Development Team, please call:

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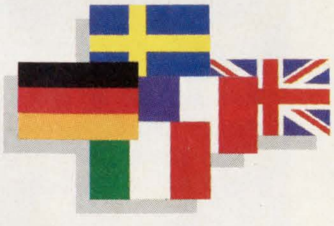

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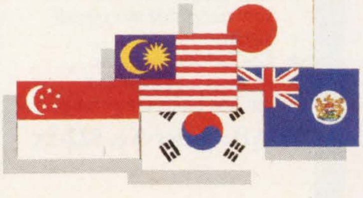

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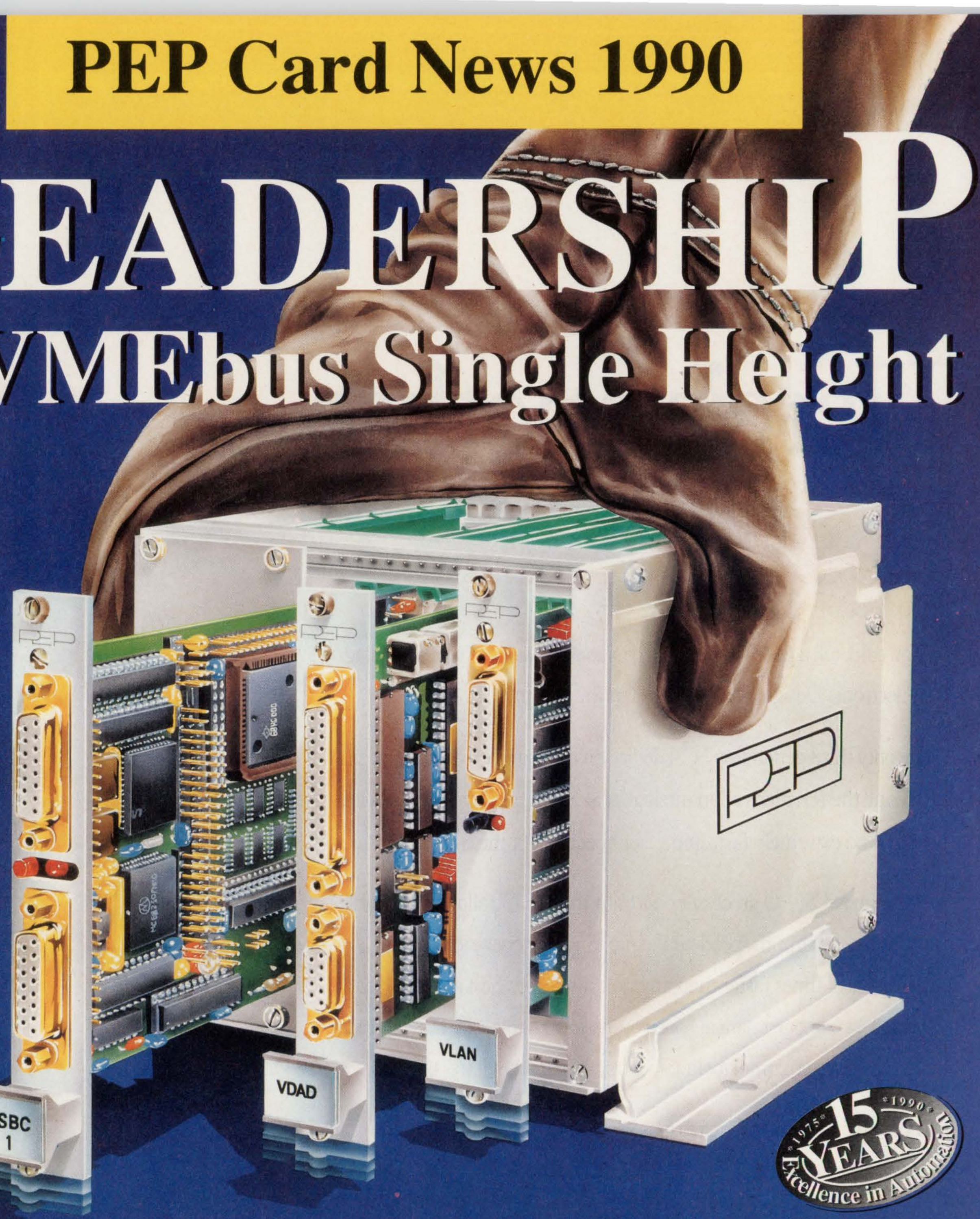
PEP Card News 1990

LEADERSHIP in VMEbus Single Height



OS-9 Trademark of Microware Inc.
PDOS Trademark of Eyring Research Inc.

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CMOS Single Board Computer

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ADC/DAC and Digital I/O Module

- ★ 16 channel multiplexed, 12-bit A/D
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CIRCLE 193

FDDI Chip Set Takes On Copper Cable

The Supernet chip set for Fiber Distributed Data Interface (FDDI) local-area networks is now ready for use, without modification, in FDDI applications that use copper cabling. The developer of the chip set, Advanced Micro Devices Inc., Sunnyvale, Calif., announced that tests at its own laboratories and at key customer sites support this statement. The announcement is timely in view of the effort by the ANSI-accredited X3T9.5 work group to find less costly solutions to the current FDDI documents that specify glass fiber-optic cable as its medium. The work group is expected to define the transformer, carrier-detect functions, and equalization standards required for FDDI over wire. Except for yet-to-be-standardized carrier-detect functions and passive components for equalization, AMD says Supernet products are ready for FDDI over wire today. *ML*

Ultrafast Thermometer Captures Transients

Scientists at the Univ. of Rochester in N.Y. have devised a way to measure the temperature of the top few atomic layers of a material's surface in less than one picosecond. Called picosecond reflection high-energy electron diffraction, the method uses a pulsed-laser beam to heat the sample surface and another beam to activate an electron gun. The electron gun directs electrons onto the sample surface at a shallow angle—just a few trillionths of a second after the sample is heated by the laser. Electrons bouncing off the sample surface pass through an amplifier and form a reflection high-energy electron diffraction pattern on a phosphor screen. The screen indicates the angle at which the electrons are deflected and their intensity. These two quantities determine surface temperature to within 10°C. Funded by the Department of Energy, the work is expected to benefit the electronics industry by giving deeper insight into the thermal behavior of material surfaces used in the production of microchips. *ML*

Real-Time Consortium Pushes Open BIOS

The Real Time Consortium has completed a preliminary specification for OBIOS, an Open Basic Input Output System designed to provide interoperability between hardware platforms and software operating systems from various vendors. The OBIOS standard supplies an efficient physical I/O interface that sharply reduces the programming time needed to create device drivers. Independent of operating system, bus, and microprocessor types, the standard eliminates the need to continuously rewrite device driver modules for each new marriage of hardware and operating systems or real-time kernels. A preliminary specification will be expanded into a first draft by the consortium's Technical Committee, which will be ready at Buscon next January. The draft will include driver code for connecting to several classes of drivers, including serial I/Os, networks, SCSI ports, and timers and counters. The consortium expects OBIOS software to be ready by next spring. Charter founding members of the consortium include Ready Systems Corp., Sunnyvale, Calif.; Wind River Systems, Alameda, Calif.; Lynx Real-Time Systems, Los Gatos, Calif.; Heurikon Corp., Madison, Wis.; and Force Computers Inc., Campbell, Calif. Heurikon is presently working on OBIOS hardware drivers. *RA*

Buses Brought Forward At Buscon

Several developments unfolded at the recent Buscon Trade Show held in Marlborough, Mass., such as:

A 61% Multibus II growth in 1990, reported by the Multibus Manufacturers Group, Aloha, Ore. Actual volumes are expected to be 58,000 units, compared with 36,000 units shipped in 1989. The figures were based on data supplied by Multibus II bus-interface vendors.

A Futurebus+ chip set from National Semiconductor Corp., Santa Clara, Calif., to be unveiled next January. All parts should be available in sample quantities by that time.

A single-board computer from Ziatech Corp., San Luis Obispo, Calif., that conforms to STD 32, the long-heralded 32-bit specification for the STDbus. While STD 32 isn't an official specification yet, companies have started to develop products for it. The 8901, a 286-compatible board, boasts a mean-time-between-failure of 20 years. The 16-bit board works with 16- and 32-bit backplanes for universal compatibility. The board contains a 16-MHz NEC V53 processor, up to 1 Mbyte of on-board, battery-backed static RAM, and 1 Mbyte of ROM. *RN*

FUTUREBUS+ STANDARDS KEEP ROLLING ALONG

The Futurebus+ committee for standards met recently to exchange views on ten different standards activities concerning Futurebus+. Some of the proposed activities were granted sponsor ballot status, meaning that the proposals are considered completed in their respective work groups. From here, the acting members vote on the proposals, and if passed, they become specifications. Otherwise, the committee must rework the proposals. In addition, some new work groups were started. These include the conformance-testing group and the group for the VMEbus-to-Scalable-Coherent-Interface (SCI) bridge. One standard discussed in detail was the Futurebus+ Logical Layer (P896.1). This specification was voted on and rejected by a slim margin, mainly due to the speed of the arbitration circuitry as well as the circuit's overall cost.

The focus of item P896.2 (physical layer) revolves around the work done by Raytheon Corp. and Digital Equipment Corp. The companies were asked to apply their high-bandwidth expertise in an exhaustive set of simulations to help finalize the specifications. Over 11,000 Spice elements per signal were simulated to develop a comprehensive noise-margin-analysis methodology. Other parts of the Futurebus+ specification discussed were node management, the I/O architecture, the military and telecommunications profiles, and bridges from Futurebus+ to VMEbus and Multibus II. *RN*

STREAMLINED 68030 TACKLES EMBEDDED USES

Although a number of applications already use the 68030 complex-instruction-set processor in embedded systems, many of its features suitable for Unix and large memory environments often go unused. That adds an unacceptable cost premium to the chip. To combat that problem, designers at Motorola Inc., Austin, Texas, made several adjustments: they streamlined the central processor by removing the memory-management unit, moved the chip to a 1-μm process rather than the 1.5-μm process used by the 68030, and housed the chip in a relatively inexpensive plastic pin-grid-array package. The final product—the MC68EC030—was unveiled last month at Microprocessor Forum. It delivers double the throughput of the older 68020 at about the same price. The first version of the 68EC030 is actually the same silicon circuitry as the 68030, but some metal-mask changes were made to permanently disable the MMU. That reduces testing time and contributes to the lower price. By the second half of 1991, designers expect to finish a redesign that physically removes the MMU circuits to further shrink the chip area. Complete emulation support for the chip is available from Applied Microsystems Corp., Redmond, Wash. Contact Jim Reinhart, (512) 891-2931. *DB*

MICRO LINEAR GETS 1-μM BICMOS FROM AMCC

The world of mixed-signal analog arrays, and circuits built from them, will soon see a new player in the biCMOS arena. Micro Linear Corp. (MLC), San Jose, Calif., and Applied Micro Circuits Corp. (AMCC), San Diego, Calif., announced a joint agreement in which Micro Linear would license AMCC's 1.5- and 1-μm biCMOS process. AMCC will supply process know-how and technology details so that MLC can produce its own products using the processes. As part of the agreement, MLC will supply foundry services for AMCC. The availability of a viable biCMOS process will permit MLC to develop a more complex range of mixed-signal semicustom and standard product ICs. Like Analog Devices, Wilmington, Mass., MLC will be able to build ICs using bipolar devices for precision analog circuits, and CMOS devices for analog switches and dense logic. *FG* **CIRCLE 400**

TWO MINDS IMPROVE FUTUREBUS+ CHIP CHOICE

Futurebus+-compatible system design took major strides toward simplicity earlier this year when Philips Components-Signetics (PCS) Corp., Sunnyvale, Calif., released its chip-set approach to the interface. Now, in a product exchange and codevelopment deal signed with Texas Instruments Inc., Dallas, both companies will pool their efforts to design future chip-set members. In addition, the companies will alternate-source each other's Futurebus+ products. All of the bus-interface chips and two of the three LSI chips that were previously disclosed by Philips Components-Signetics will be alternate-sourced by TI (ELECTRONIC DESIGN, *May 10, p. 63).* The one chip that won't be alternate sourced—the packet-data FIFO memory—must be redesigned to meet the latest changes already adopted by the Futurebus+ committee. The family will be called the FB2000 series by Signetics, and the TFB2000 by TI. Futurebus+ chips haven't been released by Texas Instruments yet, but the company already developed a few that will be part of the family: the 2001/2002 parallel protocol controller, the 2011 competition transceiver, and the 2021 data-

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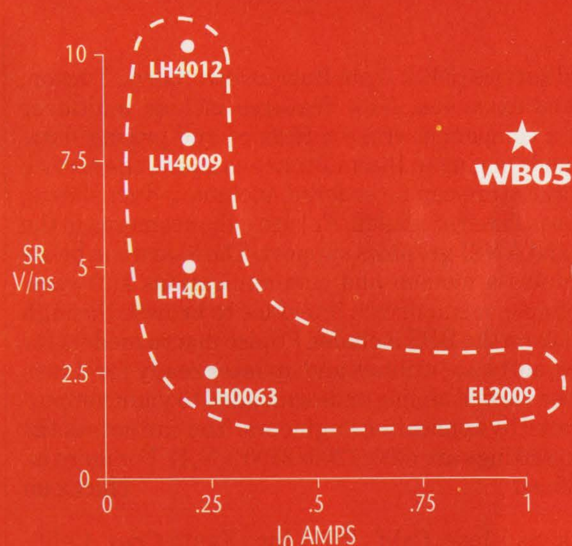

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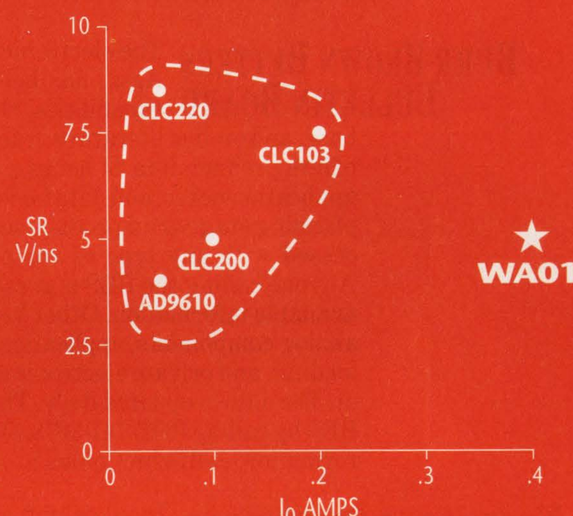

APPLICATIONS

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CIRCLE 192

path unit. The five-year deal doesn't cover process technology—each company will use its own proprietary biCMOS processes to fabricate the chips. Samples of several interface chips are now available, but the more complex chips won't be ready until the first quarter. *DB*

Motorola Fine-Tunes Wireless Net Design

Following FCC action earlier this year to allow low-power in-building radio communications, the Radio-Telephone Systems Group of Motorola Inc., Arlington Heights, Ill., initiated its WIN (wireless in-building networking) program to overcome the limitations of existing wireless communications technologies. Compared to hard-wired systems, wireless in-building networks that transmit information through the electromagnetic spectrum require less expense, time, and effort to install, maintain, and reconfigure. However, existing wireless systems do have drawbacks. For example, spread-spectrum networking is an unlicensed technology that lacks service guarantees, is vulnerable to interference, and is limited to about a 2-Mbit/s data rate. Infrared fares no better in terms of bandwidth capability—its transmission pattern is limited to line-of-sight, and it's not transparent to network operating systems. Essential to Motorola's program is the development of four hardware building blocks: a gallium-arsenide monolithic microwave IC (MMIC) transceiver chip, a 6-sector intelligent antenna that avoids interference by dynamically selecting the best signal, a radio-frequency digital-signal processor for specialized modulation and demodulation techniques, and a single-chip packet switch and network interface with standard-protocol transparency. The desktop system will operate in the interference-free 18-GHz microwave band with a 15-Mbit/s data rate. To meet both present and future networking requirements, the system uses 10-MHz channels. Hardware and software will become available next year. *ML*

Burr-Brown Betters Bulletin Board

The electronic bulletin board service (BBS) from Burr-Brown Corp., Tucson, Ariz., has been improved and expanded. New features include multiuser capabilities, the addition of a component cross-reference and pricing database, and on-line literature ordering. Accommodating up to 16 simultaneous users, the service offers product data 24 hours a day. Various literature can be ordered, including data sheets, application notes, and data books. Information is faxed or mailed. Future enhancements in the planning stage are a product-selection guide and ANSI graphics support. The board can be accessed with any type of computer that contains a modem and communications software. Anyone calling the BBS is presented with a simple, menu-driven interface to browse through available information. Other key information from the BBS includes PSpice macro models for analog components, application tips and notes, software utilities and updates ready for downloading, and private electronic mail. Files can be viewed on-line or downloaded to your computer. The data is updated daily. The BBS is operated by application engineers. You can access the BBS by calling (602) 741-3978. Communication settings are (300/1200/2400 8,N,1). For more information, call John Conlon at 1-(800) 548-6132. *FG* **CIRCLE 401**

Networked Controller Manages Remotely

In an exhibit at Interop '90 in San Jose, Calif., TVG Inc., Santa Cruz, Calif., demonstrated a new technology that controls any analog or digital device over a telecommunications network. The firm specializes in networking and applications software for Digital Equipment's VAX/VMS computers. TVG showcased its Simple Network Management Protocol (SNMP) device controller, which uses the TCP protocol suite that includes the SNMP and the Serial Line Internet Protocol (SLIP) link module. Exhibiting a "trial balloon" rather than a product offering, the device was applied in an AM/FM/CD stereo unit connected to the show network. The controller is a small Motorola 68000-based unit containing customized off-the-shelf hardware that links to a stereo remote-control system and the CD player. From a VAXstation using an X-Windows graphical interface, an operator was able to control all aspects of the stereo system, including CD track selection, audio input and frequency selection, and volume. *ML*

Second-Generation RISC Ups 88K Speed 3-5 Fold

By combining the functions of the previous-generation 88100 and 88200 RISC CPU and cache-memory and management units onto one chip, a forthcoming RISC processor will deliver three to five times the processing throughput. The 88110, unveiled by Motorola Inc., Austin, at last month's Microprocessor Forum, will include the integer and floating-point processors of the previous CPU in addition to several en-

hancements: a 3D graphics-execution unit and an 80-bit wide data path to handle extended double-precision math. Improvements in the instruction set will permit the processor to sustain more than one instruction per clock cycle. Acceleration in the branch section will help maintain continuous-instruction execution whether or not a branch is taken. To pack the more than 1.4-million transistors on the chip, designers opted for a triple-level-metal 0.8-μm CMOS process. Also disclosed were plans to release a family of RISC-based chips optimized for embedded control—the 88300 series. That family will use of large standard-cell building blocks from the 68300 design library to quickly add customized functions to the chip. *DB*

TECHNOLOGY DEAL NETS NEW GAAS IC SOURCE

Vitesse Semiconductor Corp., Camarillo, Calif., struck a deal with Thomson-CSF, Paris, which would provide gallium arsenide manufacturing technology to Thomson in exchange for manufacturing capacity. The initial result of the deal gives Vitesse a European seller of its products as well as access to a new manufacturing facility built by Thomson in Grenoble, France. In return, Thomson has made an equity investment in Vitesse that will permit Vitesse to pursue new product and technology development. Furthermore, the deal gives Thomson-CSF exclusive distribution rights for all Vitesse products in Western Europe and the option to second-source all logic and communication products, including the Vitesse Fury gate-array family. That broadens Thomson's portfolio, giving them a digital GaAs process that complements their microwave GaAs monolithic microwave IC (MMIC) capability. *DB*

SENSORLESS CONTROLLER IC DRIVES DC MOTORS

A family of single-chip motor controllers from Philips Components-Signetics, Sunnyvale, Calif., can drive full-wave, brushless dc motors without the need for commutator sensors. Targeted for such applications as laptop-computer disk drives and handheld tools, the devices require no microprocessor support for startup, but instead control the coil-energizing sequence, according to the back-emf sensed in the motor windings. A proprietary startup protocol also eliminates hunting and jitter. The bipolar controllers draw less than 5 mA from a 4-to-18-V unregulated supply. Each circuit has a tachometer output, and some contain facilities that monitor rotor position with an external sensor. Thermal-protection and current-limiting features are also included. The TDA5140A drives loads up to 0.6 A, and the TDA5141 drives loads up to 1.8 A. The TDA5142 is for heavier loads. Prices are $2.45 and $2.15 for the TDA5141 and 5142, respectively; the TDA5140A costs $2.25. Call Joseph Resendes, (408) 991-5396. *ML* **CIRCLE 402**

TRANSCEIVER LINKS LAN HUB TO 10BASE-T

The LXT903 hub transceiver from Level One Communications Inc., Folsom, Calif., connects multiport LAN hub repeaters to unshielded twisted-pair LAN lines. In the software mode, the device supplies an interface to operate with any standard microcontroller for media-access-unit (MAU) management functions. The hardware mode makes the chip a standalone hub transceiver. Features of the LXT903 include automatic detection and correction of received polarity reversal, 10Base-T integrity testing, and watchdog timing to jab continuous transmission. Also provided are pre-distorted signals to the transmit filter, programmable squelch circuits, a differential or single-ended transmit input, and LED drivers for jabber, link, and reversed polarity. The device requires an external 20-MHz clock signal, and transmitter and receive filters. In lots of 10,000, the 24-pin plastic DIP version costs $7.98; in a 28-pin PLCC, the part costs $8.30. Call (916) 985-3670. *ML* **CIRCLE 403**

IMAGING CHIP CONVERTS BILEVEL TO GRAY-SCALE

An image scaler and rotator circuit from Brooktree Corp., San Diego, Calif., can scale bilevel images to produce a more readable gray-scale result when displayed on gray-scale and color monitors. The Bt710 includes two DMA channels that manage read operations from source image buffers and write operations to destination image buffers. The DMA channels also support address translation for image rotation and bit-aligned block transfers to window or frame-buffer pixel boundaries. The scaling range is from 6% (scale down) to 750% (scale up), and the scaler output can be bilevel (one bit) or 4-bit gray. An on-chip lookup table offers image inversion, gamma correction, or mapping from 4-bit gray to 8-bit pixels. The Bt710 is supported by a software toolkit for PC, Macintosh, and Sun platforms. Packaged in a 132-pin PGA, the Bt710 is being sampled for $132 in lots of 100. Call (619) 452-7580. *ML* **CIRCLE 404**

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New 12-Bit, 3-Wire Serial A/D, D/As Now Available In 8-Pin Mini-Dips

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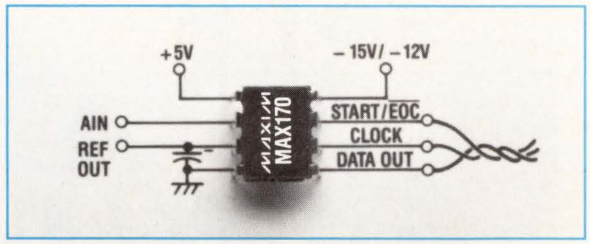

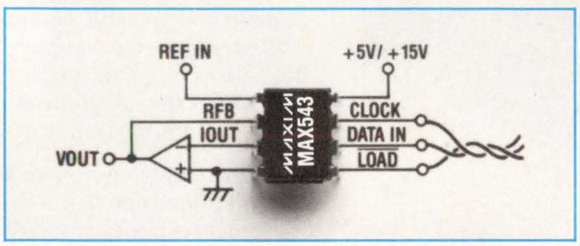

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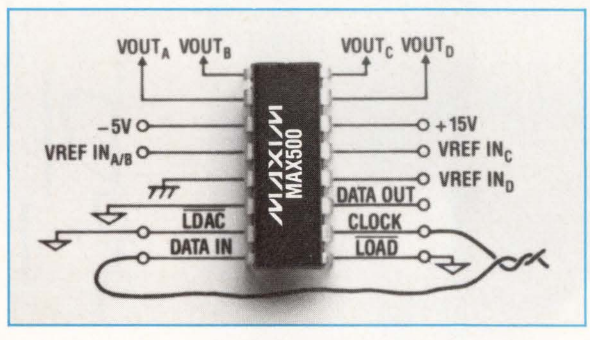

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CIRCLE 220

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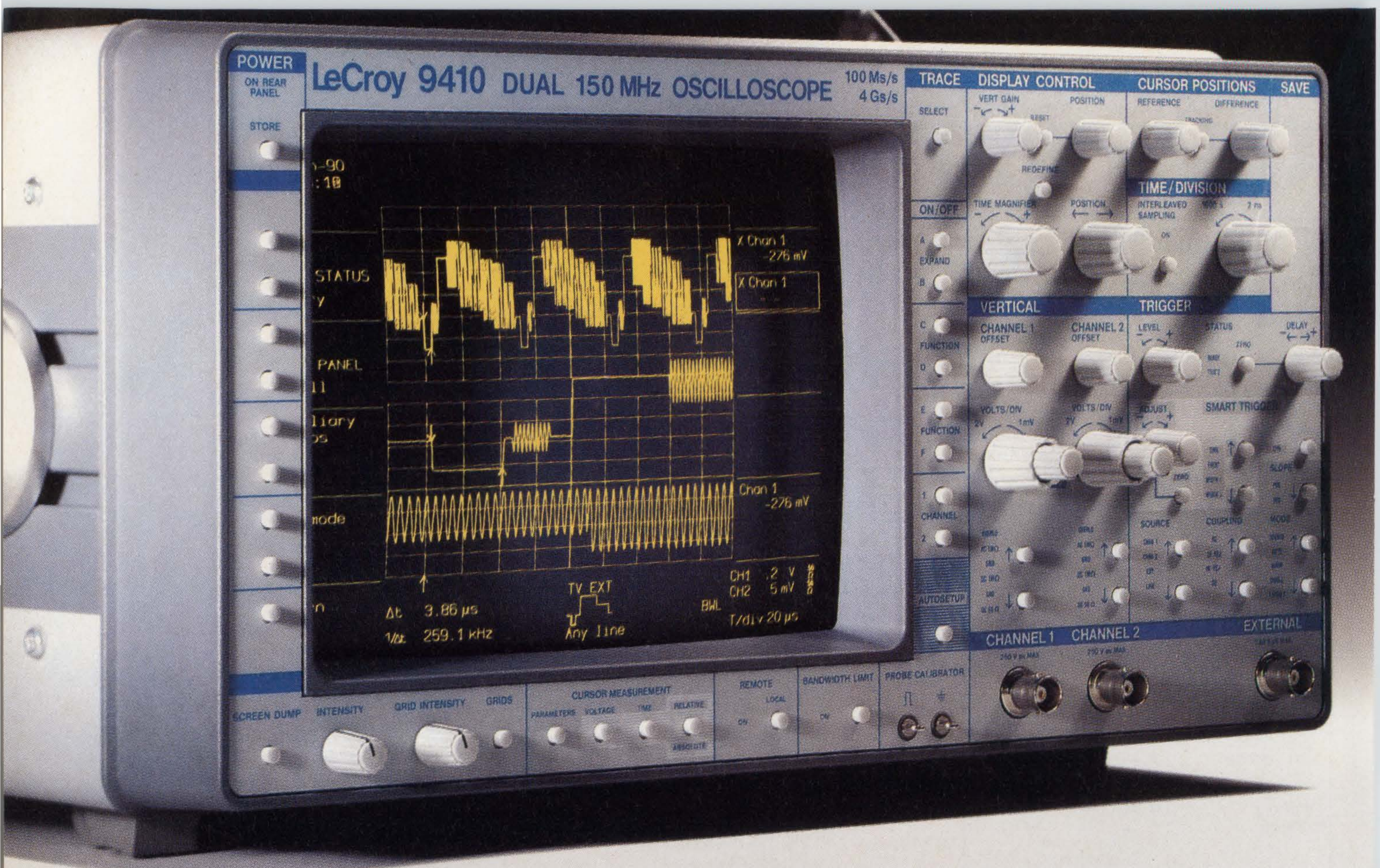
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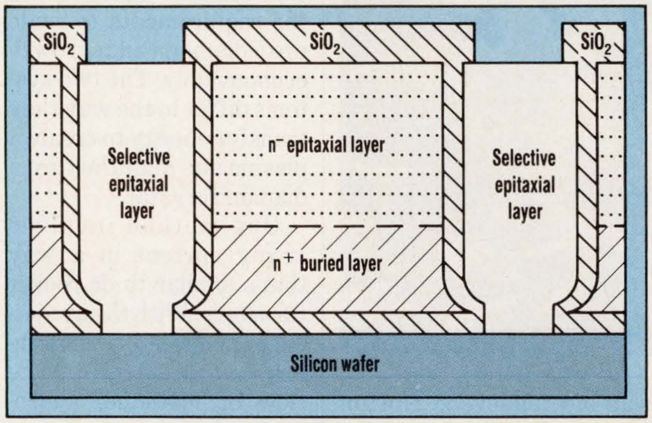


The possible long-sought replacement for building dielectrically isolated (DI), high-performance ICs may be found in Tizer (Trench Isolated Selective Epitaxial Regrowth). The technology, created by Silicon General, Garden Grove, Calif., has been used to build marketable DI diode arrays (ELECTRONIC DESIGN, *Sept. 27, p. 23)*. If this silicon-on-insulator (SOI) process can build DI-demanding ICs at costs equal to or less than present DI processes, it could be a Tiger.

An ideal SOI process must permit its users to build monocrystalline silicon-filled DI tubs on a purchased silicon wafer, using conventional lithography. And for many applications, the silicon in the tubs must be able to build good bipolar transistors—often thick or large ones. Tizer meets those demands.

Its starting wafers aren't just sliced off a boule, they're also processed. Silicon General has two wafer sources: Kopin Corp. of Taunton, Mass., and IBIS Inc. of Danvers, Mass. Each source uses a different technology. Starting material from both sources consists of an insulating layer of silicon dioxide, SiO_2, or oxide, sandwiched between a silicon wafer and bipolar-transistor-quality silicon.

Kopin supplies wafers called ISE, built on a modified zone-melted recrystallized (ZMR) process. To build the wafers, Kopin grows the oxide layer on the wafer, deposits a layer of polysilicon on the oxide, and with proprietary techniques (related to the way silicon boules are grown), turns the polysilicon into a layer of monocrystalline silicon. The oxide layer is 1-μm thick; the silicon layer is 2-μm thick.

IBIS offers SIMOX wafers. They're built by implanting oxygen ions beneath the wafer's surface. Then the surface is heated so that the oxygen oxidizes the silicon, forming a 0.4-μm thick layer of oxide beneath 0.4 μm of silicon.

That's the starting material for Silicon General. It grows 1.6 μm of epitaxial silicon on the IBIS wafers to bring the exposed silicon to the thickness of the Kopin material.

The first step in the Tizer process is to selectively implant the silicon layer with antimony to form an n^+ low-sheet-resistance (20-Ω/square) buried layer. This is followed by the growth of seven to ten microns of epitaxy, depending on the function of the final ICs to be built in the material. Next, a heavy oxide layer is grown on the surface for later use as a hard mask when etching the bottom oxide layer. During oxide growth, updiffusion occurs from the buried layer to the epitaxial layer. Trenches are then cut in the silicon down to the bottom oxide layer with a reactive ion etcher (RIE) followed by a lateral etch, which causes an oxide-overhang on the surface.

Next, the sidewalls of the trenches are oxidized to a thickness of 0.5 to 0.6 μm, followed by reaction ion etching of the trench-bottom oxide to expose the substrate silicon. Selective epitaxial growth techniques can then fill the trenches without the need for planarization *(see the figure)*. The oxide's top layer is removed and the wafer is full of oxide-isolated tubs filled with silicon ready to build most transistors with any process.

Unlike conventional DI tubs, standard lithography has determined the dimensions of Tizer tubs as part of the chip layout. There's no limit on epitaxial thickness or tub size, like conventional DI. Moreover, thermal-expansion characteristics are closer to those of bulk silicon, and the vertical sidewalls increase transistor density.

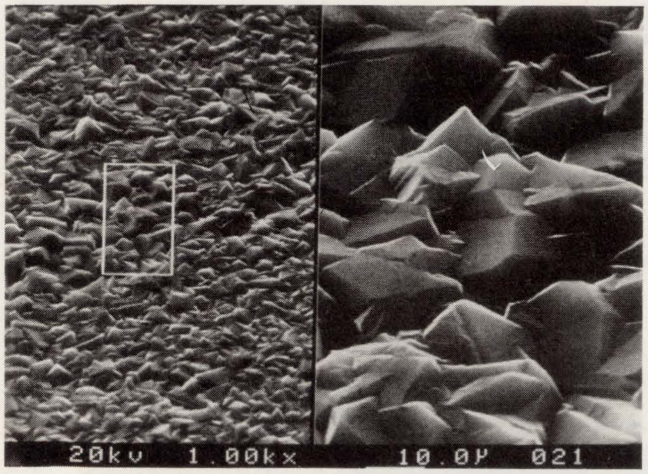
While the process was developed to build radiation-hardened ICs, it's a natural for high-speed analog and digital chips, as well as power ICs. The reduced collector-substrate capacitance enhances analog and digital circuit speed. Analog performance is enhanced further with its ability to build fast vertical pnps. According to Richard Belanger, a Silicon General design engineer, "Because of the inherent capabilities of the SOI devices at high temperature, we're exploring operation at 300°C. The isolation is stable at 300°C, but the transistors become very soft. However, we're evaluating new techniques to resolve the problem." For more information, call Richard Belanger at (714) 898-8121

FRANK GOODENOUGH

DIAMOND FILM STANDS POISED TO ICE HOT CHIPS

Besides being the world's hardest substance, diamond conducts heat faster than any other solid. Its thermal conductivity is almost three times that of silver. Heat sinks incorporating diamond film are an ideal solution to thermal management of the multichip modules that will be the building blocks for the next generation of computers. And now, there's an economically feasible process to deposit diamond film on free-standing substrates large enough to serve as heat sinks.

As packaging engineers



jam circuitry closer together in modules, heat dissipation becomes a critical factor. When it's coupled with higher clock speeds that account for more current draw, even more heat is dispersed. Norton estimates that the thermal characteristics of diamond could permit clock speeds of 100 MHz or more.

In its pilot process that's ready to scale up to full production, Norton Co.'s Diamond Film Division, Northboro, Mass., combined several proprietary manufacturing techniques to achieve diamond films of sufficient size and quality for use as heat sinks or, potentially, as diamond-based ICs. More than 100 academic and corporate labs—including some 70 in Japan alone—have strived to scale up production of diamond-film products.

The free-standing diamond-film heat sinks offer a lightweight solution to thermal management. They also make it possible to place electronic equipment in harsher thermal environments, such as military aircraft or missile-guidance systems, with a higher degree of reliability. Circuit densities ten times greater than today's can be achieved, Norton claims. Furthermore, the company says it can now get metal to adhere directly to diamond substrates. Those substrates can be overlaid with polyimide for microelectronic-circuitry etching.

For several years, researchers worldwide have focused their diamond-production efforts on plasma-assisted chemical-vapor-deposition (CVD) processes, which deposit carbon from the vapor phase onto a supporting material at low pressure and moderate temperatures. Typically, methane gas and hydrogen are used as raw materials.

After five years of investigation, Norton scientists settled on two methods that fulfilled almost all of the requirements to scale up to diamond-film growth economically. The two systems differ in the way they transfer energy to create a plasma and manufacture a diamond crystal.

One method involves arcing current in a way that's similar to dc rocket thrusters. With the arc-jet-engine method, researchers can manipulate the flow of methane, hydrogen, and other gases to create films with the desired characteristics. The other technique, microwave processing, centers on a tunable microwave cavity that's adjusted in terms of its geometry to produce the most efficient plasma.

Under an agreement with Darpa, Norton is developing real-time computer control systems that regulate the deposition process, to ensure that diamond films are made with no impurities. Real-time process control is essential to economical mass production with high quality.

DAVID MALINIAK

Parallel-Processor Systems For DSP Applications Become Easily Expandable

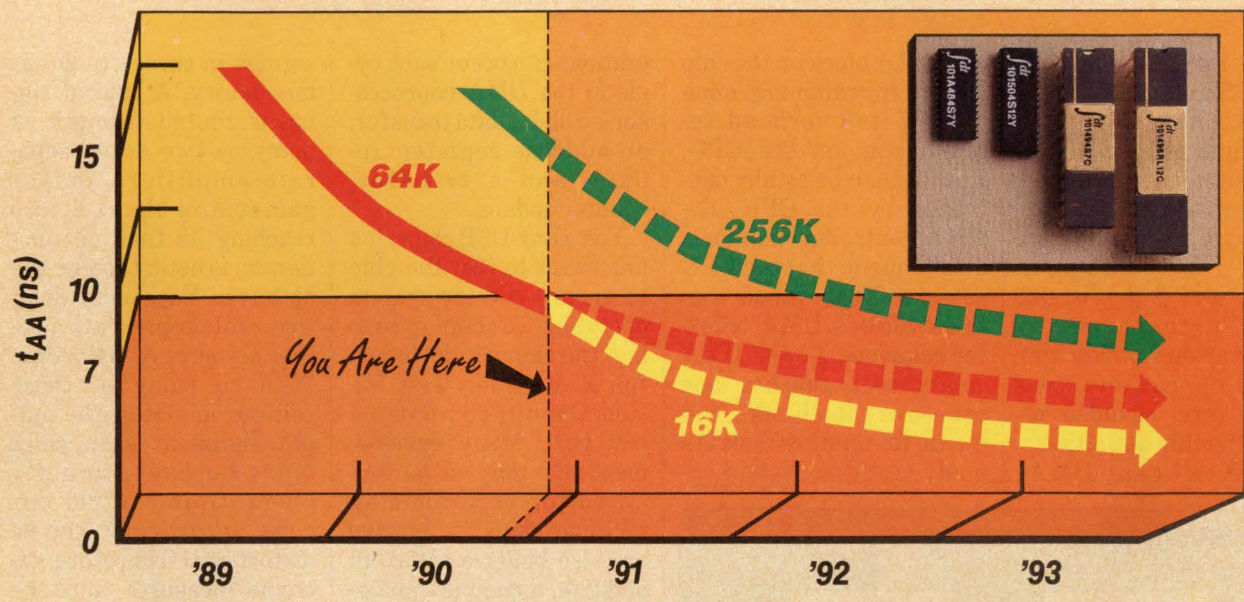
With multiple communication ports and intelligent DMA control, a forthcoming digital signal processor can take on applications that demand the high performance of parallel processing. Each DSP chip can execute 275 million operations per second (MOPS). As a result, designers can create arrays with any number of chips, and can now easily confront computational problems previously too complex or time-consuming for uniprocessors or limited arrays of processors.

Based on the same integer and floating-point processor core used by Texas Instruments Inc., Houston, in its TMS320C30 DSP chip, the TMS320C40 is designed for parallel processing. The processor architecture has been extended—the program counter was increased from 24 to 32 bits. There are four more extended-precision registers, bringing the total to 12; divide and square root instructions are incorporated; and the pipeline is streamlined to improve efficiency.

Six on-chip byte-wide serial ports and another half-dozen DMA controllers handle an aggregate data-transfer rate of 320 Mbytes/s. Those byte-wide ports, similar in concept to the bit-wide serial ports on the Inmos Transputer chip, are bidirectional and handle interprocessor communication as well as I/O operations. Each port includes the eight data lines plus four control lines—Strobe, Ready, Acknowledge, and Request—giving designers total control of the transfers. Multiple ports can be set up to operate in parallel for 16-, 24-, 32-bit-wide, etc. data transfers. Various system architectures—linear pipeline arrays, bidirectional rings, tree structures, a variety of 2D schemes for image processing, and even 3D or 4D system architectures—are practical and can be implemented efficiently.

What's more, parallel processing occurs on the chip, because the communication ports, DMA controllers, and integer and floating-point sections can all operate in parallel. That gives the chip its peak throughput of 275 MOPS. The floating-point unit and integer processor operate with 80-ns and 40-ns instruction cycle times, respectively, resulting in re-

Break Through 7ns



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IDT101484	16K (4K × 4) 101K ECL	7	700
IDT10490	64K (64K × 1) 10K ECL	8	420
IDT100490	64K (64K × 1) 100K ECL	8	320
IDT101490	64K (64K × 1) 101K ECL	8	420
IDT10494	64K (16K × 4) 10K ECL	7	700
IDT100494	64K (16K × 4) 100K ECL	7	500
IDT101494	64K (16K × 4) 101K ECL	7	700
IDT10496RL	64K (16K × 4) 10K STRAM	12	1000
IDT100496RL	64K (16K × 4) 100K STRAM	12	800
IDT101496RL	64K (16K × 4) 101K STRAM	12	1000
IDT10504	256K (64K × 4) 10K ECL	12	800
IDT100504	256K (64K × 4) 100K ECL	12	600
IDT101504	256K (64K × 4) 101K ECL	12	800

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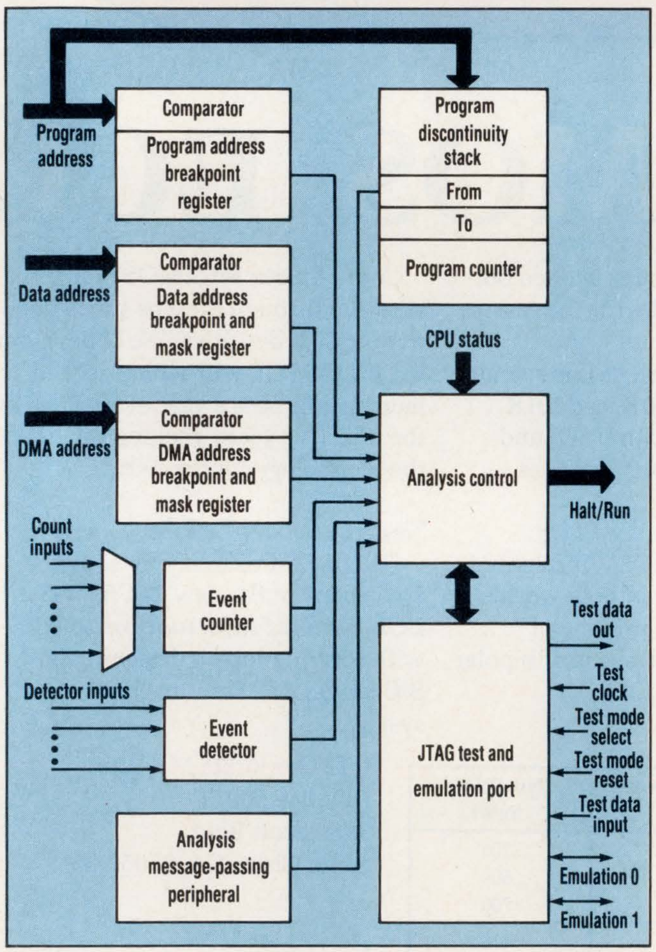
CIRCLE 191

spective throughputs of 50 MFLOPS and 25 MIPS. To ensure that the high throughput is maintained, TI's designers plan to add lots of memory—a 128-word-by-32-bit cache, a pair of 1-k-by-32 static RAMs, and a 4-k-by-32 ROM. Furthermore, to handle various timing and control operations, two timers were included as part of the chip definition.

The intelligent DMA-controller block on the chip is self-programming, minimizing its overhead requirements on the CPU. Rather than be totally controlled by the CPU, the DMA controller examines a task queue that the CPU sets up. That queue contains various DMA transfer requests. As the DMA coprocessor finishes one transfer, it checks the queue for another task. As many as three system operations can occur each cycle in the DMA coprocessor—a 32-bit data transfer, an address register update, and a transfer-counter update.



For many DSP chips, it's important to test the chip to ensure correct system operation. To simplify testing, the chip will include a full JTAG (Joint Test Action Group)-compatible test port. Many development tools that will be optimized for programming multiple chips in parallel are also being crafted. In addition, a complex analysis block was included on the chip to aid in system debugging. The block contains breakpoint comparators for program, data, and DMA accesses, a program-trace stack, and an event counter for benchmarking *(see the figure)*.

TI and several partners are developing an optimizing and parallelizing C compiler, assemblers and linkers with support to map the program and data to parallel processors, software behavioral models, and a version of the SPOX operating system that includes parallel processing support. Samples of the chip are expected in the second quarter of next year; software tools will appear in the first quarter. Contact TI at (214) 995-6611, Ext. 700; in the U.S., (800) 336-5236, Ext. 700.

DAVE BURSKY

SAMPLE-AND-HOLD AMPLIFIER ON VIDEO AMPLIFIER IC PERFORMS DC RESTORATION

An innovative IC improves the performance of conventional dc-restoration techniques (many of which introduce their own distortion) and cuts pc-board space. The EL2090 from Elantec Inc., Milpitas, Calif., holds a video amplifier and a sample-and-hold amplifier (SHA) *(see the figure)*. The chip is expected to help designers of electronic circuits for recording and broadcast-studio equipment.

Dc restoration of video signals in these studios is mandatory. A typical signal is routed through as many as two dozen separate amplifiers and/or gain-control blocks before reaching its final destination: magnetic tape or the airwaves. Each point along that route represents a potential source of distortion. With so many of these sources in series, the output signal at each point must be exceptionally clean. Gain-control circuits, in particular, can be distortional. Therefore, extreme measures must be taken to optimize their performance. Studio engineers often employ a simple trick. They position each gain control's video signal at its own unique "sweet spot"—the range of dc input offset voltages for minimum distortion.

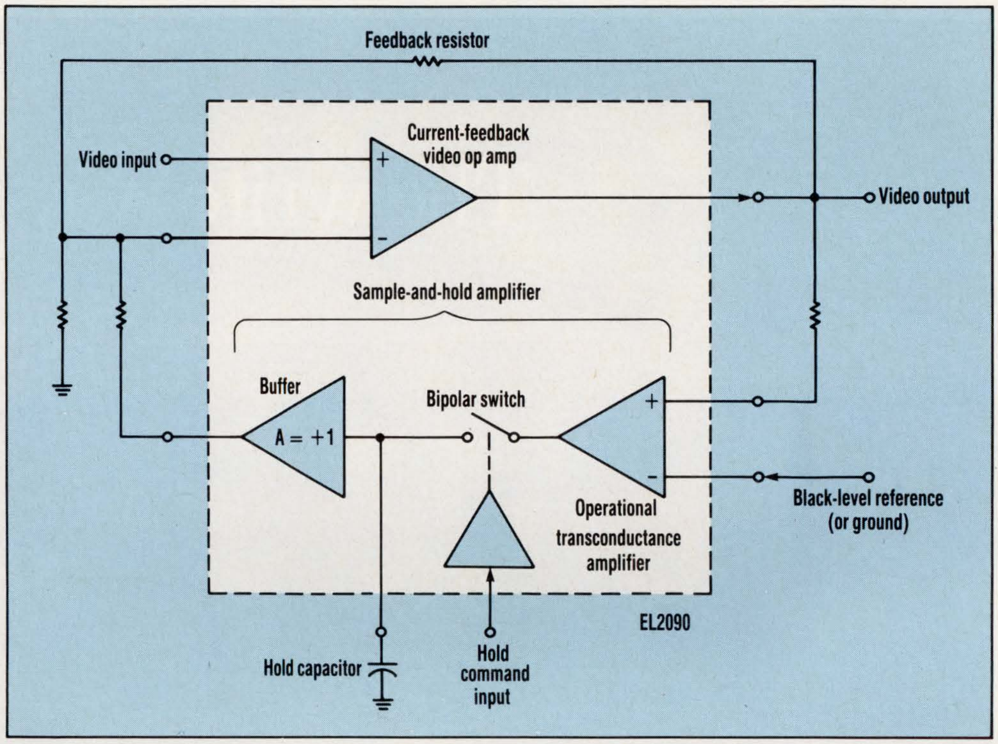
Though the technique reduces distortion, it causes other problems. If dc-coupled, the many cascaded circuits produce large dc offsets. If ac-coupled, the dc level is unknown and alters the signal's actual video content. Either way, dc restoration is required. In addition, the chroma-burst portion of the video signal must occur absolutely at a constant dc level. This is so the minute differential gain and phase aberrations in the circuits don't alter the chroma phase reference, which also takes dc restoration. As a result, the input to virtually every block in a video signal chain is dc-restored.

And dc restoration may be repeated several times within the block. Moreover, the process eliminates the effects of any 50/60-Hz noise that's picked up in cabling located between the blocks.

The Elantec chip is built on a complementary bipolar dielectrically isolated process. Its video amplifier employs a current-feedback architecture and offers a 3-dB bandwidth of 100 MHz. Once per video line, during the "back porch," or black period of the signal, the SHA compares the video amplifier's output level against a dc-clamp (black-level) reference applied to the SHA's minus input. The SHA stores the correction voltage that offsets the "back porch" to the clamp level on the Hold capacitor. It restores a 1.4-V output offset to zero in under 10 μs.

While the SHA logic-level Hold input is low, its plus input tracks the video amplifier's output. During the video-line period, the Hold input is high and the SHA holds the offset-correction voltage.

The chip is basically an autozeroed, video-bandwidth dc amplifier. It can be used for that purpose in various applications. In fact, it's the first time autozero techniques have been applied to a video or current-feedback amplifier.



The SHA's input stage is an operational transconductance amplifier (OTA) that converts the input voltage to a current that charges the Hold capacitor. By current steering, the bipolar switch switches from track to hold in under 2 ns. Although the output buffer is an open-loop complementary follower, the OTA, switch, and buffer form a negative-feedback loop around the video amplifier. At the same time, the Hold capacitor is charging. Because the capacitor is in the feedback loop, it charges accurately.

Additional specifications include differential gain and phase within 0.01% and 0.02°, respectively (at 3.58 MHz while driving 150 Ω and at 6-dB gain), and a 600-V/μs slew rate. Droop is less than 2.5 mV during a video line. The chip can put ±2.5 V across 50 Ω while operating from ±5 V, and ±12 V across 200 Ω running off ±15 V. Open-loop gain typically exceeds 60 dB. For more information, call Aki Kaniel at (408) 945-1323.

FRANK GOODENOUGH

HIGH-SPEED OPTICAL BACKPLANE TO BE MADE OF ORDINARY GLASS

Ordinary window glass forms the basis of a solid-state optical backplane system under development at the Institute for Applied Optics, Erlangen, Germany. The backplane will be used to interconnect circuit-card racks in high-speed data-processing and telecommunications applications.

To make the optical backplane system, scientists at the institute use a single glass sheet, on which they bond together holographic patterns, each 1-mm^2. The patterns direct 850-nm-wavelength laser lightbeams carrying data from a printed-circuit card into the glass.

By carefully calculating the hologram pattern, the beams are deflected at the correct angle to follow a "zig-zag" path through the glass. They're then reflected between the internal surfaces of the glass to provide optical data "pick-off" points at intervals along the surface of the glass sheet.

The two-year project is backed by the German government and by three leading European industrial companies, Siemens A.G., AEG A.G., and Alcatel SEL A.G. Dr. Norbert Siebl, project leader, says the purpose of the project is to produce a technology demonstrator with 16 parallel data tracks that are 1 mm apart, with each capable of carrying data at a rate of 100 Mbits/s over a distance of 1 m.

Once the laboratory development of the backplane is finished, the three participating companies will take over commercial development. So far, scientists at the Institute have made a laboratory prototype that proves the feasibility of the technology with a single 100-Mbits/s 10-cm-long connection.

PETER FLETCHER

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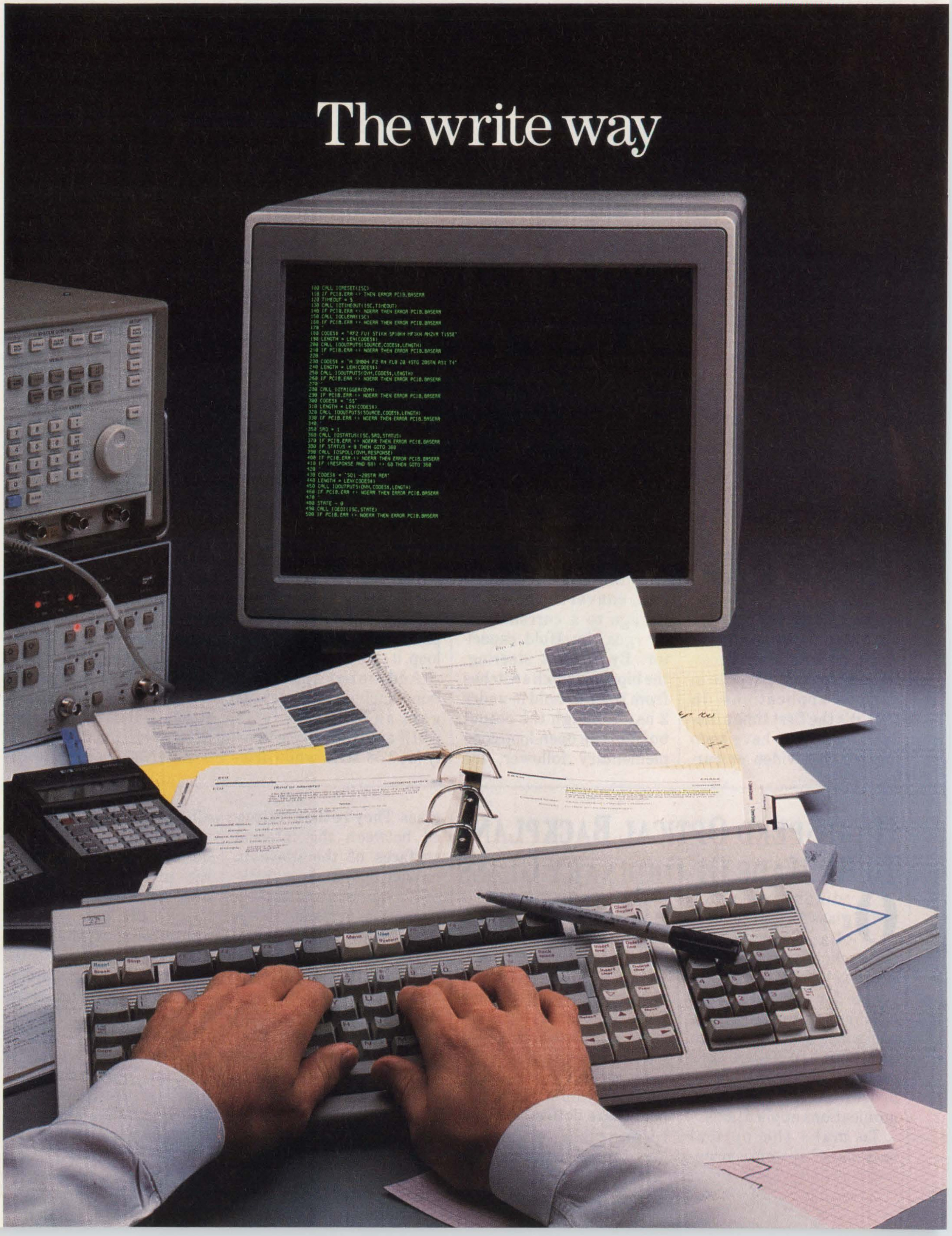

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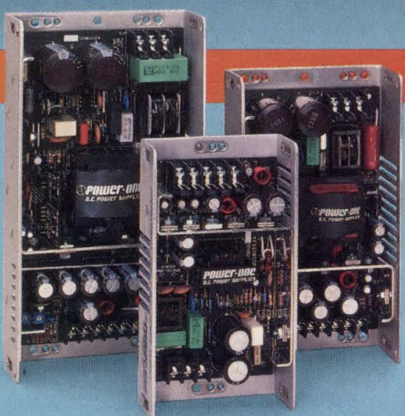

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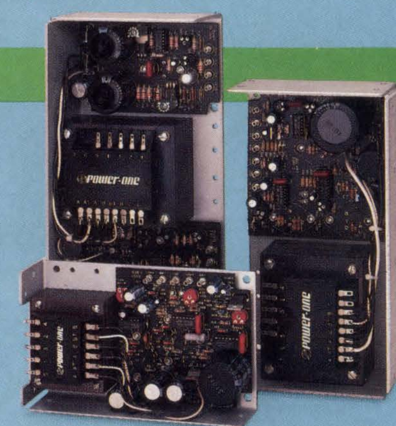

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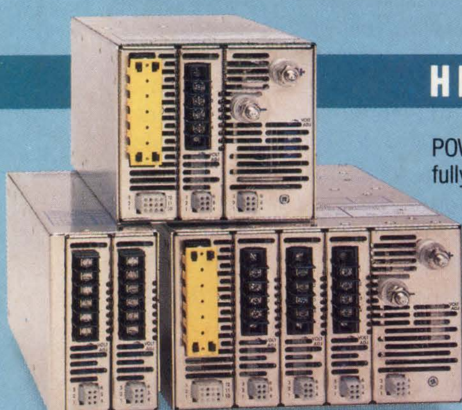

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CIRCLE 155

THIS YEAR'S FALL COMDEX WILL HIGHLIGHT PCS BUILT AROUND THE 486 CHIP AND MORE POTENT NOTEBOOK PCS.

POWERFUL SYSTEMS, LAPTOPS MUSCLE INTO SPOTLIGHT

RICHARD NASS

High performance is the key phrase when describing the latest wave of personal computers based on 80486 microprocessors, and laptops based on the 80386SX processor. These two growing areas will be the focus of attention at this year's Fall Comdex, Nov. 12 through 16 in Las Vegas. Moreover, the show's "high-end" slant will spill over into the technical program, where standards and networking are examined.

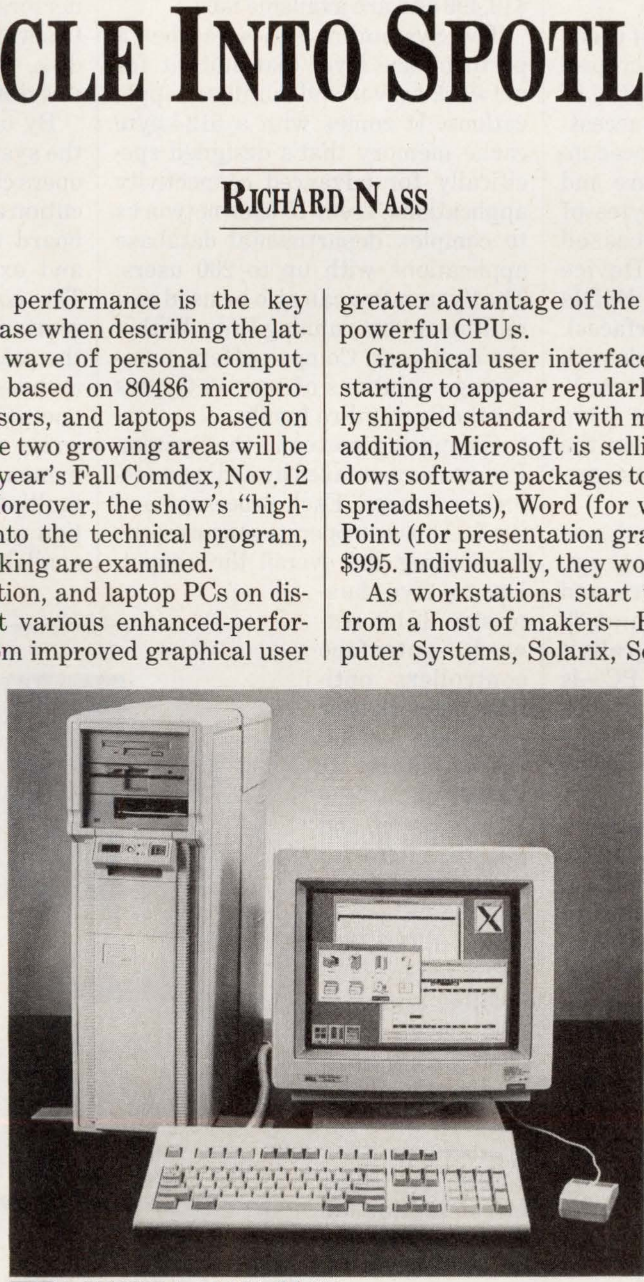
Desktop, tower-configuration, and laptop PCs on display at Comdex will exhibit various enhanced-performance features, ranging from improved graphical user interfaces to better networking capabilities to improved data bases. Many of these performance improvements owe their existence to the greater power of the 486 and 386 processors, the availability of software packages to take advantage of the processors' power, and improved peripheral products.

As the 80486 microprocessor continues to mature, systems built with this chip are becoming more prominent. The 486 (as well as the 386) contains a protected mode that runs software, like Windows 3.0 from Microsoft Corp., more efficiently. And the growing popularity of the Enhanced Industry Standard Architecture (EISA) bus is making the 486 microprocessor a more natural selection. This is because the chip can take greater advantage of the bus' functionality than less-powerful CPUs.

Graphical user interfaces, such as Windows 3.0, are starting to appear regularly in PCs. Windows is currently shipped standard with many PCs, not as an option. In addition, Microsoft is selling three of its popular Windows software packages together as one unit: Excel (for spreadsheets), Word (for word processing), and PowerPoint (for presentation graphics) combined now sell for $995. Individually, they would cost about $1500.

As workstations start to appear for under $10,000 from a host of makers—Hewlett-Packard, MIPS Computer Systems, Solarix, Solbourne Computer, and Sun Microsystems, among others—there's a push for desktop PCs to be more cost-competitive for the same set of performance features.

One PC-based system headed in that direction is the System 433TE from Dell Computer Corp., Austin, Tex. This tower system not only houses a 33-MHz 486 processor, but is also designed using the 32-bit EISA bus. The 433TE, with its 64-Mbyte main-memory capability, can be used as a Unix-based multiuser host system or as a work group or PC-network server. It incorporates a password protection that "locks" the system from unauthorized access.



1. WITH A 24-IN. CASE that fits under a standard desk, the System 433TE from Dell Computer Corp. can be used as a Unix-based host or as a PC-network server. This 33-MHz, 486-based system is based on the EISA architecture.

Although the 433TE is a tower configuration, it measures only 24-in. high, enabling it to fit comfortably under most desks *(Fig. 1)*. A lockable side panel gives users easy access to vertically mounted option cards. Cable connections are located at the top of the machine. Moreover, eight EISA expansion slots are available. An integrated 16-bit VGA adapter comes standard with 512 kbytes of RAM, and it displays up to 1024 by 768 pixels in 16 colors.

In addition to the 8 kbytes of cache memory built into the 486 microprocessor, Dell included 128 kbytes of external cache. Faster RAM accesses are achieved with an advanced interleaved-memory architecture and shadow RAM. Up to 1.6 Gbytes of hard-disk storage are accessed through IDE (Integrated Device Electronics) interfaces and ESDIs (Enhanced Small Device Interfaces).

The 433TE is fully compatible with MS-DOS, OS/2, and Unix System V. Prices for the 433TE range from $8949 to $17,599, depending on the configuration. A 25-MHz version—the 425TE—is also available.

Two other 486-based machines come from Compaq Computer Corp., Houston, Tex. Their DeskPro and SystemPro systems both run at 33 MHz. The DeskPro—Compaq calls it the most powerful desktop PC—is suitable for design automation, scientific analysis, software development, and resource-sharing workgroup environments.

To increase system performance, the machine is built around the EISA bus. The PC contains a second-level cache controller and 128 kbytes of internal cache memory to service up to 98% of all processor requests at zero wait states. An integrated floating-point unit performs compute-intensive math applications, such as finite-element analysis. A socket for an optional 33-MHz 4167 Weitek math coprocessor is supplied for extremely demanding applications.

The system is designed for configuration flexibility with its nine expansion slots: a 32-bit system processor slot, a 32-bit high-speed system-memory expansion slot, and seven full-size 32-bit EISA slots. But the EISA slots can also hold 8- or 16-bit boards. The DeskPro also incorporates Compaq's Flexible Advanced System Architecture that uses two buses, one for the microprocessor and memory subsystem and an EISA expansion bus for compatibility. Four Mbytes of enhanced page memory, expandable to 100 Mbytes, is standard. Three hard-disk sizes are available: 650, 320, and 120 Mbytes. The units range from $13,999 to $19,499 and are available now.

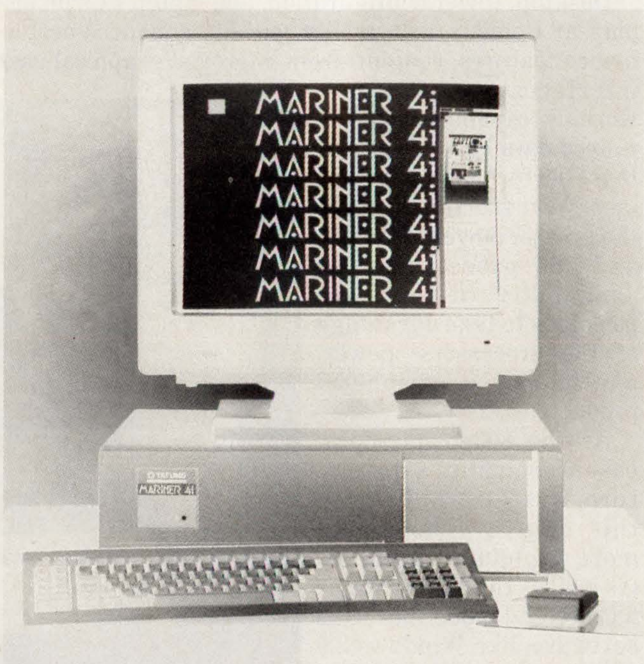
The SystemPro series reaches a performance level that suits it for network-server and multiuser applications. It comes with a 512-kbyte cache memory that's designed specifically for advanced connectivity applications, from 15-user networks to complex departmental database applications with up to 200 users. The SystemPro can also be used as a multiuser host running Unix. Within the next year, Compaq offers mass-storage solutions of over 10 Gbytes for the SystemPro family.

Computing power in the SystemPro can be increased by adding a second processor. Each processor and the I/O bus can operate concurrently, maximizing the overall throughput. Up to five bus-master 32-bit network - interface controllers optimize network-user response time. Prices start at $20,999 for a 240-Mbyte system and go up to $29,999 for an 840-Mbyte system.

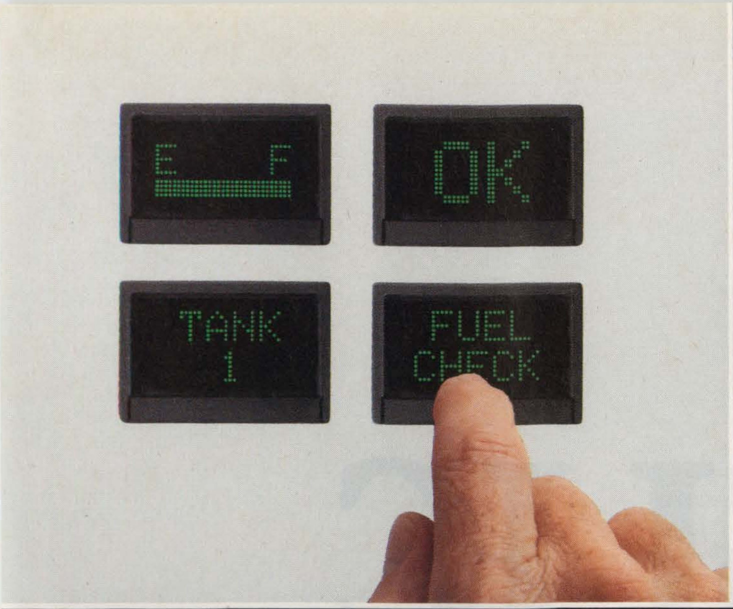
The DTC3290E SCSI cache controller, which is also designed for the EISA bus, supports a 32-bit burst bus-master transfer rate across the EISA bus at a maximum data-transfer rate of 33 Mbytes/s. The board, from the Data Technology Div. of Qume Corp., Milpitas, Calif., decreases the I/O bottle neck with 300 disk I/Os per second. And optional dual SCSI ports permit even higher speeds with parallel data transfer.

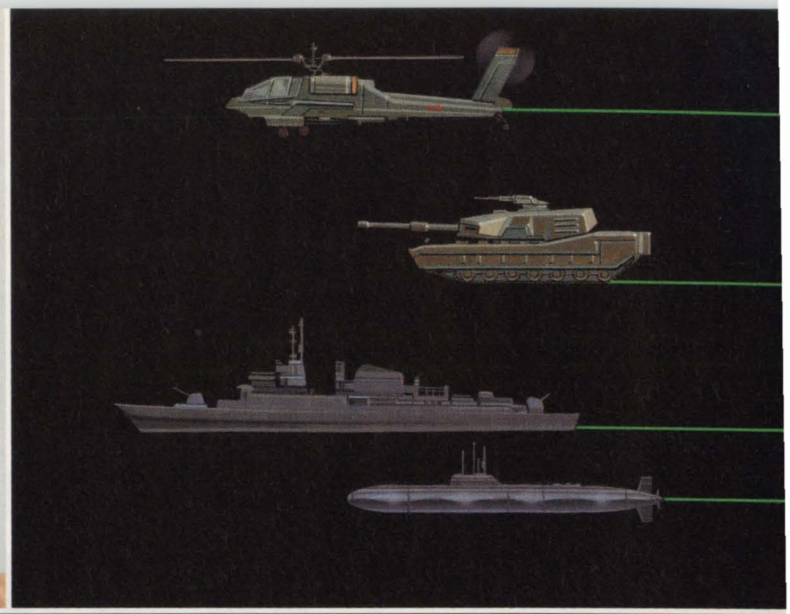
The controller board uses an Intel EISA BMIC (bus master IC) as the host interface chip, supplying optimum compatibility between the EISA system and controller cards. With internal and external SCSI connectors, the DTC3290E supports up to seven SCSI devices, such as a hard disk, tape drive, CD-ROM drive, or rewritable optical drive.

By using mailbox architecture as the system-interface protocol, developers can multithread command execution and queuing. This enables the board to fetch multiple commands and execute them simultaneously. The controller also supports data scattering and gathering through the mailbox architecture. With this architecture, the developer can issue one SCSI command to read and/or write data to and from different memory locations, rather than use multiple SCSI commands. Production quantities of the board will be available in January. It costs $895



2. ALTHOUGH SIMILAR to a SPARC workstation, the Mariner 4i, the result of a joint effort between Mars Microsystems and Tatung Co., can also operate as a PC running DOS. The optional DOS module contains a 386 processor and VGA graphics.





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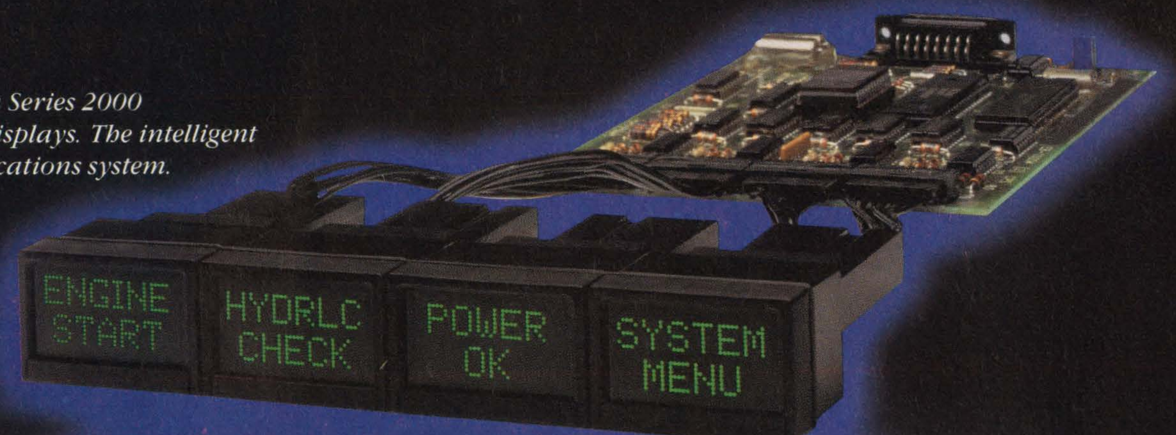

SERIES
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CIRCLE 85

with 512 kbytes of RAM; the dual-SCSI-port version goes for $995.

Intel Corp., Santa Clara, Calif., is releasing two 486 machines, one with the EISA bus and one with the ISA bus. Both systems support DOS, OS/2, and Unix. The 402 is a 25-MHz system that contains eight ISA expansion slots. It comes with 4 Mbytes of RAM and is expandable to 8 Mbytes. The 403E is a 33-MHz model that was designed as a server. It's more flexible than the 402—it has ten EISA expansion slots, up to 64 Mbytes of on-board RAM, and optional external cache memory. Either is available as a board or a complete system (the 402 as a desktop and the 403E in tower form).

Bridge The Unix-DOS Gap

A joint effort between Mars Microsystems, Mars, Pa., and Tatung Co., Taipei, Taiwan, resulted in a product that combines Sparc and PC technologies in one workstation *(Fig. 2)*. The Mariner 4i enables Unix and DOS application software to run on the same platform, both with full functionality. The system is basically a Sparc workstation in which users can add DOS compatibility with an 80386 microprocessor and VGA graphics. In addition, the PC applications run independently of the Sparc system.

The Mariner 4i runs Sparc/OS 1.0, a derivative of SunOS, Sun's version of Unix. This makes it fully compatible with the 2100 hardware and software solutions available for Sparc workstations. The system is built on a standard PC/AT-size motherboard, integrated on an ISA bus. Its 25-MHz Cypress Semiconductor Sparc CPU offers 16.8 MIPS of performance.

The DOS-processor module, which simply plugs into the motherboard, includes an independent 1 to 8 Mbytes of memory, 32 kbytes of cache, and an optional floating-point accelerator. A diskless unit with a 16-in. monochrome monitor costs $5995. With all of the extras, including the DOS module, the system sells for $10,995.

Oracle Corp., Redwood Shores, Calif., has released several database servers for PC Unix. They run on a full range of high-performance single- and multiprocessor PCs, including Compaq's SystemPro.

One server supports SCO Unix MPX and is the first implementation of native symmetrical multiprocessing (SMP) database management for the PC environment. SMP offers huge performance improvements over nonSMP or uniprocessor systems. As more processors are added to a system, SMP makes it possible for each processor to run a complete version of Oracle. This results in significant transaction-throughput gains as processors are added. This marks the first time SMP has been implemented on a PC.

3. CONNECTING TO A STATIONARY docking station is NEC's Prospeed SX/20, a 386SX-based laptop computer. With the docking station, users can add expansion cards, drives, or other peripherals through the interface slots.

Oracle servers for PC Unix are based on the company's relational database-management system (RDBMS) Version 6.0, which operates identically on more than 80 different hardware platforms. It requires a minimum of 6 Mbytes of RAM and 80 Mbytes of disk space. Prices begin at $5100 for a two- to eight-user single processor.

Intended for such high-end applications as network servers or CAD/CAM, the MAE486 from Mylex Corp., Fremont, Calif., is an 80486-based EISA system board that runs at 33 MHz. Its 128-kbyte external zero-wait-state write-back cache augments the 8 kbytes that are internal to the 486 chip. The board, with its PC/AT form factor, supports up to 32 Mbytes of DRAM. It's compatible with MS-DOS and Unix.

Mylex also developed three peripheral boards to go with the MAE486: the DCE376 32-bit caching SCSI host adapter, the LNE390 high-performance Ethernet LAN adapter, and the GXE020 high-resolution TIGA graphics controller, which is based on TI's 34020 graphics processor. The system board is priced from $4620 to $5200, depending on volume.

Peripherals, Too

To go along with these high-end systems, Fujitsu Component of America Inc., Santa Clara, Calif., released a high-resolution 18-in. diagonal ac-memory, plasma-display monitor. The FPF17000S standalone unit features a resolution of 1024 by 816 pixels and two-level gray scale. It's suited for workstations and PCs with split-screen and graphics-intensive applications. It has a contrast ratio of 20:1 and a 160° viewing angle.

However, these features don't occupy lots of space. The monitor boasts a 3-1/2-in. profile and weighs just 5 lbs. It comes mounted on an adjustable tiltstand for viewing comfort. Samples, available now, cost $4500. Production starts in January.

For higher performance, laptop makers, specifically notebook PC makers, will build their portable PCs with 386SX processors. Judging from the crop of 386SX-based lap-

TEXAS INSTRUMENTS

A PERSPECTIVE ON DESIGN ISSUES:

Creating systems with an analog edge

IN THE ERA OF

MegaChip

TECHNOLOGIES

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Challenge: Design a compact, cost-efficient direct broadcast satellite TV descrambler for consumer use.
Solution: TI's TLC5602 8-bit Video DAC. Our LinEPIC™ process combines one-micron CMOS with precision analog to satisfy the demands of the application for video speeds and low-power operation.

U.S. Robotics

Challenge: Build a modem for high-speed data transmission between computers; allow flexible operation and minimize data errors.
Solution: Our TLC32040 Analog Interface Circuit (AIC). A product of our Advanced LinCMOS process, the AIC combines programmable filtering, equalization, and 14-bit A/D and D/A converters with such digital functions as control circuitry, program registers, and a DSP interface.

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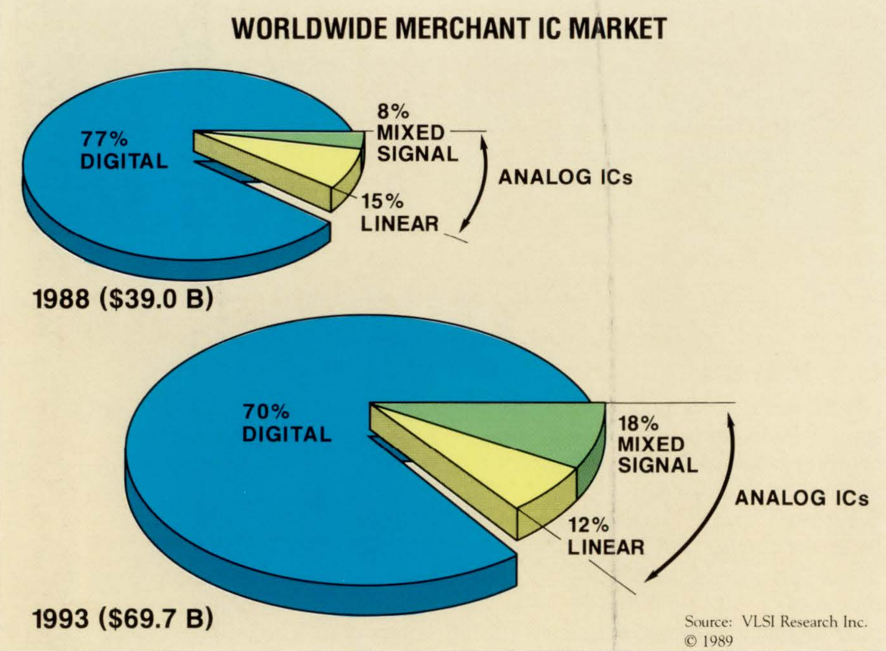
All of these examples point to one conclusion: TI's Advanced Linear functions are adding an analog edge to many system designs. They are contributing significantly to the enhanced system performance that marks a market winner.



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An increasing share of the total analog market is being captured by mixed-signal devices. As they gain more widespread acceptance, they are driving the expansion of the overall analog market (*see above*).

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TEXAS INSTRUMENTS

tops at the show, few sacrifice little if any performance when compared to their desktop counterparts.

One newsworthy entry is the TravelMate 3000 notebook PC from Texas Instruments. The PC, built at TI's Temple, Texas location, features a 20-MHz 80386SX microprocessor; a 10-in. diagonal black-on-white VGA display; a 1.44-Mbyte, 3.5-in. floppy-disk drive; and a 20- or 40-Mbyte hard-disk drive. All this fits in a box just 8.5 by 11 by 1.8 in., weighing 5.7 lbs. with the battery.

The display, taken from TI's TravelMate 2000, employs triple supertwist LCD technology. Its resolution is 640 by 480 pixels with 32 gray scales. This allows the computer to run such applications as Windows 3.0. It comes standard with 2 Mbytes of RAM that's expandable to 6 Mbytes in 2-Mbyte increments.

The PC comes with DOS 4.01 loaded onto its hard disk. Other software is also bundled, such as LapLink for easy data exchange with a desktop PC; BatteryWatch, which tells users how much life is left in the battery; BatteryPro, a battery conservation application; display utilities; and a laptop file-management system.

The removable nickel-cadmium battery holds a charge for about three hours. Standard features are a parallel and a serial port, interfaces for an external monitor, a mouse, and an external numeric keypad. Options include extra batteries and a 2400-baud modem with facsimile capabilities. The TravelMate 3000 costs $5199 and $5799 for the 20- and 40-Mbyte models, respectively.

Stiff competition for TI's TravelMate comes from the Premium Exec 23V and 43V PCs from AST Research Inc., Irvine, Calif. These notebook laptops are also built around the 386SX processor running at 20 MHz, and they come with either 20- or 40-Mbyte hard-disk drives. The PCs are 9 by 11.4 by 2.2 in. and weigh 6.5 lbs. A 1.44-Mbyte, 3.5-in. floppy-disk drive is standard, as is a 3-1/2-hr removable NiCd battery.

The Premium Execs' display is a cold-cathode fluorescent-tube backlit LCD that uses 32 shades of gray. It has a resolution of 640 by 480 pixels. The computer's 2 Mbytes of RAM are expandable up to 8 Mbytes; a 2400-baud modem is optional. The notebook PCs come loaded with LapLink, BatteryWatch, DOS 3.3, and some utilities from AST Research.

NEC, Wood Dale, Ill., tossed its notebook-PC hat into the ring with a 12-MHz 286-based model that weighs in at 6.5 lbs. The UltraLite 286V features a 10-in. backlit display with VGA resolution, 1 Mbyte of RAM expandable to 5 Mbytes, and a 20-Mbyte hard-disk drive. Its 2-1/2-hr. battery can be changed on-the-fly without any data loss, and can be recharged in four hours. The company's 286V comes with a RAM card slot for either proprietary NEC RAM cards or ROM-card software from third-party vendors. It's also bundled with an external 3.5-in., 1.44-Mbyte floppy-disk drive. The PC retails for $3699.

A second laptop from NEC is the ProSpeed SX/20. This 386SX-based machine, with dimensions of 10.6 by 13.4 by 3.4 in., is slightly larger than the UltraLite. It weighs 12.9 lbs. with the battery. Running at 20 MHz, the laptop plugs into a fixed docking station to supply instant desktop features *(Fig. 3)*. The docking station offers such desktop features as expansion slots, space for hard-disk, floppy-disk, CD-ROM, or tape drives, a full complement of peripheral ports, and a locking mechanism so that the complete two-piece unit also becomes portable.

The list of bundled software includes MS-DOS 4.01, an extended-memory driver, a DOS and user's guide, and a diagnostic utility. With a 40-Mbyte hard-disk drive, the ProSpeed SX/20 retails for $5999. The optional docking station costs $1199.

At the component level, Allegro Microsystems Inc., Worcester, Mass., has launched the 8900 family of mixed-signal ICs consisting of eight motor controllers and drivers. The first three parts from Allegro, the 8901/2/3, drive the three-phase brushless dc spindle motors used in hard disk drives for laptops and desktops. These chips combine back-EMF (electromotive force) sensing with power DMOS outputs and programmable control logic to supply drive makers with the control and system flexibility they need. In 1000-piece quantities, the chips range from $6 to $6.50.

Two other ICs designed to drive three-phase, brushless dc motors—the 8922 and 8925—are used in tape and hard drives, respectively. The 8925 specifies a continuous output current of ± 4 A to supply faster "up-to-speed" times. The 8922 is similar except that it specifies an output current of ± 3 A with an on-resistance of 0.25 Ω. The 8925 costs $8 and the 8922 $7.50, in quantities of 1000.

The last three parts, the 8931/32/58, are 5- and 12-V voice-coil ICs with sense FET outputs. The output current of the chips' on-board full-bridge amplifier can be determined through an externally applied control voltage or current. Each voice-coil IC is priced at $6 in 1000-piece quantities. All eight devices can be had in low-profile packages suitable for surface mounting. They're available now in sample quantities with production to start in January.

By glancing at the technical conference schedule for Comdex, it's easy to see that it's becoming a high-end show. You'd almost think it was a workstation show rather than a PC show. One session revolves around standards. PC makers never were too concerned with standards. But now that the PCs are reaching workstation performance levels, the makers are having the same concerns as their workstation counterparts.

A second Comdex technical session is titled "Network Computing, The Challenge of the 90s: Client-Server Applications Come of Age." This indicates that high-end PC makers are feeling the heat from the low-end workstation makers. Workstations always had a decided advantage over the PCs as far as networking goes. Now, PCs makers have more reason to go to battle.□

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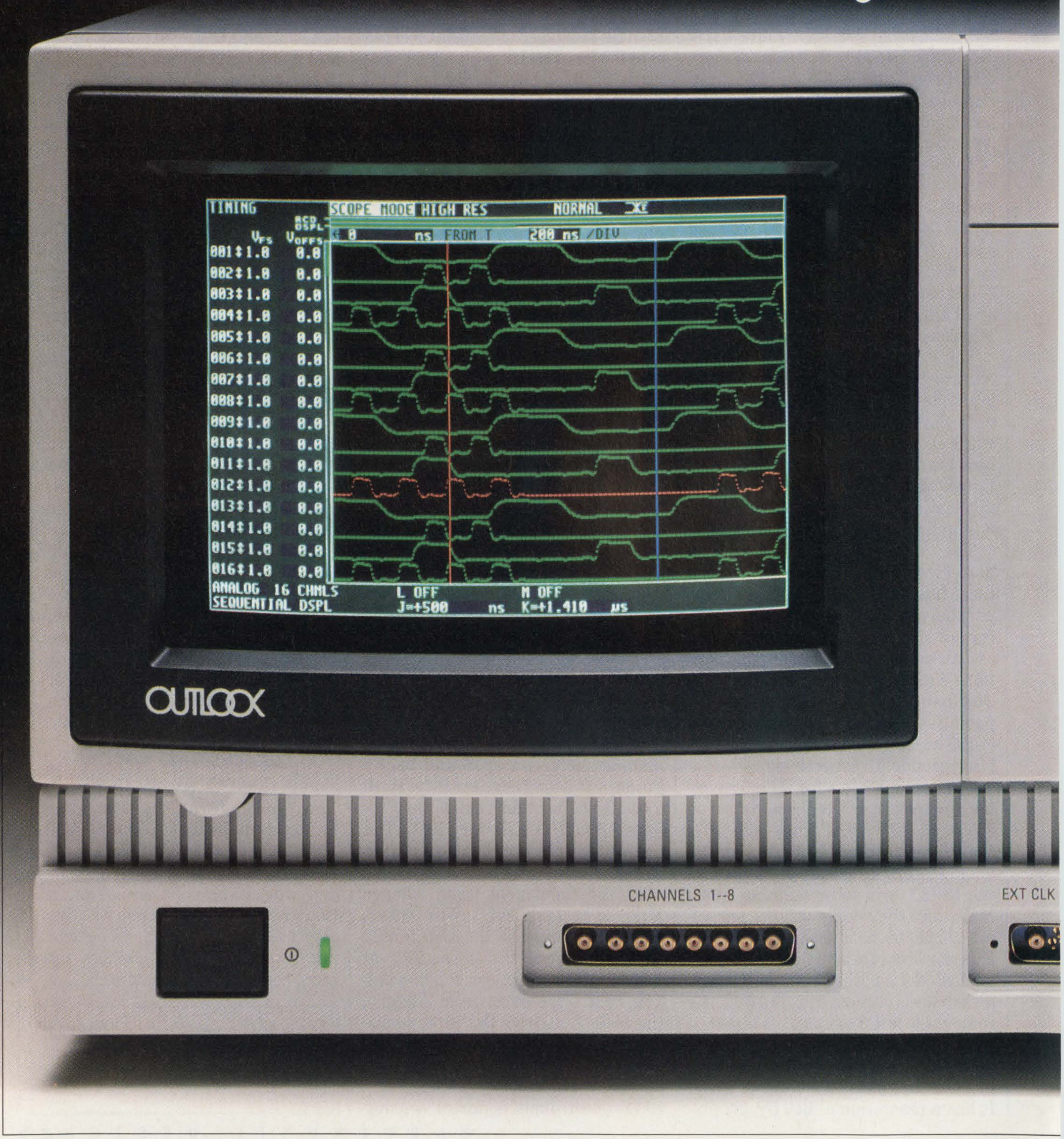

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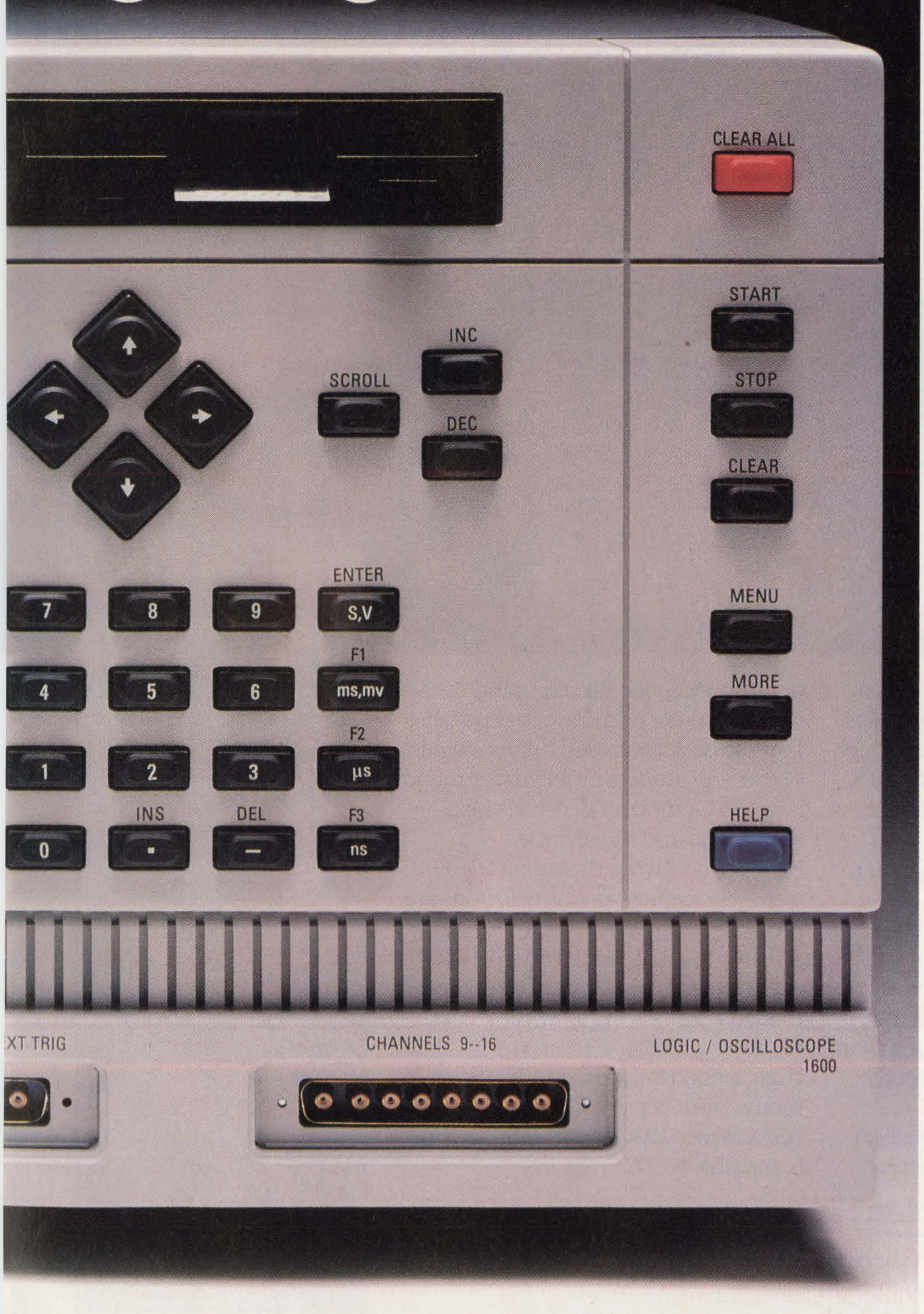

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CIRCLE 98

The First Embedded Controller Based On The Sparc Core Packs Caches, Peripheral Functions, And Enhanced Math For Faster Control.

Register Windows Speed Real-Time Control Tasks

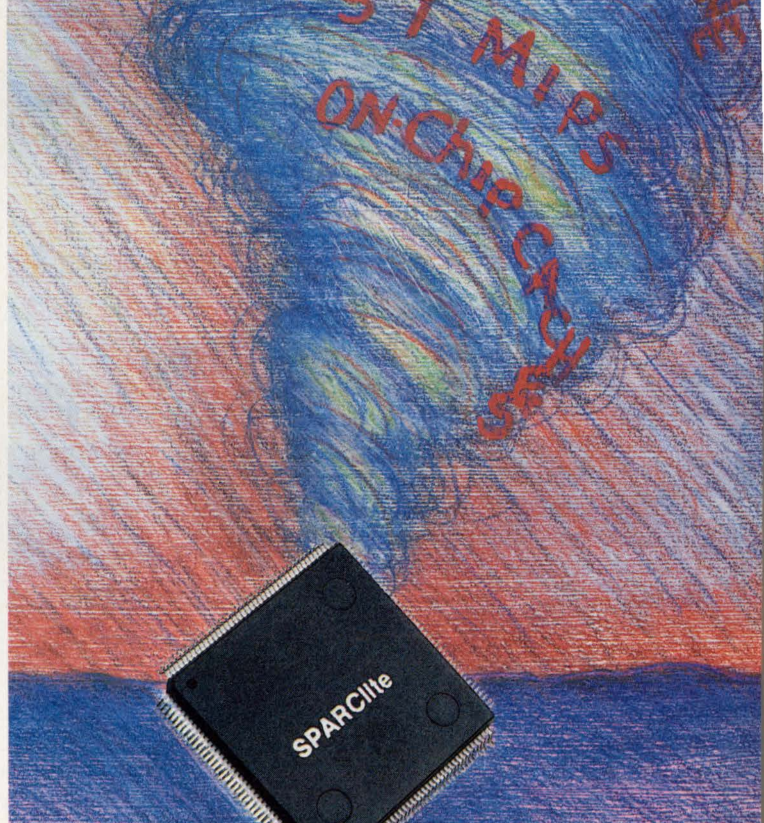
Dave Bursky

Although high-speed RISC processors satisfy the throughput needs of embedded-control systems, most RISC-based systems can't meet the board area and cost restrictions imposed by the applications. Fast responses to interrupts, high-speed math computations, and high levels of system integration are all key to taking on tough applications and meeting them with processing power to spare.

As a supplier of general-purpose Sparc processors licensed from Sun Microsystems, Fujitsu took note of the benefits and shortcomings of the current Sparc implementations. Fujitsu enhanced the best features of its previous Sparc processor by instituting a five-stage pipeline that achieves close to one cycle per instruction for most general-purpose code. It also improved the instruction set and integrated many of the off-chip circuits onto the processor chip. An eighth register window was added for more flexible task switching. All of these enhancements were incorporated into the MB86930, a new processor chip that becomes the first member of the company's Sparclite family. A soon-to-arrive multifunction companion support chip, the MB86940, has also been designed.

The processor will be offered in speeds of 20 to 40 MHz (18.5 to 37 MIPS). When idling, its static CMOS logic keeps system power drain to a minimum. This is because the clock can be stopped without losing data held in on-chip registers. On-chip instruction and data caches of 2 kbytes each store the most critical data or instruction loops for fastest access *(see the figure)*.

Unlike direct-mapped caches on some re-



cently released high-integration RISC processors, the MB86930's caches are two-way set-associative. As a result, they produce a higher hit rate while imposing a penalty of just a few tag bits per word.

Separate instruction and data caches of 2 kbytes each give designers what the company expects to be the best trade-off between chip cost and performance benefits for most embedded applications. A majority of high-volume embedded applications have only a small amount of code that benefits from being executed from a cache—tight inner loops forming the bulk of most compute-intensive algorithms. The processor's internal Harvard architecture coupled with the caches makes it possible for two words to be pulled simultaneously from the caches. That, in turn, enables the CPU to achieve a very low cycles-per-instruction ratio without resorting to superscalar circuit approaches.

Cache is also important when storing small amounts of interrupt service code to minimize interrupt latency. To that end, the instruction cache was designed to permit each 4-word line of the cache to be "locked" (write protected), so that normal cache updates won't overwrite the key routines or data. Because a two-way set-associative organization enables a memory location to be mapped into either of two cache entries, the cache can still work effectively even if one of the two entries is locked. Consequently, one entire bank (1024 bytes) can be locked. The remainder can be kept as a fully functional direct-mapped cache. Furthermore, the data cache can be locked. In that case, locked entries are treated as local scratchpad RAM—writes to locked locations aren't reflected externally to off-chip memory.

Many Registers

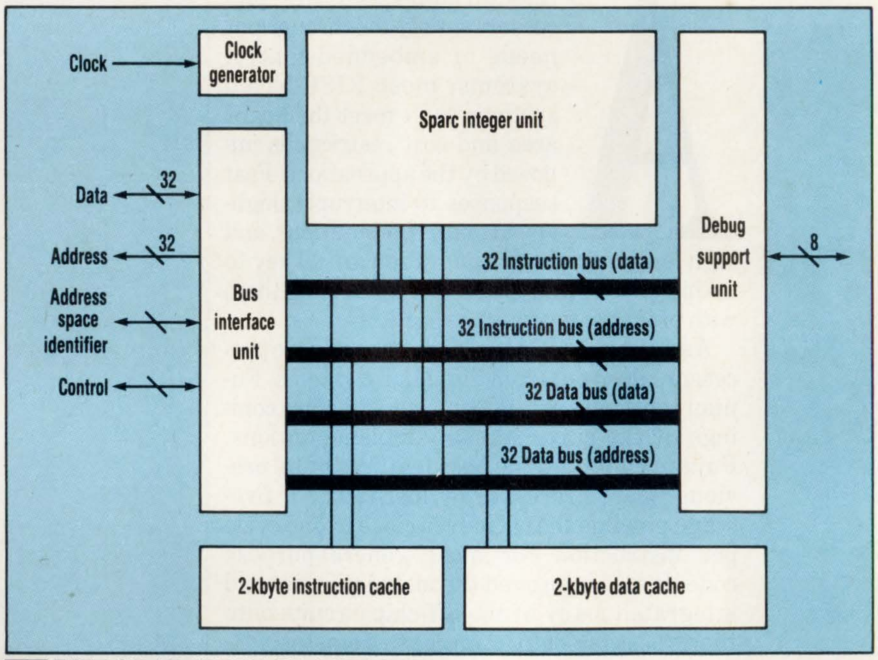
A total of 136 registers, each 32 bits wide, are included on the Sparclite processor. The registers appear to users as eight overlapping banks (or windows) that consist of 32 registers—eight are "global," and remain the same in each of the windows. Unlike simple microcontrollers that just switch entire banks of registers, the Sparc architecture employs a more sophisticated approach. In the register windows approach, key parameters can be transferred from task to task without rewriting them into the register file. This is possible because eight registers of the current window are accessible in the next window. Thus, only 16 registers change when windows change. The 16 registers take on slightly different characteristics, depending on which window they were in and the window that they're currently in.

With such a windowing system, C procedure calls and task switching can be implemented efficiently. The calling program can write parameters that are passed into the "out" registers portion of the 16 registers. When the window changes, those parameters appear in the "in" registers. Nothing actually moves, only the register names change to match their task in the window. That eliminates the memory overhead associated with writing and reading parameters, and effectively caches the top of the C run-time stack in the hidden register windows.

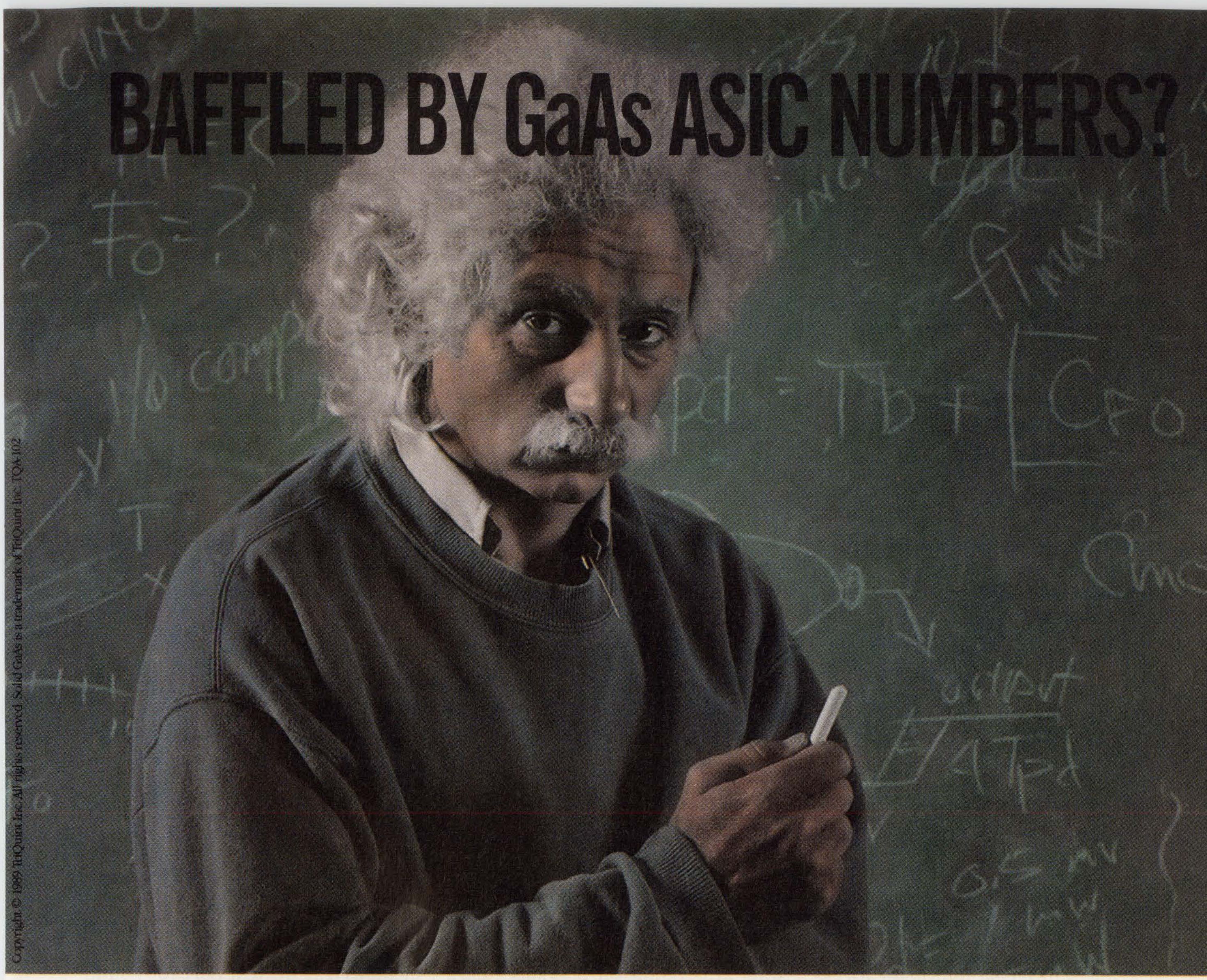
To readily handle real-time control applications, interrupt latency must be extremely short—just four cycles are required by the MB86930 from the time the trap instruction is fetched to when the trap target is fetched. At 20 MHz, that translates to about 200 ns. With the automatic decrementing of the current window pointer during a trap, a trap service routine can execute quickly. This can occur because it has at least eight registers that are unable to impinge on the user's process that trapped. The trap service time is also low because there's very little state information that the trap service routine must save in order to reenter the trapped program (just the program status register and the Y register need be saved—and only if the service routine or another trap service routine will alter those values).

Furthermore, by using the Window Invalid Mask instruction, supervisor code can segment the register set into a smaller number of window sets. This reduces the number of windows, and thus the number of consecutive Save operations without a window overflow trap. In turn, users can trade off between the nested procedure call time and context or process switch time, if the process is a real-time event service routine and it's desirable to reduce the process switch time.

The processor chip also includes a clock generator that requires just an external crystal (alternatively, a simple single-phase clock can be sup-



THE SPARCLITE PROCESSOR takes advantage of a full Harvard architecture internally, which enables the integer unit to simultaneously pull both data and instructions from the dual 2-kbyte caches. The bus interface block not only provides full 32-bit data and address buses, but also supplies all of the timing needed for DRAM subsystem control.



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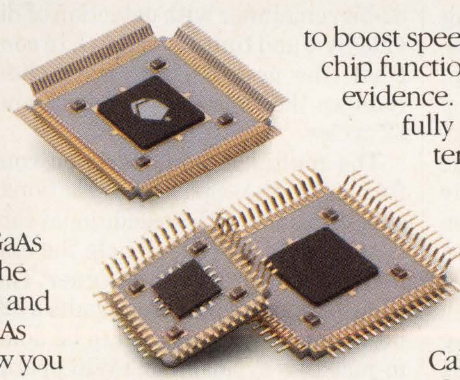

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CIRCLE 180

plied to the chip), and a dynamic-RAM interface and address decoder. The DRAM block contains eight programmable wait-state generators. It also contains another eight programmable chip-select lines that simplify the attachment of off-chip, low-cost DRAMs.

Special page-mode detection logic helps minimize the cache-miss penalty. Each time there's a cache miss, a worst-case assumption is that the first word accessed is in a new memory page. That typically isn't the case, because most code is sequential: If instruction n caused a miss, instruction n+4 will also cause a miss (a cache line is four words long). Because pages in external DRAM are much larger than the 4-word cache-line boundary, the fetch of instruction n+4 can often be treated as a page-mode address. The circuits included as part of the cache subsystem will take advantage of such cases automatically, treating the DRAM page as if it were a secondary cache memory.

MULTIPLIER ADDS POWER

More computational power was embedded in the Sparclite by adding a 32-bit multicycle multiplier (organized as 32-by-8) and several multiplication instructions, a Scan command, and an improved division capability (a new Divide-Step instruction) to accelerate physical data processing. Multiplications, along with additions and the combined multiplication-accumulation operation, are workhorse operations in many control algorithms in linear, quasi-linear and non-linear domains. The on-chip multiplier allows the MB86930 Sparclite chip to perform floating-point emulations with a throughput of about 1 MFLOPS.

To see the improvement in throughput, consider the following example of the previous MB86901 Sparc integer processor. An MB86901 converts 8-bit pixels from red, green, and blue planes to 8-bit pixel intensity planes over a 1024-by-1024-pixel image. When running at 20 MHz, the MB86901 requires 2.57 seconds to do the operations when it uses 0-wait-state static RAM to hold the data.

In contrast, the MB86930 needs just 0.93 seconds, and requires much-less-expensive 1-wait-state DRAM to hold the data. Thanks to the multiplication instruction, the pixel-conversion routine needs only 32 words of storage. And it can be held in a locked portion of the cache for maximum speed.

Scan is a new single-cycle operation that examines a register to see how many leading bits are the same; then it returns the count. The equivalent operation done with standard Sparc instructions would require between 43 and 52 clock cycles. The new Scan instruction peeds the software floating-point post-normalization so that the integer unit can take care of floating-point operations during initialization and outer-loop execution. The scan operation also accelerates interrupt selection and run-length encoding for compression.

The Divide-Step instruction improves division speed over the original Sparc integer unit considerably, with a minimal impact on hardware cost. It performs a one-bit cycle of a non-restoring shift-before-add, signed or unsigned division. The standard coding on previous Sparc processors requires between 243 and 258 cycles to perform the division of a signed 64-bit number by a signed 32-bit number (and obtain a signed 32-bit quotient and correctly signed 32-bit remainder with detection of divide-by-0 and finite overflow). In contrast, the new Division instruction reduces the time to between 48 and 62 cycles.

The multiplication operation conforms to the Sparc International specifications with an additional early terminate feature to help the embedded-control system designer. The early terminate feature permits a 32-bit-by-8-bit multiplication to be done in just two cycles, a 32-by-16 operation to be completed in three cycles, and a 32-by-32-bit multiplication in just five cycles.

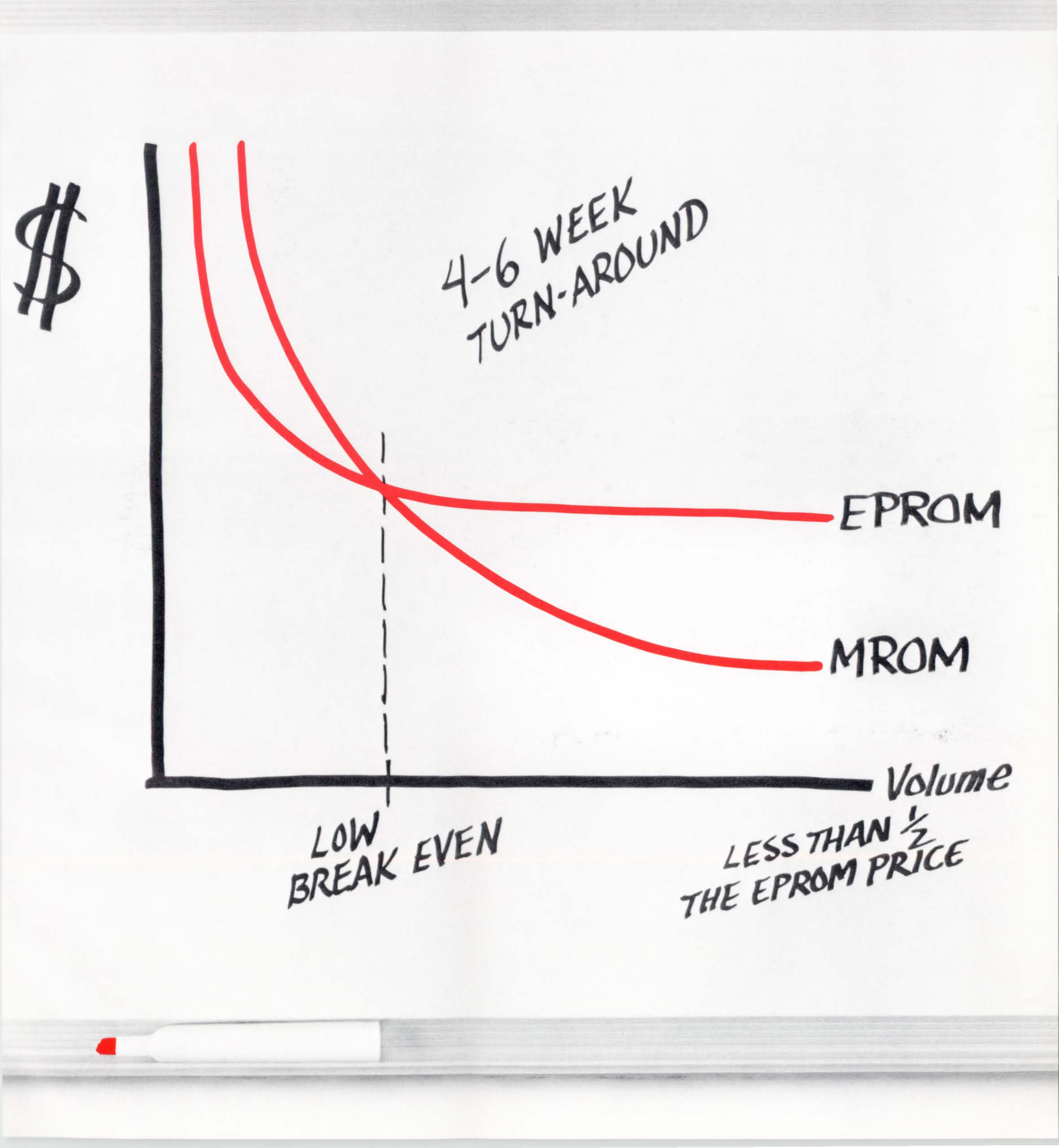
Four variations of the multiplication instruction actually exist: unsigned multiply, signed multiply, unsigned multiply and modify condition code register, and signed multiply and modify condition code register. By using condition codes, multiplies can be programmed more efficiently when products aren't more than 32 bits wide. In addition, the codes still retain the ability to detect and handle exceptions.

To make systems easier to debug, Fujitsu's designers included a separate 8-bit analyzer bus on the Sparclite chip. The bus, which carries coded bus-trace information to an emulator, is needed because the on-chip caches of the processor hide lots of bus activity from the outside world. The separate bus also makes the emulator connection non-intrusive to the system side of the processor. As a result, any loading or other performance-deteriorating effects are eliminated from the host system.

The chip also contains hardware breakpoint registers that, when used with target monitors to generate complex breakpoints, further aid in program debugging. There are two registers for instruction breakpoints, two for data address breakpoints, and two others for data-value breakpoints. To ensure that board-level systems are testable, the chip includes a JTAG test port for boundary-scan testing.

In control systems, the compute subsystem must often perform other tasks, such as interrupt control, counting and timing, and data communications. The MB86940 companion chip will offer all of this support integrated into one 100-lead quad-sided flat package. The chip will include an interrupt controller that deals with 15 interrupt requests. It will have a selectable interrupt trigger and both masking and polling registers. Four 16-bit counter-timers will also be incorporated, each with a programmable prescaler. Each timer can respond to either an internal or external clock, and each has its own capture and compare registers. Inputs can respond to a wide range of trigger events, while the timers deliver a wide range of pulse or level outputs. In addition, a pair of universal synchronous/asynchronous serial ports are integrated on the chip. Each is 8251-compatible and can be

Take Advantage of Sharp Mask ROMs.

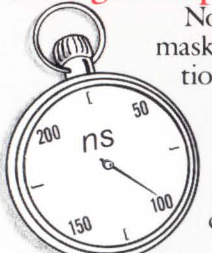


Whatever nonvolatile memory path you should be heading

To Sharp. The world

You've chosen mask ROMs for their density. But now you can choose them for their high speed as well. And you can choose the best of both worlds in one place. Sharp.

Setting New Speed Records—And Getting Faster.



Now available from Sharp: a 100-ns, 4-Meg mask ROM. That's a speed/density combination unprecedented in the industry. But that's only the beginning.

This milestone is one step on a technology path initiated by Sharp to produce ever-speedier mask ROMs. The key is a chip design focused entirely on speed.

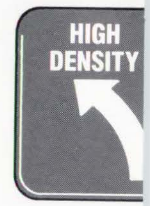
Sharp will take this layout to new speed levels in the 1990s. Look for a 35-ns, 1-Meg mask ROM from Sharp as early as the end of 1990.

And Sharp will continue on this unrivaled speed path for years to come. You can look forward to a new generation of mask ROMs, reducing wait state requirements. All available in a wide range of standard DIP and leading-edge surface mount packaging, for maximum design flexibility.

Sharp High-Speed Mask ROMs

1 Meg	Max Speed	Org.	DIP	QFP	SOP	PLCC	Intro.
LH530800	150 ns	x8	32		32	32	
LH530xx	35 ns	x8	32				2H90
LH530xx	55 ns	x16	40	44			1H91
2 Meg							
LH532300	150 ns	x8	32		32	32	
LH532L00	120 ns	x8	32		32	32	
4 Meg							
LH534300	150 ns	x8	32		32	32	
LH534500	150 ns	x16	40	44			
LH534L00	120 ns	x8	32		32	32	
LH534600	100 ns	x16	40	44			
8 Meg							
LH538xxx	150 ns	x16	42	64			1991
LH538xxx	150 ns	x8	32		32		1991

Setting New Density Records—And Delivering Lowest Cost Per Bit.



Now available from Sharp: a 16-Meg mask ROM at 200ns. Another milestone in the industry. The key is a totally different die. And a totally different technology called Flat Cell.

With greater and greater densities in mind, Sharp has produced a cell half the size of its high-speed counterpart. But while some speed has been traded off for die size, Sharp's higher-density mask ROMs are pretty speedy as well (see table that follows).

Moreover, in addition to producing a record-setting 16-Meg mask ROM, the effort has delivered extremely cost-effective 4-Meg and 8-Meg versions, now in volume production. All exemplify Sharp's commitment to deliver what many system designers consider their most important requirement. Lowest cost per bit.

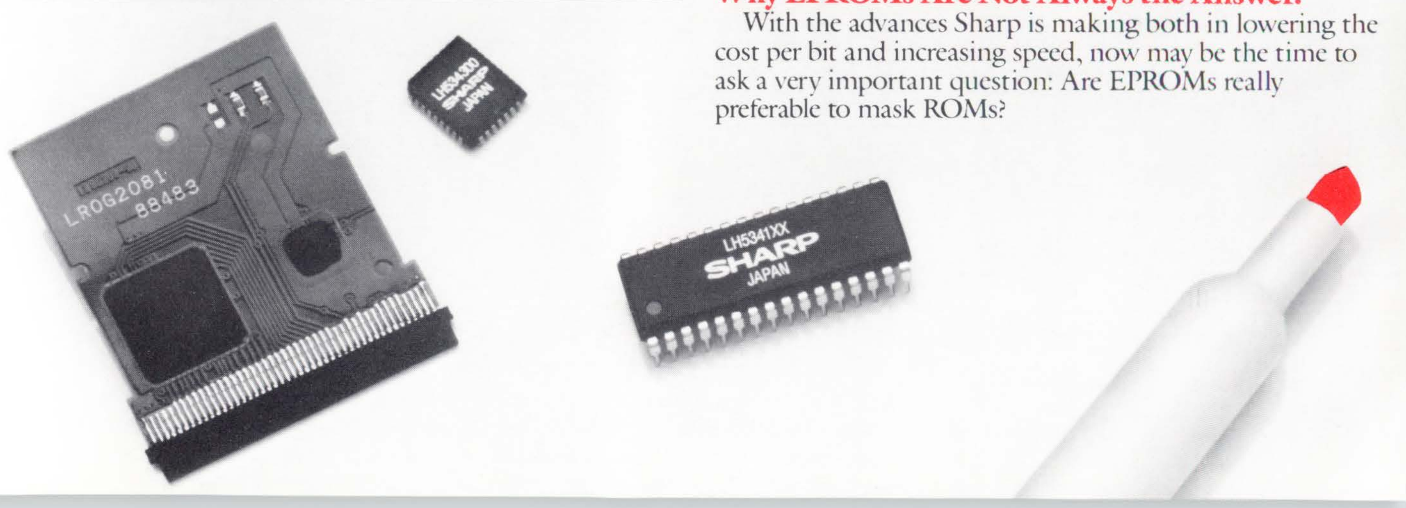
And the commitment to delivering lowest cost per bit is long-term. Even now, Sharp designers are working on a 64-Meg mask ROM for the early 1990s. So you know you can always depend on Sharp to deliver ever-denser mask ROMs. And ever-lower cost per bit.

Sharp High-Density Mask ROMs

2 Meg	Max Speed	Org.	DIP	QFP	SOP	PLCC	Intro.
LH532000B	200 ns	x16	40	44			
LH532100B	200 ns	x8	32		32	32	
4 Meg							
LH534000B	200 ns	x16	40	44			
LH534100B	200 ns	x8	32		32	32	
8 Meg							
LH5380xx	200 ns	x16	42	64			
LH5381xx	200 ns	x8	32		32		
16 Meg							
LH531600	200 ns	x16	128				2Q90

Why EPROMs Are Not Always the Answer.

With the advances Sharp is making both in lowering the cost per bit and increasing speed, now may be the time to ask a very important question: Are EPROMs really preferable to mask ROMs?



ou're on–highest density or speed–
n one direction.
eader in mask ROMs.

For many of you, the answer is now no. It's time to re-examine conventional thinking about EPROMs.

For example, if your code is stable and your annual volume is moderate, then you simply can't afford *not* to consider Sharp mask ROMs.

One of the advantages that EPROMs have over mask ROMs is their ability to be erased and reprogrammed. However, for most users the flexibility that makes EPROMs a lot more expensive than mask ROMs will never be needed. And if your code is stable, a lot of money will have been wasted.

Moreover, as you know, even if field changes are required, most EPROM users won't reprogram the units in the field. Instead, the EPROM will simply be dumped and replaced. And considerably more expense will be added.

Because mask ROMs are custom parts, another alleged EPROM advantage is the ability to inventory the unprogrammed devices. However, the ability to stockpile master EPROMs is increasingly being offset by the cost incurred by the system manufacturer who must program the EPROMs on his factory floor.

Why Sharp Mask ROMs Are the Answer.

Now consider some clearcut advantages you will get with mask ROMs. Thanks to Sharp.

For one thing, mask ROMs have always been much denser. But Sharp has made that density advantage even more pronounced—and it will only get greater. This is good news for those users who would need to use multiple OTP EPROMs to satisfy increasing bit requirements. With Sharp's extensive line of high-density mask ROMs, no problem. Simply use one high-density Sharp mask ROM instead of multiple OTP EPROMs. And also lower your cost per bit to levels that EPROM users can only dream about.

Moreover, through Sharp's creation of and commitment to a speed path, mask ROMs no longer suffer a speed disadvantage. You can look forward to new generations of high-speed mask ROMs. And with greater densities than EPROMs. From Sharp.

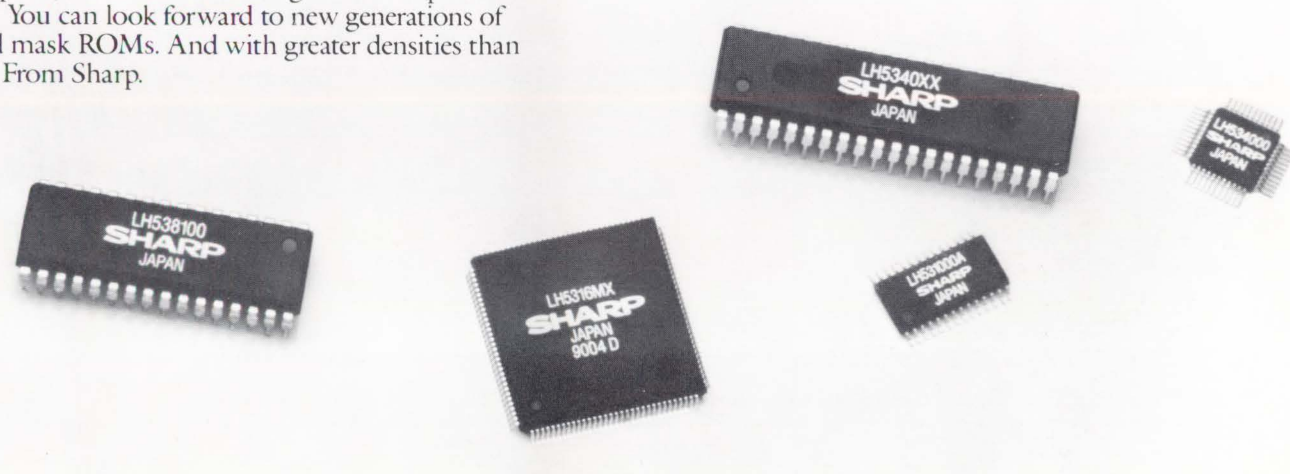
Take Advantage of Sharp's Unrivaled Mask ROM Development.

When you come to Sharp, you can take advantage of our unrivaled leadership in developing distinctive, leading-edge speed and lowest-cost-per-bit (density) paths. And you can choose from a wide range of high-speed or high-density products. Right now.

Whatever mask ROM technology path you require, you will capitalize on several features that have helped make Sharp a world leader in mask ROM development:

- **Simple Processing.** Sharp uses a single-poly, single-metal process for all its mask ROMs to keep costs down. You know you can look forward to new, cost-effective generations of higher-density and higher-speed mask ROMs.
- **Fast Turnaround Time.** Expect initial quantities within 4 to 6 weeks. Not the usual 12 to 16 weeks. And at a fraction of the cost of EPROMs. The reasons: late programming (pre-metal)—even on the highest-density parts—along with fast, U.S.-based satellite code transfer, combined with speedy in-house mask making and assembly/testing.
- **Wide Selection of Leading-Edge Packages.** This includes JEDEC standard DIPs most common for EPROMs. But at Sharp, high-density PLCC and even higher-density QFP and SOP surface mount packages are all standard. And COB and TAB are available on request.
- **Rock Solid Customer Support.** Whatever technology path you're on—speed or density—you can count on Sharp to meet our commitment to deliver what we promise to deliver. Speed or density. Every time.

To find out more about Sharp's full line of mask ROMs, call: 1-201-529-8757 • FAX: 1-201-512-2020. Or write to: Sharp Electronics Corp., Microelectronics Division, Sharp Plaza, Mahwah, New Jersey 07430.



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SPARC-BASED EMBEDDED CONTROLLER

programmed for stop bit, parity, character length, and baud rate.

If users don't want to use the new multiplication commands, all previous software development tools can be employed to develop application programs. Some of those tools include native (Sun-4) and cross tools (Sun-3 and IBM PC and compatibles)—C compilers, linkers, loaders, librarian, libraries, target monitor, and so on.

For additional software, Fujitsu struck a deal with Microtec Research Inc., Santa Clara, Calif., for that company to develop a high-performance compiler that applies interprocedural data-flow analysis and run-time feedback, as well as other optimizing techniques. An evaluation board containing the 40-MHz processor, 4 Mbytes of 80-ns DRAM, 128 kbytes of EPROM, an 8-bit parallel port, two serial ports, 32- and 16-bit timers, various indicators, and an expansion port will be ready in the second quarter of 1991.

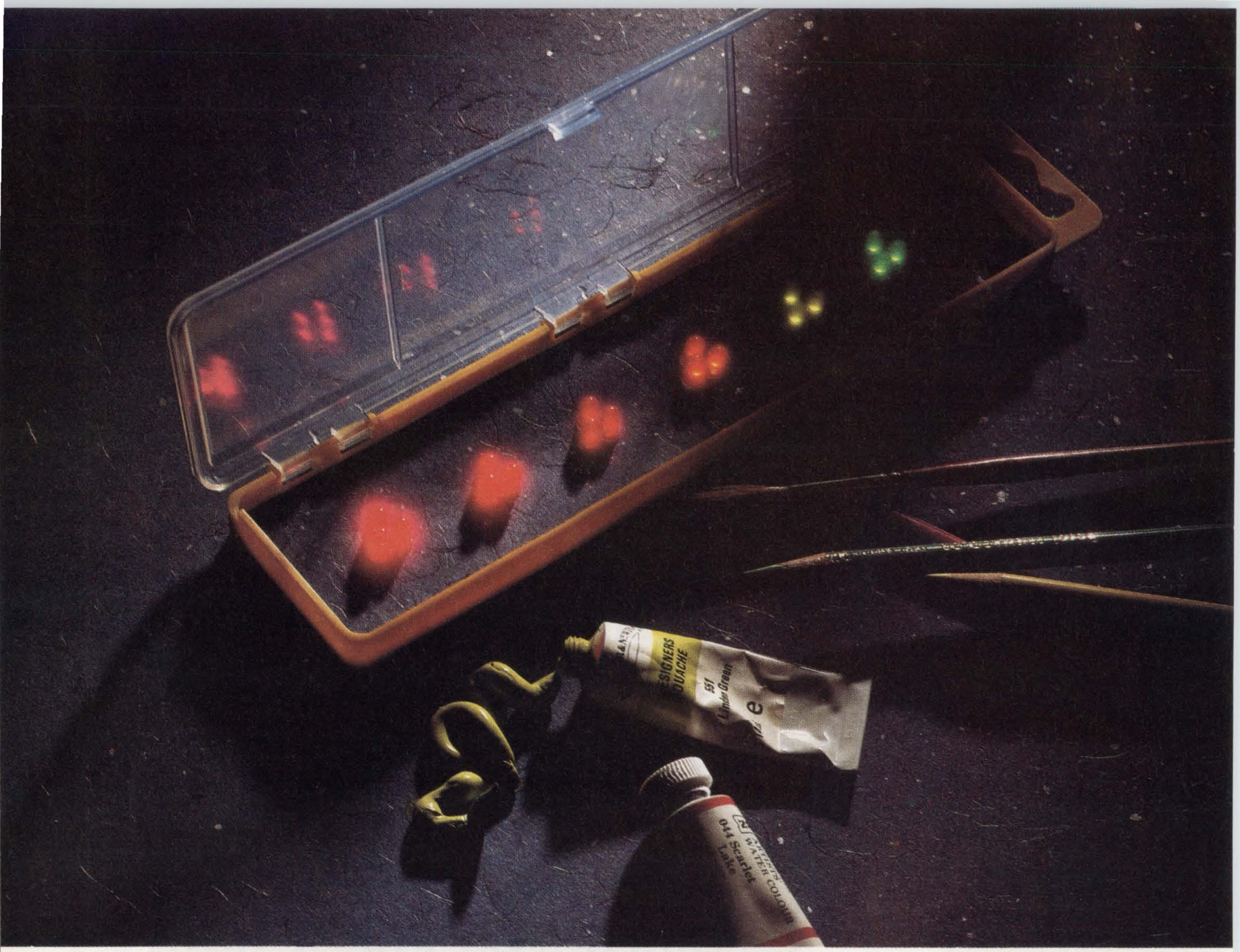
Microtec will also develop a version of its XRay source-level debugger that's compatible with native host, architectural simulator, execution vehicle, and hardware emulators. Furthermore, real-time operating systems are also available from Wind River Systems Inc., Alameda, Calif., Ready Systems Inc., Sunnyvale, Calif., and JMI Software Inc., Spring House, Penn. Step Engineering Inc., Sunnyvale, Calif., is crafting a hardware emulator that's expected to be ready in the first quarter of next year.☐

PRICE AND AVAILABILTY

Full-speed samples of the MB86930 Sparclite processor and the MB86940 support chips will be available in the early second quarter of 1991. Prices for the processor will start at less than $50 in lots of over 1000 units when housed in a 160-lead, plastic quad-sided flat package. Production is expected in the third quarter.

Fujitsu Microelectronics Inc., Advanced Products Div., 50 Rio Robles, Bldg. 3, M/S 356, San Jose, CA 95134-1806; Peter von Clemm, (408) 922-9722. CIRCLE 514

HOW VALUABLE?	CIRCLE
HIGHLY	535
MODERATELY	536
SLIGHTLY	537



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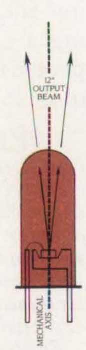

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CIRCLE 164

Wescon®/90

CAE, MEMORIES HEADLINE AT WESCON

Historically, Wescon's broad-based agenda includes something of interest for everyone in electronic engineering. This year's show, which runs from November 13 to 15 in Anaheim, Calif., will be no exception: A 36-track technical session will run the gamut from component technology to system-integration issues. But in 1990, Wescon finds itself a growing venue for manufacturers of CAE tools, whose offerings are keys to keeping designers competitive and productive in the months and years to come.

The show's second day of conferences is being billed as Technology Day, which will be devoted to exploring global technology trends and advances in microtechnology. Among the highlights of the day's technical program is a full slate of CAE sessions *(see "CAE day at Wescon," p. 72)*. In those sessions, attendees will receive up-to-the-minute information on some of today's critical design issues. They'll also learn how they can best utilize available electronic-design-automation resources. Other key session tracks will emphasize memory-subsystem design, high-density packaging and interconnects, issues confronting system design with ASICs, and MIL-STD communications.

As microprocessor speeds outstrip memory speeds, such advanced-memory architectures as caching must be employed to keep wait states from slowing the system throughput. Trends in cache architectures will be the subject of a paper by Paul Reeber of Texas Instruments, Dallas. Dynamic-RAM (DRAM) technology has evolved to the point where caches can significantly improve performance at 20 or 25 MHz. As DRAMs become faster, the logical cost-performance point for adding a cache will continue to increase. In the 1993-to-1994 time frame, Reeber asserts, that point will move to 33 MHz.

A trend has already begun toward moving much of the cache onto the micro-

DAVID MALINIAK

processor itself. Intel Corp.'s i486 and Motorola's 68040 processors each contain 8 kbytes of cache. When the speed of these machines rises to 33 MHz and beyond, a large secondary cache will be needed.

CAN'T CACHE UP

As semiconductor minimum feature sizes continue to decrease, microprocessors will integrate even more cache on the chip. The next-generation Intel machine, the 80586, is expected to have from 32 to 64 kbytes of on-chip cache. But with the advent of multitasking, multiprocessing, and multimedia presentations, the size of programs and the number of frequently used instructions and data will increase dramatically. Secondary caches of 512 kbytes to 2 Mbytes will be needed to keep systems running without wait states. According to Reeber, this means that the trend toward integrating cache memory into microprocessors will not keep pace with the requirement for caching.

When system-clock cycles approach 50 MHz, or 20 ns, cache memory requires a 10-to-12-ns cycle time. Such high-speed static RAMs (SRAMs) are rare in CMOS. In the ECL arena, a 100-MHz system, which corresponds to a 10-ns clock cycle, calls for fast ECL SRAMs. But in an ECL machine, a 1-ft. board trace would represent 20% of the clock cycle. That precludes using asynchronous SRAMs, because so much of the clock cycle is taken up by timing skew.

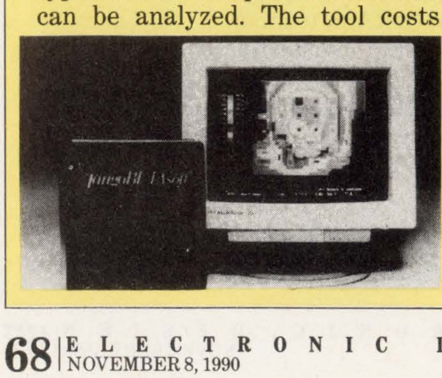
This has spurred on the development of synchronous self-timed RAMs (STRAMs), which internally generate write-pulse signals and I/O latches. David F. Naren, of Synergy Semiconductor Corp., Santa Clara, Calif., describes a new generation of STRAMs that simplify design and optimize CPU performance.

The STRAM operates in a synchronous mode, which eliminates many of the problems associated with asynchronous static RAMs. In the STRAM, all inputs and outputs are latched or registered, and both read and write operations are initiated with a common clock. A major advantage of the devices is their on-chip write-timing generator, which delivers a truly balanced read and write cycle. One problem with STRAMs, though, is the hold time of output data after clock initiation. The data must be held long enough to satisfy the input hold time, clock, and data skews of the receiving circuits, which takes about 1 to 2 ns. Most STRAMs guarantee a hold time of 0.3 ns at best.

Advanced STRAMS (ASTRAMs) are now addressing this problem. They feature a separate output-register clock, which is generated on the

Wescon®/90 PRODUCTS

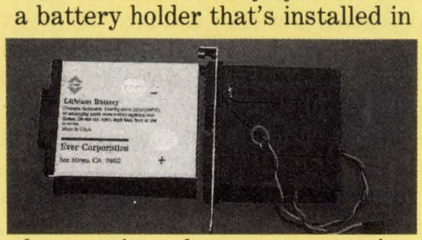
Reliability-analysis tool spots thermal problems during board design. Now designers can analyze the thermal and reliability parameters of boards during their design phase with the Tango-BETAsoft tool. Analysis of boards with the tool shows that the highest IC-junction temperatures may not correspond to the highest failure rates. The tool reveals both temperature and failure rates for individual components as well as the MTBF for the entire board. Up to 400 component types and 600 components on a side can be analyzed. The tool costs



$3195 for double-sided boards and $2195 for single-sided boards. Delivery is from stock.

Accel Technologies Inc.
San Diego, Calif.; (619) 554-1000.
Booth 423 **Circle 300**

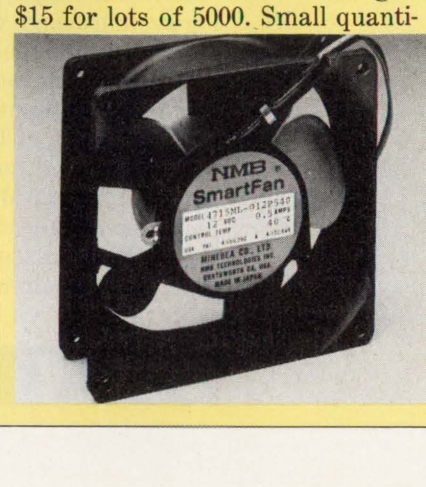
Lithium time-clock battery for computers makes replacement easy. Now the clock battery for computers can be replaced without powering the machine down or even removing its cover. The Battery-Guard lithium-battery system uses a battery holder that's installed in



the opening above an expansion slot at the back panel. Once installed, battery replacement is done from outside the case. The battery, which is less than 0.2-in. thick, incorporates lithium manganese dioxide chemistry for high energy output. Call for pricing and delivery.

Ever Corp.
San Mateo, Calif.; (415) 572-1077.
Booth 2544 **Circle 301**

Smart dc cooling fan cuts noise while maintaining temperature level. Significant noise reduction is achieved while the SmartFan cooling fan maintains a consistent temperature level inside an enclosure. The fan offers a longer life than earlier models because it usually runs at a reduced speed. The fan incorporates a closed-loop temperature-regulating system that automatically controls the air flow to hold ambient temperatures constant within enclosures. Pricing is $15 for lots of 5000. Small quanti-



chip, a hidden write cycle, parity checking, and scan diagnostics. All inputs and outputs are registered with a second internal clock that clocks the output registers. This guarantees a minimum hold time of 2.5 ns—long enough to transfer data to the next stage even when the system clock is running at the memory's spec-sheet limits. Synergy Semiconductor is developing the industry's fastest ASTRAM with a 2-kbit-by-9 organization.

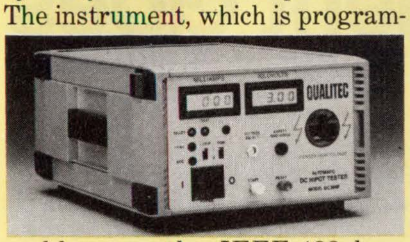
One way to address the clock skews and attendant system-timing problems in high-speed systems is to minimize wiring runs and to keep interconnections as short and close as possible. Multichip-module technology is the key to such packaging improvements. Three scientists from General Electric's Corporate Research and Development Center, Schenectady, N.Y., will report on the status of the company's High-Density Interconnect (HDI) multichip-module technology.

In the HDI process, complex chips of various types are placed virtually edge-to-edge in cavities machined into a ceramic, silicon, or aluminum-nitride substrate. A multilayer interconnection structure is built up on top of the chips, and the surrounding substrate directly forms the chip-to-chip electrical connections. A 1-mil-thick polyimide film is bonded over the top surface of the chips and the ceramic substrate with a thermal

ties are delivered from stock.

NMB Technologies Inc.
Chatsworth, Calif.; (818) 341-3355.
Booth 1596 **Circle 302**

IEEE-488-programmable hipot tester jams several tests into one cycle. Arc detection with 3-μs sensitivity, leakage-current detection in microamps and milliamps, and ground-continuity testing from 0.1 to 10 Ω are performed in one test cycle by the DC310P hipot tester. The instrument, which is program-



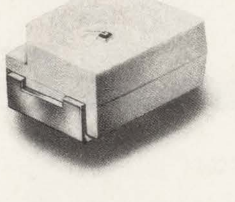
mable over the IEEE-488 bus, sports separate audible, visual, and remote failure alarms for each test. It simplifies compliance with UL, CSA, VDE, IEC, and other international standards. The tester costs $7000 and is available now.

Qualitec Technologies Inc.
Fremont, Calif.; (415) 498-1046.
Booth 949 **Circle 303**

SIEMENS

Our New LED Agreement Goes Beyond The Surface.

When it comes to surface-mount (SMT) LED indicators, Hewlett-Packard and Siemens are making a world of difference. Through our extensive co-development efforts, we can offer you standard, multi-sourced SMT LEDs.



By combining our expertise in the optoelectronics field, we've done more than respond to your need for a global standard. Our SMT LEDs are designed to give you performance comparable to through-hole LEDs.

To brighten your design outlook even further, our LED indicators will provide SMT manufacturing process compatibility for ease of placement and soldering. Plus, we'll offer a full range of LED colors, and light intensity that outshines all others.

Best of all, these lamps are from HP and Siemens. So you're assured of our commitment to excellence in service, support and reliability.

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Optoelectronics Division
19000 Homestead Road
Cupertino, CA 95014-0799

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CIRCLE 128

plastic adhesive. The film bridges the gaps between the chips and the ceramic frame. A laser "drills" via holes directly to the chip pads, and the surface is metallized and patterned to form the first-layer interconnects and via metallization.

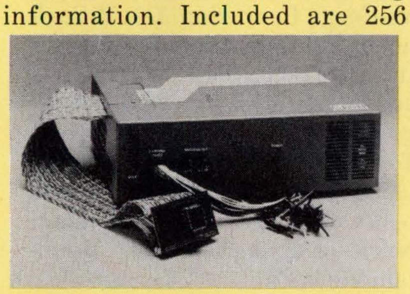
The second-layer dielectric and all subsequent dielectric layers are formed by spinning or spraying on a different polyimide. Via drilling and metal-patterning steps are then repeated. Multichip modules have been built with two or four interconnect layers. Typical feature sizes are 1-mil vias, 1-mil lines, and 2-mil spaces.

Rework or repair of the modules can be performed either with in-line processing steps or after module testing is performed. Lasers can be used to correct opens or shorts for random defects found during a layer inspection, or to completely remove and reapply a metal layer if widespread defects occur. The HDI overlay can be removed by peeling the polyimide film off after the substrate was heated to soften the adhesive. A defective chip can then be removed and replaced in the substrate.

An advantage of the HDI approach is that complex bare chips can be fully tested and burned-in without risking damage to the chips. The pro-

Wescon®/90 PRODUCTS

Real-time emulation arrives for Motorola's 68332 microprocessor. Support for the Motorola 68332 microprocessor is now featured in the HMI-200 series emulators. The units offer four complex break and trigger points and two 4-kbit-by-104-bit trace buffers with 16 external trace bits and 32 bits of time-tag information. Included are 256



kbytes of emulation memory with an option for 1, 2, or 4 Mbytes. The emulators are integrated with SourceGate, a windowed high-level-language debugger. Pricing is $16,000 for the emulators and $1500 for the IBM PC version of SourceGate. Call for delivery information.

Huntsville Microsystems Inc.
Huntsville, Ala.; (205) 881-6005.
Booth 317 **Circle 304**

cess includes a chip coating that protects the chips from test, probe, handling, or processing damages. Temporary wire-bond pads can be formed on the polymer overcoat, which facilitates full functional testing and burn-in. The chips can then be easily restored to bare condition for installation in modules.

As with multichip modules, 3D integrated packaging is an emerging technology that can help packaging engineers meet the density demands of new computer systems. Manufacturing issues for 3D packaging are discussed in a paper by Stuart Shanken and Ronald Indin of Irvine Sensors Corp., Costa Mesa, Calif.

The company's approach to 3D packaging involves stacking as many as 128 memory ICs on their edge with multiple chip-to-chip interconnects—up to 16,000 per side. Before stacking, the ICs are shaved to thicknesses as small as 2 mils.

In the manufacturing process, ICs in wafer form are given a second metal layer to fan their input and output leads to the edge of the die. Therefore, they can be accessed after the die is stacked. The wafers are burned-in, shaved to the desired thickness, and diced for stacking into module form. The resulting cube's face is lapped to expose the leads, and the IC edges are passivated so that subsequent metallizations aren't shorted to the silicon. Metals are deposited to provide input and output signal lines onto which solder bumps are placed. The module is then flip-chip-bonded to a carrier substrate.

According to Shanken and Indin, the reliability of the manufacturing process depends on testing and burn-in procedures as well as on module reworkability. The die are tested at the wafer level to assure that only working die go into the module. Functional testing is performed again at the module level. Even so, redundant chips are included in the stack. Burn-in is a die-stressing procedure that's done before final testing. If it was performed before wafer-level testing, then only working, robust die would go into the modules. But wafer-level burn-in is expensive and time-consuming. The trade-off is the need to include redundant chips in the stack.

Thermal modeling and analysis showed that each IC in the module can dissipate more than 0.6 W without the junction temperature exceeding 90°C or military standards. This indicates that the junction temperature inside the working module

CAE DAY AT WESCON

Electronic-design automation (EDA) is working its way into every facet of the electronic engineer's job. Without it, few of today's highly complex systems could exist. That's why this year's Wescon will feature an all-day track of technical sessions called "CAE Day." In four session tracks devoted to the fast-evolving world of EDA, attendees can learn how to maximize their productivity using EDA tools. They'll also discover how VHDL affects various segments of the design cycle. A panel discussion will tackle the question of when PCs end and workstations begin as EDA platforms. And, scientists from the Jet Propulsion Laboratory, Pasadena, Calif., will describe three software-development environments they've created.

The sessions are sponsored jointly by Electronic Design Automation Companies (EDAC), an EDA-industry group, and ELECTRONIC DESIGN magazine. Two of the four sessions were organized by Lisa Maliniak, ELECTRONIC DESIGN's CAE technology editor.

In the EDAC session, which will forecast EDA directions in the 1990s, EDA-industry leaders will speak and then be led in a panel discussion by Jim Hammock of Mentor Graphics, San Jose, Calif. The shift from device-level design to system-level design is the theme of a talk by Wayne Gutschick of Minc Inc., Colorado Springs, Colo. Lowering testing costs through EDA usage will be covered by Leif Rosqvist of Test Systems Strategies Inc., Beaverton, Ore. EDA also reduces time-to-market, a topic that Alain Hannover of Viewlogic Systems Inc., Marlboro, Mass., will speak on. Other panel members include Prabhu Goel of Cadence Design Systems Inc., Lowell, Mass., and Bob Fulks of Valid Logic Systems, San Jose.

With VHDL now gaining acceptance as a standard, the interest level in the language is running higher than ever. At Wescon's VHDL session, presentations begin with top-down design and move through each design phase. A description of how VHDL statements can be combined with other inputs to design an entire system will be given by Paul Lindemann of Racal-Redac, Westford, Mass. VHDL modeling at a conceptual level is the topic of a talk by David Jakopac of Vista Technologies Inc., Schaumburg, Ill.

The session then moves to a presentation on mixed-signal, multilevel simulation with VHDL, led by Glenn House of Mentor Graphics Corp., Beaverton. David Coelho, of Vantage Analysis Systems Inc., Fremont, Calif., will discuss advanced simulation and debugging in the VHDL environment. To close out the session, a system using VHDL to link design and test will be described by Ghulam Nurie of ExperTest Inc., Mountain View, Calif.

A panel session moderated by Steve Scrupski, ELECTRONIC DESIGN's editor-in-chief, will decide when PC-based CAE is sufficient and when designers would be wise to move up to workstations. Representatives from Aldec, OrCAD Corp., P-CAD, Racal-Redac, and Sun Microsystems will discuss the pros and cons of both approaches.

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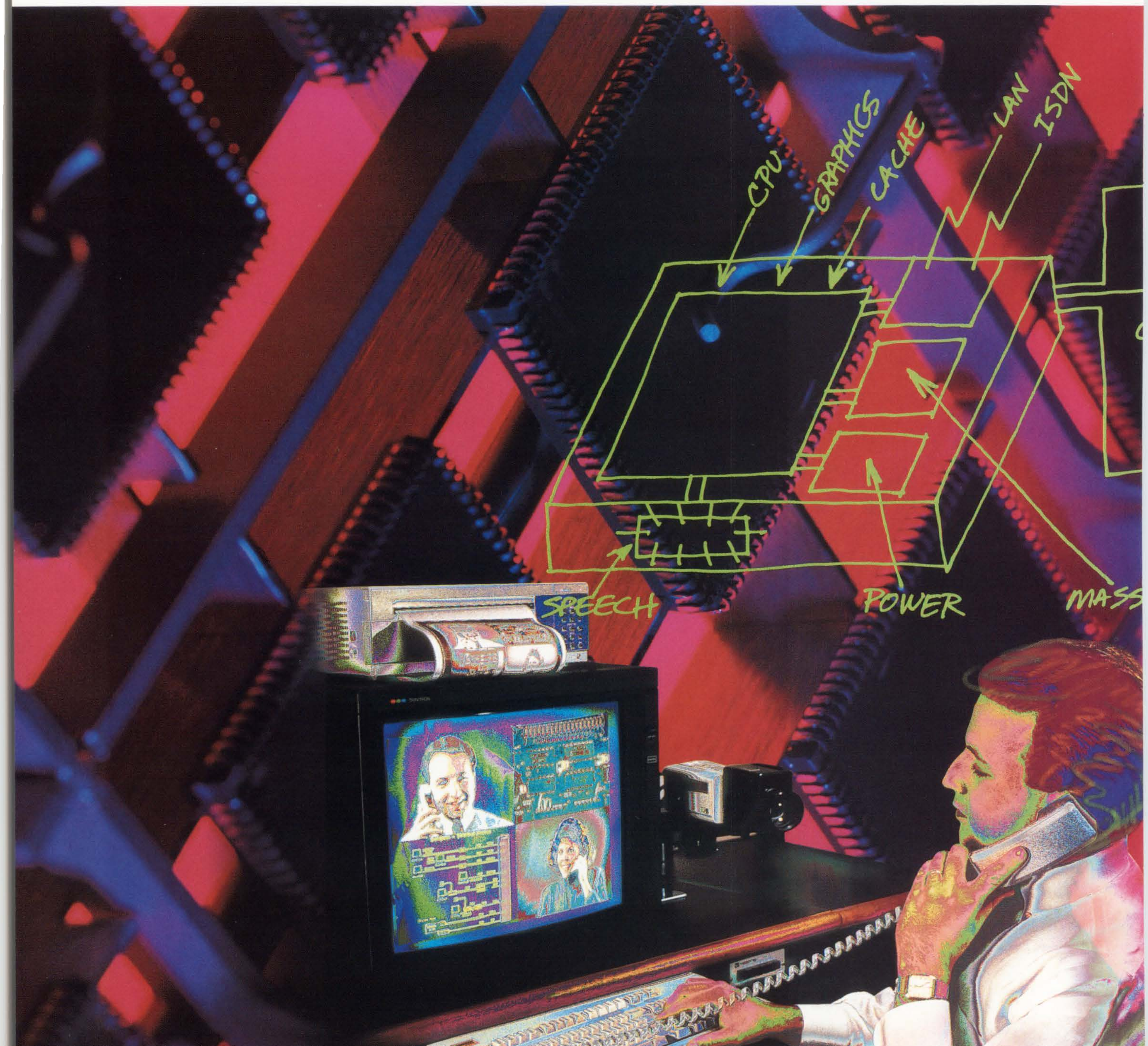
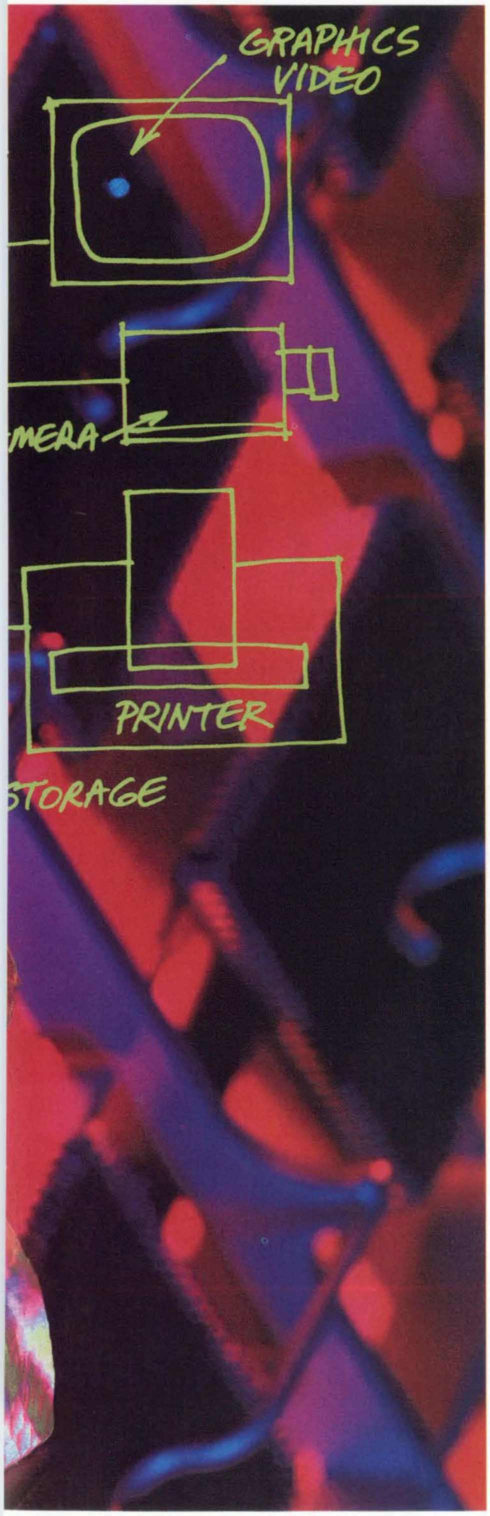


less "what-now."

"Customer*izing*."



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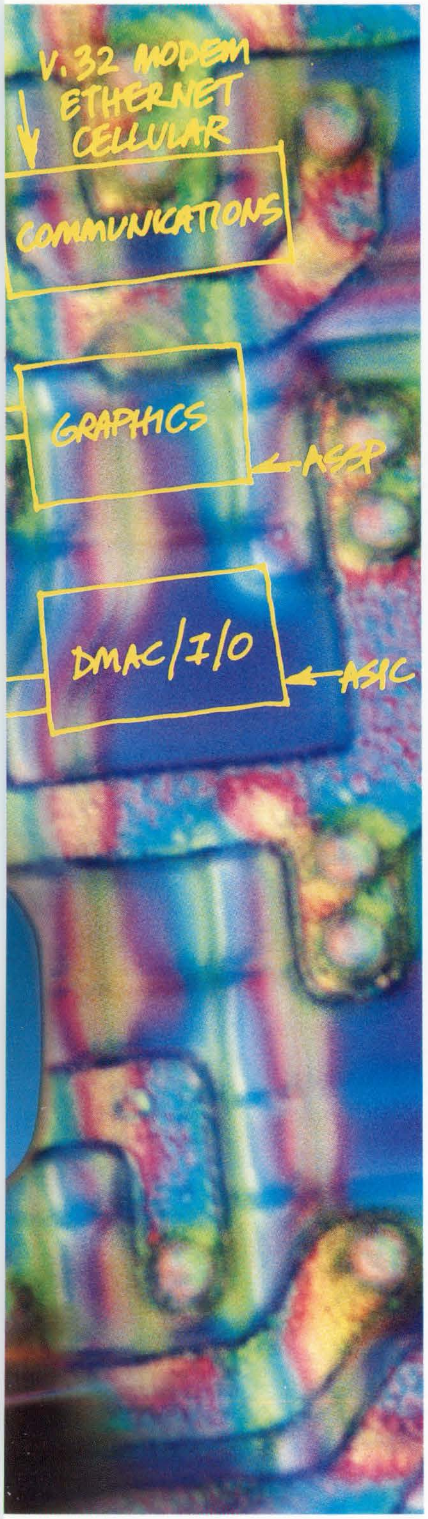

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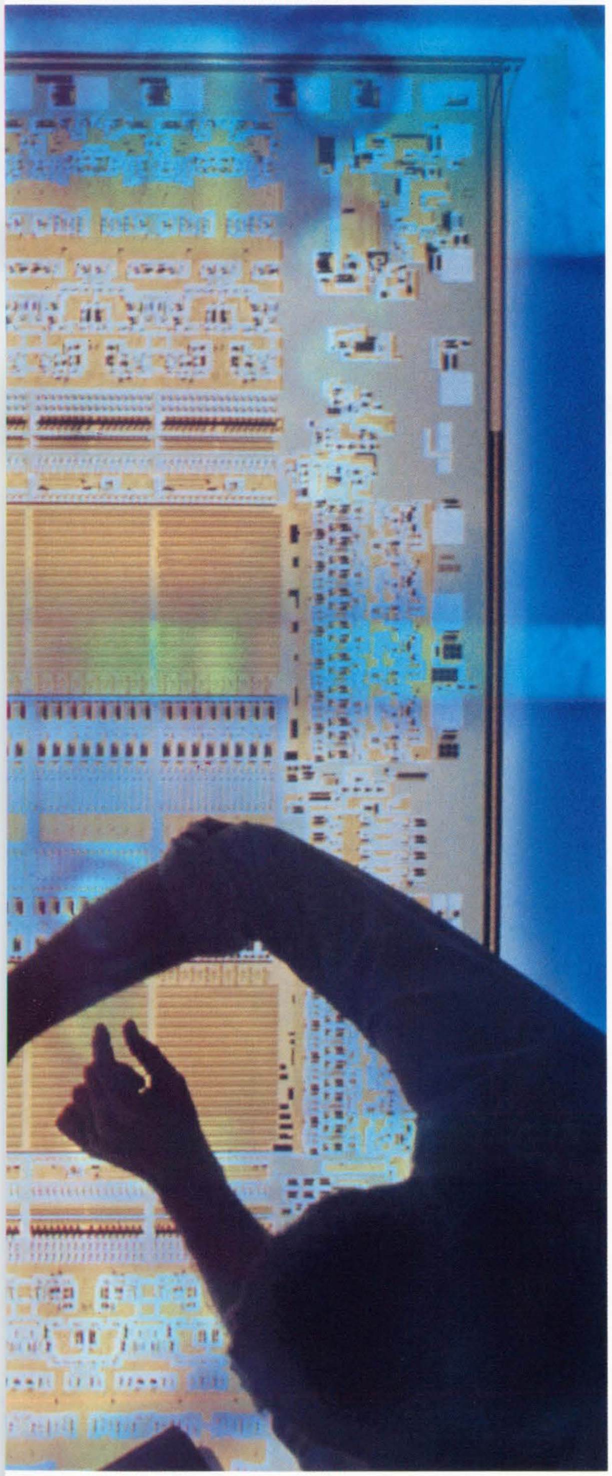

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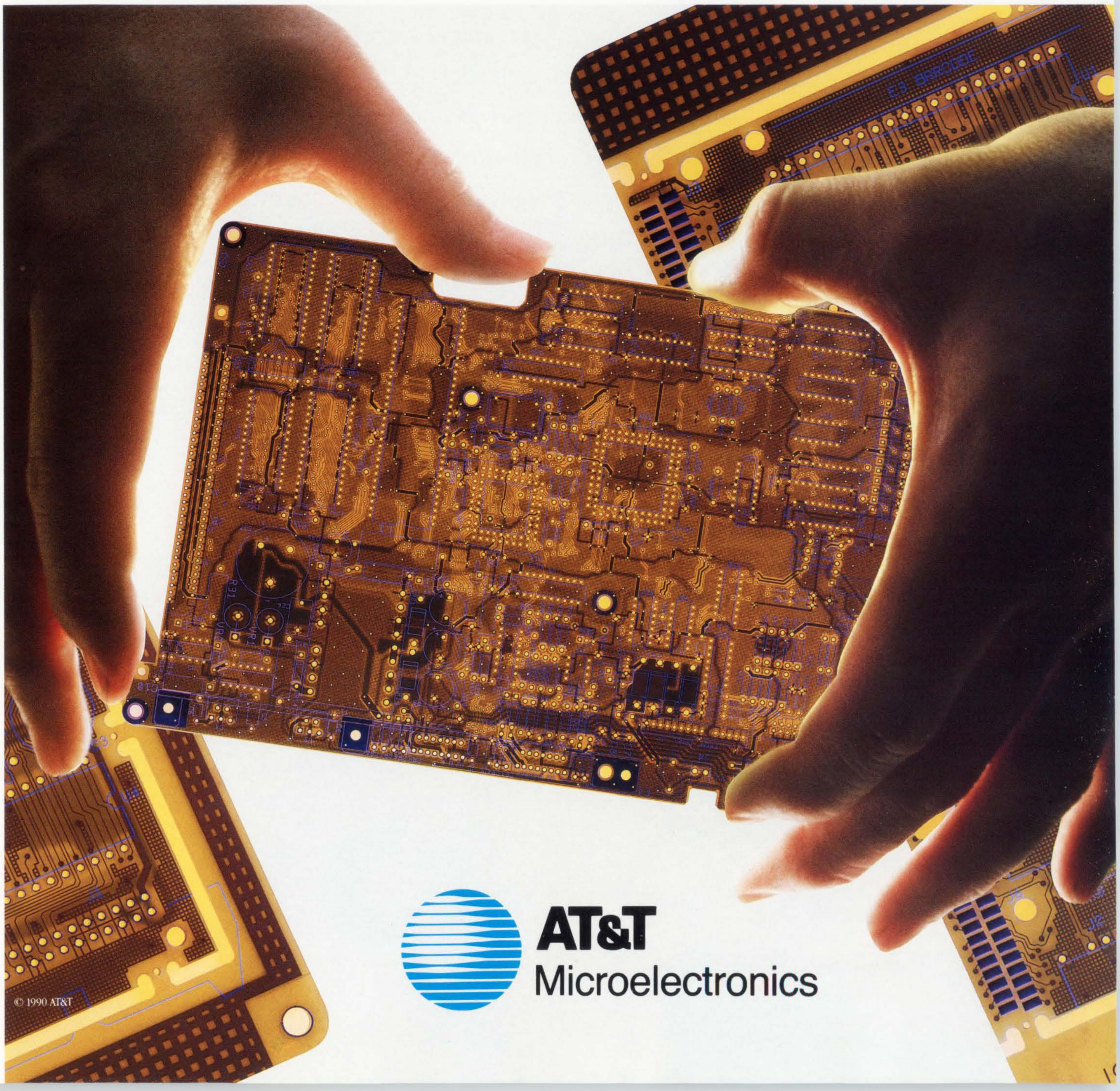


should not be high enough to adversely affect device lifetimes.

PACKAGING PROWESS

Packaging issues are among those confronting system designers working with ASICs. The advantages and limitations of quad flat packs (QFPs) and the feasibility of various types of multichip modules are the topics of a paper by Thomas Wong of Hitachi America's Semiconductor Division, Brisbane, Calif. Disadvantages cited by Wong include the higher thermal resistance of plastic QFPs compared with ceramic packages, their limited ability to handle large die, their special handling requirements, and their tendency to absorb moisture. But these are offset by the availability of additional pins without increasing the body size or decreasing the pin pitch. Unspecified pins are available to designers as extra power and ground pins to minimize noise.

Multichip modules, such as those described by General Electric, are another packaging alternative for system designers using ASICs. Wong groups the latest developments into three categories based on the substrate materials: cofired ceramics, silicon or metal substrates, and printed-circuit boards. Silicon substrates can potentially handle the highest power dissipation and wiring density, Wong asserts, but are likely to make for expensive modules.

A constraint of multichip modules,

Wescon/90 PRODUCTS

Pc-board-prototyping system makes boards quickly and at low cost. With the CAPtech prototyping system, etched, production-like pc boards can be produced in-house. Component legends, drilling, and resist application are all automatically controlled from CAD output files. The system handles a plotting size of 11 by 17 in. with a repeat accuracy of ±0.0039 in. and minimum line width of 0.010 in. In less than four hours, users can produce a typical 4-by-6-in. board with over 500 through holes. The system costs $13,850 and is delivered 30 days from receipt of order.

HiTech Equipment Corp.
San Diego, Calif.; (619) 566-1892.
Booth 1439 **Circle 305**

Three-color pc-board indicators boast high luminous intensity. Two GaP solid-state LED chips make up the series 550-3505 pc-board indicator. The three-leaded device, which

comes in a T-1-3/4 package, produces red, green, and yellow light, as well as a range of colors in the spectrum between red and green. Because it cuts down the need for multiple lamps, the indicator is well suited for use as a logic-status, circuit-board, and position indicator. Pricing is $.97 in lots of 1000. Delivery is from stock to eight weeks.

Dialight Corp.
Manasquan, N.J.; (908) 528-8932.
Booth 2328 **Circle 306**

Digital voltmeter boasts 1-nV sensitivity with 15-nV noise ceiling. The highest accuracy available for measuring extremely low voltages is claimed for the model 182 sensitive digital voltmeter. The instrument offers 1-nV sensitivity while holding noise to 15 nV pk-pk on its lowest range. A high input resistance of more than 10 GΩ on all ranges further ensures accuracy by pre-

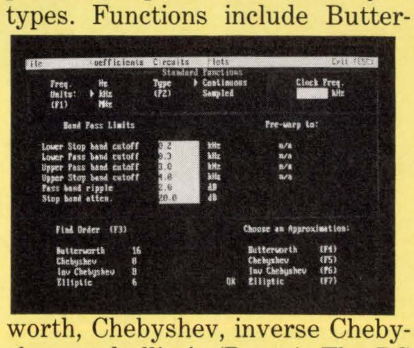
venting the meter from affecting the measurement. The meter costs $3695 and is available four weeks from receipt of order.

Keithley Instruments Inc.
Cleveland, Ohio; (800) 552-1115.
Booth 523 **Circle 307**

48-V dc-dc converters squeeze 10 W into 1.6-by-2-in. space. Operating from the 48-V input power that's common to most telecommunication systems, the TC series of dc-dc converters combine a small footprint with 500 V dc of isolation in a six-sided, shielded case. The 10-W, pc-board-mounted units offer a choice of three dc outputs: 5 V at 2000 mA, 12 V at 850 mA, or 15 V at 700 mA. Line and load regulation are 0.01% and 0.1%, respectively. Single quantities go for $105 each and availability is from stock.

Calex Mfg. Co. Inc.
Pleasant Hill, Calif.; (800) 542-3355.
Booth 2792 **Circle 308**

Active-filter design package supports various filter types. The Advanced Filter Designer is an interactive design aid for the PC and Macintosh II. It gives users the ability to design and analyze active filters, including low-pass, high-pass, band-pass, and band-reject types. Functions include Butter-



worth, Chebyshev, inverse Chebyshev, and elliptic (Bauer). The PC and Macintosh versions cost $1800 and $2700, respectively. Less sophisticated standard versions go for $600 and $900, respectively. Delivery is from stock.

MicroSim Corp.
Irvine, Calif.; (800) 245-3022.
Booth 358 **Circle 309**

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The cost-effectiveness of the 478 RAM DAC makes it very attractive. But of course you can't use it for high-end graphics. Or at least you couldn't until the new Samsung part, rated at 120 Mhz, came on the market. It makes things quite different. An industry-standard part, it provides resolution previously available only with 451/458 RAM DACs — up to 1280 x 1024 on 60 Hz non-interlaced displays. And, like our 80 Mhz 471 and 476 RAM DACs, our 478 also gives you "snow-free" operation.

though, is the scarcity of bare die, tape-automated-bonded, or flip-chip ASICs. Wong concludes that multichip modules show promise but aren't in the mainstream yet.

In another arena, federal spending for the military is on the decline. As a result, the market for MIL-STD circuit boards is shifting toward military communication systems and high-reliability, non-military applications. In a session titled "Emerging New Roles for MIL-STD Communication Boards," five board vendors will discuss solutions to challenges presented by these new applications.

One market possibility lies in the use of adapter cards to link PCs to MIL-STD buses. In an overview paper, session organizer and chairman Milt Leonard, ELECTRONIC DESIGN's senior communications editor, describes the MIL standards that adapter boards must be based around. In other session papers, Rahim Sabadia, Sabtech Industries, Anaheim, Calif., discusses the conversion of low-cost PCs into military data-communication peripherals. Stanag, the 3910 NATO standard for a 20-MHz fiber bus, is described in a paper by Mike Glass, ILC Data Device Corp., Bohemia, N.Y.□

HOW VALUABLE?	CIRCLE
HIGHLY	553
MODERATELY	554
SLIGHTLY	555

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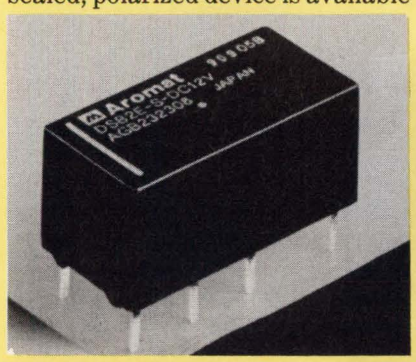
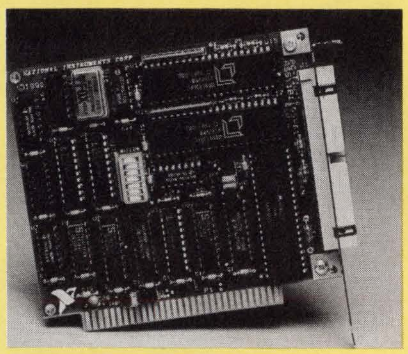
Telecommunications relay boasts 4000-V rms breakdown from contacts to coil. Thanks to a molding technique used to encapsulate the relay's coil, the DSB relay offers telecommunications designers a 4000-V rms breakdown voltage between the contacts and coil. The sealed, polarized device is available



in a 2 Form C contact arrangement and nominally switches 2 A at 30 V dc. Call for pricing and delivery.

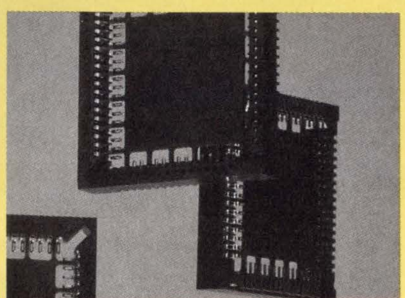
Aromat Corp.
New Providence, N.J.; (201) 464-3550.
Booth 2482 **Circle 310**

Board equips PCs for frequency and pulse measurements and waveform generation. With its 10 channels of 16-bit counter-timers, and 8-bit TTL-compatible digital input and output ports, the PC-TIO-10 data-acquisition board outfits a PC for frequency and pulse measurements. The counters can be con-



trolled by software, level gating, or edge gating. The board runs the new version 2.0 of LabWindows, which contains an extensive set of libraries to help with development of instrumentation applications. Pricing for the board is $335 in single quantities.

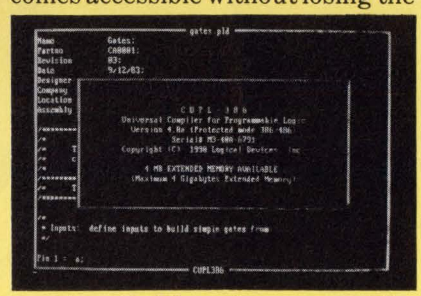
National Instruments Corp.
Austin, Texas; (512) 794-0100.
Booth 702 **Circle 311**



Surface-mounted PLCC socket has same footprint as chip carrier. Precision stampings, high-temperature plastics, and Samtec's body and contact designs distinguish its PLCC series of plastic leaded chip carrier sockets. The liquid-crystal polymer body permits high-temperature vapor-phase and infrared-reflow soldering. Sockets are available for carriers with 28, 32, 44, 52, 68, and 84 leads. Pricing starts at $1.50 for lots of 1000 with delivery in seven days.

Samtec Inc.
New Albany, Ind.; (812) 944-6733.
Booth 3542 **Circle 312**

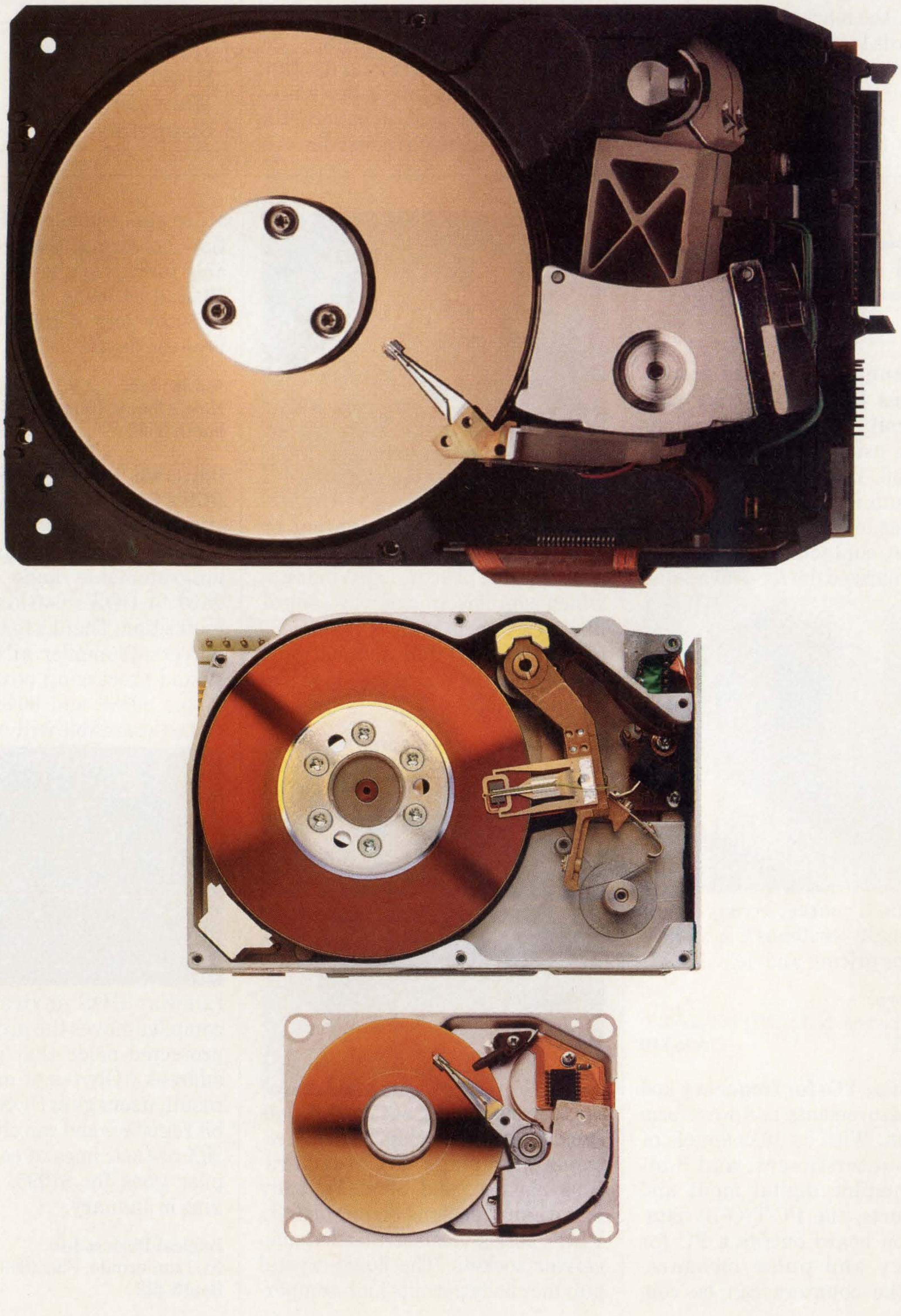
Universal logic compiler smashes DOS's 640-kbyte barrier. Very large state machines and other logic systems can now be implemented in programmable logic without regard to DOS's 640-kbyte memory restriction. Thanks to the CUPL386 universal compiler, all of the memory and processing power available in the 80386 and 80486 CPUs becomes accessible without losing the



familiar DOS environment. The compiler moves the processor into a protected mode that permits it to address 4 Gbytes of memory. As a result, users gain DOS access to 32-bit registers and can eliminate up to 20% of their lines of code. The compiler goes for $1995. Delivery begins in January.

Logical Devices Inc.
Ft. Lauderdale, Fla.; (800) 331-7766.
Booth 422 **Circle 313**

At Analog Devices, it's our goal



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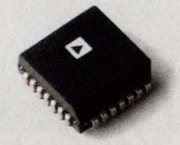

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ANALOG DEVICES

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CIRCLE 168

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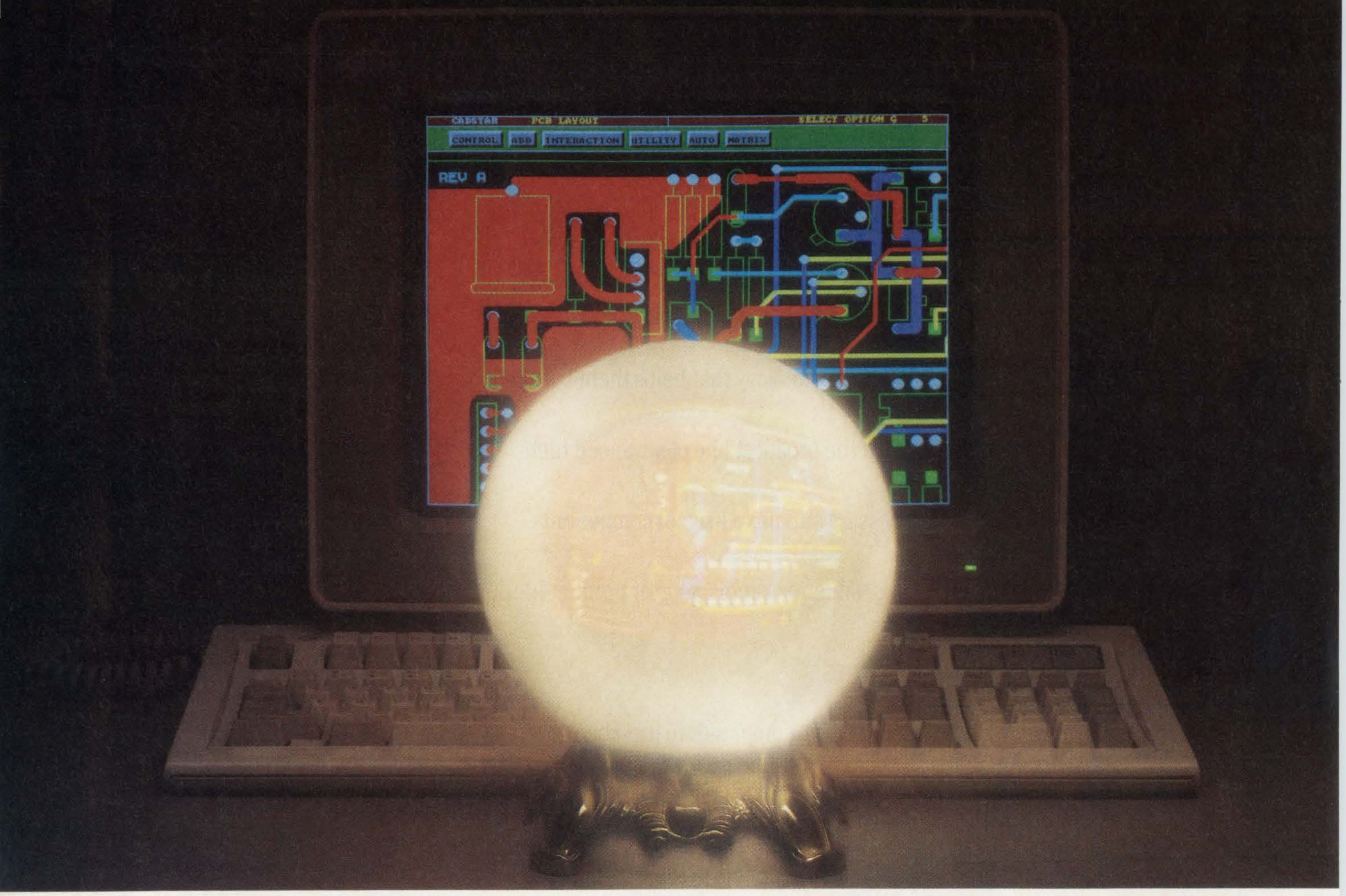

IT ALMOST READS YOUR MIND.

CADSTAR's revolutionary new user interface almost reads your mind, anticipating your next move and intelligently defaulting to the most likely action. For example, if you pick a part, CADSTAR lets you move it without selecting an action from a menu. If you pick a connection, you can manually route it instantly.

CADSTAR's new Motif style graphical interface has clear, logical menus integrated across all functions. The best part is, you'll rarely need to use those menus! Imagine software so smart, it knows what you want to do next. CADSTAR is easy to learn, and it drastically reduces keystrokes, saving you hours.

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RACAL

SEE US AT WESCON, BOOTH #308

DATA CONVERTERS: GETTING TO KNOW DYNAMIC SPECS

THE ONGOING EVOLUTION IN DATA CONVERTERS REQUIRES THAT THEY BE CHARACTERIZED BEYOND STATIC ACCURACY AND THROUGHPUT.

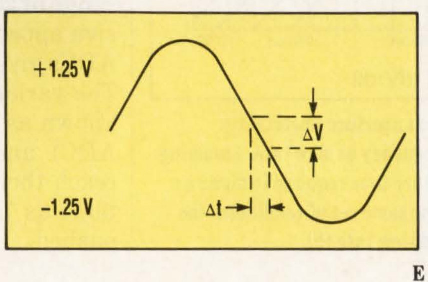
ROBERT E. LEONARD JR.
Datel Inc.,
11 Cabot Blvd.,
Mansfield, MA 02048;
(508) 339-3000.

A kaleidoscope of architectures is available for today's data converters. But ensuring that a data converter can obtain a desired transfer rate and accuracy at a particular input frequency is more important than any architectural nuances. Now that converter data sheets carry frequency-domain specifications, designers are finally gaining insight into how they'll perform on the job.

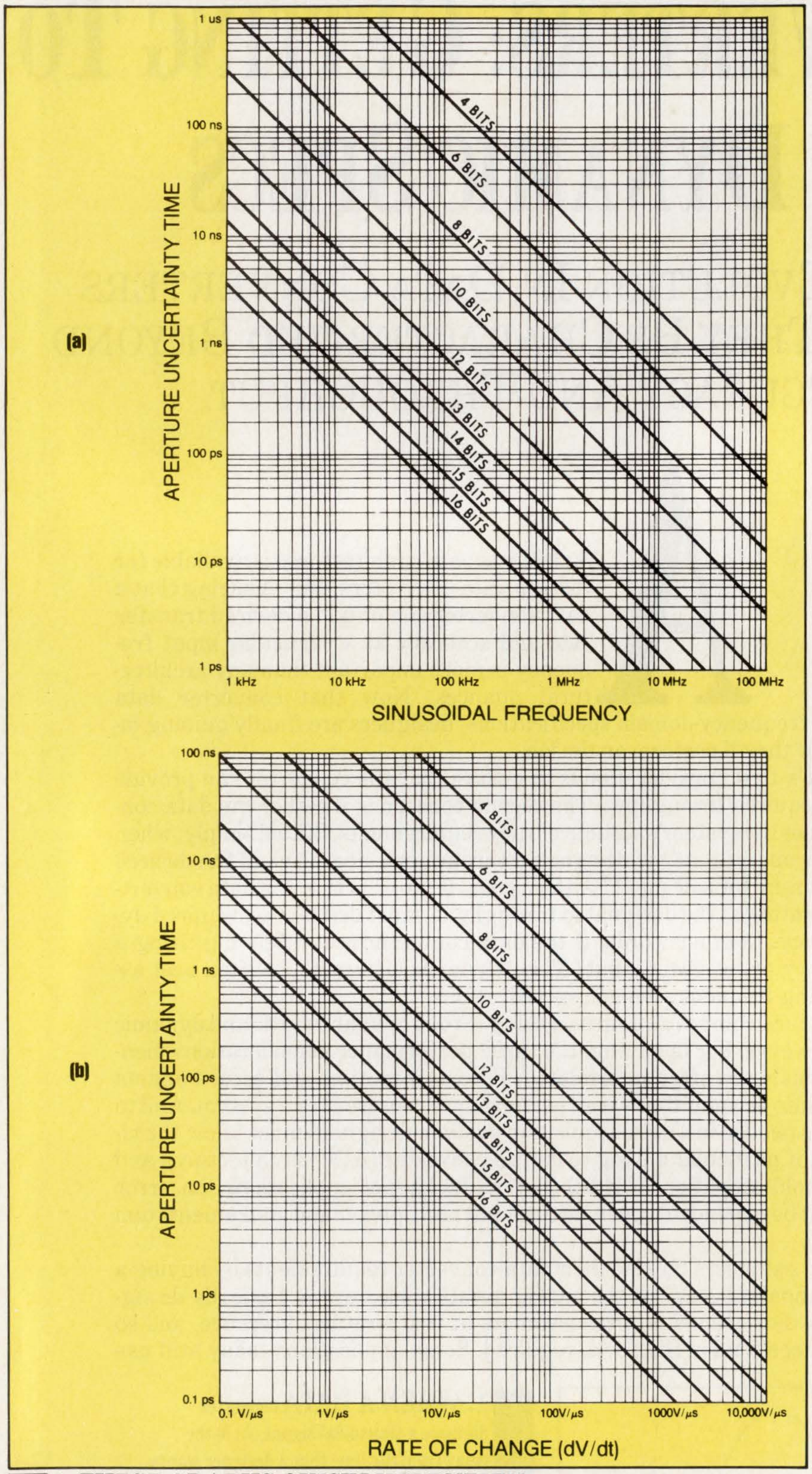
A designer's first consideration is to ensure that the converter can provide data at the required throughput. The second concern is whether the data converter can meet the system's static accuracy requirements. Stated simply, when the converter operates at the designated throughput, does it yield the desired transfer accuracy for a dc input? A third consideration is that the data converter, when operating at the designated throughput, must deliver the required dynamic accuracy. In other words, is the data converter accurately digitizing a high-frequency or transient input? This "dynamic accuracy" is often best assessed by using frequency-domain specifications.

Designers face many pitfalls in assessing throughput and static and dynamic accuracy, however. For one thing, the three performance considerations mentioned previously are often interrelated. For another, time and error budgets need to take into account the overall performance required for a system. And to assess what's needed in a data-acquisition system, designers must know the idiosyncrasies of particular analog-to-digital converter (ADC) architectures and sample-and-hold amplifiers (SHAs). For multichannel applications, an error analysis must be expanded to include the input multiplexer and instrumentation amplifier.

In the past, engineers tackled their data-converter requirements by buying a separate, standalone ADC. If the analog inputs were beyond basically dc signals, such as those found in measurements of temperature, pressure, and so forth, then a companion SHA was required. Some applications today still use



1. WHEN A DATA converter digitizes a sinusoidal signal, Δt is the delay from the time that a designer wants to read the voltage to when the voltage was actually sampled. This period is called the aperture delay time. ΔV is the difference between the exact voltage that's digitized from the desired voltage.



2. THESE GRAPHS QUICKLY IDENTIFY what aperture-uncertainty specification is required to keep up with a particular input frequency or slew rate. Assuming a 10-V pk-pk full-scale signal, the first graph depicts the aperture time required to digitize a particular input frequency to an accuracy of 1 LSB (a). For the same set of conditions, the other graph shows the relationship between aperture time and slew rate (b).

only an ADC because of slow input signals. Others have a separate ADC and SHA. Sampling ADCs, which include an internal ADC and SHA in one package, are growing increasingly popular.

But designers must scrutinize other factors before deciding that a sampling ADC can deliver the needed accuracy under certain dynamic conditions. Clean input digitization when the ADC operates up to the Nyquist rate (signal frequency at one-half the sampling rate) isn't a given. The flash ADC category is another example of an ADC used without a preceding SHA. The generic family of flash ADCs includes devices from 4 to 10 bits of accuracy with throughputs from 10 MHz to 500 MHz.

Some flash ADC architectures may or may not need a SHA in digitizing high-frequency signal inputs. Available flash ADC architectures include the "true flash" with a straight comparator design, an interpolation/folding design, and a two-pass design. Two factors determine if a SHA is needed. One is the aperture jitter specification, which often depends on architecture. The other deciding factor is the ability to drive the flash ADC's dynamic input impedance at the desired frequency.

As previously noted, there's a proliferation of ADC architectures today. For example, the integrating ADC with various slope architectures is still focused on slow, high-resolution applications—it doesn't require an external SHA.

The successive-approximation ADC and companion SHA have long been workhorses for medium speed and resolution. Now they share some of these applications with the delta-sigma ADC.

The delta-sigma architecture has an inherent SHA function built in. To obtain increased speeds beyond the range of 20 kHz to 1 MHz, the successive approximation and delta-sigma ADCs give way to the two-pass ADC. The various types of two-pass (also known as a two-step or subranging ADC) and companion SHAs also reach their speed/resolution limitations as next-generation limits are pushed.

Food For Thought About Field Programmable Gate Arrays.

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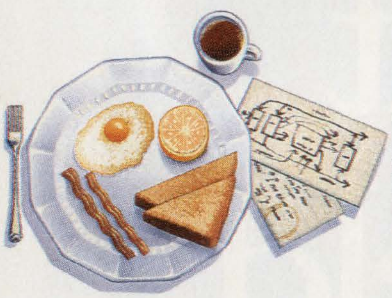

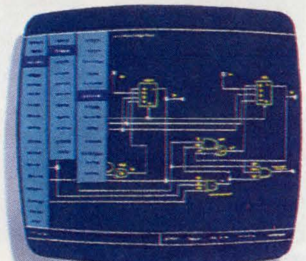

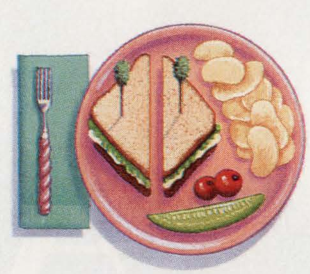

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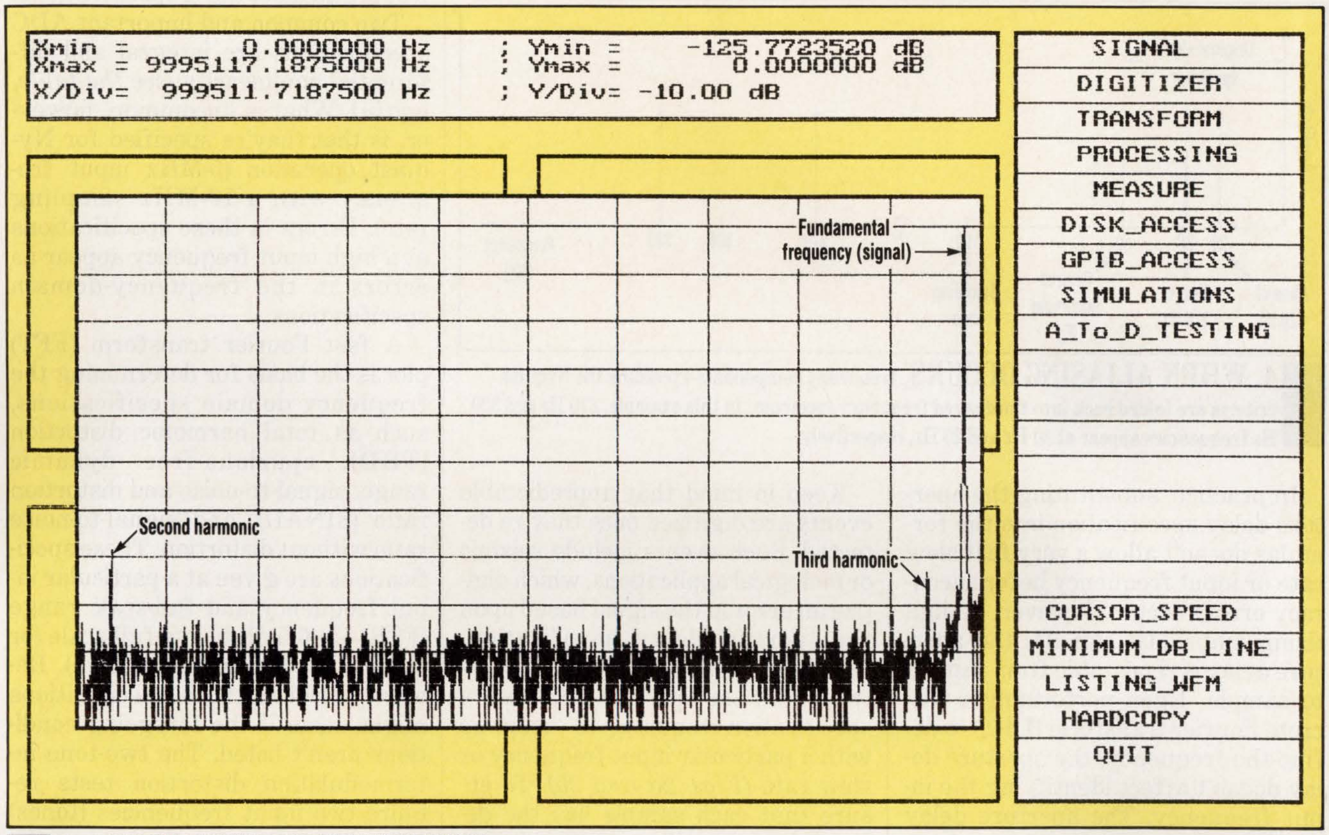


3. A FAST FOURIER TRANSFORM plot is a handy method for viewing unknown input frequencies or distortions introduced by a data converter. This plot is based on data from an ADS-130 ADC.

The successive-approximation ADC and two-pass ADCs' speed (kilohertz to megahertz range) suit most applications beyond dc measurements. They use sample-and-hold amplifiers that can be combined with the ADC either externally or internally. An analysis of the constraints on the data-acquisition system's dynamic performance should start with the sample-and-hold amplifier to be used.

Sinusoidal Signals

To ensure appropriate accuracy at a particular frequency, sinusoidal signals must be explored. Assume that the 2.5-V pk-pk sinusoidal signal will be digitized by a data converter to 12-bit accuracy *(Fig. 1)*. When designers want the ADC or sample-and-hold amplifier in front of the converter to take a sample, timing delays occur. As a result, the exact point that was originally intended isn't acquired.

Δt represents the delay from the time that designers want to read the voltage to when the voltage was actually sampled. This aperture-delay time appears on the data sheets for SHAs and for flash ADCs, where appropriate. The amplifier's aperture-delay time is affected by the logic threshold voltage on the pin that controls going into the sample or hold mode.

For TTL or other logic families, there's an internal delay in the digital logic going from a logic 1 (assume a sample-mode) to a logic 0 (assume a hold-mode) and the time the internal switch actually opens. The sample-and-hold amplifier also experiences an analog delay as the input goes through the input buffer to be stored on the hold capacitor. The difference between the digital and analog delays is known as the "effective" aperture delay time.

The aperture-delay time prevents designers from digitizing the sinusoid at exactly the right moment. The exact voltage that's digitized differs from the desired voltage by ΔV *(Fig. 1, again)*. For a 12-bit converter with a $\pm$1.25-V input (1.25-V full scale, 2.5-V full-scale range), 1 LSB equates to:

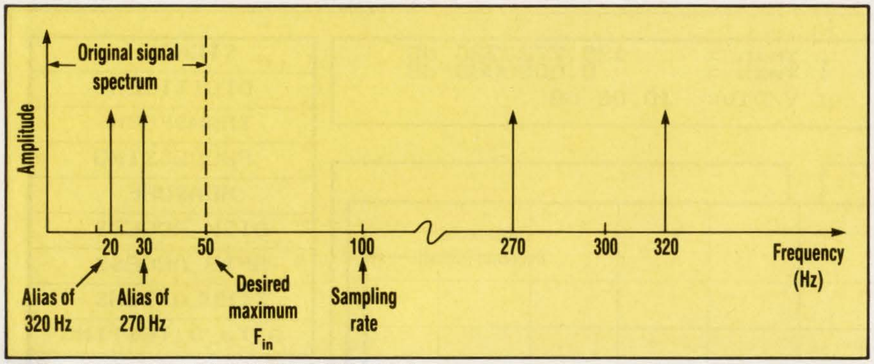
$2.5\ V/2^{12} = 2.5\ V/4096 = 1\ LSB = 610\ \mu V$

Maintaining 12-bit, $\pm$1-LSB accuracy requires that during the aperture-delay time (Δt), the voltage change (ΔV) is held to $\pm$1 LSB maximum. The change in voltage over the change in time ($\Delta V/\Delta t$) is the maximum slew rate of the input signal allowed. Mathematically, formula 1 is derived as:

$\text{Slew rate} = \Delta V/\Delta t = 2\pi fV$

This yields the maximum input frequency of the sinusoid, which can be digitized as formula 2:

$f = \Delta V/(\Delta t 2\pi V)$
where f = maximum input frequency
V = full-scale voltage



4. WHEN ALIASING OCCURS, frequency components exceeding the Nyquist criteria are folded back into the desired frequency spectrum. In this example, 270 Hz and 320 Hz frequencies appear at 30 Hz and 20 Hz, respectively.

In practice, substituting the aperture-delay specification into the formulas doesn't allow a very fast slew rate or input frequency before accuracy errors occur. However, in digitizing sinusoidal signals, the aperture delay is repeatable from sample to sample. Upon performing a discrete Fourier transform (DFT) to define the frequency, the aperture delay doesn't affect identifying the input frequency. The aperture delay now just represents itself as a phase shift.

However, designers interested in capturing single-shot events would be limited in accuracy by the "effective" aperture delay. In contrast, the maximum sinusoidal frequency that can be acquired isn't limited by the repeatable aperture delay times. Now, the input-frequency limiting factor is the uncertainty of the delay from sample to sample.

This uncertainty can be derived from the effect that various noise sources create when changing the exact threshold voltage of the sample-and-hold amplifier's digital control command. The aperture uncertainty (jitter) now becomes the limiting factor (Δt) in determining the maximum input frequency. A digital-signal-processing application on repetitive sinusoidal signals is one area whose ultimate performance and upper-frequency range depends upon the aperture-uncertainty specification. For example, the upper-frequency range of a spectrum analyzer becomes limited by the aperture-uncertainty specification.

Keep in mind that unpredictable events are digitized once they're detected. Such events include seismic or biological applications, which digitize an error in the signal based upon the aperture-delay specification. Graphing formulas 1 and 2 can quickly identify the aperture-uncertainty specification required to keep up with a particular input frequency or slew rate *(Figs. 2a and 2b)*. To ensure that each sample has the desired accuracy, the aperture uncertainty should be a peak value vs. root mean square (rms).

Frequency Domain

It's essential to determine whether the SHA or the flash ADC can meet the input frequency and accuracy requirements based on aperture-uncertainty or slew-rate considerations. Although they're prerequisites, these specifications are insufficient in judging the performance to be obtained. Designers must also consider other dynamic specifications.

For example, because the ADS-130, 12-bit, 10-MHz sampling ADC combines an ADC and SHA in one package, it allows dynamic specifications that are often reserved only for system instruments to be published *(see the table)*. As a result, sampling ADCs are easing the manufacturer's ability to specify data converters in the frequency domain. If a standalone ADC had these specifications and a companion sample-and-hold amplifier were still required, there's no guarantee that an overall system would still meet these specifications.

Two common and important ADC specifications are integral and differential nonlinearity *(see the table, again)*. What is uncommon, however, is that they're specified for Nyquist operation (5-MHz input frequency with a 10-MHz sampling rate). Errors in these specifications at a high input frequency appear as errors in the frequency-domain specifications.

A fast Fourier transform (FFT) plot is the basis for determining the frequency domain specifications, such as total harmonic distortion (THD), spurious-free dynamic range, signal-to-noise and distortion ratio (SINAD), and signal-to-noise ratio without distortion. These specifications are given at a particular input frequency and full-scale range (FSR) of –0.5 dB below full scale (or about 95% of the input range). Beware of what these specifications might mean if the foregoing conditions aren't listed. The two-tone intermodulation distortion tests require two input frequencies (tones) to be generated for testing vs. the single fundamental for the other tests.

An FFT plot is an excellent way to identify unknown input frequencies *(Fig. 3)*. Actually, a discrete Fourier transform (DFT) is performed on the discontinuous data from the data converters. Various windowing functions then ensure that the DFT's fast Fourier transform algorithm is for data representing complete cycles when noncoherent sampling is used. Examples of windowing functions include the Blackman-Harris or Hamming windows, whose functions are to prevent the signal energy from "leaking" into other frequencies.

If a continuous bandwidth-limited signal contains no frequency components higher than the analog input frequency (F_{in}), then the original signal can be recovered without distortion if it's sampled (F_s) at more than twice the analog input frequency (Nyquist rate). Because of imperfect filters, which go to zero asymptotically and introduce phase distortion, the sampling rate might be a minimum of four times the analog input in practice.

If the sampling frequency (F_s) isn't high enough or if harmonics are generated by the input or data converter, part of the spectrum folds over into the original signal spectrum *(Fig. 4)*. This undesirable effect, called frequency folding, creates an alias frequency in the original signal spectrum as given in the following example:

The input frequency is analyzed as $F_{in} = K(F_s/2) + \delta F$, where:

(a) K is an odd or even integer that's a multiple of half the sampling period.

(b) $0 \leq \delta F \leq Fs/2$

Case 1. Alias frequency = $(F_s/2) - \delta F$ if K is odd.

Example: If F_{in} = 270 Hz and Fs = 100 Hz, then 270 Hz = 5 (100/2) + 20, where K = 5

K is odd so that 270 Hz has an alias appearing at (100/2) – 20 = 30 Hz in the original signal spectrum

Case 2. Alias frequency = δF if K is even

Example: if F_{in} = 320 Hz and F_s = 100 Hz, then 320 Hz = 6(100/2) + 20 where K = 6

K is even so that 320 Hz has an alias appearing at 20 Hz in the original spectrum.

Designers should also be careful when it comes to signal-to-noise ratios (SNRs). When inspecting the FFT plot, the classic definition defines the signal as the fundamental frequency. Noise is defined as all of the other unwanted errors (harmonics, spurious frequencies, and the noise floor) in the FFT plot. In practice, the term SNR may not always include the harmonics.

In specifying ADCs, manufacturers now use the term SINAD, for siginal-to-noise and distortion ratio. Or they note if the signal-to-noise ratio includes or excludes distortion. After mathematical derivation through Gaussian quantization errors, the ideal SNR and distortion specification (rms signal to rms noise) is expressed in formula 3 as:

SNR = 6.02n dB + 1.76 dB, where n is the number of bits

For harmonics, the specification THD includes all harmonics. The in-band harmonic specification is meant to include the worst harmonic (usually the second one). The spurious-free dynamic range resembles the in-band harmonic specification. In practice, the spurious occurrences and noise present are lower than the harmonics. Total harmonic distortion, the ratio of the sum of all the harmonics to the fundamental signal as analyzed at the ADC output can be expressed in formula 4 as:

$$THD_{rms} = \sqrt{\left[10^{\left(\frac{\text{2nd Harmonic}}{20}\right)}\right]^2 + \left[10^{\left(\frac{\text{3rd Harmonic}}{20}\right)}\right]^2 + \ldots}$$

While total harmonic distortion is a more conservative specification, the in-band harmonic and spurious-free dynamic-range specifications can be of interest for particular ap-

ADS-130 DYNAMIC SPECIFICATIONS

	Minimum	Type	Maximum	Units
Integral nonlinearity				
@ f_{in} = 5 MHz, +25°C			±1	LSB
0 to +70°C			±1	LSB
–55°C to +125°C			±2	LSB
Differential nonlinearity				
@ f_{in} = 5 MHz, +25°C			±1	LSB
0 to +70°C			±1	LSB
–55°C to +125°C			±2	LSB
Total harmonic distortion (–0.5 dB)				
Dc to 500 kHz	–68	–70		dB below FS
500 kHz to 2.5 MHz	–65	–67		dB below FS
2.5 MHz to 5 MHz	–65	–67		dB below FS
In-band harmonics				
Dc to 500 kHz	–69	–70		dB below FS
500 kHz to 2.5 MHz	–66	–67		dB below FS
2.5 MHz to 5 MHz	–66	–67		dB below FS
Spurious-free dynamic range				
Dc to 500 kHz	–69	–70		dB below FS
500 kHz to 2.5 MHz	–66	–67		dB below FS
2.5 MHz to 5 MHz	–66	–67		dB below FS
Signal-to-noise ratio (without distortion, –0.5 dB)				
Dc to 500 kHz	–67	–70		dB below FS
500 kHz to 2.5 MHz	–65	–69		dB below FS
2.5 MHz to 5 MHz	–65	–69		dB below FS
Signal-to-noise ratio and distortion, –0.5 dB				
Dc to 500 kHz	–65	–66		dB below FS
500 kHz to 2.5 MHz	–63	–65		dB below FS
2.5 MHz to 5 MHz	–63	–65		dB below FS
Effective bits, –0.5 dB				
Dc to 500 kHz	10.6	11.0		bits
500 kHz to 2.5 MHz	10.2	10.5		bits
2.5 MHz to 5 MHz	10.0	10.2		bits
Two-tone intermodulation Distortion (f_{in} = 2.2 MHz, 2.3 MHz, F_s = 8 MHz, –0.5 dB)	–72	–75		dB below FS
Input bandwidth				
Small signal (–20 dB input)	50	65		MHz
Large signal (0 dB input)	30	40		MHz
Slew rate	175	200		V/µS
Aperture delay time		5	7	ns
Aperture uncertainty		5	7	ps
Sample and hold acquisition time to 0.01% (2.5 V step)		30	50	ns
FS = full scale				

ADC SPECIFICATIONS

plications. For example, insufficient usable dynamic range that enables noise and harmonics to intrude on the measurement could interfere in distinguishing a low-level radar signal. In the effective-bits specification, a mathematical representation of an ideal sine wave is compared with the sinusoid digitized by the data converter. Numerical method algorithms help compute the accuracy, which is specified in bits.

Basically, the effective-bit specification is a combination of all the other errors. Any errors from differential and integral nonlinearity, aperture uncertainty, and missing codes show up as part of the overall rms error. In what "no missing codes" means to ADCs and "monotonicity" to DACs, effective bits will likely be the leading comparative specification for the dynamic performance of sampling ADCs.

Effective bits can be derived from the SNR (and distortion) specification in formula 5 as:

$$\text{Effective bits} = (\text{SNR} - 1.76)/6.02$$

If the signal-to-noise ratio without distortion is employed, then the THD specification can be used to derive the effective bits in formula 6 as:

$$\text{Effective bits} = 20\log\{[10^{(\text{SNR}/20)} + 10^{(\text{THD}/20)} - 1.76]/6.02$$

The specification of input bandwidth is also important. Most dynamic specifications already discussed are based upon sinusoids. It's certainly commendable that a data converter can operate at its Nyquist rate for sinusoidal inputs. The data converter would then digitize minus full-scale signals to plus full-scale signals on alternative samples.

Some applications, however, encounter a more difficult situation, such as when channels are switched from a multiplexed input. In this case, the sample-and-hold amplifier doesn't get to track the input all along. This is a tougher test of its input bandwidth than other, less-demanding applications.

Similarly, fast-slewing transient conditions need wide input bandwidth and short sample-and-hold acquisition time to acquire the signal. A wide-input-bandwidth data converter also minimizes phase shifts on the signal being digitized.

As mentioned, ADC specifications have different significance with respect to various applications. The input bandwidth, for example, becomes important in avoiding phase shifts between in-phase and quadrature channels in a radar system. Imaging systems, whether based on a charge-coupled device or on infrared, step changes from one pixel to the next. This resembles multichannel signals being switched through a multiplexer. In an imaging application, the edge between a black object on a white background simulates this step condition.

Fast acquisition times and wide input bandwidth ensure performance for these applications. Some applications require that the harmonics, spurious frequencies, and noise not be as large as the lowest signal to be digitized. Spurious-free dynamic range becomes important to these users. In practice, the in-band harmonics specification yields essentially the same information because the worst harmonic is usually greater than the noise floor and spurious frequencies.

Digital storage oscilloscopes (DSOs) take advantage of the aliasing of a data converter and its sampling rate to digitize repetitive frequencies outside the normal range of a data converter. Here, the effective-bits specification yields the DSO's overall accuracy at particular frequencies. Communication systems may have multiple frequencies (tones) and their interaction is of interest. In this case, specifications of two-tone (two-frequency) intermodulation distortion give the needed insight into ADC requirements.☐

Bob Leonard, product marketing manager for Datel, received a BSEE from Northeastern University, Boston, Mass.

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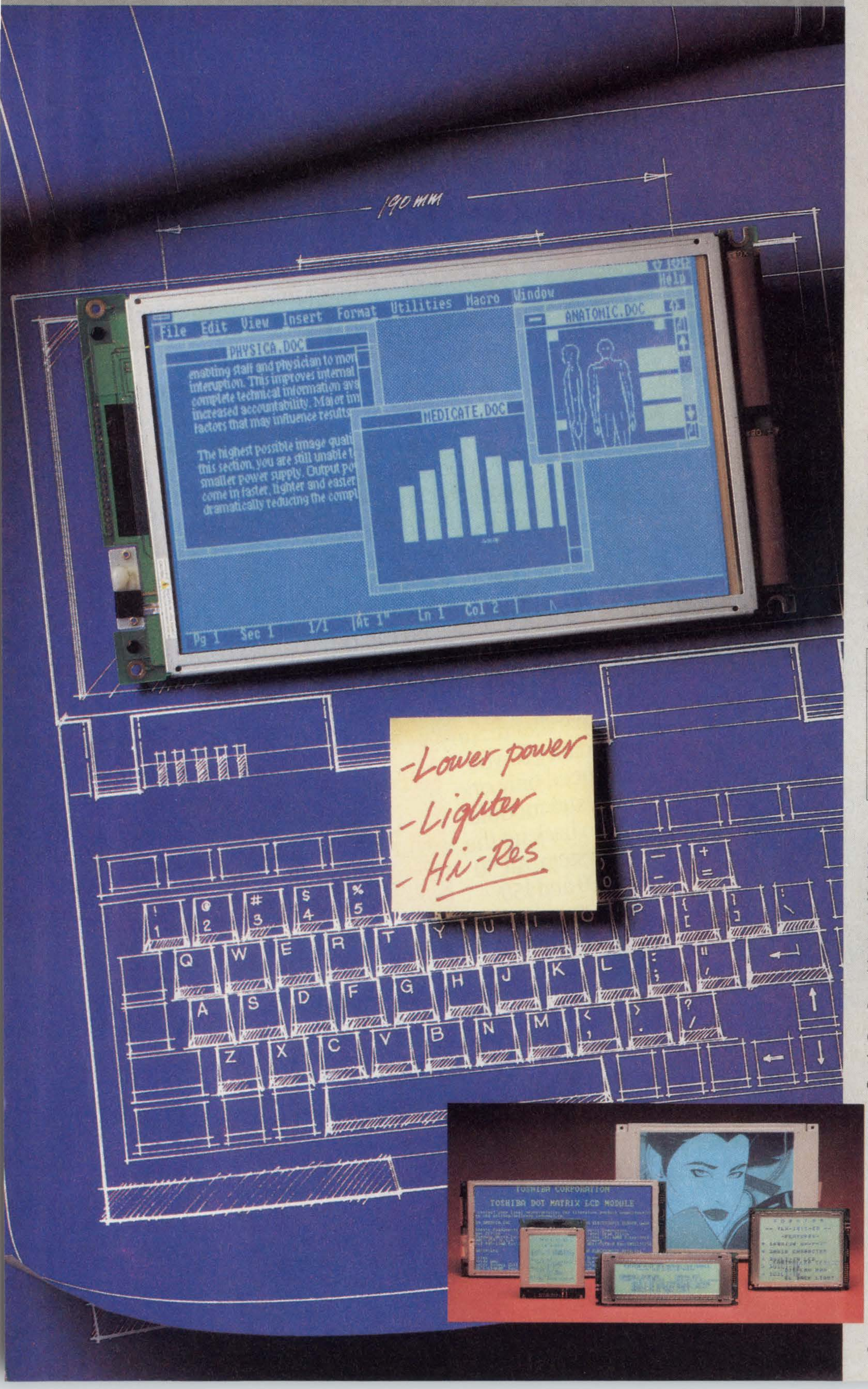

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TLX-1551A-C3M	640×480	276×182×20.5	700g	M-ST	CCFL
TLX-1342-G3B	640×200	275×126×14	450g	B-ST	EL
TLX-711A-EO	240×64	180×65×12	150g	W-ST	EL
TLX-1013-EO	160×128	129×104.5×14	150g	W-ST	EL
TLX-1391-EO	128×128	84.4×100×14	105g	W-ST	EL

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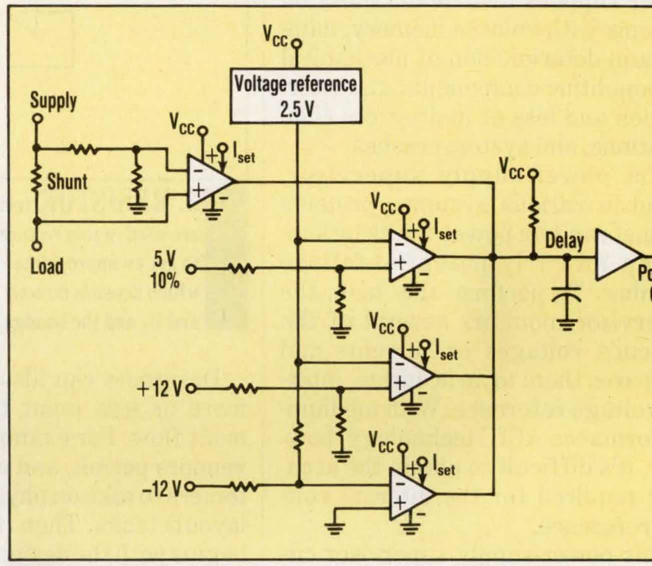
CIRCLE 181

ACHIEVE PRECISION IN LINEAR ASIC DEVICES



1. BASED ON **an analog macrocell, this power-supply supervisor monitors three voltages and a current. If all supplies are within tolerance, a Power OK signal is generated during startup.**

WHEN THE BUILDING BLOCKS OF AN ASIC REQUIRE HIGH SPEED AND ACCURACY, TRY RESISTIVE-TRIMMING TECHNIQUES.

EDWIN LUGO
Raytheon Co.,
Semiconductor Division,
350 Ellis St.,
Mountain View, CA 94043;
(415) 968-9211.

Potential linear ASIC users typically submit applications consisting of medium-performance standard products. Consequently, most linear houses employ a proven, reliable medium-performance technology for their main product line. Such a bipolar technology would feature npn transistors with, say, an f_t equal to 500 MHz and a BV_{CEO} in the 32-V range. This technology is much easier to create and less costly than those needed to implement high slew rates or precision op amps.

But what happens when the proposed application contains one or more blocks requiring higher speed and accuracy? System designers are usually faced with two choices: either leave these components off the ASIC and sacrifice cost, efficiency, and board space, or move the entire application to a higher performance technology where the price of the ASIC can skyrocket.

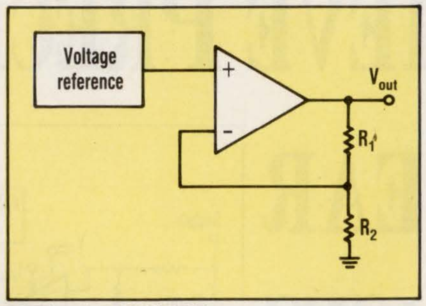
However, a third alternative exists: Use the medium-performance technology and employ resistive-trimming techniques to enhance the precision of the critical blocks. The process is best illustrated by examining the development of a power-supply supervisor circuit. Designers must often implement this function in an ASIC or with standard parts that are restrictive in scope and performance, and occupy extra board space.

ACHIEVE LINEAR ASIC PRECISION

Power-supply malfunctions cause many of the system breakdowns due to some components' delicate nature. The concerns created by faulty power supplies include data loss on systems with volatile memory, damage and deterioration of mechanical or monolithic components, the interruption and loss of in-progress computations, and system crashes.

The power-supply supervisor, found in various systems, protects against random power faults by supplying an early potential-failure warning. To perform this task, the supervisor monitors several of the system's voltages or currents and compares them to an accurate, internal voltage reference. With medium-performance ASIC technology, however, it's difficult to obtain the accuracy required for the internal voltage reference.

This power-supply supervisor circuit uses the most common mode of development interface between the ASIC vendor and the system house. Here, system designers work out the design and system concepts, translate the schematics into the ASIC components, and evaluate the performance through simulation and breadboarding. The ASIC house assists through schematic capture and simulation. They can also advise on choosing the proper tools. However, the final functioning design responsibility rests on the system house. The ASIC vendor finishes the integration by doing circuit layout on silicon and completing the remaining manufacturing process.



2. RESISTOR-trimming techniques are used in this voltage-reference circuit to get an appropriate value for V_{out}, which depends directly on the ratio of R_1 and R_2 and the bandgap voltage, V_{bg}.

Designers can also choose to add more or less input to the development flow. For example, some ASIC vendors permit, and encourage, customers to take on physical-design (IC layout) tasks. Then, the integration begins with the designers evaluating their needs and design concepts.

Most complex, multiple power-supply systems already incorporate some sort of guard against catastrophic faults. Designers can choose among several available predetermined standard-voltage supervisors. In addition, backup power supplies and battery systems are often used to protect against undervoltage. Supervisor chips also warn of overcurrent situations, which can be caused by an internal component's failure (shorting). Other considerations are therefore required. To facilitate proper supply power-up, which would avoid potential overcurrent conditions, power-up and -down systems can be implemented by software.

To make the right choice, designers must first analyze the function's specific requirements. All power-supply schemes start with degradation and fluctuation detection of a power supply outside the permissible limits. In accordance with the system specifications, this detection must be accurate and quick enough to let the system's "brains" activate emergency system-protection mechanisms. In a multiple power-supply system, for example, a 5-V supply may be required for CMOS and TTL logic, a 12-V supply for the analog transducer, human interface, and other linear functions, and a second 12-V high-current supply for the motor drives and servo mechanisms. The number of supplies, as well as their voltage levels and specifications, can vary widely for each application. Yet existing off-the-shelf power supervisors have a predetermined number of controls as well as restrictive specifications. And in many cases, they aren't cost effective. At this point, designers should consider a semicustom solution.

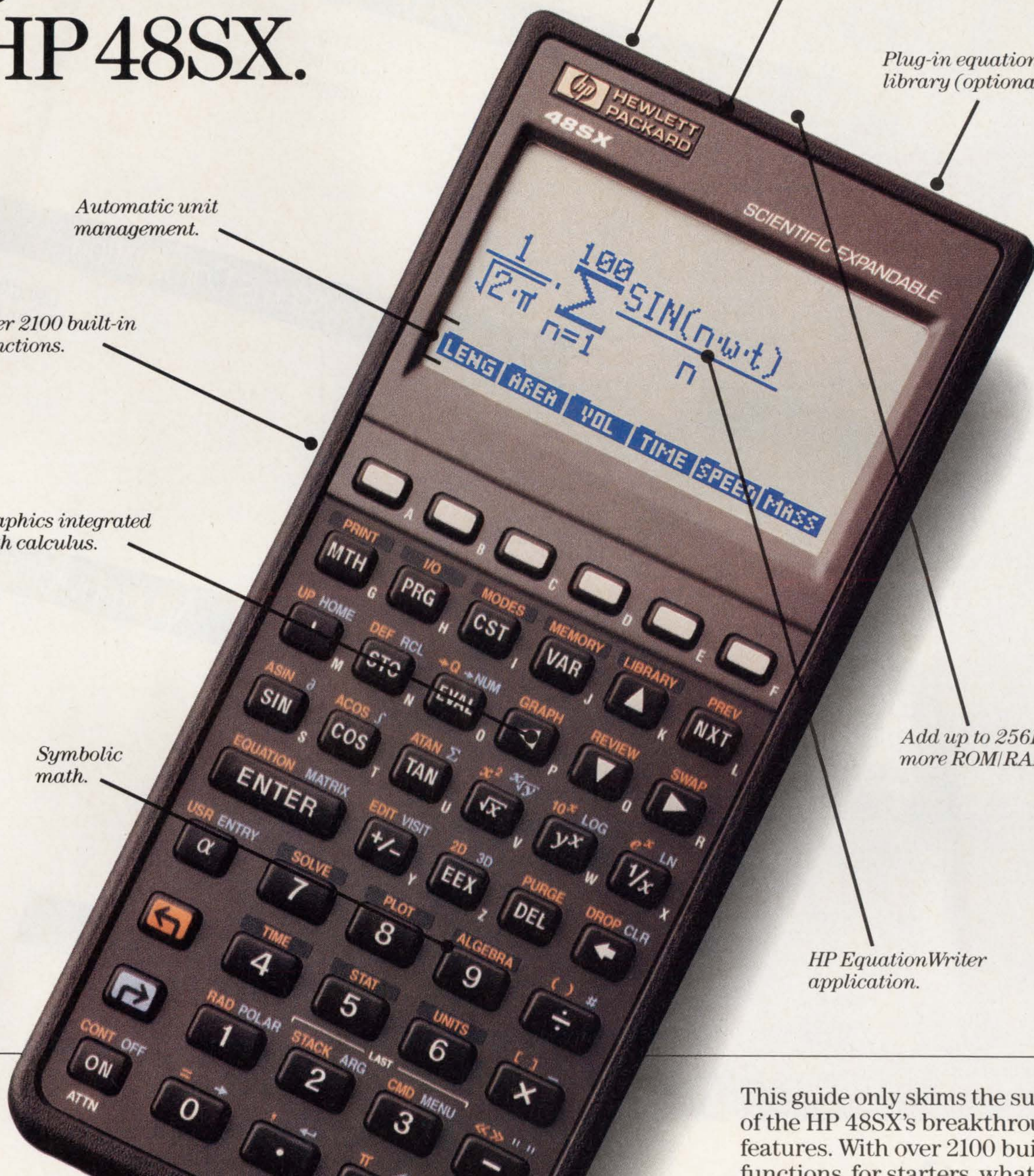
For instance, a macrocell-array approach proves to be a simple, inexpensive alternative in these applications. In this voltage-supervisor application, the designer put together a scheme to monitor three different supplies for undervoltage and one for overcurrent *(Fig. 1)*. In some applications, designers may need special regulation support and error feedback from a key supply. This can be done by adding a few simple array components. In this particular integrated solution, the system receives a TTL Power Up signal when all supplies comply with preset system specifications. The Power Up signal is maintained while in operation by logically ORing all supplies to indicate a healthy system. If any supply fails by falling outside the specified level, the system immediately receives a signal to start power-down procedures, protecting circuitry, motors, and servo mechanisms.

By understanding the power supply's capabilities and the system's sensitive areas, the system designer defines the IC specification in this stage. The designer's logical choice is to implement this function in an IC. Current can be monitored with a shunt configuration, which effectively converts the current to a known voltage. Other power supplies can be monitored using medium-performance comparators with

```
10   FOR N=0 TO 31
20   Z1=(N) AND (1)
30   Z2=((N) AND (2))/2
40   Z3=((N) AND (4))/4
50   Z4=((N) AND (8))/8
60   Z5=((N) AND (16))/16
70   R1=37.5+1/(Z3/85+1/(10+1/(1/5+Z2/12.5+Z1/27.5)))
75   R1=1/(1/R1+1/(25+1/(Z4/60+1/12.5)))
80   R2=15/167+1/(1/5.167+Z5/5.3)
82   R2=R2*13.5/(R2+3.5)
83   VOLD=V
85   V=1.374*(R1+R2)/R2-5.075
86   DV=V-VOLD
88   HALF=VOLD+DV/2
90   LPRINT USING "###";Z5,Z4,Z3,Z2,Z1;
100  LPRINT USING "###.###";V,DV, HALF
200  NEXT N
```

3. A BASIC program calculates the effect of different Zener zapping combinations on the output of a voltage reference. It finds the total resistance of networks A and B.

The power-user's guide to the new HP 48SX.



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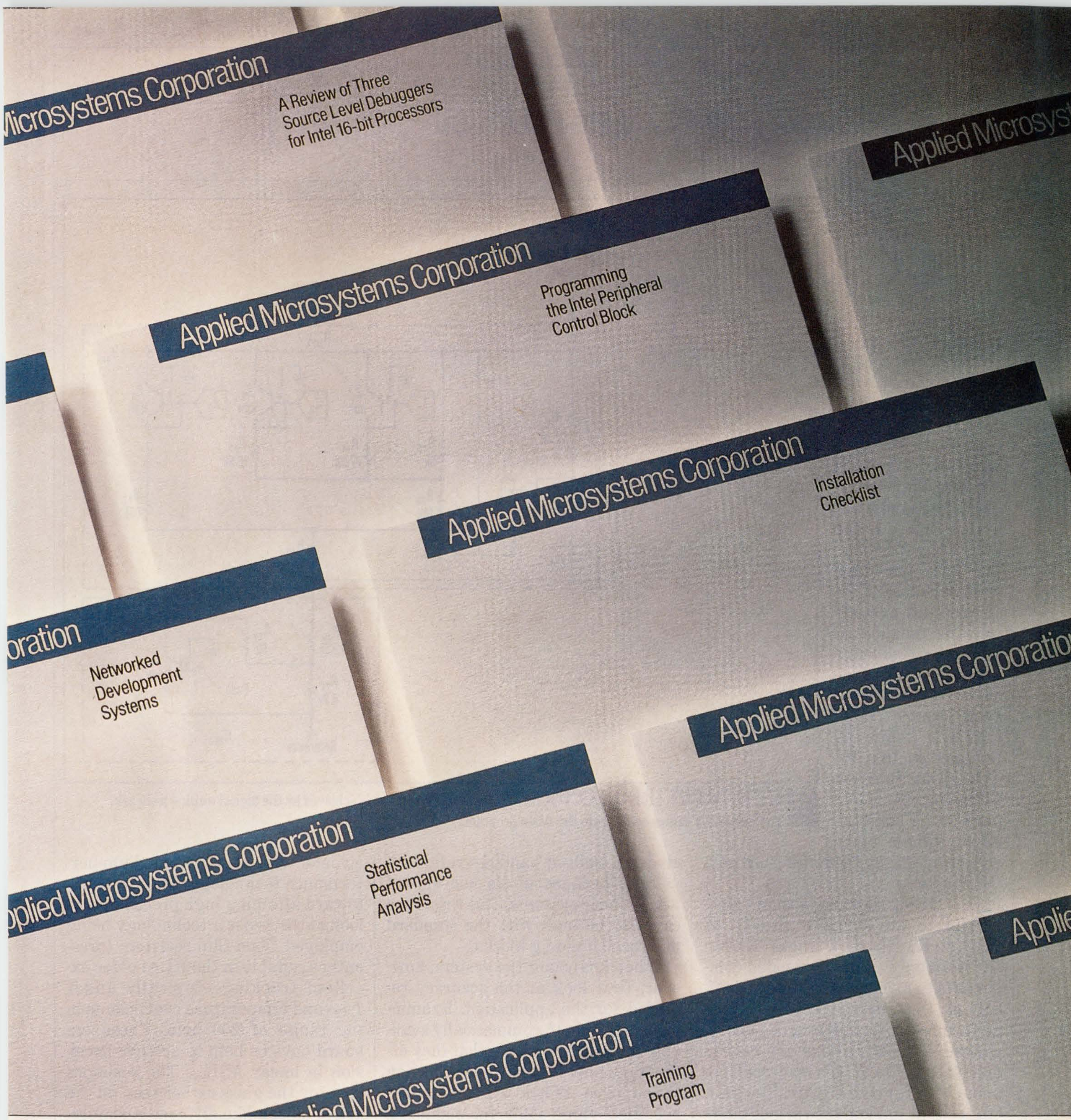
CIRCLE 111



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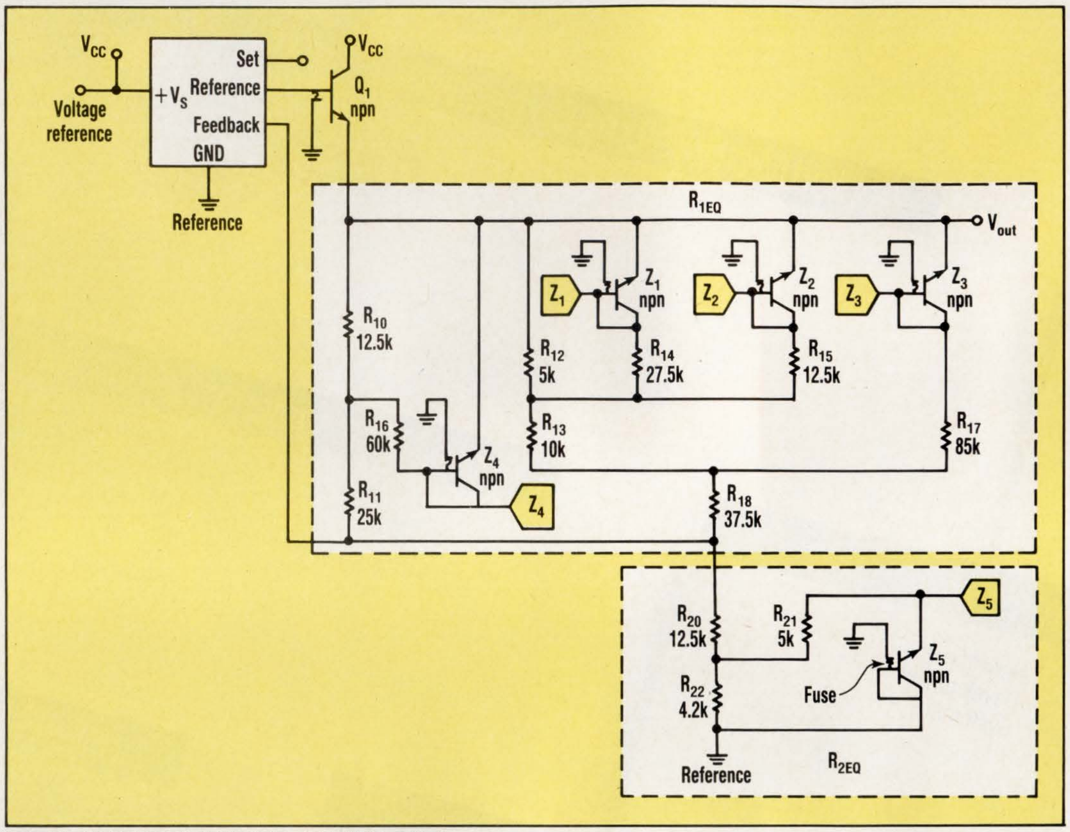
CIRCLE 172

transition times of 1 to 10 μs. They compare the supply voltage to an internally generated voltage. This voltage level is then monitored by relating the good voltage reference to the compared voltage outside the supplies.

Judiciously chosen resistor-voltage dividers limit external voltages to a level that's close to the internal reference. The ASIC permits a wide selection of resistors and customizes the finished IC to these preset supply values. Good resistor matching and temperature tracking are desirable features in this IC. The ORing function following the comparators is completed by simple open-collector logic implementing a wired-OR function.



4. THE REQUIRED ACCURACY for voltage reference is achieved by the digital nulling network. The network's values come from the Basic program.

This ORing concept is then transferred to an existing family of ASICs. Raytheon's linear ASICs (RLA) supply all of the needed components to meet the required specifications. Designers pick these components directly from the RLA library, where all specifications are clearly delineated. The RLA's macrocell approach offers configurable gain stages that implement various functions, including comparators and op amps. The comparator's configurations easily meet the requirements to protect the design in question.

Achieving Accuracy

When looking at the IC's full implementation, one important accuracy issue remains—delivering sufficient precision from the voltage reference supply. A voltage-reference function is simple to implement. In fact, the largest array offered by Raytheon, a 16-macrocell IC, includes a built-in bandgap reference voltage because of its widespread use in linear systems. This reference can also be built with the standard macrocell building blocks.

When analyzing the system, however, first look at the accuracy required for the application. Examining off-the-shelf, commercially available components shows that they offer data-sheet performance when the supplies are held within 5% of the specified value (10% for military). Outside this range, the output levels and functionality can't be guaranteed. Such fluctuations must be detectable to advise the system of malfunctions. A second look at this requirement reveals another aspect. To achieve a satisfactory level of detection within a voltage-supervisor monolithic application, a voltage reference that's stable enough to within one order of magnitude (about 1% voltage accuracy) better than the supply being monitored is needed.

This level of precision is difficult to achieve with standard medium-performance technology. The first step toward attaining high precision is to look at the resistor technology being employed. Thin-film resistors (presently available in the RLA) offer excellent tracking—typically under 1%—and temperature coefficients in the range of 200 ppm. These onboard devices help to achieve precision in linear ASICs. The resistors lay atop the glass rather than on the active silicon like diffused resistors. This avoids parasitic effects and side diffusion, two sources of process errors and inaccuracies.

Spice and data-sheet-parameter analysis of Zener-voltage references built with thin-film resistors and standard npns (f_t = 500 MHz, IgfinC = 200 mA) and pnps can uncover some vital information. Accuracies up to 5% are achievable with this technology, including variations for process. But 5% is still inadequate for this application. Further investigation is needed to meet the ASIC's requirements without resorting to larger macrocells and resistors.

Smart design techniques are a concern when searching for added precision. Designers can refer to other sources of circuit ideas for better designs. One possibility is a bandgap voltage reference with an initial accuracy of about 4%. It's a 1% improvement over the first consideration, yet not enough to meet this application's requirements.

Taking advantage of process variation distributions is another way of attaining more accurate parts. Engineers from the ASIC house, experienced in these matters, can give ASIC designers a good idea of the process distribution for a particular parameter. In the voltage-reference circuit, an accuracy reading of the worst-case distribution extends past the 4% limit. By sorting die to a ±2% limit, 50% of the distribution could be obtained. However, low die yields can lead to higher chip prices. Even with this yield loss, the expected requirements still aren't met. Other undesirable considerations at this point would be to move to a more expensive, higher-performance technology or simply leave the voltage reference outside altogether.

TRIM BY ZENER ZAPPING

One way to get higher precision in the ASIC without moving to more expensive options is to adjust and eliminate error sources with resistor trimming. Although laser trimming is common, it's still considered a "high-technology" method. But in spite of its popularity, laser trimming is a costly solution to a relatively simple problem. Therefore, this option isn't always practical.

Raytheon now offers ASIC designers the trimmable Zener-resistor network method. Zener diodes in parallel or series with pre-chosen resistor values create a digital nulling network that can be trimmed to specific values. This trimming network achieves better accuracy in certain functions, such as a voltage reference. The Zener diodes have relatively high breakdown voltages and never operate in the Zener mode. Moreover, they can short out serially

5	4	3	2	1	Voltage Change		
0	0	0	0	0	0.004	0.004	0.002
0	0	0	0	0	– 0.019	– 0.023	0.008
0	0	0	1	0	– 0.039	– 0.020	– 0.029
0	0	0	1	0	– 0.052	– 0.013	– 0.045
0	0	1	0	0	– 0.064	– 0.013	– 0.058
...							
...							
...							
1	1	1	0	0	0.014	– 0.012	0.020
1	1	1	0	1	– 0.003	– 0.017	0.005
1	1	1	1	0	– 0.018	– 0.015	– 0.001
1	1	1	1	1	– 0.028	– 0.010	– 0.023

5. THE BASIC PROGRAM'S OUTPUT shows the change in the voltage reference's output produced by different zener zapping combinations. The table comes into play later, to create the actual zapping program used during screening.

placed resistors or bring in new parallel resistance. High reverse current through the diode shorts the junction, creating a reliable, low-resistance conductor. This opens a conductive path through the Zener. Therefore, either parallel resistance can be added or serial resistance eliminated.

To benefit from this technique, determine how and when resistor trimming can improve performance. The voltage reference needs an accuracy within 0.5% for a 5-V V_{out} signal. Designers would start with a conventional bandgap voltage reference whose initial accuracy is about 4% typical. V_{out} depends on the ratio of R_1 and R_2 *(Fig. 2)*. This is an ideal opportunity for resistor trimming techniques. The value of V_{out} is:
$V_{out} = V_{bg}[(R_1/R_2)+1]$, where V_{bg} equals the 1.25-V bandgap voltage.

Small variations in resistors R_1 and R_2 will vary the final value of V_{out}. By adjusting their values, higher precision can be achieved, setting the stage for resistor trimming. One way to adjust these values is to add resistance in parallel or series. Designers then choose resistor values that, when added, have a desired predetermined effect on the final value of V_{out}. R_{1EQ} and R_{2EQ} are the total resistor equivalence for the R_1 and R_2 networks. By reducing R_{2EQ}, the resulting V_{out} is reduced. Conversely, V_{out} is increased by reducing R_{1EQ}.

Determining how fine a given application should be adjusted is an important factor. It's desirable to have every Zener-zapped trim (addition or deletion of resistor values) improve the output's accuracy by a factor of two. In other words, one trim improves V_{out} by a factor 2, two by 4, and so on. Unless all possible errors can be identified, it's safer to add one extra trim as a guardband.

Another important consideration is choosing the overall resistor values, as similar values tend to select similar resistor sizes or aspect ratios (the ratio of a resistor's length to its width). This effect maximizes temperature and time-tracking performance. Every trimming option would need a separate bonding pad to be accessible for zapping. And, these pads won't be bonded out to the package.

One tool that can calculate the effect of resistor zapping comes in the form of a Basic program *(Fig. 3)*. The program computes the total resistance of network A (R_1) and B (R_2) based on all zapping combinations. The program iteratively calculates all binary combinations and computes the total amount of V_{out} change produced by the different values of R_{1EQ} and R_{2EQ}. The program also calculates the difference between the alternative zapping combinations.

By inserting different values into the program, a digital nulling network is chosen *(Fig. 4)*. In this case, five different zapping options were selected that could improve the performance by a factor of 32. The main resistor value for R_{2EQ} was chosen as 12.5 because there are many 12.5-kΩ resistors available for voltage references. Trimming resistors with ratios of 12.5 can optimize temperature tracking performance. All other re-

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Overall Performance	0.65	1.35	1.63

(1) All data normalized to DECstation 3100. Comparable configurations tested. Geometric mean used to combine results. Performance will vary depending on applications and environment. (2) Graphics and windowing data measured using X11perf benchmark. CPU Integer and Floating Point performance measured from running SPEC V1.0 workload. (3) SPEC performance estimate based on SUN 4/330 results published by Sun Microsystems, Inc.

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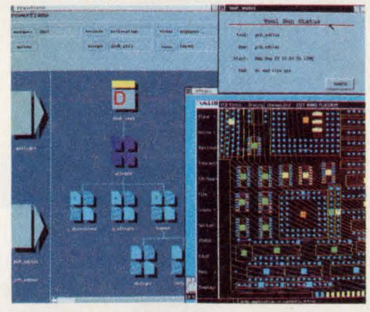

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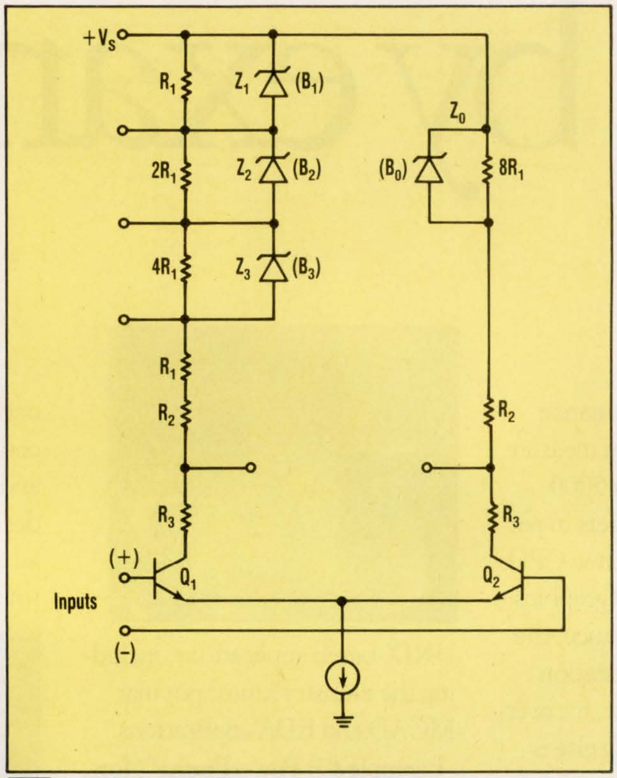
sistor values used in the network were chosen for the amount of change they could produce in the output.

In the finalized network, R_{1EQ} has the equivalent resistance of network A, while R_{2EQ} has the equivalent resistance of network B. All selected resistor values improve the accuracy by a specified percentage. Adding R_{17} (Zener zap 3) improves the accuracy by 1.25%, R_{15} (Zener zap 2) improves the accuracy by 6%, and R_{14} by 3%. The exact values of the changes can be read in the Basic program's output *(Fig. 5)*. The binary table shows the different zapping combinations and its corresponding change on the final value. This table will later create the actual zapping program used during screening.



6. THIS DIGITAL NULLING network controls V_{OS} of the op amps by adjusting the collector-resistor ratio.

Raytheon does the actual zapping or trimming of resistor values during the wafer-sort stage of manufacturing. The values and effect of the different zapping combinations created are submitted to the test engineers, who create a high-level ATE language to execute the zapping loop. The adjustment procedure works as follows: The tester measures the untrimmed V_{out} obtained at the output and finds the difference between the measured and ideal voltages. Then, by accessing a lookup table based on the Basic program's result, the optimal zapping combination is chosen (identified as 0-32) to bring the voltage closer to the desired value. For example, to control whether V_{out} should increase or decrease, zap R_{21} (Z_5).

This process continues iteratively with a programming loop where the tester continually measures V_{out} and chooses the zapping combination based on the required change until the value is brought within the specification. The actual zapping is done by high-current injection supplied by the tester. This method of automatic equipment-control trimming cuts high-volume manufacturing costs.

The procedure that assures an accurate voltage level for all parts is performed on all die at the wafer-sort stage, and is completed within milliseconds. In this case, a 5-V reference with an accuracy better than 0.3% is produced from a medium-performance process and is guaranteed regardless of process variations and transistor matching. In specific and rare cases, the actual zapping can be done on a assembled package by bonding out the appropriate zapping bond pads.

IMPROVE V_{OS}

Another useful and common application of Zener zapping is to minimize V_{OS} on an op amp. The procedure is similar to that for reference-voltage adjustment. In this case, the op amp's input-offset voltage can be adjusted by varying the collector-resistor ratio. In this type of circuit *(Fig. 6)*, if the difference in the two collector resistors (R_C) is a small increment, V_{OS} can be written as:

$$V_{OS} = T_T \ln[(R_C + \Delta R_C)/R_C] = V_T \ln[1 + (\Delta R_C/R_C)].$$

For $\Delta R_C/R_C << 1.0$, $\ln[1 + (DR_C/R_C)] \approx \Delta R_C/R_C$.

As a result, $V_{OS} \approx V_T(\Delta R_C/R_C)$.

$R_2 + R_3 >> 8R_1$, thus:

$$V_{OS} \approx -V_T[R_1/(8R_1 + R_2 + R_3)](7 - B_3B_2B_1) \text{ for } B_0 = 1$$

or

$$V_{OS} \approx V_T[R_1/(R_2 + R_3)](1 + B_3B_2B_1) \text{ for } B_0 = 0.$$

where $B_{0\text{-}3}$ are binary numbers that correspond to the state of zener diodes $Z_{0\text{-}3}$ and V_t is the thermal equivalent voltage, equal to –2.6 mV *(Fig. 5, again)*. The change in V_{OS} is:

$$\Delta V_{OS}(25°C) \approx [-2.6 \text{ mV} (7 - B_3B_2B_1)R_1]/(8R_1 + R_2 + R_3) \text{ when } B_0 = 0.$$

B_N equals 1 when Z_N is unshorted, and equals 0 when Z_N is shorted. $B_1B_2B_3$ will then equal a binary numbers from 000 to 111 or 0 to 7 decimal.

$$\Delta V_{OS}(25°C) \approx [2.6 \text{ mV} (1 + B_3B_2B_1)R_1]/(R_2 + R_3) \text{ when } B_0 \text{ equals } 0.$$

This formula can then determine the effect of the different zapping combinations on the op amp's V_{OS}. Again, by choosing the correct resistor values, designers can adjust the range of flexibility as well as the maximum accuracy required for the application. As in the previous example, once the resistor values and its desired effects are chosen using the formula, the information (in binary lookup table form) is used by Raytheon test engineers to implement the ATE high-level-language zapping loop at wafer sort. V_{OS} is then guaranteed on every die to fall within the required precision. This technique is useful in other applications, such as instrumentation-amp configurations where the common-mode rejection ratio must be controlled to more than 60 dB.

These techniques open up a new dimension in linear ASIC applications.

DESIGN APPLICATIONS

ACHIEVE LINEAR ASIC PRECISION

Nothing can replace smart design techniques when dealing with a system. Therefore, it's best to start with an optimized design for the parameters that are critical to the application. However, by using this trimming technique, relatively high-precision components can be attained, such as voltage references and op amps, while maintaining a medium-performance technology to minimize risk, cost, and engineering.

Using all of the procedures described, ASIC designers can start a design with components contained in the linear-array library. Some necessary functions may have already been implemented and presented in Raytheon's linear applications manual. As in all ASIC designs, the primary steps consist of evaluating the existing technology in light of the system requirements. This is done by checking the data-sheet parameters of typical functions implemented with this technology, such as op amps or comparators, and see how they compare with the present system or the one needed. If the existing technology doesn't meet the system requirements, designers may look for different ways to implement the function in question. One approach is to change the gain-stage design by using individual transistors rather than preconfigured gain stages. Taking advantage of the on-board thin-film resistors is another way to achieve higher accuracy. To reemphasize, standard linear manuals and textbooks can also be a good source of novel circuit ideas.

After the circuit design is optimized for performance for the specific need, it's always best to check the simulated results using the complete Spice parameters supplied by Raytheon. Kit parts are also available to evaluate real-life performance employing the same silicon geometries that are used for final integration. Temperature and voltage effect can also be determined in a real-life environment.

If the performance still falls short of the requirements, consider using the techniques described in the article. Designers first must determine if the parameter in question can be controlled by a resistor network. If so, the level of accuracy to be achieved should be determined in relation to the existing performance. Yield considerations can also be evaluated.

By using the procedures described in this voltage-reference application, designers can put together an appropriate network and determine its effect on the parameter's final value. Helpful tools, such as previously discussed Basic program, can be provided. This is an iterative process that gives designers total flexibility in customizing the function. The final results, in lookup-table form, can build a zapping loop on high-level language to be used by the ATE. Resistor trimming is usually done in packaged parts at the customer site, similar to field-programmable parts.

One drawback of resistor trimming with Zener zaps is the extra pads used within the linear array. For every zapping point, one pad must access that diode with the necessary programming current to metallize the Zener junction. This current is in the range of 400 to 600 mA for about 2 ms. This current capability must reside in the user's tester. With a little ingenuity, users don't need many extra pads to get the performance level that's typically seen only on high-performance systems.

Designers' familiarity with linear ASICs is still nowhere near that of digital arrays. However, by properly utilizing existing tools and with some ingenuity, designers can get higher and more efficient levels of integration without investing in more sophisticated designs or moving to more expensive technologies. Good design practices coupled with flexible technologies helps solve integration problems.

Edwin Lugo, a field applications engineer for Raytheon, received a BSEE from the University of California at Berkeley.

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Now you can build the Multibus II discipline right into your system for the price of VME or EISA. Multibus II's new MPI bus interface chip is perfect for building simple analog, digital, or serial interface boards. It costs just $40 in quantities over 100.

The Multibus II product line has expanded, too. In the last year alone, we've added over a dozen I/O and CPU board products. And you can choose from the more than 500 Multibus II products on the market, including 150 full-size Multibus II boards.

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To view the entire expanse of Multibus II products — from over 100 vendors — call Intel at (800) 548-4725, Dept. AA60. Ask for a free copy of the *1990 Multibus II Product Directory.*

So don't delay. Call now, and start a change for the better.

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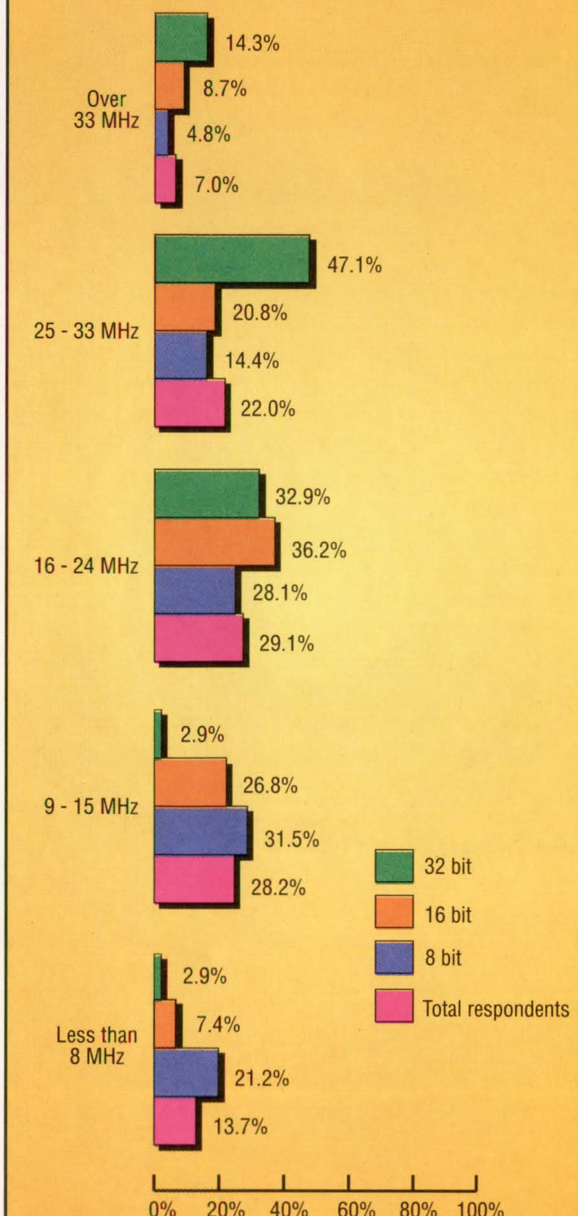
CIRCLE 113

QUICKLOOK

EDITED BY SHERRIE VAN TYLE

WHAT IS THE FASTEST MICROPROCESSOR SPEED YOU REQUIRE IN YOUR SYSTEMS ?



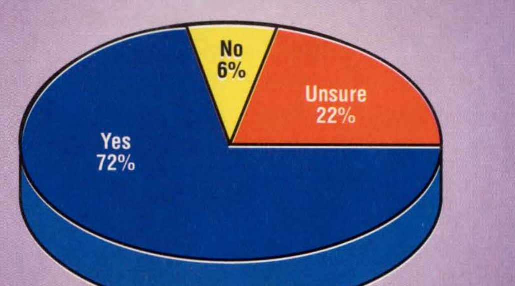
Source: a survey of Electronic Design readers conducted by the Adams Co., Palo Alto, Calif.

MARKET FACTS

Software developers are scrambling to come up with Windows 3 versions of their applications now that this latest edition has taken off. More than 1 million copies of Windows 3 have shipped since May. Replacing cryptic DOS commands with icons, Windows 3 affords multitasking and data exchanges between applications. The total software market should be worth about $6.5 billion this year, according to International Data Corp., Framingham, Mass.

Robertson Stephens & Co., a San Francisco-based market research company, recently surveyed 83 Fortune 500 sites. With about 300,000 PCs installed at these sites, 72% of the microcomputer managers said that they planned to use Windows 3. Although the software lists for $149—with a $99 street price—running Windows doesn't come cheap. The managers surveyed said it costs an average of $950 to equip a PC for Windows—that includes the cost of boosting RAM to 2 Mbytes and buying Windows versions of applications. Moreover, that price tag doesn't include upgrading hardware—running multiple applications under Windows 3 requires a 386 processor.

DO YOU PLAN TO USE WINDOWS 3?



Source: a Robertson Stephens & Co. Survey

OFFERS YOU CAN'T REFUSE

Connectors of all sorts are described in a free 576-page catalog. The *Electronic Interconnection Systems Product Ordering Guide* has specification drawings and photos of EM Electronic Products Division products. The catalog has information on IC socket connectors, board- and wire-mount socket connectors, stacking connectors, headers, cable, and assembly equipment. Products are indexed by grid spacing, part number, and product type. To request a copy, write to 3M Electronic Products Division Catalog, P. O. Box 3064, Cedar Rapids, Iowa 52406-3064.

-Time, Big-Time.

One glance at the full array of options Motorola offers in real-time, and you'll see why it's become the developer's platform of choice. For both target and host environments, no other single vendor has anything like it.

One reason is our long-time experience with real-time technology, beginning with our pioneering work back in 1980. Another is the broad spectrum of our product line, which includes ICs, boards, systems, and software. In short, Motorola has everything you need to build real-time applications ranging from simulation to industrial automation to imaging and more.

CISC
RISC

Yet another reason to choose Motorola is our unending commitment to open standards. Our real-time platform gives you standards-based choices at various levels of integration. The centerpiece of this non-proprietary approach is VMEexec,™ our wide-open, totally integrated development environment. VMEexec allows you to use standard UNIX® interfaces to write a single set of application code, and then reuse it for other projects. Better still, you can combine any software product that conforms to these standards. VMEexec includes a high-performance real-time executive, a strong run-time connection to UNIX-based systems, flexible and efficient real-time I/O and file systems, as well as powerful development and debug capabilities. And because VMEexec is integrated with the hardware, you can begin software development even before the hardware is available.

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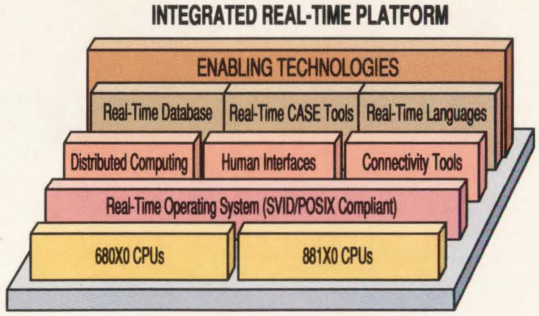
INTEGRATED REAL-TIME PLATFORM



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QUICKLOOK

BEST SELLERS

Which technical books are the most popular in Silicon Valley?

ELECTRONICS:

1. *Art of Electronics* by Paul Horowitz and Winifred Hill. Cambridge University Press, 1989. ***$47.95.***

2. *Noise Reduction Techniques in Electronic Systems*, 2nd ed. by Henry W. Ott. Wiley, 1988. ***$47.95.***

3. *SPICE: A Guide to Circuit Simulation and Analysis Using PSPICE* by Paul Tuinega. Prentice-Hall, 1988. ***$20.60***

4. *Logic Design Principles* by Edward J. McCluskey. Prentice Hall, 1986. ***$50.***

5. *Introduction to VLSI Design* by Eugene D. Fabricus. McGraw-Hill, 1990. ***$48.95.***

COMPUTER SCIENCE:

1. *Object-oriented Design with Applications* by Grady Booch. Addison Wesley, 1990. ***$37.25.***

2. *Computer Architecture: A Quantitative Approach* by John Hennessy and David Patterson. Morgan Kaufman, 1990. ***$54.95.***

3. *Designing Object-oriented Software* by Rebecca Wirfs-Brock, Brian Wilkerson, and Lauren Wiener. Prentice-Hall, 1990. ***$26.95.***

4. *Object-oriented Software* by Ann L. Winblad. Addison- Wesley, 1990. ***$28.50.***

5. *Object Orientation* by Setrag Khoshafian and Razmik Abnous. Wiley, 1990. ***$26.95.***

This list is compiled for *Electronic Design* by Stacey's Bookstore, 219 University Ave., Palo Alto, CA 94301: (415) 326-0681; fax (415) 326-0693.

ACRONYMS

EISA	Extended industry standard architecture
MMACS	Million multiply-accumulates per second
OODB	Object-oriented database
SPOX	DSP operating system
SQL	Structured (database) query language
SSOP	Shrink small outline package
UGBW	Unity gain bandwidth, a measure of op amp performance
V_{on} DMOS	On voltage for double diffused MOS

HOT PC PRODUCTS

Some software calls for entering key combinations again and again. So it often makes sense to store these strings of keystrokes as macros. The Chameleon device, which attaches to a PC keyboard, stores 8k worth of macros in nonvolatile RAM. Keys can be remapped or redefined. Key combinations can be up- and downloaded from the host. Sirius Industries' Chameleon is IBM PC, XT, and AT compatible. The unit, which takes up no host memory, draws its power from the keyboard. Users can safeguard their macros by unplugging the Chameleon from the keyboard and taking it home. The Chameleon lists for $89. For more information, contact the company at 21608 North 20th Ave., Phoenix, AZ 85027; (800) 229-0034; fax (602) 780-0140.

With Agiler's Touchman, users move their fingers over a panel rather than roll the pointing device. Because Touchman stays put, it's suitable for laptop and notebook computers; it also can be built into a regular size keyboard. Touchman lists for $89. For more information, contact Contek International Corp., 66 Field Crest Rd., New Canaan, CT 06840; (203) 972-3406; fax (203) 972-0156.

KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458

Changes in technology and new-product development time are tightly coupled. Time to market must be held to a minimum so that technological change does not obsolete the product currently under development. Said another way, the best insurance for getting a project done is to keep its development time short so that technological change does not affect delivering the product to market.

The technical people involved in setting the product's definition have a difficult balancing act to perform. They must select a technological sword that gives a competitive advantage without excessive cost, as well as one that has reasonable developmental risk. Also, they must look ahead to ensure that the technology selected will remain competitive when the product reaches the market. These factors need to be addressed and incorporated in the product's definition.

On me-two-with-a-twist products, technology selections must be made almost entirely on time-to-market considerations. Selections are made up front and they must be right! Product development must stay in phase with the cycle time of technology. If Intel and Motorola produce a new generation of microprocessor every 18 months, then products based on that technology must follow suit within a few months of supplier introduction to remain competitive. It's becoming well accepted knowledge within the cyclic product development environment that a few months' savings on each product turn can produce a 6- to 12-month advantage by the time the third turn takes place. This time advantage is generally sufficient to gain a dominant competitive position. The Definition Matrix gives developers of me-too-with-a-twist products adequate checks and balances to select the appropriate technology up front so that it will not require revision in the planning and executive phases. This type of development cannot tolerate a technology change and still remain competitive.

Other efforts are likely to assume more technological risk. It is not unusual to have technological development and product development occurring concurrently on first-of-a-kind, derivative, and next-generation product efforts. The Definition Matrix provides the initial structure to assist in the management of the explosive mixture. Later, elements will be added to assist in the planning and execution phases of the project. A product development team that completes the new product development matrix will have identified most technological risk areas and will have thought through most of the management details associated with moving forward at an aggressive pace.

QUICKLOOK

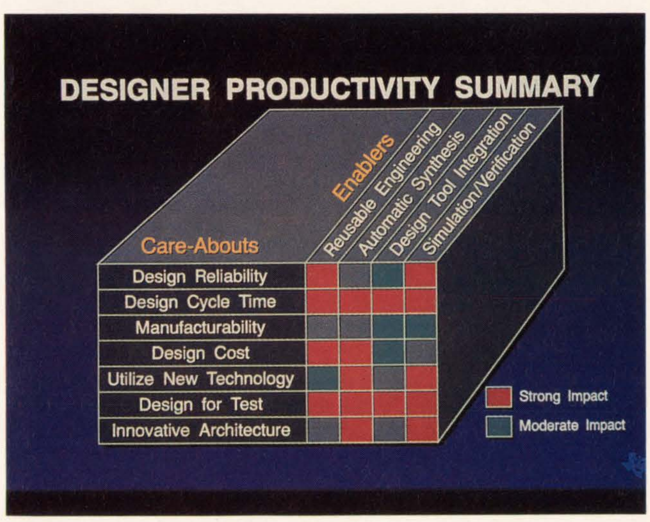
TIPS ON INVESTING

An engineering maxim says: The only constant is change. Nowhere is that truer than in investing. Today's rapidly changing economic and political scenes are reshaping the investment world. A return to basic investment principles helps engineers achieve long-range goals of building wealth, preserving capital, planning for retirement, and paying for their children's education. Two commonsense principles, patience and discipline, not only build wealth, but help engineers avoid investment pitfalls. Here's a checklist of common investor errors.

- Fuzzy goals. An engineer must first ask, "Why am I investing—for immediate income or long-term capital gains?"
- Investing without understanding. An engineer must understand what each of his investments represents. He should never buy an investment because someone wants to sell him one.
- Not adjusting to changing market conditions. Just as an engineer's goals can change over time, the long-term prospects of financial markets may change greatly. Investors must respond to trends.
- Investing in today's marketplace with yesterday's investments. Today's market is made up of much more than stocks and bonds.
- Inconsistent security selection. The more riskes assumed, the greater the potential for profit, or loss. Investors must weigh each investment according to these parameters.
- Profits taken too soon. Some investors takes profits early for shortern gains, shrinking profit potential.
- Losses allowed to run. If an investment performs poorly, engineers may be better off cutting their losses quickly.
- Lack of understanding of tax laws. Engineers must rethink investment strategies because of recent tax reforms.
- Ignorance of the time value of money. There is good earning potential in long-term investments in which interest or dividends are compounded over time, expecially if interest accrues on a tax-free or tax-deferred basis.
- Unrealistic expectations. Some investors demand dramatic and immediate return from investments. Yet investing in securities is a means of putting money to work toward a financial end.

An engineer who finds himself facing any of these issues should seek the help of a professional financial advisor.

by Henry Wiesel, a financial consultant with Shearson Lehman Bros., Shrewsbury, N. J. Questions and comments are invited in care of the news editor, Electronic Design.



1-MINUTE OPINIONS

What do you think about the education that young engineers are getting these days?

In Stephen Scrupski's editorial regarding engineering education (*Electronic Design*, Aug. 23), he states, "I must question the wisdom of many humanities courses for engineers when there's so much new technology to be learned—what courses are they forfeiting to fit these non-engineering subjects into the curriculum?"

The more important question to be asked here is: What part of their education would they be forfeiting by *not* including these "non-engineering" subjects in the curriculum? One of the present complaints by industrial managers is the lack of communication skills of most engineers. Any knowledge of a new technology is useless if an engineer cannot effectively communicate his ideas.

An engineering education should prepare an engineer for life, not just for his first job upon graduation. Today's new technologies become tomorrow's obsolete technologies, but engineering fundamentals such as Ohm's law remain the same. An engineering curriculum should provide a solid theoretical foundation as well as develop good communication skills. **Ted Manikas**, *Research Triangle Park, North Carolina.*

Communication skills are poor. Engineering colleges have lower verbal SAT score entrance requirements than the liberal arts colleges. Communication skills should be developed in high school.

Our college professors have shortened the length of the semester by 19%, down from 16 weeks to 13 weeks during the last 20 years. Our educators don't want to educate.

Computers are used extensively in college engineering. Shouldn't high school typing be a mandatory prerequisite for computer usage? One semester of typing would increase speed and accuracy. Typing isn't in vogue.

College teaching assistants (TAs) have poor communication skills. English is a second language. Engineering courses are demanding enough without facing a TA who can't communicate.

To address your questions specifically, four years should be adequate to provide the engineering foundation to perform effectively. The course structure should stick to basics of engineering, math, and physics and should not push superficial subjects that are in vogue. Volleyball isn't worth three credits.

Education is only the starting point. The first few years out of college require some guidance and mentoring while developing good engineering skills. You don't get this in school or at companies that lose or replace their senior engineers with inexperienced personnel.

As an associate of mine put it: The younger engineers are running around looking for information that our senior engineers have at their fingertips. **Richard F. Tax**, *River Vale, N. J.*

What's your opinion on the education of today's young engineers? Are there any subject areas that are being under- or over-emphasized by college or university curriculums? What role should courses in the humanities play in engineering education? Are four years enough to give young engineers a good foundation in their field or are five years required? Send your opinions to our Reader Opinions fax number, which is (201) 393-0637. Or send your comments to Compuserve address 75410,3624. Or mail your responses to *Electronic Design*, Reader Opinions, 611 Route 46 West, Hasbrouck Heights, NJ 07604.

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Get on board. Call today for more information on our motherboard VGA solutions.
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This full 16-bit CL-GD5320 lets you implement 16-bit or 8-bit VGA capabilities on your motherboard with as few as 5 other chips and two 256K x 4 DRAMs. Get a complete solution that saves time, space, power, and expense. You still get all the speed, features and flexibility you're looking for.

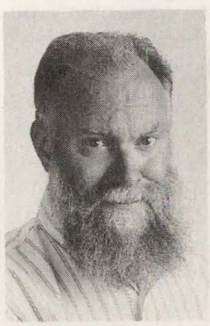
CIRRUS LOGIC

C L O S I N G T H E G A P

WHAT'S ALL THIS CMRR STUFF, ANYHOW?

Recently, many people have asked me about how to test op amps for common-mode rejection ratio (CMRR), which is defined as the delta of the offset voltage (V_{OS}) versus the common-mode voltage (V_{CM}). The first thing I tell them is how *not* to measure CMRR *(Fig. 1)*. If you drive a sine wave or triangle wave into point A, it seems like the output error, as seen by a floating scope, will be (N+1) times (V_{CM} divided by the CMRR).

But that's not quite true: you will see (N+1) times (the CM error *plus* the gain error). So, at moderate frequencies where the gain is rolling off and the CMRR is still high, you will see mostly the gain error, and your curve of CMRR vs. frequency will look just as bad as the Bode plot. That's because with this circuit, that's just what you will be seeing!



BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

It turns out that a few op-amp data sheets still exist in which the CMRR curve is stated to be the same as the Bode plot. The National LF400 and LF401 are two examples; next year we will correct those curves to show that the common-mode rejection ratio is actually much higher than the gain at 100 or 1000 Hz.

Ah, let's avoid that floating scope. We'll drive the sine wave generator into the mid-point of the power supply, and ground the scope and ground point A *(Fig. 2)*. Then we'll get the true CMRR, because the output won't have to swing. Right? Wrong! The circuit function hasn't changed at all; only the viewpoint of the observer changed. The output *does* have to swing, referred to any power supply, so this still gives the *same wrong answer*. You may *say* that you asked for the CMRR as a function of frequency—but the answer is, in most cases, the curve of gain vs. frequency.

What about, as an alternative, the well-known scheme where an extra servo amplifier closes the loop and doesn't require the op-amp output to do any swinging *(Fig. 3)*? That's okay at dc. So it's adequate for dc testing with automatic test equipment (ATE), for production test, and for stepped dc levels.

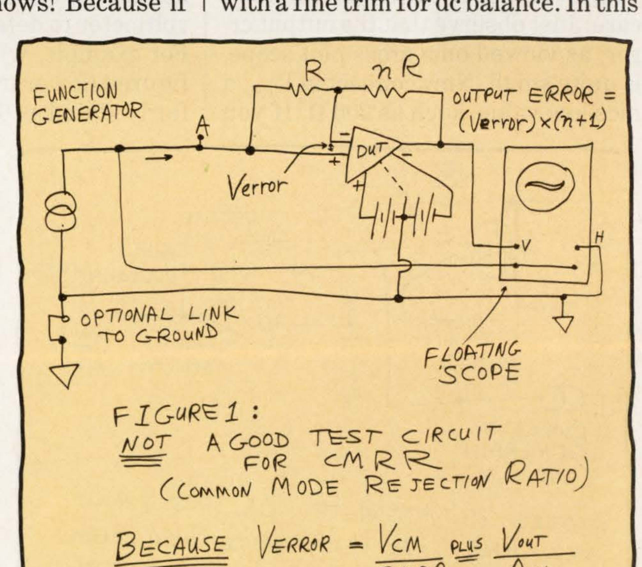
And it will give the same answer as my circuit (which I'll discuss a little later) at all low frequencies up to where it doesn't give the same answer. Now what frequency would that be? Nobody knows! Because if you have an op amp with low CMRR, the servo scheme will work accurately up to one frequency. And if you have an op amp with high CMRR, the servo scheme will work accurately only up to a different frequency.

Also, the servo amplifier adds so much gain into the loop that ringing, overshoot, or marginal stability at some mid frequencies is inevitable. That's much too horrible for me to worry about. I'll just avoid that by using a circuit which gives very consistent and predictable results.

When I ran an LF356 in the circuit of figure 1, I got an error of 4 mV pk-pk at 1 kHz—a big fat quadrature error, 90 degrees out of phase with the output *(Fig. 4, upper trace)*. If you think that's the CM error, you might say the CMRR is as low as 5000 at 1 kHz, and falling rapidly as the frequency increases. But the actual CMRR is about 0.2 mV pk-pk *(Fig. 4, lower trace)*. As a result, the CMRR is about 100,000 at 1 kHz or any lower frequency. In addition, the CM error on this unit isn't really linear. As you get near –9 V, the error gets more nonlinear (this is a –9-V to +12-V CM range on a 12-V supply; I chose a ±12-V supply so my function generator could overdrive the inputs).

As you can see, this business of CMRR testing isn't trivial. Just how, then, can we test for CMRR and get the *right* results? Well, there's a darned fine circuit I invented myself about 22 years ago *(Fig. 5)*. It has limitations, but it's the best circuit I've seen. Let's choose $R_1 = R_{11} = 1k$, $R_2 = R_{12} = 10k$, and $R_3 = 200k$ and R_4 = a 500-Ω single-turn carbon pot, or its equivalent.

These values will permit us to set up a more-or-less balanced bridge, with a fine trim for dc balance. In this



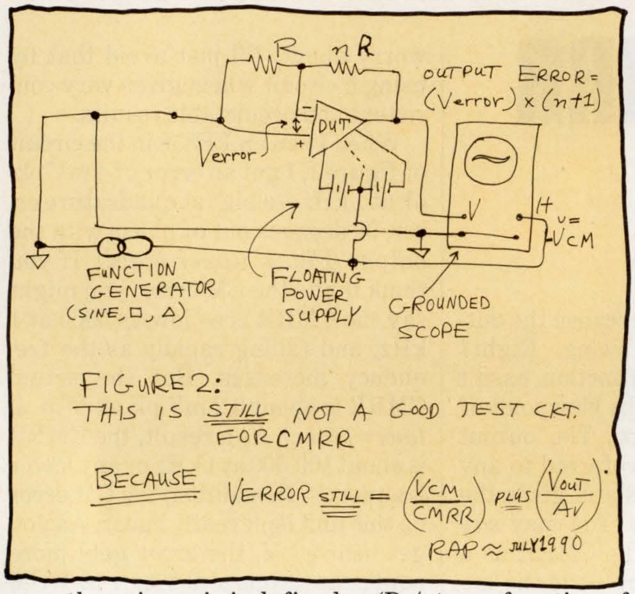


FIGURE 2: THIS IS STILL NOT A GOOD TEST CKT. FOR CMRR BECAUSE VERROR STILL = (VCM/CMRR) PLUS (VOUT/AV). RAP ≈ JULY 1990

case, the noise gain is defined as (R_f/R_{in} + 1), or about 11. Let's put a ±11-volt sine wave into the signal input so that the CM voltage is about ±10 volts. The output error signal will be about 11 times the error voltage plus some function of the mismatch of all those resistors.

Okay, first connect V_{in} to the scope's horizontal input, V_{out} to the vertical input, and operate the scope in cross-plot (X-Y) mode. Trim pot R_4 until the output error is very small, or until the slope is nominally flat. We don't know if the CMRR error is balanced out by the resistor error or whatever, but it turns out we don't care. Just observe that the output error, as viewed on a cross-plot scope, is quite small. Now connect in R_{100a} a nice low value, such as 200 Ω. If you sit down and compute it, the noise gain rises from 11 to 111. Namely, the noise gain *was* (1 + R_2/R_1), increasing to (1 + R_2/R_1) plus (R_2 + R_{12})/R_{100}. In this example, that's an increase of 100. So, you're now looking at a *change* of V_{out} equal to 100 times the input error voltage, (and that is V_{CM} divided by CMRR).

Of course, it's unlikely for this error voltage to be a linear function of V_{CM}, which is why I recommend you look at it with a scope in X-Y mode. Too many people are inclined to make a pretend game that CMRR is constant at all levels and CM error is a linear function of V_{CM}. So they just look at 2 points and assume every other voltage has a linear error; and that's just *too* silly. Even if you want to use some ATE you will want to look at this error in at least 3 places—maybe even at 4 or 5 voltages.

Another good reason to use a scope in the X-Y mode is so you can use your eyeball to subtract out the noise. You certainly can't use an ac voltmeter to detect the CMRR error. For example, with the waveform of figure 4 (lower trace), the CM error is fairly stated as 0.2 mV pk-pk, not 0.5 mV pk-pk (as your meter might say if you let it include the noise).

Anyhow, if you have a good amplifier with a CMRR of about 100 dB, the CM error will be about 200 μV pk-pk. When it's magnified by 100, you can easily see an output error of 20 mV pk-pk. If you have a really good unit with CMRR of 120 or 140 dB, you'll want to clip in the R_{100b}, such as 20 Ω, and then the delta (noise gain) will be 1000. The noise will be magnified by 1000, but so will the error, and you can see what you need to see. *Now,* I won't get embroiled in the question: Are you trying to see exactly how good the CMRR really is, or just if the CMRR is better than the data-sheet value? In either case, this approach is the best way I have seen.

For use with ATE, you don't have to look with a scope; you can use a step or trapezoidal wave and look just at the dc levels at the ends, or the middle, or wherever you need. Note that you needn't trim that resistor network all of the time, nor do you have to trim it perfectly. All you have to know is that when the noise gain changes from a low value to a high value, and the output error changes, the *change* of the output error is of interest—not really the pk-pk value before or after, but the delta. You don't *have to* trim the resistor to get the slope perfect, but that's the easy way for the guy working at his bench to see and appreciate the changes.

This is a great circuit to fool around with. When you get it running, you'll want to test every op amp in your area, because it gives you such a neat high-resolution view. It gives you a good *feel* for what's happening, rather than just hard, cold, dumb numbers. For example, if you see a 22-mV pk-pk output signal that's caused by a 22 μV error signal, you know that the CMRR really is way up near a million, which is much more educational than a cold "119.2 dB" statement.

Besides, you learn rather quickly that the display's slope and curvature are important. Not all amplifiers with the same "119.2 dB" of CMRR are actually the same. Some have a positive slope, some may have a negative slope, and some curve madly, so that if you took a 2-point measurement, the slope would change wildly, depending on which two points you choose (if you increase the amplitude of the input signal, you can also see plainly where severe distortion sets in—that's the extent of the common-mode range).

Limitations: If you set the noise

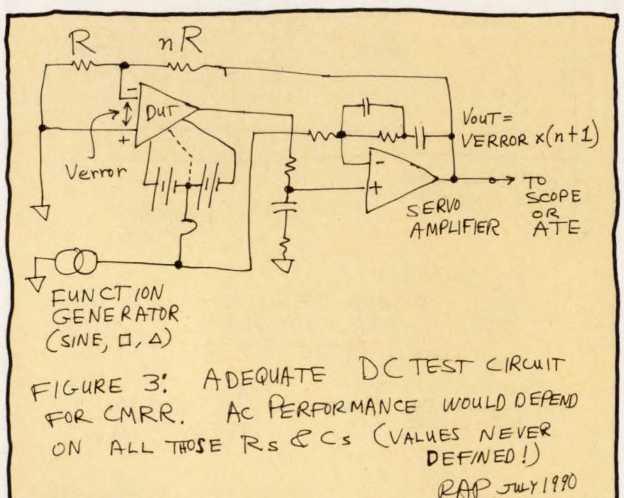
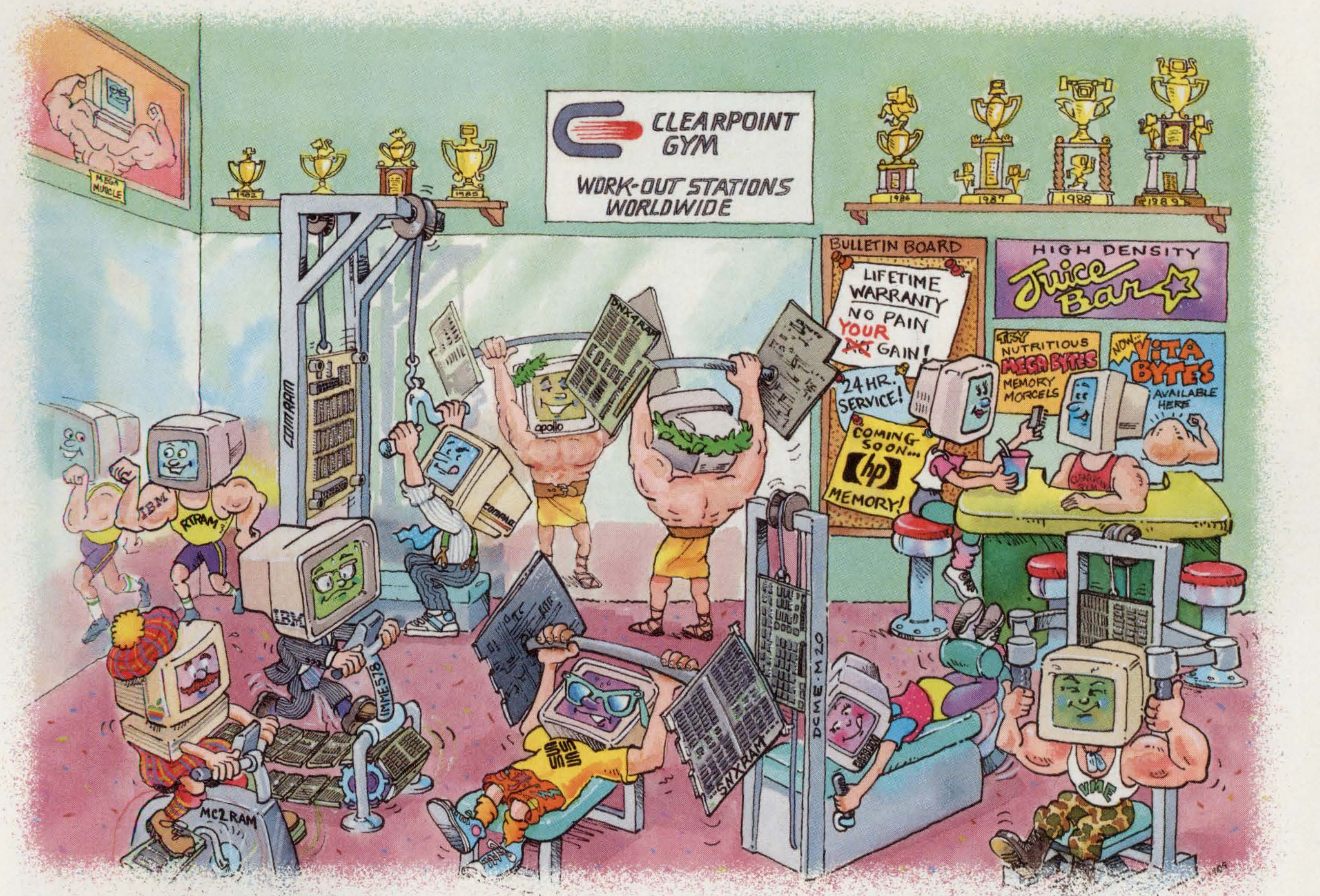


FIGURE 3: ADEQUATE DC TEST CIRCUIT FOR CMRR. AC PERFORMANCE WOULD DEPEND ON ALL THOSE Rs & Cs (VALUES NEVER DEFINED!) RAP JULY 1990

Pump Up Your Performance



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- 3/60, 3/80, 386i, 4/60, 4/1xx, 4/3xx
- 3/E

APOLLO Family Compatibles
- DN 3010A, 3500, 4000, 4500
- DN 3000

COMPAQ Family Compatibles
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- Deskpro 20e expansion memory

APPLE Family Compatibles
- All Macintoshes excluding the 512

IBM Family Compatibles
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CIRCLE 178

PEASE PORRIDGE

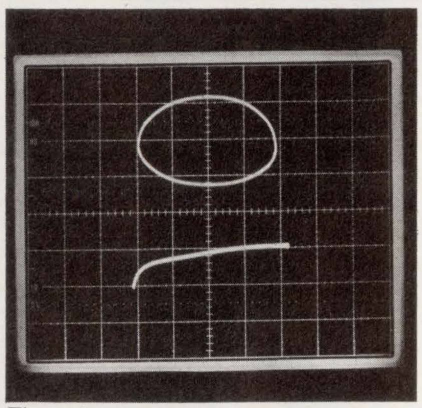

Figure 4

gain as high as 100, then this circuit, of course, will be 3 dB down at (F_{GBW}) divided by 100, so you would only use this up to about 1 kHz on an ordinary 1-MHz op amp, and only up to 100 Hz at a gain of 1000. That's not too bad, really.

To look at CMRR above 1 kHz, you might use $R_{100c} = 2k$ to give good results up to 10 kHz. In other words, you have to engineer this circuit a little to know where it gives valid data. You can't avoid the fact that thinking is required. Sorry about that.

For really fast work, I go to a high-speed low-gain version where $R_1 = R_{11} = 5k$, $R_2 = R_{12} = 5k$, and $R_{100} = 2k$ or 1k or 0.5k. This works pretty well up to 50 kHz or more, depending on what gain-bandwidth product your amplifier has.

For best results at ac, it's important to avoid stray capacitance of wires or of a real switch at the points where you connect to R_{100a} or R_{100b}. Usually I get excellent results from just grabbing on to the resistor with a mini-gator clip. You can avoid the stray pF that way. If you use a good selector switch, with all of the wires dressed neatly in the *air* (which is an excellent insulator) you may be able to get decent bandwidth, but you should be aware that you are probably measuring the ac CMRR of your set-up, not of the op amp. Actually, I was discussing this circuit with a colleague, when I realized the best way to make up this 20-Ω resistor is to connect one 10-Ω resistor to each input, and then clip the other ends together with a mini-gator clip up in the air. Balanced strays, and all that.

If you have an op amp with low gain or low gm, you may want to add in a buffer follower at a-b *(Fig. 5, again)*, so the amplifier does not generate a big error due to its low gain. The LM6361 would need a buffer as it only has a gain of 3000 with a load of 10k, and its CMRR is a lot higher than 3000. Altogether, I find this circuit has better resolution and gives less trouble than any other circuit for measuring CM error. And the price is right: a few resistors and a mini-gator clip.

All for now. / Comments invited! / RAP / Robert A. Pease / Engineer

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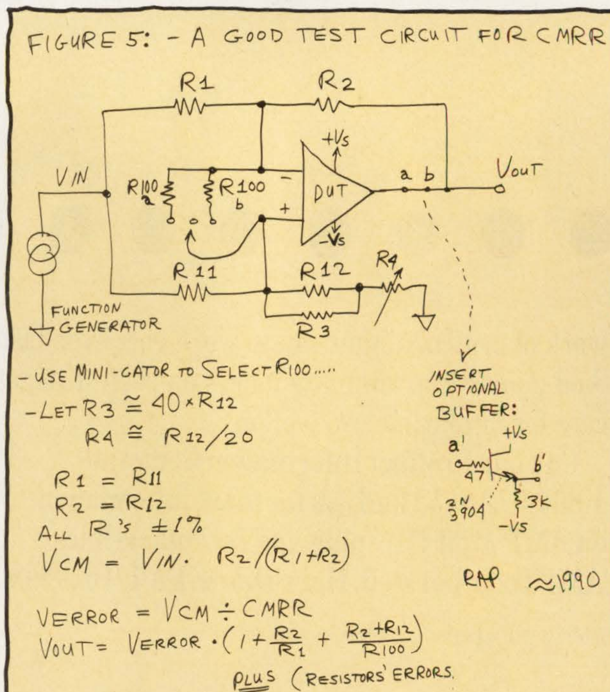

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Product Selection Guide

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FPF8050HRUK	640 x 400	4	10″
FPF8050HFUGA*	640 x 400	1	10″
FPF8060HRUM	640 x 480	1	10½″
FPF8060HRUK	640 x 480	4	10½″
FPF8060HRUS-120	640 x 480	16	10½″
FPF12896HRUF*	1024 x 768	1	15″
FPF128102HRUF*	1024 x 816	1	18″

*Also available as a monitor.

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CIRCLE 212

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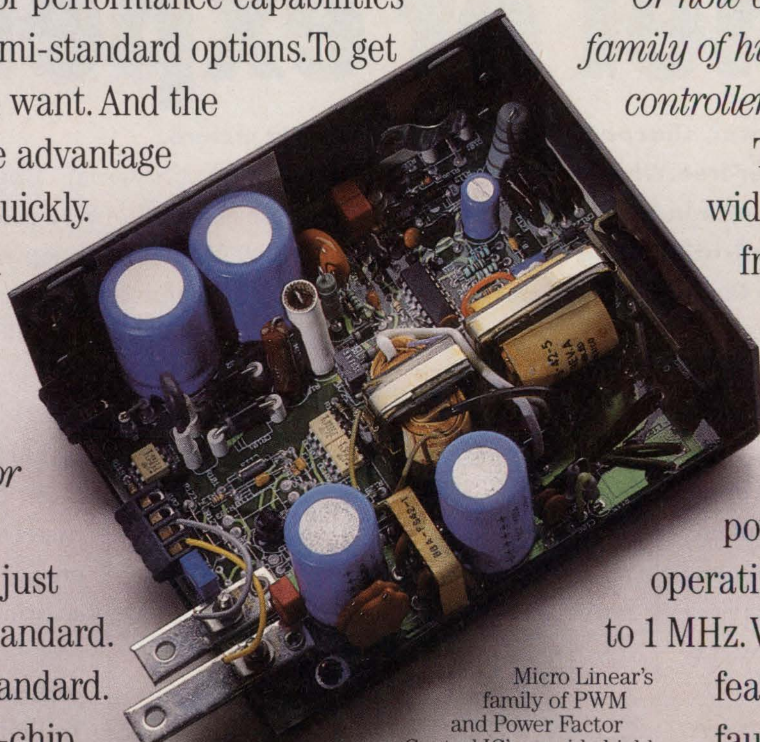

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Product Category	Features
Power Factor Control	High Efficiency Flyback or Boost
PWM Controllers	1 MHz, Additional Fault Protection, Synchronization
Resonant Control	ZVS and ZCS to 3 MHz
Motor Control	BLDC Sensorless Commutation

of the power curve.

capability. Even stability improvements.

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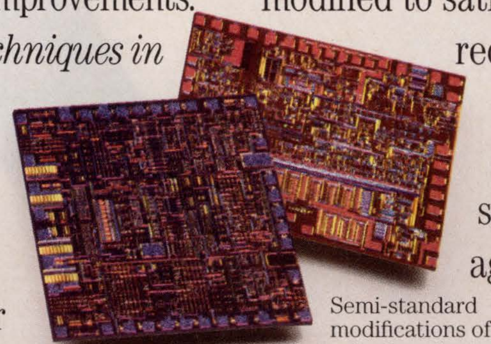

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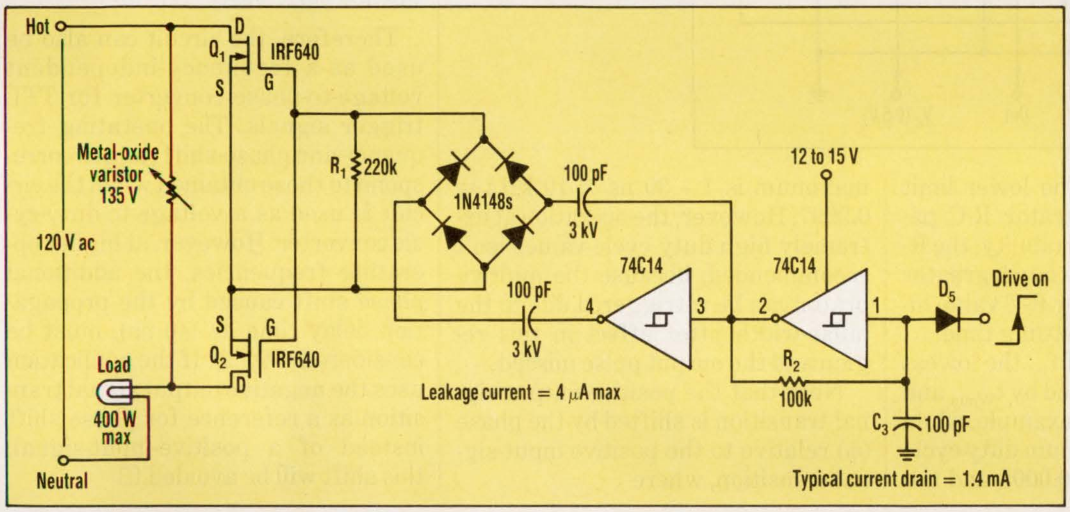
CIRCLE 187

CIRCLE 521 ATTAIN DRIVE FOR MOSFET RELAY

DAVID JOHNSON
10198 W. Berry Dr., Littleton, CO 80127; (303) 973-8408.

The necessary drive for a MOSFET bidirectional relay, used to switch power to 120-V ac loads, can be supplied by a circuit where two CMOS Schmitt triggers (74C14) form a 100-kHz square-wave oscillator with complementary outputs *(see the figure)*. The two output signals are coupled to the FET gates of the relay circuit through a pair of 100-pF capacitors and a bridge rectifier that converts the ac voltage to dc. Sufficient gate-source capacitance within the FETs eliminates the need for any added filtering.

Resistor R_1's value (220 kΩ) is chosen to discharge the capacitance and turn the transistors off in about 2 ms once the drive signal has been disabled. Faster switching times are possible using lower values of R_1 and higher drive frequencies. With the values shown, less than 2 mA of current is needed from a 12- to 15-V supply to drive the circuit. In addition, with such a small coupling capacitance, the leakage current from the power line to the CMOS driver circuit is less than 5 μA, which is sufficient isolation for many applications. Leakage currents less than 1 μA are possible by using a 1-MHz drive frequency and 12-pF coupling capacitors.□



TO SUPPLY the drive needed for a MOSFET bidirectional relay, the Schmitt triggers (74C14) form a 100-kHz square-wave oscillator with complementary outputs. The outputs are rectified bridge and applied to the FET gates of the relay circuit. R_1 turns off the transistors.

CIRCLE 522 CONVERT V_C TO DUTY CYCLE

B. STASICKI
Max Planck Institut für Strömungsforschung, Göttingen, W. Germany; (0551) 709-1.

A voltage-to-duty-cycle converter can be useful in many applications such as pulse-forming networks. This externally-triggered circuit generates a rectangular TTL (high-speed CMOS) signal with a duty cycle that's a linear function of the control voltage (V_C). The period of the TTL signal is given by the trigger frequency, f_{in}. The duty cycle is frequency independent over a wide range.

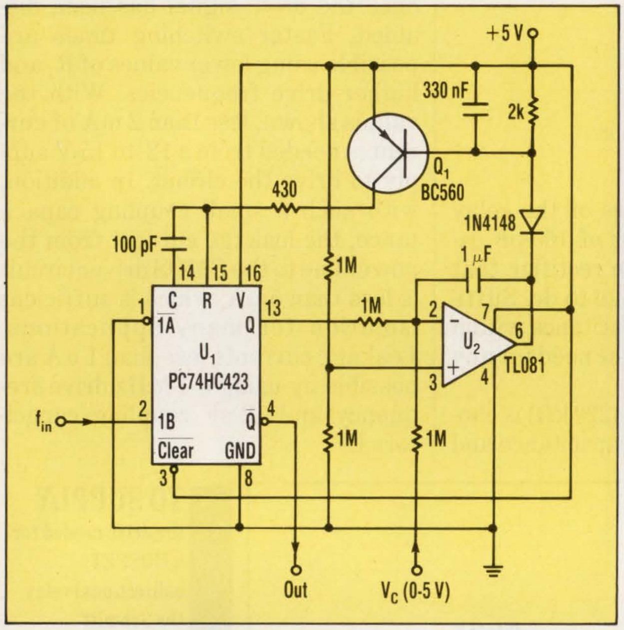
The circuit consists of a positive-edge triggered monostable multivibrator (U_1) and an analog integrator (U_2) *(Fig. 1)*. U_1, from an HC or HCT family, generates rail-to-rail pulses of duration t_W, controlled by the collector current of Q_1. The duty cycle of U_1's output equals $t_W \times f_{in}$.

The mean value of a rectangular signal is proportional to its duty cycle. As a result, U_2 will supply an error signal for the feedback loop. This signal controls U_1's output-pulse width, t_W, keeping the duty cycle at a constant value given by the control voltage, V_C, where

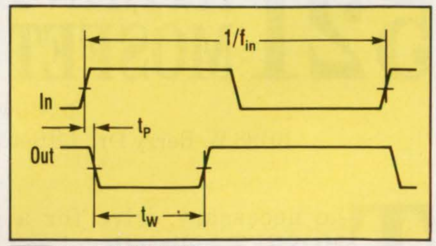
$$\text{duty cycle} = 1 - V_C/5.$$

To get a duty cycle directly proportional to the control voltage, add an analog inverter that supplies $5\text{ V} - V_C$.

The circuit is powered by a +5-V supply. Because this voltage is also used as a reference, is must be stable to obtain good voltage-to-duty-cycle-conversion accuracy. With the components specified in figure 1, the converter is stable and accurate in the range from 100 Hz to above 1 MHz. The settling time for large and fast V_C changes is about 1 second. The upper-frequency limit is due to the minimum pulse width t_{Wmin} (50 ns) that can be generated by a multivibrator and the multivibrator recov-



1. THIS circuit converts voltage to duty cycle by taking the output of a monostable multivibrator (U_1) and sending it through an integrator (U_2). The integrator then supplies a signal that controls U_1's output-pulse width, keeping the duty cycle at a constant value (V_C).



2. AT HIGH frequencies, when the circuit is used as a voltage-to-phase-shift converter, propagation-delay time (t_P) must be considered. The shift caused by t_P can be avoided if a negative-output transition is used as a reference.

ery time t_R (30 ns). The lower limit depends on the integrator R-C parameter. To maintain stability, the R-C parameter should be much greater than $1/f_{in}$. But a higher R-C value increases the circuit's settling time.

For a given value of f_{in}, the lowest duty cycle is determined by t_{Wmin} and the highest by t_R. For example, when $f_{in} = 10$ kHz, the minimum duty cycle is 50 ns × 10 kHz = 0.0005 and the maximum is 1 − 30 ns × 10 kHz = 0.9997. However, the operation at extremely high duty cycle values isn't recommended, because the multivibrator can be retriggered due to the pulse-width jitter effect in this region and the output pulse missed.

Note that the positive-output signal transition is shifted by the phase (ϕ) relative to the positive-input-signal transition, where

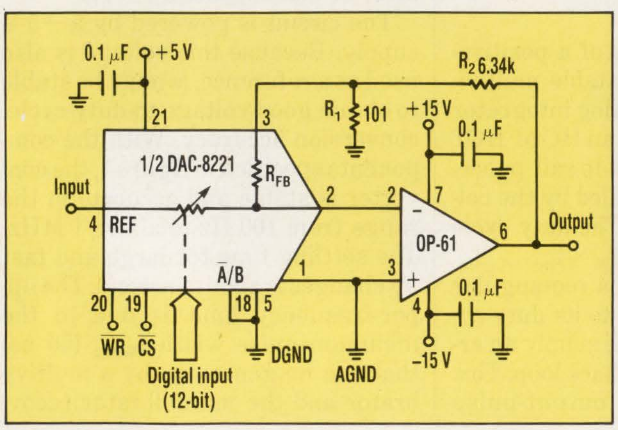
$$\phi(\text{degrees}) = 360(1 - V_C/5).$$

Therefore, the circuit can also be used as a frequency-independent voltage-to-phase converter for TTL trigger signals. The operating frequency and phase-shift ranges correspond to those obtained when the circuit is used as a voltage-to-duty-cycle converter. However, at higher operating frequencies, the additional phase shift caused by the propagation delay time, t_P (40 ns), must be considered *(Fig. 2)*. If the application uses the negative output signal transition as a reference for phase shift instead of a positive-input-signal, this shift will be avoided.☐

CIRCLE **523**

ADD PROGRAMMABLE GAIN, ATTENUATION

JAMES WONG
Analog Devices, Precision Monolithics Div., 1500 Space Park Dr., PO Box 58020, Santa Clara, CA 95052; (408) 727-9222.



1. BY adding R_1 and R_2 in the feedback loop around a DAC, the circuit functions as a digitally-programmable amp. The gain or attenuation is variable over the range of 1/64 to 64. The resistors are connected in a T-configuration.

By adding two resistors to the output-amp feedback loop of a current-output digital-to-analog converter (DAC), both gain control and attenuation control can be achieved *(Fig. 1)*. This digitally programmable amplifier produces gain and attenuation in the range of 1/64 to 64. The circuit gets its range from a 12-bit CMOS DAC.

The design works because the transfer function from the DAC's input to its output is purely voltage at-

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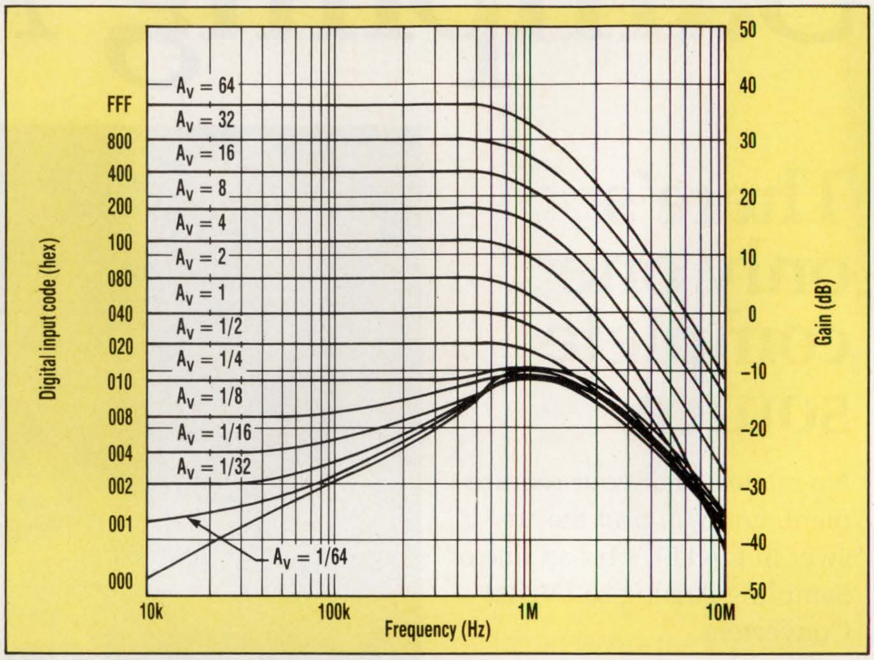
Bruce C. Trump, Burr-Brown Corp., 6730 S. Tucson Blvd., Tucson AZ 85706; (602) 746-7347. His idea: *"PC Detects Remote Switch Closures."*

tenuation. Connecting R_1 and R_2 in a "T" configuration inside the output amp's feedback loop produces a voltage gain from the resistor junction to the output. If R_1 is much less than R_{FB} (11 kΩ in this example), the gain produced nearly equals $1 + (R_2/R_1)$, or 64. The result is a programmable gain amp with a transfer function of

$$A_V = -(D/4096)(64),$$

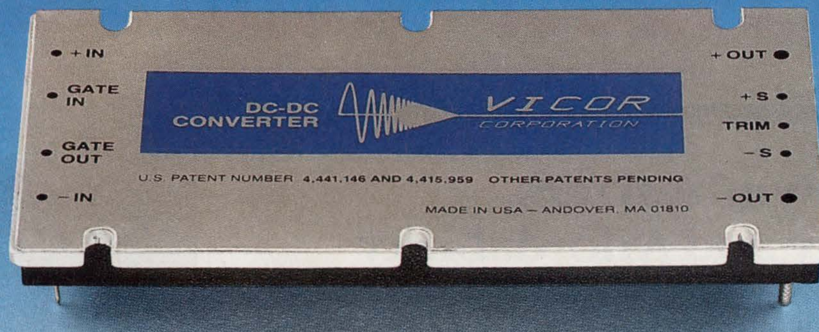
where D represents the DAC's binary-weighted digital code. Of course, the added gain of the T-network increases the circuit's noise gain. Therefore, it's important to choose first a low-noise amplifier.

By using a low-noise, high-frequency op amp, such as the OP-61, the circuit will have a wide bandwidth performance even at high gain settings. The circuit's frequency response can be plotted at different gain settings *(Fig. 2)*. At high gains, the amp has a 1-MHz bandwidth.□



2. GAIN IS PLOTTED **versus frequency for various digital inputs of the DAC. The amplifier has a 1-MHz bandwidth at high gains, but it drops for gains below 1/4.**

1985 : smallest



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1990 : smaller

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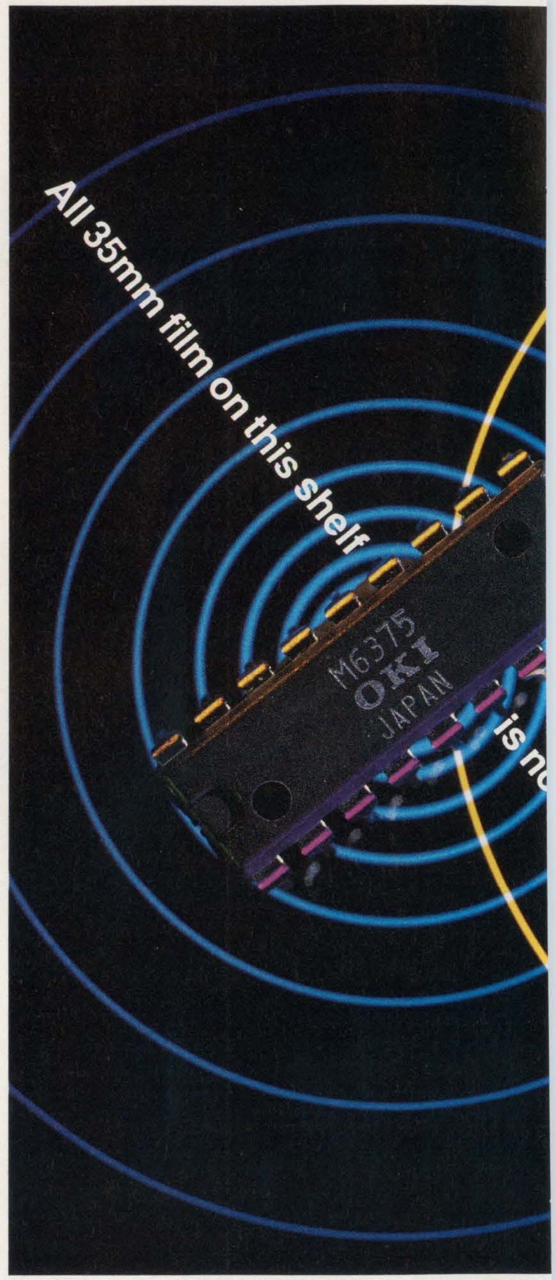

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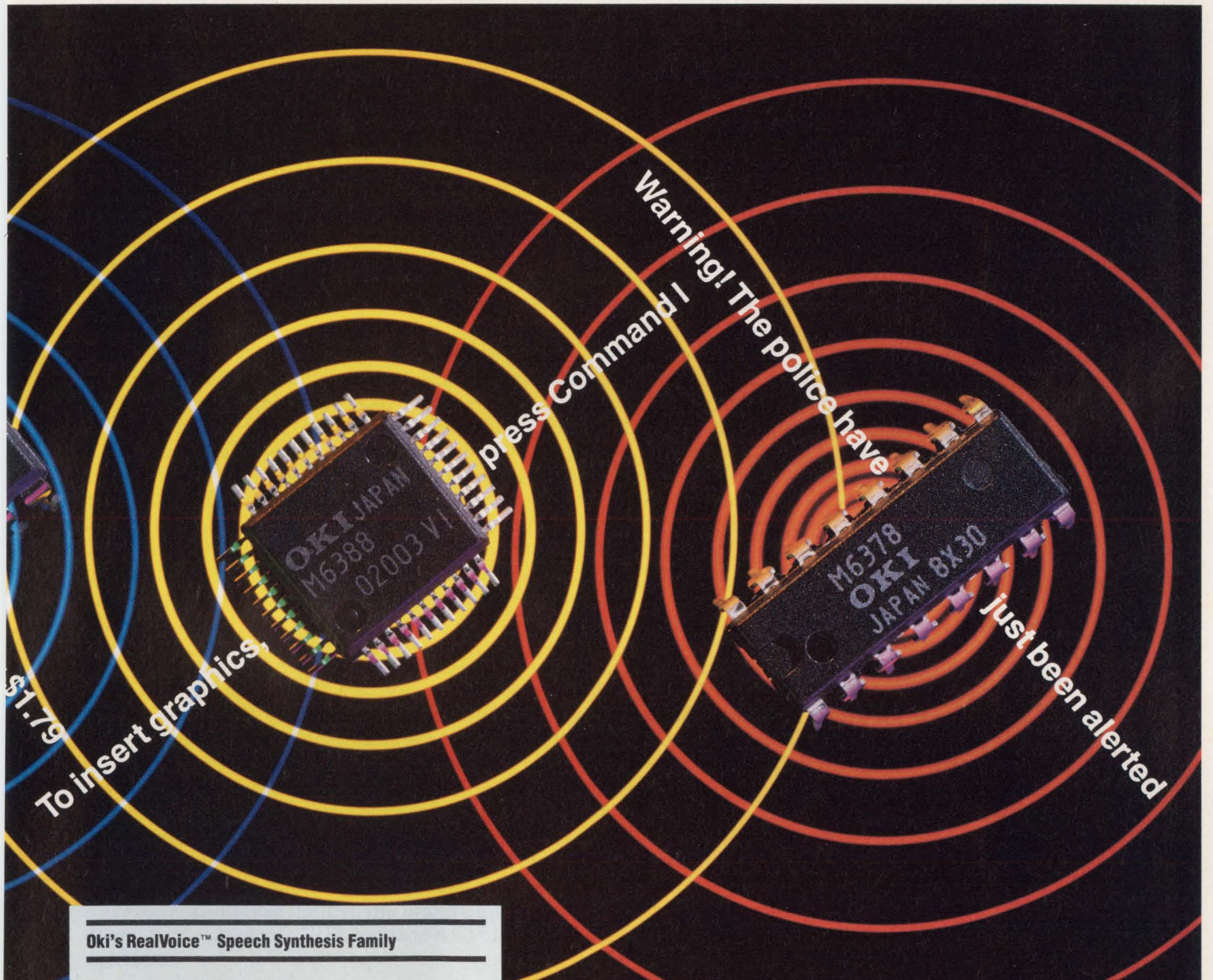

Oki's RealVoice™ Speech Synthesis Family

Part Number	Description
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MSM6372	Speech synthesizer with 128K ROM, 5 secs
MSM6373	Speech synthesizer with 256K ROM, 10 secs
MSM6374	Speech synthesizer with 512K ROM, 20 secs
MSM6375	Speech synthesizer with 1M ROM, 40 secs
MSM6376	Evaluation chip for MSM6372/73/74/75
MSM6378	Speech synthesizer with 256K OTP ROM
MSM6388	Solid-state recorder/1M serial register I/F

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CIRCLE 213

Scaled Math Chip Ups Floating-Point Speed

By moving the 80387 floating-point math coprocessor's original design to its advanced, 1-μm CMOS process line, Intel Corp., Santa Clara, Calif., improved the chip's throughput by almost 20%. The fabrication line now yields chips that operate at system clock speeds of 16, 20, and 25 MHz, as well as a high-speed design (previously in production) that runs at 33 MHz. Intended for computer systems that employ the 80386DX full 32-bit processor, the enhanced math chip accelerates such programs as Quattro Pro from Borland, AutoCad from Autodesk, and Freelance Plus from Lotus, plus over a thousand others. The finer-line process also reduces the chip's power consumption by about one-third over the previous 387 math chip. Prices for the 80387 math coprocessor start at $570 for the 16-MHz version and increase to $647, $814, and $994, respectively, for the 20-, 25-, and 33-MHz versions. Samples and production quantities are available immediately. Contact Dennis Carter, (408) 987-8080. *DB* **CIRCLE 391**

Fast IGBTs Cut Energy Losses To New Lows

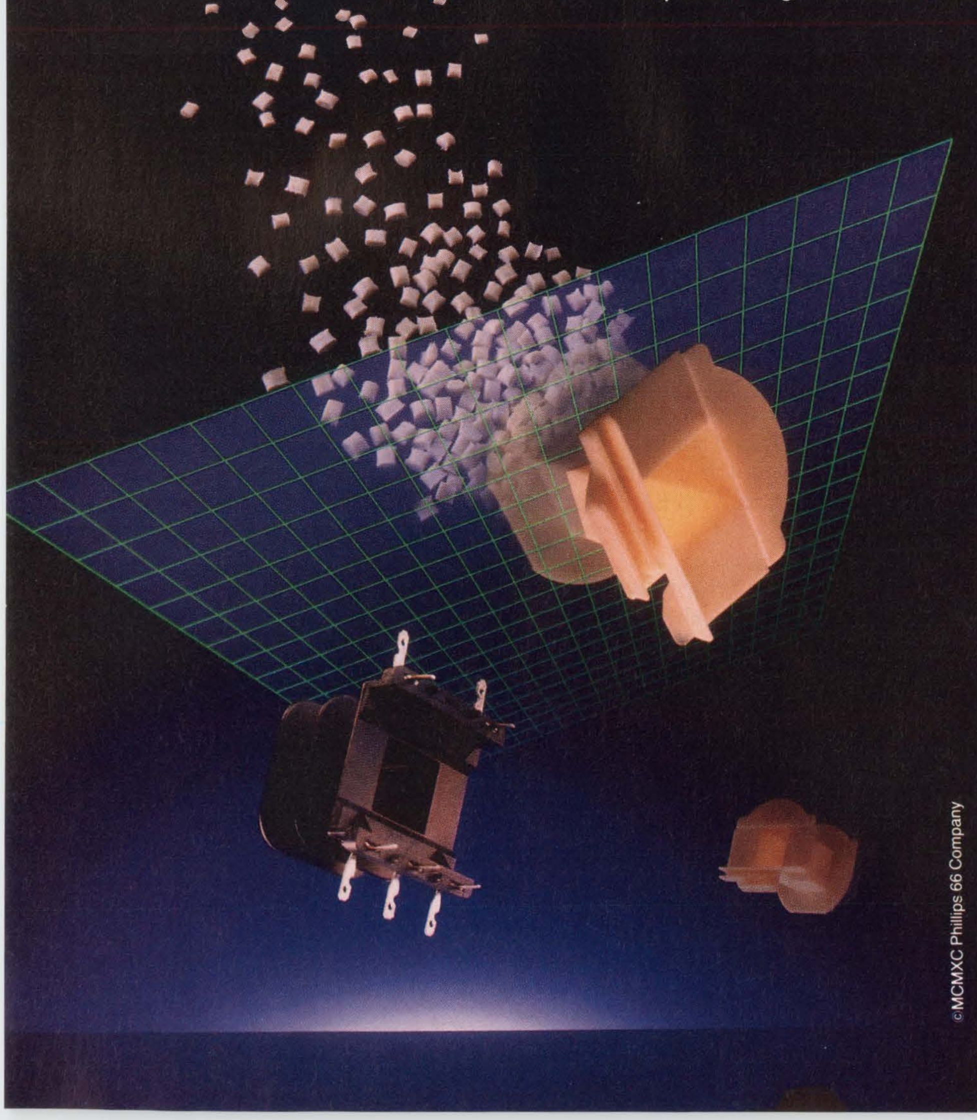
Insulated-gate bipolar transistors (IGBTs) can now move from motor control to center stage in large switching power supplies running at 50 kHz or higher thanks a new family of these transistors. "UltraFast" IGBTs from International Rectifier, El Segundo Calif., possess the lowest switching energy losses yet per unit of current density—an efficiency about 50% greater than that of existing IGBTs (ELECTRONIC DESIGN, *July 12, p. 36)*. These new power switches have delay-plus-turn-off times as low as 300 ns for a 600-V, 50-A device. IR suggests that these efficient power switches need an improved rating technique. To that end, they propose the concept of total switching energy losses, or E_{TS}. This measure of efficiency will be specified, in millijoules, for all of the UltraFast devices. The parameter is supported by three sets of device data: switching losses vs. gate resistance; switching losses vs. case temperature, and switching losses vs. collector current. With this data, designers can calculate total switching losses without worrying about actual voltage and current wave shapes, the tail current, or quasi-saturation. E_{TS} for new 600-V IGBTs with a saturation voltage of 3 V range from 0.5 mJ at 6.5 A for a size 2 die (the IRGBC20U rated at 13 A continuous) to 2.8 mJ at 27 A for a size 5 die (the IRGPC50U rated at 55 A continuous). In quantities of 1000, they go for $4.65 and $22.09 each, respectively. Call Howard Abramowitz, (213) 607-8900. *FG* **CIRCLE 392**

Upgrade Path For HC11 Widens CPU To 16 Bits

Extending the performance of an 8-bit microcontroller often leads to a non-compatible family of 16-bit processors. Not so with the popular 68HC11 series from Motorola Inc., Austin, Texas. The company has developed the 68HC16 family—a 16-bit series of microcontrollers that will be assembly-code-compatible with the 8-bit controllers, but offers six times the sustained throughput. Interrupt latencies have been cut to 3 μs—a six-fold improvement over the HC11 family. Furthermore, the processor core can address two separate 1-Mbyte memory spaces, one for instructions and one for data. The chip design is highly modularized. For customer-defined versions, it can take advantage of predefined functions that exist in the design library for the 68300 embedded-processor family. The first member of the family is the ROMless HC16Z1, which contains a 16-bit CPU core, a queued serial module (including two serial ports), a system integration module (bus interface controller), a timer block, 1 kbyte of RAM, and a 10-bit 8-channel ADC. Contact John Suchyta, (512) 891-2062. *DB* **CIRCLE 393**

Programmable Dot-Clock IC Simplifies PC Video

The SC11410 and 11411A digitally controlled clock synthesizers from Sierra Semiconductor Corp., San Jose, Calif., with outputs of up to 100 MHz, generate all of the dot-clock frequencies typically needed by a PC-compatible video graphics card. They can be programmed to deliver any one of eight predefined video-dot-clock frequencies from 25 through 65 MHz. The input timing source can be a standard 14.318-MHz crystal or host-system bus clock. A simple serial interface enables a host processor to program the timing generator for an output frequency from 4 to 100 MHz. In addition, any of the eight preprogrammed output frequencies can be mask-customized for different values. The 11411 differs from the 11410 in that it doesn't have the serial programming port and must be hard-wired to set the frequency. Proprietary circuits keep jitter on the generated frequency to less than 200 ps. The chips consume just 500 mW when run from 5 V. The SC11410 comes in either a 28-lead plastic leaded chip carrier or 20-pin DIP, while the 11411 comes in a small-outline 16-lead package. Both are available immediately and sell for $3.09 and $2.41, respectively, in 10,000-unit lots. Contact Zaheer Hassan, (408) 263-9300. *DB* **CIRCLE 394**



C++ Advancements Hasten Code Development

Three object-oriented programming (OOP) advancements for the HP 9000 and Apollo platforms support the latest version of C++ from AT&T. The three tools, from Hewlett-Packard Co.'s Computer Products Sector, Fort Collins, Colo., include the HP C++ 2.1 compiler on HP-UX, Domain/C++ 2.1, and the HP C++ Developer on Domain/OS. The "true" compiler generates object code directly from C++ source code and improves compile-time performance up to 75%. The Domain/C++ gives users advanced programming features, such as multiple inheritance, class libraries, and source-code debugging. Because HP C++ and Domain/C++ 2.1 are OOP languages, programmers can reuse code, reduce the complexity of an application development, and reduce code-maintenance costs. With the developer—a standalone X-window application tool—users can graphically browse through class definition and member function source code, add and modify classes and inheritance hierarchies, generate source-code templates, and diagnose and correct errors automatically. The compiler is priced at $1700, Domain/C++ starts at $1615, and the developer costs $2000, with discounts for large quantities. All three tools will be available in the first quarter of 1991. *RN* **CIRCLE 395**

80386SX Processor Turns Up In Notebook PC

The 80386SX microprocessor has finally appeared in a notebook PC: The LTE 386s/20 from Compaq Computer Corp., Houston, contains a 20-MHz processor, 4 kbytes of cache memory, 2 Mbytes of RAM (expandable to 10 Mbytes), a 3.5-in., 1.44-Mbyte floppy-disk drive, and a 30- or 60-Mbyte hard-disk drive. The PC's 9-in. VGA edge-lit monitor displays 16 shades of gray so that graphics software, such as Windows 3.0, can be run. The enhanced NiCd battery lasts more than three hours and recharges in 1-1/2 hours. The 7-1/2 lb. LTE 386s/20 can be plugged into Compaq's Desktop Expansion Base, which adds space for two mass-storage devices and two standard expansion boards. It also lets users easily connect an external monitor and keyboard, and can simultaneously recharge the PC's battery during operation. The 30-Mbyte PC sells for $6499, while the 60-Mbyte version costs $6999. The expansion unit goes for $1499. *RN* **CIRCLE 396**

Burst-Mode Controllers Ease CPU System Design

A pair of burst-mode memory controllers—one for the Intel Corp. i960 RISC-based embedded controller (including the CA), and the other for the Advanced Micro Devices Inc., Am29050 floating-point RISC processor—simplify the design of high-performance memory subsystems. The V96BMC from V3 Corp., Toronto, Ontario, Canada, manages single- or double-banked page-mode memory subsystems for the i960. Therefore, when burst accesses are allowed, data can be read or written at the rate of one word per clock cycle. Housed in a 132-lead plastic quad-sided flat package, the chip can control up to 128 Mbytes of memory directly, minimizing design complexity. The CMOS chip sells for $36 in quantities of 1000; units will be available next month. Housed in a similar package, the V29BMC manages burst and pipelined accesses to the memory subsystem of an Am29050. It enables the RISC processor to achieve zero-wait-state performance at full clock speed while using relatively slow DRAMs. The controller manages address spaces from 2 to 32 Mbytes. As with the V96BMC, up to four controllers can be cascaded to quadruple available memory space. In 1000-unit lots, the V29BMC sells for $55 (33-MHz version). Contact Mike Alford, (416) 266-5511. *DB* **CIRCLE 397**

Video RAMDAC Adds Complex Timing Logic

By adding programmable video timing and control logic to basic palette functions, a highly-integrated color-palette chip simplifies system design and reduces system cost. The single chip replaces up to 30 chips typically required in the video-control circuitry that usually surrounds the palette chip. The 34075 VIP chip from Texas Instruments can provide 24-bit true-color images with an 8-bit overlay. With its register-programmable features, the control circuits can implement various interfaces with 1, 2, 4, 8, or 32 bits per pixel. Screen resolutions ranging from VGA and below up to 1024-by-768 pixels with noninterlaced or interlaced monitors can be configured through software. That flexibility allows one board design to cover a wide range of price and performance points (resolutions and colors) by just changing the register values and adding more RAM. Though optimized to tie into the company's TMS34010 and 020 video controllers and video RAM chips, the integrated palette can easily tie into most other video controllers as well. Volume prices for the 66-MHz U.S. version of the chip will be under $20; the 75-MHz European version will go for under $30. Contact TI at (214) 995-6611, ext. 700. *DB* **CIRCLE 398**

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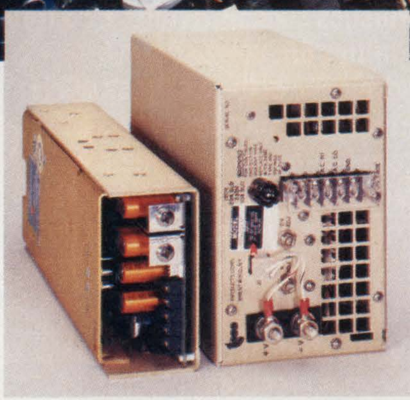

Designed for high-end computer products, TODD's MAX-750 combines a compact size, 13.5" x 5" x 2.6" compared to the typical 5" x 8" x 11" shoebox switcher (see photo insert), and very competitive pricing. OEM product designers can reduce product size with a MAX-750 or build in power supply redundancy, replacing one "shoebox" switcher with two MAX-750's in the same space.

The small package size, high power density of 4 watts/in., high peak current for motor starting, and cooling options, make the MAX-750 the power supply of choice for VMEbus systems, workstations, file servers and mini-computer systems. The switcher provides 120 amps of +5 volts for logic and memory, and features up to three auxiliary outputs providing high efficiency, tightly regulated 12 volts or −5.2 volts at up to 20 amps. Designed for world wide use, the series offers AC power fail, AC autoline select, and meets International Safety standards and Class A RFI requirements of FCC and VDE 0871.

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High Efficiency DC Converters Fit AC To DC Footprint

TODD's DC to DC converters provide up to 350 watts from 48 volts DC input. Designed as companion units to TODD's standard line of AC input power supplies, they are fit, form, and function compatible with the MAX-350, MTC-250, MTC-350, and certain single output SC series products.

Available in a 250 watt "DC" single output series and a 350 watt multi output "DCX" series these power supplies have up to 50 amp main output of tightly regulated 5V power, two fully regulated, high-efficiency, post-regulated mag-amp outputs and one low-power three-terminal regulated output.

CALL 1-800-223-TODD, OR CIRCLE #219

New Technology Shrinks 500 Watt Power Supply

TODD's MAX-500 switchers pack 25% more power into TODD's 400 watt package size (11.5" x 5" x 2.5"). The series incorporates a new SMT circuit, newly-available components, improvements to TODD's VERI-DRIVE current-fed inverter topology, monocoque construction, and a high efficiency FLUX-GATE switching mag-amp auxiliary post regulation. Result: higher performance, higher reliability (approaching 100,000 hours MTBF) and lower cost.

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Super Micro Supply Has a Cool 350 Watts

Targeting the computer-based OEM, TODD engineers developed the 9" x 5" x 2.5" MAX-350 series of competitively priced switching power supplies. Low component count, extensive use of SMT and raising efficiencies to 80% with attendant reduction of heat sink requirements results in MTBF approaching 100,000 hours.

The series features up to 50 amps of +5 volts for logic and memory and fully regulated high efficiency mag-amp outputs to power up to four disc drives. Auxiliary outputs power common peripherals like ECL monitors, RS232 outputs, communications drivers, etc.

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Arcnet Chip Tackles Real-Time Embedded Control

Teamed Up With A Microcontroller, An IC Cuts Cost For Peer-To-Peer Networking Over Arcnet.

Milt Leonard

With a 2.5-Mbit/s data rate, support of up to 255 network nodes, and data packet sizes of up to 512 bytes, the Arcnet local area network (LAN) is a popular solution for networking PCs in office-automation applications. However, Arcnet has seen limited use in embedded-control applications, such as factory automation and process control. That's because the controller usually requires external buffer memory and up to a dozen support chips for a typical network node, resulting in relatively high cost. Standard Microsystems Corp. now incorporates the Arcnet token-passing protocol in a 24-pin package that reduces node chip count by one-fifth. The result is half the node cost of competitive approaches.

To implement the Arcnet protocol, SMC's COM20020 universal LAN controller includes a microsequencer, a 2-kword-by-8-bit dual-port buffer RAM, an assortment of registers, bus-arbitration circuitry, a generic microcontroller interface, a flexible media interface, and a transceiver *(see the figure)*. Network nodes can be configured in star, bus, or tree topologies connected with twisted-pair, coaxial, or fiber-optic cable.

Controller Operation

In operation, the 20020's companion microcontroller or other intelligent peripheral device sends data over the network by loading a data packet and a destination identification (ID) number into the 20020's RAM buffer. It then enables the transmitter. When the controller receives the token, it verifies that the receiving node is ready to receive and then transmits the data packet. The packet is followed by a 16-bit cyclical redundancy check. When the packet is received successfully, the receiving node transmits an Acknowledge message. This allows the source node to set status bits, which trigger an interrupt to its host microcontroller, indicating a successful packet transmission. If the receiving node can't accept the packet (when its receiver is inhibited, for example), it issues a Negative Acknowledge signal. Thereupon, the source transmitter passes on the token.

For boosted network performance, the 20020's command-chaining mode makes it possible for successive data transmissions and/or receptions without intervention by the microcontroller. In this mode, a dual two-level first-in first-out buffer pipelines transmit and receive commands and status bits, thereby enabling new packets to be received before the previous packet interrupt is acknowledged and serviced. Command-chaining prevents wasting tokens on the network by guaranteeing that a buffer is always available to receive a data packet.

Several unique features eliminate the need for multiple support chips. For example, the 20020 adapts to network changes by incorporating Arcnet's automatic self-reconfiguration protocol. Whenever the controller senses that a new node is activated or deactivated, it sends a signal that terminates all activity on the network. It then reconfigures the network by adjusting the destination-node ID numbers stored in internal registers. Network reconfiguration time, which typically ranges between 24 to 61 ms, depends on such factors as the number of nodes on the network, the propagation delay between nodes, and the highest ID number on the network.

Users can set the destination ID number so that the controller transmits a data packet simultaneously to all nodes on the network. Similarly, with the appropriate setting of the command register, each node can ignore broadcast messages.

On-Chip Memory Benefits

One of the most significant features of the 20020 is the 40-ns, dual-port RAM. Previous LAN controllers used external buffer memory that requires multiplexed address/data buses and control interfaces, plus support devices, such as latches and other glue logic. The 20020's integrated RAM reduces the chip's package size by 50% and eliminates costly support logic.

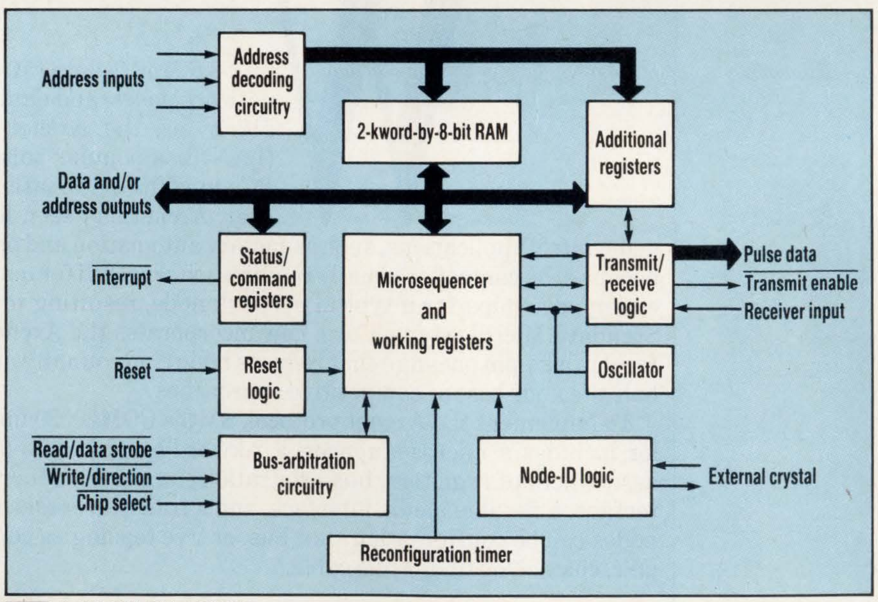
During typical operation, the RAM is partitioned as four 512-byte pages—two to transmit and two to receive. This leaves up to four memory pages for scratch-pad storage. For most control applications that use smaller packet sizes, the memory can be partitioned as any combination of 256-byte and 512-byte pages.

The 20020 interfaces directly with popular microcontrollers from Intel, Motorola, NEC, and Zilog. The interface consists of an 8-bit data bus, an address bus, and a control bus. To support various microcontrollers with a minimum number of pins and without the use of glue logic, the 20020 detects and adapts to the microcontroller interface being used automatically.

Upon hardware reset, the chip first determines if the microcontroller has separate Read and Write signals (as in Intel's 80XX family), or a Direction and Data Strobe (as in Motorola's 60XX family). The controller also determines whether the microcontroller bus is multiplexed or nonmultiplexed. Both determinations require software to access external memory. In each case, the 20020 remains in the selected mode until the next hardware reset occurs.

The chip also has a flexible transmission-media interface. A standard Arcnet transceiver interface is offered for applications requiring long transmission distances, or for networks with other nodes that also use a transceiver interface. In this arrangement, a device such as SMC's HYC9068 hybrid transceiver transfers pulse-code data between twisted-pair or coaxial cable and the 20020. Containing support logic and coupling for good isolation and common-mode rejection, the hybrid device converts the 20020's pulse waveform output to sinusoidal form. It also supplies the appropriate termination impedance for a star topology, bus topology, or an Arcnet topology, using twisted-pair cable.

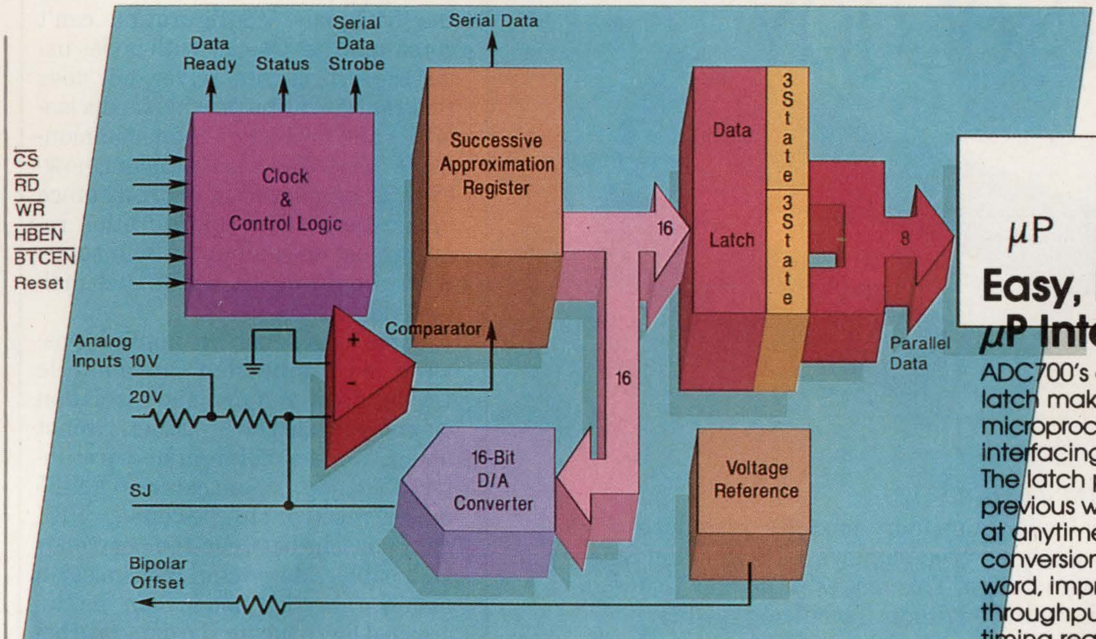
For cost-sensitive, short-distance



A KEY PLAYER in the COM20020's architecture is the 2-kword-by-8-bit RAM. Its dual ports and 40-ns access time enables the 20020 and companion microcontroller to arbitrate for, and access, the memory in one clock cycle without using wait states and without impacting the network data rate. Because most microcontrollers have no Ready line, previous LAN controllers handling arbitration and microcontroller address decoding could not extend the microcontroller's read/write cycle. This requires the microcontroller to operate at a much slower speed.

INTRODUCING ADC700

New 16-Bit ADC with Direct μP Interface



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ADC700's output buffer latch makes microprocessor interfacing fast and easy. The latch permits the previous word to be read at anytime during conversion of the next word, improving throughput and relaxing timing requirements on software interrupts.

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ADC700 excels in low, low noise so you can squeeze out greater resolution. A wide choice of input and temperature ranges increases your design flexibility.

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- No missing codes to 14 bits over temp
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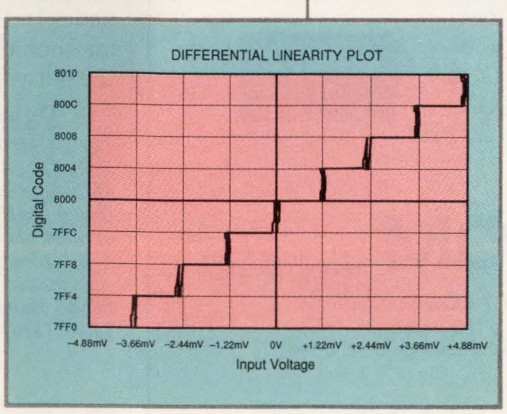


BURR-BROWN®

CIRCLE 174

ARCNET CONTROLLER CHIP

applications, such as backplanes and instrumentation, a Backplane mode connects the controller directly to the media to transmit straight non-return to zero (NRZ) data rather than pulse-coded data. Nodes with the backplane configuration can't communicate directly with nodes using the hybrid transceiver, nor does this configuration provide media isolation and protection from common-mode noise. The noise problem, however, is minimized in short-distance applications. This configuration requires just one pull-up resistor somewhere on the media, not on each individual node.

Some cost-sensitive applications, such as embedded automobile LANs, don't require node isolation or compatibility with other Arcnet nodes. Here, a differential-driver interface mode uses an external RS485 driver/receiver to dc-couple NRZ data passing between the controller and cable. Maximum transmission distance in this mode can be increased by reducing the data rate below 2.5 Mbits/s.

Bits in the on-chip diagnostics status register help prevent and isolate faults, and support network management. Before entering the network, the 20020 first checks a register bit to see if there's activity on the network. Another bit tells the controller if a token is circulating on the network. A duplicate ID bit indicates when another network node has the same ID number as the entering node. In this case, the 20020 selects another ID number before entering the network.□

PRICE AND AVAILABILTY

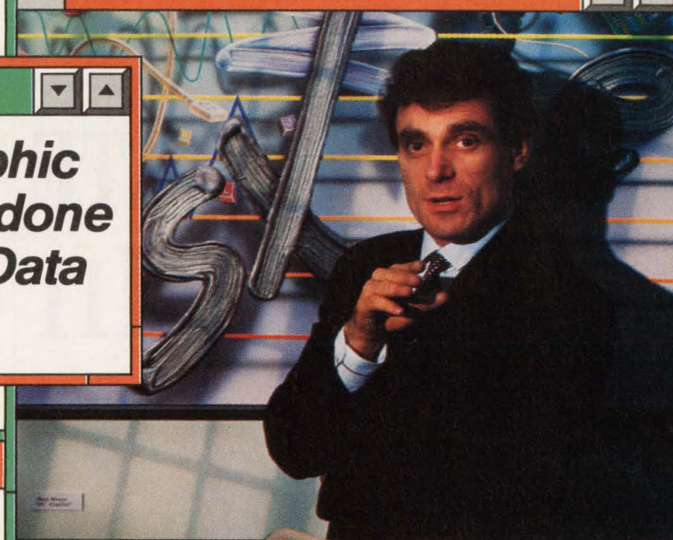
The COM20020 universal LAN controller costs $16.23 in 1000-piece lots and is available now in sample quantities. Production quantities are scheduled for January of next year. Evaluation boards will be available in December 1990.

Standard Microsystems Corp., 35 Marcus Blvd., Hauppauge, NY 11788; Ralph Malboeuf, (516) 273-3100.

CIRCLE 516

HOW VALUABLE?	CIRCLE
HIGHLY	547
MODERATELY	548
SLIGHTLY	549

"I was looking for a graphic example of what could be done with a laptop PC... Zenith Data Systems showed me two."



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CIRCLE 3

GaAs Gate Arrays Hit 100,000+ Gates/Chip

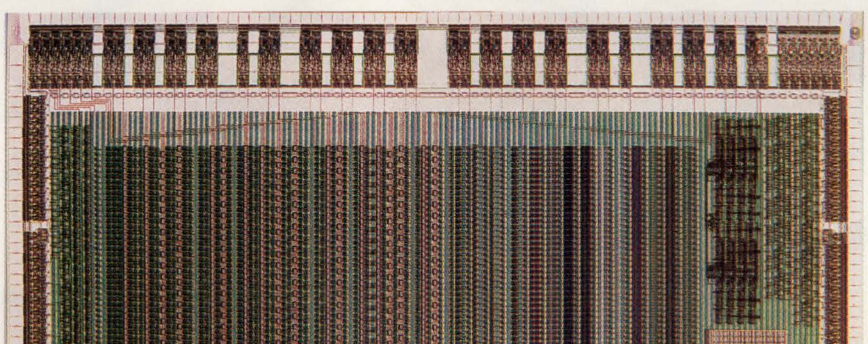
High-Performance System Design Just Got Easier With A Family Of GaAs Gate Arrays That Hold More Of The Complex Circuit On One Chip.

Dave Bursky

High-performance-system designers often rule out using gallium-arsenide gate arrays because the chips didn't have the desired density, or were too expensive. However, as the integration level of GaAs chips increases while the per-gate price drops, and the cost of high-performance biCMOS or ECL and their associated cooling requirements increases, GaAs arrays become an attractive alternative to power-hungry biCMOS or ECL.

The latest GaAs offering—a family of gate arrays with complexities of 100,000 usable gates—now puts GaAs arrays on par with biCMOS and ECL for complexity and speed, while cutting the power consumption by one-half to one-third over that of ECL *(see the figure)*. The FX series of arrays from Vitesse Semiconductor will offer gates that deliver two to three times the performance of biCMOS, which is competitive with ECL, with comparable pricing. The 100,000+ complexities of the larger family members will be the largest GaAs gate arrays manufactured by any company around the world.

The availability of such large GaAs gate arrays opens up new systems possibilities because more of the increasingly complex system logic can now be integrated on one chip. Such integration eliminates many performance-diminishing signal delays associated with multichip solutions. This enables higher-performance sys-



THE JUST-RELEASED FX FAMILY **of gate arrays from Vitesse offers nearly a seven-fold density improvement over the company's previously released Fury family. The FX-100K holds over 100,000 gates and has an expected gate utilization between 50 and 70%.**

Make your move to P&B for new general purpose and power P.C. board relays.

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Extensions to our line of RK series relays feature 8mm coil-to-contact spacing for 4,000V isolation. SPDT models switch loads to 20A, and DPDT models switch up to 5A. Both sealed and unsealed types are offered.

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Relays in our T90/T91 series have SPDT contacts for loads to 30A. T90 is available as a sealed or open-style relay. T91 has quick connect terminals for load connections and is offered with either a sealed or unsealed enclosure. High temperature units are available.

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tems to be built, even if they don't operate at higher clock frequencies. And the availability of many gates allows large register files and memory blocks to be included on the logic chip, improving system speed even further. This is because memory accesses don't have the long delays of off-chip memories.

To make the jump from its previous Fury family, which had a 30,000-gate chip as its largest member, Vitesse developed an improved finer-line process, H-GaAs III. Gate lengths for the GaAs MESFETs are trimmed to 0.6 μm—that's about a 25% reduction over the previous process. The three levels of metal interconnections and line-to-line spaces were scaled by close to 40%, so that on the lowest level, 1.2-μm metal lines are separated by 1.8-μm spaces. Furthermore, a fourth level of metal interconnection is available, making the FX arrays more routable than any of the company's previous chips.

In addition to shrinking the basic feature sizes, the company revised its basic cell building block. As a result, close to seven gates can now be squeezed into the area originally occupied by one gate in its previous family. The overall net result of the changes yields gates that consume about 50% of the power required by the previous generation—0.16 mW vs. 0.32 mW. Also, propagation delays are less than 70% that of the previous family—46 vs. 65 ps for an unloaded 2-input NOR, and 153 vs. 216 ps for a buffered 2-input NOR gate with a fan-out of 3.

In a typical application, a chip with 100,000 active gates would consume about 14 W, which is considerably less than what an equivalent ECL circuit would require. The lower power level also translates into a simpler cooling requirement. For example, forced air rather than liquid cooling could result in a significant system overhead savings.

Two FX family members have been defined by Vitesse, one packing 100,000 cells, and the second 200,000. A third array with about 300,000 cells will probably be defined in four to six months. Gate utilization for the channelless arrays is estimated at between 50 to 70%.

The first two arrays will have 196 and 256 signal I/O pads, respectively. They come in packages with plenty of power and ground lines—211 or 256 pins for the 100,000-gate chip, and 344 pins for the 200-k circuit. Maximum and typical power consumption for each chip are estimated at 15 and 8 W for the smaller chip and 25 and 14 W for the larger one.

In addition to logic cells, the FX series will eventually have family members with embedded blocks of up to 128 kbits of static RAM. A 72-kbit block of RAM would occupy about 60% of the logic core area of the 100,000-gate chip, which still leaves 40,000 raw gates for the designer to use. On the FX-200K array, the RAM needs just 30% of the chip; 140,000 gates remain available for other logic. Access time for the embedded blocks of RAM is about 3 ns.

The design library developed for the Fury family has been redefined for the advanced process used in the FX family. Consequently, designers that have already created a circuit with the previous family can move that design into the higher-density array. Then, perhaps, they can merge the circuitry with yet another function to improve system integration. For new designs, the FX library can be installed on a number of workstations, which behaves just like any other macrocell library. □

PRICE AND AVAILABILTY

The macrocell library for the FX family of gate arrays is immediately available for designers wishing to capture a design. Delivery of engineering samples from approved net-list submittal is 6 to 10 weeks, with production quantities available in the first quarter of 1991. Array prices vary depending on the package and complexity, but packaged chips will typically sell for between 0.5 to 1.25 cents per used gate. Non-recurring engineering charges (including 5 prototype chips) typically range from $125,000 to $175,000, assuming Vitesse does the placement and routing. □

Vitesse Semiconductor Corp., 741 Calle Plano, Camarillo, CA 93010; Robert Nunn, (805) 388-3700. CIRCLE 512

HOW VALUABLE?	CIRCLE
HIGHLY	527
MODERATELY	528
SLIGHTLY	529

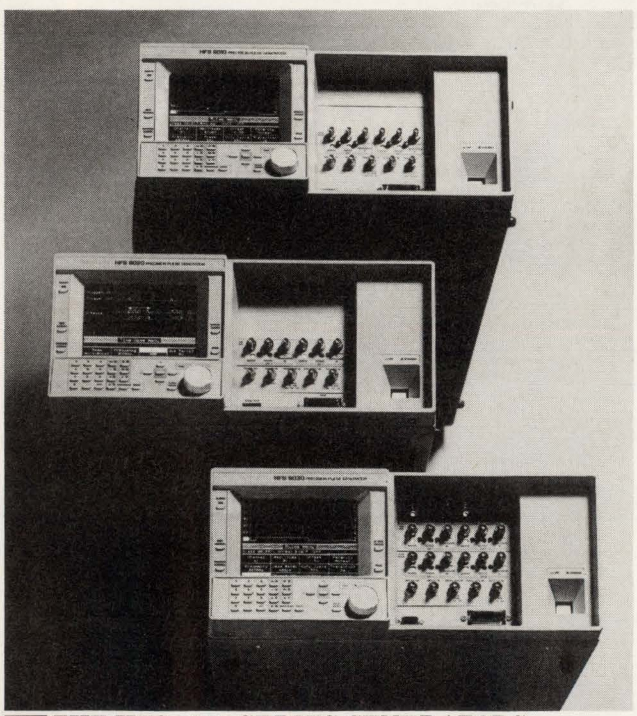
PULSE GENERATORS SPORT HIGH ACCURACY

THREE MODELS AIM AT DEVICE CHARACTERIZATION.

JOHN NOVELLINO

Characterizing today's high-performance ICs accurately is a tough job—checking ones and zeros with a pattern generator may not be enough. With devices running at 33 MHz and above, such critical timing parameters as setup and hold times, f_{max}, and propagation delay must also be measured in order to evaluate devices properly. Therefore, designers need an accurate, programmable, multichannel stimulus.

Moving in to fill this void is the Tektronix HFS 9000 series precision pulse generators. The modular instruments offer repetition rates to 600 MHz, pulse widths down to 400 ps, and the ability to compensate for external cable skews. Four channels are standard and six are optional, with each edge able to be specified independently. The rms jitter is a low 15 ps ±0.05%. The generators owe their excellent accuracy to a new totally digital pulse-synthesis architecture that replaces older monostable-based techniques.



THE HFS 9000 SERIES GENERATORS feature a modular architecture that permits from two to six channels in one mainframe. An electroluminescent display shows a graphic representation of the output as well as the numeric parameters.

The three models that make up the HFS 9000 series supply pulse outputs for various logic families *(see the figure)*. The HFS 9010—aimed at ECL, GaAs, and other high-speed devices—delivers a maximum repetition rate of 600 MHz and a fixed transition time of less than 200 ps. For its targeted TTL and CMOS devices, the HFS 9020 has a maximum repetition rate of 300 MHz, programmable transition times down to less than 1 ns, and outputs of -2 to +5.5 V. The HFS 9030 combines the features of both other units. Edge placement resolution is 10 ps for all three models.

Users can program the location of rising and falling edges, delay, width, and duty factor. Output levels can be individually set. Each channel supplies both true and complement outputs that can be either active high or active low. A push-button control makes it possible for the operator to disable the outputs.

A particularly useful feature is the pulse-rate off command, which holds a pin at a fixed voltage level. That pin's output can be held at the programmed low level while other channels execute a programmed burst of pulses. For instance, users can hold a flip-flop's reset pin low while the test setup characterizes clock-to-output propagation delay. Then the pin can be actively clocked while the tester characterizes reset-to-output propagation delay.

To simulate data for flip-flop setup and hold-time measurements, users can select the pulse-rate half command. This feature sets a channel to one-half the operat-

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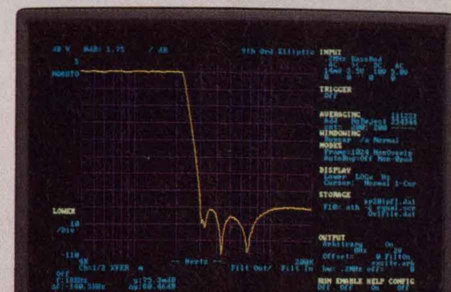

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CIRCLE 134

PULSE GENERATORS

ing frequency of the main cycle, while still allowing independent placement of the rising and falling edges. The odd cycles then safely clock the flip-flop to a low state as the even cycles stress setup and hold-time requirements by clocking the device high.

The HFS 9000 series increases trigger flexibility by allowing a Trigger Out signal to occur on any period in the burst of pulses. This capability improves accuracy in tests of devices where the internal state changes on input clock signals. In cases like these, the device's output signals of interest may occur late in a burst of activity.

With a conventional monostable-based pulse generator, the oscilloscope used in the test setup must trigger off the generator's Trigger In signal. Then the scope's main position must be adjusted to the needed delay, which could be 255 periods if the user looks at rollover in an 8-bit synchronous counter. Because of jitter in the generator, this delay could hurt the measurement's accuracy. But by using the HFS 9000's Trigger Out signal, the scope can be triggered on the desired cycle, and no delay is needed.

The HFS 9000's electroluminescent display offers an intuitive graphic interface for easy setup. Users can look at a graphic representation of the output, as well as the complete timing setup of the output parameters. A keypad speeds entry of numeric parameters, and a knob allows fast, high-resolution adjustments. Users can program the generators through an RS-232 port or over the GPIB using the expanded GPIB standard (IEEE-488.2).□

PRICE AND AVAILABILTY

The HFS 9010 and HFS 9030 cost $37,500; the HFS 9020 goes for $36,500. The standard configuration is four channels with options for six or two channels. Delivery is 12 weeks from receipt of an order.

Tektronix Inc., P.O. Box 19638, Portland, OR 97219-0638; (800) 426-2200. CIRCLE 511

HOW VALUABLE?	CIRCLE
HIGHLY	524
MODERATELY	525
SLIGHTLY	526

SIMPLIFY CONVERTER CONNECTION TO DSPS

LINK DIGITAL SIGNAL PROCESSORS TO DACS AND ADCS WITHOUT GLUE LOGIC.

FRANK GOODENOUGH

To link a typical 16-bit analog-to-digital converter (ADC) or digital-to-analog converter (DAC) to an IC digital signal processor (DSP), usually between 11 and 35 digital ICs are required for glue logic, depending on the flexibility required. As a result, designers haven't been able to cost-effectively use available low-cost DSP ICs to process real-world analog signals digitally. Burr-Brown has made that connection easier and more practical with four high-performance converters in 28-pin plastic DIPs—the DSP101, DSP102, DSP201l, and DSP202. The first pair are single and dual 18-bit sampling, successive-approximation ADCs, respectively. Their mates, the DSP201 and DSP202, are single and dual, voltage-output, 18-bit DACs.

The four converters connect directly with all of the common DSP ICs, whether they're from Analog Devices, AT&T, Motorola, or Texas Instruments, over a serial link, without a single glue-logic chip *(see the figure)*. Just three wires are required between the DSP IC and the ADC or DAC. The ADCs offer a minimum throughput rate of 200 kHz; the DACs update data at up to 500 kHz. The dual DAC accepts data words at two separate ports. While in the cascade mode, both channels are updated with a 32-bit word at one port.

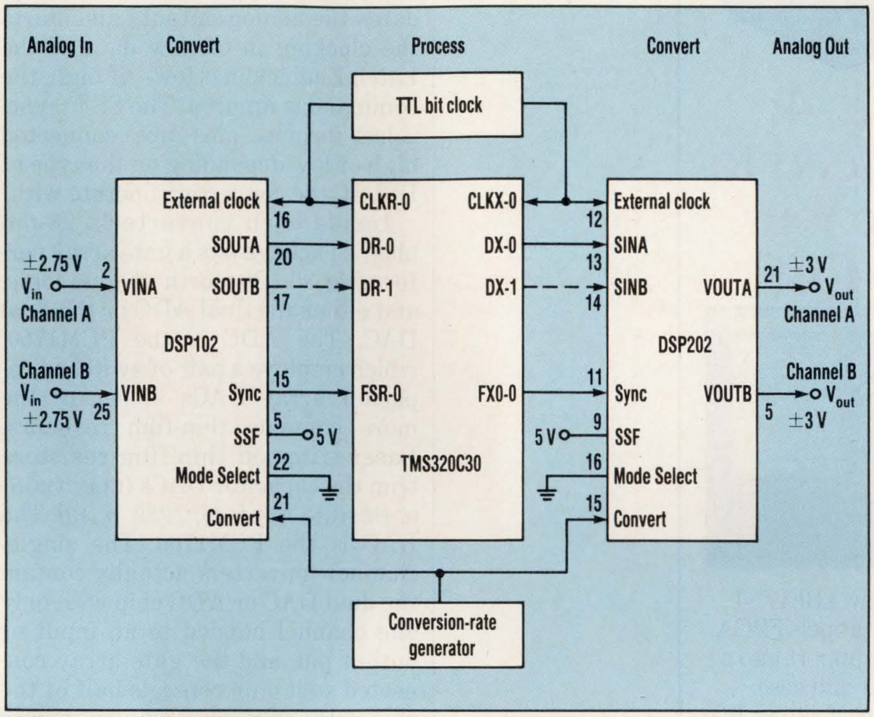
The converters are based on Burr-Brown's dual, digital-audio chips and were the result of a team approch *(see "Design team cuts time-to-market," p. 161)*. Their dc and dynamic specifications aim toward typical DSP applications. While they have 18-bit resolution and dynamic range, their accuracy runs from 13 to 15 bits. That's more than enough for most DSP or general-purpose data-acquisition applications. Moreover, virtually any DSP can improve a signal's signal-to-noise ratio by simple averaging.

The DSP102 essentially gives you two 14-bit-accurate ADCs that sample at high speed for just $30. It's suitable for applications ranging from souped-up, low-cost, 14-bit analog I/O boards for PCs and other buses to sophisticated vibration-analysis systems (if only need one ADC per system is required, the cost per converter goes to $24). Other applications include audio analyzers, process-control and weighing systems, and noise cancellation.

The DACs should find their way into various signal sources from arbitrary-waveform generators and frequency synthesizers to test equipment and electronic musical instruments—anyone of which could wind up as, or on, a plug-in board for a PC. With a DAC or ADC, it's easy and inexpensive enough to add one or more shift/storage registers if a parallel interface is preferred.

The ADCs sample and convert ± 2.75-V input signals in under 2.5 μs maximum, resulting in the minimum throughput rate of 200 kHz. They offer 14-bit

DSP-IC INTERFACE ADCS AND DACS



REAL-WORLD SIGNALS can be processed by feeding them to a DSP102 for analog-to-digital conversion, and then passing their serial digital output words to a DSP IC, such as the TMS320C30, for analysis and processing. To regain the analog signals after processing, apply the DSP IC's serial output to a DSP202 DAC.

no-missing-code conversions. Integral and differential nonlinearities (INL and DNL) run under ±0.003% (15 bits); aperture jitter is 300 ps (rms). All specifications are from 0 to 70°C for every device, and accuracy specifications are typical.

While sampling 1-kHz sine-waves at 160 kHz, signal-to-(noise + distortion), or S/(N + D), runs 90 dB (14.7 bits) for the premium K-grade ADCs, and 86 dB (14 bits) for the J-grade units. When sampling at 25 kHz, S/(N + D) runs 82 dB (13.3 bits) for both. Total harmonic distortion (THD) is –92 dB (15 bits), and spurious-free dynamic range is 94 dB (15.3 bits). Full-scale gain error runs a maximum of 5%, and gain mismatch between the two channels of the DSP102 is just 1%. Both use 400 mW maximum from ±5-V rails.

The DACs' throughput, or update rate, is a minimum of 500 kHz. Their output op amps can typically put ±3 V across 375 Ω. INL and DNL errors run ±0.004% for the premium K-grade DACs, and 0.006% for the J-grade DACs. While putting out 1 kHz, S/(N + D) for the K-grade devices is a minimum of 88 dB (14.3 bits) and 82 dB (13.3 bits) for the J-grade parts. At 10 kHz, these figures drop to minimums of 86 dB (14 bits) and 80 dB (13 bits), respectively. Maximum THD runs –88 dB (14.3 bits) and –92 dB (15 bits) for the J and K grades, respectively. Gain error and gain-error mismatch for the dual unit are a maximum of 3%. Channel separation on the dual DAC runs 105 dB from 1 to 100 kHz. Both DACs need 450 mW maximum from ±5-V rails.

INS AND OUTS

In the cascade mode, a TI TMS320C30 DSP IC, with a DSP102 handling its inputs and a DSP202 managing its outputs, represents a typical application for these converters *(see the figure, again)*. Just three lines carry serial ADC output words or DAC input-update words, clock, and synchronization signals between each dual converter and the DSP IC. The first 16 bits of the 32-bit serial word carries the 16 most-significant bits of channel A; the second 16 bits carry those of channel B. To operate in the normal mode, the SOUTB pin of the ADC is connected to the DR 1 pin of the TMS320C30 (shown dotted), and the CASC pin of the converter is connected to 5 V instead of ground. In the normal mode, both serial words are transmitted simultaneously over the two lines.

Analog-to-digital conversion starts on the falling edge of the Conversion Rate Generator (the convert command), which switches the ADCs sampling circuits into Hold, starts the successive-approximation register (SAR) running, and transmits the last conversion's results to the DSP IC along with a pulse from the Sync output. The bit clock drives the SAR and the serial data transmission. The falling edge of the convert com-

DESIGN TEAM CUTS TIME-TO-MARKET

To get the DSP converters to market quickly, Burr-Brown went to the team approach of two IC designers, a test engineer, and a marketing engineer/project manager. The team met weekly for a year, calling in processing, production, purchasing, and other required personnel. The swift meetings concentrated on what was needed to get to the next milestone, allowing resources to be reallocated to reach them.

Personal interaction among the team members yielded better and more manufacturable products. This process was started by encouraging design, test, and manufacturing inputs during the final revisions of product proposals from marketing. It continued through design, test development, characterization, prototype production, and qualification. Each member was encouraged (and expected) to ask questions, make suggestions, and offer alternatives throughout the process. Eventually, the team approach cut the time-to-market by 6 to 9 months.

DSP-IC INTERFACE ADCS AND DACS

mand, when applied to the DAC, updates the analog outputs and starts the clocking in of new data, if the Latch Enable pin is low—if high, the command is ignored. The SSF (sync-select-format) pins are connected high or low depending on the type of DSP IC the converters operate with.

Inside each converter's 28-pin plastic package sits a gate array performing 35 ICs worth of glue logic, and either the dual ADC or the dual DAC. The ADC is the PCM1750, which employs a pair of switched-capacitor array DACs in lieu of the more common thin-film resistors. Laser-trimmed thin-film resistors trim the capacitor DACs (ELECTRONIC DESIGN, *Sept. 14, 1989, p. 49)*. The DAC is the PCM1700. The single-channel converters actually contain the dual DAC or ADC chip with only one channel bonded to an input or output pin, and the gate array connected so it only controls half of the chip (this explains similar power drains for single and dual converters). Single-channel converters cost less, but have the same silicon.

If typical specifications are an anathema, but a need for these converters is perceived, they still may be worthwhile to try. Over the next six to twelve months, Burr-Brown will be recording the actual ac and dc specifications of large numbers of both ADC and DAC die to get true production characterization. When reliable yield figures to improve performance are obtained, premium-grade units will be given up-graded and guaranteed specifications.□

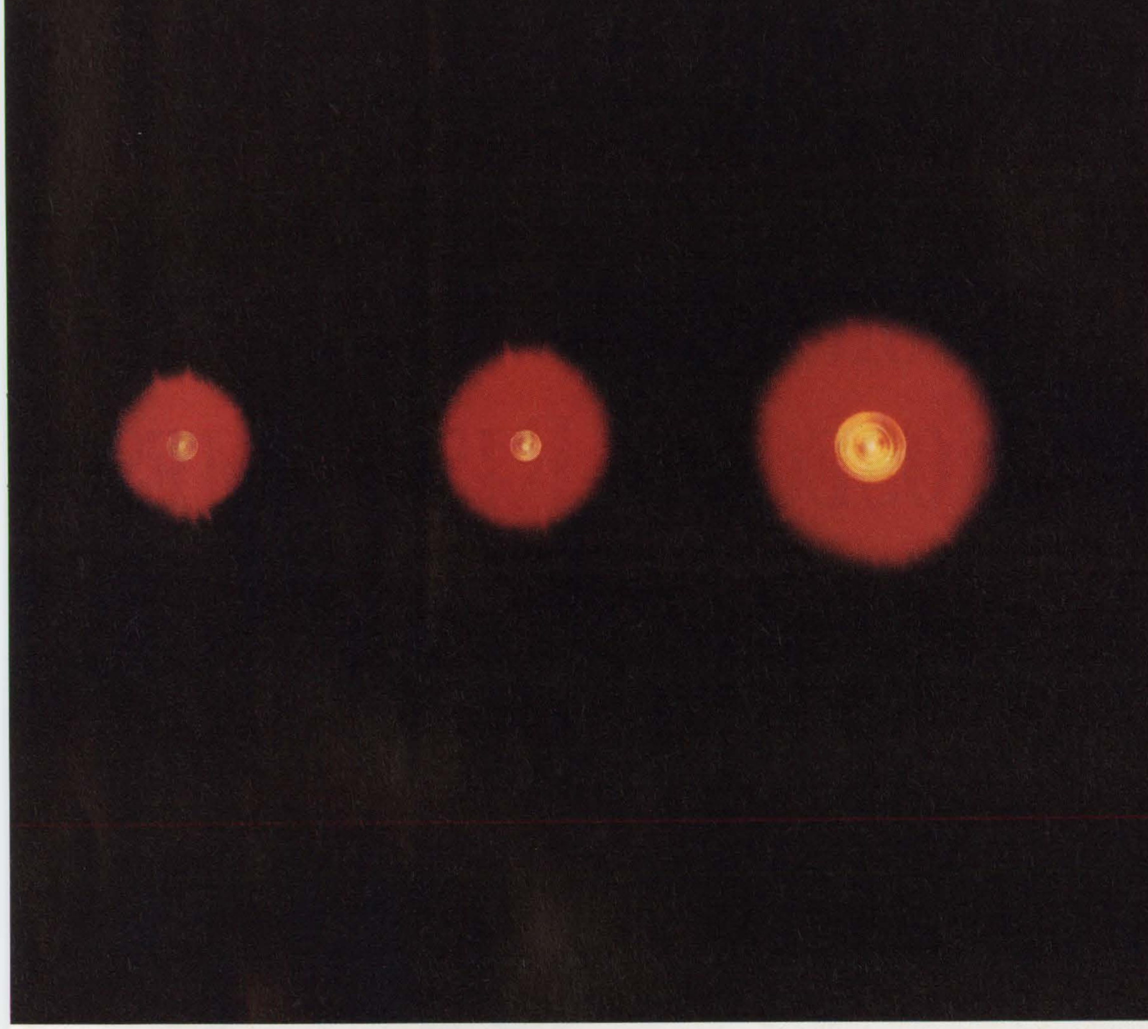
PRICE AND AVAILABILTY

In quantities of 1000, unit pricing for the 18-bit ADCs starts at $23.95 for the single-channel DSP101, and $29.95 for the dual-channel DSP102. In similar quantities, the single-channel DSP201 DAC goes for $19.95, and the dual-channel DSP202 for $24.95. The DACs are available now; the ADCs will be available by year's end.

Burr-Brown Corp., P.O. Box, 11400, Tucson, AZ 85734; John Conlon, 1-(800) 548-6132. Also contact the Burr-Brown bulletin board at (602) 741-3978. **CIRCLE 513**

HOW VALUABLE?	CIRCLE
HIGHLY	531
MODERATELY	532
SLIGHTLY	533

BRIGHT, **BRIGHTER AND BRIGHTEST**



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BY ACTING LIKE A DIGITAL TRANSMISSION LINE, A CONNECTOR ELIMINATES THE NOISE ROADBLOCK TO HIGHER SYSTEM THROUGHPUT.

CONNECTORS PASS PULSES WITH NANOSECOND RISE TIMES

DAVID MALINIAK

Up to now, board-to-board and cable-to-board connectors have represented a digital roadblock to realizing the dream machines of system designers. No matter how fast they could get signals to zip around a board, there would be a connector representing an impedance discontinuity at its output. This slowed the signals down to disappointingly ordinary speeds. The connectors would degrade the fast digital pulses, rounding edges and generating noise. In contrast, AMP Inc.'s Micro-Strip connector system acts as a high-speed digital transmission line, passing digital pulses with sub-nanosecond rise times with minimal noise and distortion. And the connectors offer high density—40 signal contacts per linear inch.

To gain speed and performance, system designers often adapt conventional connectors by committing up to 50% of the signal pins to ground. That practice consumes board real estate and chews up connector costs. The Micro-Strip connectors control transmission characteristics by adjusting dimension, spacing, and dielectric properties, rather than by sacrificing signal pins.

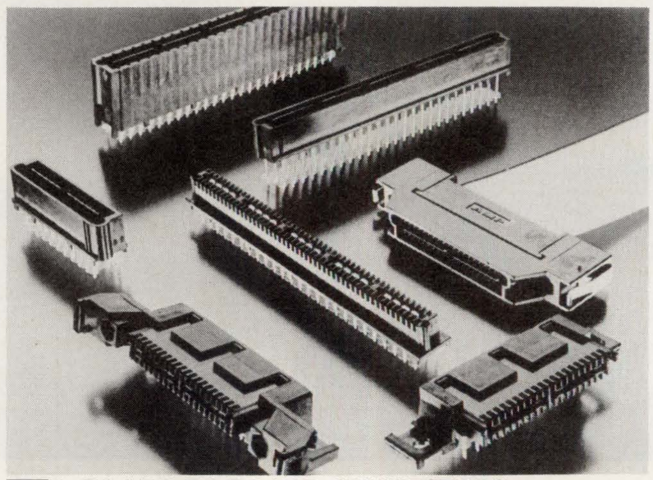
The receptacle contact design presents a uniform flat metal surface that faces the ground plane. This surface provides a controlled-impedance transmission path, when properly spaced from the ground plane, to help control transmission.

By maintaining a 50-Ω (±10%) interconnection impedance, the Micro-Strip connectors minimize impedance discontinuities. Crosstalk is limited to less than 4% at 1-ns rise times (measured as active-quiet-active). Because every pin can carry a signal, the effective density is greater than that of conventional connectors.

Because of their high transmission performance, the connectors will benefit designers of supercomputers, superminicomputers, minicomputers, workstations, high-end desktops, and high-end memory modules. Circuit runs can be longer with less related ground noise.

Moreover, all members of the product family have the same signal-and-ground bus-contact systems. That means users who test and qualify one connector style can use all of the connectors in the family.

All three connector styles in the family—vertical stacking, right-angle board-to-board, and cable-to-board—are similar in design *(Fig. 1)*.



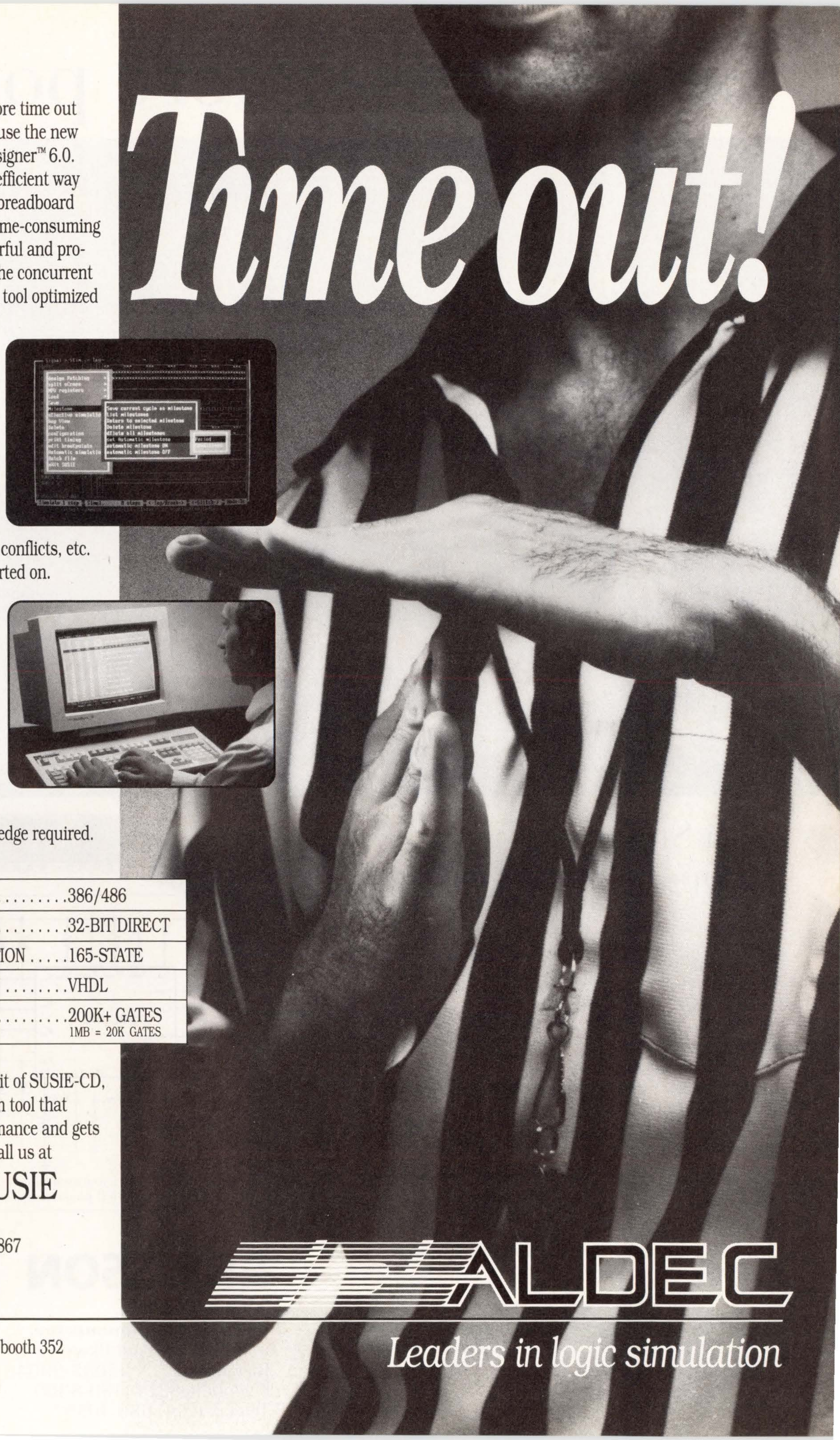
1. BOARD-TO-BOARD CONNECTORS in vertical and right-angle configurations, as well as cable-to-board styles, are offered in AMP Inc.'s Micro-Strip connector family.

The standard Micro-Strip package connects to boards with a staggered five-row grid footprint. The footprint contains 40 signal pins and two ground-bus segments per linear inch. Two staggered rows of signal contacts are located on each side of a separable ground bus situated along the centerline of each connector.

The mating connector sections consist of two rows of signal contacts. The rows are spaced 0.1-in. apart and are bisected by the ground bus. Spacing between contacts in each row is 0.05 in. When the plug and receptacle mate, the ground connection is carried from one pc board to the other by the metal ground bus.

Ground-bus segments, each about 0.5-in. long, are designed in increments of 20 pins each. This enables users to tailor the connector configu-

Time out!



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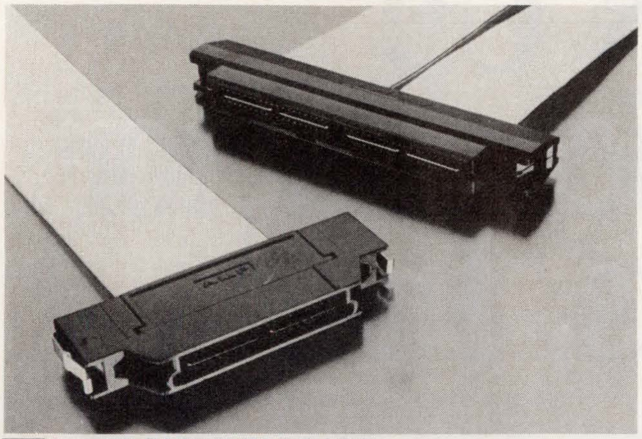
CIRCLE 101

HIGH-SPEED CONNECTOR SYSTEM



2. FOR CABLE-TO-BOARD applications, a newly designed ribbon cable is mass terminated to the cable connector using a precision-controlled technique.

ration for each specific application. In applications where transmission control is required in the complete connector, individual ground-bus segments are commoned by the pc-board ground.

The vertical stacking connectors ease parallel board-to-board mounting. Two stacking heights are available: 0.430 and 0.738 in. The vertical receptacle in each is the same; only the plug height changes to create two different board spacings. The plug half of the vertical-stacking connector has signal contacts ending in a 0.015-in. square post to mate with the corresponding receptacle contact. When the connectors mate, the ground bus engages first, completing the ground circuit before the signal contacts mate. On the board side, barriers prevent solder from bridging between pins. The vertical-stacking connector comes in 20 to 240 positions in ground-segment increments of 20.

To link daughterboards to backplanes, the right-angle board-to-board connector substitutes a right-angle receptacle for the one used in the vertical-stacking connector. The male plug is the same. Because right-angle connectors are often used in applications where tolerances may exceed 0.035 in., a second version contains metal guide pins, which provide a 0.090-in. radial pickup.

For cable-to-board applications, the Micro-Strip connector plugs terminate newly designed ribbon cables with 20 and 40 signal positions *(Fig. 2)*. Applications calling for larger cable sizes require a modular approach, in which clam-shell covers group 20- and 40-position modules into 60-, 80-, 100-, and 120-position assemblies. The cable plugs mate with pc-board receptacles that come in both vertical and right-angle styles to suit many applications.

To effectively take advantage of the Micro-Strip technology in a cable assembly, AMP developed a compatible transmission ribbon cable and a new termination method. The cable has 31.5-gauge silver-plated copper conductors on 0.0125-in. centerlines. Teflon is used as the cable insulator to get the highest possible propagation speed. The resulting conductor size and spacing yields a cable with 50-Ω impedance.

Such narrow conductor spacing ruled out conventional insulation-displacement techniques. Instead, AMP developed a termination method it calls mass termination/reflow solder, which selectively removes insulation. The conductors are mass-inserted into slots in the rear of the signal-pin and ground-bus units. The entire cable-connector assembly is then reflow-soldered using a precise, controlled technique that guarantees a highly reliable interface.□

PRICE AND AVAILABILTY

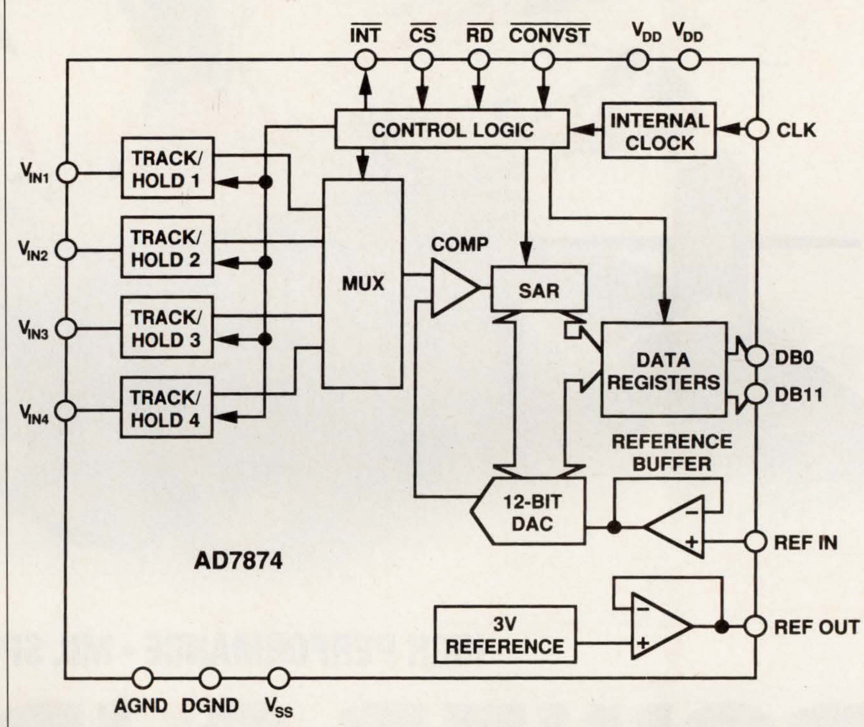
Board-to-board connectors in volume quantities go for $0.15 to $0.21 per mated line, depending on configuration. Initial production quantities are available 10 to 12 weeks after receipt of order.

AMP Inc., P.O. Box 3608, Harrisburg, PA 17105-3608; (800) 522-6752. CIRCLE 515

HOW VALUABLE?	CIRCLE
HIGHLY	538
MODERATELY	539
SLIGHTLY	540

FIRST SIMULTANEOUS SAMPLING IC ADC GRABS 4 SIGNALS TO 12-BIT ACCURACY

FRANK GOODENOUGH



The Analog Devices AD7874 is the first monolithic analog-to-digital converter that simultaneously samples—puts into hold—more than one input signal and then sequentially digitizes them all. When it's given an encode command ($\overline{\text{CONVST}}$), its four sampling amplifiers on its frontend go into hold and a 12-bit analog-to-digital conversion of one of the four held voltages begins *(see the figure)*. Until now, you were stuck with either using a module, or adding a quad IC sample-and-hold amplifier (SHA) ahead of your ADC. The latter required working out your own timing, data storage and data transfer.

This ADC not only offers 12-bit resolution, but 12-bit static and dynamic accuracy as well. Just 35 µs passes from the time it grabs four input signals, until it's ready to grab four more. That time translates to a minimum throughput rate—for all four channels—of 29 kHz. And sampling at 29 kHz, it's 12-bit accurate for 14.5-kHz (Nyquist rate) signals. That 35 µs also includes time to sequentially transfer the four 12-bit digital words stored in on-chip registers to a processor bus. When switching into hold, aperture delay matching among the four sampling amplifiers is a maximum of 4 ns and aperture uncertainity, or jitter, for each, is typically 200 ps. (Although jitter is a typical specification, because of the cost of production testing, it's sample-tested to insure conformity.)

What do you do with a simultaneous SHA-digitizer? Its forte is digitizing multiple signals with critical phase or timing relationships between them. That includes converting the same signal at multiple locations in a circuit—or in space, for example monitoring an explosion at several sites. The majority of these jobs represent the acquisition of signals for a large class of digital signal processor applications. These include phased-array sonars, the analysis of mechanical vibrations (ranging from seismic signals to those from internal combustion engines), and vector control of large, three-phase ac motors to optimize torque. The last involves controlling not only the frequency of the voltage driving the motor, but its phase as well. The IC samples the current in two of the three motor windings and the voltage across two of them.

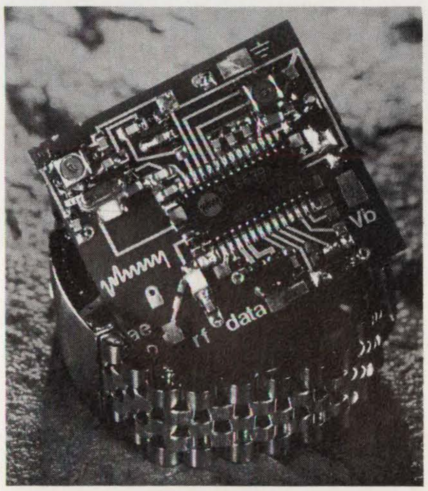
The $\overline{\text{CONVST}}$ command is asynchronous and independent of the AD7874's internal clock. Where timing is critical, it can be triggered by events or by a precision clock. Its rising edge switches the four SHAs from their tracking (acquisition) mode to hold where they remain until their four outputs have been digitized. The command also starts conversion of channel one. When it's complete, the digital word is stored in register one and the conversion of channel two starts. The sequence is repeated until the digital words representing the four held voltages are stored in registers. At that time $\overline{\text{INT}}$ goes low returning the SHAs to the track mode and telling a host that conversion is complete. The SHAs each acquire new input signals (±10 V, fullscale) to 12-bit accuracy in under 2 µs maximum.

Sampling 10-kHz sine waves at 29 kHz typically results in better than ±1/4 LSB differential linearity. Under similar conditions signal-to-noise ratio is a minimum of 70 dB. Total harmonic distortion (THD), spurious noise, and intermodulation distortion (IMD) are a maximum of -80 dB (IMD is specified while sampling 9- and 9.5-kHz sine waves.). Integral linearity of the premium B grade is ±1/2 LSB, that of the A grade ±1 LSB. The AD7874 comes in 28-pin plastic and ceramic DIPs and plastic SOICs, and extended-industrial and military temperature ranges. Unit pricing in 100s, ranges from $30 to $43.

Analog Devices Inc., 181 Ballardvale St., Wilmington, MA 01887; (508) 937-1428. **CIRCLE 314**

Receiver-On-A-Chip Converts 200 MHz FSK RF To 1.2 kB/s Data

A complete, direct-conversion radio receiver-on-a-chip from Plessey Semiconductors Corp., known as the SL6639, converts a fequency-shift-keyed modulated radio-frequency carrier signal to baseband. The carrier can range from a frequency of 100 MHz up to 200 MHz. The FSK modulated signal can have a data rate as high as 1200 bits/s. All active devices in the SL6639 receiver, including channel filters implemented by gyrators, lie on the chip—which fits in a 28-pin SOIC package.



The device is aimed at low-power, personal communications systems such as miniature pagers and modems. It features a typical power drain of just 5 mW. In its power-down mode, power use drops to a few microwatts.

The gyrator-filters, which are tuned with a single potentiometer, eliminate the space and cost of difficult-to-tune, multi-pole, ceramic or crystal filters. Moreover, external filters often require double conversion to achieve the same channel selectivity as the gyrators—adjacent-channel rejection is in excess of 70 dB—with 25-kHz channel spacing.

With its sensitivity of -124 dBm (0.14 μV) at a frequency of 150 MHz from a 50-Ω source, operation directly from an antenna is possible in most applications. However, an RF stage can be added ahead of it.

Other features include high current-beeper and LED drive currents of 200 mAand 50 mA, respectively, and a low-battery flag. The LED is pulsed at a frequency of 32 kHz. A typical receiver uses 1.6 mA of current from a 1.3-V battery, and 0.5 mA of current from a 2.3-V source. An evaluation board is available to simplify trying out the chip. Operating temperature range is -20 to +60°C. In quantities of 100,000, the SL6639 receiver chip goes for $7.27 each.

***Plessey Semiconductors Corp.**, 1500 Green Hills Rd., Scotts Valley, CA 95066; Ashi Majid. (408) 438-2900.* **CIRCLE 315**

■ *FRANK GOODENOUGH*

THREE S-D CONVERTERS CRAM INTO TINY CAN

Aimed at three-axis positioning systems for measuring such things as roll, pitch and yaw, the SDC-14610 from ILC Data Device Corp. contains a trio of synchro/resolver-to-digital converters. Because they're based on a custom CMOS chip, the converters are squeezed into a double-DIP 36-pin metal can less than 2-in. long. All three of these completely independent converters have a resolution of 14 bits and an accuracy of 4 minutes of arc plus 1 LSB. Differential linearity and repeatability are both within 1 LSB maximum. Each a linearity of 1% of fullscale. They provide velocity feedback in a typical closed-loop servo system, replacing three tachometers. Internal, solid-state Scott-T circuits condition the input from the synchros. The three converters need a total of just 51 mA from ±5-V rails. In quantities of 100, the commercial-temperature range SDC-14610 goes for a price of $565 each.

ILC Data Device Corp., 105 Wilbur Pl., Bohemia, NY 11716; Bill Cullum. (516) 567-5600, extension 389. **CIRCLE 316**

LOW-NOISE, 1.5-PA-I_b OP AMP NOW IN DIP

Until now, if you wanted an IC op amp with 1 or 2 pA of bias current, an offset voltage under 1 mV, and low noise, you were stuck with devices in expensive metal cans. That's no longer the case.

Analog Devices' AD645K is a low-noise op amp IC that sports a maximum (warmed-up) bias current (I_b) of just 1.5 pA. It also sports a maximum offset voltage of 400 μV, and a guaranteed—and 100% tested for—voltage noise from 0.1 to 10 Hz of 2.5 μV pk-pk. And in quantities of 1000, it goes for just $3.76 each, about half the price of similarly specified op amps in TO-99 metal cans. (It should be noted that offset voltage and offset drift of the competitive units are superior.)

These op amps are designed to convert currents from photodiodes, particularly the numerous photodiodes found in CAT scanners, to voltages. Op-amp voltage noise must be low, because a photodiode is not a true current source. Thus noise gain, usually unity in an I-to-V converter circuit, arises to amplify voltage noise.

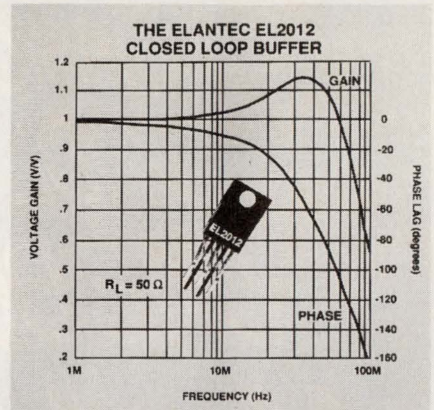
Analog Devices Inc., 181 Ballardvale St., Wilmington, MA 01887; (508) 937-1428. **CIRCLE 317**

CHIP COMBINES ATE LOAD, DRIVER, COMPARATOR

The Bt698 integrates the load, driver, and comparator functions of automatic-test-equipment pin electronics into one IC. The chip's three-statable driver can force –3 to +8 V at ±25-mA static drive currents and 100-mA dynamic edge current. The dual comparator handles the same voltage input range and has a high impedance for direct connection to the device under test without an external buffer. The window comparator can be transparent or the input data can be strobed into a register by an external clock. In 100-piece quantities, the Bt698 costs $130 in a 44-pin plastic J-lead chip carrier. Samples are available now; production quantities in the second quarter 1991.

Brooktree Corp., 9950 Barnes Canyon Rd., San Diego, CA 92121; (800) 843-3642. **CIRCLE 318**

80-MHZ CLOSED-LOOP BUFFER DRIVES 50 X

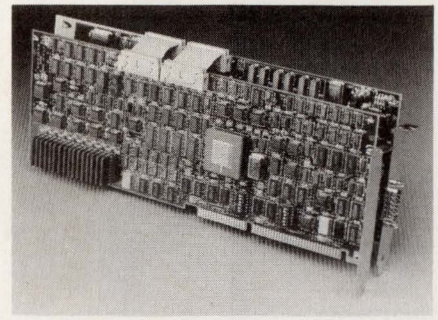


VOLTAGE GAIN & PHASE LAG

Housed in a 5-pin TO-220 package, Elantec's EL2012 80-MHz closed-loop buffer IC looks like a power device, but it's pure analog too. It puts a 6-MHz ±10-V, sinewave across a load of 50 Ω, which represents twice the drive of competitive devices. Moreover, its gain with that load is 0.999, not the 0.6 typically expected from an open-loop buffer. Its job is to drive cables, capacitive loads, and analog-to-digital converters with precision. Built on Elantec's dielectrically isolated process, it bolts directly to a heat sink—without the need for insulation. In quantities of 100, the EL2012 goes for a price of $8.07 each.

Elantec Inc., 1996 Tarob Ct., Milpitas, CA 95035-6824; (408) 945-1323. **CIRCLE 319**

TWO IMAGE-PROCESSING BOARDS INCREASE SPEED, FLEXIBILITY



Two image-processing boards from Data Translation Inc., the DT2878 and the DT2868, connect directly to the company's DT-Connect-compatible frame grabbers to accelerate image-processing-intensive computations. The flexible 2878 advanced processor features true fast-Fourier-transform capability that allows data from partial or whole frames to be processed and analyzed in the frequency domain. And because data transfers bypass the PC/AT bus, the PC host can perform graphics, data analysis, or other operations while data values transfer over DT-Connect.

The 25-MFLOP, 32-bit floating-point board is built around AT&T's DSP32C digital-signal processor chip. The chip's 80-ns instruction cycle supplies high-speed floating-point operation. Data can be processed in either floating- or fixed-point formats. Users can also take advantage of Data Translation's advanced image-processing library.

The 2868 high-speed frame processor is a faster version of Data Translation's DT2858 auxiliary frame processor. With its pipelined architecture, the 2868 isn't as flexible as the 2878, yet it performs image-processing operations three times faster than the 2858, and up to 100 times faster than the PC/AT host computer. The board can carry out 10 million additions or multiplications per second.

The 2868's on-board 16-bit ALU performs over 40 of the most common processing operations at speeds up to 10 MHz. In addition, it supports convolutions, hardware zoom, pan, and scroll, histogram generation on single or multiple frames, and division and normalization.

The 2878 is available in two versions, with either 2 or 4 Mbytes of data memory. It costs either $4495 or $5495 and is available now. An 8-Mbyte version is in the works. The 2868 comes with 512 kbytes of frame-store memory. It costs $1995 and will be available December 15. Large-quantity discounts are available on both boards.

***Data Translation Inc.**, 100 Locke Dr., Marlboro, MA 01752; (508) 481-3700.* CIRCLE 377

■ *RICHARD NASS*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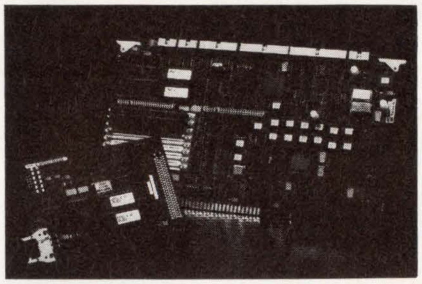
ADD DOS COMPATIBILITY AND A 386SX PROCESSOR TO A MULTIBUS I SYSTEM

By using a 16-MHZ 386SX PC and putting it onto a Multibus I form factor, the iSBC board, from Intel Corp., lets users add 32-bit performance and DOS compatibility to their Multibus I systems. It gives them the functionality of a PC in a Multibus I form factor. The board can be used in a new design, or it can replace several existing boards to upgrade a system. In addition to replacing a CPU board, it can replace a peripheral controller board and any add-on modules for local memory or access to printers or a keyboard.

The board also runs Intel's iRMX 32-bit real-time operating system. iRMX III is suitable for controlling real-time processes common to industrial, communications, and other time-critical applications. The iSBC can also run DOS and iRMX III concurrently with full data exchange between the DOS and real-time applications. Using iRMX III, programmers can design high-performance, real-time systems with easy-to-use DOS user interfaces.



The iSBC board holds the complete set of on-board I/O, real-time, and peripheral-control resources that are typically found on a PC/AT motherboard. Included on the board are a floppy-disk drive controller, a Winchester hard-disk controller for a 40- or 80-Mbyte drive, two asynchronous serial ports, a parallel port, interrupt controllers, a real-time clock, and two 16-bit iSBX connectors. VGA graphics can be added by using an optional module, the iSBC 272. There's also a socket on board for an 80387SX numeric coprocessor. The board has a capacity of 8 Mbytes of RAM using plug-in SIMM packages. A complete on-board BIOS can be stored in EPROM. Typical power consumption is 6 A. The iSBC board operates in the temperature range of 0 to 60° C.

With 512 kbytes of memory, the board costs $1450. The price rises to $1800 with 2 Mbytes. Either way, it's available in December. The VGA graphics module, also available in December, sells for $400.

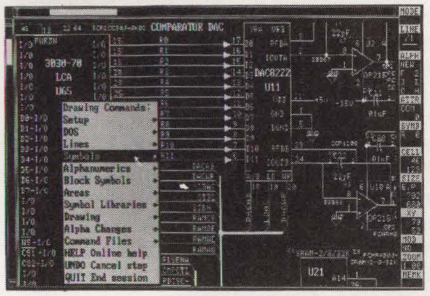
***Intel Corp.**, 3065 Bowers Ave., Santa Clara, CA 95051; (800) 548-4725 or (408) 765-8080.* **CIRCLE 385**

■ *RICHARD NASS*

CIRCLE 112

CAPTURE SCHEMATICS IN A WINDOWED INTERFACE

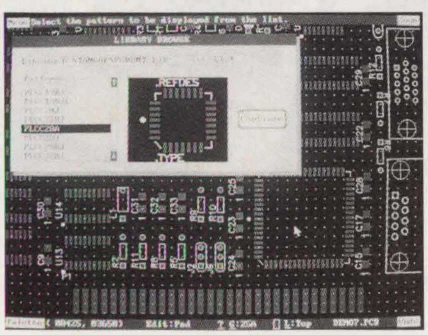
Data I/O Corp. has made the latest version of the FutureNet schematic-capture software, FutureNet-5, easier to use with a windowed interface and an expanded design feature set. Safety features such as periodic auto-saves protect work from being lost in the event of power or system failures. Other safety features minimize mistakes when commands are executed unintentionally. Also, the software alerts users



when drawing memory is low, providing the opportunity to save the drawing before available memory is depleted. FutureNet-5 combines a menu-driven design environment with dialog boxes. Dialog boxes visually prompt the user for input, providing a list of possible options for completing a particular command. FutureNet-5, which runs on IBM PCs and compatibles, is shipping now. It cost $499 in quantities of ten, and $895 for single-site versions. Existing FutureNet users can update for $595.

Data I/O Corp., 10525 Willows Rd. N.E., P.O. Box 97046, Redmond, WA 98073-9746; (206) 881-6444. **CIRCLE 320**

AUTOPLACEMENT BEEFS UP TANGO PCB TOOLS



Autoplacement heads the list of more than 30 features that have been added to the newest release of Accel Technologies' Tango family of pc-board design tools. A few of the more important features of Version 2.0 are: polygon fill; power and ground planes that can be edited; the addition of four mid-layers, increasing the total to 23 layers; autopanning; and user-definable keyboard macros. In addition, maze routing was enhanced with a second routing pass using a larger grid area. The four Tango packages in the pc-board design family (Tango-PCB, Tango-PCB Plus, Tango-Route, and Tango-Route Plus) range from $495 for individual entry-level tools to $1695 for a bundled, professional pc-board and autoroute combination. Version 2.0 programs will be available later this month.

Accel Technologies Inc., 6825 Flanders Dr., San Diego, CA 92121; (619) 554-1000. **CIRCLE 321**

SOFTWARE SYNTHESIZES MICROWAVE CIRCUITS

RFSynthesist is a new synthesis tool from ingSOFT Ltd. that creates rf and microwave circuits. The tool performs filter synthesis, calculation of transmission-line characteristics from physical dimensions, synthesis of microstrip lines, and calculation of coupled transmission-line characteristics in stripline and microstrip configurations. It can create Butterworth, Chebyshev, elliptic, and coupled-resonator filters. In addition, the company provides user support in the form of a 500-page user's manual, an on-line manual, a newsletter with practical examples, and active consulting in rf engineering. The synthesis software works as a standalone application or as a part of the RFDesigner system, ingSOFT's complete rf and microwave engineering environment. RFSynthesist runs on all Macintosh computers. It's available now for $1200.

ingSOFT Ltd., 213 Dunview Ave., Willowdale, Onatario, M2N-4H9, Canada; (416) 730-9611. **CIRCLE 322**

SABER LIBRARY ADDS 40 OP-AMP MODELS

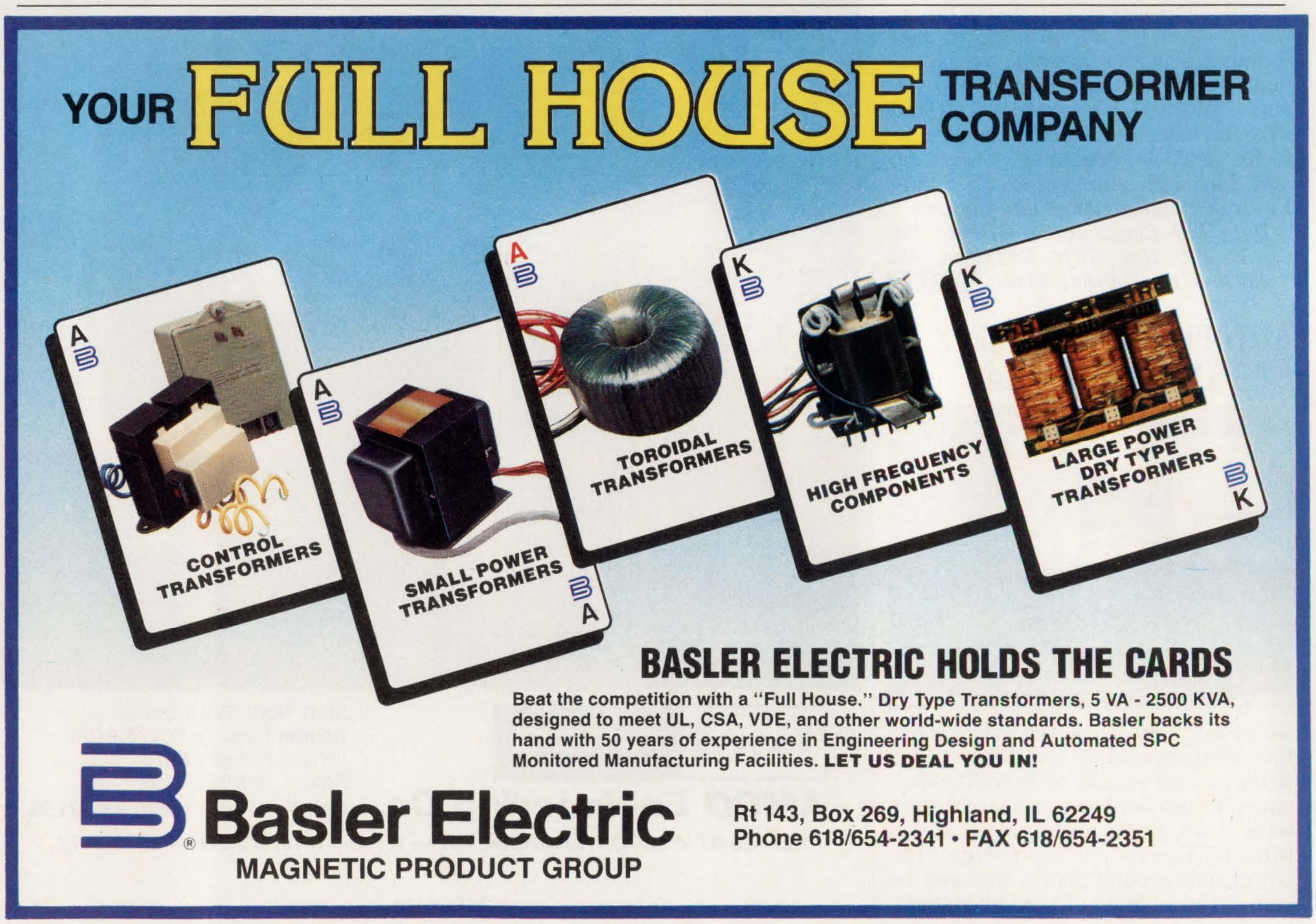
An agreement between National Semiconductor Corp., Santa Clara, Calif., and Analogy Inc. has produced over 40 behavioral op-amp models for Analogy's Saber simulator. National worked closely with Analogy in model definition and verification. Analogy will offer two levels of op-amp models. OP1 models are used in the top-level design stage that takes into account first-order effects. OP2 models are used to simulate both first- and second-order effects. In addition to many standard capabilities, OP2 models include such features as external compensation, crossover distortion, nonlinear output inductance and resistance, asymmetry in the output stage, and accurate noise analyses. OP1 models are available now and OP2 models will be available early in 1991. The OP1 models are included in the standard-parts library, which costs $3600 a year.

Analogy Inc., 9205 S.W. Gemini Dr., Beaverton, OR 97005; (503) 626-9700. **CIRCLE 323**

ENHANCED SIMULATOR DEBUGS IN 2D

The newest release of the Silos II fault and logic simulator, version 90.1, contains new features such as 2D interactive debugging, support for FutureNet-compatible ASIC part libraries, analog behavioral modeling, and a facility that lets users create custom reports. Debugging can take place in both the time and topology dimensions. When users discover that a node has transitioned to an incorrect state, they can interactively trace the cause of the transition backwards in time and through the fan-in parts of the node, as well as through device layers. Also, version 90.1 lets users scan a time range for spikes or unknown levels. Silos II version 90.1 is shipping now. It runs on a wide variety of platforms, including PCs, Macintosh computers and workstations, and mainframes. Pricing ranges from $5000 to $80,000, depending on hardware platform.

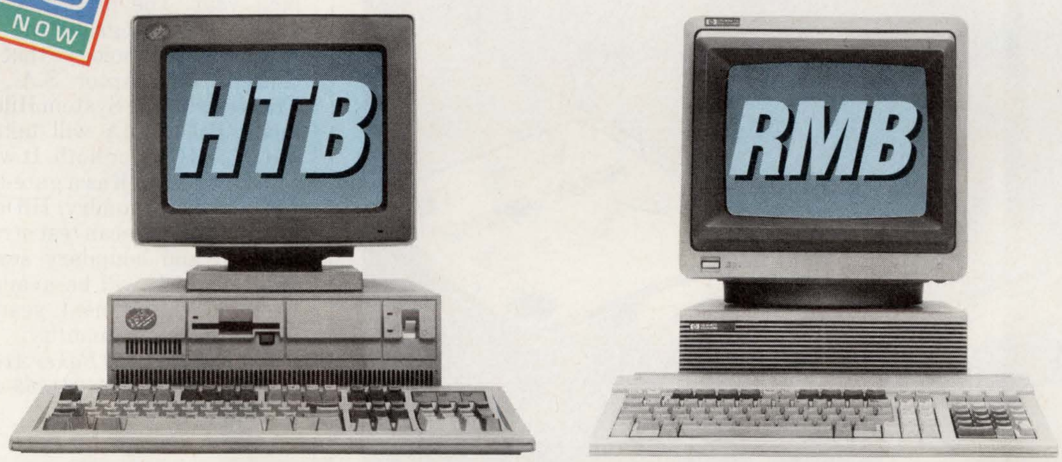
Simucad Inc., 32970 Alvarado-Niles Rd., Suite 744, Union City, CA 94587; (415) 487-9700. **CIRCLE 324**



CIRCLE 194

All the features of HPBASIC, and more. For less.

TransEra HTBASIC 3.0 ORDER NOW



HTBasic	BASIC FEATURES:	HP BASIC
YES	IEEE-488 GPIB (HP-IB), RS-232 Instrument Control	YES
YES	Integrated Environment: Mouse, Editor, Debugger, Calculator	YES
YES	Supports 16 Megabytes of Memory (breaks DOS 640K barrier)	YES
YES	Engineering Math: Matrix Math, Complex Numbers	YES
YES	High Level Graphics: Screen, Plotter, Printer	YES
YES	Structured Programming with Independent Subprograms	YES
YES	Runs on Industry Standard Personal Computers	NO*
YES	Industry Standard Graphic Printer Support: Epson, IBM, lasers, etc.	NO
YES	Industry Standard Network Support: Novell, IBM, Microsoft, NFS, etc.	NO
YES	Industry Standard IEEE-488 Support: National Instruments, IOtech, etc.	NO
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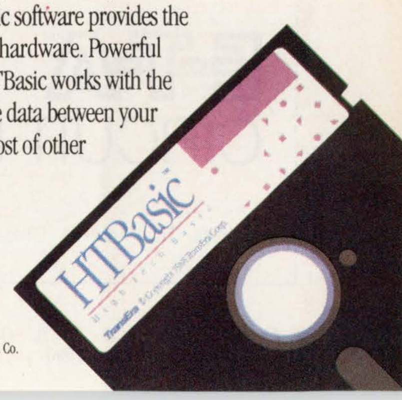
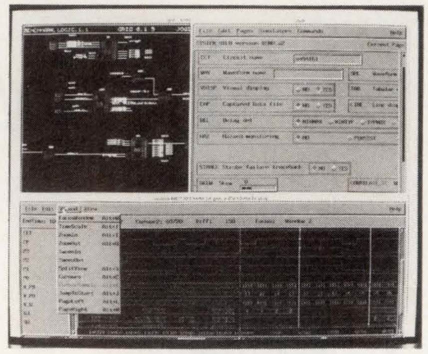


CIRCLE 133

SYSTEM HILO BOASTS IMPROVED SIMULATION

Enhanced simulation is one highlight of the newest release of GenRad's System Hilo design tools, System Hilo 4. All the tools have increased functionality, are faster, and more accurate. System Hilo 4 can operate with VHDL and GenRad's own hardware-description language, GHDL. VHDL and GHDL models can be mixed at any level. The new software has source-level debug facilities for both languages. Users can breakpoint, single step, and examine and change variables interactively during simulation. In addition, GenRad is working on a project that will bring logic synthesis into the Hilo environment next year. The project, called HiDesignA, will integrate the company's synthesis technology that was purchased from Aptor S.A., Grenoble, France, with the System Hilo 4 environment. HiDesignA will take in either VHDL, GHDL, or both. It will output a schematic as well as a gate-level netlist for the ASIC foundry. HiDesignA will also synthesize scan test structures for internal and boundary scan. System Hilo 4, which will be available in the first quarter of next year, will cost $18,000 in single quantity.



GenRad Inc., 300 Baker Ave., Concord, MA 01742-2174; (508) 369-4400.

CIRCLE 325

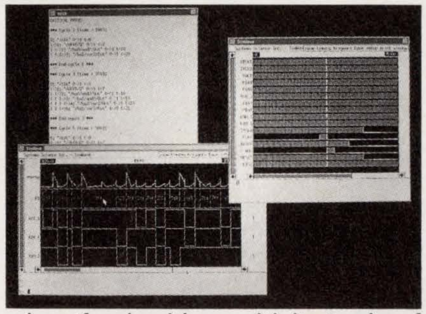
FPGA TOOLS INCREASE UTILIZATION BY 20%

Plustran 2.0 is the newest version of Plus Logic's FPGA design tools. The new release broadens support for 80286- and 80386-based CAD tools, and adds support for Sun workstation-based tools. Through automatic partitioning, minimization, and optimization, Plustran 2.0 uses FPGA silicon 20% more efficiently than the previous version. With the improved logic minimization, a 4000-gate equivalent part becomes a 4800- or 5000-gate equivalent part. The density increase is due to improvements in the optimizer-minimizer that merge and combine functions in one timing pass through the chip. In addition, the user interface has been improved to make it easier for designers to get started. Plustran 2.0 is available now for $2800. The design system includes software, documentation, Plus Array Programmer, a choice of symbol library, and one year of maintenance. It runs on 80286- and 80386-based PCs and Sun workstations.

Plus Logic Inc., 1255 Parkmoor Ave., San Jose, CA 95126; (408) 293-7587. **CIRCLE 326**

COMPUTE IC POWER, SKEW, ON A HARDWARE ACCELERATOR

The Advanced ASIC Designer software package from Zycad Corp. analyzes circuit power consumption, input-output skew timing margins, and critical paths at hardware accelerator speeds. ASIC Designer works with the company's Mach and XP hardware simulation-acceleration systems at speeds up to 2.5 million events per second.



The package consists of three tools, all developed by System Science Inc., Palo Alto, Calif. PowerSim uses functional or test vectors to compute the power consumed by CMOS circuits during operation. Power is calculated by performing a special simulation that takes into account the switching activity and capacitance of all nodes, the constant leakage current for each primitive, and the operating voltage. The information is then fed into a series of equations to compute the instantaneous energy consumption at each time point for the whole circuit, or any part of the circuit. Post-processing determines the peak and average power within any time period.

The second tool, PinSkew, determines the circuit's sensitivity to signal timing variations. The software simulates circuit operation with functional or test vectors while varying the input stimulus timing and the output strobe timing. PinSkew tests the circuit to determine if its operation matches the results generated with databook timing.

Finally, Critical PathFinder analyzes critical circuit paths using functional or test vectors. It can be used to speed up a circuit or determine where delays occur. Advanced ASIC Designer costs $60,000.

***Zycad Corp.**, 1380 Willow Rd., Menlo Park, CA 94025; (415) 688-7400.* **CIRCLE 327**

■ *LISA MALINIAK*

PC-BASED ASIC TOOL OUTPUTS WAVEFORMS

Now engineers designing gate arrays on their 80286- and 80386-based personal computers with International Microcircuits' PC-EasyGate software can get simulation results outputted as waveforms. Users can display up to 14 traces at once through a selected range of cycles. Viewing features include zooming and forward and backward scanning. In addition, help menus aid users in selecting software functions. The PC-EasyGate package helps designers create digital gate-array circuits with up to 12,000 gates. It performs simulation and autotest program generation. The PC-EasyGate simulator will accept both OrCAD and Futurenet schematics. PC-EasyGate with waveform-output capability is available now. The software requires MS-DOS 4.0 or higher, 640 kbytes of RAM, VGA graphics, and a 20-Mbyte hard disk drive. It costs $1250.

International Microcircuits Inc., 525 Los Coches St., Milpitas, CA 95035; (408) 263-6571. **CIRCLE 328**

PCB LAYOUT TOOL DOES FAST AUTOROUTING

The latest release of Ultimate Technology's pc-board layout software, Ultiboard Version 4.2, now has a gridless interactive autorouter that lets engineers specify autorouting by window, net, or component. In addition, the company's batch router has increased tremendously in speed. For example, a complex, surface-mounted, double-eurocard-size board typically routes in less than two hours. Version 4.2 also adds block functions that maintain design integrity. The Ultiboard real-time design-rule check operates throughout the block commands, making it impossible to cause design-rule violations without overriding the system. Both the interactive and batch routers will be included free in all Version 4.2 packages, which will ship this month. Entry-level DOS-based systems start at $995. A free evaluation copy is also available for the asking.

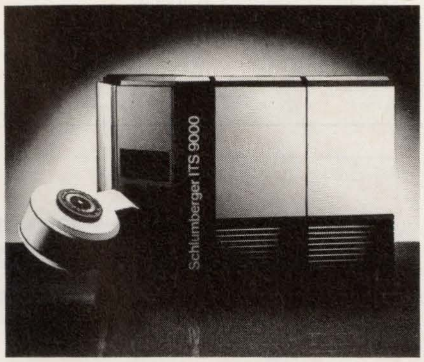
Ultimate Technology, 269 Mt. Herman Rd., Suite 105, Scotts Valley, CA 95066; (408) 439-8944. **CIRCLE 329**

ICON-BASED SOFTWARE AND TESTER ARCHITECTURE SPEED PROGRAMMING

A new hardware architecture and powerful software help the ITS 9000 series component testers slash test-program generation time. The multifunction system offers embedded memory and scan capabilities, as well as single-insertion test coverage of mixed-signal devices.

The new hardware architecture, called Sequencer Per Pin (SPP), is a timing system based on proprietary ASIC technology that allows a true replication of the simulator environment on the tester. Device functionality is directly checked against the simulator output, so manual modifications of CAD-generated vectors are not needed. As a result, test engineers using SPP can generate complex waveforms.

The SPP architecture is tightly coupled with the Advanced Symbolic ATE Programming (ASAP) software. This package is an icon-driven environment that uses interactive windows to create, test, debug, and modify test programs in real time, without the need to recompile. ASAP is self-checking and self-complete, so the programmer can test the program as it's being written. Once a test icon is saved, it becomes part of a library that can be used to create new programs.



Systems are available with clock rates to 200 MHz and data rates from 40 to 200 MHz for up to 512 pins. Overall edge-placement accuracy is 175 ps. The SPP architecture permits expansion to 1024 pins. ITS 9000 prices range from $1.8 to $2.8 million for a 256-pin unit to $3.1 to $4.8 million for 512 pins. The system can be ordered now.

***Schlumberger Technologies, ATE Div.**, 1601 Technology Dr., San Jose, CA 95110-1397; (408) 453-0137.* CIRCLE 330

■ *JOHN NOVELLINO*

TOOLS SPEED WRITING OF TEST-PROGRAMS

Four software tools help users develop linear and mixed-signal component tests on the Teradyne A500 family of test systems. The individual packages offer assistance that ranges from automatically generating program code to generating whole programs from symbolic-level code modules. The set includes Image ExPress, a code-producing display that works with the A500 testers or a workstation running Teradyne's Image Simulator/Workstation software. The engineer specifies the test instrument setup by pointing and clicking on the graphic display with a mouse. Other tools are the Progen test database management system, device testing libraries in the Progen format, and Analyzer tools specific to certain device families. Prices for the software range from $5000 to $30,000. Deliveries will begin in the first quarter of 1991.

Teradyne Inc., Industrial/Consumer Div., 321 Harrison Ave., Boston MA 02118; (617) 482-2700. CIRCLE 331

500-MHZ TESTER HANDLES ULTRA-FAST MEMORIES

The Ando-9048 500-MHz memory tester has features aimed at a variety of memory types. The system has independent timing generators at each pin, a 128-kword fail memory, and a 256-word, 68-bit-wide data-log memory. Programmable drivers deliver a 2-V pk-pk swing from −2 to +2 V. Accuracy is ±200 ps. Users can program the synthesizer-based timing system for cycle widths from 2 to 128 ns, with 128-ps resolution. Up to 16 timing sets can be used on-the-fly. The 9048's 12X and 12Y address capability allows testing of up to 16-Mbit RAMs. For static RAMs, the tester offers data verification to within 8 ps of the end of four complete cycles. For cache memories, the 9048 can test devices up to 32-bits wide. A 96-pin version of the Ando-9048 costs about $2 million, with delivery in 4 to 6 months, depending on configuration.

Ando Corp., 480 Oakmead Pkwy., Sunnyvale, CA 94086; (408) 738-2636. CIRCLE 332

0.99 Power Factor Corrected Switcher With Universal Input

1000 watt single and multiple output switch-mode power supplies operate from 120 VAC 15 Amp service, or as Universal Input from 90 to 264 VAC line without strapping. Units meet IEC 555-2 harmonic distortion and UL, CSA, VDE, EN, and FCC safety and EMI specifications. Other models operate from 48 VDC or 120/230 VAC.
Contact: **Qualidyne** (619) 575-1100

Qualidyne ▶ **CIRCLE 641**

Compact, Modular Switchmode Supply Meets Class B EMI

Compact power supplies can provide up to 400 watts with hundreds of volt/amp combinations of from 1 to 7 DC outputs. Units are available with in-line or side-mount I/O terminals and operate from 120/230 VAC. Options include Auto Current-Sharing with a isolated Power Supply Fail signal, ideal for N+1 use.
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Qualidyne ▶ **CIRCLE 642**

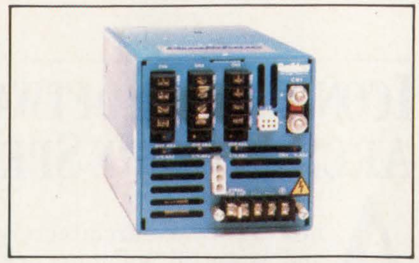
Low Profile/Low Cost Supplies Are Only 2" to 3" High

Compact switchers feature robust, high-current main and auxiliary outputs to suit OEM needs. Single and multiple output models provide from 250 to 1000 watts. Wide user-adjustment ranges, auto AC line select, integral fan-cooling, margining, and inhibit are among the features and available options.
Contact: **Qualidyne** (619) 575-1100

Qualidyne ▶ **CIRCLE 643**

Modular 5" x 5" & 5" x 8" AC-DC Switchers & DC-DC Converters

Hundreds of models with up to 9 independent outputs can be easily configured to meet custom requirements without delays. Providing 800 to 3000 watts, units operate from 48 VDC or 120/230 VAC. All meet EMI and safety specs from UL, CSA, EN, FCC and VDE. Wide adjustable and current sharing outputs available.
Contact: **Qualidyne** (619) 575-1100



Qualidyne ▶ **CIRCLE 644**

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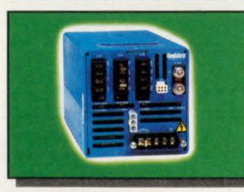

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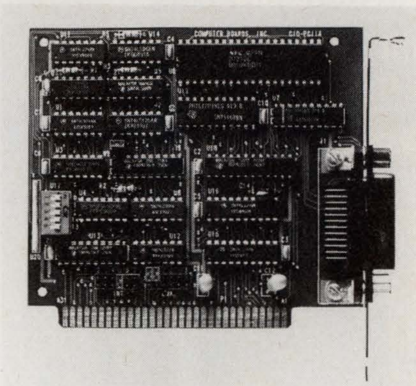
▶ **CIRCLE 645**

LOW-COST BOARD OFFERS GPIB-TO-PC INTERFACE

The CIO-PC2A is a low-priced IEEE-488 (GPIB) interface board for IBM PC/XT/AT computers. The board, which is based on a standard NEC uPD7210 interface chip, offers complete talker/listner/controller capability. Data transfer rates up to 300



kbytes/s are possible using direct memory access (DMA) on one of the three available channels. Six interrupt lines support transparent enabling and disabling. The board is a half-size card equipped with an rf-shielded IEEE-488 cable connector. The CIO-PC2A costs $125 each in quantities up to nine, $99 each in lots of 10 to 24, and $85 each for orders over 25. A 2-m IEEE-488 cable costs $59.

Computer Boards Inc., 44 Wood Ave., Mansfield, MA 02048; (508) 261-1123. **CIRCLE 333**

50-MHZ TESTER FEATURES TIMING EDGE FLEXIBILITY

The Polaris 50 is a 50-MHz production tester optimized for the current generation of logic products. Like its "big brother," the 100-MHz Polaris 100, the new system has a second-generation test-per-pin architecture. But the Polaris 50 is aimed primarily at high-volume testing of today's mainstream logic products, such as popular microprocessors and ASICs. It can be configured with from 32 to 384 pins. The Polaris 50's ability to place timing edges over four cycles makes automatic generation of test programs much simpler and faster. Additionally, the system's 4-million vector memory depth satisfies the higher memory requirements of test programs generated directly from CAD tools. Timing accuracy is ±150 ps. The system is field-upgradable to the 100-MHz version. A 256-pin Polaris 50 costs $1.7 million, with availability 6 months after receipt of an order.

Megatest Corp., 880 Fox Ln., San Jose, CA 95131; (408) 437-9700. **CIRCLE 334**

TEST SOFTWARE FEATURES RELATIONAL DATABASE

A software package for test-data collection and analysis includes a network-wide distributed relational database, automated data collection tools, and an extensive set of reporting and analysis tools. The system, dataVision, features a platform-independent graphical interface based on X Windows and OSF/Motif. The distributed database has a true next-generation "peer-to-peer" architecture, which provides fault-tolerant protection that eliminates traditional bottlenecks caused by networks or overworked central servers. The software supports the LTX Synchromaster, Micromaster, Validmaster, and Deltamaster test systems. The package's integrated analysis tool offers transparent access to the distributed database, statistical-analysis routines, graphic display system, and tabular report generator. All plots and displays are on-line, so users can quickly generate histograms, scatter plots, X-bar-R charts, and trend charts.

LTX Corp., LTX Park at University Ave., Westwood, MA 02090; (617) 461-1000. **CIRCLE 335**

TEST PACKAGE SUPPORTS TI 320C2X-BASED BOARDS

Designers of boards based on the Texas Instruments 32020, 320C25, and 320C26 digital signal processors can now test those boards on the Fluke 9100A digtal test system. Testing is done through the reconfigurable 9132A memory interface pod using the new 9132A-320C2X processor support package. The package includes a processor-specific personality module, a sync module adapter, a software disk, and a manual. Besides the standard ROM and RAM tests and checks of the Read and Write functions, the package includes a microfloppy of 9100A programs with enhanced diagnostic capabilities for kernel hardware faults. The 9132A also incorporates the HyperTest algorithm, which can test 1 Mbyte of the unit-under-test's RAM in a little as 1 second. The 9132A-320C2X list price in the U.S. is $2500. Delivery is within 8 weeks.

John Fluke Mfg. Co. Inc., P.O. Box 9090, Everett, WA 98206; (800) 443-5853., ext. 88. **CIRCLE 336**

Speedy VGA Controller Packs Cursor Hardware

Offering over eight times the video display throughput of the IBM VGA display controllers, the 77C22 from NCR can use inexpensive DRAMS yet deliver the performance of systems built with video RAMs. The IC includes support hardware for a bit-mapped cursor, a 16-bit bus interface with deep 32-word by 16-bit FIFO registers, and latched address and data lines. Via various control-pin configurations, the same chip can tie directly into AT, EISA, or Micro Channel host buses, simplifying off-chip logic for an adapter card and for embedding the chip on a system motherboard.

Basic VGA display modes are in 640-by-480-pixel resolution in up to 256 colors. Application-software drivers can let the chip display extended-resolution screens that show 1024-by-768, or 800-by-600 pixels with 16 colors, as well as lower-resolution EGA and earlier-standard screens. Dynamic control of the FIFO buffer allows the 77C22 to outperform most other FIFO-buffer-based VGA chips. The data transfers can be done at maximum host transfer rates, reducing the number of wait states required by the video subsystem. The result: measurably faster performance for text and graphic environments such as Microsoft Windows 3.0 and Presentation Manager.

The chip supports video rates of up to 65 MHz and font widths of 4, and 7 through 16 pixels, and frame buffers of up to 4 Mbytes. Special addressing logic allows simple-frame buffer copying and automatic offset addressing. A second version of the chip, the 77C22E, provides a pin-compatible superset of features as well as higher transfer rates, interlaced video modes, an even faster system interface, and support for 16-bit wide DRAMs. Production quantities of the NCR 77C22 are available at $26 in 10,000-unit lots when housed in a 160-lead plastic quad-sided flat package; the 77C22E costs $2 more in the same quantity.

NCR Corp.*1635 Aeroplaza Dr. Colorado Springs, CO 80916; (719) 596-5612* **CIRCLE 337**

■ *DAVE BURSKY*

Speedy Programmable Logic IC Packs More

The tradeoffs between speed and density usually relegate higher-complexity CMOS circuits to the slower-speed grade ICs. This locks the chips out of applications such as data paths and fast state machines. By applying its advanced 1-mm CMOS UV EPROM process, Intel has developed a high-speed version of the popular Altera EP910, the 85C090. The new chip can implement state machines that run with external clock frequencies of up to 50 MHz (66 MHz internal). Pin-to-pin propagation delays across the chip are also much shorter than those of the 40-pin Altera chip—just 15 ns vs. 25 to 30 ns. Similarly, the clock-to-output delays are also about half of those of the Altera chip—the Intel 85CO90 delays the signal by just 9 ns.

A direct pin-to-pin replacement for the EP910, the 85CO90 offers 24 macrocells, each of which permit their registers to be configured as D, T, J-K, or R-S type flip flops. Up to 36 inputs are available for the chip—12 dedicated and the remaining 24 are programmable as inputs or outputs. Two synchronous lock inputs are available on the chip and all macrocells can be set up for asynchronous clocking. Each macrocell has eight P terms, and selectable polarity for the Output, Clear, and Output-Enable terms for each macrocell. Each 85CO90 can replace the equivalent of about 3 PAL devices, thus reducing board space while delivering better overall system performance.

A programmable low-power standby option limits the power drain to just 60 mA. During normal operation, the chip draws about 105 mA when running at 50 MHz and 5 V. Samples of the 40-pin plastic DIP version of the chip are immediately available and sell for $17.75 in 1000-unit lots. Windowed DIPs as well as plastic and windowed 44-lead plastic leaded chip carrier versions will also be produced.

Intel Corp.*, 3065 Bowers Ave., P. O. Box 58065, Santa Clara, CA 95052-8065; (408) 987-8080*

CIRCLE 338

■ *DAVE BURSKY*

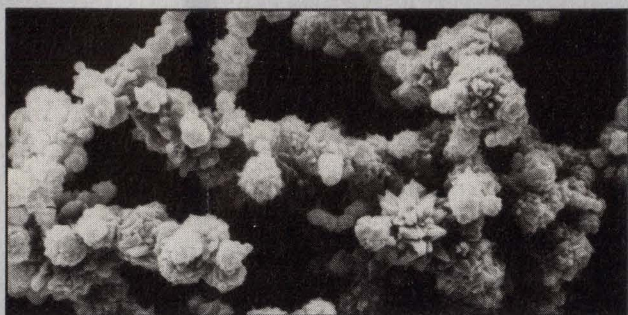
Fast Chip Does Polar To Rectangular At 20 MHz

With the ability to convert complex polar coordinate descriptions into cartesian coordinates at rates of up to 20 MHz, the PDSP16340 can simplify calculations in applications such as radar and sonar signal processing, medical imaging, and many others. The CMOS chip is a 16-bit processor that has registered inputs with separate clock enable lines for the magnitude and phase inputs. Real and imaginary result outputs are also held in registers and each has its won three-state enable control line. There are a number of user-programmable options that allow different word formats to be used for both the input and output operations. The chip runs from a 5-V supply and comes in an 84-lead pin-grid-array package. Samples are immediately available and sell for $330 in 1000-unit lots.

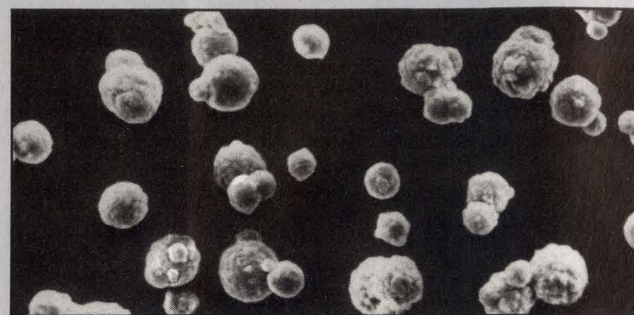
Plessey Semiconductors Corp., Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, CA 95066; Steve Brightfield, (408) 438-2900.

CIRCLE 339

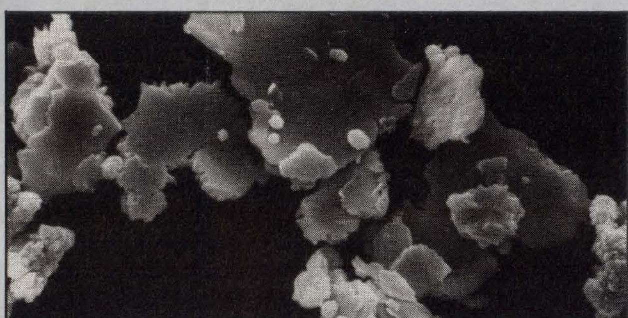
SPECIFY INCO SPECIALTY POWDERS FOR WIDE RANGE OF ELECTRONIC APPLICATIONS



Inco Type T 287 Filamentary Powder, particle size (FSSS) 2.6-3.3 microns, apparent density 0.75-0.95 g/cc, relative surface resistivity 0.30 ohms per square ($\square$).



Novamet Silver Coated Nickel Spheres, 15% Ag, 2.5 g/cc apparent density, particle size 10 microns, screen mesh 99%-250, surface resistivity 0.03 $\Omega/\square$.



Novamet HCA-1 Flake, screen mesh 98% minus 400, apparent density 0.90 g/cc, thickness 1.0-1.1 microns, surface resistivity 0.25 $\Omega/\square$.

Novamet Nickel Coated Graphite, 60% fully encapsulated Ni, apparent density 1.6 g/cc, particle size (FSSS) 100 microns, screen mesh 63% −150/+250, surface resistivity 0.3 $\Omega/\square$.

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The development of computer processed control coupled with the continuous powder production improvements enables us to meet your most stringent powder specifications for electronic applications.

In addition to the products pictured above, INCO SPP has available the following high performance powder products. Novamet Conductive Nickel Spheres, particle size (FSSS) 8-9 microns, apparent density 3.2-3.5 g/cc, surface resistivity 1.0 ohms per square. Novamet 525 Conductive Nickel Pigment, screen mesh 100% minus 400, particle size 3.2 microns, 0.65 BET surface area m^2/g, surface resistivity 0.35 ohms per square. Silver Coated Nickel Flake, 15% Ag, 2.6 g/cc apparent density, particle size (FSSS) 15 microns, screen mesh 99% minus 200, surface resistivity 0.04 ohms per square.

Magnetic ferrites and surge arrestor applications also use our specialized range of nickel oxides. High Purity Black Nickel Oxide, 77.2% Ni, BET 75 (m^2/g) particle size (FSSS) 5.2 microns, minus 325 mesh 99% plus. Green Nickel Oxide, 78.5% Ni, BET 3 (m^2/g) particle size 1.6 microns, −325 mesh 100%.

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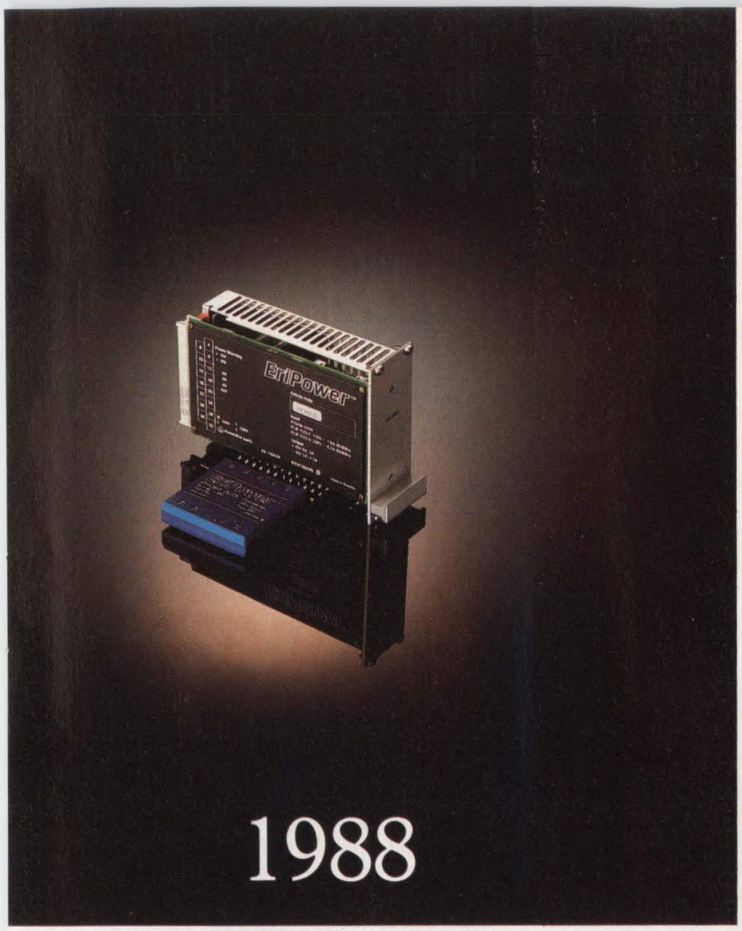
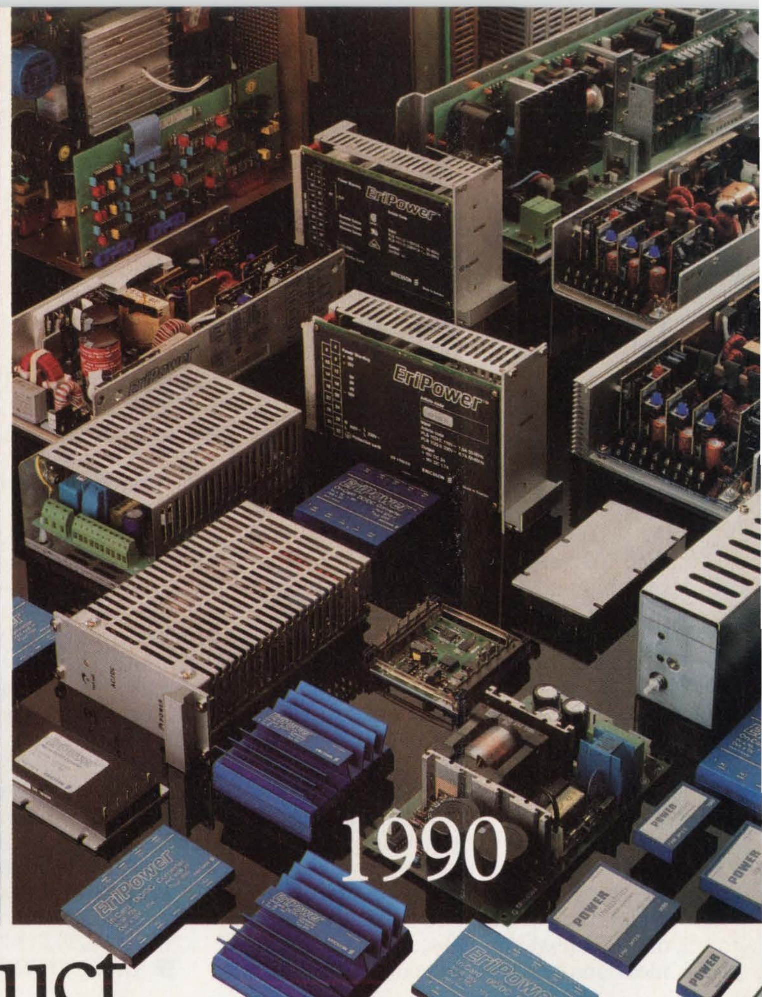
15/Fl Wilson House, 19-27 Wyndham Street Central, Hong Kong

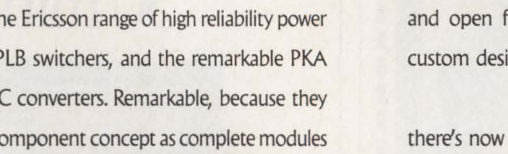
CIRCLE 87



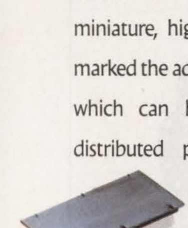


The power product range from Ericsson has been putting on weight recently

Right up to 1988, the Ericsson range of high reliability power supplies was limited - Eurocard PLB switchers, and the remarkable PKA miniature, high frequency DC/DC converters. Remarkable, because they marked the advent of the power component concept as complete modules which can be used to realize distributed power architecture.



The new PLY: versatile 150-400W open frame switchers



PKY: 30-200W modules have standard pinning/ footpring (Note: Only available in Europe)

Since then things have changed. Today the EriPower™ range includes DC/DC converters from 0.3Watts to 200Watts. And most of them are also designed to be paralleled for system upgrading.

What's more, the AC/DC power supply range covers 60 Watt to 400 Watt requirements with Eurocard and open frame power supplies. When necessary, there's even a full custom design facility for high volume users.

In short, the EriPower™ range has put on a lot of weight, and there's now a product for almost every need.

But one or two things haven't changed. For example, EriPower™ power supplies still meet or exceed international standards for safety and RFI/EMI emission. They all represent the very latest technology of their kind. And they all feature the demanding MTBF performance you'd expect of products from Ericsson - over 200 years in some cases. After all, as a part of one of the world's leading telecommunications companies, reliability is a vital part of our culture.

As you've probably realized, the EriPower™ range is expanding fast. Simply get in touch and we promise to keep you up to date, as we continue putting on weight.

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CIRCLE 97

ERICSSON

REAL-TIME COMPRESSION BOOSTS DISK DATA SPACE

Available in either chip, board, or software form, the Stacker, a real-time lossless data-compression technology, promises to effectively double or triple the amount of disk-storage space. Designers can buy the 9703 or 9704 compression coprocessor chip and embed that chip into systems of their own design. Or, they can buy Micro-Channel-Adapter or AT-compatible cards that can be inserted into an existing system. And for systems that don't have a spare slot, a software-only version can also be had.

The 9703 and 9704 coprocessors are similar, but the first can deliver a throughput of 1 Mbyte/s, while the latter ups the average throughput to 1.8 Mbytes/s. Both chips implement QIC-122, a standard for 1/4-in. data-cartridge tape drives, but can also be used on SCSI host adapters, in data-communications systems, helical-scan 4- and 8-mm tape drives, and other systems. All versions of Stacker are 100% compatible with both DOS 3.x and 4.x and work with environments such as Windows 3.0., disk-caching programs, and utility programs.

Also available is a developer's kit that allows engineers to integrate the chips into new system designs. Purchasers of the kit, which sells for $10,000, get a royalty-free license to redistribute the Stacker device driver when used in conjunction with the 9703 or 04. Both chips are housed in 100-lead plastic quad-sided flat packages. In 1000-unit lots, the 9703 and 04 sell for $35 and $45, respectively. A 9703-based board sells for $229, and the software-only version sells for $129. All versions are available from stock.

Stac Electronics, *5993 Avenida Encinas, Carlsbad, CA 92008; Gary Clow, (619) 431-7474.* **CIRCLE 373**

■ *DAVE BURSKY*

FAST FIFOS ACCESS DATA IN 25 NS, PACK 4 KWORDS

With an access time of just 25 ns, the CY7C433 FIFO register offers the shortest access time of any 4-kword-by-9-bit circuit. And, thanks to the use of a submicron manufacturing process, the chip is housed in a space-saving 300-mil-wide 28-pin package, rather than one that's 600 mils wide. A 600-mil-wide version, the CY7C432, is also available. Read and write operations are asynchronous at either port, permitting separate clock signals to control each port. The FIFO register also includes Full, Half-Full, and Empty flags, and has Expansion-in and Expansion-out signals to allow multiple registers to be cascaded. In addition to plastic and ceramic DIPs, the chip is available in leadless ceramic chip carriers, plastic leaded chip carriers and small-outline J-leaded packages. In 100-unit lots, the plastic DIP version sells for $89.30.

Cypress Semiconductor Corp., 3901 North First Street, San Jose, CA 95134; (408) 943-2600. **CIRCLE 374**


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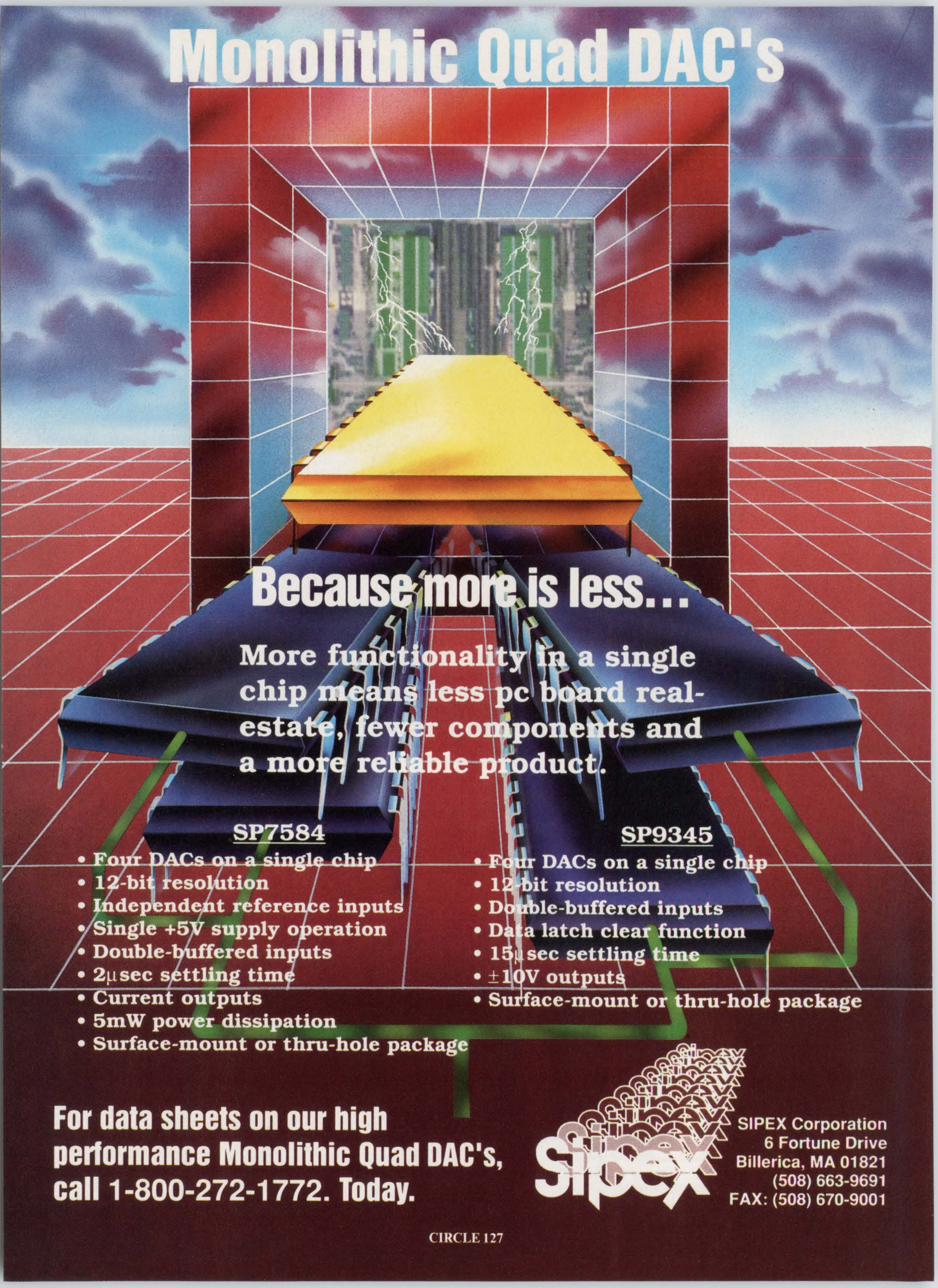

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CIRCLE 127

FULL FFT PROCESSOR FITS IN SINGLE CHIP

Containing all the data memory as well as all the necessary computational resources, the PDSP16510 fast-Fourier transform processor is a complete subsystem on a CMOS chip. The Plessey processor employs 16-bit data and coefficient values and can perform computations with block-floating-point math to improve the chip's dynamic range. A complex FFT with 1024 points can be computed by the chip in just 96 μs, when the chip is clocked at 40 MHz. That computational result is equivalent to 450 MIPS of CPU throughput.

Either a Hamming or Blackman-Harris window operator can be internally applied to the incoming real or complex data. The operator values are calculated internally and do not require an external ROM, nor do they incur any time penalty. There are three internal control units in the FFT chip that, in the continuous mode, overlap the new data to be loaded with the present data to be transformed, and the previous results to be dumped. The user can choose to overlap the data blocks by 0, 50 or 75%. The FFT processor operates from a 5-V supply and comes in an 84-lead pin-grid array. In sample quantities, the PDSP16510 sells for $1195. Production quantities will be ready next spring.

Plessey Semiconductors Corp., Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, CA 95066; Steve Brightfield, (408) 438-2900. **CIRCLE 340**

■ DAVE BURSKY

HIGHLY INTEGRATED VGA CHIP TRIMS BOARD SPACE

Designed to directly reside on 80286, 80386SX and 80386DX CPU buses, the HT216 VGA controller reduces the printed-circuit-board space and chip count in cost-sensitive systems. Housed in a 160-lead plastic quad-sided flat package, the controller can operate at dot clocks of up to 75 MHz and can employ either 64-k-by-4, 265-k-by-4, or 64-k-by-16-bit dynamic memories, depending on the operating modes. Although the chip can operate with inexpensive 100-ns DRAMs, the controller's fast-page-mode capability greatly reduces access time to the screen memory. When running with a 75-MHz dot clock, the chip can provide non-interlaced 1024-by-768-pixel displays with 16 colors and a 72-Hz refresh rate, which minimizes eyestrain. The chip can self-boot from either an 8- or 16-bit external EPROM, which would typically hold the video BIOS. In addition to the video memory, the controller only requires a RAMDAC and the various clock signals. Also on the chip is the 46E8 port, used to add special features to the VGA subsystem. The HT216 is priced below $25 each in quantities of 10,000. Samples will be available in 8 weeks.

Headland Technology Inc., 46221 Landing Parkway, Fremont, CA 94538; (415) 623-7857. **CIRCLE 341**

CIRCLE 107

High-Speed Crossbar Switch Simplifies Bus Connections

Offering four 20-bit-wide input ports and the same number of wide output ports, a BiCMOS crossbar switch gives designers the first chip capable of routing large buses. The SC2001 crossbar has an aggregate switching rate of up to 8 Gbits/s, and provides simultaneous multiple-source to multiple-destination synchronous switching. Organized as 4-ports by 4-ports by 20 lines per port, the Silicon Connections' chip can run at cycle times as short as 10 ns thanks to its BiCMOS construction. The four independent 20-bit-wide input ports can be switched to the four corresponding output ports during each cycle. Each of the input ports can be directed to as many as four output ports, but no output can contain more than one input.

Two modes of output-port addressing are available—input-port priority arbitration or direct-output port-address selection. Each port includes handshake signals that can be used in some arbitration schemes such as in fair queues or round-robin approaches. Multiple crossbar chips can be operated in parallel when data paths wider than 20 bits must be switched. Furthermore, the crossbars can be cascaded when there are more than 4 data paths to be switched.

Inputs and outputs of the chip are ECL 10KH-compatible. Several pins are dedicated for scan testing to permit full user testing in the system. The chip consumes about 7.2 W at 100 MHz. Inside the IC's 235-lead pin-grid package is an aluminum-nitride heat sink to efficiently remove the heat. Samples of the chip are available and sell for $280 in lots of 1 to 99.

***Silicon Connections Corp.**, 6160 Lusk Blvd., Suite C-204, San Diego, CA 92121; (619) 535-0422.* CIRCLE 342

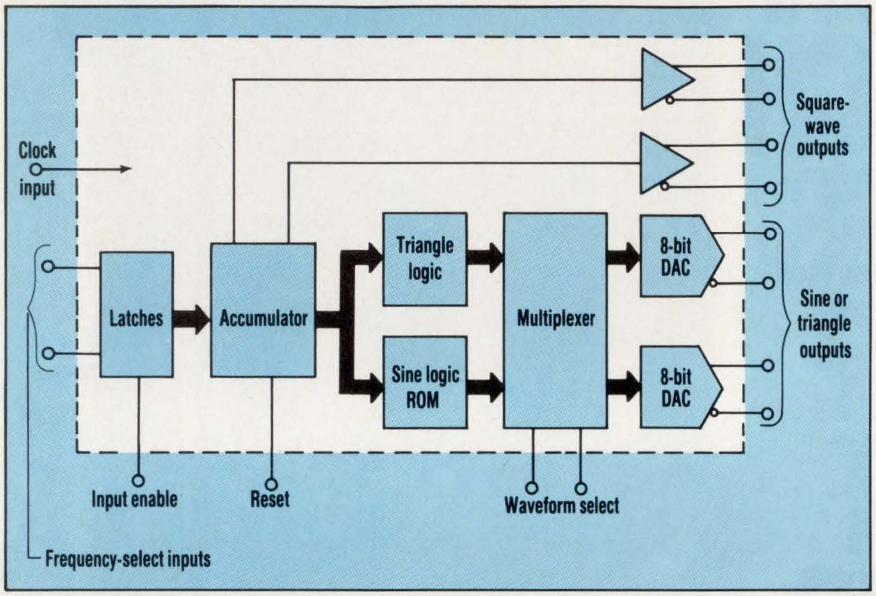
■ *DAVE BURSKY*

Oscillators Enclosed in SMT Packages

A line of surface-mounted crystal-controlled oscillators, designated the VF 315 series, cover the frequency range of 1.5 to 55 MHz. They incorporate TTL and CMOS circuit designs into a packaging format that uses a minimum amount of board space and accommodates automated assembly. Just 0.55 in. long and 0.34 in. wide, the packages have four J-lead surface-mounting terminations on 0.2-by-0.3-in. spacing. The packages are compatibile with high-speed pick-and-place equipment and other automated-manufacturing techniques. A range of available function options includes enable-disable control, and packaging in a tape-and-reel or a conventional platic-tube format. Priced at $3.69 each in quantities of 10,000, the delivery lead time for the VF series of surface-mounted crystal-controlled oscillators is eight weeks.

Valpey-Fisher Corp., 75 South St, Hopkinton, MA 01748; (508) 435-6831. CIRCLE 343

WAVEFORM SYNTHESIZER IC OUTRUNS GAAS EQUIVALENTS



An ECL direct-waveform synthesizer IC from Plessey Semiconductors generates a user-selectable sine-, square-, or triangular-wave output with frequencies up to 500 MHz. It's designed for use in ultra-high-speed switching applications in commercial and military communications and instrumentation systems. The output frequency can be programmed upwards from 1 Hz in 1-Hz steps by means of an externally applied 30-bit word, which yields a 0.5-Hz frequency resolution from dc to 268 MHz, with a 1.074-GHz clock. The fine resolution, coupled with 10-ns switching between frequencies at the maximum clock frequency of 1.6 GHz, makes the SP2002 suitable for use in frequency-agile radio and radar applications.

The chip includes a 31-bit data accumulator, a lookup table for the three waveforms, two 8-bit DACs, and a multiplexer. This integration level eliminates the time delays associated with off-chip connections. Square-wave outputs come directly from the accumulator. A sawtooth waveform from the accumulator is converted to triangular- and sine-wave forms by on-chip logic circuitry and the DACs. The user selects the required waveform through control pins to the multiplexer. Depending on the output option chosen, unused circuits are automatically deenergized to save power.

Inphase, quadrature, true-phase, and complementary-phase outputs are available for all waveforms. The quadrature outputs are useful for carrier-recovery loops in MPSK modems. With a rapid data-update rate which supports frequency steps as fast as 25 ns, the 2002 is also suited for frequency-hopped systems. With all circuits energized, maximum supply current is 1.05 A. The 2002 comes in a 68-lead pin grid array with two threaded studs for attaching a heat sink. The price is $1400 each in lots of 100.

***Plessey Semiconductors Corp.**, 1500 Green Hills Rd., Scotts Valley, CA 95066; Ashi Majid, (408) 438-2900.* **CIRCLE 344**

■ *MILT LEONARD*

QUAD-PORT RAM EASES DSP SYSTEM DESIGN

Containing a total of 16 kbits of multi-access storage, the PDSP16520 has those bits arranged as four 16-bit-wide blocks, each holding 256 words. Each block can be accessed via a pair of 16-bit input buses and a pair of 16-bit output buses, with each memory block accessible from any input or output port. Within any clock period, data can be read from any two of the memory blocks, and new data can be written to any two blocks. Separate read and write address inputs are available. If the host system tries to read and write to the same location, the old data will be read before new data are written. Such an arrangement is a perfect match for digital signal processing operations such as radix-2 butterfly calculations in fast-Fourier transforms, which require two reads and two writes in a single cycle. All address and data lines, as well as control inputs, are fully registered to permit all events to be synchronized to a common system clock, which can run at speeds of up to 20 MHz. Furthermore, the user can program a delay of between 0 and 15 clock cycles before the write operation specified on the input pins actually occurs. That eliminates the need for separate address generators and thus simplifies the support circuitry. The PDSP16520 is immediately available in a 144-lead pin-grid-array package and sells for $295 in lots of 1000.

Plessey Semiconductors Corp., Sequoia Research Park, 1500 Green Hills Rd., Scotts Valley, CA 95066; Steve Brightfield, (408) 438-2900.

CIRCLE 345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CIRCLE 136

CONVOLVER FOR 2D INCLUDES DELAY LINES

Able to modify the center pixel of an 8-by-8-pixel field, depending on the values of surrounding pixels, the Plessey PDSP16488 two-dimensional convolver integrates more features than other convolvers. For starters, in addition the array of multiplier-accumulators, it contains a 32-kbit RAM that can either provide four or eight line delays. The length of each delay can be programmed to suit the application, up to a maximum of 1024 pixels per line. The line delays are physically set up as two groups on the chip and can be internally connected in series, or set up to accept separate pixel inputs, thus permitting either interlaced video or frame-to-frame operations to be handled.

The convolver handles pixel rates of up to 40 MHz and has up to eight internal line stores. With eight line delays, window regions of up to 8-by-8 pixels can be evaluated. The 8-bit coefficients for each pixel value are stored on the chip and are typically downloaded from the host or loaded from EPROM.

The CMOS PDSP16488 is housed in an 84-lead pin-grid array package and sells for $395 in lots of 1000. To help designers evaluate the chip, an IBM PC-compatible add-in card is available from Spectrum Processing Inc., Westborough, Mass. (508) 366-7355), the U.S. office for Loughborough Sound Images, U.K. The board, which sells for $3295, includes the 16488 convolver and picture digitization, a field store, a color look-up table, and video output, all controlled by a graphics-based program running on the host PC.

Plessey Semiconductors Corp.*, Sequoia Research Park, 1500 Green Hills Rd., Scotts Valley, CA 95066; Steve Brightfield, (408) 438-2900.* **CIRCLE 346**

■ *DAVE BURSKY*

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A unique integrated circuit is specifically designed to protect the design and firmware of any printed circuit board from unauthorized copying. When integrated into the hardware of an add-in board, the SentinelChip receives unique data patterns assigned to each manufacturer and built into the firmware by the manufacturer. These data patterns are recognized and answered by the SentinelChip, which uses a proprietary algorithm technique that never provides a fixed response and, thus, cannot be duplicated. The use of scattered data patterns with corresponding responses from the SentinelChip ensures that the security device is in place. An unanswered call renders the board inoperative. It comes in both surface-mount and dual-in-line packages, priced at $19 each for high-volume orders. An evaluation kit containing the chip, software, and instructions is available for $50.

Rainbow Technologies Inc., 18011-A Mitchell South, Irvine, CA 92714; (714) 261-0228. **CIRCLE 372**

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CIRCLE 137

COLOR FLAT-PANEL VGA CHIP SET EASES DESIGN

A trio of chips that control either a color LCD panel or a CRT display integrate almost everything designers need for a minimum-chip-count display subsystem. The chips include the 82C457 VGA flat-panel/CRT controller, the 82C411 color-flat-panel palette and triple digital-to-analog converters, and the 82C401 clock synthesizer. Bringing full-color CRT-like display quality to color flat panels, the 82C457 contains special logic to coax thousands of colors from the color panels.

Able to support multiple flat-panel types, the controller provides full VGA compatability and backward compatibility with all previous video standards. A proprietary vertical compensation scheme in the controller allows application software with smaller resolutions than the physical screen to completely fill the display in all modes. Almost any width DRAM can be used for the screen memory—4-, 8- and even the new 16-bit-wide DRAMs or pseudostatic RAMs can be used.

The companion 82C411 contains the 256-word by 18-bit palette and triple 6-bit converters as well as color-reduction logic, the equivalent of an LM339 voltage comparator, and a current or voltage reference. All those features considerably simplify the design of a VGA subsystem. Similarly, the 82C401 simplifies the timing circuitry, replacing the multiple crystals typically used to generate the video clocks for VGA or EGA as well as extended VGA modes up to a 40-MHz dot clock.

The 82C457 comes in a 160-lead plastic quad sided flat package, while the C411 comes in a 64-lead PQFP, and the C401 comes in a 16-lead DIP or small-outline package. Samples of the chips are immediately available and sell as a set (the C457/411/401 plus the video BIOS) for $86.90 in lots of 1000.

***Chips and Technologies Inc.**, 3050 Zanker Road, San Jose, CA 95134; Keith Angelo, (408) 434-0600.*

CIRCLE 347

■ *DAVE BURSKY*

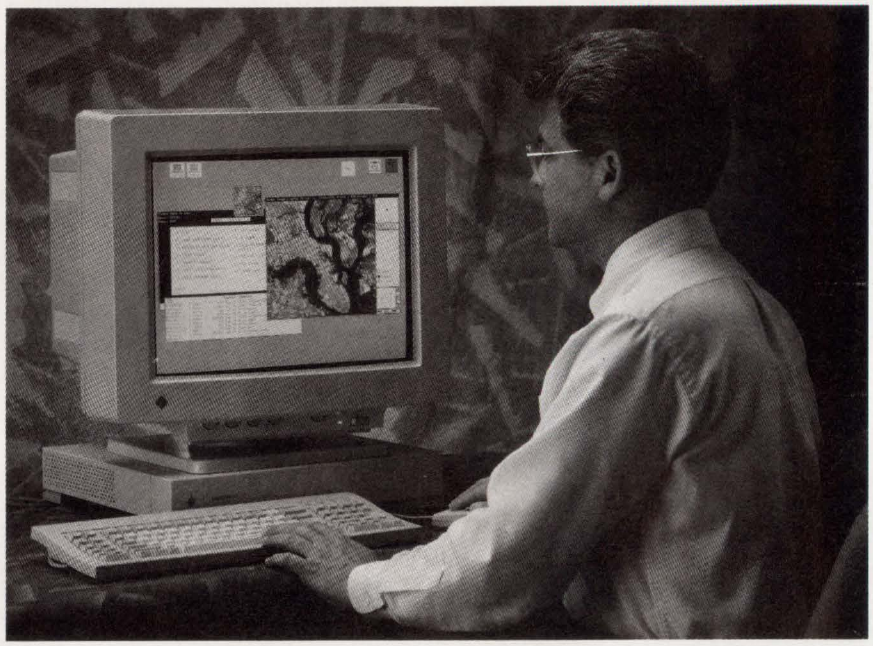
CMOS DAC CONTAINS 256-BY-18-BIT RAM

The first of a new line of data-conversion products for use in personal-computer graphics, the TMC0171, a triple monolithic-CMOS 6-bit DAC, works at 35 MHz and includes a 256-by-18-bit RAM. It is pin-compatible with the Inmos IMS G171 and Brooktree Bt 471. Operating on a single 5-V power supply, the low-power DAC provides 256,000 color choices, color read back, RGB analog output, composite blanking, TTL compatibile inputs, and VGA, EGA, and CGA compatibility. Available off-the-shelf in plastic-DIP (TMC0171N6C) or PLCC (TMC0171R2C) enclosures, the DACs cost $3.20 each in 1000-piece quantities.

TRW LSI Products Inc., P.O.Box 2472, La Jolla, CA 92038; (619) 457-1000. CIRCLE 348

SPARC-BASED WORKSTATIONS BOAST FASTER CPU, BETTER I/O, MORE FEATURES

DAVE BURSKY



Pushing the CPU clock frequency up to 40 MHz, designers at Sun Microsystems have developed their fastest desktop systems to date, the Sparcstation 2 series. These workstations achieve a SPECmark rating of 21 with a throughput of 28.5 MIPS, the highest numbers yet for Sparc-based platforms. Accompanying the release of the workstations are two new graphics accelerators for 3D solids modeling—a mid-range product called the 2GS that fits inside the workstation, and a high-end external "tower" housed subsystem, the 2GT. There's also a server configuration based on the Sparcstation 2 computer. The system consists of the CPU box and two small expansion boxes to hold up to 7.6 Gbytes of Sun-supplied storage and 18 serial ports.

Employing the same pizza-box-like housing as used for previous CPUs, the Sparcstation 2 delivers about twice the performance of the Sparcstation 1+. The new CPU board also sports an improved I/O architecure and cache subsystem to boost system efficiency and achieve a 50% improvement in data transfers. An enhanced DMA controller, for example, now lets SCSI data move synchronously at 4 Mbytes/s and a new software driver permits read/write clustering. Furthermore, purchasers of Sparcstation 1 and 1+ systems can upgrade their systems by swapping the CPU board for a nominal charge.

The base color Sparcstation 2 comes with 64 kbytes of cache for the CPU, 16 Mbytes of RAM, a 207-Mbyte hard-disk drive, the GX graphics accelerator (previously an option on I and I+ platforms), all the standard I/O ports of the previous systems, and the operating system and utilities pre-installed on the disk. A 19-in. monochrome (1-bit pixels), diskless version of the system sells for less than $15,000, while the 19-in. color system with the previously released GX 8-bit color card sells for less than $22,000. The same GX accelerator can now be added to the previously released Sparcstation IPC, which brings the system price up to just under $15,000.

The new graphics accelerators provide 24-bit color with up to eight separate light sources for solids modeling. The 2GS can draw 3D vectors at up to 150,000/s, or 20,000 Gouraud-shaded triangles every second, and includes Z-buffering for hidden-surface removal. The accelerator comes with a low-flicker 76-Hz 19-in. monitor. When bundled with the workstation, the package sells for less than $27,500.

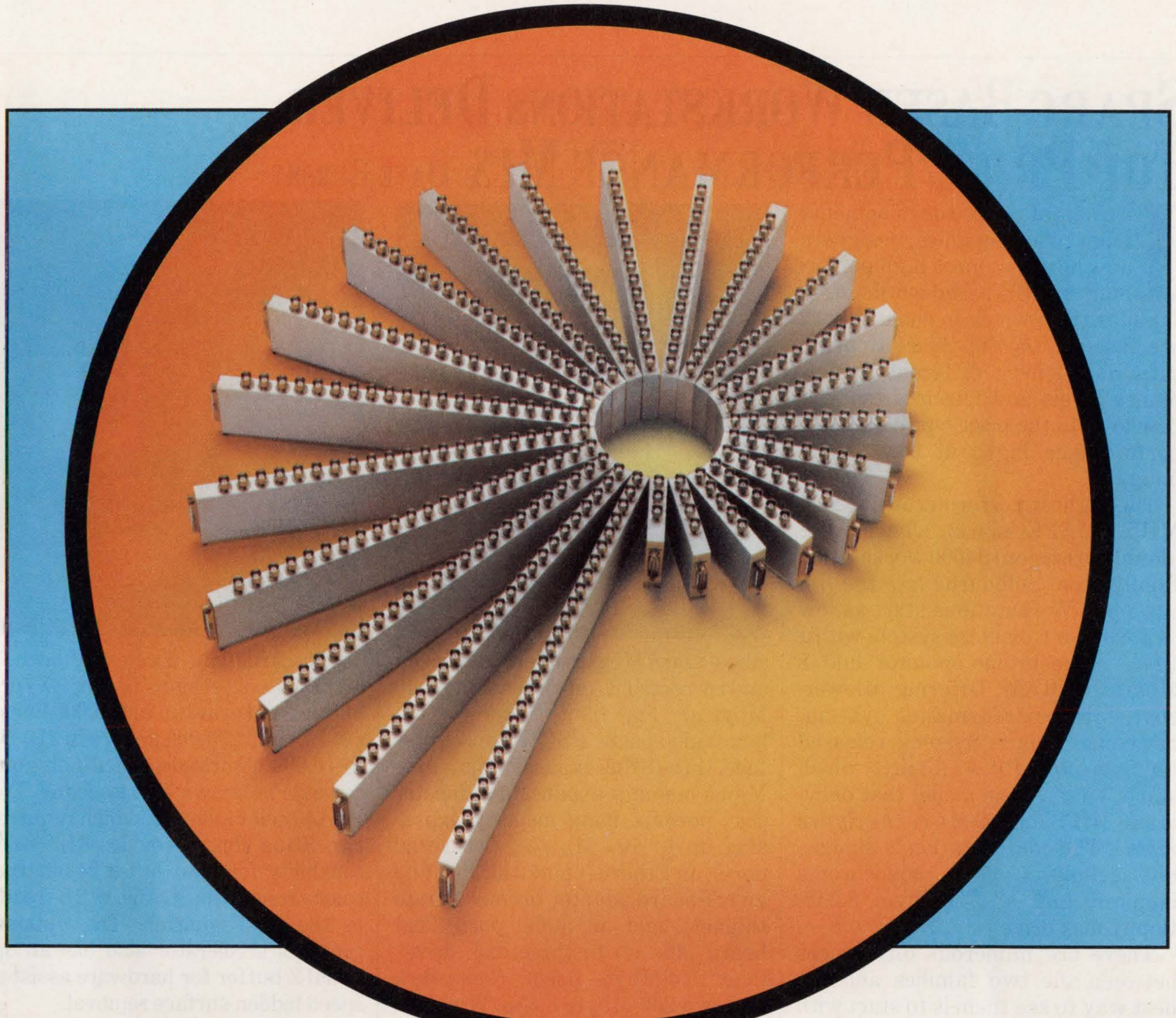
For high-end imaging, the 2GT delivers about five times the drawing speed of the GS and includes a new antialiasing scheme for jag-free image edges. The graphics subsystem gets some its punch from an i860 superscaler processor and nine custom chips to maximize throughput. Advanced software schemes such as a virtual display-list accelerator for standard PHIGS applications lets the system quickly move and redraw images. A 24-bit Z buffer provides realistic quality to the images. Requiring a single SBus slot, the external tower-encased GT sells for $53,000, including the workstation and a 21-in. 1280-by-1024-pixel monitor.

Lastly, the server configuration of the Sparcstation 2 replaces the Sparcstation 1+ as the entry version. The server comes with 16 Mbytes of RAM, a 669-Mbyte SCSI hard-disk drive, a 150-Mbyte tape drive, and a CD-ROM drive. Thanks to the improved I/O of the new CPU board, the server delivers the highest throughput of any comparable unit. The system comes with one SCSI channel. Additional SCSI controllers can be installed in the SBus slots to allow additional storage to be attached, up to a maximum of 7.6 Gbytes of Sun-supplied peripheral storage. Third-party storage could up that level further.

The Sparcstation 2 is immediately available, as is the 2GS graphics accelerator. The 2GT accelerator will be available in the first quarter of 1991.

Sun Microsystems Inc., 2550 Garcia Ave., Mountain View, CA 94043; Mary Swastek, (415) 336-9246.

CIRCLE 349



SPARC-BASED WORKSTATIONS DELIVER TOP PRICE/PERFORMANCE MIX

DAVE BURSKY

In a pair of related developments from two companies, designers now have two more high-performance RISC-based workstation families from which to choose. Both are based on the Sun Sparc architecture but deliver different performance levels and features that set new lows in the price curve and new performance highs at those price points.

The highest performer is the 25.5-MIPS (12 SPECmark), 1.7-MFLOPS (double precision) S4000 workstation family from Solbourne *(see the figure left)*. Workstations start as low as $8995 for a diskless system with a 19-in. monochrome monitor and 8 Mbytes of RAM. Offering a lower-cost, lower-performance system, newcomer Solarix Systems released its Solarix/4 PW+ family, which starts with a base model that delivers 18 MIPS for $6995 *(see the figure right)*. The configuration is similar, but includes a 17-in. monochrome monitor, and a 1.44-Mbyte 3.5-in. floppy-disk drive.

There are numerous differences between the two families and the best way to see them is to start with one as the baseline—the Solbourne S4000.

The S4000 is based on a 64-bit version of the Sparc processor that Solbourne and its development partner, Matsushita Electric Industrial Co. Ltd., Osaka, Japan, described earlier this year at the International Solid-State Circuits Conference. The processor is the first CMOS Sparc chip to contain a 64-bit data path, as well as on-chip floating-point processor, both data and instruction caches, and an MMU with a translation look-aside buffer. Multiple custom chips were also developed to simplify the main processor board. Four custom chips on the board handle memory control, SBus interface, SBus control, and various "glue" logic functions.

The system CPU board contains the RISC processor, the four custom chips, and 8 Mbytes of error-checked and corrected RAM (extendable to 40 Mbytes). For data transfers, the board also packs a SCSI-2 disk interface, three SBus expansion slots, one M-bus memory expansion connector that permits main memory expansion up to 104 Mbytes, two serial ports, an Ethernet port (thicknet and an off-board adapter to convert it to thinnet), and an audio port. That board plus up to three disk drives (one 1.44-Mbyte 3.5-in. floppy-disk and two 200-Mbyte 3.5-in. Winchester-disk drives) and the power supply all squeeze into a 17-by-17-in. case about 5-in. high. The monochrome or basic color display adapter requires one of the SBus slots, and that adapter delivers 1280-by-1024-pixel resolution. System software includes the company's OS/MP Unix operating system which is derived from SunOS, SunView, X Window system, some utilities, and a C-language compiler.

An optional graphics accelerator for 2D and 3D color displays can replace the basic single SBus slot monochrome or color frame buffers. It delivers the same 1280-by-1024-pixel resolution but provides a major improvement in drawing speed thanks to a pair of 32-bit floating-point DSP chips and some custom chips that accelerate the computations.

The cards can accelerate both X and Phigs extensions to X (PEX) primitives and draw up to 450,000 lines/s in 2D, and 200,000 lines/s in 3D. Up to 10,000 Gouraud-shaded polygons can also be drawn every second. The SGA40 color adapter, which requires two SBus slots, provides 8-bit color capability for now, but a 24-bit true-color version, the SGA50, will be ready in the first quarter. The optional graphics accelerator also has an optional Z buffer for hardware assist to speed hidden-surface removal.

In addition to the diskless base configuration, Solbourne offers a 19-in. monochrome system with a 200-Mbyte hard-disk drive, and a 1.44-Mbyte 3.5-in. floppy-disk drive for $10,495. Several color options are available—with a 16-in. monitor, 200-Mbyte hard-disk drive, and basic color frame buffer.

The system sells for $12,995. The same CPU hardware but with a 19-in. monitor, a second 8-Mbytes of main memory, and the SGA40 accelerator costs $2500 more.

Taking a slightly different architectural approach, Solarix put the key CPU building blocks on a single M-bus-compatible palm-sized module (called the A module). To upgrade a system, that module can be removed and replaced with a higher-speed A module.

In such a way the company ex-

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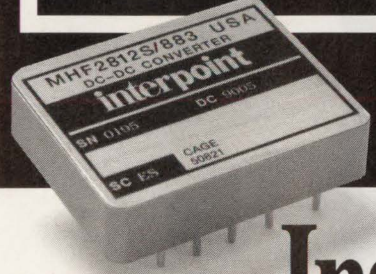

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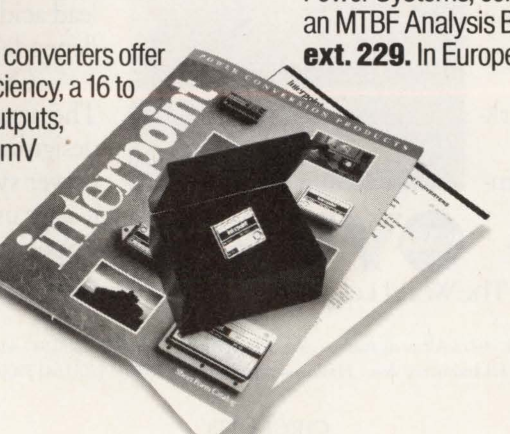

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CIRCLE 202

pects its systems to be able to deliver throughputs from 18 to 40 MIPS with minimal upgrade costs. The first CPU A module is based on the 25-MHz Cypress Semiconductor Sparc processor, 64 kbytes of off-chip cache, and a Sparc reference MMU. The monochrome or color display subsystems provide 1152-by-900-pixel resolution—the same resolution as Sun Microsystems provides on its own base workstations.

The A module employs a proprietary programming scheme the company calls FlexScale. The programming scheme permits the SBus interface to be programmed to operate at a different clock than that of the CPU subsystem. That allows slower SBus cards to be used with higher-speed CPUs.

The system's main logic board holds 8 to 32 Mbytes of RAM, both thick and thin Ethernet ports, two serial ports, one Centronics port, SCSI drive controller, and a floppy-disk drive interface. Housed in a mini-tower cabinet that has six drive bays, the system has plenty of room for expansion. Additional internal RAM can be added via the company's optional SIMM modules, which can boost the system capacity from 64 to 128 Mbytes.

The Solarix operating system is a licensed version of the SunOS Unix operating system and thus allows the hardware to run all Sun-compatible software. Expansion options such as a 104-Mbyte internal SCSI hard-disk drive or a 19-in. monochrome or 17-in. color monitor are optionally available.

The hard-disk drive adds $1000 to the price tag, while the 19-in. monochrome monitor ups the price by about $800. A full 19-in. color system with a 104-Mbyte hard-disk drive and 8 Mbytes of semiconductor RAM goes for $10,995.

Solbourne Computer Inc., 1900 Pike Rd., Longmont, CO 80501; Brian Doyle (303) 772-3400. **CIRCLE 375**

Solarix Systems Inc., Div. of Able Technologies Inc., 46791 Fremont Blvd., Fremont, CA 94538; Pamela Sloane, (415) 659-1544. **CIRCLE 376**

386SX PC TAKES HALF THE SPACE OF TYPICAL PCS

The Infinity desktop computer, from Falco Data Products Inc., is an 80386SX-based computer that takes up half the desk space of standard PCs. It measures a paltry 13.6 by 10 by 2.75 in. Another feature of the machine is that nearly all peripheral functions reside on the motherboard. But it does contain two 3/4-length 16-bit expansion slots. The slots are intended for local-area-network, facsimile, or modem cards.

The zero-wait-state system contains a socket for an 80387SX math coprocessor. It also comes standard with 1 Mbyte of RAM, expandable to 2, 4, or 8 Mbytes. The Falco VGA design includes the Paradise chip set and supports all standard and extended VGA modes including 640 by 480 pixels in 16 colors with 256 kbytes of DRAM. With the optional 512 kbytes, additional modes can be supported, up to 1024 by 768 pixels.

The Infinity PC uses low-power components and a convection-cooled case. And it incorporates a virtually silent cooling fan to eliminate the hum associated with standard PCs.

Four configurations are available. The first, a diskless model, sells for $1170. A 1.44-Mbyte, 3.5-in. floppy-disk system costs $1555. The PC with a 40-Mbyte hard disk is priced at $2315, while a 100-Mbyte hard disk pushes the price to $2765. The systems are compatible with DOS 4.01 and all OS/2 software. Optional color or monochrome monitors are also available from Falco.

***Falco Data Products Inc.,** 440 Potrero Ave., Sunnyvale, CA 94086; (408) 745-7123.* **CIRCLE 351**

■ *RICHARD NASS*

MILITARY GETS RUGGED 15.8-MIPS SPARCSTATION

Based on the Sparcstation 1+ CPU from Sun Microsystems, the Codar Technology 300M Sparcstation can deliver 15.8 MIPS of throughput in a rack-mountable cabinet. To complement the workstation, Codar has also developed a ruggedized 19-in. multi-sync monitor with 1280-by-1024-pixel resolution, a ruggedized keyboard and trackball, and a tough, Tempest-tested system chassis. The 300M includes shock and vibration isolation for the CPU and up to two full-height or four half-height 5.25-in. removable SCSI peripherals, which provide up to 2 Gbytes of internal storage. A total of 10 Gbytes of on-line storage can be employed by adding additional drives to the external SCSI port.

Operation of the system is specified over a temperature range of 0 to 50°C, per Mil-Std.-810D. Up to 20 Gs of shock, 3.6 Grms or random vibration, and 2.5 Gs of sinusoidal vibration can be tolerated by the system during operation. Mean-time-between-failures for the system is rated at least 21,500 hours through the extensive use of hermetically packaged ICs, military-grade componets, conformal coatings, and Mil-Spec connectors. The 300M Sparcstation is certified to Mil-Std.-810D for shock, vibration, temperature and humidity; Mil-Std.-461B/Procedure A4; and NACSIM 5100A (Tempest) for EMI. A specially designed power supply lets the system also meet the power and transient requirements of Mil-Stds.-1399, 704D, and 5400T.

Extensive built-in-test features were also added via the company's proprietary system monitoring board which reports the status of temperature, ac and dc power, date, time, and fault conditions on a 16-character front-panel display. With that data, service time can be kept to less than 30 minutes. Prices depend on options and test conditions and delivery is 90 to 120 days.

***Codar Technology Inc.** 2405 Trade Centre Ave., Longmont, CO 80503; (303) 776-0472* **CIRCLE 352**

■ *DAVE BURSKY*

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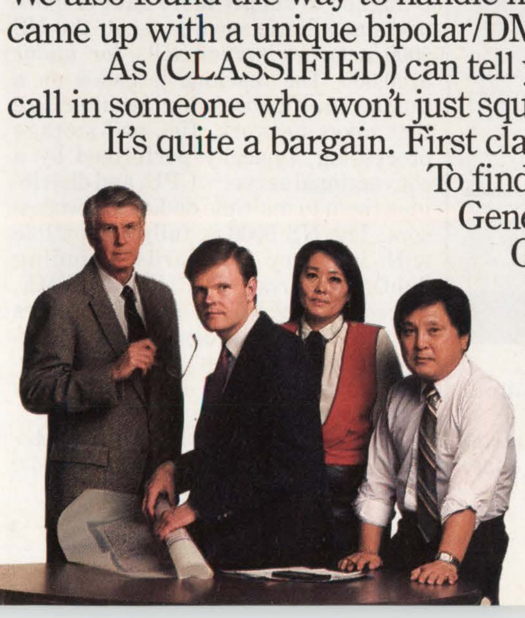

To find out more, contact Silicon General, 11861 Western Avenue, Garden Grove, CA 92641.
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CIRCLE 214

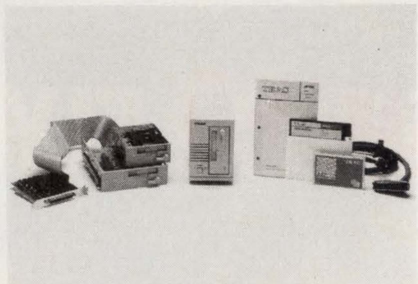
TAPE-BACKUP DRIVES TRANSFER DATA AT 7 MBYTES/MIN

A family of tape-backup systems from Teac America Inc. can back up 100 Mbytes of data in under 15 min. The TurboTape products consist of complete systems that require no additional parts or software when used with PC/XT/AT or compatible computers.

The family includes two internal models, the Mach 5 and 7, and an external version, the Mach 7X. The Mach 5 holds 60 Mbytes, while the other two each hold 160 Mbytes and feature a data-transfer rate of 7 Mbytes/min. All three drives come with a host interface card, software, cables, and manuals. The internal versions also come with mounting hardware. The internal drives can fit into either a 3.5- or a 5.25-in. form factor.

The tape drives are built with all mechanical parts resident within the drive, rather than in the tape like similar drives. Twin motors and servo-controlled circuitry precisely manipulate the relative speeds of the tape's take-up and supply reels to control the tape's speed, tension, and positioning.

The drives also feature dual-gap ferrite recording heads that supply dura-



ble, error-free performance using a read-after-write data-verification capability. Hard-error rates are restricted to a maximum of one per every 10^{14} bits.

For networking applications, the drives' software has a queuing feature that enables files that are active during back-up to be automatically reported and queued for a retry at the end of the back-up session. Network security is supported through multilevel password protection that limits access.

The Mach 5 and 7 are priced at $1095 and $1395, respectively. The 7X costs $1695. All are available now.

***Teac America Inc.**, 7733 Telegraph Rd., Montebello, CA 90640; (213) 726-0303.* **CIRCLE 357**

■ *RICHARD NASS*

PUSH SPARCSTATION TO 65 MIPS

Designed as an addition to Sun's SparcStation, the SkyStation, from Sky Computers Inc., accelerates existing applications without requiring any source-code modification. For under $10,000, the SkyStation increases performance to 65 MIPS. The accelerator has the same dimensions and appearance as the SparcStation, and it easily fits above or below the workstation. It simply plugs into the computer.

The SkyStation, built with both the Intel i860 and i960 processors, is fully compatible with the SunOS operating system. By using enhanced Fortran and C compilers, the SparcStation reaches levels not previously attainable. Appropriate applications include simulation, modeling, finite-element analysis, seismic analysis, and fluid dynamics. The maximum-memory level is boosted to 256 Mbytes. Because an entire application can run on the SkyStation, the SparcStation's 5-Mbyte/s SCSI-2 transfer rate isn't affected. Available now, the SkyStation starts at

$9550 with large-volume discounts available.

Sky Computers Inc., 27 Industrial Ave., Chelmsford, MA 01824; (508) 250-1920. **CIRCLE 358**

DISK DRIVES SHRINK TO 2.5 IN.

Portable computers just became lighter with the Go-Drive series of 2.5-in. hard disk drives. The two-member family is also suitable for noncomputer storage applications, such as laser printers and fax machines. The drives, with formatted storage capacities of 42 or 84 Mbytes, contain embedded SCSI or PC/AT bus controllers. The disks' average seek time is 19 ms. Their maximum data-transfer rate is 4 Mbytes/s. The drives offer multiple power-saving

modes (0.1 W in sleep mode) and a high resistance to shock, as well as an MTBF of 80,000 power-on hours. Evaluation units of the 42-Mbyte drive will be available in January, with volume production slated to commence in March. It will sell for $395. The 84-Mbyte unit, priced at $595, will be available in mid 1991.

Quantum Corp., 1804 McCarthy Blvd., Milpitas, CA 95035; (408) 432-1100. **CIRCLE 359**

MULTIPROCESSING SERVER COSTS UNDER $100,000

Designed to supply more data to more users at a lower cost-per-seat, the NS 5000 network server sells for under $100,000. The machine is based on a unique multiprocessing architecture that takes network, file, and storage processing, typically performed by a conventional server's CPU, and distributes them to multiple dedicated processors. The NS 5000 is fully compatible with industry standards including SunOS, Ethernet, TCP/IP, and VME. Priced at $99,900, the server comes with 663 Mbytes of formatted disk storage and two Ethernet ports. More storage and ports can be added later. It is available now.

Auspex Systems Inc., 2952 Bunker Hill Lane, Santa Clara, CA 95054; (408) 492-0900. **CIRCLE 360**

CIRCLE 118 →

ACCELERATOR BOARD OFFERS 240 MFLOPS

Sun Microsystems' SparcStation 330VX and 470VX visualization workstations house the VX accelerator board that offers 40 MIPS and 60 MFLOPS. A multiprocessor MVX board can be added to boost performance to 160 MIPS and 240 MFLOPS. The VX accelerator contains a 40-MHz Intel i860 microprocessor. It features a 16-Mbyte, 32-bit frame buffer for image display and an 8-bit frame buffer that's used to display Sun's OpenWindows environment. The board integrates the output of these two buffers for display on a 21-in. high-resolution monitor. The MVX version adds four i860 processors, each with 4 Mbytes of memory. Either board can transfer data at a rate of 320 Mbytes/s. The SparcStation 330VX and the 470VX sell for $55,900 and $86,900, respectively. Or the VX can be purchased separately as an add-in option to all deskside SparcStations and high-end SparcServers for $24,000. The MVX board can than be added for $30,000. Shipments will begin in March of next year.

Sun Microsystems Inc., 2550 Garcia Ave., Mountain View, CA 94043; (800) 821-4643 or (800) 821-4642. CIRCLE 361

3.5-IN. DRIVE PACKS RECORD 535 MBYTES

With a maximum storage capacity of 535 Mbytes, the LXT-535, a 3.5-in. hard-disk drive, gives designers the most disk storage in a 3.5-in. format. The multiplatter drive can also have one platter removed to offer a still impressive 437 Mbytes of storage. The drives have an average seek time of 12 ms for read operations, 13 ms for writes, and a track-to-track seek time of 3 ms. An embedded SCSI controller lets the drives deliver 5 Mbytes/s in the synchronous-transfer mode and 3 Mbytes/s in the asynchronous mode. Optionally, an AT-interface version of the drive provides data at 4 Mbytes/s. SCSI command overhead is less than 600 μs and the AT bus overhead is about half that number. The drives weigh in at about 2.2 lbs. and dissipate about 11 W. They are also format-compatible with the company's previous LXT family members, the 200, 213, and 340. Volume prices for the drive start at $1450 for the LXT-535 and $1250 for the LXT-437. Samples are immediately available, with volume deliveries expected to begin in early 1991.

Maxtor Corp., 211 River Oaks Pkwy, San Jose, CA 95134; Lisa Sklar (408) 432-1700. CIRCLE 362

OPTICAL DRIVES USE REMOVABLE 3.5-IN. MEDIA

The Most RMD series of optical disk drives, packaged in a industry-standard 5-1/4-in. half-height form factor, use removable, rewritable 3.5-in. media. The media can hold 128 Mbytes of data, with a shelf life of more than 10 years. The optical drives offer access times significantly faster than other magneto-optic drives and many fixed magnetic disks. The average seek time is rated at 35 ms. A unique short seek-scan function makes data within a 128-track band accessible within 9 ms. The data-transfer rate is 512 kbytes/s, with SCSI burst transfer rates of 1.5 Mbytes/s in asynchronous mode and 3 Mbytes/s in synchronous mode.

The drives possess a unique split-optics positioner that also helps to shorten the seek time. Data security is enhanced by a software-controlled media interlock command that prevents premature media removal. An internal user-configurable EEPROM is available to customize specific drive functions. The drives' MTBF is better than 30,000 power-on hours. The drives are available now and prices depend on configuration and quantity. The optical media sells for about $120.

Most Inc., 11205 Knott Ave., Cypress, CA 90630; (714) 898-9400. CIRCLE 363

TRANSPUTER CARD INTERFACES NETWORKS

A credit-card-sized module provides an interface between parallel computer networks and up to seven peripherals devices, all connected via a standard SCSI bus. The IMS B422 SCSI TRAM includes a 20-MHz 16-bit transputer processor and 64 kbytes of two-cycle static RAM. The transputer provides local processing and control. Four 20-Mbits/s communications links allow direct connection to larger transputer networks. The transputer implements connection to the SCSI bus, allowing common SCSI sequences to be carried out without processor intervention. Low-level software interfaces for initiator and target modes permit the IMS B422 to act as a host-computer system interface or target-peripheral interface. In the initiator mode, interfaces permit Common Command Set SCSI commands to be built and executed by a specified SCSI target.

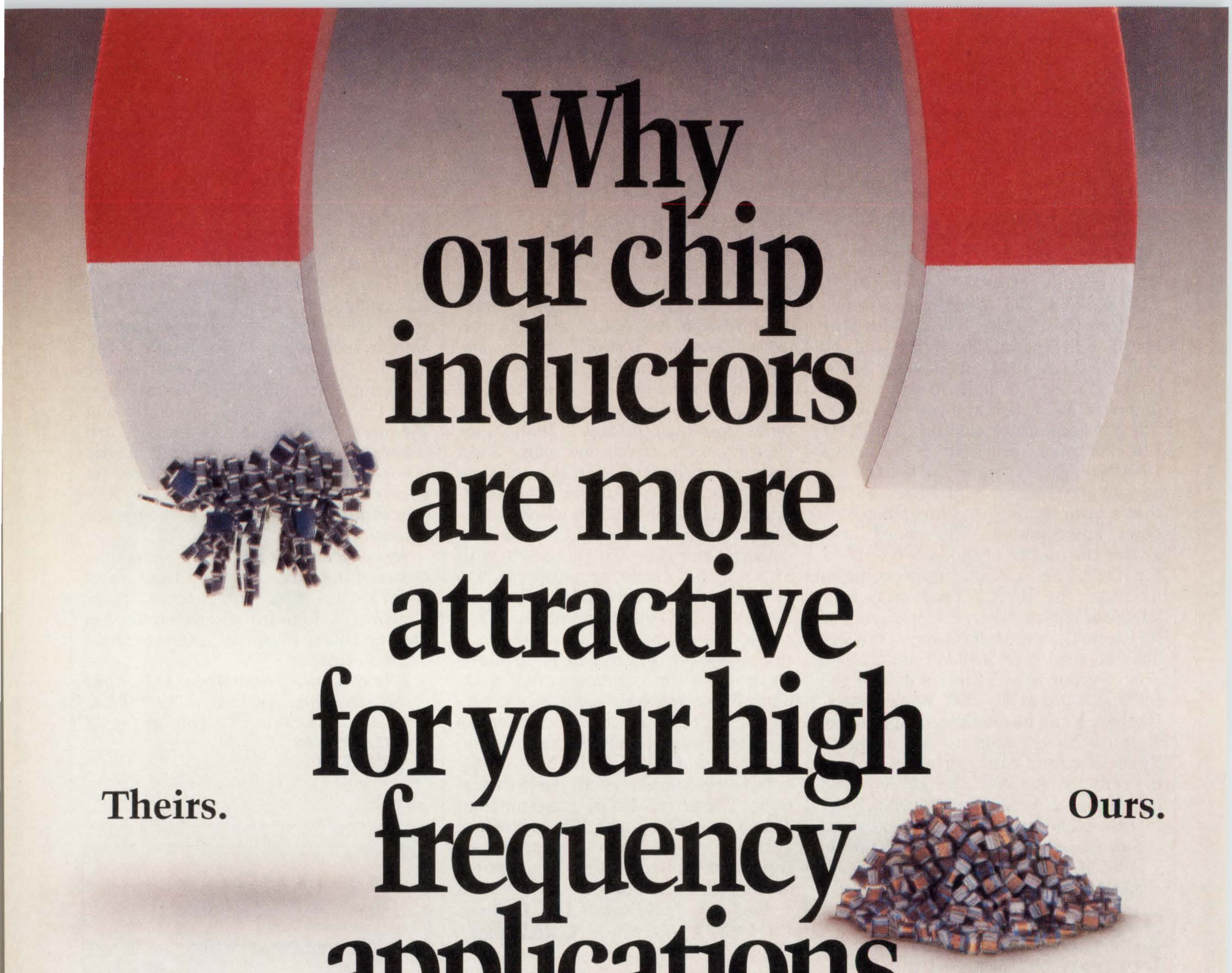
INMOS Ltd, 1000 Aztec West, Bristol BS12 4SQ, United Kingdom. Telephone: +44 (0)454 616616. CIRCLE 364

TOUCH SCREEN REPLACES MOUSE

Macintosh personal-computer users can replace their mouse-pointing devices with a touch-screen produced by Ellinor Technology Ltd of Reading England. The Touchstar screen fits over the computer's screen. It has two layers of conductive glass, one rigid and the other flexible. The two layers are separated by an array of small plastic insulators. When the top layer is pressed against the bottom layer, X-Y coordinates of the point of pressure are sensed.

A controller card and software driver make the screen self-configure and calibrate itself on computer startup. Features include full mouse emulation and the ability to run all software without modification.

Ellinor Touch Technology, Arkwright Rd., Reading, Berkshire, RG2 0EA, United Kingdom. Telephone: +44 (0)734 311066. CIRCLE 365



The point of this little demonstration is that Coilcraft surface mount inductors are made of ceramic. A decidedly non-magnetic material.

Most other chip inductors are made of ferrite. Which is great for demonstrating the principles of magnetism, but not so hot for high frequency magnetics.

Take self resonance, for example. SRFs on our coils are up to 3 times higher than equivalent ferrite chips. And located a safe distance away from your operating frequency.

The actual inductance you'll get with Coilcraft chips at higher frequencies is very predictable and consistent. Not so with ferrites. Beyond the test frequency, their inductance curves rise steeply and vary significantly from part to part.

Coilcraft ceramic chips also have a low temperature coefficient of inductance: +25 to +125 ppm/°C, depending on inductance. TCLs on ferrite chips are often two to four times higher!

And if you need close tolerance parts, we offer even more advantages. Thanks to our computer-controlled manufacturing and ceramic's neutral properties, it's easier for us to make 5% or 2% parts. We can even production-test at your operating frequency! Other chip makers have to cope with ferrite's permeability variations, so their yields are lower. Which means delivery can be unpredictable.

So next time you're selecting surface mount inductors, forget the ferrite and stick with Coilcraft ceramic chips.

For complete specifications and information on our handy Designer's Kits of sample parts, circle the reader service number. Or call **800/322-COIL**.

CIRCLE 153

See our catalog in Vol. A, Section 1800
eem/electronic engineers master

Coilcraft

1102 Silver Lake Rd., Cary IL 60013 800/322-COIL Fax 708/639-1469

FIRST, NEGATIVE, LOW-DROPOUT LINEAR REGULATOR HANDLES 3 A

Now for the first time, you can get a low-dropout (LDO) linear regulator that can provide negative voltages. The LT1185 from Linear Technology can control up to 3 A providing an output voltage between 2.5 and 25 V. Voltage drop across the npn pass transistor is a maximum of 1 V at 3 A, and just 370 mV at 500 mA. The accuracy of the chip's internal reference permits setting the output voltage to within 1% accuracy with two resistors.

Another first for an IC regulator, the LT1185 offers a user-adjustable current limit. Typically, the current limit of earlier 3-A regulators is set at 5 A which can cause a factor-of-two overload on input devices such as the transformer and diodes.

The ability of the designer to program the maximum current of the LT1185 (with a single 1/8-W resistor) to just over the current needed by the load minimizes potential stress on the input components. Additionally, the device can shutdown by bringing the current-limit programming pin to ground. If no current limit is programmed, an internal current limit kicks in to prevent self-destruction. The LT1185 operates on power dissipation, so with less than 10 V across the pass transistor, it allows 3 to 4 A to flow. However, if the drop increases to 30 V, it limits the current to no more than 1 A. Thus under some conditions, the internal limit can override the programmed limit. The regulator is also protected by thermal shutdown.

Line and load regulation run 0.3% and 0.01%/V maximum, respectively. The 1185 can also operate as a positive low-dropout regulator from a floating power source such as a multiple-output switching supply. In that case, the negative line is grounded and the output taken from the pin that would be normally grounded. The LT1185 comes in 4-pin TO-3 cans for military applications and 5-lead plastic TO-220 packages rated for 0 to 125°C. In quantities of 100, the latter goes for just $3.70 each.

***Linear Technology Corp.**, 1630 McCarthy Blvd., Milpitas, CA 95035-7487; Bob Scott. (408) 432-1900.*

CIRCLE 366

■ *FRANK GOODENOUGH*

LOW-COST UPS SUPPLIES UP TO 3 KVA

The 2000 series of uninterruptible power supplies provides continuous, low-cost backup protection for small multiuser minicomputers, LANs, and clustered microcomputers. Units feature a no-break, on-line design that eliminates the risk of inverter switching, thereby providing constant, reliable power. Models are available with ratings from 2 to 3 kVA and offer an RS-232-C interface, I/O plug and receptacle configurations, a remote emergency power-off interface, and automatic circuit breakers. Prices range from approximately $3500 to $5000.

Deltec Corp., 2727 Kurtz St., San Diego, CA 92110; (619) 291-4211.

CIRCLE 369

CORRECTION

Pricing for Powercube Corp.'s model 28DC515-150 dc-dc switching regulator module was stated incorrectly on p. 118 of our Sept. 13 issue. The price should read $1283 in quantities of 100.

ICS POWER DISK DRIVE HEAD POSITIONERS

Designed to drive head-positioning motors in 3.5- and 2.5-in. disk drives for portable PCs, Elantec's EL2026 and EL2027 can qualify as "smart-power" ICs. Their class-AB linear H-bridge outputs control 1.25 W off a 5-V rail.

The output stage of the EL2027 is a complementary H-bridge; that of its lower-cost sibling holds just the npn transistors—low-cost pnps are added externally. Otherwise, the two ICs are virtually identical. Features include a total harmonic distortion of 1%, a "park" circuit that runs off the motor's back-emf, and a low-voltage detector for the 5-V supply that shuts off the output and actuates the "park" circuit. Additionally, gain can be changed by a factor of 4 to optimize "track" and "seek" modes. When not in use, the ICs have a sleep mode available. In their 28-pin SOIC and in 1000-unit lots, the EL2026 and EL2027 go for $5.95 and $6.95 each, respectively.

Elantec Inc., 1996 Tarob Ct., Milpitas, CA 95035-6824; (408) 945-1323.

CIRCLE 367

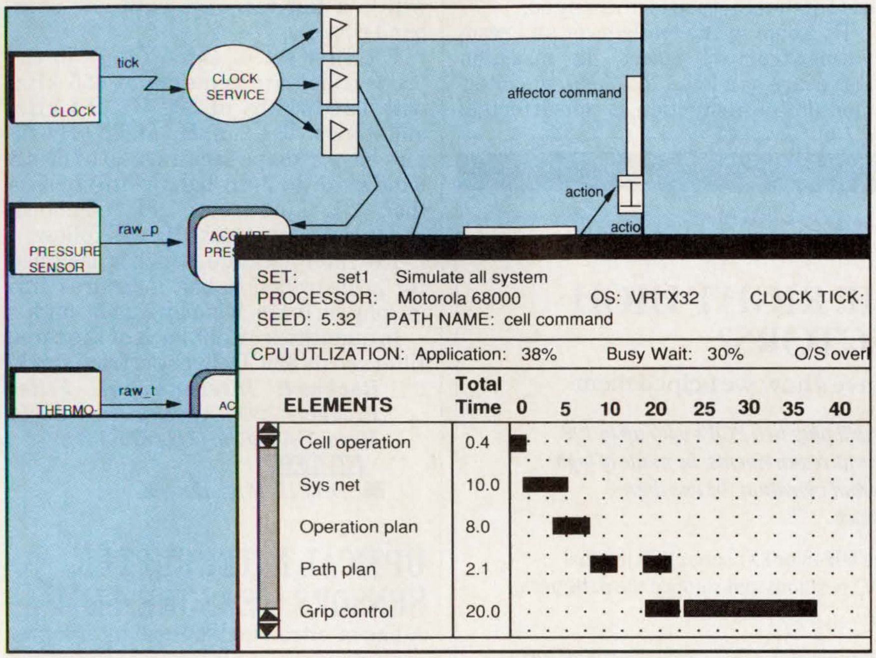
SCHOTTKY DIODES SWITCH IN UNDER 100 PS

Dual Schottky-barrier diodes from Zetex Ltd, Oldham, can switch in less than 100 ps. Designed for rf switching and fast protection, three versions are available, all in surface-mount packaging. All feature a breakdown specification of 70 V and 2 pF capacitance. Electrical characteristics are identical with reverse-leakage current of 200 nA or less, and forward-current handling of 15 mA maximum. But their interconnection varies. The BAS70-04 is a series pair while the BAS70-05 is a common-cathode device. The BAS70-06 has a common-anode connection. The SOT-23 package the diodes come can dissipate 350 mW at 25°C when mounted on a 80-mm^2 ceramic substrate. Suggested applications include use as rectifiers, mixers and protection circuits in detector-mixers, or for surge protection in MOS circuits. An operating-temperature range of -55 to +150°C makes the diodes suitable for military use.

Zetex plc, Fields New Rd., Chadderton, Oldham, OL9 8NP. 44 61 627 5105. United Kingdom.

CIRCLE 368

SOFTWARE EASES DESIGN OF REAL-TIME SYSTEMS



Giving designers the ability to model real-time control applications even before a line of code is written, the VRTX designer software package should speed system development. The software allows software developers to create behavioral models of real-time control systems and perform simulation through the use of graphical icons that represent the different operations. Icons model the architecture and represent the multitasking, priority-based preemptive software. The icons represent objects such as tasks, interrupt service routines, external drivers and subsystems. Communication and synchronization mechanisms such as mailboxes and queues can also be simulated. Embedded rule-based design checking and quality assurance reporting assures complete evaluation of the system. A syntax-driven editor allows designers to specify the internal logic and timing behavior of tasks. For each task, the control statements, the probabilities of each software construct, and the time needed to run each sequential section of application code, can all be specified. Interrupts from external devices can also be simulated, as can the timing behavior and operating-system overhead of multiple paths within the software architecture.

The initial release of VRTXdesigner will be on Sun 3 and Sun 4 platforms, with a single-user price of $12,500. If purchased before Dec. 31, 1990, the special promotion price is $9950.

***Ready Systems Inc.**, 470 Potrero Ave., Sunnyvale, CA 94086; (408) 736-2600* **CIRCLE 370**

■ *DAVE BURSKY*

UNIX SPREADSHEET RUNS UNDER X-WINDOWS

Taking full advantage of the X-Window system, eXclaim! is Unix spreadsheet software that runs under the Motif user interface developed by the Open Software Foundation (OSF). The X-Window system adds windowing, a mouse, dialogue boxes, and pull-down windows to the spreadsheet. Because the spreadsheet runs on Unix, it's suitable for networked platforms. The software's flexibility lets users port their applications to most Unix hardware platforms, including X-Window display terminals, workstations, servers, mainframes, and supercomputers. Depending on the configuration of licenses, eXclaim! ranges in price from $1000 to $10,000. It will be available in the second quarter.

***Quality Products Software Co.**, 5711 W. Slauson Ave., Suite 240, Culver City, CA 90230; (213) 410-0303.* **CIRCLE 385**

CASE TOOL SUPPORTS IBM'S AD/CYCLE

An OS/2-based CASE package supports IBM's recently announced AD/Cycle application development strategy for the Systems Application Architecture (SAA). The Application Development Workbench provides integrated support, from information-systems planning through analysis, design, and code generation. It is divided into four tool sets, each addressing a different phase of the software development cycle. The Design Workstation and Construction Workstation tool sets are scheduled for release during the first quarter of 1990; the Planning and Analysis Workstations are planned for the second quarter of 1990. The product line is integrated around a central intelligent encyclopedia and uses embedded artificial intelligence to ensure consistency and provide automated assistance in moving through the development cycle.

***KnowledgeWare Inc.**, 3340 Peachtree Rd. N.E., Suite 1100, Atlanta, GA 30026; (404) 231-8575.* **CIRCLE 371**

MECHANICAL FILTERS BOAST SMALL SIZE, LOW PRICE

Thanks to a new packaging concept, a low-cost line of Collins torsional mechanical filters from Rockwell International offers housings that measure just 0.12 in.^{3}. That's one-third the volume of the smallest torsional mechanical filter available before, even though the internal filter structure is unchanged.

By keeping the transducer and resonator structure intact, the insertion loss stays at a low 1 dB. Also, the intermodulation distortion is not affected: The third-order intercept point is greater than 55 dB. The filters are designed with a a flat response with low passband ripple.

The first set of three filters in the product line are centered at 455 kHz, with bandwidths of 500 Hz, 2.4 kHz, and 6 kHz. The 2.4-kHz and 6-kHz filters have a shape factor (ratio of 60-dB bandwidth to 3-dB bandwidth) of less than 2:1. Low-cost FDM telephone-channel filters at 128 kHz will follow.

The filter package, which is designed for pc-board assembly, measures 1.25 in. long by 0.4 in. wide by 0.24 in. high.

In quantities of 100, each of the three filters costs $30. Delivery is from stock.

Rockwell International, Filter Products, *2990 Airway Ave., Costa Mesa, CA 92626; (714) 641-5311.*

CIRCLE 378

■ *DAVID MALINIAK*

OPTICAL INTERRUPTER SENSORS MEASURE 4-MM^2

A line of ultra-small optical interrupter sensors for pc mounting measures just 4-mm square. The EE-SX1038, 1052, 1067, and 1068 sensors provide square-wave "no-noise" outputs and are suited for any application calling for precise switching and/or linear-motion feedback. The sensors are available in slot widths ranging from 0.9 mm to 2 mm. Their outputs are configured for phototransistors and they feature typical response time of 40 μs. Prices start at $.78 in lots of 1000.

Omron Electronics Inc., Control Components Division, One E. Commerce Dr., Schaumburg, IL 60173; (708) 843-7900. **CIRCLE 379**

TINY SMT MIXER HANDLES +14-DBM INPUT

Claimed as the world's smallest surface-mounted mixer, the RMS-2H operates over a range of 2 to 1000 MHz and has a 1-dB compression point of +14 dBm. The unit houses rf transformers and a four-diode assembly on a ceramic-alumina substrate in a tiny 0.25-by-0.3-by-0.2-in. metal case. An edge-plated design eases the task of soldering the device to pc boards. The mixer provides 43-dB rf-lo and 30-dB lo-if isolation and 7.8-dB conversion loss. Pricing is $14.95 in quantities up to nine with delivery from stock.

Mini-Circuits, P.O. Box 350166, Brooklyn, NY 11235-0003; (718) 934-4500. **CIRCLE 380**

ULTRA-LOW-PRESSURE SENSOR PLAYS WITH CPUS

Pressures as low as 2 in. of water (0.075 psi) can be measured by the NPP series of silicon piezoresistive pressure sensors. The sensors' TTL outputs are 2-to-12-MHz, open-collector types that are directly compatible with microprocessors. Additional analog-to-digital conversion circuitry is not required, which makes for a space- and cost-effective approach to airflow measurement. Three differential and gauge-pressure ranges are offered: 0.07 psi, 0.36 psi, and 1 psi. Accuracy, combining linearity, hysteresis, and repeatability, is within ±1.0% at room temperature. Unit price is $25 in lots of 10,000. Samples are delivered from stock and production lots take eight weeks.

NovaSensor, 1055 Mission Ct., Fremont, CA 94539; (415) 490-9100.
CIRCLE 381

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Sal F. Marino, Chairman and CEO, Penton Publishing, Inc.

EMI FILTER UPS CURRENT HANDLING BY 35%

With the FMB-461 emi filter, the current-throughput capability of Interpoint dc-dc converters is increased by a full 35%. But design advances permit the filter to fit in the same 1.1-by-2.1-by-0.5-in. hermetically sealed metal case as earlier lower-rated models. The filter reduces the reflected input ripple of over 30 converter models, which brings them within the noise limits of MIL-STD-461B's CEO3 standard. Attenuation is 40 dB of reflected input-ripple current over the range of 100 kHz to 50 MHz. Pricing begins at $148 in lots of 100 with delivery from stock to 30 days.

Interpoint Corp., 10301 Willows Rd., Redmond, WA 98073; (206) 882-3100. CIRCLE 382

SOLDER PASTES ARE WATER-SOLUBLE

As the ban on fluorocarbons grows increasingly tighter, engineers can eliminate solvents in circuit board cleaning through the use of water-soluble solder pastes. The high-purity pastes are designed for batch water cleaning, yet have the application and performance qualities of RMA solders. There outstanding flux activity and print definition enable users to eliminate solvents for cleaning, as well as subsequent disposal problems.

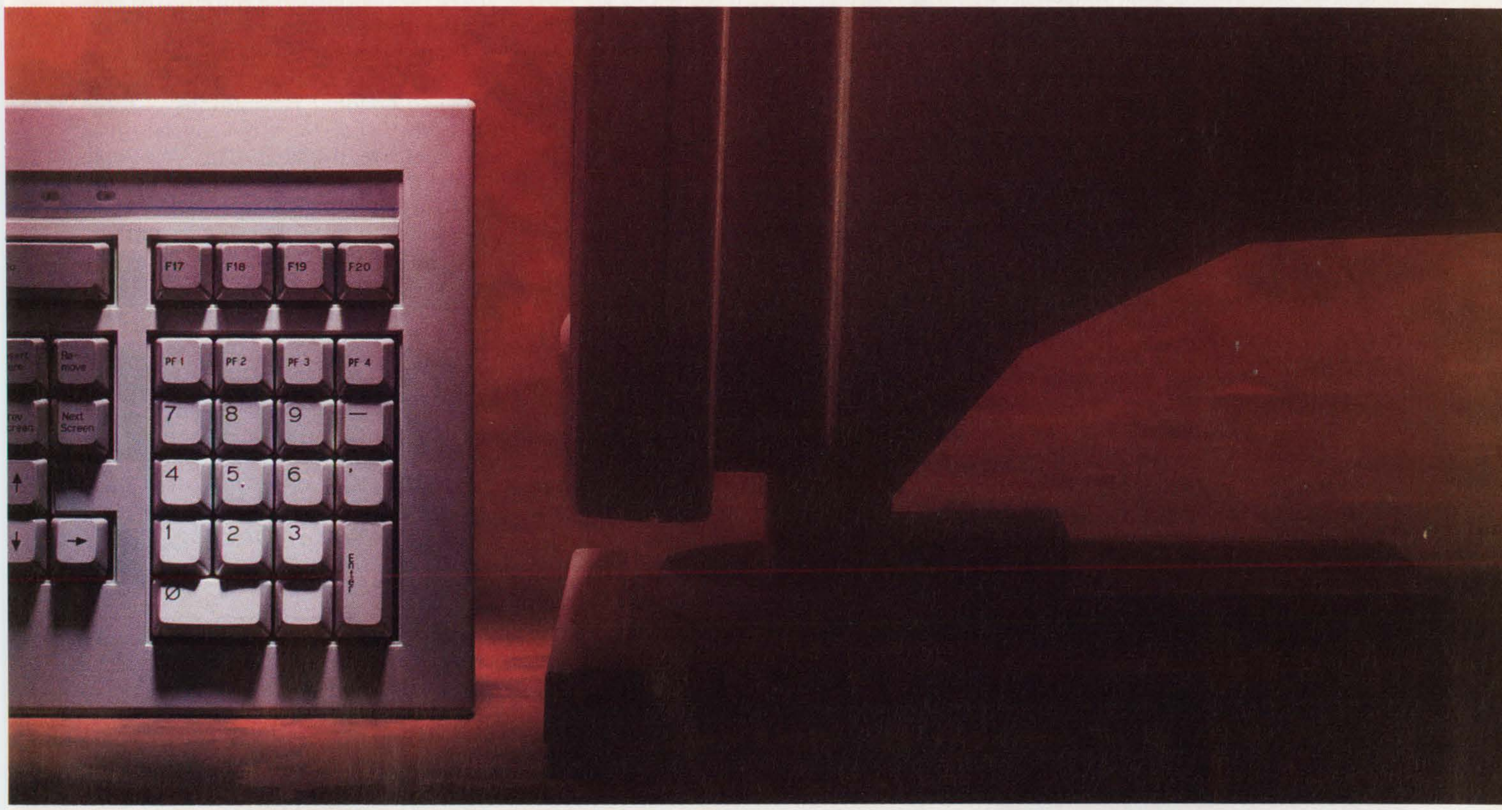
AIM Products Inc., 9 Rocky Hill Rd., Smithfield, RI 02917; (401) 232-2772. CIRCLE 383

SOLID-MATRIX FUSES STAND UP TO ABUSE

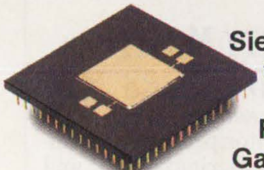
Rather than having its fusible element suspended in air, a line of solid-matrix fuses have their elements embedded in arc-quenching material. The advantages include superior amp-rating stability after exposure to soldering and cleaning. Also, I^2t let-through energy under short-circuit conditions is extremely low. Three packages are available: axial lead, radial lead, and surface-mounted. In lots of 10,000, pricing ranges from $.18 to $.53. Delivery is from stock to six weeks.

Cooper Industries, Bussmann Division, P.O. Box 14460, St. Louis, MO 63178; (314) 394-2877. CIRCLE 384

SIEMENS



Higher Intelligence.

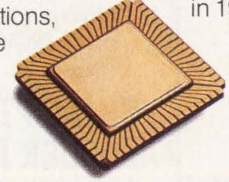


Siemens puts the work in workstations. From Sea of Gates to RISC. Armonk to Zurich.

Siemens, the European leader in 4 Megabit technology, offers a diverse line of ICs for workstation, PC, and embedded control applications.

For example, our 25 MIPS, 32-bit RISC microprocessor, based on the industry standard MIPS® architecture. Or our SAB 80286 microprocessor, running up to 16 MHz. But microprocessors are just the beginning.

Our Advanced DMA controller for 16-bit and 32-bit applications, SAB 82258A, can enhance graphic systems, communication processors or SCSI modules. Giving you an unequaled combination of transfer power and intelligent transfer control.



And for the optimal low-cost, high-speed microcontroller solution, Siemens offers you a performance range from 1 to 10 MIPS. To drive up your system speed, without driving up your system cost.

Siemens offers you a wide array of quality products with the European content for the Common Market in 1992. And for our customers who have manufacturing needs elsewhere, Siemens operates 173 plants in 35 countries worldwide. Permitting you to design systems reflecting a higher intelligence.

For details, call (800) 456-9229, or write Siemens Components, Inc. 2191 Laurelwood Road Santa Clara, CA 95054-1514. Ask for literature package M14A008.

Siemens
Practical Solutions by Design.

CIRCLE 201

GOLD-BALL BONDER ATTACHES DEVICES WITH UP TO 1000 LEADS

Devices with as many as 1000 leads can be bonded by the 1484 XQ gold-ball bonder from Kulicke and Soffa Industries. The machine offers finer looping control and improved bond quality. A new pattern-recognition system uses improved illumination techniques and a special wire-feed system with an end-of-spool detector. Recognition rates are better than 99.99%.

A patent-pending feature automatically centers the bonding position on a selected bond pad, which limits operator-caused errors. The video-lead location time is less than 30 ms per lead and detection resolution is less than 2 μm. The machine's LED illumination technology provides both oblique and direct software-controlled lighting. Sixteen different illumination levels can be chosen from, with no fluctuation from changes in the line voltage-regulator source. The LED lamp's life is four years versus the one-month life of conventional sources.

Thanks to the system's wire-feed scheme and XY-table geometries, unmatched bonding repeatability, stability, and quality on wire lengths up to 250 mils are possible. The voice-coil-controlled wire clamps eliminate wire deformation, which results in more precise, consistent looping. A wire path located directly above the bond head provides easy accessibility and improved wire tensioning. An optical sensor controls the wire-feed system.

The machine stores up to 500 process programs with up to 1000 wires per program. Production is scheduled by January of 1991. Call the manufacturer for pricing and delivery information.

Kulicke and Soffa Industries Inc., *2101 Blair Mill Rd., Willow Grove, PA 19090; (215) 784-6569.* **CIRCLE 386**

■ *DAVID MALINIAK*

SCSI TERMINATOR FITS INTO CONNECTORS

The ultra-compact SCSI 2 terminator from Methode easily installs into all high-density, D-style 0.050-in.-center SCSI 2 connectors. The terminator installs at the I/O port and creates impedance to prevent reflection of data transmissions. The device is available in single-ended, differential, and regulated circuitry. Custom circuitry is also available. Included is easy on-off latching as well as custom color sleeves and logos. Call for pricing and delivery information.

Methode Electronics Inc., dataMate Division, 7444 W. Wilson Ave., Chicago, IL 60656; (800) 323-6858. **CIRCLE 387**

SHIELD TERMINATORS SOLDER IN ONE STEP

A one-step cable shield terminator creates an insulated, strain-relieved solder termination that meets MIL-S-83519 specifications. 3M's heat-shrinkable shield terminators come in five diameters with or without pre-installed ground leads. The completed assembly provides thermal and electrical insulation, identification, strain relief, moisture sealing, and chemical protection. In use, the outer sleeve shrinks while the solder preform melts and flows to complete the connection. Finally, the thermoplastic insert melts to provide a seal. A red thermochromic indicator is included in the solder flux. When enough heat has been applied, the indicator becomes colorless to tell the technician that the soldered joint is complete. Ink markings assist in making quality-control inspections. Call for pricing and availability.

3M, P.O. Box 2963, Austin, TX 78769-2963; (800) 322-7711. **CIRCLE 388**

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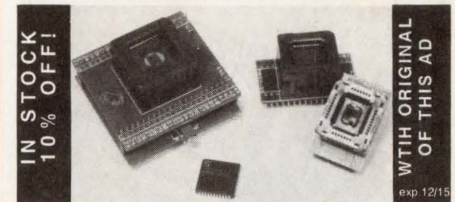

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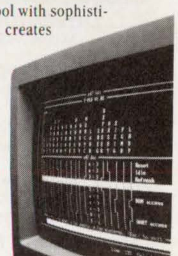

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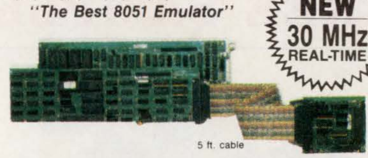

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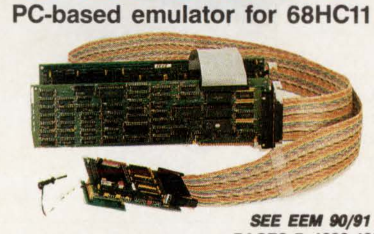

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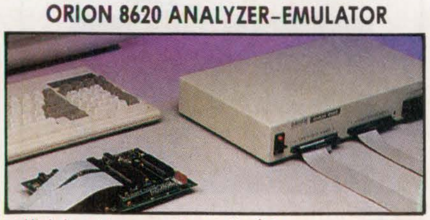

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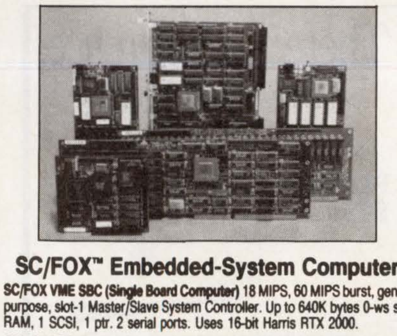

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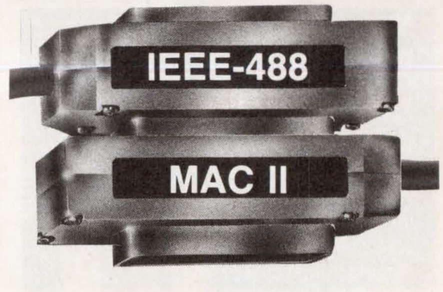

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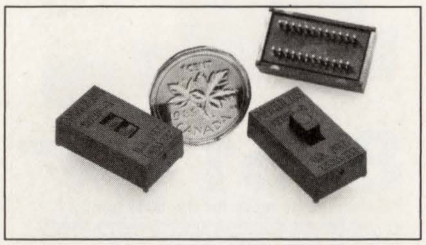

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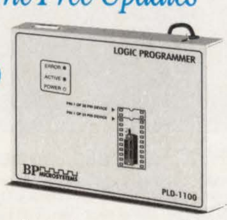

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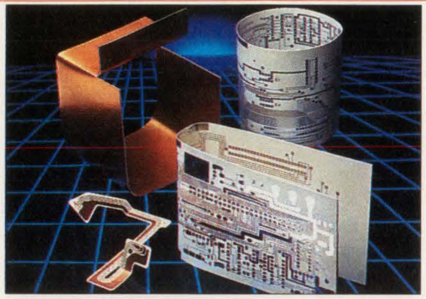

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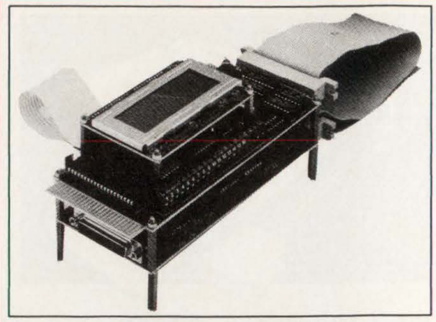

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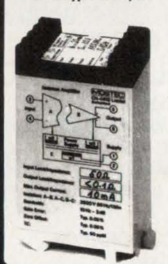

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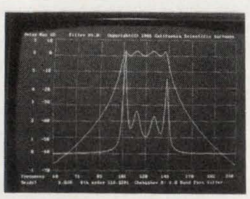

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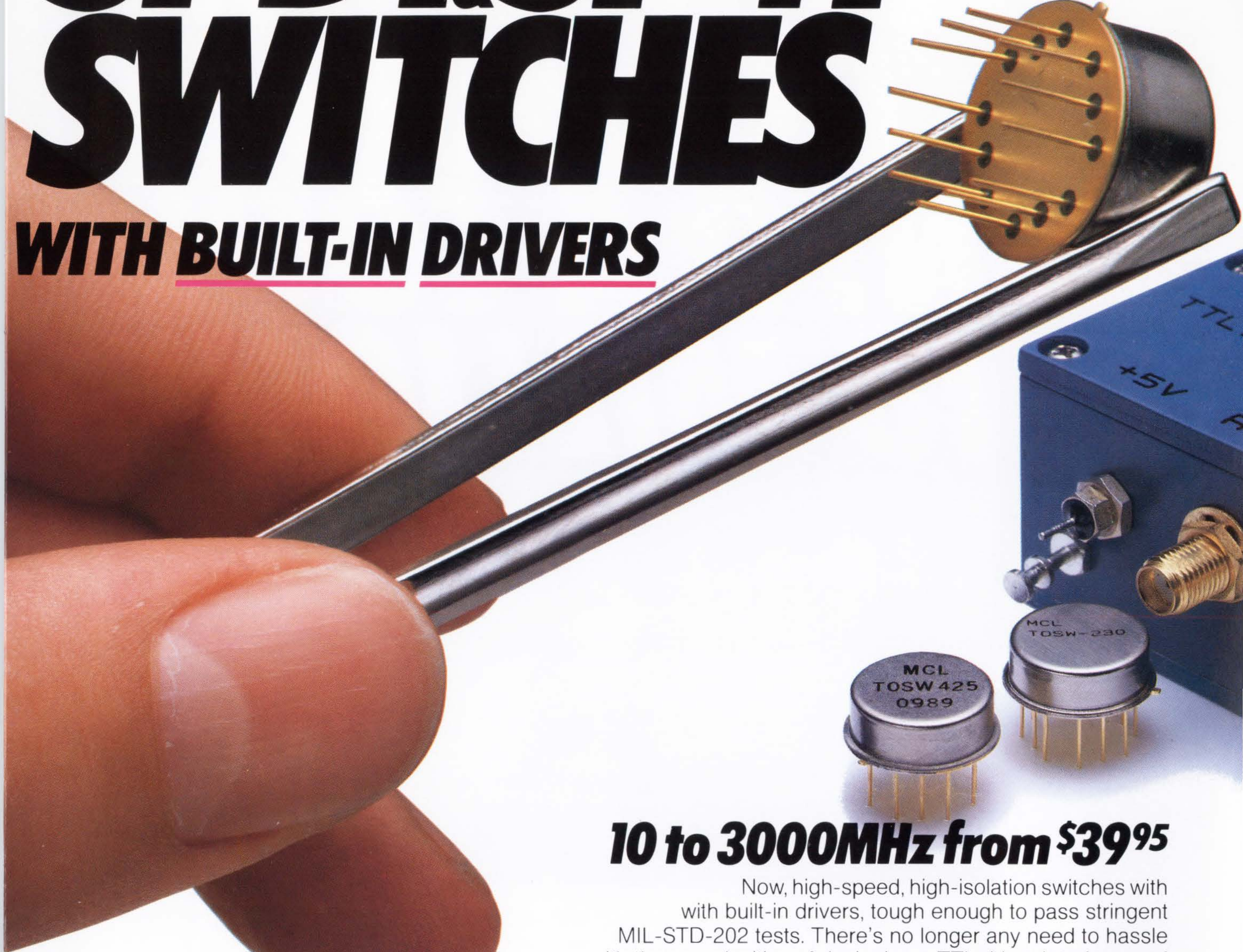

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100-1500MHz	1.1	1.9	1.1	1.7
1500-3000MHz	1.8	2.7	1.8	2.5
Isolation(dB)	typ.	min.	typ.	min.
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