

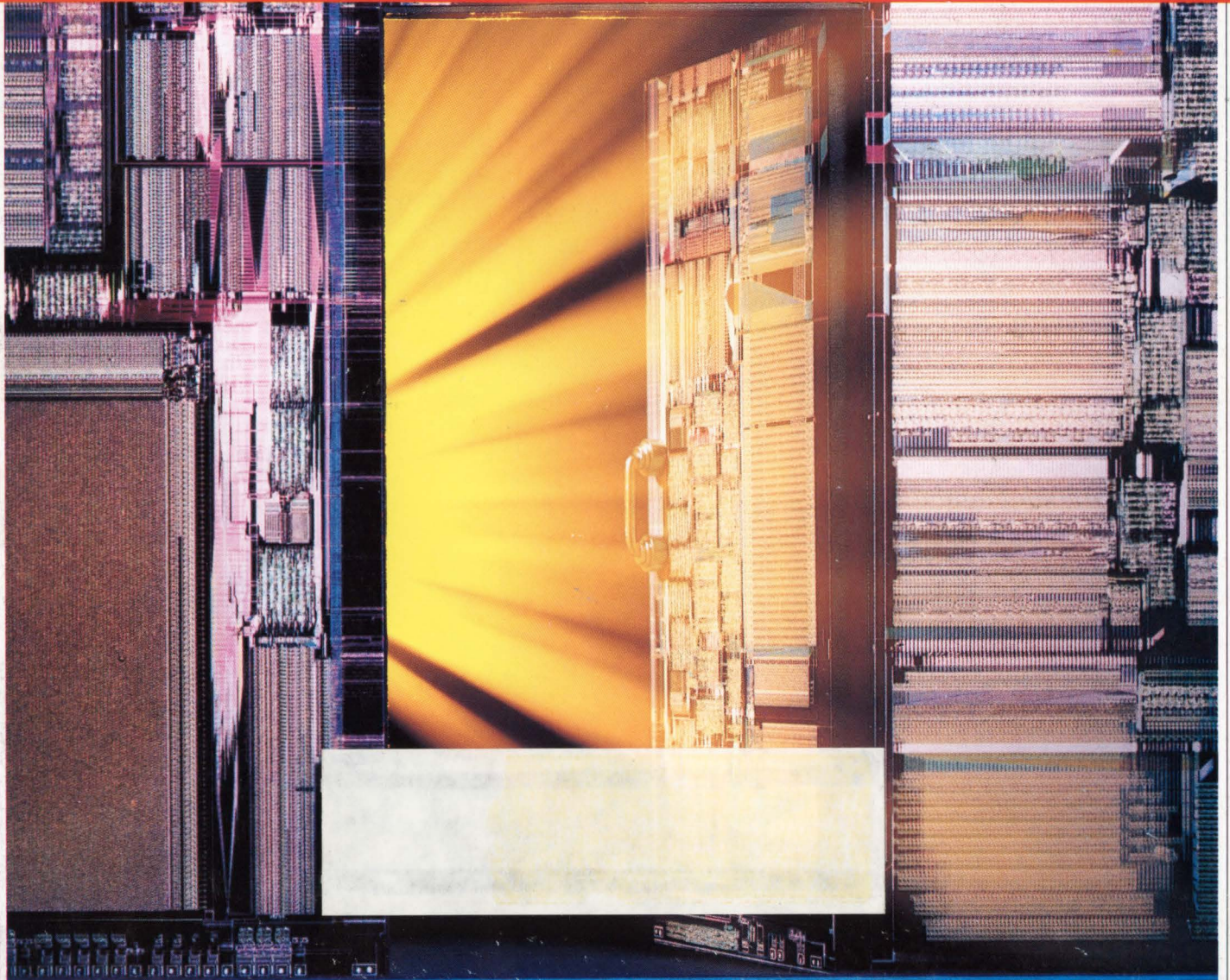
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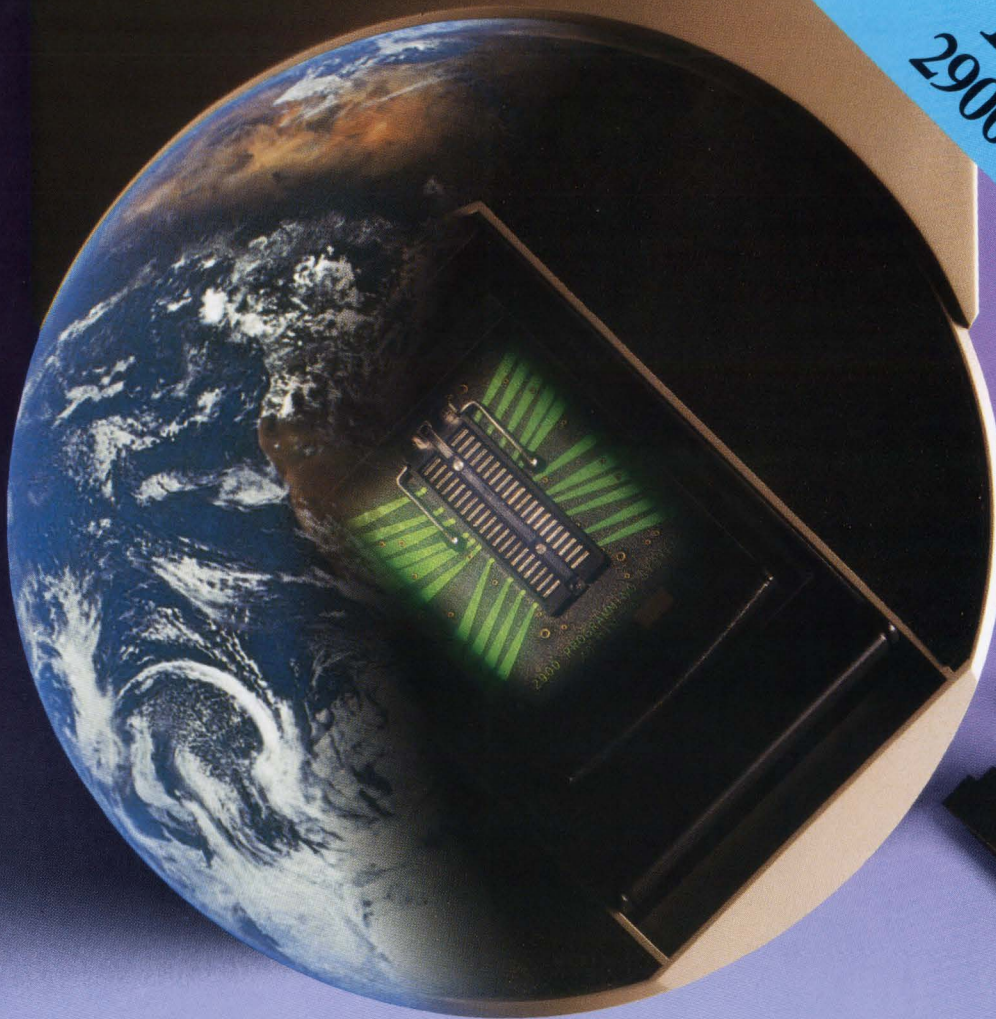
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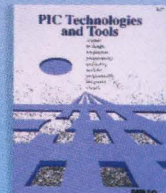
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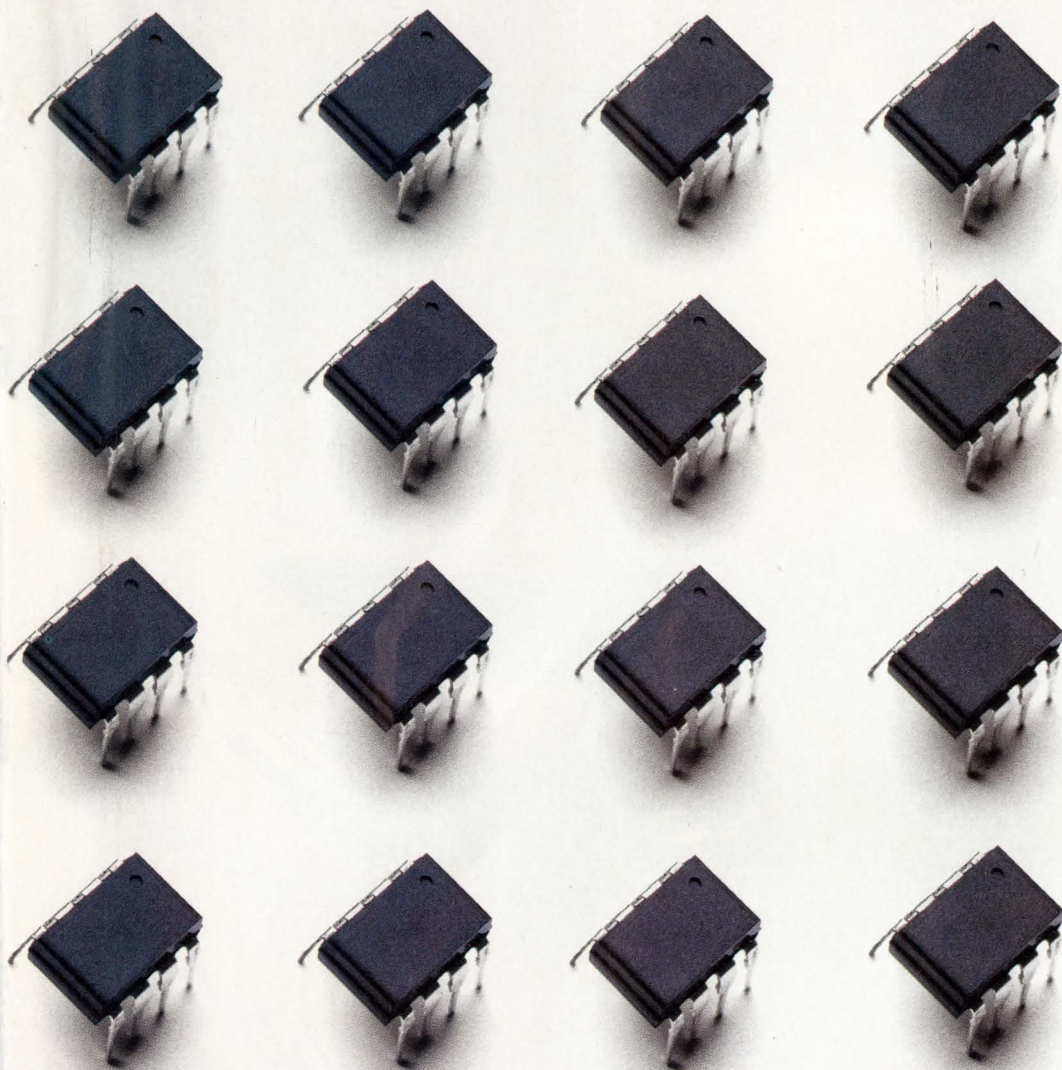
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CIRCLE 86

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had

For years Seagate has been best-known as the volume producer of disc storage products. But our reputation as solely a manufacturing

powerhouse is beginning to change.

In the past several months Seagate has received three Disc Drive Supplier of the Year awards from some of our valued OEM customers. In every case, the commendations have been earned not just for supplying quality products, but for providing superior customer service.

ICL, Britain's leading information technology company, honored us with their Vendor Award Citation for being responsive to their flexibility of delivery and cost of ownership requirements. In addition, our Wren drives exceeded their stringent reliability and "plug-and-play" criteria.

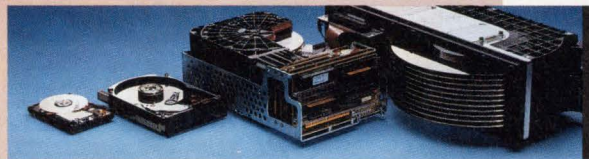
Olivetti, the Italian computer company, awarded us their Quality Award for Customer Satisfaction for the same reasons. By meeting Just-in-Time delivery schedules, listening to the customer, exchanging data from the field and providing training and support, we have helped Olivetti provide superior products and service to their customers.

Most recently, AT&T's Oklahoma City Works presented Seagate with its 1990 "Partner in Excellence" award during their Quality Month observance. Once again, Seagate was selected for its ability to meet AT&T's high standards of quality, delivery, service, cost and technical support.

So while Seagate is still the first name in disc drives, we're making quite a name for ourselves in quality and customer service, as well. To learn more about the benefits of a partnership with Seagate, call us at 800-468-DISC, or 408-438-6550.

And to our customers, we offer a couple of choice words of our own: Thank you.

H N O L O G Y

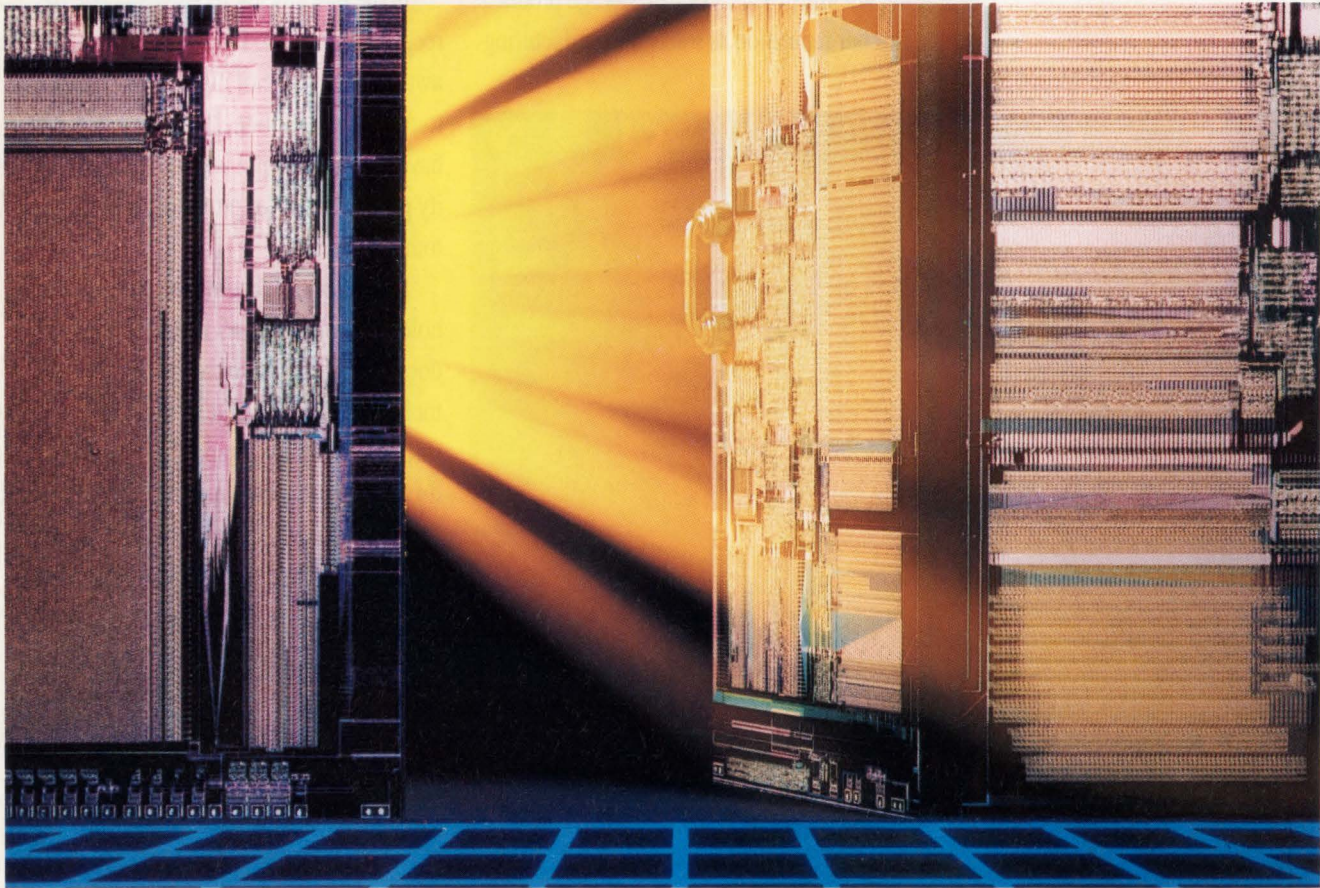


 **Seagate**

The first name in disc drives

CIRCLE 119

ELECTRONIC DESIGN



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Certificate of Merit
Winner, 1988
Jesse H. Neal Editorial
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Cover: Joe Drivas

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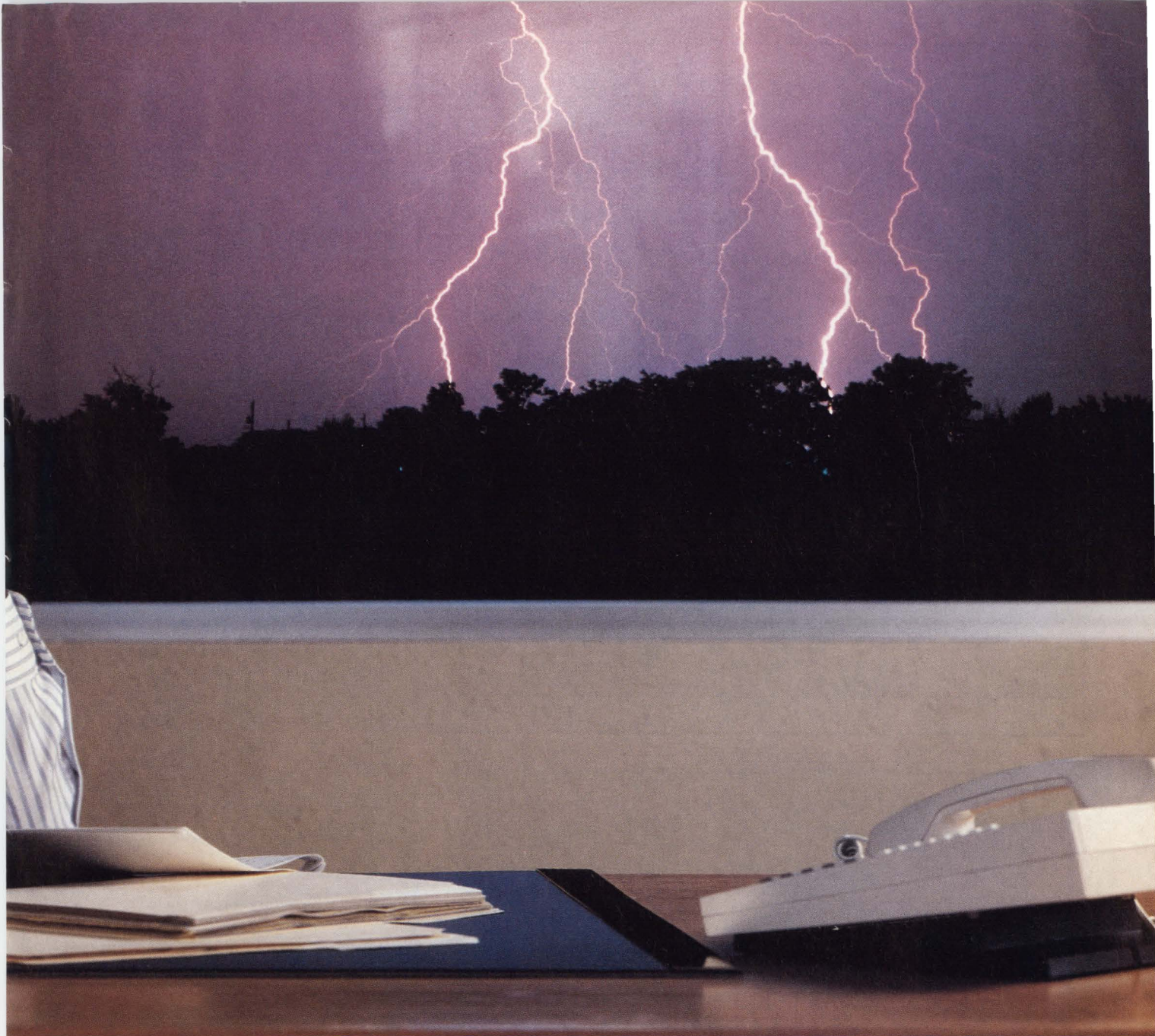
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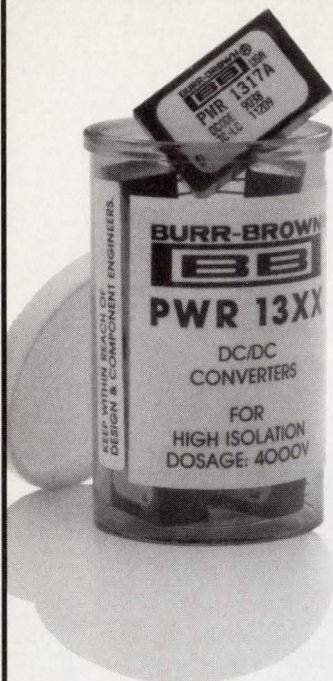


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CIRCLE 158

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CIRCLE 2

8 E L E C T R O N I C D E S I G N

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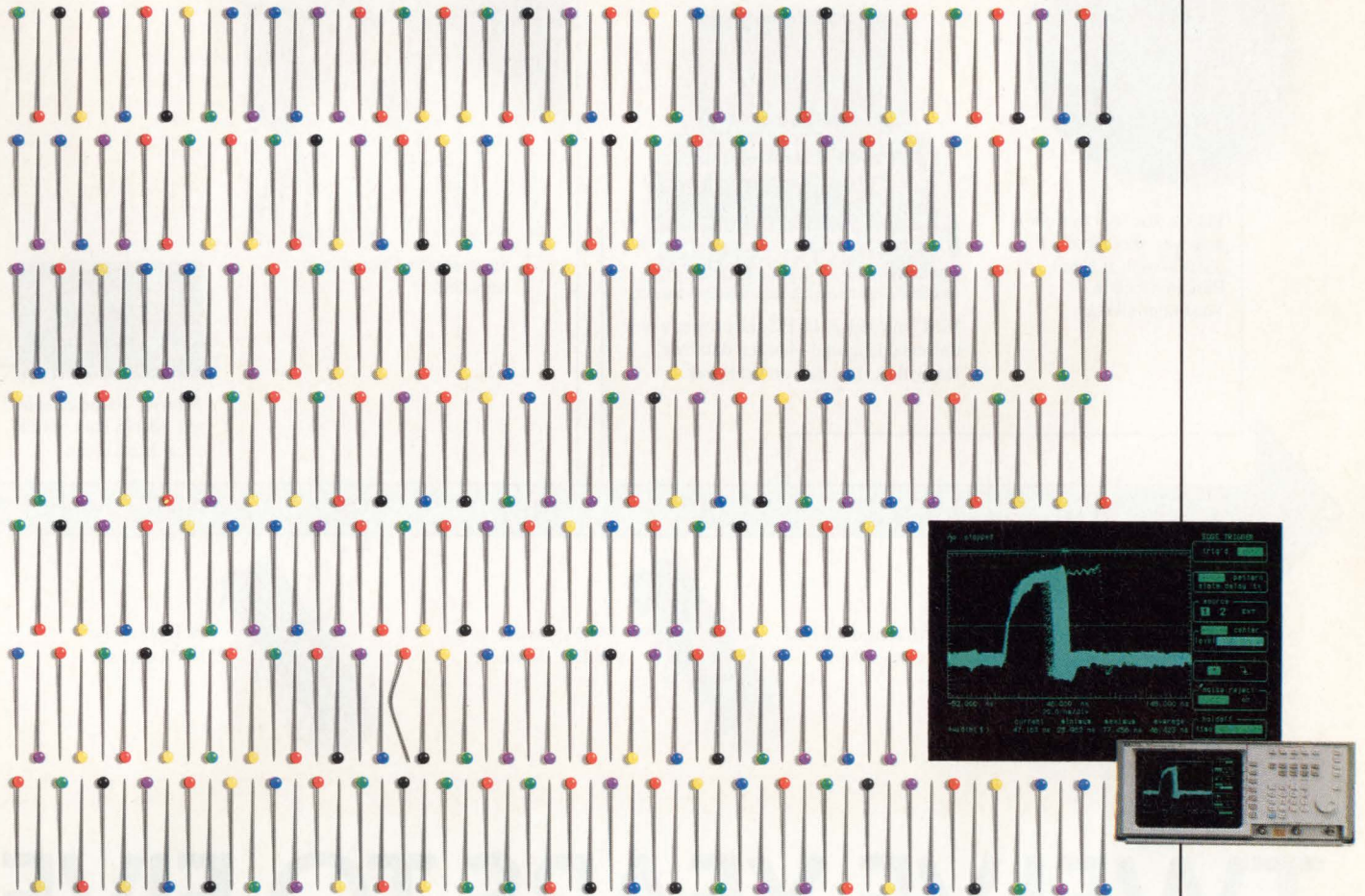
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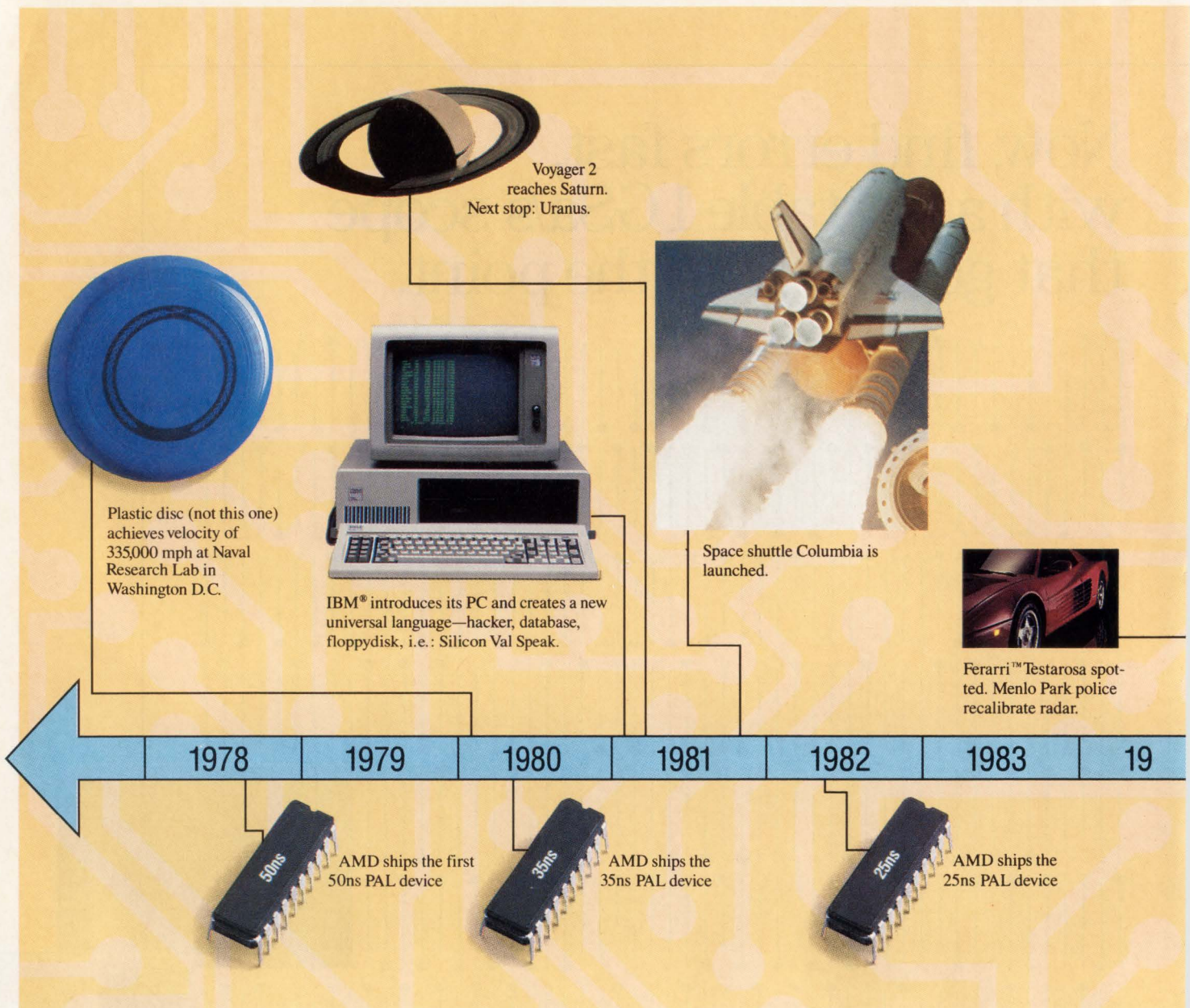
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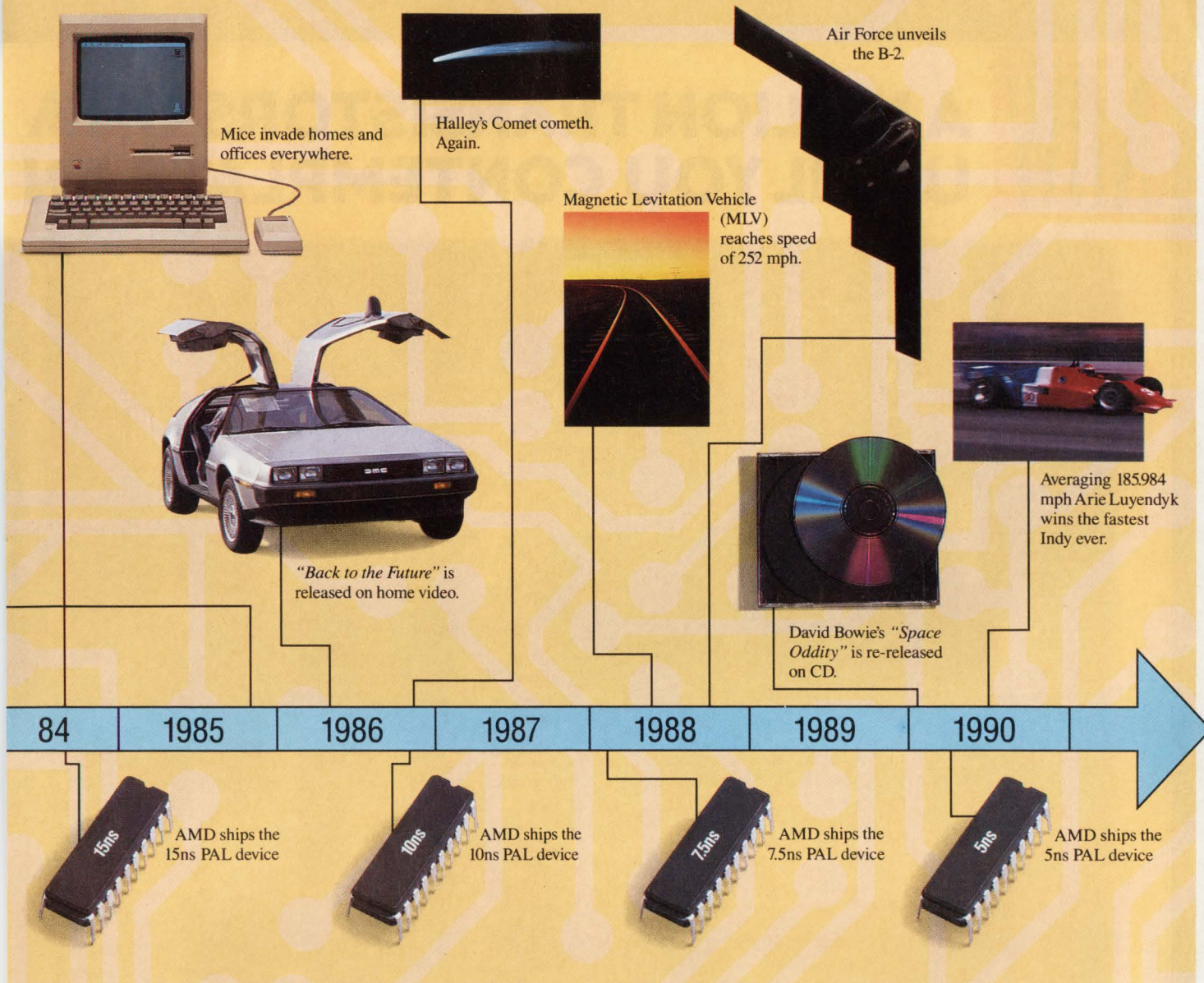
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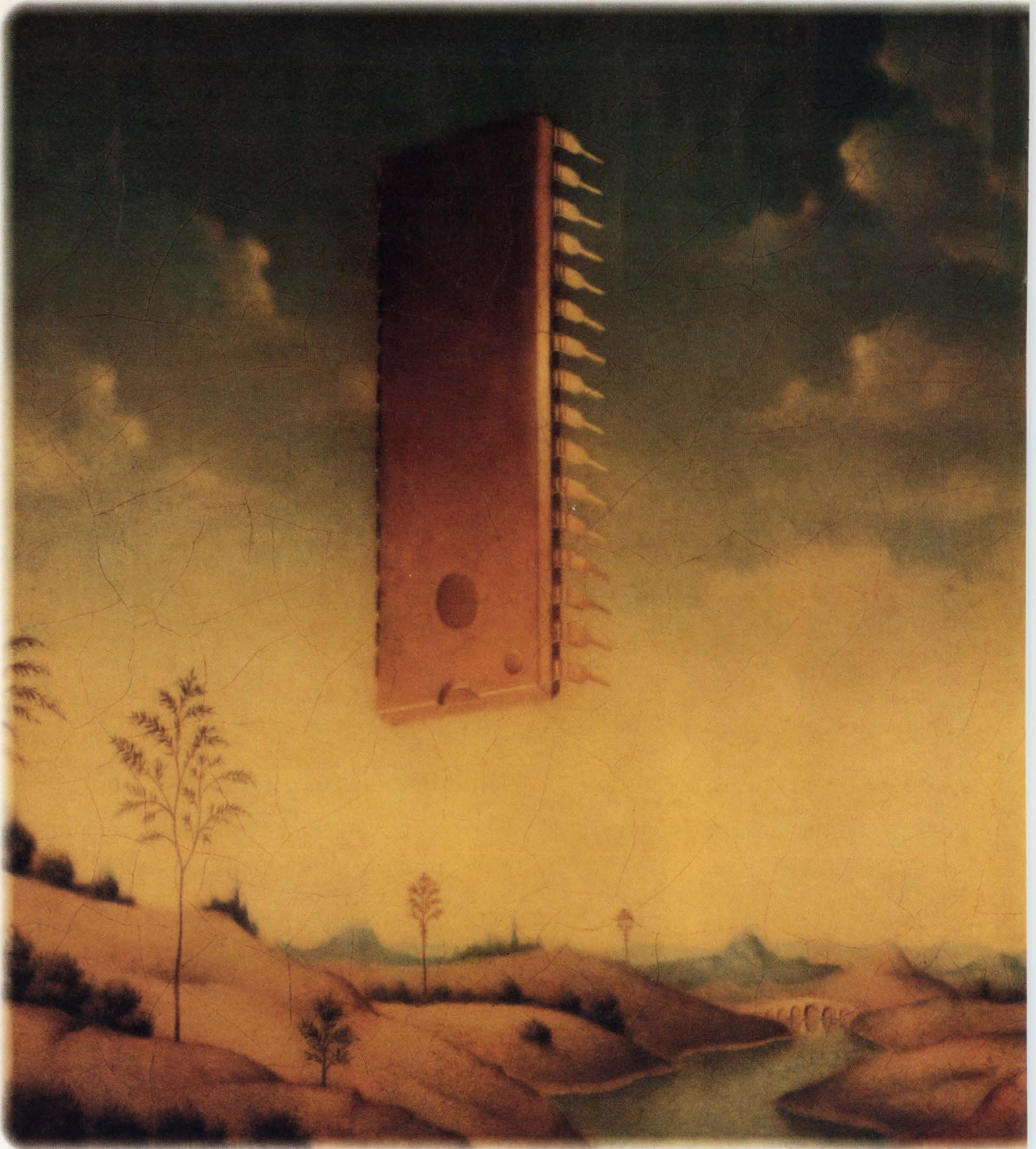
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After all, the best way to contemplate the 6.6 million transistors on the part, is to get your hands on one.

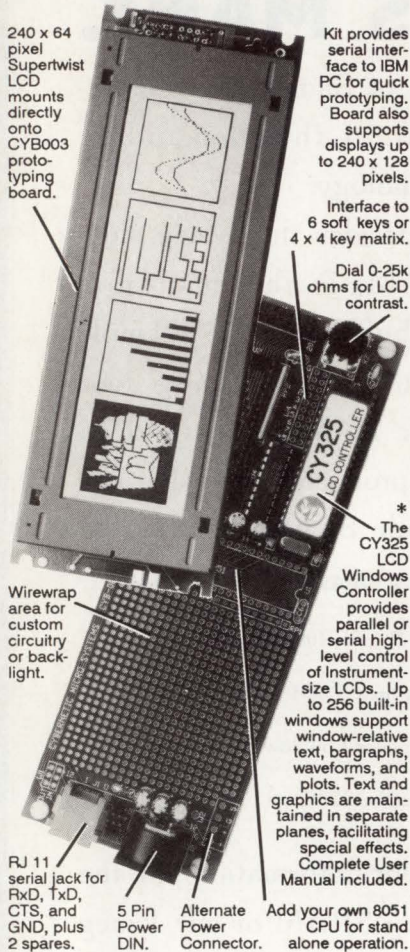


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EDITORIAL



THE ISSCC IN A YEAR OF UNCERTAINTY

Tremors of uncertainty are shaking today's world: Clouds of recession have loomed over global business and industry, while in the Middle East, much more ominous clouds darken the skies as military forces rise to an armed challenge. With so many problems coming over the horizon, it's impossible to predict how the overall picture will develop in the coming months. However, one effect of this uncertainty is abundantly clear—electronics technology has become critical in military operations.

Nevertheless, it seems a relief to focus on a subject where the difficulties do not involve human lives, international politics, or financial management. Once again, the International Solid State Circuits Conference is underway, carrying reports of man's advances in the struggle against the laws of physics involving semiconductor devices. Electronic Design's annual report on the ISSCC (a total of about 20 pages beginning on page 51) describes a broad swath of innovative designs in 64-Mbit DRAMs, high-speed analog-to-digital converters, radio-frequency receivers on a chip, and the like.

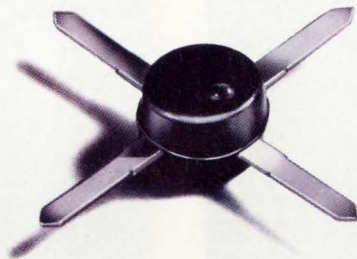
But even the ISSCC, with its elaborate array of advanced VLSI devices, carries a certain degree of uncertainty. Yet this is the type of uncertainty that we have all become accustomed to dealing with: some of the devices described there will not end up as commercial products. Of those, most will probably "fail" because of their complexity and attendant yield problems, causing them to miss their market window. But that fact hardly negates the importance of the basic developmental achievements described in each of the ISSCC paper presentations.

Undoubtedly, some of the devices described in past conferences are now deployed in war zones; let's hope that their use contributes to a lasting peace. And let's also hope that this year's devices, described in their infancy in San Francisco this week, will grow to serve their part in man's most pressing needs: life, liberty, and the pursuit of happiness. There's no uncertainty about those needs.

Stephen E. Scrupski
Editor-in-Chief

99¢

from



dc to 2000 MHz amplifier series

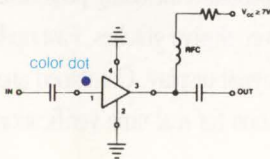
SPECIFICATIONS

MODEL	FREQ. MHz	GAIN, dB				Min. MHz	• MAX. PWR. dBm	NF dB	PRICE \$ Ea.	Qty.
		100 MHz	1000 MHz	2000 MHz	(note)					
MAR-1	DC-1000	18.5	15.5	—	13.0	0	5.0	0.99	(100)	
MAR-2	DC-2000	13	12.5	11	8.5	+3	6.5	1.50	(25)	
MAR-3	DC-2000	13	12.5	10.5	8.0	+8□	6.0	1.70	(25)	
MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.90	(25)	
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)	
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)	
MAR-8	DC-1000	33	23	—	19	+10	3.5	2.20	(25)	

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*MAR-8, Input/Output Impedance is not 50ohms, see data sheet. Stable for source/load impedance VSWR less than 3:1

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80 x 50	10%	X7R	2200, 4700, 6800, 10,000 pf
120 x 60	10%	X7R	.022, .047, .068, 1µf

† Minimum Order 50 per Value

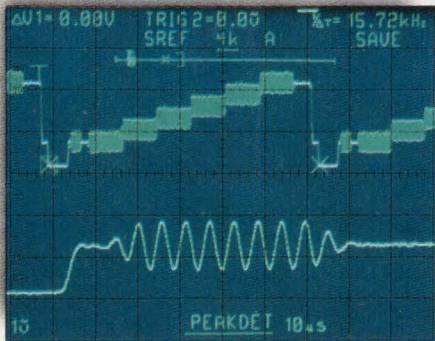
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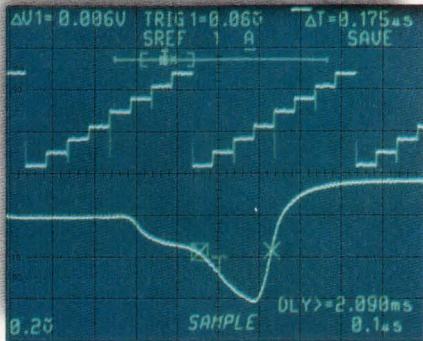
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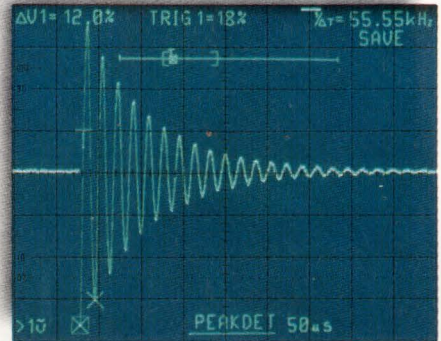
What's you



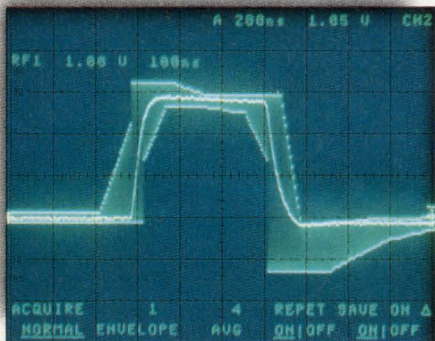
Analyzing TV and complex video signals?



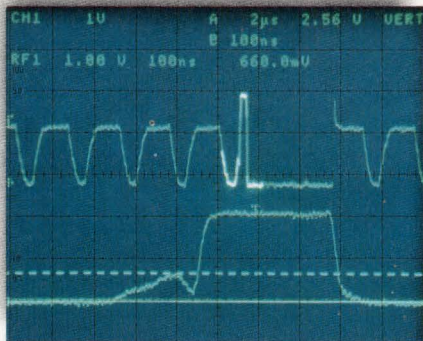
Uncovering elusive glitches?



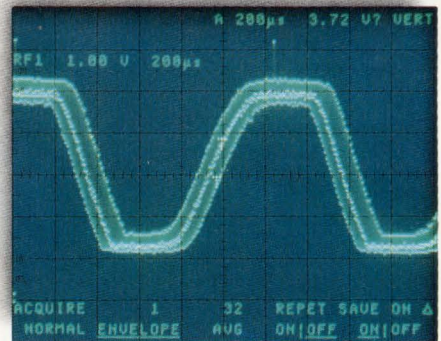
Capturing single-shot events?



Testing telecommunications signals?



Finding aberrations buried within a signal?



Automatic PASS/FAIL testing?

You can't depend on banner specs alone to solve problems like these.

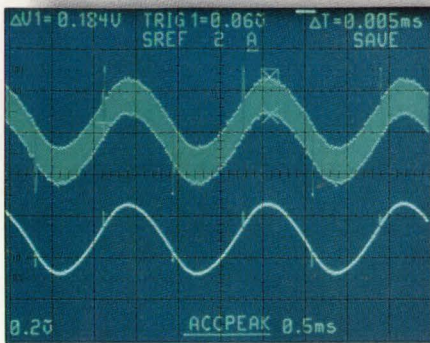
Whether you're trying to measure waveform parameters or analyze long data streams, identify infrequent events or track down glitches as narrow as 2 ns — there's all the difference between the depth of Tek troubleshooting and the trade-offs in other DSOs that compromise your results.

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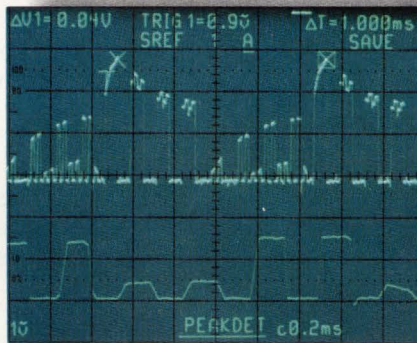
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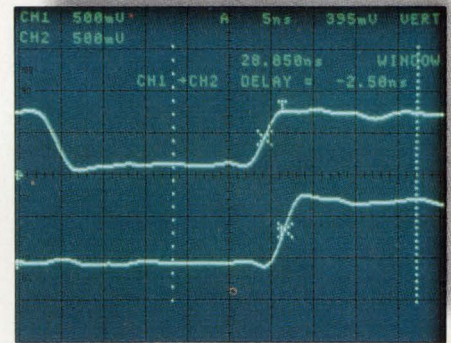
r problem?



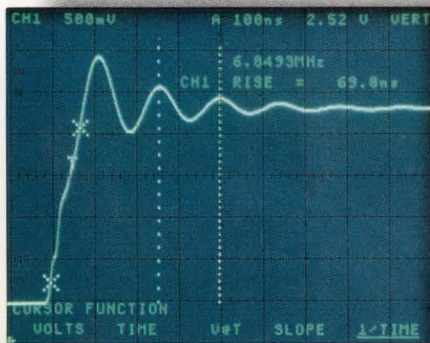
Characterizing signal noise?



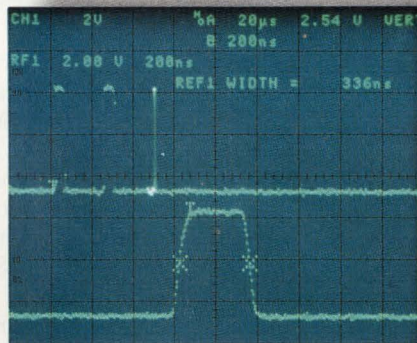
Capturing and analyzing long data streams?



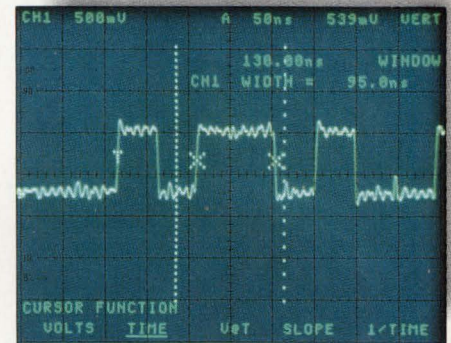
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signal. Or Save on Delta to automatically verify that all parts of your signal fall within prescribed limits. Best of all, Tek's line of 100 MS/s digitizing scopes start at just \$3995.

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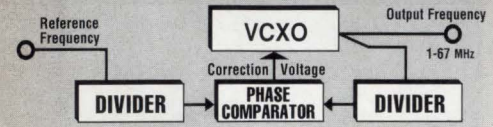
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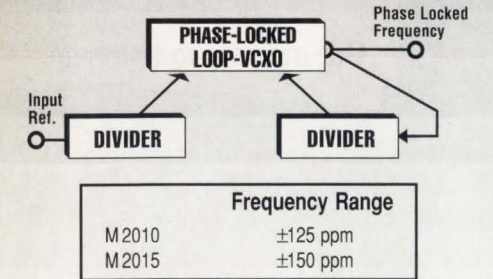
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M 2006	0 to 5V	±150 ppm
M 2007	0.5 to 4.5V	±125 -250 ppm

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SPOTLIGHT ON SOVIET TECHNOLOGY

This year's International Solid State Circuits Conference presents a special session on semiconductor technology in the Soviet Union, offering some rare insights into that country's manufacturing and R&D capabilities. An overview of Microelectronics in the U.S.S.R., by Prof. Richard Jaeger of Auburn University, Auburn, Ala., summarizes the impressions garnered from a multi-facility tour taken by a U.S. scientific delegation in late 1990. The delegation found that Soviet researchers are active in both silicon as well as compound semiconductors, with much of the research activity being state of the art. However, product manufacturing appears to lag western industry by 3 to 5 years.



DAVE BURSKY
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According to Jaeger, the most advanced manufacturing line is just ramping up—a 0.9- μ m facility that will mass-manufacture 1-Mbit dynamic RAMs. Most of the other silicon-fabrication systems are still at 1.5- to 2- μ m minimum-feature size. But some facilities handling compound materials claim they can achieve submicron features.

Due to import limitations, Russian technologists are forced to create almost all of their own manufacturing hardware, including the most critical item—the step-and-repeat lithography system. Their stepper, which has a 1- μ m feature size, 0.1- μ m precision, and a measurement accuracy that's within 0.02 μ m, does offer some cost/performance advantages over other commercially available systems.

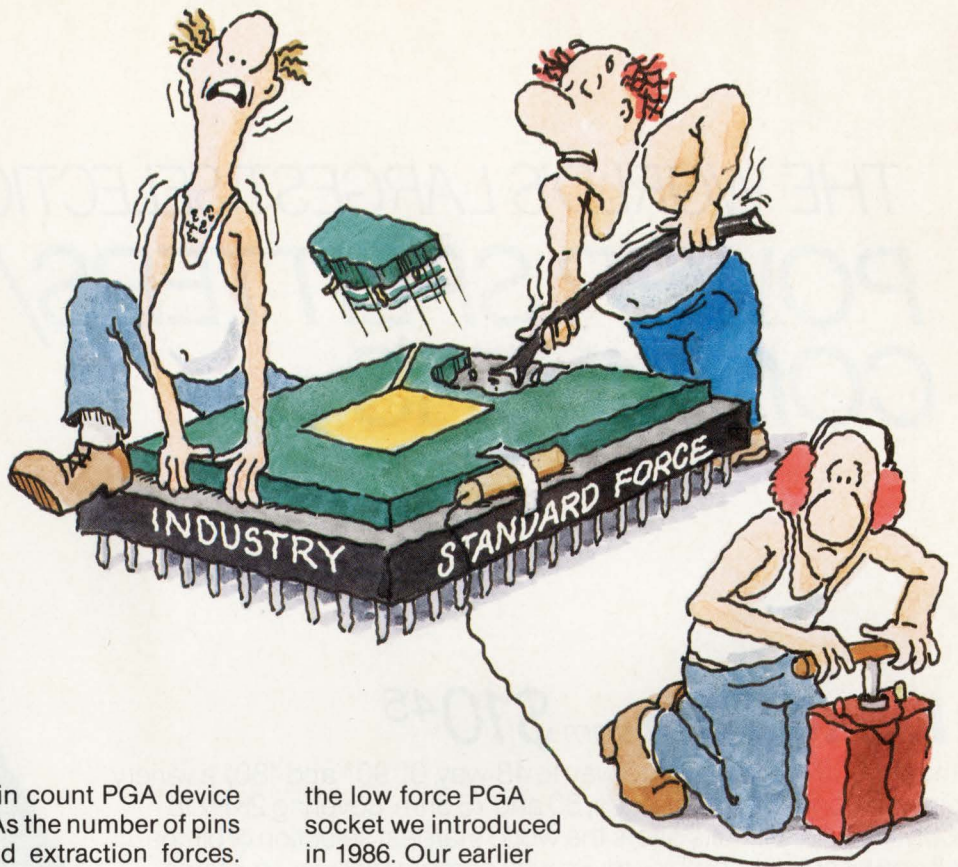
The need for quick-turnaround manufacturing for small quantities of custom chips appears to be just as important in the U.S.S.R. as it is in the rest of the world. At the Nauchny Center in Moscow, a completely automated mini fabrication center was created for this purpose. The highly modularized chip-fabrication line occupies about 200 square meters, consumes about 100 kVA of electrical power, and requires 10 people to run. The line produces silicon as well as GaAs and other compound semiconductor-based products that range from simple MOS circuits to biCMOS, to integrated sensors with on-chip microprocessors.

Each of the nearly 30 manufacturing modules, hermetically sealed to maintain a class-1 environment, performs a number of related processes in a miniature reactor. Laser-based and electron-beam inspection of incoming wafers is done to ensure uniformity, while super-cleaning and drying of each wafer reduces particulates. Wafers are moved on a conveyor-type line with individual wafer processing in miniature reactors. The single-wafer-at-a-time processing reduces the amount of reagents and gases employed during fabrication. However, the wafers typically contain just one VLSI chip, eliminating the need for scribing and breaking. Wafers with diameters of up to 200 mm can be handled, with a maximum chip area of 200 mm² on each wafer. Between 5 and 10 chips per hour can be pushed through the mini-fab facility, with a total input-to-output time (from CAD data base to finished silicon) of from 10 to over 90 hours.

When transported from module to module, the wafers are kept in hermetically sealed chambers to avoid contamination from the class-1000 working environment. Using sealed containers diminishes the high cost that would be associated with keeping the general work area at a class-1 rating. Control of the environment in each module achieves a wafer-to-wafer repeatability of the process in each module to within 0.2%.

An X-ray lithography module is currently being developed by Soviet scientists. All aspects of the X-ray lithography system are automated—from the CAD process for circuit design to wafer processing to device sealing. However, control levels can range from local autonomy within a particular module to central-processor program control.

EXTRACTING A LARGE PGA DEVICE CAN BE HAZARDOUS WORK...

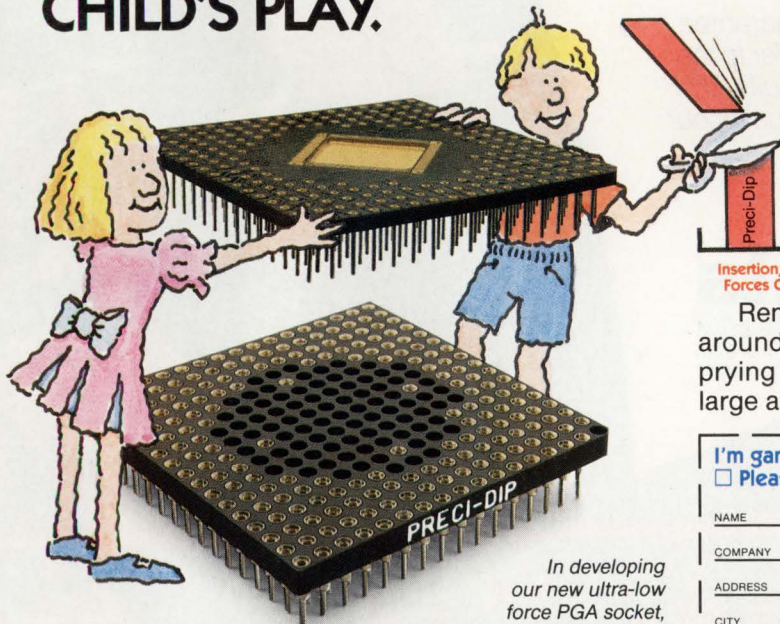


If you thought inserting a high pin count PGA device was a strain, just try removing it. As the number of pins pile up, so do the insertion and extraction forces. Delicate chip packages can be easily damaged.

But now there's a breakthrough: the new ultra low force PGA socket from Preci-Dip.® It's a modification of

the low force PGA socket we introduced in 1986. Our earlier socket became popular with its wide .028" diameter target and greater compliancy to accept bent or misaligned pins. Inside each socket is a specially coined 6-finger inner contact that drastically reduces forces. It's still the preferred choice for most PGA applications.

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Remember, damaged chips are nothing to kid around with. So call us at (516) 922-6000 and start prying into ways to solve your PGA socket problems, large and small.

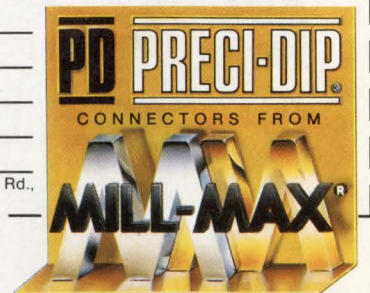
In developing our new ultra-low force PGA socket, we did our homework. Call or write for our data sheet summarizing force comparison tests that we conducted using actual PGA devices.

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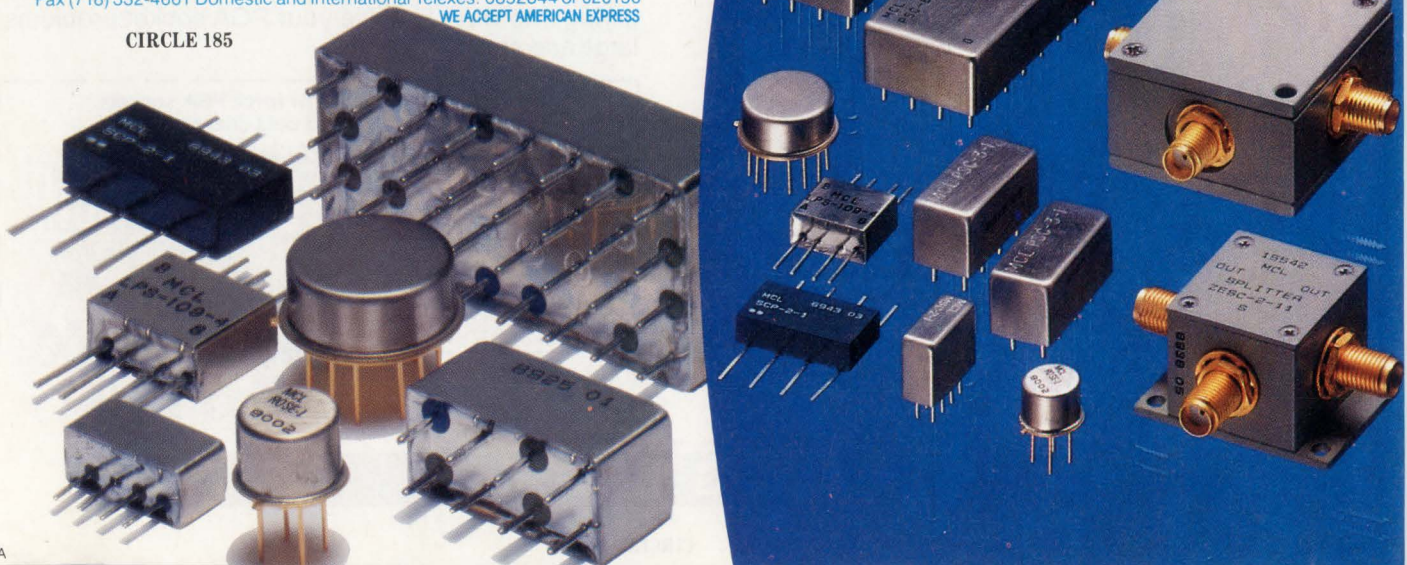
For detailed specs and performance data, refer to the *MicroWaves Product Directory*, *EEM* or *Mini-Circuits RF/IF Signal Processing Handbook*, Vol. II. Or contact us for our free 68-page *RF/IF Signal Processing Guide*.

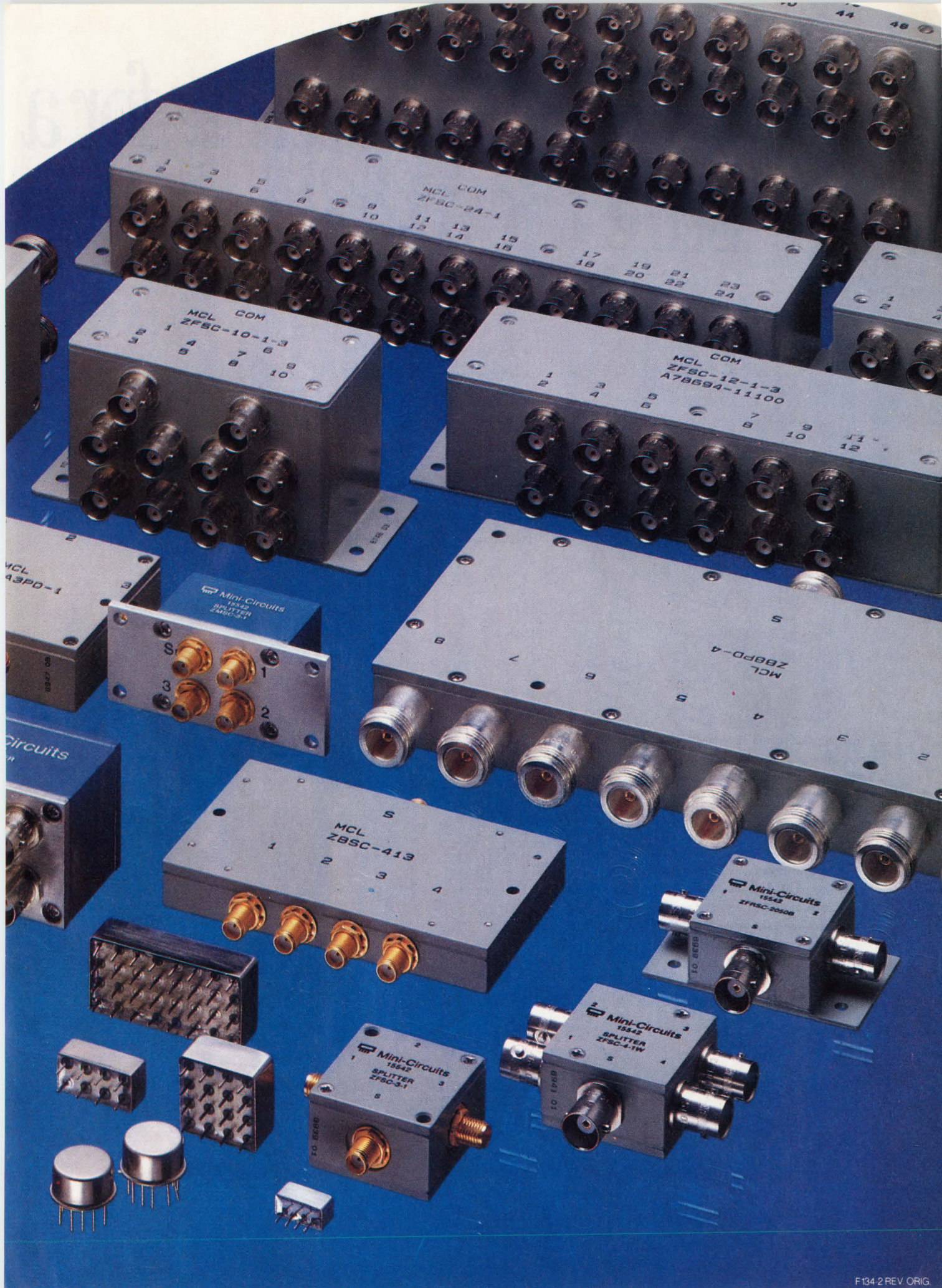
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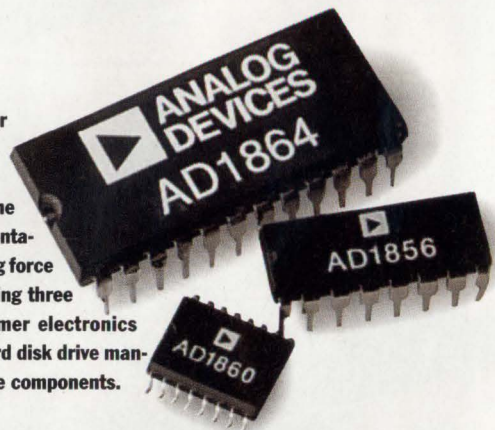
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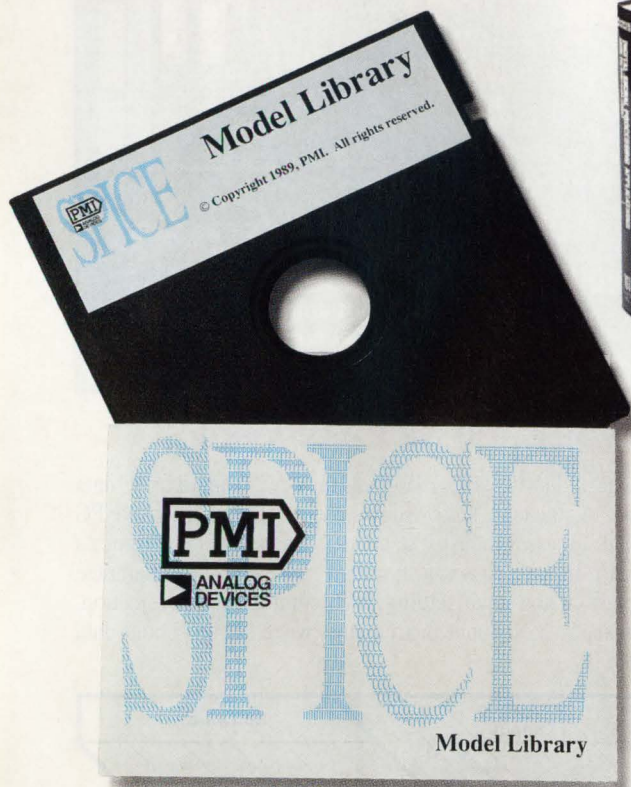


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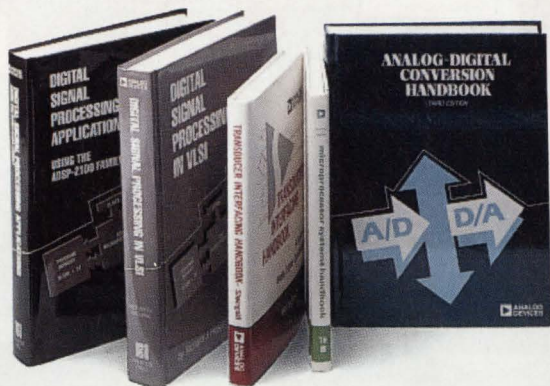
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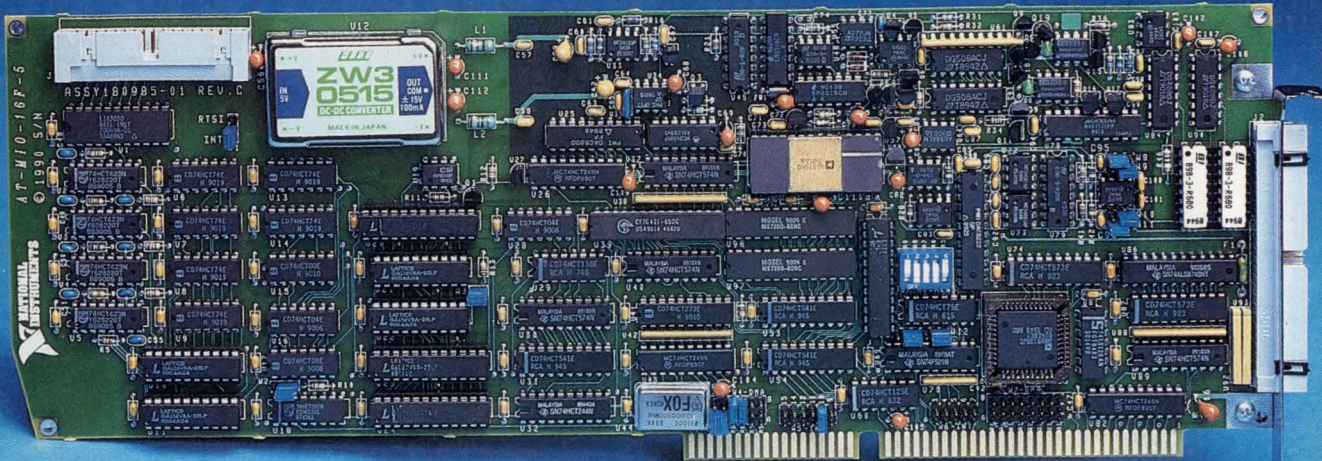
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Data Acquisition Board	Computer Bus	Analog Input					Analog Output				Software					
		Channels*	Max Sampling Rate (samples/sec)	Resolution (bits)	Ranges (V)	Gains	Channels	Resolution (bits)	Digital I/O Channels	Counter/Timers	LabWindows	DOS LabDriver	PC LabDriver	Measure	VisionScope	Third Party
AT-MIO-16F-5	AT	16 SE 8 DI	200,000	12	±5, 0 to 10	0.5, 1, 2, 5, 10, 20, 50, 100	2	12	8	3	✓	✓				✓
AT-MIO-16H-9 AT-MIO-16H-15 AT-MIO-16H-25	AT	16 SE 8 DI	100,000	12	±10, ±5, 0 to 10	1, 2, 4, 8	2	12	8	3	✓	✓	✓	✓	✓	✓
AT-MIO-16L-9 AT-MIO-16L-15 AT-MIO-16L-25	AT	16 SE 8 DI	100,000	12	±10, ±5, 0 to 10	1, 10, 100, 500	2	12	8	3	✓	✓	✓	✓	✓	✓
Lab-PC	XT	8 SE	62,500	12	±5, 0 to 10	1, 2, 5, 10, 20, 50, 100	2	12	24	3	✓	✓	✓	✓	✓	✓
PC-LPM-16	XT	16 SE	50,000	12	±5, 0 to 10 ±2.5, 0 to 5	1	-	-	16†	3	✓	✓	✓			✓
AT-DIO-32F PC-DIO-96 PC-DIO-24	AT XT XT	- - -	- - -	- - -	- - -	- - -	- - -	- - -	32 96 24	- - -	✓ ✓ ✓	✓ ✓ ✓	✓ ✓ ✓			✓ ✓ ✓
PC-TIO-10	XT	-	-	-	-	-	-	-	16	10	✓	✓	✓			
EISA-A2000	EISA	4 SE SS	1,000,000	12	±5	1	-	-	-	-	✓	✓				✓



* SE - Single-Ended, DI - Differential, SS - Simultaneous Sampling

† 8 Channels In, 8 Channels Out



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A new planar magnetron sputtering source, which operates at pressures a full decade lower than established sources, lets physical vapor deposition (PVD) handle submicron device metallization. The Quantum Source from Varian Associates Inc., Palo Alto, Calif., offers better step coverage, more consistent via filling, fewer particles, and lasts 50% longer than previous sources. Operating at lower pressure levels reduces gas scattering and low-angle vapor that typically occurs with other PVD processes. Those improvements translate into better lateral control of the metal-film growth. They also result in a substantial increase in bottom and sidewall coverage in high-aspect-ratio submicron contacts and vias across a 200-mm wafer. For deposited films less than 0.1- μm thick, step coverage as high as 35% can be obtained in contact holes that are 1- μm deep and 0.45- μm wide. In addition, the low pressure allows high-speed cryogenic baffles to be used to quadruple the pump-down speed during production. Lower background levels of residual gas are also present during film deposition, which results in more uniformly grained and better-controlled film purity. Sources are available for aluminum alloys as well as for refractory metals and their reactively formed compounds. Contact Varian at (415) 424-5532. *DB*

TURNKEY BOARD SERVICE HELPS SHRINK SYSTEMS

As computer-system geometries shrink, OEMs may find contract manufacturing preferable to the capital-intensive acquisition of new production equipment. To that end, S-MOS Systems, San Jose, Calif., is now offering board-level design and packaging, and overall subsystem manufacturing, test, and assembly capabilities. The company's Raleigh, N.C.-based business unit offers OEMs access to highly advanced board-assembly technologies, including TAB and chip-on-glass. Boards are built with up to eight layers and can carry 0.5-mm-pitch quad flat-pack devices with up to 256 pins. In addition, boards can have any combination of TAB, chip-on-board, through-hole, and surface-mounted devices. S-MOS expects its board-assembly technology to progress in time. TAB pin counts are expected to rise from their current level of 200 to 500, with inner- and outer-lead bond pitches to reach 80 and 140 μm , respectively. Call Dave Perry at (919) 878-1120. *DM*

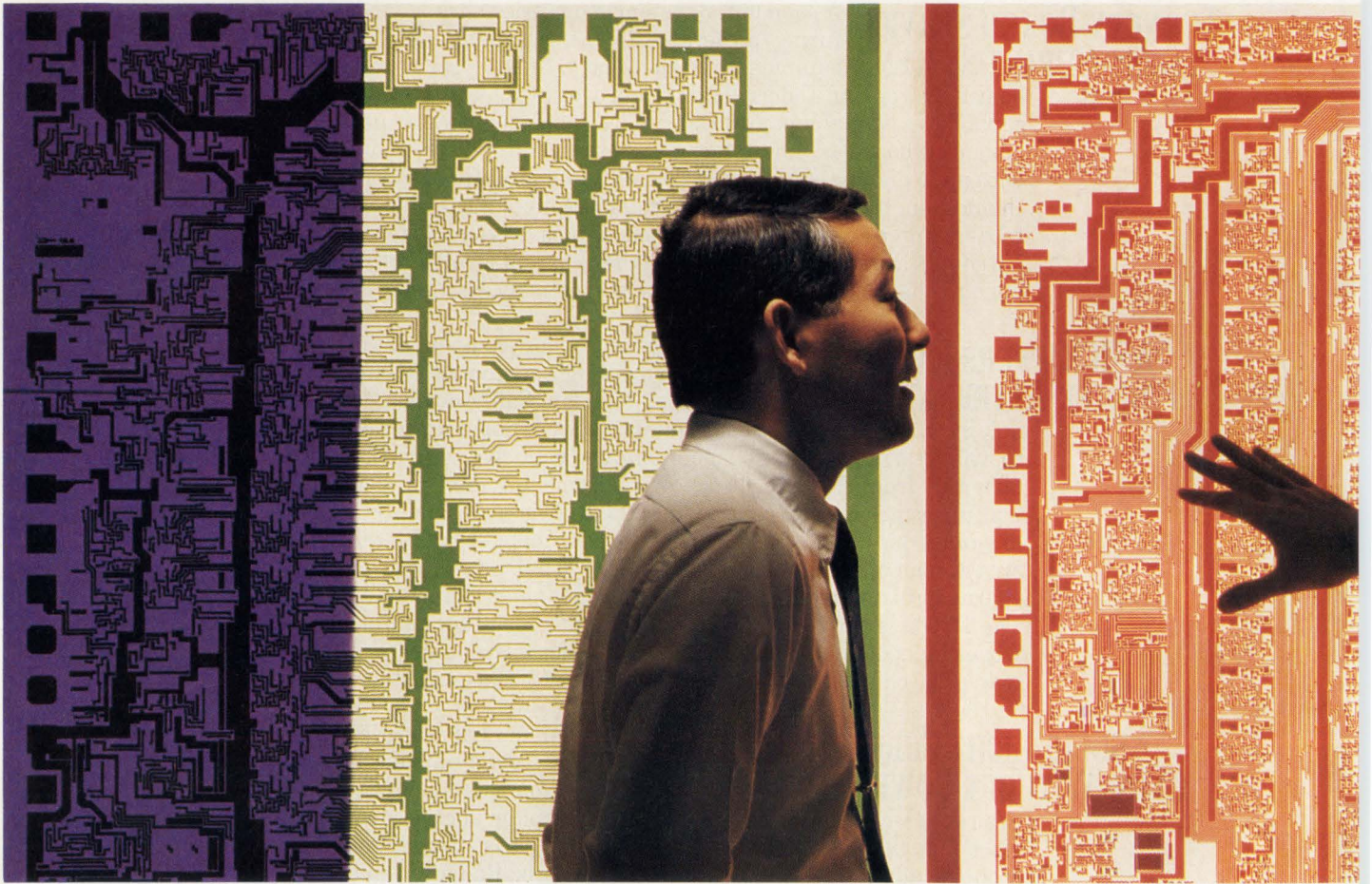
ASIC OFFERS LASER-PRINTER ALTERNATIVE

Laser-printer makers can now compete directly with Hewlett-Packard's LaserJet III printer by using a custom ASIC chip set printer controller. Destiny Technology Corp., Milpitas, Calif., developed the Edge Enhancement Technology (EET) D9001 chip set that improves the appearance of 300-dot/in. laser-printer output to 400 dots/in., thanks to smoothing and reducing jagged edges. While EET is technically different from HP's Resolution Enhancement Technique (RET), its effectiveness is equivalent to, or in some cases surpasses, the RET in improving the output images. Destiny's EET examines one line of pixels for line-segment changes, and determines how to readjust the laser spot to smooth the segment transitions. The D9001 looks for edges, which minimizes the character distortion. HP's RET, on the other hand, examines a window area around each pixel. The D9001 is programmable for different resolution and printer-engine characteristics. It works independently from printer-controller microprocessors and controller emulation software. The chip set is available now for under \$20 in quantities of 1000. *RN*

SOLID LIGHT CUBES GLOW WITHOUT POWER

Researchers at Sandia National Laboratories, Albuquerque, N.M., have developed a glowing piece of plastic—an aerogel—that requires no electrical power, can be made in various sizes and shapes, and produces almost any desired color. In the inorganic version, a phosphor, such as zinc sulfide, is dispersed in a porous silica matrix that effectively is a low-density glass sponge. Tritium gas, a source of radiation, is chemically bonded to the aerogel silica matrix. Radiation emitted by the decaying tritium excites the phosphor particles, causing them to emit light. Because the aerogel is transparent, a large part of the light escapes. Beta radiation is attenuated inside the matrix. Inorganic light cubes or sticks can be ten times brighter than commercial radioluminescent lights and can operate over 20 years. Organic versions use a styrene matrix into which organic dyes can be dissolved for colored light, but discoloration with time limits useful life. Application possibilities range from emergency lighting to photovoltaic power supplies. *ML*

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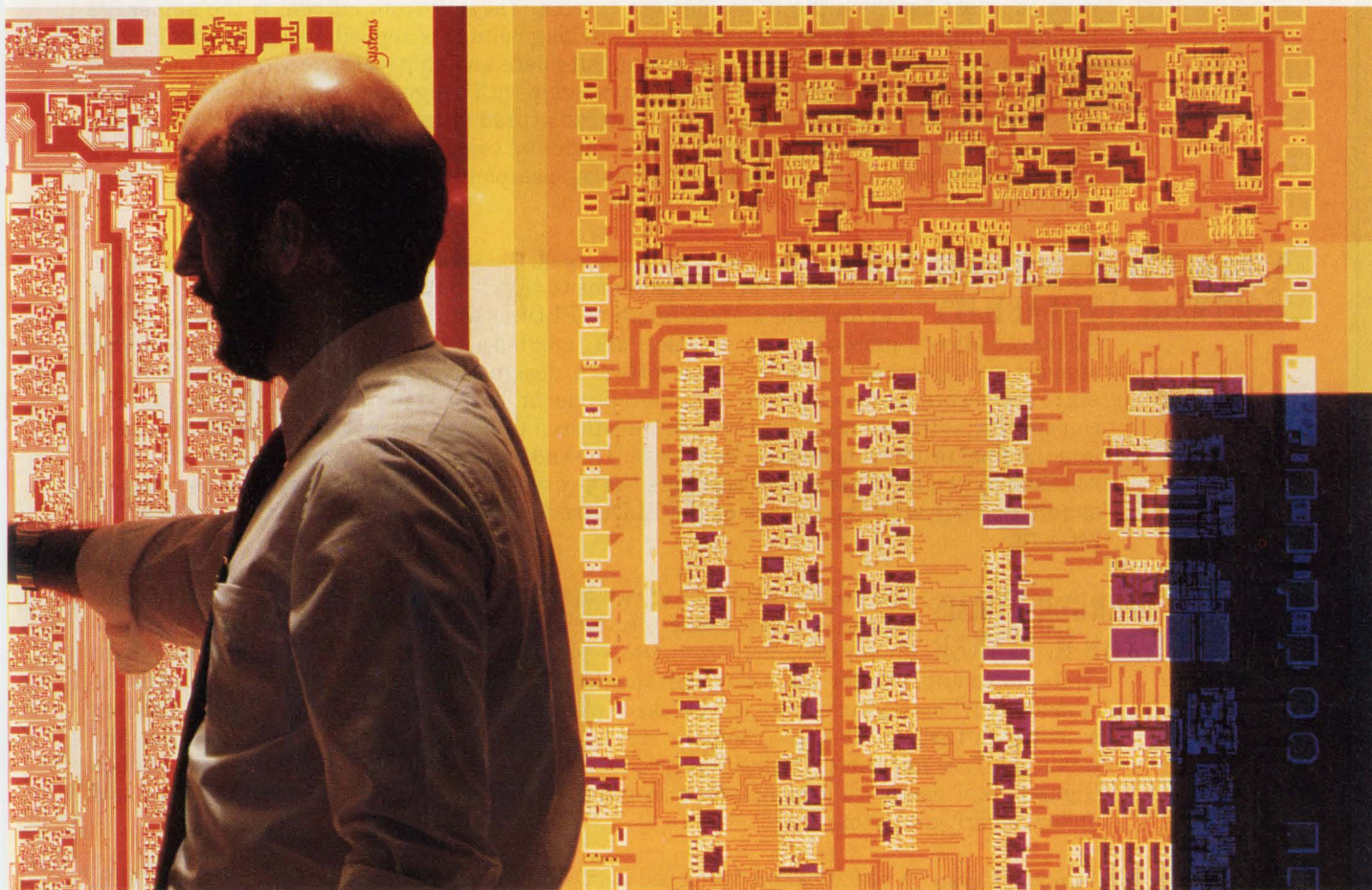
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PLD TOOL INCORPORATES SCHEMATIC SUPPORT

Engineers can now create a programmable logic device (PLD) with familiar TTL levels and then generate a standard Jedec file, thanks to new additions to Version 1.20 of Tango-PLD from Accel Technologies Inc., San Diego, Calif. The enhancements include a schematic-to-PLD translator and an 84-part schematic component library. They translate and then compile the logic into the Tango Design Language format, resulting in the Jedec file. The new component library consists of 42 TTL components, 35 generic gates, and 7 miscellaneous parts that include ports, power, and ground symbols. Also new with Version 1.20 is support for power-up reset, an option to disable logic minimization, and 13 new devices. Tango-PLD Version 1.20 costs \$495. Designers may obtain a free evaluation package by calling (800) 433-7801. *LM*

TEST DETECTS IC DEFECTS FROM QUIESCENT CURRENT

Traditionally, IC manufacturers use logic-response testing to evaluate ICs. A long series of test vectors is used as an input, and the circuit's output is monitored for proper responses. But these tests get very cumbersome with large ICs, and they can't find defects that could cause the circuit to fail. To locate hidden defects in the CMOS ICs it fabricates, Sandia National Laboratories, Albuquerque, N.M., developed a test based on the IC's quiescent current. The quiescent current is the amperage through a chip in its resting state when no switching voltage is applied. In a good CMOS chip, the quiescent current is low in all logic states. But a defective chip will have a greatly increased current in at least one logic state. Sandia says a chip with a high quiescent current should be considered defective because the current can cause premature battery failure or a malfunction in a customer's system. In addition to being more comprehensive, the new test requires fewer vectors and simpler software than the logic-response technique. For further information, contact Roy A. Hamil, (505) 844-7143. *JN*

FUSION PROGRAM BOOSTS SOFTWARE AVAILABILITY

Whenever new hardware emerges, the software needed to support new development efforts often seems to trickle out slowly. In an effort to correct that for its new Mach family of PLDs as well as for other forthcoming PLDs, Advanced Micro Devices Inc., Sunnyvale, Calif., created a Fusion program. It's a value-added support arrangement with third-party software, design tool, and programming-aid developers to accelerate the development of support products. To speed the process, AMD created silicon-specific software modules that are transferred to the tool developers and incorporated into the final product, hastening its release. The end products are then certified by AMD and released by the third-party tool suppliers. As a result, the support products can be released simultaneously with the release of the PLDs from AMD. Contact Andy Robin at (408) 732-2400. *DB*

COMPANY MERGER FORMS LARGEST GAAS IC MAKER

The proposed merger of two of the leading gallium arsenide chip manufacturers—Gigabit Logic Inc., Newberry Park, Calif., and TriQuint Semiconductor Inc., Beaverton, Ore.—promises to yield the world's largest merchant GaAs chip manufacturer. Such a merger should improve the efficiency of research and development activities because there will be less duplication of research projects and R&D funding will stretch further. The new company will be jointly owned by the existing investors and retain the TriQuint name. Digital logic products will be marketed under the well-established Gigabit Logic name, while monolithic microwave ICs (MMICs) and analog circuits will be sold under the TriQuint name. *DB*

NEW SPECIFICATION LETS UNIX ACCESS APPLE TALK

A specification developed jointly by Apple Computer Inc., Cupertino, Calif., and AT&T Computer Systems, Berkeley Heights, N.J., will offer a standard framework for programmers accessing the AppleTalk networking protocols from AT&T's Unix operating system (System V, release 4). With the specification, software developers can create Unix-based AppleTalk networking application programs that perform file sharing or handle electronic mail or client-server applications. The specification also enables the AppleTalk application software to be ported quickly from one vendor's Unix system to another's system. AppleTalk application programming interfaces, as described in the specification, are already implemented by AT&T. They're installed on the company's StarGroup server for Apple Macintosh clients. Apple plans to implement the interfaces on its next release of the portable AppleTalk source code that it licenses to developers. Contact Randy Battat at (408) 996-1010. *DB*

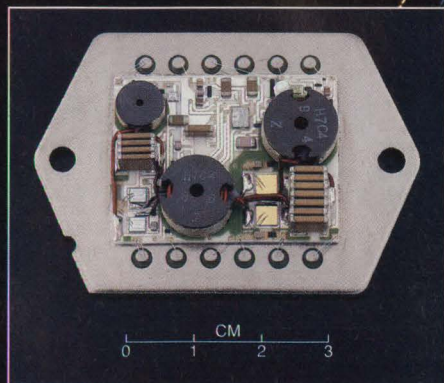
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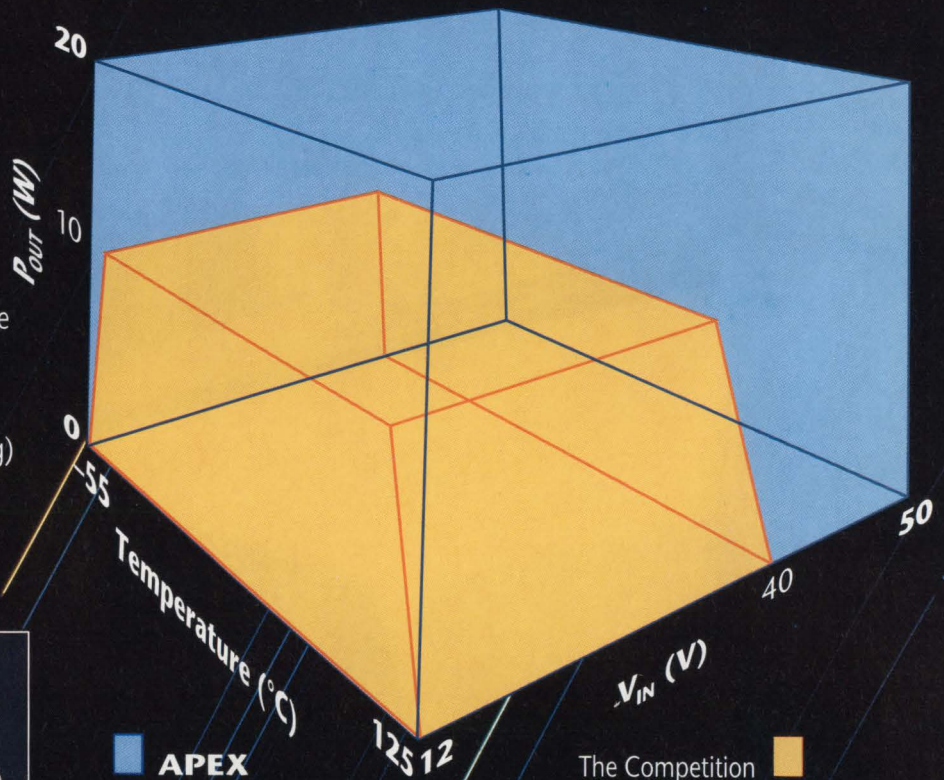
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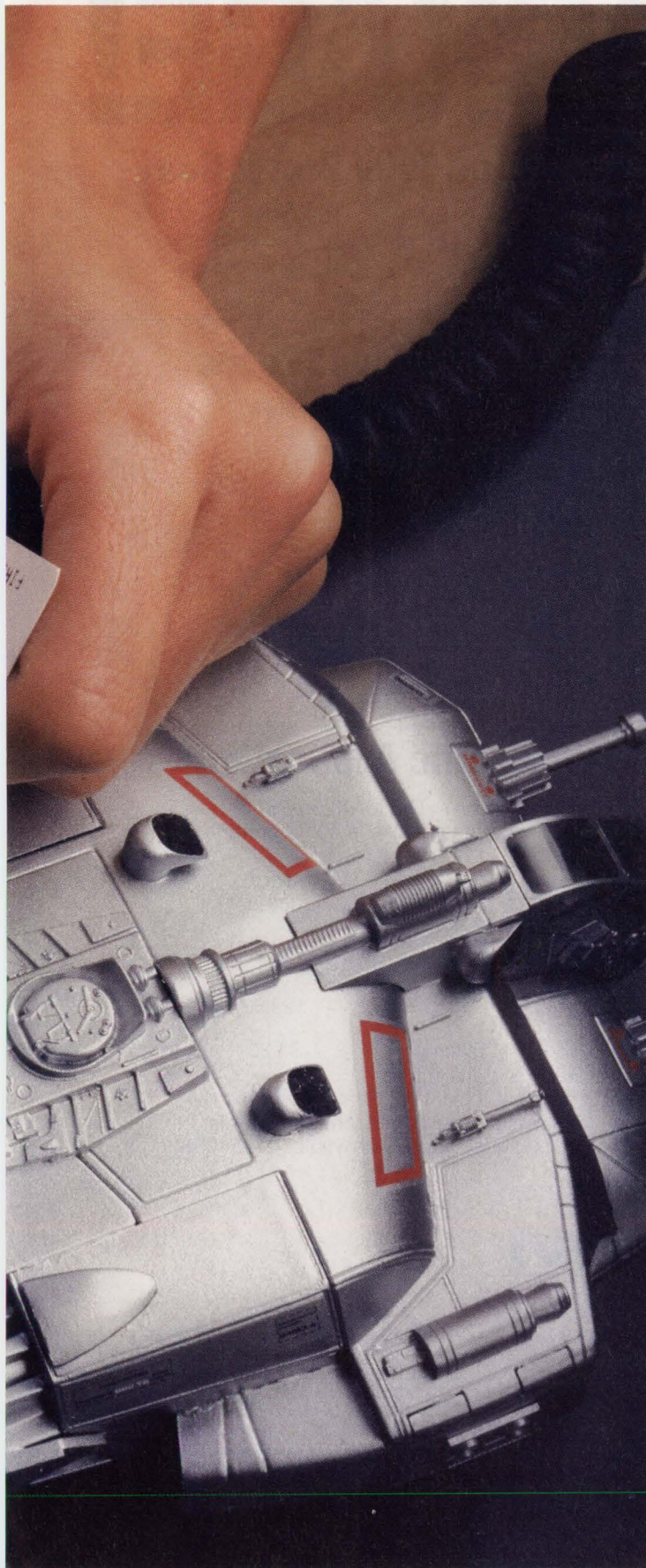


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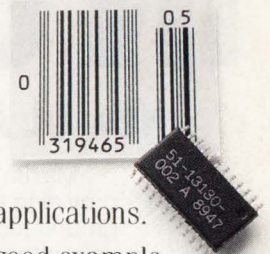
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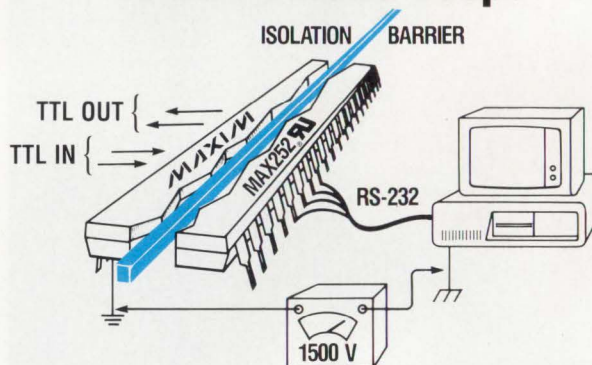
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NEXT-GENERATION RISC CPU GETS 50 TO 100 MIPS FROM 64-BIT INTERNAL ARCHITECTURE

Attracting customers has been relatively easy for CPU manufacturers—just make the CPUs faster and larger to achieve major improvements in throughput and system integration. However, most companies have already reached the practical limits of scaling. Consequently, attention must be paid to architectural changes so that the advantages of fine-line CMOS or bipolar processes are maximized.

The RISC architecture of the R2000 and R3000 family processors from Mips Computer Systems Inc., Sunnyvale, Calif., was innovative when first released. Since then, how-

ever, many tricks have been learned, both in silicon architecture implementation and in compiler design. Mips puts many of those improvements to work in its next-generation family, the R4000 series, to achieve throughputs of 50 to over 100 MIPS from a CMOS CPU.

The first change from the previous families is a move to a two-instruction-issue superpipeline. It increases the integer and floating-point performance beyond that expected for the clock speed. The approach employed by Mips also extracts instruction-level parallelism with no issue restrictions for load/load, load/store,

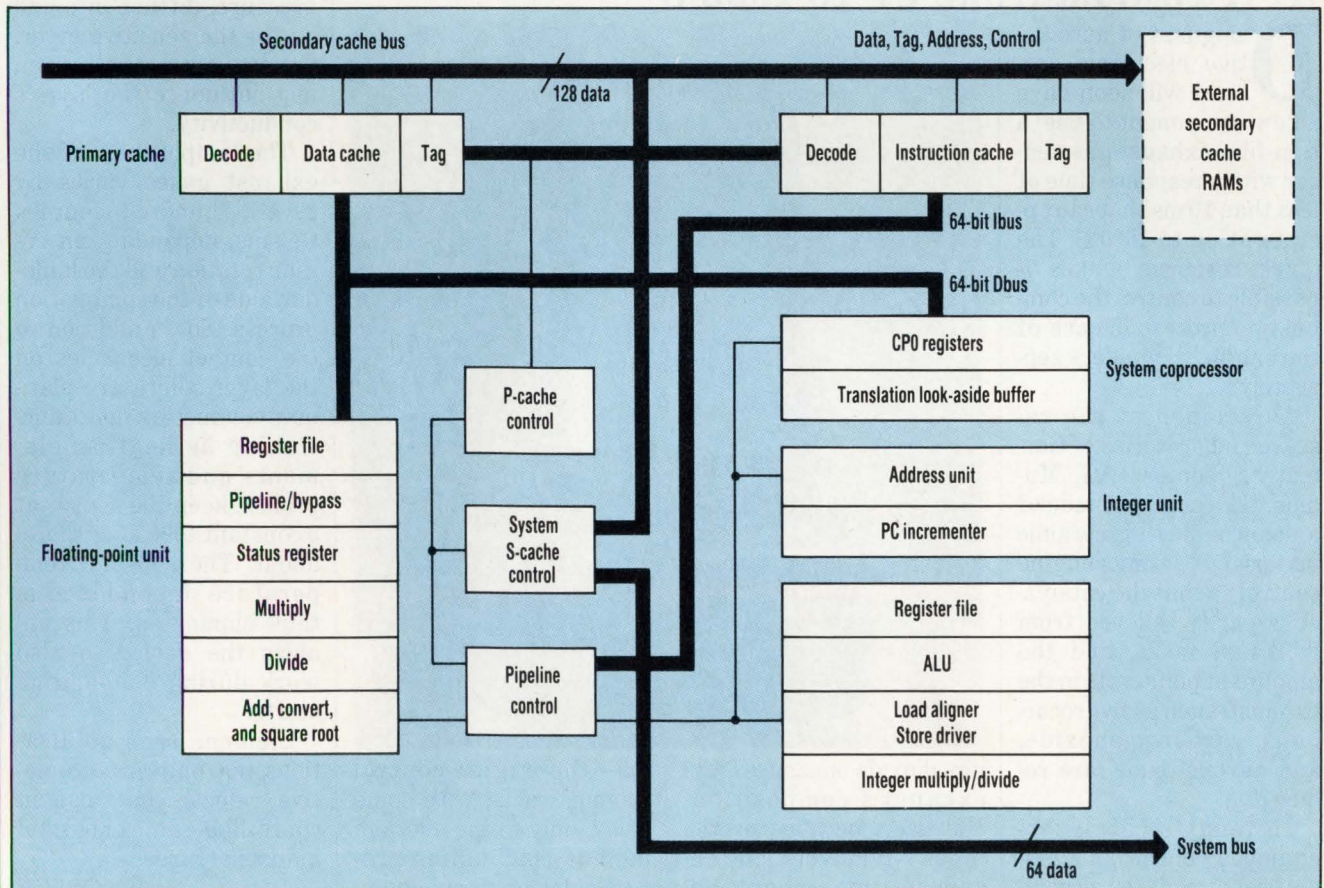
store/store, and ALU/ALU operations. A deeper instruction pipeline than the 5-stage pipeline employed on the R3000 enables the two instructions to be issued during each clock period so that more can be done every cycle.

Integration also plays a part in the forthcoming processor. Mips designers moved the processor to a full 64-bit architecture to give programmers access to a flat, unsegmented address space many times that of a 32-bit CPU. This type of address space will be needed by applications such as large data bases, display-list based graphics, and others.

To call the processor a

true 64-bit machine, designers at Mips feel the chip must handle a 64-bit virtual address, have a 64-bit integer ALU, contain 64-bit integer registers, offer 64-bit compatibility with 32-bit products, maintain 64-bit data paths to cache and main memory, and pack a 64-bit IEEE-754 compliant floating-point ALU. Making all of that possible on one chip required a considerable amount of integration to keep the pin-count reasonable. As a result, designers have combined a full 64-bit floating-point unit, instruction and data caches of 8 kbytes each with a 128-bit-wide interface to external memory, and a 64-bit integer processor with a 64-bit interface to external systems (*see the figure*).

The embedded cache



controllers ensure data integrity by providing parity protection on the primary caches, and error checking and correction on the secondary, off-chip cache of 128 kbytes to 4 Mbytes. That secondary cache can be set as either a split instruction/data cache, or as a joint secondary cache. An on-chip translation look-aside buffer holds up to 96 entries, all lockable, and permits a cache coherency policy to be set on a per-page basis. Both the cache depth and line size are configurable. Furthermore, to ease multiprocessing applications, physical tags supply flags to programs.

As part of the multipro-

cessing features, the cache controller responds to requests for secondary cache snoops, cache invalidates, and updates, all independent of the CPU. Synchronization primitives are designed around cache coherency mechanisms; synchronization doesn't depend on long bus locks. The controllers support snoopy, directory-based, and other interconnection schemes. As a result, they give designers the ability to fine-tune the memory subsystem for optimal performance in a particular application.

To ease system software development and hardware debugging, Mips also

included some debug features on the chip—a watch breakpoint register for software debugging, a fine-grained process timer, and exception-state and diagnostic registers. Also included is a JTAG-compatible external boundary-scan test port, and a tightly coupled master/checker interface if redundant CPUs are needed to ensure maximum system software integrity. Many other system interface features have been added so that hardware designers can optimize the interfaces for memory timing, signal slew rates, and data ordering.

DAVE BURSKY

It then adjusts the composition of the fuel-air mixture accordingly. The control system can't optimize the combustion process in individual cylinders.

The new Siemens exhaust gas sensor overcomes this problem to help provide a cleaner exhaust. Its short, 10-ms response time results from the thin sensor layer it uses. In fabricating the sensor, a 1- μ m film consisting of a semiconducting metal-oxide material is deposited by reactive-cathode sputtering on a ceramic substrate of aluminum oxide. The sensor is about 3000 times thinner than conventional lambda probes.

The materials' sensing effect derives from the oxygen ions that, in accordance with the environment's partial oxygen pressure, diffuse into and out of the sensitive layer. Consequently, the oxygen ions influence the layer's conductivity.

The temperature of the exhaust gases varies by several hundred degrees Celsius, depending on engine rotation and the lambda value of the combustion process. So, in addition to the contact electrodes on the layer, there are platinum conductors that, functioning as heating elements and temperature probes, keep the sensor at a constant 1000°C, or thereabout. The sensor's temperature dependence is thus eliminated. This enables the device to also work during cold-engine starts.

Siemens sees applications not only in automotive vehicles but also in controllable household and industrial furnaces.

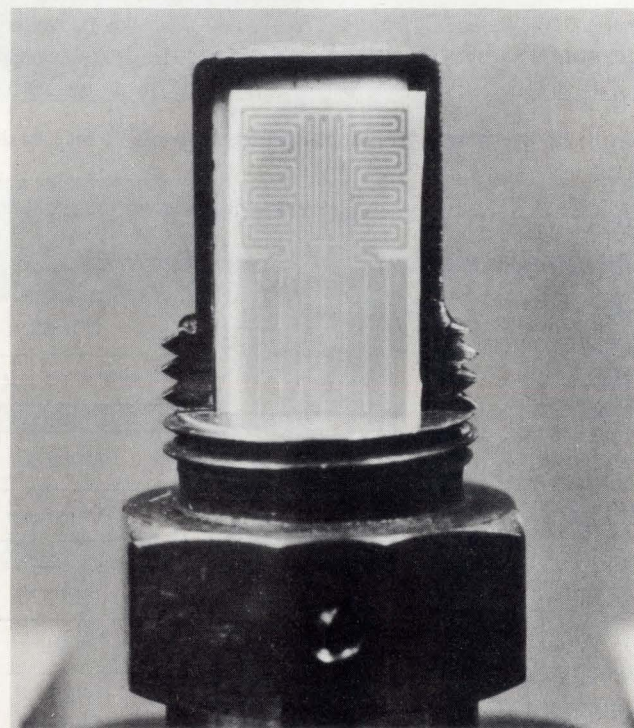
JOHN GOSCH

AUTOMOTIVE GAS SENSOR WORKS IN 10 MS AT A TEMPERATURE UP TO 1000°C

Designers of automotive electronic systems will soon have a new component to use: a thin-film exhaust-gas sensor with a response time of less than 10 ms that can operate at up to 1000°C. The quick response makes it possible to control the combustion process in each of the engine's cylinders separately.

Developed at the research laboratories of Germany's Siemens AG, Munich, the sensor is made of a semiconducting ceramic material. It permits engine control so that the catalyzer is partly relieved from its usual tasks, and the amount of pollutants in the exhaust, such as hydrocarbons, carbon monoxide, and nitrous oxide, are reduced.

In today's catalyzer-equipped vehicles, a lambda probe made of zirconi-



um dioxide measures the exhaust's composition. However, because of the probe's relatively long response time—about 100

ms—the engine-control system reacts, with some delay, only to the average lambda combustion-process value of all cylinders.

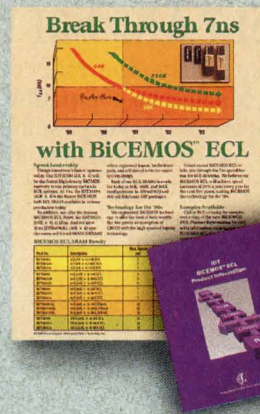
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APPLE MACINTOSH CLONES NOW POSSIBLE WITH THREE-CHIP SET AND SOFTWARE

A soon-to-appear landmark chip set will let designers create a fully compatible system that runs Apple Macintosh software without tapping into an original ROM set. Start-up Nutek Computers Inc., Cupertino, Calif., the set's developer, states that it has worked in a "total clean-room environment" for the last two years. The company has been crafting the motherboard chip set and system software to duplicate all of the functions of the Macintosh, making it possible for companies to build low-cost NuBus-based compatibles.

Currently, the market for Macintosh-compatible computers is very small since most require that another Macintosh be cannibalized or that a ROM-based operating system be obtained from Apple. However, if a legal, compatible operating system, user interface, and underlying hardware such as Nutek's can be established, analysts predict a market with a high growth potential.

Nutek is hoping to create an Apple-compatible marketplace similar to the IBM PC-compatible market that chip-set makers in the last decade created. It

has designed the three key elements needed by a computer system manufacturer—the logic chip set, the internal operating system, and a graphical user interface. The chip set will consist of three rather complex custom chips that replicate the principle logic functions of a Macintosh system board. Designers only need to add the SCSI controller, CPU, up to 64 Mbytes of RAM, and some glue logic.

A Macintosh-compatible operating system will be supplied on a disk and boot ROM combination. The combination is similar to

that used by the IBM PCs, allowing simple software updates of the operating system. It will enable companies to design full-function personal computers that run all Macintosh published specifications. The combination will also work with nearly all standard add-in boards and peripherals that come from both Apple and third-party developers.

Of the three chips, two incorporate a NuBus interface that can tie into standard Motorola 680X0 microprocessors and supply all of the memory management. The third chip handles all of the I/O functions. Included on it are the serial ports, sound input and output channels, flop-

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Dear Brad,

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TECHNOLOGY ADVANCES

py-disk controller, and keyboard and mouse interfaces.

The chips have been implemented in prototype form and are undergoing simulation and validation testing at the company's laboratories. They're designed to support burst-mode memory transfers, DMA, sound generation, and as part of the floppy disk controller, to give the user the same capability as the Macintosh Superdrive, reading and writing Macintosh and DOS-compatible 3.5-in disks.

With the chips, systems operating at clocks up to 33 MHz can be implemented. Although that clock speed is lower than the 40 MHz used by Apple's top-of-the-

line 68030-based IIfx, designers can actually leapfrog the IIfx's performance by basing system designs on the more powerful 68040. The 68040 operates at 25 MHz, and will probably have a 33-MHz upgrade option in the next year.

One minor difference in Nutek's system implementation is that there will be no equivalent to the Apple Desktop Bus that's typically used to connect the keyboard and mouse to the CPU. Instead, system designers will have to employ direct-connect keyboard and mouse ports, much like the IBM PC and compatibles world.

Written from the ground up without reference to the

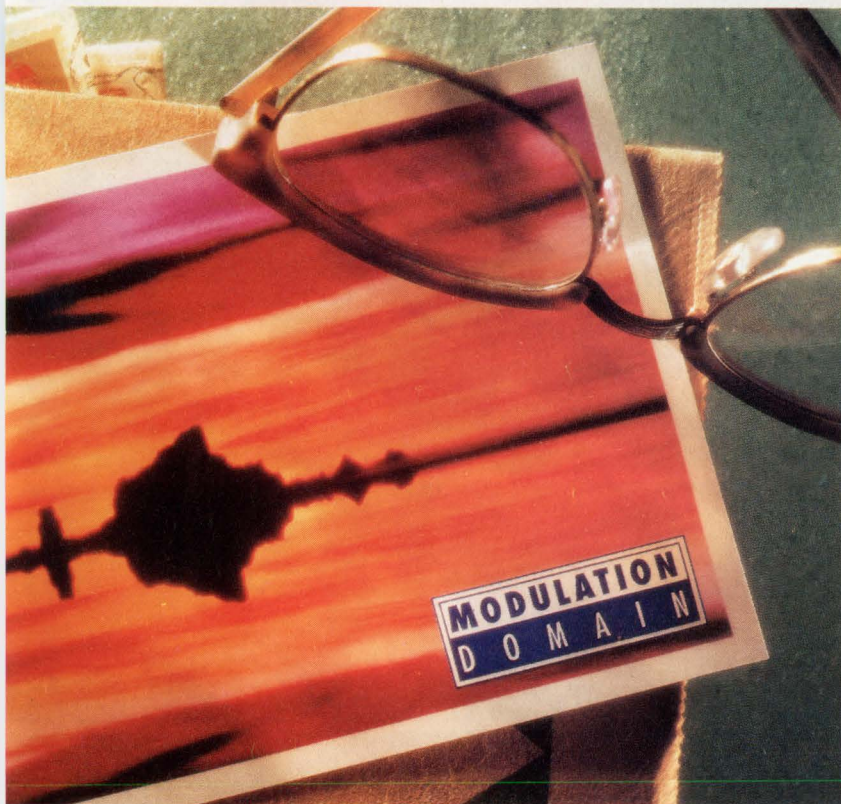
internal code of the Macintosh, the operating-system software will replicate the more than 760 specific functions performed by Apple's operating system. The company will base its user interface on a native-language version of the Motif graphical user interface from the Open Software Foundation, and will incorporate the functionality of Apple's version 6 of the Macintosh operating system. Although the software incorporates the same windowing functionality as the Macintosh user interface, the Motif images have a more three-dimensional appearance. Furthermore, in the Nutek approach, the menu bar appears at the upper edge of

the top-most window instead of always just appearing at the top of the screen, as in a Macintosh display.

The Motif-based interface will also be offered as a standalone package for existing Macintosh users. Samples of the chips and final software will be ready in the fourth quarter. However, unlike chip-set suppliers in the PC industry who offer products to all purchasers, Nutek would like to establish partnerships with a limited number of system manufacturers. Licensing fees, chip prices, and royalty arrangements haven't yet been established. Contact Benjamin Chou at (408) 973-8857.

DAVE BURSKY

a fix on jitter.

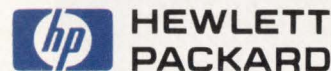


Until now, when you looked at jitter on an oscilloscope, all you could see was fuzz. And the only way to find the source was by trial and error. In the Modulation Domain, you can actually display jitter as a function of time. That way, you know exactly how much there is and when it occurs, so it's easier to tell where it comes from. You can even examine the jitter spectrum and quantify the jitter gain (transfer function). All in a matter of minutes.

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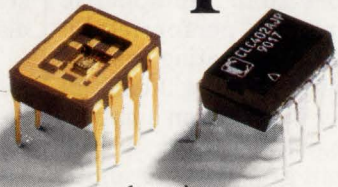
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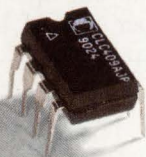
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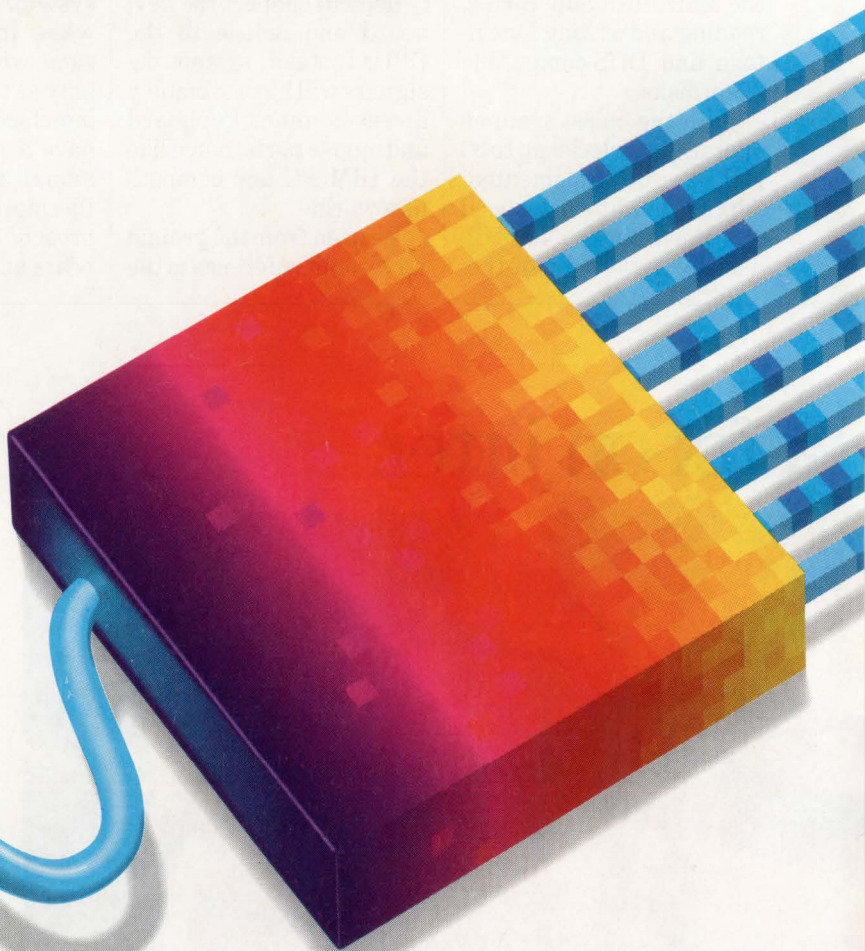
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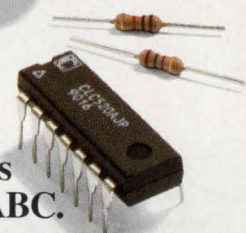
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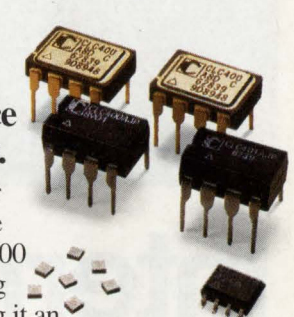
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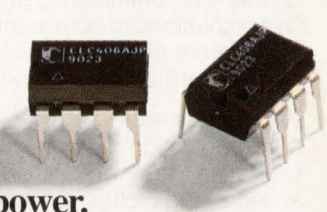


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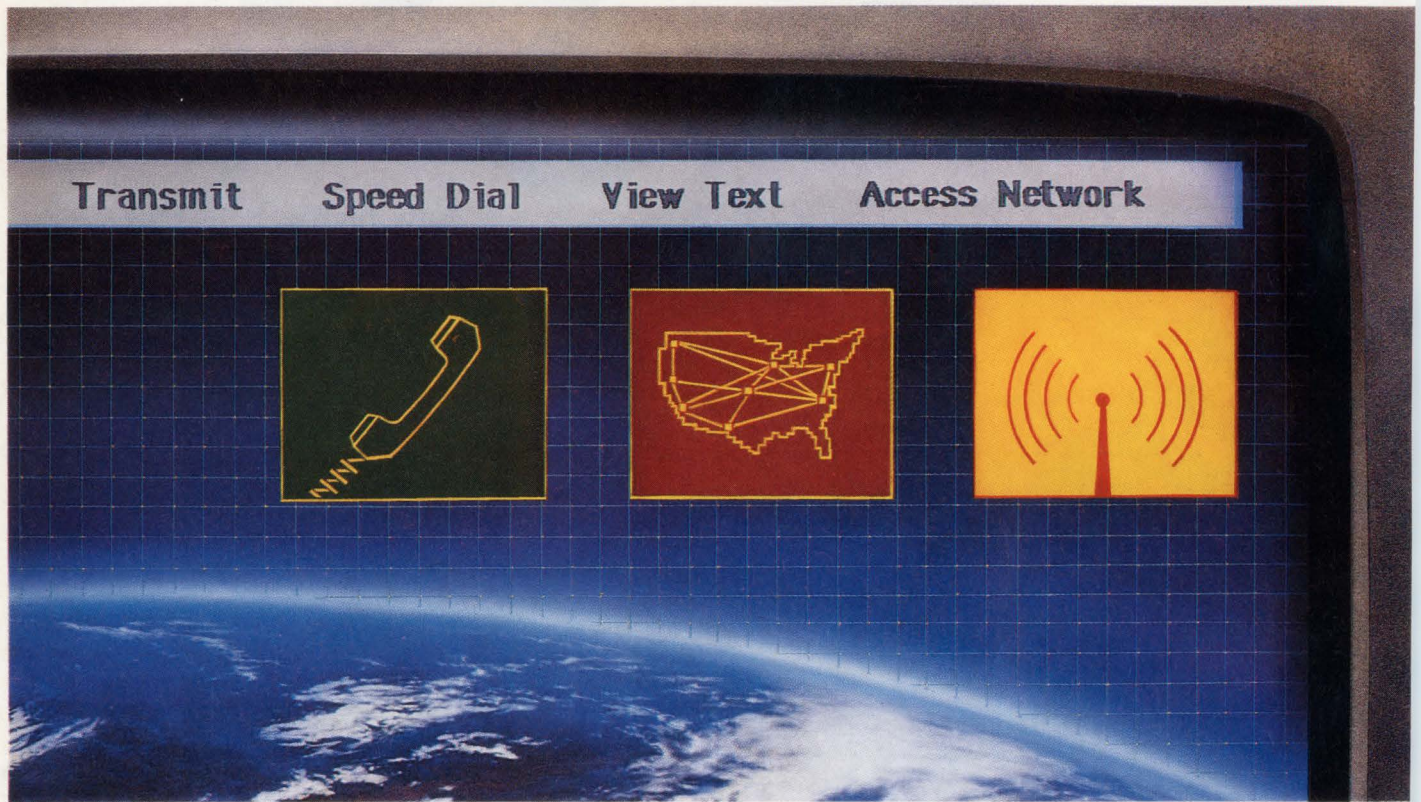
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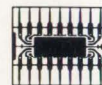
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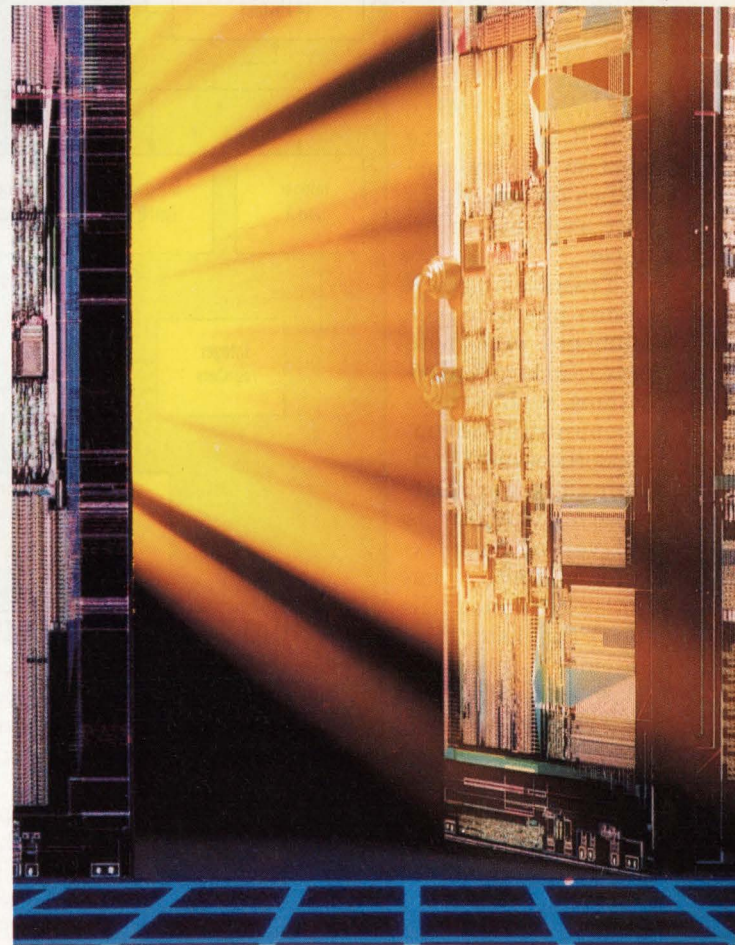
WITH A PEAK THROUGHPUT OF 100 MIPS, A 64-BIT EMBEDDED CONTROLLER PACKS DSP ENHANCEMENTS TO ALSO HANDLE IMAGE AND SIGNAL PROCESSING.

DAVE BURSKY

Meeting each different system processing requirement with a separate dedicated controller or application-specific IC may soon be passe. The new wave for general-purpose controllers, as they get more powerful, is to have them include specialized subprocessors. By combining a 64-bit superscalar general-purpose processor with a floating-point math unit and digital-signal processing functions on one IC, National Semiconductor has created a multiple-processor chip that can be shared by several embedded-control tasks in the same system.

By downloading a new control program, the 1.1-million-transistor chip, code-named Swordfish, can be switched from serving as, say, a laser-printer controller to a fax-modem processor, data modem, or an image processor. As a result, this one IC could replace the dedicated controller and the signal or image-processing chips currently used in such applications. And the ability to handle multiple tasks at high speeds could help create new types of multifunction peripherals that would, for instance, combine printing, scanning, data compression, and data communications.

To manage all of those tasks, designers gave the Swordfish processor a full 64-bit internal architecture with two four-stage integer pipelines, as well as other hardware and software enhancements. Furthermore, an on-chip IEEE-754-compatible double-precision floating-point unit (FPU) has its own pipeline. This enables



both integer and floating-point computations to be done in parallel (except for multiplications, because the multiplier is used by both the FPU and integer units). During one cycle, the chip can execute either two integer instructions or one integer and one floating-point instruction.

The processor is designed to run from an external 25-MHz clock oscillator. At that clock rate, the processor can execute 100

COMBO CPU/DSP EMBEDDED PROCESSOR

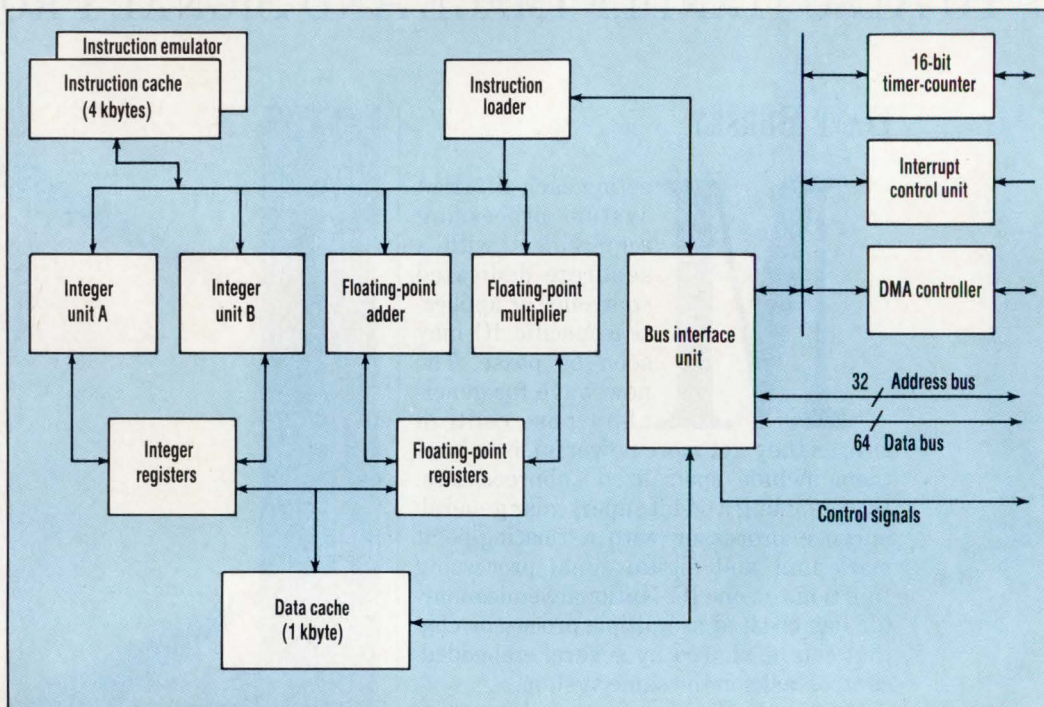
million instructions per second (MIPS). If that throughput number doesn't seem to follow from the oscillator frequency, you're right. The chip designers actually included a phase-locked loop on the chip. The PLL doubles the clock frequency so that internal logic runs at 50 MHz. And, because the chip executes two instructions per clock, it can hit the 100-MIPS mark. When running at 50 MHz, the processor executes 115,000 Dhrystones/s and 20 MFLOPS for the double-precision Linpack inner loop. Another advantage to the lower-frequency external clock is that system designers can run off-chip hardware at 25 MHz, which reduces the system cost and simplifies the board layout and bus interfaces.

Translating all those performance numbers into more practical terms, algorithms, such as those encountered in image processing (1024-point integer fast-Fourier transforms as well as complex-integer finite-impulse-response filters), run faster than on most dedicated DSP chips. For instance, according to National, when compared with the DSP56001 from Motorola Inc., Austin, Texas, the Swordfish executes the integer FFT about 70% faster, running the algorithm in just 1.5 ms (National bases this comparison on DSP56001 performance data reported in the October 1989 issue of "Microprocessor Report," published by MicroDesign Resources Inc., Sebastopol, Calif.). A 1024-point floating-point FFT takes just over 1 ms on the Swordfish, while an 8-by-8 discrete cosine transform needs just 35 μ s with integer numbers and 32 μ s when using floating-point numbers.

Similarly, a complex finite-impulse-response filter section takes just 1/3 the time, running in just 100 ns/tap. In laser-printer applications, National estimates that the processor runs Adobe Postscript files at least twice to three times as fast as the 25-MHz Am29000 RISC processor offered by Advanced Micro Devices Inc., Sunnyvale, Calif. (based on AM29000 performance data published, again, by "Microprocessor Report"). That RISC chip previously held the speed

technology, lets the processor achieve more than a six-fold throughput improvement. Programs written in 32000/EP assembly language can be assembled by the Swordfish assembler and generate Swordfish binary code. Although the Swordfish is the first National chip to use the superscalar RISC architecture, it won't be the only one—the core CPU can be used to create other family members.

The high throughput, explains



1. DUAL INTEGER PIPELINES plus a separate floating-point pipeline let National's Swordfish superscalar processor deliver a peak throughput of 100 MIPS when running from a 25-MHz external clock. An on-chip phase-locked loop doubles the input clock frequency, and two instructions can be executed each clock cycle to achieve the 100 MIPS. To support the embedded control tasks, the chip also packs a counter-timer, an interrupt controller, and dual DMA channels for fast data movement.

title for Postscript printers.

The Swordfish is the latest addition to National's family of embedded 32-bit processors, which started with the 1-MIPS 32CG16 and progressed up to the 15-MIPS 32GX320 released in 1990. Although the Swordfish maintains the basic programming model of the previous CG and GX CPU cores and is assembly-language compatible with the previous members of the 32000/EP family, it employs an advanced RISC architecture. That architecture, coupled with optimizing compiler

Ran Talmudi, engineering manager of National's design center in Herzlia, Israel, is because the two integer pipelines are virtually identical: both can handle integer arithmetic operations and load/store instructions. Consequently, the compiler has an easy time distributing operations between the two pipelines. In contrast, explains Talmudi, the i860 superscalar processor from Intel Corp., Santa Clara, Calif., imposes restrictions on the instruction combinations that can be assigned to either of the two pipelines on that chip. It's not that

COMBO CPU/DSP EMBEDDED PROCESSOR

National's chip has no restrictions. One such recommendation is that branch and jump operations should be assigned to pipeline B. However, these conditions can be handled by the high-level-language or source-code compilers.

The dual integer pipeline A and B paths share the data and instruction caches of 1 and 4 kbytes, respectively, as well as a six-port register file that permits four reads and two writes every cycle (Fig. 1). With the caches, the dual integer units quickly access data and instructions and thus continually run without waiting

pointer, the processor status, and dispatch table for interrupts and traps. The FPU section has its own bank of 32, 32-bit registers that can also appear as 16, 64-bit-wide registers for double-precision operations.

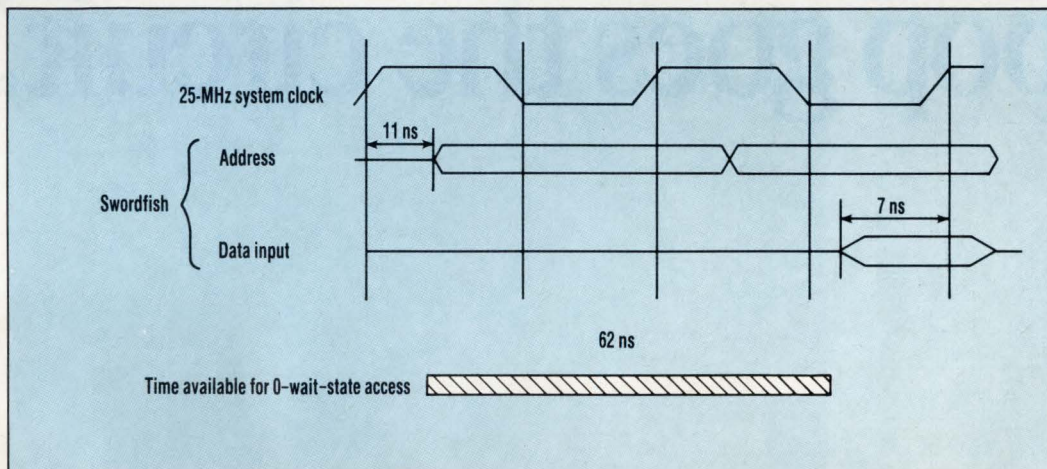
One special feature of the chip, in its integer mode, is its complex-number-calculations ability. Two of its 32-bit registers can each be split into two 16-bit half words. With two special half-word multiplication instructions, just five cycles are required for the 10 operations (two loads, four multiplications, and four additions) needed for a complex signed-16-bit

sure the data in the cache and external memory are as current as possible. A load-scheduling mechanism is used by the D-cache to prevent pipeline stalling with a cache miss.

Because the Swordfish was designed for embedded control applications, other resources were added on the chip—a 16-bit counter-timer, a two-channel DMA controller, and a 15-level interrupt-control unit. The timer can be used in a pulse-width-modulated (PWM) mode, as an external-event counter, or as an input-capture register. Both fly-by and memory-to-memory transfer operations are possible

with the DMA controller, and up to 15 encoded interrupt-priority levels can be dealt with by the interrupt controller.

The chip's bus interface is very efficient — just one clock per address or data transfer is needed and support logic on the chip permits dual interleaved banks of memory and/or cache for maximum bus bandwidth. Thus, when operating with a 25-MHz system clock, the Swordfish gives the system over 60



2. BY DOUBLING THE INTERNAL operating frequency and keeping the external bus interface at a frequency of 25 MHz, the Swordfish's memory timing becomes very relaxed: Off-chip memory accesses have 62 ns available while still maintaining zero-wait-state operation. That makes it possible for relatively low-cost dynamic RAMs to be used. In comparison, other RISC processors typically require expensive high-speed static RAMs or complex, interleaved memory subsystems.

for new data. Similarly, the multi-port register file allows both integer units to each read two operands simultaneously and write back a result. Dedicated logic resolves data dependencies between concurrently executed instructions.

The register file contains 32 general-purpose 32-bit registers. Half of those registers can be restricted for use by the chip only when it enters its supervisor mode. By allocating the registers this way, 14 of the general-purpose registers can be dedicated to handling high-priority interrupts. That speeds interrupt service by eliminating the need to save and restore registers. Just four extra registers hold all of the CPU key values—the program counter, the stack

multiply-accumulate calculation. For integer operations, a full 32-by-32-bit multiplication executes in one clock cycle. The calculation is done on the FPU's multiplier. Thus, during the same cycle, only a floating-point ALU operation or a second integer operation can be done in parallel with the multiplication.

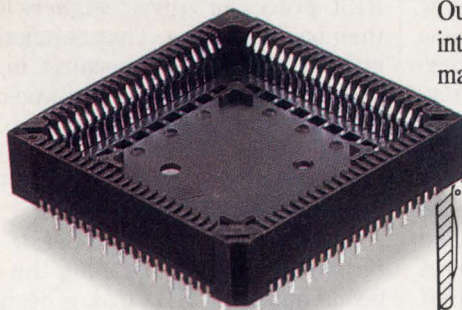
The data and instruction caches are both two-way set associative and allow individual line entries (eight bytes) to be locked to ensure that critical code or data doesn't get invalidated. Up to 1024 instructions (32 bits each) can be held in the I-cache, while up to 1 kbyte of data can go in the D-cache. Hardware supports cache coherency, while a write-through algorithm is employed to en-

ns per access to achieve zero-wait state operation (Fig. 2). Most other RISC processors give designers less than half that time. That restriction inflates system cost because high-speed static RAM or fast static-column dynamic RAMs would be required. With National's chip, low-cost standard DRAMs used in the page mode would be sufficient.

Although the chip can operate internally at 50 MHz, running the external bus at 25 MHz makes designing the bus interface much simpler. However, if high-speed external peripherals are available, the internal clock doubler can be bypassed and a 50-MHz clock fed into the chip.

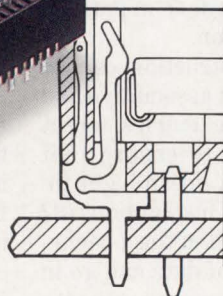
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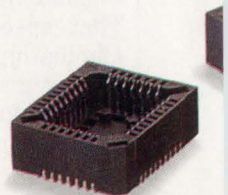
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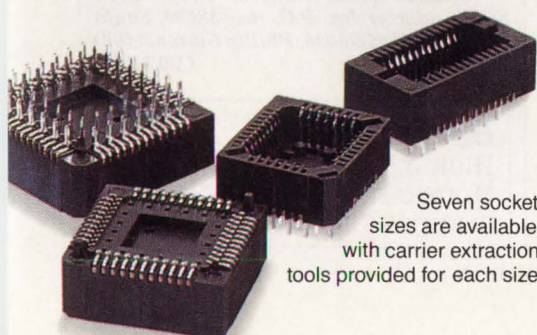
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COMBO CPU/DSP EMBEDDED PROCESSOR

development processes—the chip designers included three hardware breakpoints for instructions and data, and an on-chip 32-bit counter that can be used during performance analysis. Also included in the chip's design is an in-system emulation mode that allows designers to trace the internal program counter. One part of the emulation mode is a serial line, which makes it easy to reload or unload the chip's internal registers.

Furthermore, once the chip is designed into a system, a self-test capability lets users test the I/O buffers, initiate an internal self-test upon reset, and initiate an external-memory self-test. In systems needing extreme integrity, a shadow mode can also be invoked—one processor monitoring the operations of another. If a mismatch occurs, the shadow processor signals that an error occurred and holds that condition until the master processor is reset.

Software and hardware development tools will include a C-language compiler, assembly-language debuggers and monitors, and a development board with the Swordfish. DRAM, EPROM, serial I/O, an Ethernet port, and an expansion connector for the AT bus are also included on the board. The software tools will first be set to run on the Sun Sparc-Station platforms, plus the Hewlett-Packard HP 9000 series and Opus Systems' RISC-based platform. □

PRICE AND AVAILABILITY

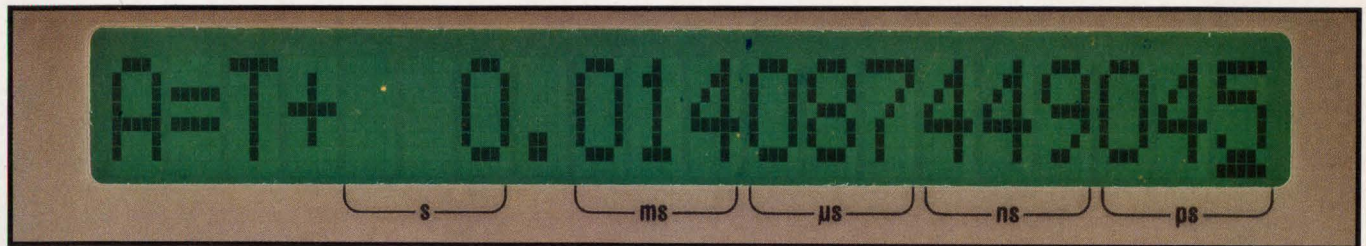
The Swordfish processor, also known as the NS32SF640, will initially come in a 223-lead pin-grid-array package. Engineering samples will be available in the third quarter. Engineering samples of a 33-MHz internal-clock version will sell for under \$1200 in single-unit quantities. An evaluation board, in single units, will go for \$10,000. An assembler and associated software tools for VAX hardware will run \$6000; for Sun workstations, the cost is \$3000. C compilers for the VAX and Sun workstations are priced at \$3000 and \$1800, respectively.

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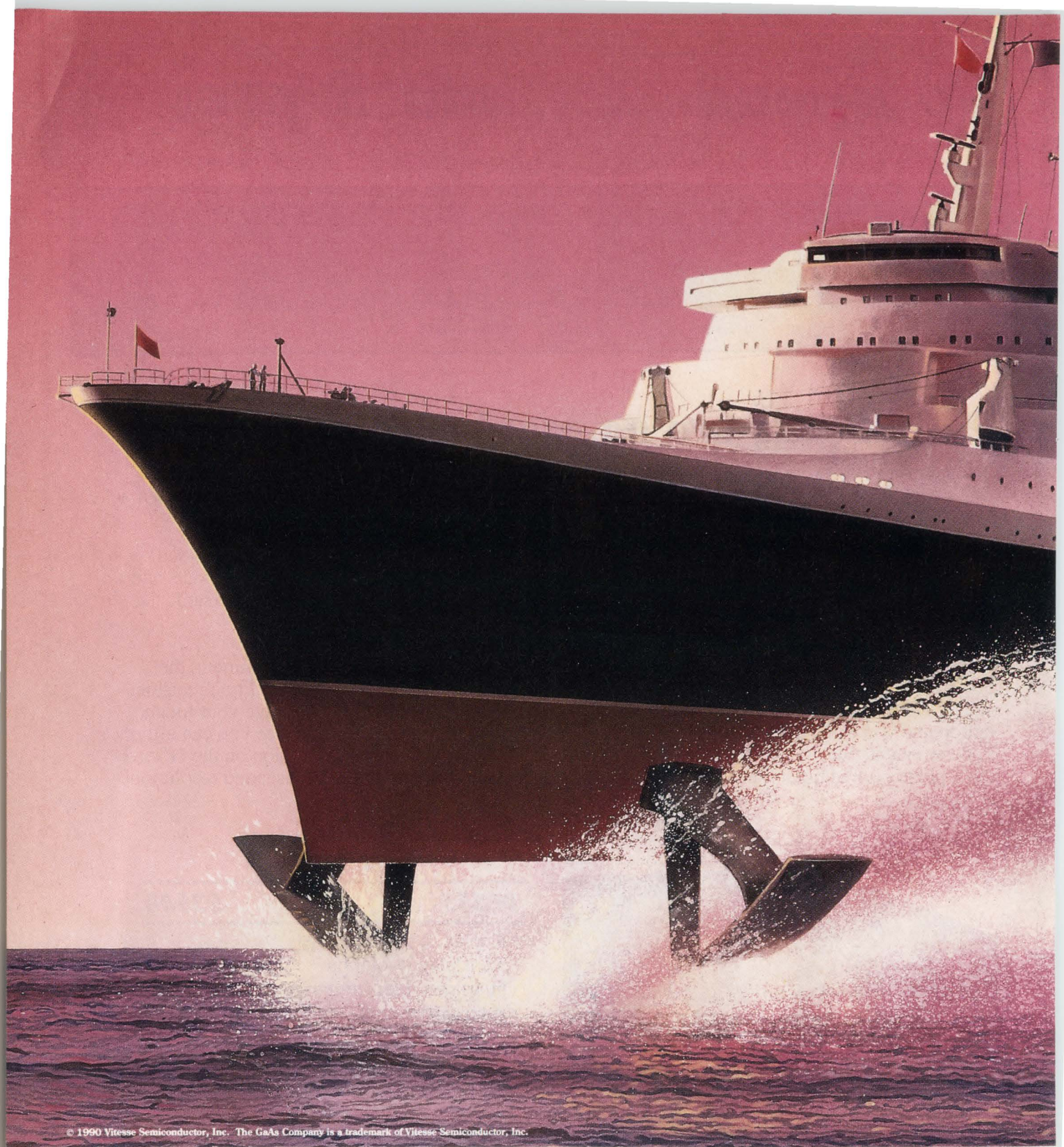
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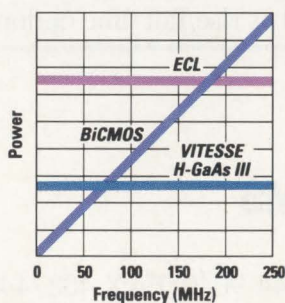


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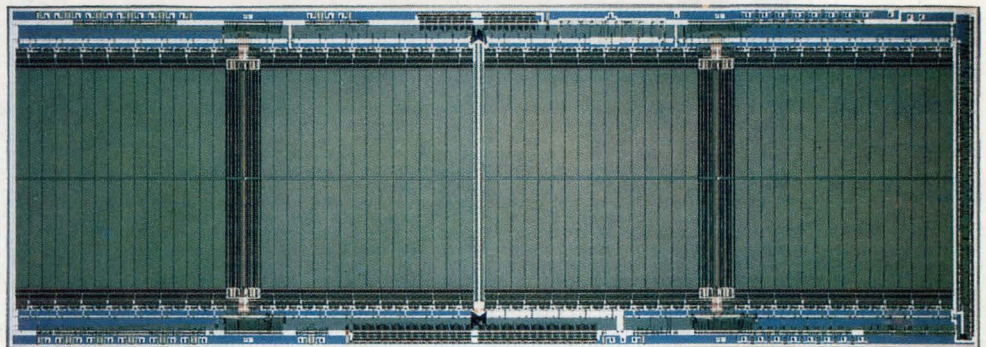
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The 38th annual International Solid State Circuits Conference, held in San Francisco this year from Feb. 13 to 15, again is a gallery for the major advances in integrated circuit designs. For nearly 40 years, the conference has pictured the cream of the crop of avant-garde developments in semiconductors. The Electronic Design Special Report on the following pages presents the highlights of the 1991 ISSCC in three sections: digital, analog, and communications technology.

In the overview of digital technology, written by Semiconductors Editor Dave Bursky, tremendous strides in system performance resulting from the ability to put more than a million transistors on a CPU chip or several



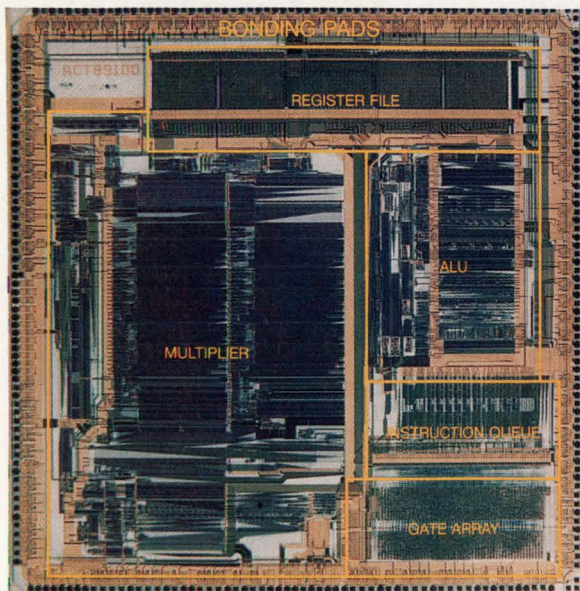
MITSUBISHI ELECTRIC CORP.

hundred thousand gates on a logic chip are presented. We see the impact of pipelining techniques on throughput, the refinement of RISC architectures, the potential of neural network ICs, and more. Each year, the ISSCC takes on more of an international flavor, and this year's conference marks the first time that significant developments in the Soviet Union are covered. A sidebar within the digital technology section summarizes many of the advances described at the conference.

Following the digital section is an overview of analog IC developments by Analog Editor Frank Goodenough. This section canvasses the many IC implementations that employ sampling techniques of one form or another.

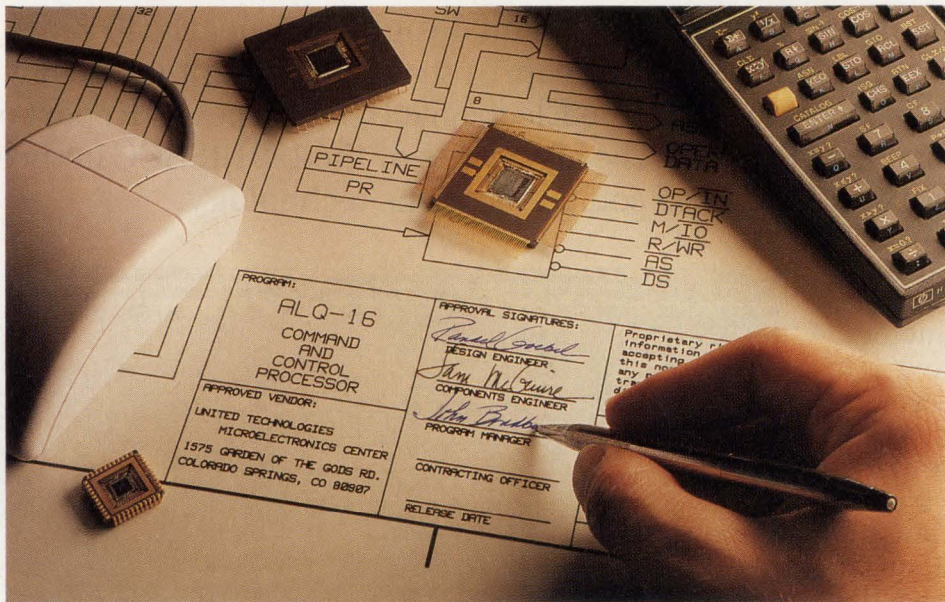
The Report concludes with a description of advances in communications devices by Communications and Industrial Electronics Editor Milt Leonard. Here, the emphasis is on single-chip receivers, digital-signal-processing ICs, and imaging.

As in past years, Electronic Design's editors extend our thanks to the 1991 ISSCC committee members and the conference authors for their cooperation. Without their help in obtaining details of the technical papers, we could not have developed this comprehensive Report for our worldwide readers.



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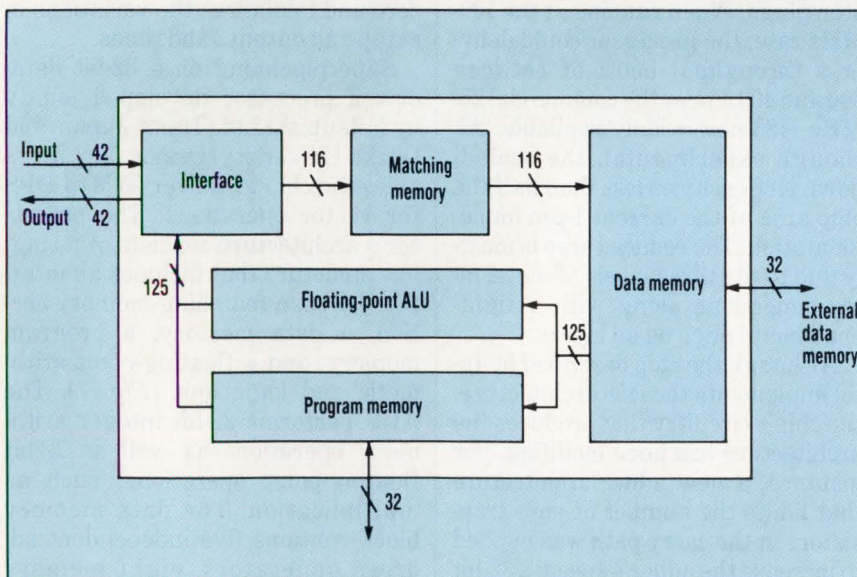
DIGITAL TECHNOLOGY

The past few years have seen the catch-phrase "a system on a chip" describe the huge leaps in the level of integration possible on a VLSI chip. However, the CPUs with over a million transistors, the logic circuits that pack several hundred thousand gates, and the memory chips that pack 64 million storage cells described at this year's ISSCC illustrate that our past perceptions of systems were somewhat rudimentary and simplistic. The new levels of integration go far beyond the brute-force packing of more of the same type circuitry on chips. They're opening the door to far more complex, more functional systems on one chip.

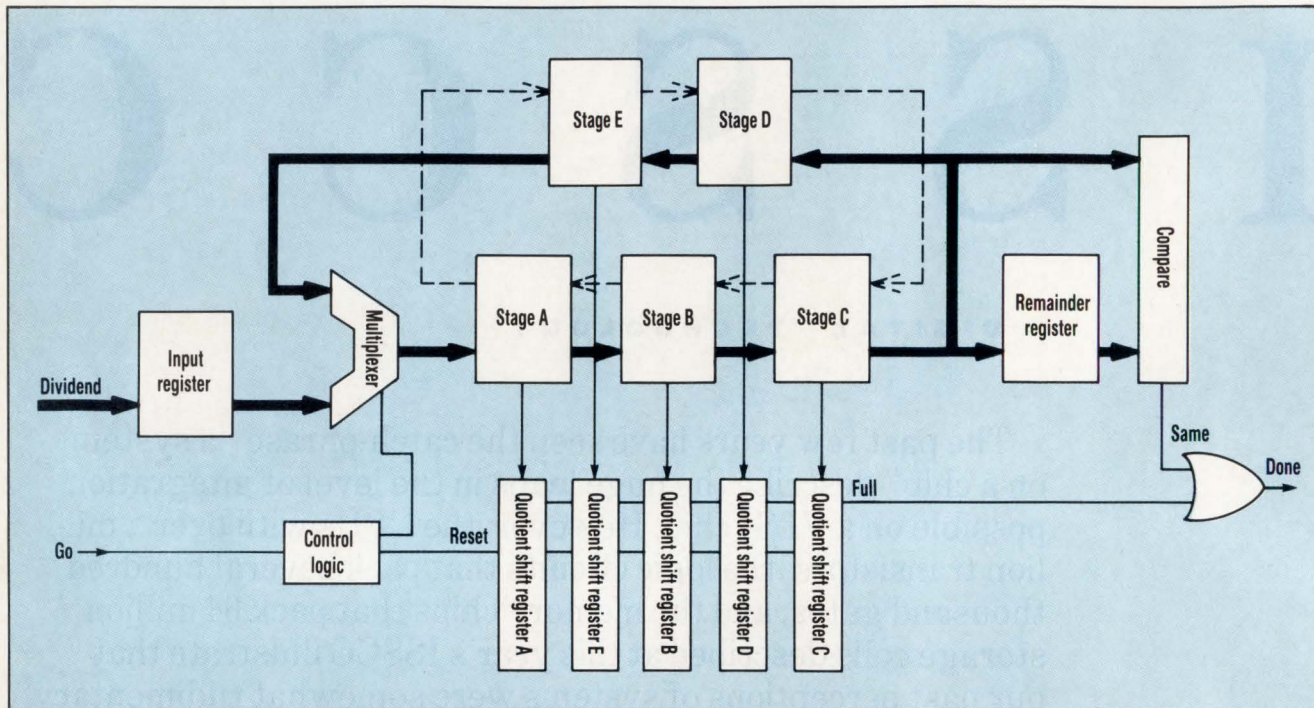
Today's advanced CPUs, for instance, are much more sophisticated than those of just a few years ago. They take advantage of much more

on-chip parallelism and significant amounts of closely coupled on-chip memory. With such resources, processors now achieve supercomputer-level performance numbers, with throughputs hitting 100 million instructions/s (MIPS).

One such processor, a 64-bit superscalar device with an on-chip floating-point unit and enhancements to han-



1. WITH SUPERPIPELINING APPLIED to a data-flow processor, computational rates can hit 50 MFLOPS for single-precision floating-point computations. Mitsubishi used a self-timed clocking scheme between functional blocks to eliminate problems due to high-speed clock skew and distribution.



2. A SELF-TIMED 54-BIT DIVISION CIRCUIT employs five computational stages, each consisting of multiple carry-save adders, carry-propagate adders, and other elements. Each of the five stages implements one step of a modified radix-2 redundant division algorithm. As the bits in the quotient are determined, they're collected by the five quotient shift registers.

dle digital-signal processing (DSP), is the result of research at National Semiconductor Corp., Santa Clara, Calif. The processor employs a 64-bit-wide data bus, and contains two identical 64-bit integer units as well as a separate 64-bit floating-point pipeline. To make it easier to embed the chip into systems, designers start with a 25-MHz off-chip clock. Then by using an on-chip phase-locked loop, the frequency can be doubled internally so that the chip runs at 50 MHz. And, when running at 50 MHz, the chip can execute two instructions every internal clock cycle, thus hitting the 100-MIPS throughput claim. The DSP enhancements also let the chip tackle such applications as data and voice communications, facsimile, and image processing at performance levels comparable or better than some dedicated DSP chips (*for more about the National processor, see "Combo CPU And DSP Chip Performs A Sea Of Tasks," p. 41*).

Designers at Intel Corp., Santa Clara, Calif., were able to push their i486 processor's speed to 100 MHz by

taking its architecture down to a sub-micron process (0.6- μ m effective gate width). The process employs three levels of metal that have planarized dielectric layers with tungsten plugs. When running at the 100-MHz rate, the processor could deliver a throughput boost of between 300 and 400% over the commercial 25-MHz i486 now widely available. Although experimental, the scaled-down i486 occupies less than half the chip area of the current 1- μ m implementation. The reduced area is mostly due to the three levels of metal interconnections along with a tightened metal pitch on all layers.

Although the chip described by Intel implements the i486 architecture, the chip's circuitry that produces the architecture has been modified. For instance, a new adder architecture that limits the number of pass transistors in the carry path was applied to increase the adder's speed: a 32-bit carry path takes just 1.8 ns. As the chip area decreases, so do the values of the performance-degrading parasitic elements. In addition, to reduce clock skew and I/O timing, Intel de-

signers also applied a phase-locked loop (PLL) to the clock circuitry. Intel's PLL approach, different from that of National Semiconductor, manages to reduce the hold time to zero and minimizes the variations in setup and output valid times.

Superpipelining on a 32-bit data-driven processor developed jointly by Mitsubishi Ltd., Itami, Japan, and Osaka University, Osaka, Japan, enables the chip to deliver 50 MFLOPS for vector operations. The processor's architecture consists of a ring-like structure that includes an interface block, a matching-memory section, a data memory, a program memory, and a floating-point arithmetic and logic unit (*Fig. 1*). The ALU performs 32-bit integer arithmetic operations as well as 32-bit floating-point operations, such as multiplication. The data memory block contains five independent address generators, eight memory banks, and switching matrices that connect the address generators to the memory banks. Up to five memory accesses can be done in parallel.

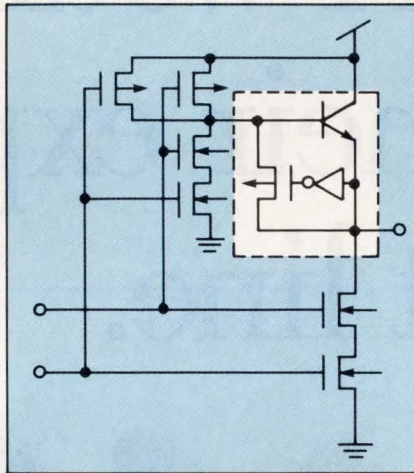
External data words are fed into

the chip through the interface block. The words are interleaved with internally circulating data by an asynchronous arbitration circuit that packetizes the data with an instruction, destination tag, and operands. In the matching-memory section, an incoming packet's tag is compared with tags of all packets that arrived prior to the present packet. If a matching tag is found, a pair of data for a dyadic operation is assembled and sent to the data memory; otherwise the incoming packet is pooled in the matching-memory unit. Vector data packets are generated every 20 ns to achieve the peak chip performance of 50 MFLOPS.

Because pipeline stalls created by data problems don't occur in data-flow architecture, superpipelining works well. In fact, each on-chip processor block is further subdivided into small pipeline stages ranging from 6 for the matching memory to 12 for the floating-point unit. And rather than use a high-frequency clock, which might cause additional design problems due to clock skew and waveform degradations, designers applied a self-timed clocking scheme. All circuits on the chip are controlled not by an external clock, but by internal self-timed clocks. As a result, even at a very high packet flow rate, the processor operation throughput is stable and standby current is almost zero.

SAVVY SELF-TIMING

Self-timing is also the approach chosen by a research team at Stanford University, Calif., in developing a 54-bit CMOS divider that runs at 160 ns. The research was partially funded by DARPA and an SBIR (small business innovation research) contract through Silicon Engines Inc., Palo Alto, Calif. The self-timed iterating ring implemented in a 1.2- μm process computes the mantissa quotients for a floating-point division operation. It does this using only a fraction of the area employed by a combinatorial-logic-based divider circuit. Local control handshaking between the fully asynchronous logic blocks is used to implement the self-timing for all operations. To



3. THE ADDITION of a small PMOS transistor and an inverter between the emitter and base of the npn output transistor in a biCMOS gate enable Toshiba designers to get full rail-to-rail switching with no speed degradation. Furthermore, the transistor comes in handy as the load element when flip-flops or memory cells must be configured.

avoid a requirement for matching path delays, completion information is embedded in the data throughout the design by employing dual-monotonic wire pairs.

The ring is organized as a series of adjoining stages that are each composed of precharged blocks (Fig. 2). To remove control dependencies that can degrade performance, the design used enough stages in the loop to fully utilize and encompass the time taken by the control circuits so that its delay is completely hidden. Five such stages are used by the divider. Data flows continually at the same rate it would flow through an "unwrapped" combinatorial array. Meanwhile, zero control overhead is added to the latency of the basic computations. Once the input registers are loaded with the dividend and divisor, a Go signal triggers the self-timed ring to begin its iterations. The ring then proceeds to loop a maximum of 11 times to fill the five shift registers with a total of 55 bits for a double-precision result.

Pushing for high-speed math operations, a floating-point coprocessor capable of 33.2 MFLOPS when running at 65 MHz was jointly developed

by Hewlett-Packard Co., Ft. Collins, Colo., and Texas Instruments Inc., Dallas. The chip, intended to support HP's RISC CPU, has about 640,000 transistors crammed onto a 502-by-520-mil chip using 0.8- μm design rules. The coprocessor implements a copy of the HP Precision Architecture instruction pipeline and receives 32-bit instructions from the same instruction cache that feeds the CPU. Data words are transferred over a 64-bit bus to a common data cache. Several extensions to HP's coprocessor have also been implemented to handle a three-register multiply and an independent two-register add or subtract. Furthermore, support for graphics operations now include accelerated clip tests, reciprocal square root, and integer multiplication.

The coprocessor performs single- and double-precision ALU and multiplication operations with a three-cycle latency. The function units are able to accept a new operation every second cycle. To minimize the size of the 64-by-64-bit multiplier, octal recoding was used. Partial products are summed in a binary tree. A nine-port register file containing 64 32-bit registers allows all sections of the chip to obtain data as fast as possible. There are five read ports, three write ports, and one feedthrough port that can't write into a register, but can be the source of data for any of the read ports. Each of the write ports can also be a source for feedthroughs to a read port.

VERSATILE SUBPROCESSOR

Rather than focus on numerics processing, designers at Hitachi Ltd., Tokyo, Japan, looked at a hardware emulation approach that combines a programmable subprocessor on the same chip as the CPU. The subprocessor can be configured to implement various elements, including timers, serial communication ports, and other functions. The intelligent subprocessor can perform multiple-task processing by a sort of time-shared task scheduling, and can thus emulate the desired peripheral functions.

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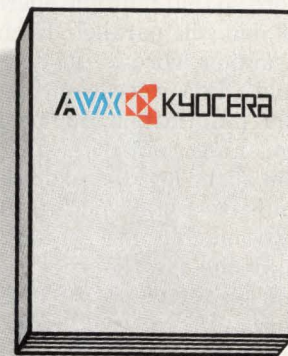
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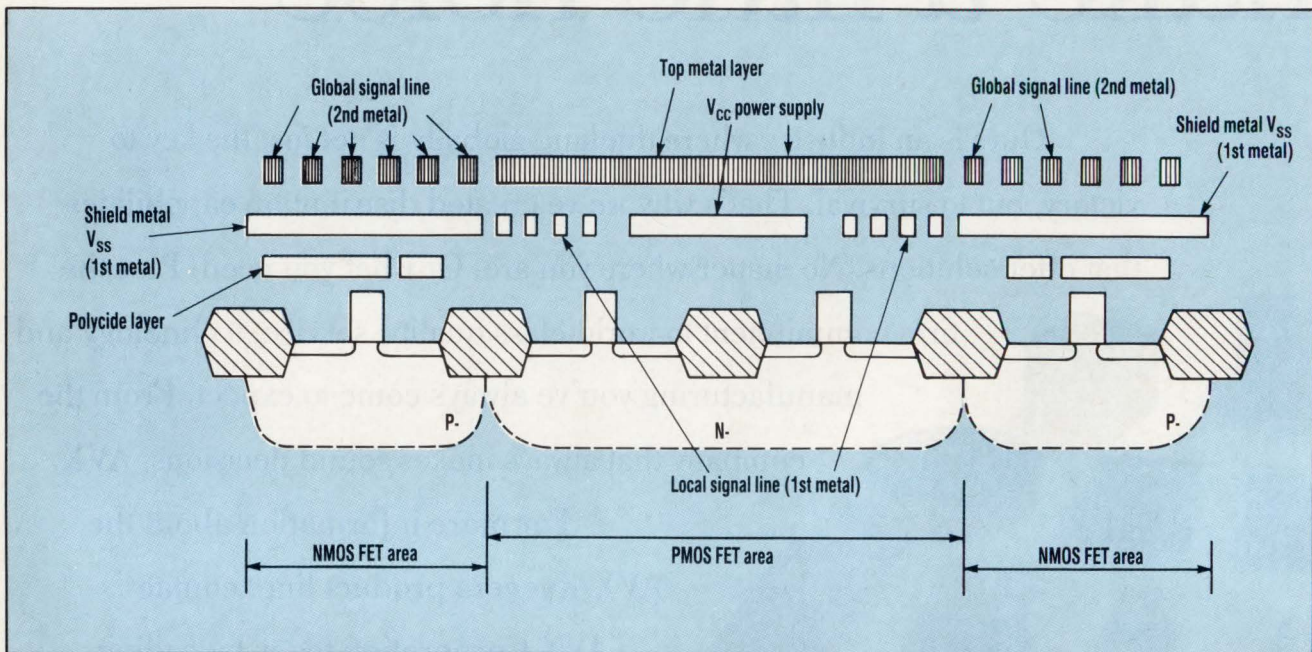


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ng. Tick. Hum.”





4. BY ADDING MESHEDED POWER LINES and a V_{SS} ground shield, designers at Matsushita reduced noise and crosstalk on their 64-Mbit DRAM. Now they can build a version with a 16-bit-wide data bus that doesn't degrade from switching noise generated inside the chip.

clock, the subprocessor executes a microinstruction every 50 ns. To do a great deal in that short period, the chip employs a long microinstruction word so that multiple operations can be done in parallel. Each microinstruction word is divided into four fields: data processing, bit manipulation, nullification, and program control. Each controls a different portion of the logic so that all of the circuit's sections operate in parallel. Two on-chip high-speed EPROMs hold the configuration information—a 512-word-by-64-bit program memory and a 64-word by-6-bit schedule-control memory.

Additional blocks on the subprocessor include a 16-bit execution unit, a peripheral interface flag section that provides 64 programmable flags containing 24 port interface flags, and various interrupt and internal flag lines. All of the lines can be programmed to modify an ALU operation, control an output, or nullify a microinstruction based on a specific condition. By performing all of these control operations in parallel, the processor can emulate complex hardware functions in fewer cycles than a conventional processor. For example, a pulse output operation

based on an event counter needs just one long microinstruction; most microcontrollers would require five instructions for the same result.

The multitask scheduling capability also demonstrates the device's level of sophistication. It allows up to 12 tasks to appear to run in parallel thanks to a time-sharing approach to use of the flag lines. System designers would typically assign time slots for each task according to the desired throughput or resolution for the desired task. The time assignment and task number would be stored in the schedule control memory. When the task number is read from a location in the memory, the task can be executed directly with no task-switching overhead time. Consequently, the throughput for each task is 20 MOPS times the time-slot assignment ratio. Tasks can be read out sequentially thanks to built-in counters, or external signals can be used to request specific tasks.

Another processor of sorts, one dedicated to the task of computing DNA match sequences in biomedical applications, was jointly developed by the University of North Carolina, Chapel Hill, and MCNC, Research Triangle Park, N. C. The 1.5-million-

transistor chip runs at 50 MHz and implements a basic function common to several widely used sequence analysis algorithms. When running at 50 MHz, the chip can perform 6.8-billion 16-bit computations/comparisons per second. The mathematical function operates on two strings of characters and computes a sequence-alignment score.

To do the computations, the chip contains 2196 processing elements (PEs) that compute incremental sums of different diagonal paths. The paths represent the search pattern and database sequence for DNA strings. Those PEs are fed by an internal RAM that holds 448 28-bit words. Due to the large number of simultaneous operations of all the PEs, the chip power consumption is close to 4 W. Clock circuits account for almost 75% of the power because a two-pin, non-overlapping clock scheme was needed to drive large 520-pF loads on each of the four globally routed clock lines.

Trying to duplicate the way the human brain learns and computes, a trio of emerging technology papers show off some of the most complex neural-network chips to date. The largest, an 11-million-transistor cir-

circuit jointly developed by Inova Microelectronics Inc., Santa Clara, Calif., and Adaptive Solutions Inc., Beaverton, Ore., can perform 1.6-billion connections/s. Employing a multifold imaging approach, the chip divides the problem among 64 single-instruction, multiple-data processors integrated on the chip (ELECTRONIC DESIGN, Nov. 22, 1990, p. 30). The two remaining neural chips are based on analog structures. The first, from Mitsubishi, contains the equivalent of 336 neurons and 28,000 synapses. The second, from AT&T Bell Laboratories, Holmdel, N.J., implements 4096 synapses and can be programmed to have as few as 16 neurons with 256 inputs each, or as many as 256 with 16 inputs, or it may have some combination in between.

Employing a branch-neuron-unit (BNU) architecture, the Mitsubishi approach employs two chips to form the neural network. Those chips can

be tied into multiple chips to expand the number of neurons 200-fold (assuming a 30% firing rate and a 1% fluctuation of each neuron unit). Such a network would supply 3300 neurons and 5.6-million synapses—equivalent to 11.2-million symmetrical connections. The BNU approach distributes the neuron function in multiple chips, making the speed performance independent from the number of interconnected chips. Moreover, although two types of chips are needed in this approach—a synapse-only chip and a combination neuron and synapse chip—master-slice gate-array-like design methodologies can readily produce the required chips.

Each synapse chip has a learning control circuit that follows the Boltzmann Machine learning algorithm (first published by David Ackley and others in *Cognitive Science*, Vol. 9, No. 1, January-March 1985). Learning time is less than 4 μ s per one-

teach pattern. That's the time it takes for the alternate shift-in of the teach-pattern data and the neuron property data, the settling time for each learning phase, and the time to modify every synaptic weight.

The programmable analog neural processor from AT&T manages to achieve a sustained throughput of 5-billion connection updates/s on a chip that measures just 4.5 by 7 mm. Internally, all calculations are done with analog circuit functions; all inputs and outputs to the chip are digital. Computations are performed to 6-bit accuracy for the weights and 3 bits for the states—sufficient for use in many pattern-classification applications.

The chip's basic function is to concurrently evaluate several dot products of state and weight vectors and apply a nonlinear squashing function to the results. Actual computations are done by eight banks of vector multipliers, with each bank con-

LOOKING INTO THE SOVIET'S SEMICONDUCTOR TECHNOLOGY

This year's ISSCC includes a special session detailing semiconductor technology in the Soviet Union (see *Technology Briefing*, pg. 18). Two digital-technology papers from researchers at the Nauchny Center in Moscow describe a novel nonvolatile static RAM (SRAM) that combines a 4-kbit SRAM with a 16-kbit EEPROM and a pair of flash EEPROMs that pack 256 k and 1 Mbit. The NVRAM chip appears to system designers as a 4-kword-by-1-bit SRAM with a 70- to 100-ns access time over a -65 to +85° range. The data in the chip's RAM portion can be backed up by any of four pages of EEPROM storage that's organized as a 4-k-by-4-bit array. The desired page number is selected by a two-bit code sent to the chip's A10 and A11 address lines.

Data takes about 5 μ s to be recalled from the desired EEPROM page, and about 10 ms to be stored in the page. The differential EEPROM storage cells are based on silicon nitride technology and a ni-

tride oxide data dielectric. To achieve the fast access times, the SRAM flip-flop serves double duty: During nonvolatile memory accesses, the flip-flop turns into a sensitive amplifier, which improves the performance of the nonvolatile memory cells. When being accessed, the chip consumes about 120 mA. When it stands by, the current drops to 35 mA.

The flash-type EEPROM cell developed at Nauchny is employed in both a 32-k by 8 and a 128-k by 8-bit chip. The cell structure consists of a thin silicon dioxide layer over the transistor's channel region. That layer is, in turn, covered with a thicker silicon nitride layer. The resulting 1-transistor EEPROM cells—the fabricated 2.5- μ m features in the 32-kbyte chip and the 2.0- μ m features on the 128-kbyte memory—are very area-efficient, requiring just 47 and 27 μ m², respectively. This translates into chip areas of 46 and 60.5 mm², which is very competitive with chips made with

dual-transistor cells and much smaller features.

Unlike most MNOS storage cells, the Russian designers employ positive thresholds for both logic states (1.5 and 3.5 V) of the cells. Positive-polarity pulses control each cell. A 24-V external power supply is, however, needed for the program and erase modes. The array offers three erase modes—bulk erase in one cycle, one 256-byte block (or 512-bytes for the 1-Mbit chip), or one line (32 or 64 bytes, respectively)—with any mode requiring 10 seconds to erase the cells. The 256-kbit chip has a read access time of 350 ns, while the megabit chip requires 700 ns. As with most flash-memory chips available in the U. S., the Russian memories have a guaranteed number of programming cycles somewhere between 1000 and 10,000 cycles. The chips also have several special control modes, which the designers claim can extend the number of programming cycles and accelerate the store and erase operations.

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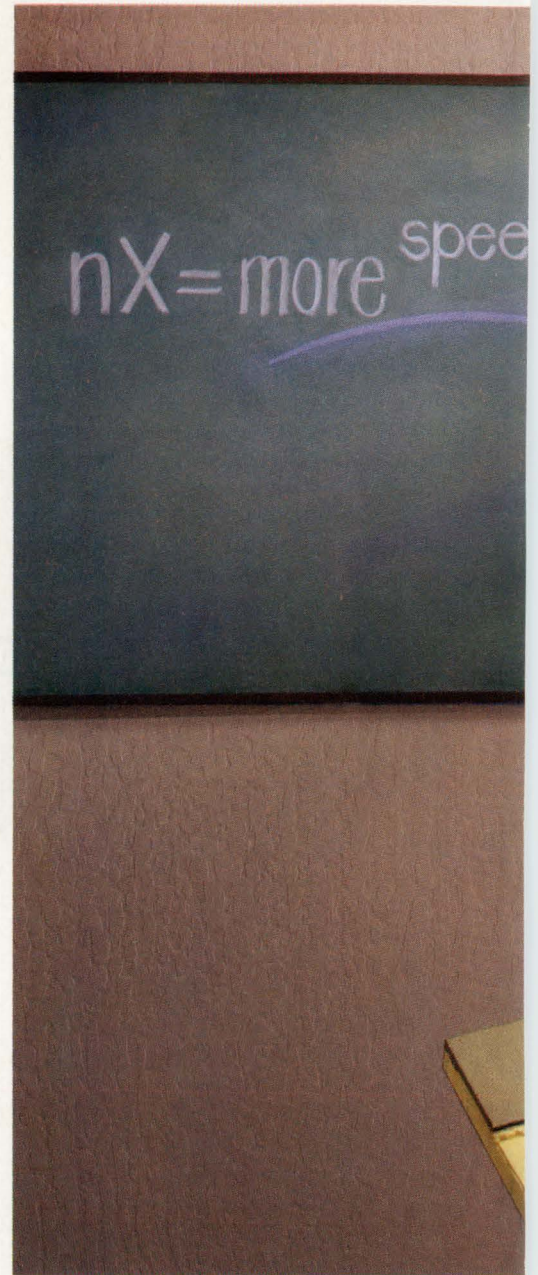
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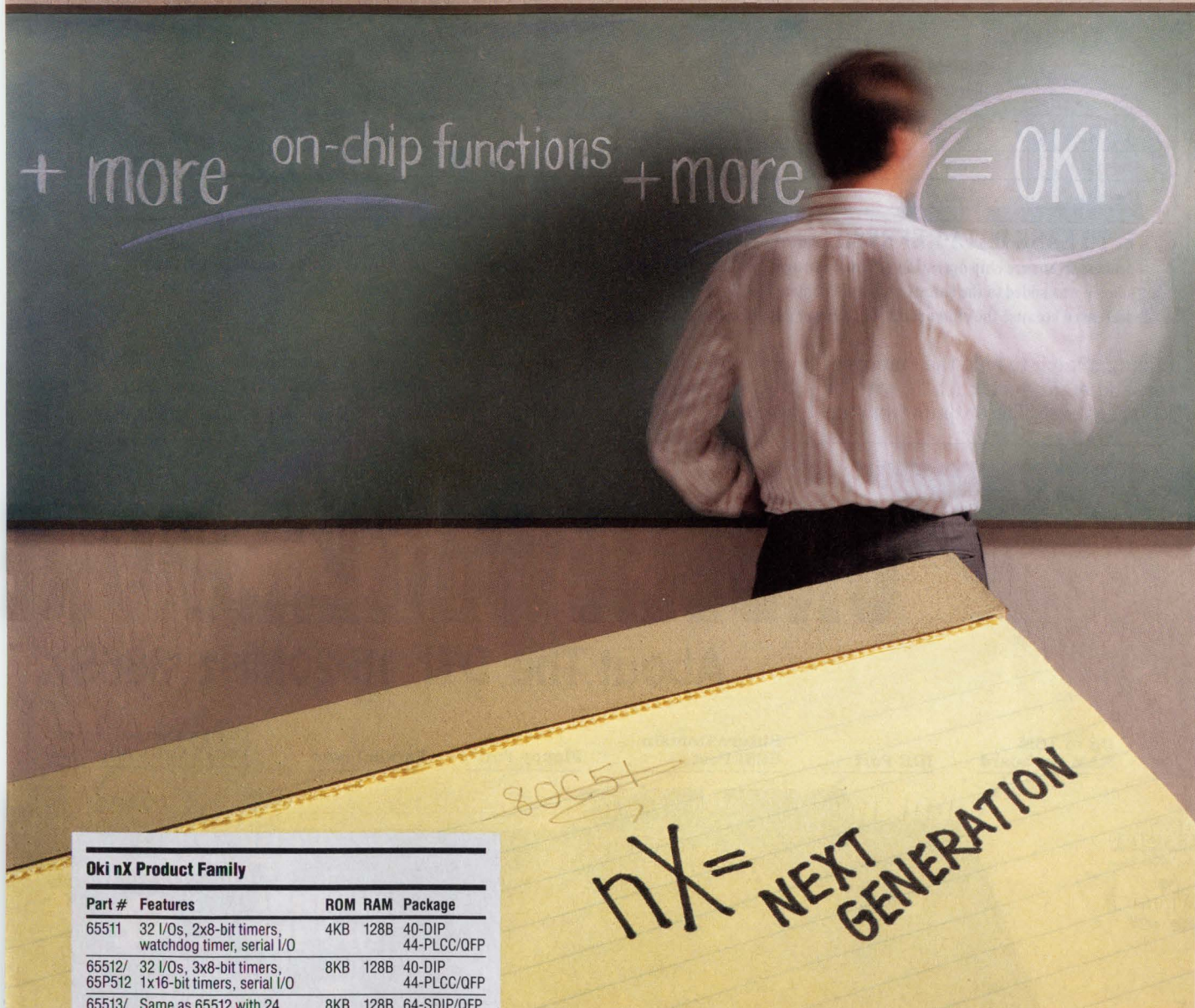
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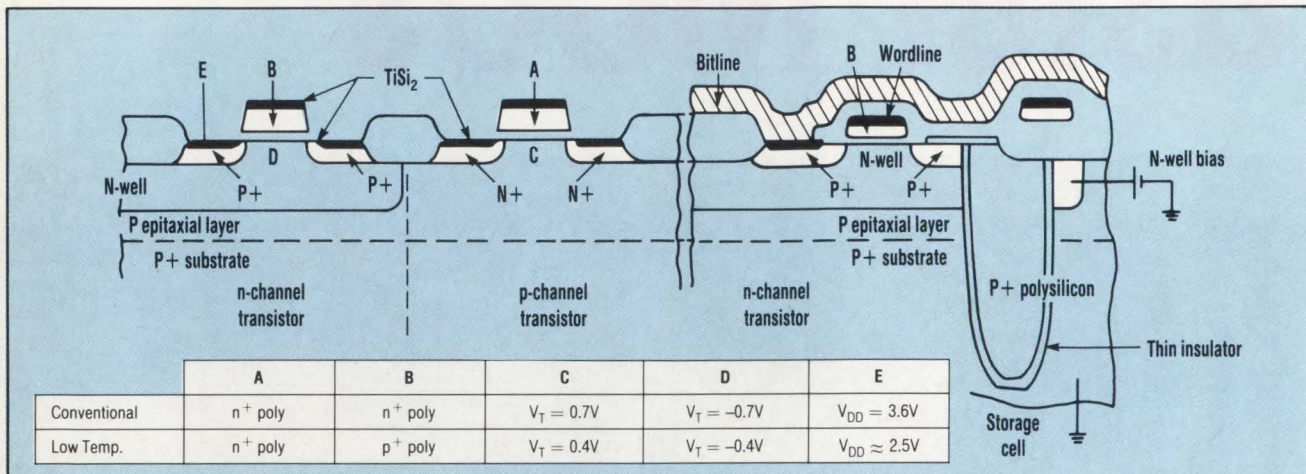
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65513/ 65P513	Same as 65512 with 24 additional I/Os	8KB	128B	64-SDIP/QFP 68-PLCC
65524/ 65P524	Same as 65512 with 2x8-bit PWM, 8-bit A/D, additional ROM/RAM	16KB	384B	64-SDIP/QFP 68-PLCC
66201/ 66P201	• 48 I/Os • 10-bit A/D	16KB	512B	64-SDIP/QFP 68-PLCC
66207/ 66P207	• 4x16-bit timers • 2x16-bit PWM	16KB	512B	64-SDIP/QFP 68-PLCC
66301/ 66P301	• Serial interface • Transition detector	32KB	1KB	64-SDIP/QFP 68-PLCC
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5. TO EASE DATA-REFRESH requirements by designing chips for low-temperature operation, designers at IBM tweaked the process to ensure chip operation at liquid nitrogen temperatures. The gate polysilicon on the n-channel transistor was changed and titanium silicide was added to the source and drain contacts to lower the contact resistances. In addition, the transistor threshold voltages were decreased because the chip operates at a lower supply voltage. The table inset sums up the changes.

taining a latch to hold the state vector, and eight vector ALUs with 64 synapses each. The outputs from the

vector multipliers are routed to the neuron bodies by a multiplexer, which can be configured to combine

the contributions from one to four vector multipliers. The configurable routing plus the ability to program

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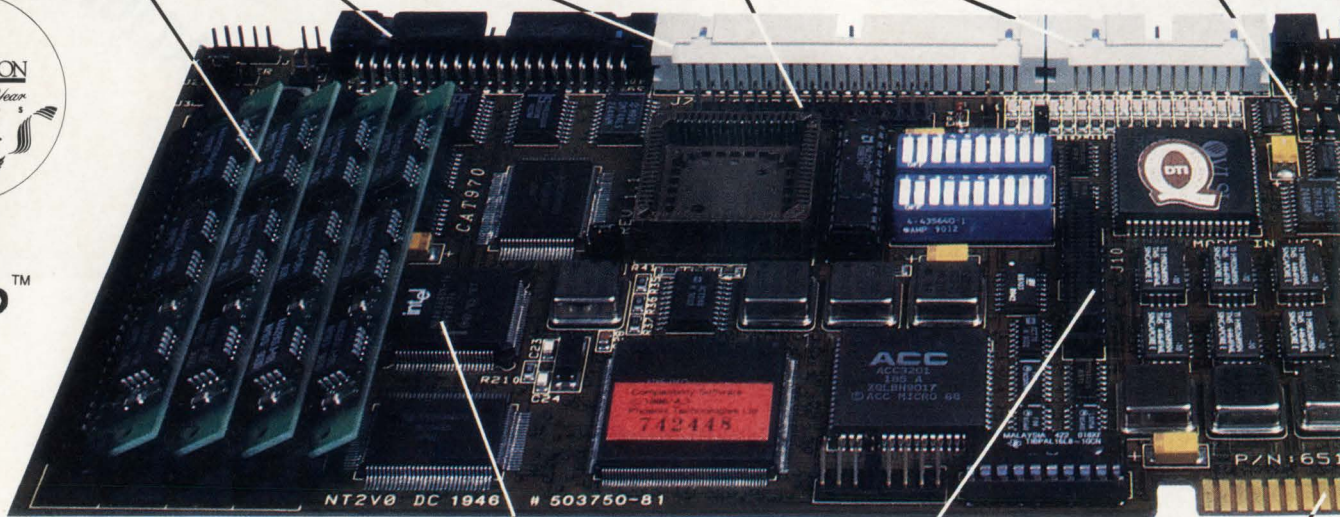
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the internal shifter and register file enables designers to set the chips' overall configuration.

GROWING GATE ARRAYS

Even as custom chips grow in size and complexity, so do some of the more standard logic chips such as gate arrays. One of the largest biCMOS gate arrays is a 2-million-transistor chip developed by Toshiba Corp., Kawasaki, Japan. The channelless array employs a novel biCMOS cell that contains an extra PMOS transistor to supplement the conventional CMOS cell with the npn output transistor (*Fig. 3*). The chip is designed to operate from a 3.3-V power supply and offers typical gate propagation delays of 230 ps (with a fanout of 7).

Dubbed biPNMOS by the company, the structure uses the small-size added PMOS device to boost the output swing to the full rail-to-rail val-

ues. To do that, the transistor's gate is controlled by a small inverter that delivers an inverted version of the output signal. That signal causes the transistor to turn on or off without causing any leakage current from the next logic stage. A simple resistor can't be used because it can't have a small value—a low value would cause the base current to be bypassed, and that could lead to current leakage from the next stage. The result is degraded performance from the npn transistor.

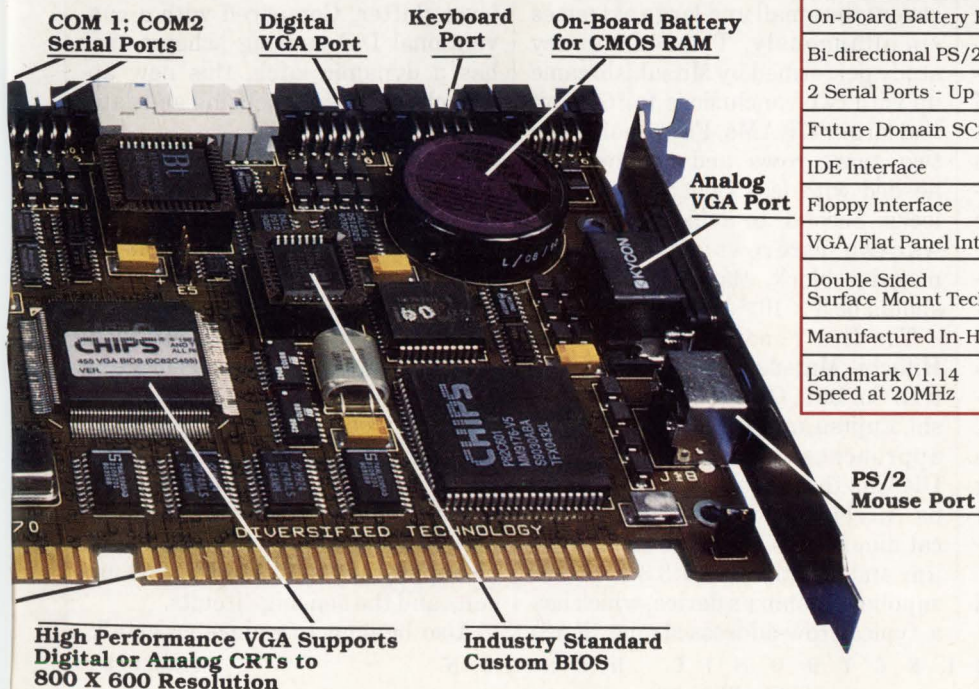
The small-size PMOS transistors add yet another benefit: They're helpful when individual flip-flops, registers, or RAM cells must be implemented because such cells don't require the PMOS load transistors to drive long lines. Blocks of RAM implemented with the cells can be configured for high speed or high density. The high-speed option keeps the access time to 2.7 ns (with a fanout of

7), while the version configured for better density accesses in about 4 ns. Measuring almost half an inch on a side, the chip packs 237,120 raw gates plus 1044 I/O cells.

Pushing for high speed in gate arrays, both Fujitsu Ltd., Atsugi, Japan, and Rockwell International, Thousand Oaks, Calif., have developed arrays based on GaAs. The Fujitsu array tackles the high-density arena by employing high-electron-mobility transistors (HEMTs), while Rockwell's chip tackles the low-density but super-high-speed requirements with heterojunction bipolar transistors (HBTs). Packing 45,000 gates—the largest HEMT gate count on a chip to date—the Fujitsu chip packs two types of gates. It contains DCFL (direct-coupled FET logic) gates that have propagation delays of 35 ps, and BDCFL (buffered DCFL) structures that have delays of 50 ps. BDCFL contains the DCFL

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logic stage followed by a source-follower buffer stage and can drive heavier loads than DCFL.

Four levels of metal interconnections are used on the arrays to ensure high usability and a silylated poly-methyl silsequioxane compound is used as the interlayer dielectric due to its low dielectric constant of 3. With about 80% gate utilization, the GaAs array consumes about 11 W when running from -1.4 and -2-V supplies. The reasonable power permits the chip to be used in forced-air cooling systems.

The HBT-based GaAs array from Rockwell concentrates on speed. It can operate with flip-flop toggle rates of 15.6 GHz—close to double that ever demonstrated for a gate array. Total power consumption for the array is between 2 and 3 W, depending on the utilization and the power allocated per gate during design. The circuit approach is similar to implementations of two-level differential current-mode logic, with the current per tree selectable as 0.5, 1, 2, or 3 mA. Those choices make it possible for designers to trade off speed for lower power in the non-speed-critical portions of the circuit.

Even faster circuits can be implemented with Josephson junction (JJ) technology, as a pair of papers from Fujitsu demonstrate. In the first of the two papers, Fujitsu researchers describe a sub-ns clock cryogenic system for JJ computers jointly developed with Shinko Electric Industries Co. Ltd., Nagano, Japan, and Toyo Sanso Co. Ltd., Kawasaki. With JJ-based systems, one problem designers face is to link the JJ portion of the system to the rest of the world. By passing I/O cables through a vacuum vessel, researchers were able to employ JJ and semiconductor logic circuits while imposing just 130 ps of delay. The JJ chips are maintained at 4.4K by a closed-cycle 3-W desk-size refrigerator. A new cryostat design keeps the cable lengths to just 24 mm, minimizing the signal delay. The cables connect to the non-refrigerated circuits. Operation of a previously described 4-bit JJ microprocessor was confirmed at clock speeds of up to 1.1 GHz.

In the other paper, Fujitsu researchers describe the fastest 24-bit carry-select adder yet fabricated. The 360-ps JJ-based adder also has a carry propagation time of 300 ps. Just over 1000 gates are used to implement the adder, but those gates consume negligible power—just 1.8 mW at full speed.

Coming close to the speed limit, a paper in session 11 from National Semiconductor Corp., Santa Clara, examines using quantum devices for arithmetic and logic operations. Resonant tunneling transistors, made with GaAs/AlGaAs/InGaAs structures, are proposed as new logic devices. These devices take advantage of their negative differential resistance. The transistors are attractive for logic elements because carry outputs plus AND and OR logic functions can be obtained with just one device delay, rather than dealing with the typical multiple device delays in today's logic circuits.

SIZING UP DRAMS

Seemingly reaching down to the quantum level, the latest crop of dynamic RAMs (DRAMs) unveiled at the conference push the limits of optics with minimum feature sizes of less than 0.4 μm . With six papers describing five 64-Mbit memory chips and an optimized redundancy scheme to optimize yield, session 6 covers the small and large extremes simultaneously. The redundancy study performed by Mitsubishi came up with two conclusions for 64-Mbit and larger DRAMs. First, more than two spare rows and columns are needed with less than 1-Mbit subblocks. Second, to achieve 80% yield with two spare rows and columns per megabit block, the defect density should be 5×10^{-4} or smaller.

The five remaining papers from Hitachi, Matsushita Electric Industrial Co. Ltd., Osaka, Japan, Mitsubishi, Fujitsu, and Toshiba, all describe approaches to building 64-Mbit DRAMs that access in from 33 to 50 ns. All chips are fabricated with critical dimensions between 0.3 and 0.4 μm and operate from 3.3-V power supplies. Toshiba's device, which has a typical row-address-strobe (RAS)

access time of 33 ns, is the fastest 64-Mbit chip yet unveiled.

To get the high density, designers developed an asymmetrical stacked-trench capacitor cell that's laid out between twisted bitlines. And to keep the access time short, several circuit techniques were combined on the chip—a preboosted wordline-driveline, a bypassed sense-amplifier driveline, and a three-stage differential amplifier with a directly driven data-output buffer.

The preboosted wordline-driveline conceals the R-C delays in long and heavily loaded wordlines and drivelines laid out through the row decoders, cutting 3 ns off the access time. Increased bitline capacitance due to the large memory array causes delays in the bitline latch operation. To improve that speed, sense-amplifier drive transistors are placed in the wordline shunt regions, and the source lines (V_{SS}) are laid down along with bitlines in second-level metal.

Bitline charge isn't driven by the main driveline when the wordline is driven. The bypassed line drives the charge when the bitline is driven. That reduces the bitline latch response time by 5 ns. And to improve the data sensing time, data should be sensed and transferred continuously with small voltage swings. To do that, a quasi-static I/O sensing approach employs a complementary level shifter. Compared with a conventional I/O sensing scheme that has a dynamic latch, this new approach reduces the sensing and data-transfer time by 4 ns.

The first 16-bit wide implementation of a 64-Mbit DRAM was described by Matsushita. The chip employs a meshed power line on the chip's surface to minimize problems from power-line drops due to multiple I/O lines switching simultaneously. The chip also incorporates a ground shield around the peripheral circuits to reduce noise in the storage array (Fig. 4). Because the meshed power line can perfectly separate the sense-amplifier power line from the peripheral power line, crosstalk can be suppressed between the I/O circuits and the sensing circuits.

Also helping to reduce crosstalk,

the V_{SS} shield trims conversation between the global signal lines. The shield is formed between the polyicide layer and the top metal layer, with the lower metal layer attached to the shield plate. Thanks to the shields as well as other circuit tricks, the chip can access a location in 50 ns while consuming 130 mA.

Fujitsu's 64-Mbit chip, in addition to an impressive 40-ns typical access time, offers a compressed test mode that will accelerate chip testing by allowing 64 bits to be tested during every access. Mitsubishi's slightly slower, 45-ns memory does Fujitsu one better. Its merged match-line test architecture enables 64 kbits to be tested in parallel, allowing the DRAM to be tested in 1024 cycles.

Rather than focus on testing or high speed, designers at Hitachi examined ways to shrink the memory array and the memory cell's size. Those research efforts have yielded what the company calls a block-oriented RAM. This memory employs an array of series-connected cells in which 64 times the number of cells can be connected to one amplifier, reducing the number of amplifiers needed. Also, the dataline capacitance to that amplifier can be reduced by a factor of eight, speeding up memory access.

As impressive as the 64-Mbit DRAMs are for their density and small features, there's still plenty of activity at lower memory densities. A special CMOS 4-Mbit chip developed by IBM Corp. at its T.J. Watson Research Center, Yorktown Heights, N.Y., proves that by working at liquid nitrogen temperatures (85K), DRAMs can achieve storage times for trench cells of greater than 50 minutes. Designed for low-temperature operation, the DRAM uses p+ polysilicon gates for the PMOS FETs and n+ polysilicon for the NMOS FET gates to ensure that both types behave as surface-channel devices (Fig. 5). That's because surface-channel devices don't suffer freeze-out at low temperatures.

The power supply was also reduced to 2.5 V to minimize hot-carrier problems and reduce power dissipation. Moreover, because the low

temperature causes lower sub-threshold currents, the low-temperature V_T can be designed lower—0.4 V vs. 0.7 V—to increase speed. Test chips were made with 0.7- μ m features at 85K. With a 2.5-V power supply, the memory cells could retain data for over 50 minutes.

SPEED DEMONS

Enhancing DRAM speed is a constant goal. One alternative that may catch some interest was described by Toshiba. Designers achieved a 17-ns access time on a 4-Mbit DRAM by using a non-multiplexed address bus and a direct bitline sensing scheme with a two-stage current-mirror amplifier. The high sensitivity of the current-mirror amplifier allows it to amplify a small bitline signal without waiting for the start of the bitline latch action, lowering access time. Furthermore, the conventional I/O line was split so that there are separate data-input and data-output lines.

A test chip fabricated with the company's 16-Mbit-chip process yielded an 11.06-by-4.76-mm IC that can be housed in a 32-lead SOJ package. The process employs triple polysilicon layers, two metal interconnection layers, 0.6- μ m minimum feature sizes, and a triple-well structure on an n-type substrate. A 5-V supply powers the chip, but a down-converter reduces the internal power-supply level to 4 V.

Rather than use more pins or requiring low temperatures, Hitachi designers applied a biCMOS process with 0.8- μ m minimum features to achieve the same 17-ns access time and a 40-ns cycle time. When operating with a 60-ns cycle time, the chip draws 120 mA. To get the short access time, designers applied a noise-immune cascode amplifier to sense the signals faster and an offset cross-coupled output buffer to minimize the output delay.

Speedy 4-Mbit static RAMs are also breaking new records. Fujitsu, in a pair of papers, managed to trim the access time for a TTL biCMOS SRAM to just 10 ns and that of an ECL I/O version to just 7 ns. To cut the TTL access time to 10 ns, design-

ers allied a 0.5- μ m CMOS process for the cell array and a 0.8- μ m process for the peripheral circuits. Two-stage sense amplifiers are used to minimize the sense time. Also, a combination P and NMOS cross-coupled level converter was developed to reduce the delay when converting from the output of the bipolar differential amplifier to CMOS.

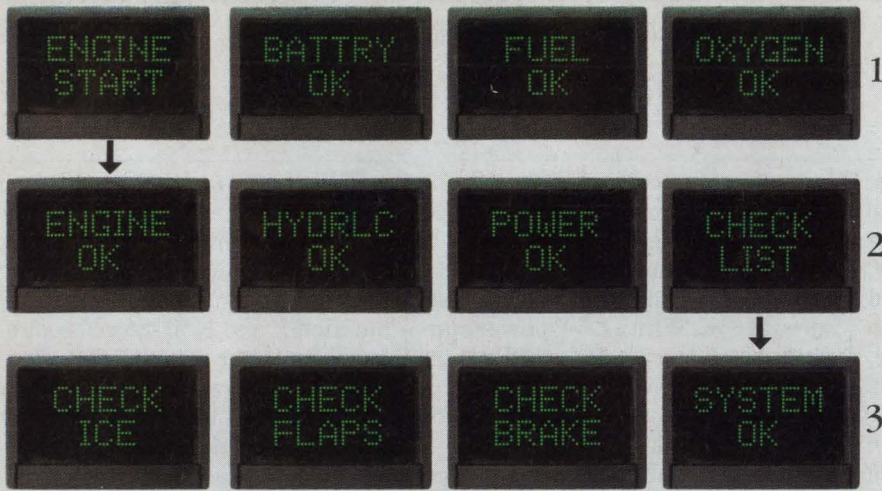
One unique aspect of the ECL I/O SRAM is its 16-bit parallel test mode to reduce chip test time. The chip will also be configurable as either a 4M-by-1, 2M-by-2, 1M-by-4, or 512k-by-8-bit array.

Ultrafast memories are always in demand for such applications as caches and even main memory for high-speed controllers or computers. A trio of papers show some new upper limits of what designers can do. Designers at IBM developed what appears to be the fastest CMOS SRAM with ECL I/O—a 512-kbit chip with a 2-ns cycle time and a 4-ns access time. The high speed was achieved through the extensive use of pipelining and six-transistor memory CMOS memory cells.

Pulling access times below 2 ns, a 1.2-ns 64-kbit GaAs memory fabricated with HEMTs was unveiled by Fujitsu. The RAM, which offers ECL-compatible I/O lines, is the largest HEMT chip to date with 0.6 μ m-features. Organized as 8k-by-8, the RAM requires three supplies: -1, -2, and -3.6 V.

Designers at Toshiba described a secondary cache subsystem that's integrated on one chip—a 64-kbyte snoopy cache memory that ties into 80486 and 80386-type microprocessors. They crammed 64 kbytes of data RAM with byte parity, a 68-kbit tag memory, a 16-kbit valid-flag memory, and 2-kbit least-recently used flag memory onto the IC. The chip performs two-way set associative mapping with 2048 sets, and employs a write-through protocol for cache coherency. □

HOW VALUABLE?	CIRCLE
HIGHLY	545
MODERATELY	546
SLIGHTLY	547



AN APPLICATIONS EXAMPLE.
While the following example is for aircraft, it could apply to any air, land, sea or space system.

SEQUENCE ONE: The four-pushbutton display reads "ENGINE START," "BATTERY OK," "FUEL OK," "OXYGEN OK." The operator selects "ENGINE START."

SEQUENCE TWO: The four-pushbutton display now changes to read "ENGINE OK," "HYDRLOC OK," "POWER OK," "CHECK LIST." The operator selects "CHECK LIST."

SEQUENCE THREE: The four-pushbutton display now reads "CHECK ICE," "CHECK FLAPS," "CHECK BRAKE," "SYSTEM OK." In this manner, the designer can program in as many sequences as required.

Design flexibility: The programmable display system.

Vivisun Series 2000, now the leading programmable display pushbutton system, interfaces the operator with the host computer. The user-friendly LED dot-matrix displays can display any graphics or alpha-numerics and are available in green, red or amber. They can efficiently guide the operator through any complex sequence with no errors and no wasted time.

They also simplify operator training as well as control panel design. One Vivisun Series 2000

programmable display system can do the work of 50 or more dedicated switches. In short, Vivisun Series 2000 gives the design engineer more control over the design.

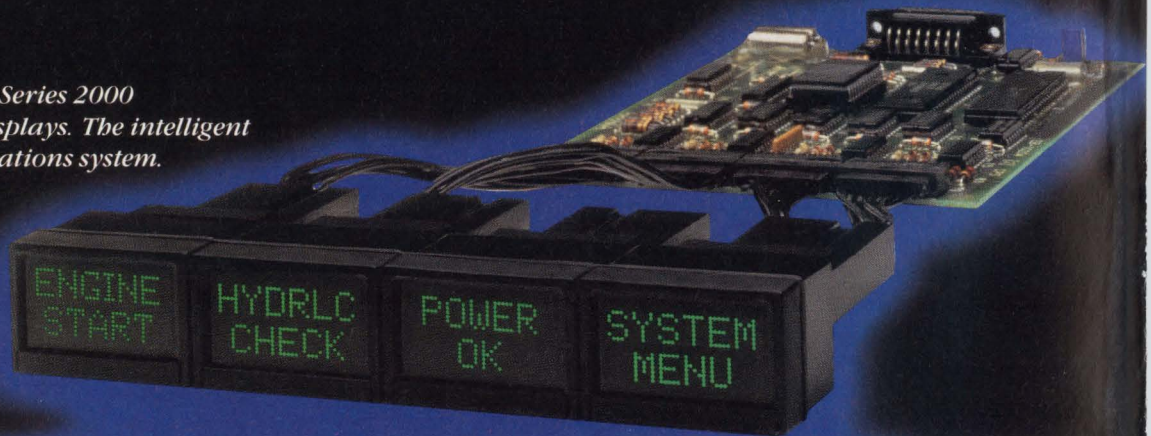
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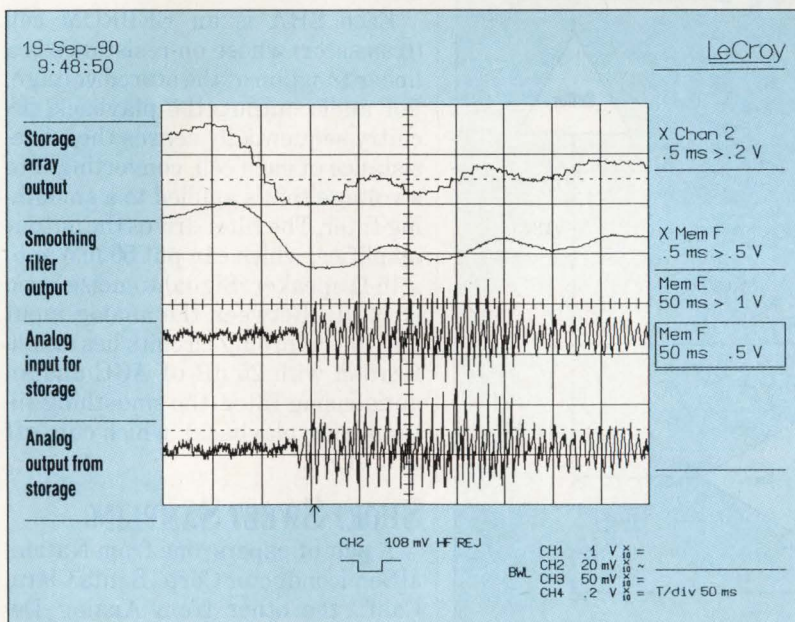
VIVISUN 2000™

ISSCC

ANALOG TECHNOLOGY

At this year's ISSCC, the 30 or so analog and mixed-signal papers feast on sampling. They sink their teeth into oversampling and undersampling, sampling ac and sampling dc, pre-quantization sampling, and even sampling for nonvolatile analog on-chip storage.

One pure-analog sampling paper on the table describes a charge-coupled device (CCD) delay-line filter for video signals, while other sampling papers range from 14-bit linear sample-and-hold amplifiers (SHAs), with acquisition times below 250 ns, to oversampling delta-sigma modulators. Circuit speed continues to soar: An 8-bit (multichip) ADC reaches a 2-GHz sampling rate, a one-chip 6-bit ADC operates at 1 GHz, and an 8-bit flash converter samples at 500 MHz.



1. A NONVOLATILE, ANALOG-MEMORY IC recorded these four waveforms. The IC stores analog voltages in an array of 128,000 analog EEPROM sample-and-hold amplifiers.

In addition to the sampling papers, a smorgasbord of pure analog papers cover chips ranging from 10-GHz GaAs and 6-GHz silicon Gilbert-cell analog multipliers to a 50-MHz 80-dB attenuator. The attenuator, unlike the other variable-gain ICs, does not use a Gilbert cell. Then there's an op amp that runs off 1 V yet handles input signals beyond both rails and output swings to both rails. Add to that rich mix a 2-GHz transimpedance amplifier in GaAs.

For icing on the cake, distributed throughout the awesome array of ICs performing black-box circuit functions are several complete "systems-on-a-chip": a nonvolatile analog memory handling dc to audio; a 10-A, 60-V buck regulator; and a

0.04% accurate, ac power-metering system. These three ICs provide a broad insight into the versatility, functional capability, and/or performance available from today's power, analog, and mixed-signal ICs.

Once again, the ISSCC proves it-

self to be the venue for the first exposure to new technology. In fact, session 11 is dubbed Emerging Circuit Technologies. For analog specialists, a paper from a new company, Information Storage Devices Inc., San Jose, Calif., stands out like a super nova. Employing an extended EEPROM technology, the chip records 16 seconds of better-than-telephone-quality audio (actually dc to 3.4 kHz) on a chip about 200 mils on a side. Furthermore, this is analog sampling and analog storage—no quantization is involved.

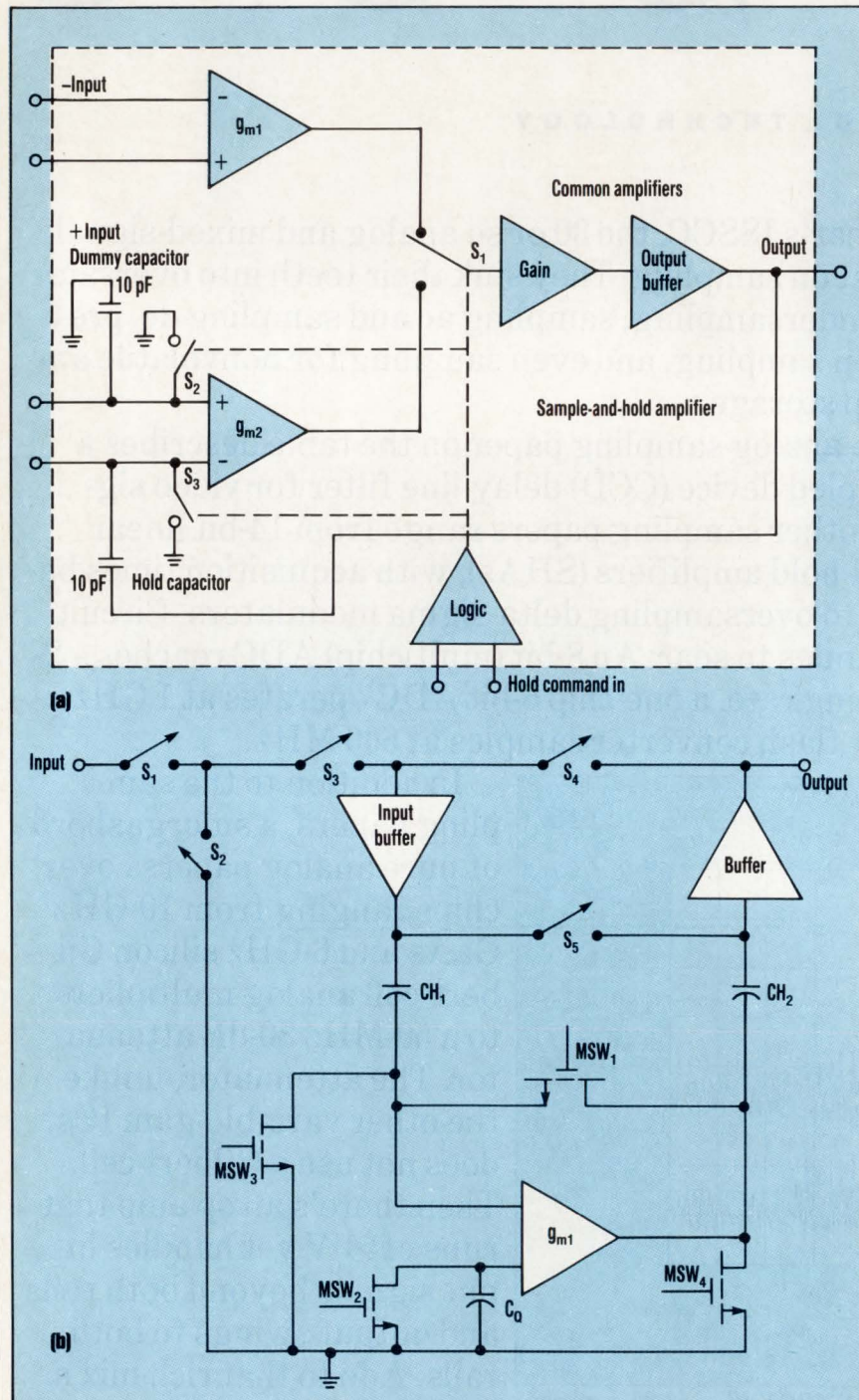
Not only is the recording nonvolatile, but it can be played back an "infinite" number of times, until a block of new data is recorded (*Fig. 1*). Moreover, the chip is truly a complete system. All that's required is to connect a microphone, a speaker, and a 5-V supply.

At the heart of the recorder chip lies an array of 128,000 SHAs, which essentially sample the 0-to-2.75-V input signal at 8 kHz. Resolution is 12 mV, the equivalent of 230 distinct levels. Compared with a digitizing approach, the IC's storage density is about 8 times that of a binary-weighted digital representation, which would need about a million bits.

Each SHA is an EEPROM cell (transistor) whose on-resistance is a linear function of the stored voltage. For audio output, the playback circuitry sequentially senses the on-resistance of each cell, converting it to a voltage that's applied to a smoothing filter. The filter drives the output amplifier, which can put 50 mW into a 16- Ω speaker. Signal-to-noise ratio is 40 dB. Between the analog input and the recording circuits lies amplification with 25 dB of AGC and an antialiasing filter (the smoothing filter during playback), which cuts off at 3.4 kHz.

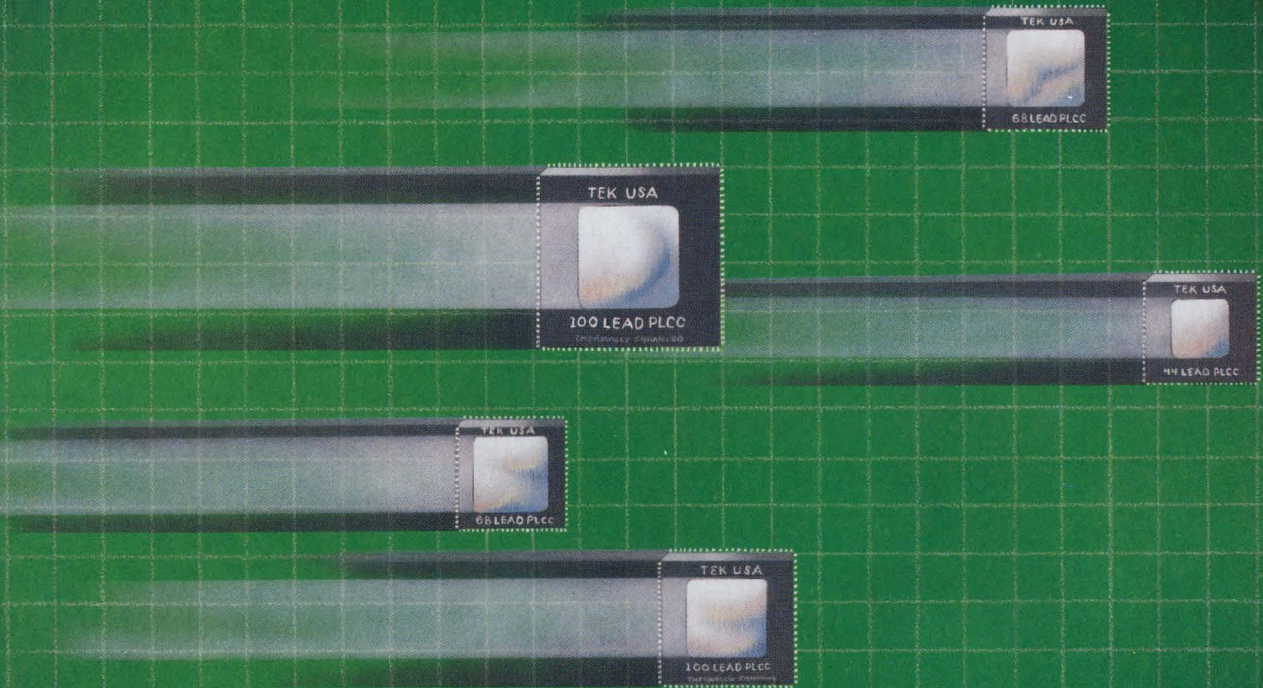
SHORT SWEET SAMPLING

A pair of papers, one from National Semiconductor Corp., Santa Clara, Calif., the other from Analog Devices Semiconductor Inc., Wilmington, Mass., describe record-breaking IC SHAs (*Fig. 2*). They are record-breakers in the combination of speed



2. FAST, ACCURATE SAMPLING AMPLIFIERS from National Semiconductor (a) and Analog Devices (b) reach 12-bit accuracy in under 150 to 250 ns. Both actively cancel the hold-step, or pedestal, errors caused by charge injection at sampling.

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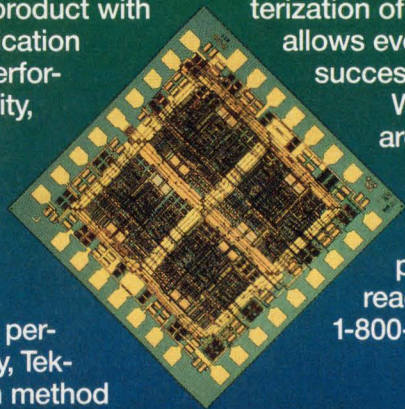
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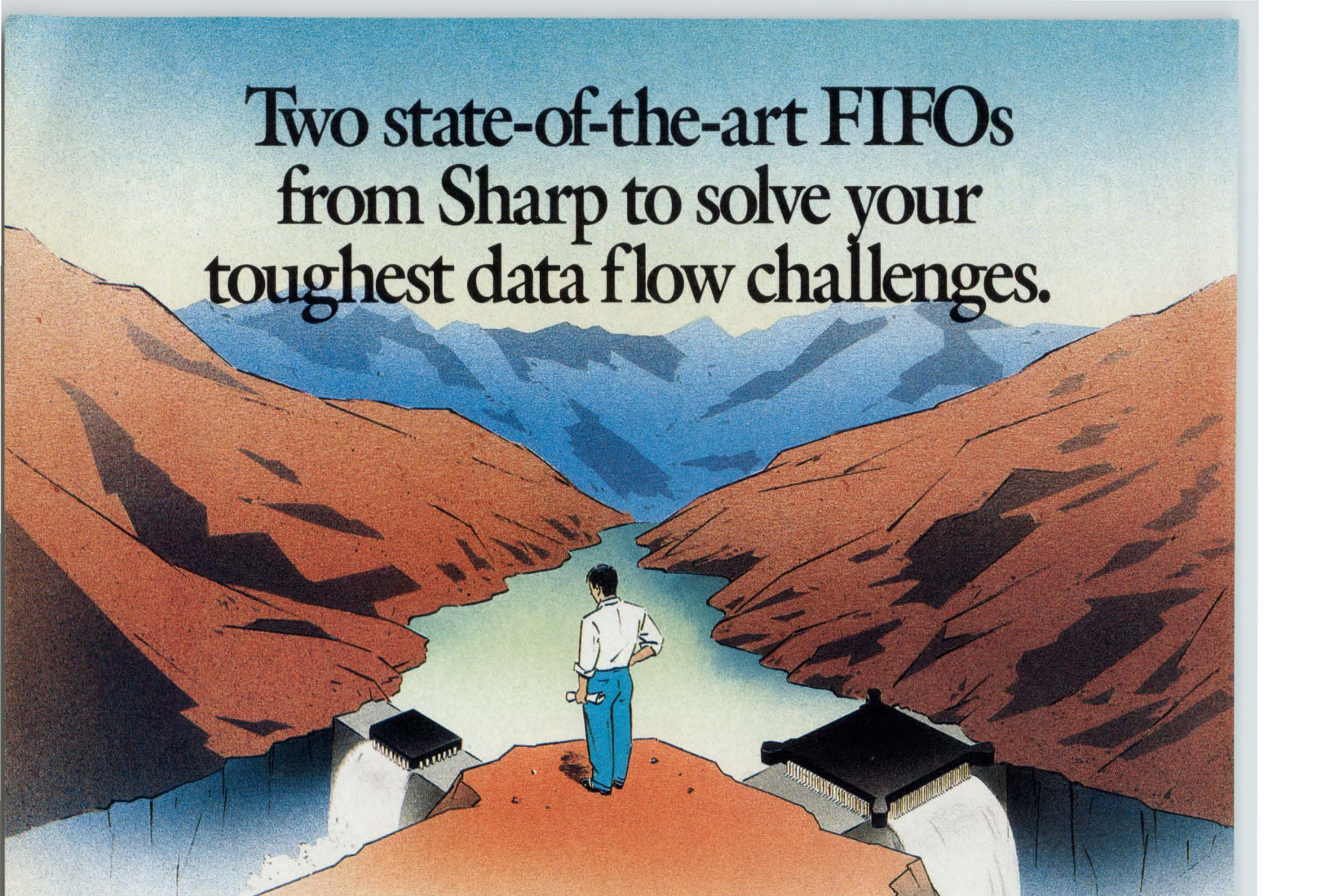
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CIRCLE 129

Two state-of-the-art FIFOs from Sharp to solve your toughest data flow challenges.



They're both *synchronous*, which greatly simplifies your board circuit and design requirements.

Their proprietary *look-ahead access architecture* delivers speedier access and cycle times while reducing power consumption.

Introducing: The LH5492 4K x 9 Clocked FIFO.

Sharp's new LH5492 is a dual-port clocked FIFO, with a 4K x 9 configuration. The clocked interface is a significant enhancement in FIFO design over previous asynchronous parts. The clocked enables on the LH5492 eliminate the requirement to shape waveforms, resulting in simpler design tasks, and lower parts count.

Its high-speed clocked interface can be used directly with the typical 40%/60% duty cycle system clock. And a separate \overline{OE} control signal provides independent control over output buffers.

The second enable pin on each part can be directly tied to the flags to simplify external logic requirements.

The LH5492 4K x 9 clocked FIFO comes in a 32-pin PLCC. It is available with access times of 20 ns, 25 ns and 35 ns, and cycle times of 25 ns, 35 ns and 50 ns, respectively.

Introducing: The LH5420 256 x 36 x 2 Bidirectional FIFO.

Sharp's new LH5420 is actually two 256 x 36-bit FIFOs in one. Operating in parallel but opposite directions to provide bidirectional data buffering that would normally require multiple independent devices.

Its 36-bit word width is an industry first. And ideal for interfacing with new generation higher-speed 32/36-bit and 64/72-bit microprocessors and buses. Moreover, a choice of 9, 18, or 36-bit word widths on Port B means efficient word width matching.

Programmable Almost Empty and Almost Full status flags on each port—in addition to Full, Half Full and Empty flags—allow you to either leave the flags set at their initialized setting of 8, or program them over the entire FIFO depth.

The LH5420 comes in a 132-pin plastic QFP package. It is available with access times of 15 ns, 20 ns and 25 ns, and cycle times of 25 ns, 30 ns and 35 ns, respectively.

SHARP.
By Design.

Sharp Electronics Corporation

and resolution, all having distinct designs and built with very different processes. National's SHA takes 100 ns to acquire a 10-V step to within 0.01% of final value. The chip from Analog Devices acquires a 5-V step in 250 ns to similar accuracy. Both samplers show nonlinearities of 0.003% (14 bits). Until now, such performance existed only in the hybrid-sampling-amplifier realm.

The National IC comes from a ± 15 -V (operational) complementary-bipolar-JFET process that builds 400-MHz f_t npn transistors and 200-MHz f_t pnps. The Analog De-

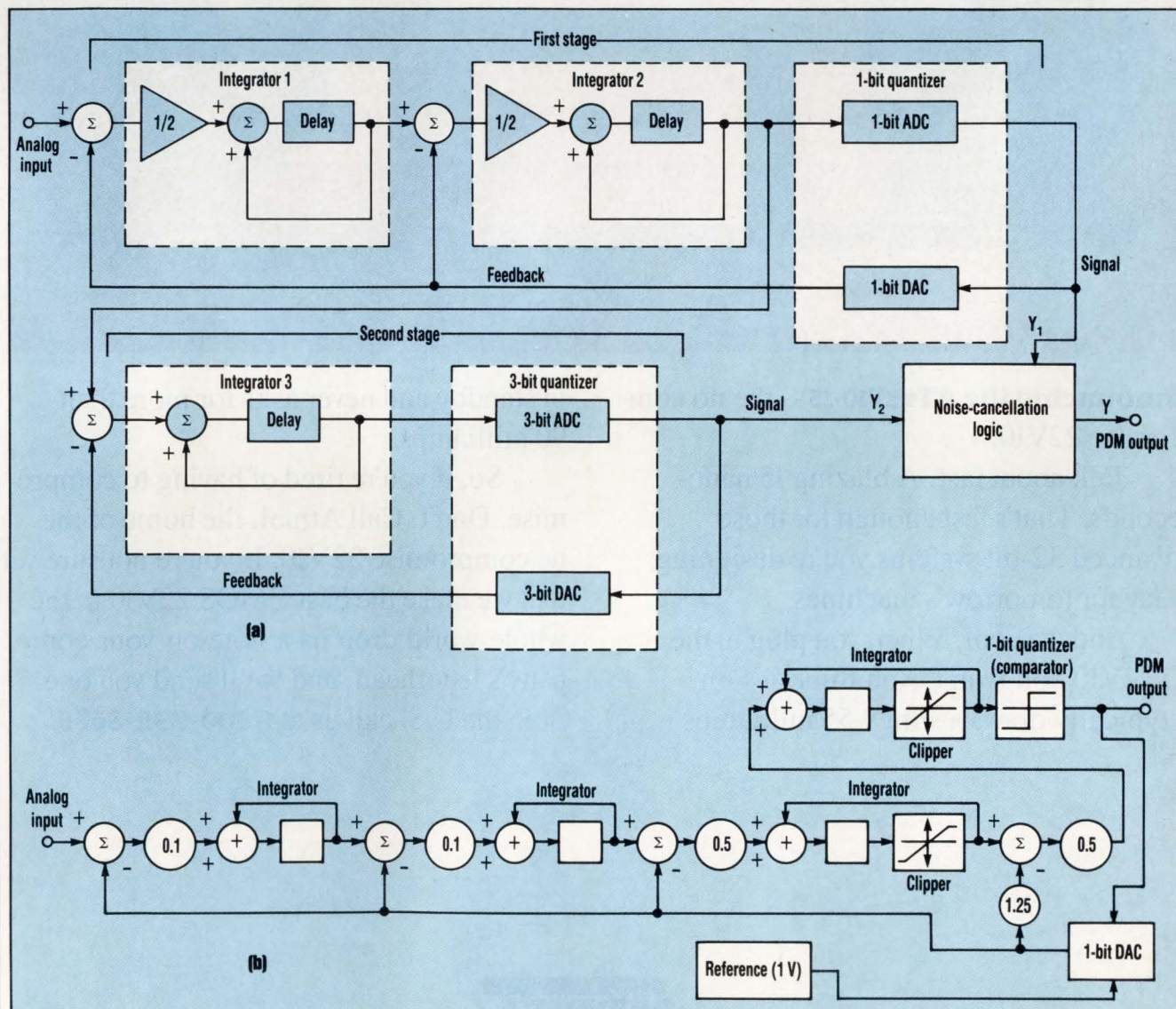
vices chip is built on a 2- μ m biCMOS process featuring 2-GHz f_t npn transistors, n-well CMOS, and laser-trimable resistors.

According to both companies, minimizing the hold-step (pedestal) error becomes the toughest job in getting such a mix of speed and accuracy. This is the offset error, introduced at the output, which is caused by charge injection when switching from acquisition to hold.

National's design takes advantage of the speed of open-loop SHAs while sampling, but cancels charge injection by duplicating it and feed-

ing it through a second amplifier when switching to hold (Fig. 2a). The circuit consists of two separate transconductance amplifiers, g_{m1} and g_{m2} , which are alternately connected and disconnected from the common, gain, and output-buffer stages. A current-steering multiplexing scheme (S_1) within the common amplifier's feedback loop drives the Hold capacitor.

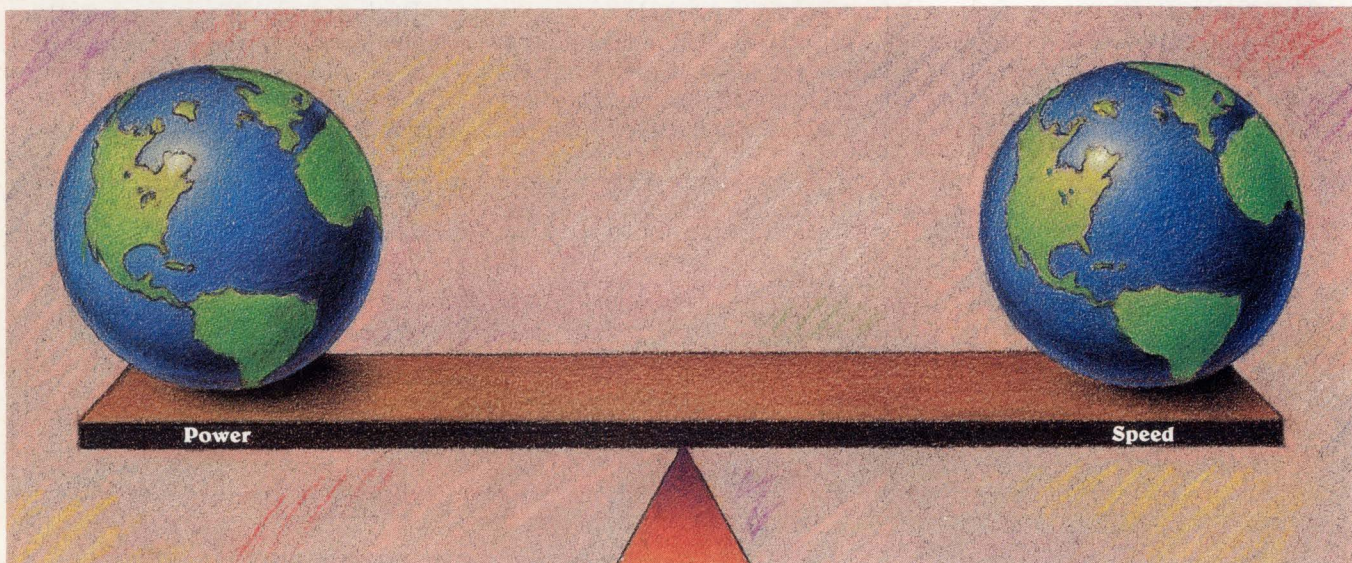
During sampling, g_{m1} connects the input signal to the common gain stages, charging the 10-pF on-chip Hold capacitor. It is connected to ground through S_3 , which is closed



3. TWO DELTA-SIGMA MODULATORS oversample 1-MHz signals to 12-bit accuracy (a) and 500 kHz signals to 14-bit accuracy (b). The former oversamples just 24 times but achieves 12-bit performance with a third-order architecture employing 1- and 3-bit quantizers. The latter oversamples 64 times, keeping its fourth-order design stable by inserting clippers within the third and fourth integrator loops.

THE NO COMPROMISE 22V10

Programmable logic always has been a give-and-take affair. If you wanted speed, the price was power — lots of it. And, if you tried to cut power, you lost the speed. It seems you could have either one or the other — but not both. **NOW YOU CAN HAVE THE BEST OF BOTH WORLDS.**



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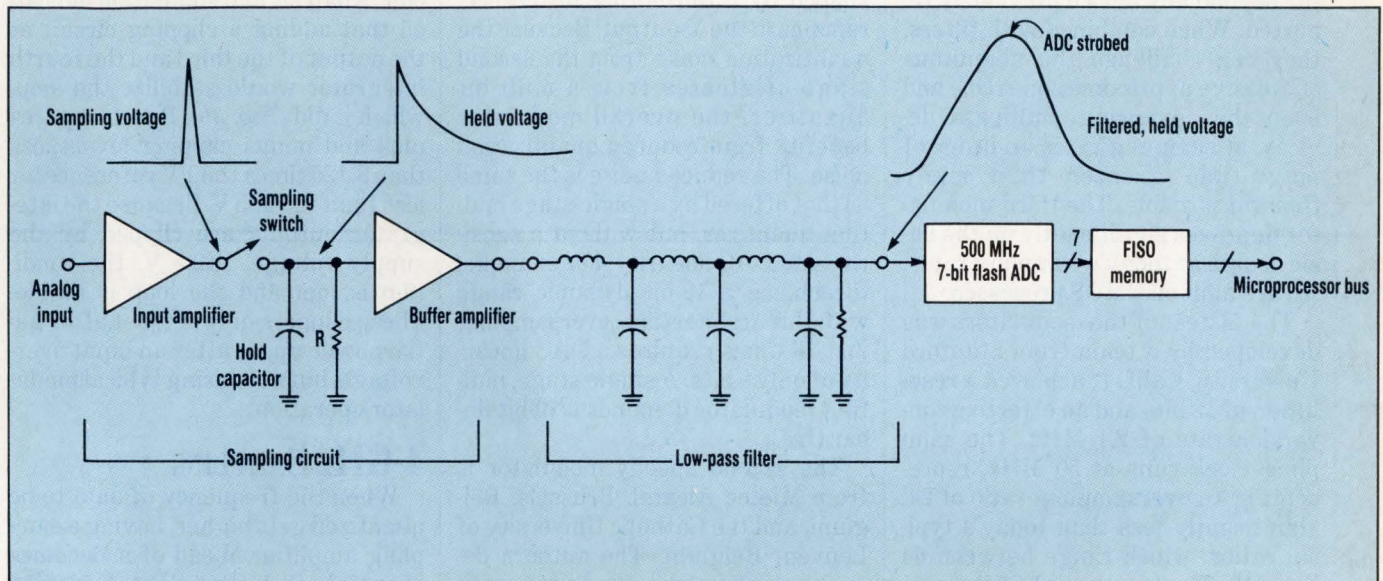
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CIRCLE 152



4. SAMPLING AND QUANTIZATION at 2 GHz is achieved by interleaving, in time, the digital output of four of these circuits, each sampling at 500 MHz. The charge (or the voltage) on the Hold capacitor leaks off at a known rate through resistor R, eliminating the need for the buffer amplifier (which is built on a bipolar process) to have a high input impedance.

(S_2 is also closed). The hold command quickly opens S_2 and S_3 (in about 1 ns) and switches the common amplifier to the output of g_{m2} . Each input of g_{m2} is the gate of a JFET follower. Opening S_2 connects the 10-pF dummy capacitor to g_{m2} , duplicating the charge injected into the Hold capacitor during sampling. With virtually equal charge injected into each capacitor, approximately equal error voltages are developed on the plus and the minus inputs of g_{m2} . Its common-mode rejection then cancels the error.

The Analog Devices sampler not only corrects for charge injection, but amplifier gain and offset as well (Fig. 2b). Its output while sampling isn't an accurate representation of the input. However, when in the Hold state, the internal feedback loop is configured to produce an output identical to the input at the instant of sampling.

When sampling switches S_1 , S_3 , and S_5 are closed, S_2 and S_4 are open. In addition, n-MOS switch MSW_1 is on, closing the feedback loop around the transconductance stage g_{m1} . Switch MSW_2 is also on, grounding the minus input of g_{m1} . The transconductance amplifier forces the voltage at the bottom of the two capaci-

tors, CH_1 and CH_2 , to ground potential. The input signal, as well as the offset voltage of g_{m1} and the input buffer, are sampled (acquired) on hold capacitor CH_1 . Charging the hold capacitor with the offset voltages autozeros the circuit.

When in Hold, S_1 , S_3 , and S_5 are open, S_2 and S_4 are closed. S_1 , S_2 , and S_3 form a "T" network that reduces signal feedthrough in Hold. Switch MSW_1 is off. The feedback path around g_{m1} now includes both capacitors and both buffers. As MSW_1 turns off, error charge is injected onto CH_1 . MSW_2 is turned off at the same time, introducing an equal error on C_Q . Switches MSW_1 and MSW_2 and capacitors CH_1 and C_Q are matched, providing a first-order cancellation of charge injection.

In addition, at the start of sample acquisition, MSW_3 and MSW_4 are turned on for about 50 ns to provide the large, initial charging current for CH_1 and CH_2 , rather than requiring it from the output g_{m1} . The technique reduces their charging time and minimizes the transient voltage swing at the amplifier's output. Overall, acquisition time is shortened by 30%. During the remaining portion of the acquisition time, the n-MOS switches are open, making it possible for the

amplifier to settle to the voltage on the hold capacitor.

Just as sampling doesn't necessarily imply quantization, an oversampling circuit doesn't necessarily imply a delta-sigma design or a complete converter. Though all ten oversampling circuits described at this year's ISSCC employ a delta-sigma architecture, only seven describe complete converters. The other three are simply delta-sigma modulators without digital filters. In fact, all three had to be connected to digital filters for even basic testing.

SEVEN CONVERTERS

Of the seven complete converters, one is a dual, two-chip ADC; two are DACs; and three contain an ADC and a DAC. Delta-sigma devices containing both converter types are being dubbed codecs because of their major application (at present). However, they lend themselves to a wide variety of "analog signal processing" applications with a digital signal processor between them. A power monitor IC represents the seventh paper of the group, covering complete delta-sigma converters.

Two of the three delta-sigma modulators raise effective delta-sigma sampling rates for a given accuracy

far beyond any device previously reported. When combined with filters, they can challenge the ubiquitous successive-approximation ADC, and even the advancing multipass devices, at sampling rates an order of magnitude greater than many thought possible. The third modulator improves significantly on the basic design at today's sampling rates. All are built on CMOS processes.

The fastest of the modulators was developed by a team from Stanford University, Calif. It achieves a resolution of 12 bits and an effective conversion rate of 2.1 MHz. The sampling clock runs at 50 MHz, representing an oversampling ratio of 24, significantly less than today's typical ratios, which range between 64 and 512. The major goal of the project was to come up with an architecture that would provide 12-bit performance at conversion rates beyond 1 MHz while avoiding stringent component-matching requirements and clock rates in the microwave region.

Low oversampling ratios significantly reduce the effectiveness of increasing the order of the modulator's noise-shaping. Alternatively, multibit quantization (where a multibit flash ADC replaces the more common 1-bit comparator) can reduce baseband quantization noise. However, the technique can impose stringent linearity requirements on the quantizer's DAC.

The Stanford team chose the multibit quantizer approach but reduced its dependency on DAC linearity by locating the quantizer in the final stage of a third-order cascaded modulator (Fig. 3a). The effects of multibit DAC nonlinearity are attenuated by second-order noise shaping. The more critical first-stage quantizer has only two analog output levels, so it's inherently linear.

The architecture is similar to a cascade of two stages with 1-bit quantization. The second integrator's output in the first stage is quantized by the second stage. The digital outputs of the two stages, y_1 and y_2 , are combined with simple digital circuits to cancel the quantization noise of the first stage. Ideally, only the quantization noise of the second stage,

shaped by a third-order difference, remains in the Y-output. Because the quantization noise from the second stage originates from a multibit quantizer, the overall modulator benefits from reduced quantization noise. The reduced noise is the same as that offered by a single-stage multibit quantizer, but without a sensitivity to DAC linearity. For example, to achieve a 12-bit dynamic range with this architecture, oversampling just 16 times requires a DAC linearity of only 6 bits. A single-stage, multibit modulator demands a 10-bit linear DAC.

The second speedy modulator is from Mietec Alcatel, Brussels, Belgium, and the Catholic University of Leuven, Belgium. The authors describe a delta-sigma modulator with 14-bit resolution and a linearity of 93 dB (15 bits), while handling a 500-kHz signal. The modulator uses an oversampling ratio of 64 (a 32-MHz sampling clock). The designers beat the speed-accuracy trade-off by increasing the order of the modulator to four. But increasing modulator order introduces stability problems. For some initial conditions, the loop is stable for the signals within the feedback loop, while for other conditions it oscillates.

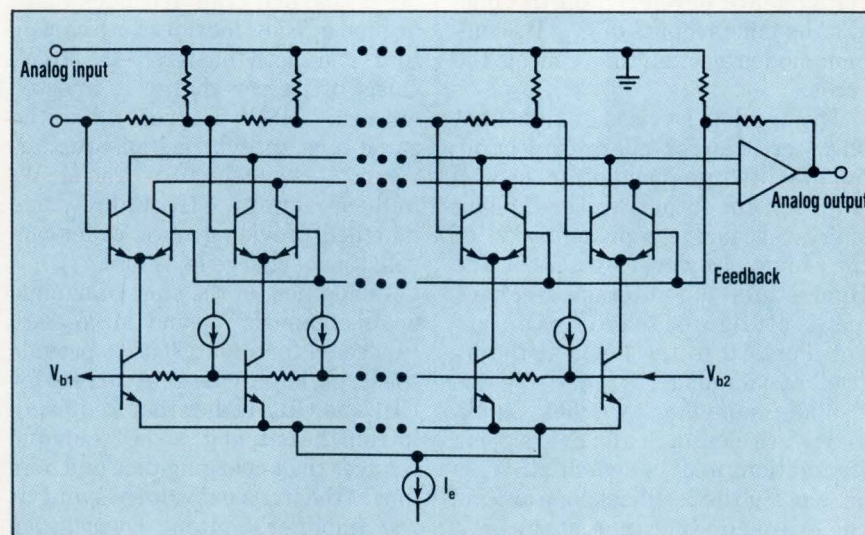
The Alcatel designers decided on a fourth-order (four integrators) cir-

cuit. Analysis and simulation indicated that adding a clipping circuit at the output of the third and the fourth integrator would stabilize the loop, which it did (Fig. 3b). But it requires plus and minus clipping levels less than 3.125 times the 1 V reference, or less than ± 3.125 V. Because the integrator outputs are clipped by the supply voltage, ± 2.5 V, the condition is met and the loop is stable. These clippers only act just after initial power-up, or after an input overvoltage, but not during typical modulator operation.

4-GHZ SAMPLING

When the frequency of data to be quantized gets higher, having a sampling amplifier ahead of it becomes essential. But that SHA becomes harder to build. Few designers will deny that when pushing speed and/or accuracy in data acquisition, the SHA is always the weak link. As a result, designers at Hewlett-Packard Co., Colorado Springs, Colo., decided a new sampling technique was needed to build a 2-GHz, 8-bit data-acquisition system—essentially a multichip ADC. Two of the ADCs running in tandem (sampling rate = 4 GHz) digitize a 1-GHz sine wave to an accuracy of 5.9 effective bits.

The "system" contains four major blocks: the new sampler, low-pass fil-

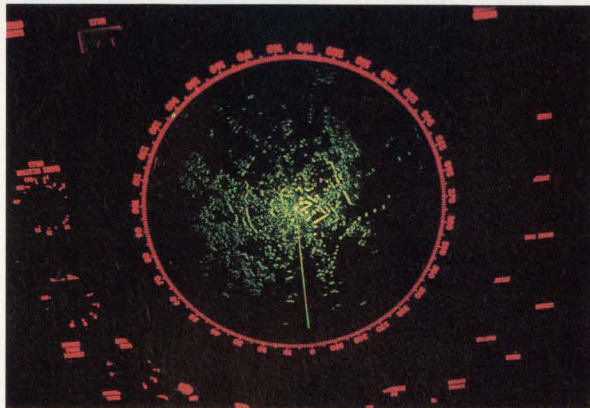


5. BY STEERING CURRENT to transconductance amplifiers composed of differential transistor pairs in this circuit developed by Analog Devices, the control voltage— V_{b1} minus V_{b2} —turns the DAC-like ladder network into a variable attenuator with 40 dB of gain control from dc to 50 MHz.

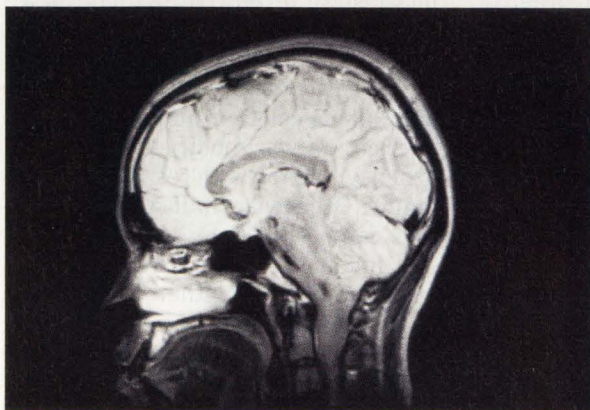
The only 16-bit, 500 kSPS SADC with guaranteed dynamic performance.

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With its wide dynamic range and low noise, the AD1382 has a great image with people working in magnetic resonance imaging applications.

The AD1382 delivers guaranteed 100% production tested SNR, THD and peak distortion performance at three input frequencies and over two input ranges – testing that gives you the confidence to design for the best possible noise performance in your system.

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And since it's a single package, it's easier to design in and uses less

board space than more expensive modular or multipackage solutions.

For a better picture of what the AD1382 can do for you, contact Analog Devices at 1-800-262-5643. Or write to Analog Devices, P.O. Box 9106, Norwood, MA 02062-9106.

AD1382



A 16-bit 500 kSPS SADC, the AD1382 provides excellent dynamic and static performance in a dual in-line ceramic package.

Guaranteed (@25°C, ± 5 V input range):

SNR

- 5 kHz 90 dB min
- 100 kHz 90 dB min
- 200 kHz 88 dB min

THD & Peak Distortion

- 5 kHz – 90 dB min
- 100 kHz – 88 dB min
- 200 kHz – 82 dB min

DC specifications include:

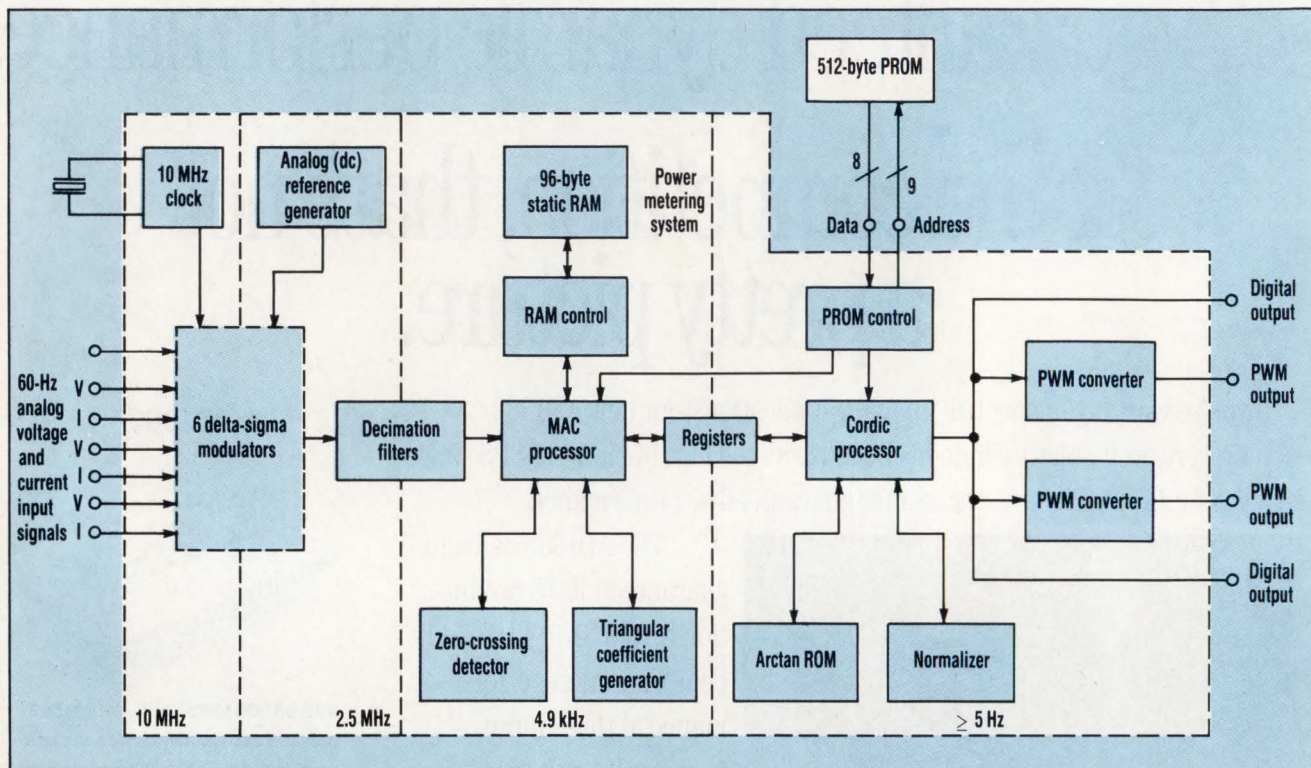
0.0015% FSR INL, 0.0006% FSR DNL and NMC guaranteed to 16-bits

Other features include:

**Zero offset autocalibration
± 5 V, ± 10 V Bipolar input range**

An evaluation board for the AD1382 is available.





6. COMBINING DELTA-SIGMA ADCS with a digital signal processor results in a power-monitor IC that takes voltage and current inputs from three-phase ac power sources and puts out digital and analog PWM signals. The signals carry computed frequency and power information based on the inputs.

ters, flash ADCs, and fast-in, slow-out (FISO) memories. The sampler, a bipolar chip, consists of four circuits using the new technique, each capable of analog sampling at 500 MHz. The samplings are interleaved in time resulting in an effective sampling rate of 2 GHz. Each of the sampler's four outputs drive a thick-film low-pass filter. They in turn feed a pair of dual, 7-bit (8-bit linear) bipolar-IC₇ flash ADCs. The outputs of the four ADCs are stored in four 4k-by-16-bit CMOS FISOs.

The ADC needs a new sampling circuit because holding a charge on a tiny capacitor, even for a few nanoseconds while reading it accurately, demands a very-high impedance buffer. This isn't easily achieved from a bipolar process. Each of the four sampling circuits consists of two amplifiers separated by the sampling switch, the Hold capacitor, and a resistor R (Fig. 4). When the switch closes, the input amplifier charges the Hold capacitor. However, its charge can leak off at a rate con-

trolled by the parallel resistor. Therefore, the buffer amplifier doesn't need a high input resistance.

The response of the high-order LC filter, driven by the buffer, dominates the response of the post-sampling circuits. The system timing clock strobes the ADC just as the filter output reaches its peak—the point at which the waveform's slew rate is a minimum—resulting in maximum converter accuracy. However, the filter's peak output voltage must settle to zero in one sample period to eliminate interference with the next sample.

GILBERT AND GILBERT

"Who needs analog multipliers?" can still be heard among designers. To respond to those doubters, they make good analog modulators and demodulators. A paper from Ruhr University, Bochum, Germany, and Telefunken Electronic, Heilbronn, Germany, describes an analog multiplier with a frequency response from dc to 6 GHz through both input ports

to the output. That gives this silicon—not GaAs—chip the ability to demodulate 8-Gbit/s differential phase-shift-keyed (DPSK) data in a coherent optical-fiber data link, its targeted application.

The basic (approximately 25-year-old) Gilbert-cell four-quadrant multiplier circuit was modified to achieve exact symmetry with respect to both inputs. Otherwise, multiplication errors can occur at the high frequencies involved. The circuit uses two multiplier cores (rather than one). Both inputs of each core are fed by the two input signals. The two outputs are summed to supply the demodulated output.

Barrie Gilbert himself, of Analog Devices' Northwest Labs, Beaverton, Ore., has taken a new tack to control gain. His paper describes an IC containing a pair of fixed-gain amplifiers each preceded by a passive resistor-ladder network. An external differential control voltage ($V_{b1} - V_{b2}$) interpolates the network continuously, creating up to 40 dB of con-

tinuous attenuation between input and output at a scale factor of 32 dB/V (Fig. 5). The circuit shows a flat response from dc to its 3-dB frequency (50 MHz) for a 1-V rms input.

Increasing the gain-control voltage sequentially steers the current source I_c through the eight transistors to which it's connected and into the differential transconductance stages connected to the resistor ladder. The effect is analogous to a DAC-type ladder network, in which the "switches" have a continuously variable on-resistance. Instead of stepped changes in gain, the gain is varied smoothly from one tap to another. The technique lends itself to many remote and automatic gain-control applications, particularly for fast or wideband signals.

SYSTEMS ON A CHIP

The buck regulator comes from a joint power-IC design team from International Rectifier, El Segundo, Calif., and National Semiconductor. Built on a 5- μ m, bipolar-CMOS-DMOS process, its basic specifications represent several firsts. The regulator's 10-A current rating is twice that of available devices and its ability to run with 60 V across the switch is one and a half times the voltage rating of 5-A regulator chips. The 80-V (maximum) power switch is a DMOS FET rather than a bipolar transistor, giving it switching speeds to 1 MHz, ten times that of present 5-A regulator chips. Other MOSFET switching regulators top out at a few hundred milliamperes, albeit with off-line voltage ratings. This chip runs off voltages that can be as low as 9 V.

Users program the IC for operation in voltage or current mode by pin-strapping. The voltage mode is faster, yielding 100-ns minimum controlled on-times, bringing minimum duty cycles as low as 10% while switching at 1 MHz. In the current mode, the minimum on time rises to 200 ns, and thus duty cycle at 1 MHz is 20%. However, current-mode operation permits paralleling of regulators and removes one pole from the loop, simplifying stabilization. In a typical buck regulator circuit, gener-

ating 5 V at 3 A from 15 V, efficiencies run 92%, 82%, and 73% at 200 kHz, 500 kHz, and 1 MHz, respectively. A circuit converting 60 V to 5 V at 10 A, and switching at 300 kHz, achieves an efficiency of 77%.

Floating driver-latch circuits turn the 120 m Ω switch on and off in under 30 ns. Small current pulses, generated by logic and level shifted by single-cell DMOSFETs, control the driver latches. The power switch is a sense or mirror FET. The current from seven of its cells is compared to a reference and the switch is turned off if its current exceeds 12 A. If the 200-ns response time of the pulse-by-pulse current-limit circuit isn't fast enough, a runaway-detection block drops the chip's oscillator to 33 kHz. The IC also incorporates ramp compensation, a function just appearing on regulator and controller ICs. It ensures loop stability while operating in current mode with duty cycles greater than 50%. An internal voltage regulator generates the supply rail for the chip's low-voltage circuits, including those that handle thermal shutdown and undervoltage lockout.

A team from General Electric's Corporate R and D Center, Schenectady, N.Y., and the Yokogawa Electric Corp., Tokyo, Japan, describe a mixed analog-digital CMOS ASIC aimed at monitoring (measuring) three-phase ac power. It takes the analog signals from three voltage and three current transformers and supplies two bit-serial digital and two pulse-width-modulated (PWM) analog outputs. The output data represents rms voltages and currents; active, reactive, and apparent power; and power factor, phase-angle, and frequency, all calculated from the analog inputs by an on-chip DSP (Fig. 6). The PWM outputs drive analog meters, the digital outputs are fed to a host computer.

Each of the six 150-mV rms, 40-to-70-Hz input signals feeds a first-order delta-sigma modulator. These fully differential switched-capacitor circuits oversample the inputs at 2.5 MHz (1/4 the master-clock frequency) and apply their output bit-streams to digital low-pass and sinc²,

finite-impulse-response (FIR) decimation filters. The filter outputs feed a special-purpose digital signal processor that calculates the output data. Other analog circuitry generates an analog ground at 2.5 V (half the supply voltage) and the 1.25-V reference for the modulators. Because they operate on the difference between the single-ended input signal and analog ground, the stability and precise value of analog ground are not critical. Gain error caused by the limited accuracy of the reference is corrected for in the digital signal processor. The PWM data is unaffected by power-supply drift because the modulator gain changes proportionally in a compensatory direction.

The output of the delta-sigma decimation filters is sent to a multiply-accumulate (MAC) processor that executes calibration, cross-product, and low-pass filtering algorithms. The MAC performs the multiply-accumulate required by the "system's" signal-processing algorithms. It gets help from a (digital) zero-crossing detector circuit, a triangular coefficient generator for the sinc² LPF coefficients, and a static RAM for intermediate variable storage. Using its bit-serial multiplier, the MAC performs a complete program for each set of sampled data from the ADCs. It performs a 16-bit-by-32-bit multiply each 3.2- μ s instruction cycle. The MAC outputs are decimated to 5 Hz and passed to the Cordic processor for LPF gain normalization and computation of the output functions.

The chip is fabricated on a 5-V, 1.5- μ m double-polysilicon CMOS process. Metering accuracy for both power and frequency is better than 0.04% of the 150-mV full-scale rated input voltage. The delta-sigma ADCs show a signal-to-(noise + distortion) ratio of 77 dB, or better than 12 bits. The device uses about 160 mW from a 5-V rail. □

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CIRCLE 104

I S S C C

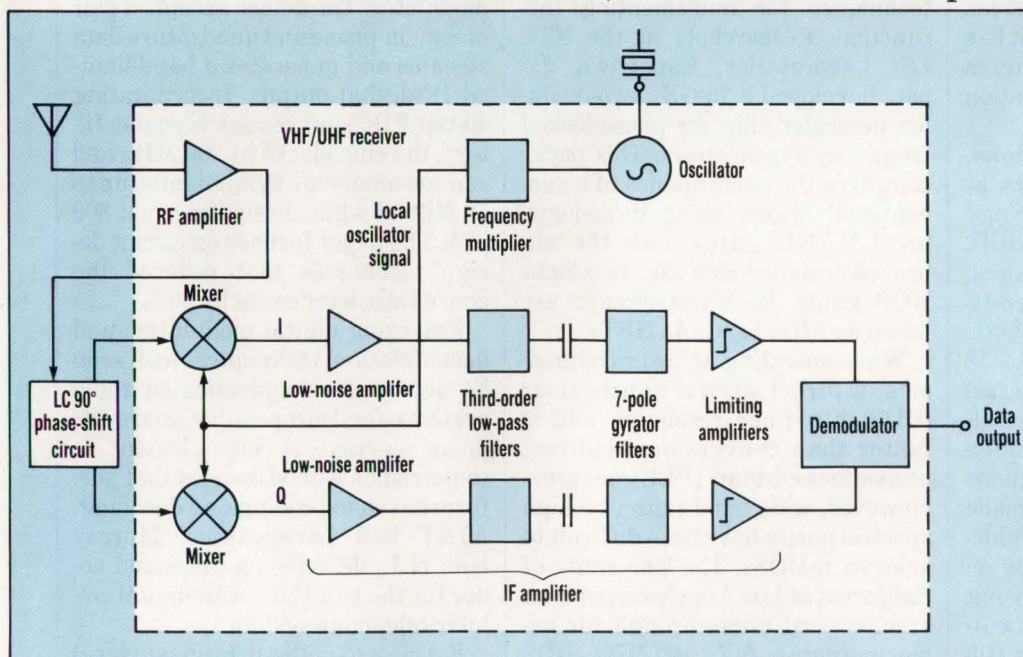
COMMUNICATIONS

The complex nature of signal-processing algorithms for communications applications has triggered the emergence of more and more devices that resemble digital signal processors. At this year's ISSCC, new communication-system building blocks that bring improvements in speed, precision, sensitivity, and circuit-integration levels illustrate this trend. These improvements promise smaller, less-costly, and more user-friendly products for all aspects of communications technology, including data transmission, imaging, and radio.

Previous single-chip receivers for paging applications were restricted to operation below 200 MHz. Operation at higher frequencies required using external channel-filtering components. However, researchers at Philips Radio Communica-

tions Systems Ltd., Cambridge, Great Britain, developed a single-chip radio receiver for VHF and UHF wide-area paging transmissions up to 500 MHz with frequency-shift keying (FSK) data rates up to 1200 baud.

The 4.6-by-3.8-mm bipolar IC integrates low-pass filters to give immunity to both 70-dB



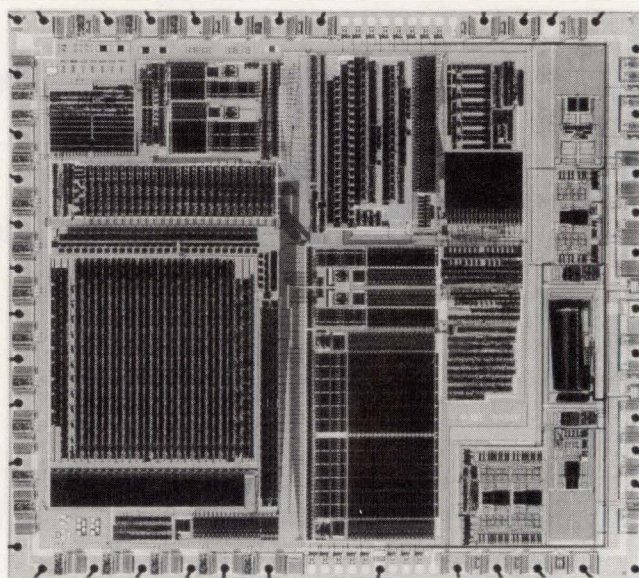
1. AIMED AT PAGERS, a 20-to-500 MHz, 1200-baud frequency-shift-keying receiver uses two identical IF channels, 90° apart in phase, to minimize die size. The technique is called "Zero IF."

adjacent-channel crosstalk and 60-dB intermodulation. Drawing 2.7 mA at 2 V, the device has a -126-dBm sensitivity. Off-chip passive components are only required for local-oscillator (LO) frequency determination and RF filtering.

The receiver employs a design technique called "Zero IF." It's a single-stage superheterodyne circuit with a nominal intermediate frequency (IF) of zero. The architecture makes possible channel filtering with integrated, minimum-power low-pass filters (Fig. 1). To separate the sidebands above and below the carrier, two identical IF channels (I and Q) carry signals mixed down in phase-quadrature from the radio frequency. That is, there's 90° of phase-shift between the signals carried by the two IF channels.

Frequency mixers are critical building blocks for communications systems operating at microwave frequencies in the gigahertz range. Although a conventional passive mixer implemented with Schottky diodes and baluns is a simple solution, it has high conversion losses and requires a high LO drive. Moreover, isolation between ports is poor.

To overcome these limitations, Hughes Aircraft Co. engineers at the Advanced Circuit Technology Center, Manhattan Beach, Calif., and Research Laboratories, Malibu, Calif., designed an active mixer IC based on a new bipolar technology. Operating at frequencies up to 16 GHz, the device uses heterojunction bipolar transistors (HBTs) fabricated with AlInAs/GaInAs (aluminum-indium-arsenide/gallium-indium-arsenide). Compared with HBTs made with other compound semiconductors, the new material reportedly reduces base and collector transmit times to get higher power-gain cut-off frequencies. The chip uses a Gilbert-cell multiplier, an LO driver, and an intermediate-frequency (IF)



2. THE DSP SECTION of NEC's 16-bit oversampling codec is located in the lower right-hand quadrant of the chip. Analog circuits are positioned vertically along the right edge to minimize interference from the digital section and power-supply rails.

output buffer. The 0.188-by-1.135-mm chip operates on +10-V and -5.2-V power supplies and dissipates 1 W.

The frequency synthesizer is a key element in high-quality radio systems with high channel density for urban networks and satellite-mobile communications systems. Two conference papers disclose improved techniques for implementing this function. Researchers at the NTT LSI Laboratories, Kanagawa, Japan, developed a 15-GHz two-modulus prescaler chip for phase-locked frequency synthesizers. This paper compares the performance of a conventional design using three-level NAND gates with the improved design, which uses two-input NOR gates. Both test circuits are based on AlGaAs/GaAs HBTs.

When operating at lower frequencies, a direct digital synthesizer (DDS) has finer resolution and is faster than conventional indirect phase-locked-loop (PLL) designs. However, wide bandwidth and high spectral purity have been difficult to achieve in DDSs. The University of California at Los Angeles reports an architectural breakthrough for implementing a 5-V, 150-MHz DDS chip. The DDS has a -90.3-dBc worst-case digital spurious output over the

entire tuning range. The 1.25- μ m radiation-hardened CMOS chip covers a bandwidth from dc to one-half the clock frequency in 0.035-Hz steps, with a 6.7-ns switching speed and a tuning latency of 13 clock cycles.

One way to increase data rates in digital-communications systems is to use more complex modulation formats to allow faster data transmission without a corresponding increase in bandwidth. Currently, most baseband signal processing is implemented with analog techniques, which are expensive and vulnerable to the effects of uncontrolled operating environments. Several conference papers introduce

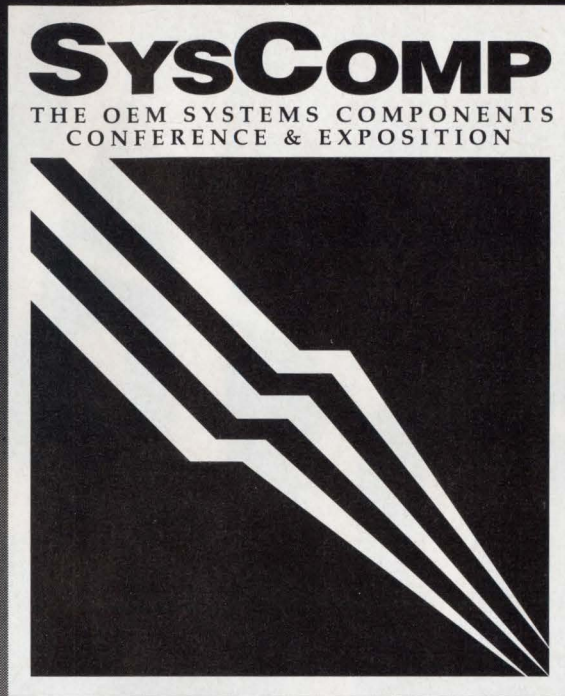
new digital modulation techniques that challenge analog approaches. Notable among these is a presentation by UCLA describing a 200-MHz all-digital modulator intended for digital-radio applications.

The 1.2- μ m CMOS chip operates as the front-end signal-processing element in a high-speed quadrature modulator. The device accepts a pair of 8-bit in-phase and quadrature data streams and generates a band-limited IF digital output. Incorporating 40-tap FIR square-root Nyquist filters, the chip clocks at 200 MHz and can accommodate symbol rates up to 50 Mbaud while dissipating just 800 mW. The paper focuses on circuit design techniques that reduced the chip's transistor count by 28%.

Emerging digital modulation and demodulation techniques will soon be deployed in sophisticated radio systems for European cellular-telephone service. A key element in these radios will be devices that perform baseband coding and decoding. AT&T Bell Laboratories, Murray Hill, N.J., describes a baseband codec for the pan-European digital cellular-telephone system.

Fabricated with a 0.9- μ m two-level poly, two-level metal CMOS process, the 21-mm² chip is a mixed-signal

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subsystem. The analog portion has 8-bit, 9-bit, and 10-bit digital-to-analog converters (DACs), 10-bit sigma-delta analog-to-digital converters (ADCs), and programmable-gain amplifiers. The digital section includes decimators, equalizers, and dc offset-correction logic, and it supplies control and timing functions.

The chip's receive and transmit sections each have two signal paths, one for the in-phase signal and the other for the quadrature-phase signal. AT&T's paper also covers the built-in scan path and test modes for testing the digital portions of the chip. To conserve power, each section of the device can be powered-down independently. The codec operates from a 13-MHz clock and has a 250-mW peak power dissipation when all sections are running.

THE POWER OF DSP

A presentation by NEC Corp., Kawasaki, Japan, illustrates the rising trend toward applying DSP circuits on codec chips to execute intensive arithmetic operations. Optimized for telecommunications and audio applications, NEC's 1.2- μm CMOS codec combines DACs and ADCs with DSP circuits that perform precision decimation and interpolation filtering (Fig. 2). The chip also includes I/O RAM, data RAM, and instruction ROM. The accuracy for analog-to-digital and digital-to-analog interfaces are 16 bits and 18 bits, respectively, at a 25-kHz signal bandwidth. To obtain this level of accuracy, second-order, noise-shaping converters with a 256 oversampling ratio and DSP filtering are used. Measuring 6.27 by 7.02 mm, the 5-V codec dissipates 200 mW.

Applying DSP techniques to magnetic storage-media technology is illustrated in a joint paper by IBM Corp.'s Research Div., San Jose, Calif., and the National Chiao Tung Univ., Hsinchu, Taiwan. The paper describes a 30-MHz trellis codec chip

designed to improve the reliability of partial-response, maximum-likelihood recording channels. Sized at 4.2 by 5.2 mm, the 1.2- μm CMOS chip has a 12-Mbit/s data rate and dissipates 0.55 mW.

DSP techniques are also appearing in devices for networking technology, which is a major driving force behind the development of complex communications chips. For example, many applications can still exploit the large installed base of twisted-pair data-transmission lines for implementing the integrated services digital network (ISDN). A presentation by Level One Communications Inc., Folsom, Calif., describes a

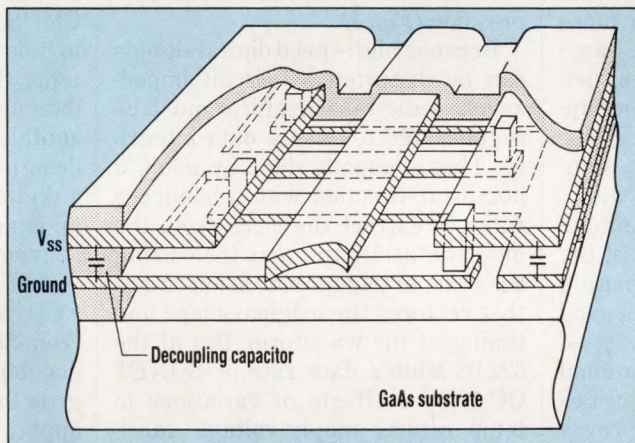
multiplier, registers, and control logic. These circuits are interconnected in an 8-step pipelined architecture. The presentation shows how the processor performs such functions as decimation, interpolation, pulse-code modulation (PCM) filtering, and PCM encoding and decoding. Other on-chip functions include ring trip and adaptive line balance. Communication with a standard microprocessor is performed through a serial interface. Fabricated with a 1- μm CMOS process, the 35-mm² chip typically dissipates 250 mW while running at 16.384 MHz.

Another critical ISDN requirement is a U-interface line-driver circuit that can drive low-impedance loads with low distortion.

A joint paper by SGS-Thomson Microelectronic, Agrate Brianza, Italy, and the Univ. of Pavia, Italy, describes an amplifier/buffer that delivers 6 V pk-pk into a 100- Ω impedance with 78-dB linearity at 40 kHz. Key to this performance is creating an in-band pole-zero doublet by applying positive feedback around the input stage to multiply the input transconductance. The circuit is fabricated with a 1.5- μm process to reduce the area occupied by output devices to 25% of the 1200-mil² die area. The 5-V chip's power consumption is just 20 mW.

New devices are also surfacing for the future broadband ISDN (B-ISDN). This network will use asynchronous-transfer-mode (ATM) transmission to interconnect various terminals, such as telephones, telefaxes, pay TVs, and workstations. Transmitted data will be formatted as 53-byte packets or cells. A key element for the B-ISDN is the ATM switch that directs data traffic between the various networked terminals. High-efficiency operation requires the switch to include FIFO buffers that are shared by all of the switch output ports and allotted to one specific port as demanded.

Researchers at Toshiba Corp., Ka-



3. THE TRANSMISSION LINE in Toshiba's MUX/DEMUX chip set consists of a high-speed signal line placed over a ladder-shaped grounded first metal. To reduce power-line noise and crosstalk, the decoupling capacitor, which has a metal-insulator-metal structure, is laid down at both ends of the transmission line.

mixed-signal transceiver chip for full-duplex data transmission over 4-wire twisted-pair telephone lines. Using alternate-mark-inversion (AMI) line coding, the transceiver has 14 user-selectable bit rates that range from 2.4 to 72 kbits/s. The paper covers design details of the line driver, which differentially drives a 2.74-V peak pulse onto a 270- Ω load.

DSP techniques in a silicon solution for data transmission over analog subscriber lines is featured in a paper from Ericsson Telecom AB, Stockholm, Sweden. The all-digital processor integrates all of the circuitry required to serve eight communications channels, including memory, accumulators, an ALU, a

wasaki, Japan, describe the development of an 8-input, 8-output ATM switch containing a 128-kbit shared buffer memory. The design is based on a 0.8- μm biCMOS, double-layer metal technology to reach a 400-Mbit/s throughput while operating at 100 MHz. This data rate exceeds the minimum requirement of B-ISDN, which at a 155.52-Mbit/s line bit rate demands a minimum memory throughput of 1.2 Gbits/s. Powered from a 5.2-V supply, the 14.5-by-14.25-mm die contains over 1 million transistors.

Switching between larger arrays of networked terminals requires larger ATM switches, which are vulnerable to contention problems. This condition occurs when two or more data cells are destined for the same output at the same time slot. In such cases, the ATM switch needs the support of a time-slot control processor. NEC Corp. has come up with a solution for a 32-by-32-port ATM switch. Based on an improved content-addressable-memory architecture, the scheduling content-addressable memory (SCAM) adds interleaved sense-and-update and quick status-shift operations to a conventional CAM circuit. NEC's paper describes how the pipelined design improves switch throughput by a factor of 5.6.

Two papers offer solutions to problems associated with the synchronous optical network (SONET). Available multibit (4 bits or more) multiplexer and demultiplexer chip sets with clock frequencies reaching

5 GHz are adequate for first-generation SONET applications. But next-generation STS-192 optical-fiber communication systems will need 8-bit multiplexers and demultiplexers that operate with 10-GHz clocks. For STS-192 applications, a report from Toshiba describes an 8-bit two-chip set made with a 0.5- μm , tungsten-tri-gate GaAs MESFET process.

Both devices have a tree-type architecture and use a dynamic divider instead of the conventional shift register and static divider. Of particular interest is the novel 50- Ω on-chip transmission line design, which has a decoupling capacitor for impedance matching to external devices and for crosstalk and power-line noise suppression (*Fig. 3*).

Because high-speed digital signals can be distorted by circuit impedances, a digital waveform must be regenerated to ensure data integrity. This is usually done by using a nonlinear function with a bandpass filter to extract the clock from the input data stream, and then using the clock to trigger a decision circuit that restores the original shape and timing of the waveform. But at the 622.08-Mbit/s data rate of SONET OC-12, the effects of variations in temperature, supply voltage, fabrication processes, and aging are magnified in conventional clock-extraction and data-retiming circuits.

Test results on a developmental circuit by Hewlett-Packard Co., Palo Alto, Calif., show a potential for overcoming these limitations. The

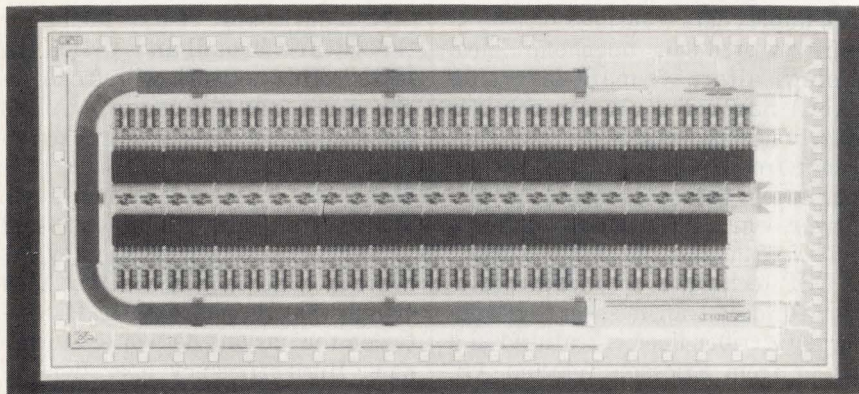
circuit integrates the clock-recovery, data-regeneration, and clock-to-data alignment functions on one chip.

ADVANCES IN IMAGING

Conference papers on developments in video-signal processing describe various performance improvements. These advances result from design efforts on architecture, logic, and circuit design, rather than through technology innovation. Fresh approaches to video-processor design culminate in higher speed and lower noise, making it possible for smaller and more economical image sensors. For example, Fujitsu Ltd., Kawasaki, Japan, describes a fully digital PLL implemented in a 1.5- μm CMOS gate array. Intended for use in television image-processing systems, the device receives 8-bit image data and synchronizes it to the horizontal sync signal (*Fig. 4*). Key to the design is a digital phase detector and a digital PPL architecture, creating an image quality superior to that of conventional analog PLL designs.

A digital signal processor for a CCD camera is the subject of a paper from Sony Corp., Tokyo, Japan. This development typifies the continued growth of DSP techniques into new application areas. Designed to reduce the size of CCD cameras while upgrading image quality, the 120k-transistor chip includes 8 multipliers, DRAM, ROM, and two DACs. The device generates NTSC (National Television Standard Committee) or PAL (phase-alternating line) outputs from CCD sensor inputs. Operating at 9.5 MHz and running on a 3.6-V power supply, power dissipation for the 8.37-by-8.72-mm CMOS die is 250 mW.

A second NTT presentation addresses a 300-MOPS video-signal processor that derives its performance from a macrocell-oriented building-block design. Architecturally resembling a classical DSP chip, the processor uses a 0.8- μm biCMOS technology to integrate four pipelined data-processing units and three parallel I/O ports on a 15.2-by-15.2-mm die. Each pipelined data path operates at 25 MHz, and 16- and 24-bit fixed-point data formats contribute



4. THE ALL-DIGITAL PLL CHIP from Fujitsu receives 8-bit image data sampled every 70 ns and synchronizes it to the television horizontal sync signal. Conventional designs use less-stable analog circuits for the phase detector, loop filter, and voltage-controlled oscillator.

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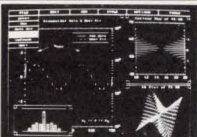
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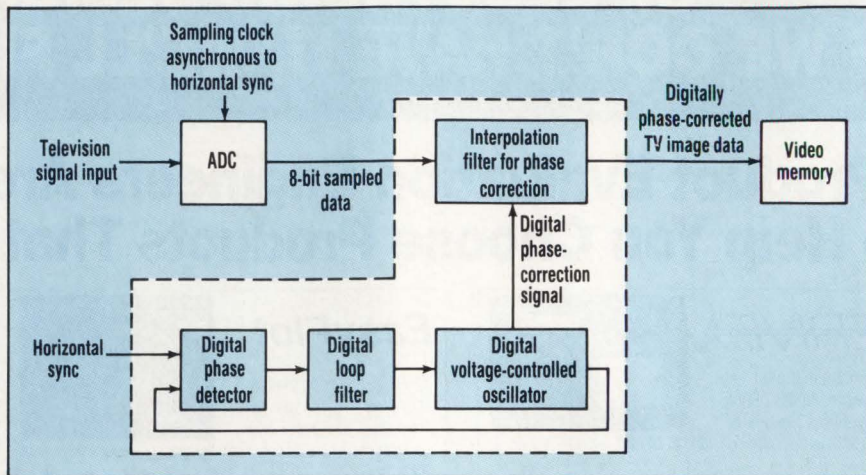
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5. TO MINIMIZE CHIP AREA, the 775-stage CCD delay line in MIT's programmable image processor has a U-shaped configuration. Floating-gate taps along the line nondestructively sense image-pixel intensity and couple the signals to the analog ports of corresponding multiplying DACs.

to the 125-Mbit/s I/O data speed. Using two power supplies—3 V and 5 V—limits power consumption of this sizable chip to 1.0 W per 25-MHz instruction cycle.

Under the sponsorship of DARPA, the Massachusetts Institute of Technology, Lexington, Mass., developed a programmable image processor that can enhance or skeletonize an image, remove signal noise, or extract feature information. Based on CCD technology, the processor performs 1 billion arithmetic operations/s while dissipating under 1 W at 10 MHz. The 27-mm² chip integrates a unique CCD tapped delay line to shift and hold gray-level image data, 49 multipliers, and 49 twenty-stage, 8-bit parallel CCD digital shift registers (Fig. 5).

MIT's paper discusses device design considerations and test results for a 500-kHz clock rate. The results indicate a transfer efficiency better than 99.999%. The processor also exhibits a dynamic range exceeding 45 dB when programmed to detect line segments with 20 different spatial orientations.

Keeping pace with advances in video-signal-processing technology, CCD image sensors are being developed with smaller pixel size, lower noise, higher sensitivity, and higher speed. One approach to getting higher sensor performance is reported by

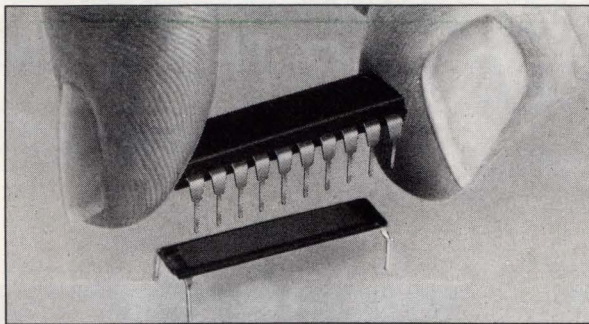
Hitachi Ltd., Tokyo. The paper describes a 410,000-pixel image sensor with an image area 4.9-mm-horizontal by 3.7-mm-vertical for a 1/3-in. lens format. To suppress video-camera background noise, Hitachi proposes using a new feedback field-plate amplifier design with reduced input capacitance and increased sensitivity. Using on-chip microlenses, the sensor's sensitivity is 41 mV/lx.

NEC describes another approach that uses a capacitance-coupled charge detector with a 94-dB dynamic range. Based on a platinum-silicon Schottky-barrier technology, the infrared CCD sensor measures 7.1 by 5.1 mm, which is suitable for a 1/3-in. lens format.

Finally, in one of the more exotic discussions at this year's conference, Russian scientists will describe a GaAs thin-film traveling-wave amplifier chip. Space-charge waves (SCWs) formed from hot electrons moving in the thin films can be used to amplify or filter microwave signals directly at the receiver input—a handy feature for such applications as phased-array radar in the 50-to-80-GHz range. □

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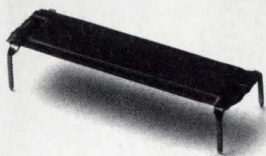
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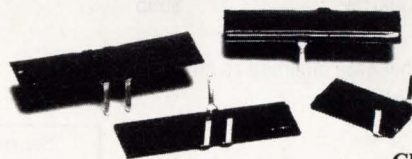
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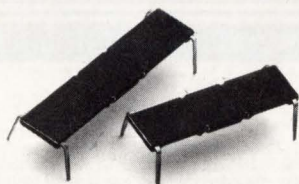
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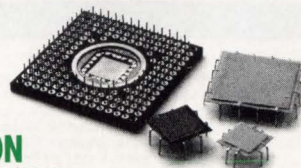
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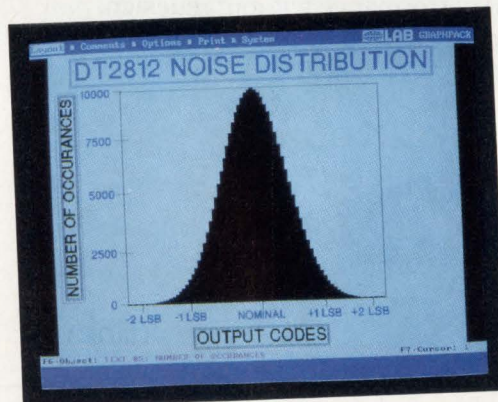
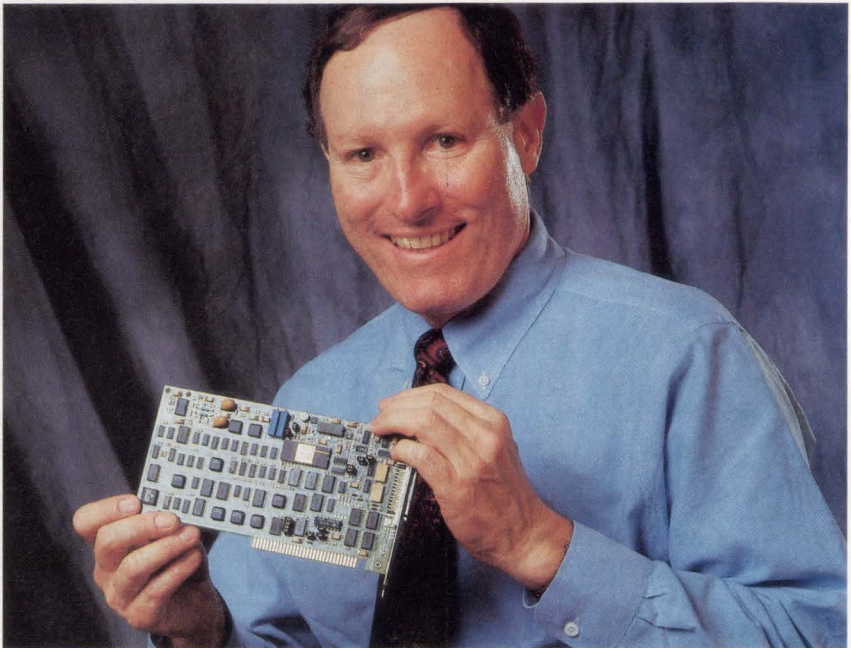
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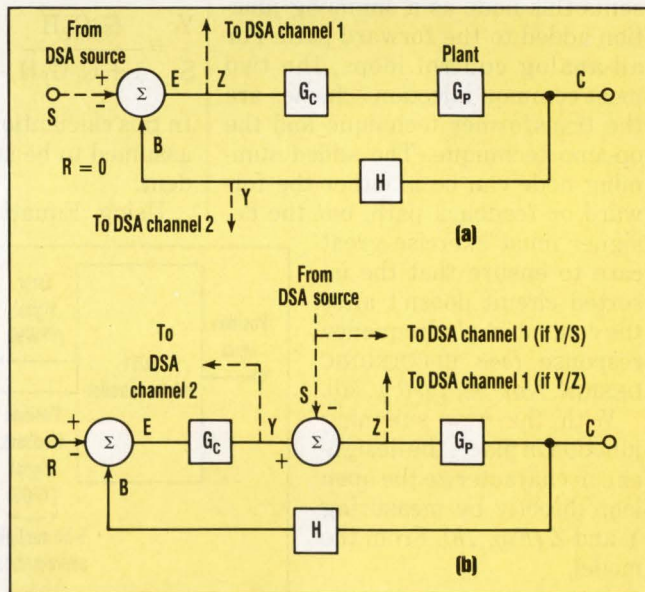
CHARACTERIZE DIGITAL CONTROL LOOPS

A SOFTWARE SUMMING
JUNCTION AND
A DYNAMIC SIGNAL
ANALYZER MAKE EASY
WORK OF OPEN-LOOP
MEASUREMENTS.

A distinct pattern is being forged in the circuit-design process: system circuit blocks traditionally built in analog form are going digital. Many control systems, for example, now have a mixed analog-digital loop that includes digital compensator and/or digital feedback circuitry. Measuring such parameters as gain and phase margin in these mixed-signal loops is a challenge.

At first glance, designers might want to adapt the well-known technique for measuring analog control systems. That method involves stimulating the loop with an external signal via an analog summing junction, then adding a DAC to convert the signal of interest to analog form. A DAC, however, would introduce major errors and also require additional complex circuitry. A better solution would be to use a software summing junction into which a digital stimulus signal is injected. The following example shows how this method can be used to characterize a pulse-width-modulated (PWM) digital control loop in a drafting plotter.

In the standard model of a single-loop control system, the G_c block represents compensation added to optimize the closed-loop performance and ensure adequate loop stability. To characterize the loop performance, designers must introduce a stimulus signal into the loop and either measure the open-loop (OL) transfer function directly or calculate the OL gain from the measured closed-loop (CL) curve. The simplest measurement setup uses a two-channel dynamic signal analyzer (DSA) with source capability (*Fig. 1a*). The source excites the loop with a



1. IN THIS STANDARD MODEL of a feedback closed-loop control system, the dashed lines show the connections to the digital signal analyzer (DSA). If $R = 0$, open-loop measurements can be made directly (a). If not, a summing junction is needed (b).

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DIGITAL OPEN-LOOP MEASUREMENTS

sine wave or broadband flat-spectrum signal while the DSA operates in the swept-sine or fast-Fourier-transform (FFT) mode, respectively.¹ The simplest measurement setup uses a 2-channel DSA with source capabilities, such as the HP3563A.

By inspection, the loop gain, as a function of frequency, is $B/E = G_C G_P H$, which is the product of all the blocks around the loop. A direct OL measurement, therefore, can be obtained

by stimulating the loop at the input reference node and taking the ratio of the feedback and error signals, $B(j\omega)/E(j\omega)$.

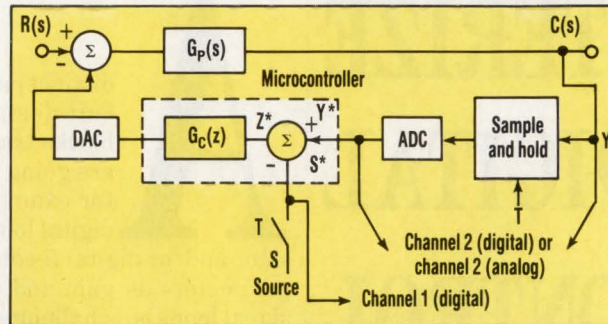
This measurement assumes that reference input R is zero or not connected, allowing the stimulus to be applied at the input summing junction. But this assumption may not be possible in many real-world control systems, such as disk-drive head positioning systems. Disk-drive control loops must be operating during a measurement.

If $R \approx 0$, the designer must create a summing node to inject the excitation signal. The loop model represents this node as a summing junction added to the forward path. For all-analog control loops, the two most common injection schemes are the transformer technique and the op-amp technique. The added summing node can be in either the forward or feedback path, but the designer must exercise great care to ensure that the inserted circuit doesn't alter the control loop's frequency response (see *ELECTRONIC DESIGN*, Nov. 22, 1990, p. 80).

With the new summing junction in place, the designer can characterize the open loop directly by measuring Y and Z (Fig. 1b). From the model,

$$Y = R G_C - G_C H G_P Z \quad (1)$$

In general, R is uncorrelated to the stimulus signal. Consequently, it can be



2. IN A MIXED ANALOG/DIGITAL system, the DSA's digital excitation source (S) is clocked into the loop and summed at the rate of T, which is the update rate of the control system.

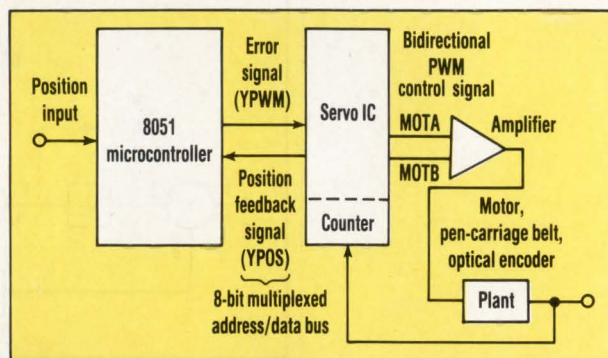
treated as noise and, using averaging, its effect on Y and Z measurements can be greatly reduced. Then, with $R = 0$, the ratio of Y/Z supplies the negative of the loop gain. The problem with this direct measurement is that even after a large number of averages, the resulting OL curve has a non-zero noise bias.

OL response can also be determined by calculating it from a measured CL curve (Y/S). This technique suffers much less from the noise-bias problem. This curve is derived by replacing Z in Equation 1 with $Y - S$ and solving for the CL transfer function Y/S :

$$\frac{Y}{S} = \frac{G_C G_P H}{1 + G_C G_P H} \quad (2)$$

In this calculation, R and S are again assumed to be statistically independent.

Using Equation 2, the designer



3. THE Y-AXIS (PEN) servo loop for a typical drafting plotter includes a microcontroller that reads the feedback signal (YPOS), compares it to the reference input, and creates the error signal (YPWM).

can calculate OL gain:

$$\text{OL gain} = \frac{G_C G_P H}{T/(1-T)} \quad (3)$$

where $T = Y/S$.

Consequently, the designer can easily calculate an OL curve from the measured CL curve by using the DSA's waveform-math capabilities.

MIXED-SIGNAL LOOPS

Many of today's control systems employ both digital and analog loop components. One common example

is a digital control loop in which the error signal is in PWM form and optical incremental encoders serve as feedback sensors. For increased flexibility, other designs implement the compensator in software or with digital hardware, while the remaining system blocks are analog. These mixed-signal designs require ADCs and DACs.

If only the compensator is digital, designers can still use the injection scheme just described to insert an analog stimulus into the loop between the reference junction and the plant. But this scheme will not work if the forward path is also digital. In that case, the designer can use the microprocessor that performs the digital compensation to sum in a digital stimulus (Fig. 2).

To accomplish this, the DSA's source outputs a series of digital words, spaced T seconds apart, that represent a sine or random noise excitation.

The control system's clock ($1/T$ Hz), which is determined by the microprocessor's computation rate, becomes the sampling frequency for the DSA's two channels at Y and Z (or Y and S) as well as the latch signal for the DSA digital source. In this example, the signals at Z and S are digital, whereas Y is available in both digital and analog form. Therefore, for a Y/S closed-loop measurement, the DSA can be set up in an all-digital or a mixed analog-

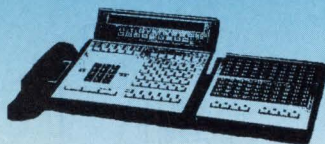
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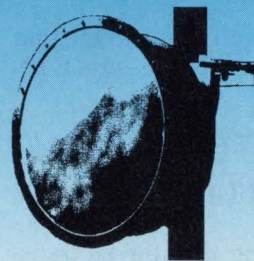
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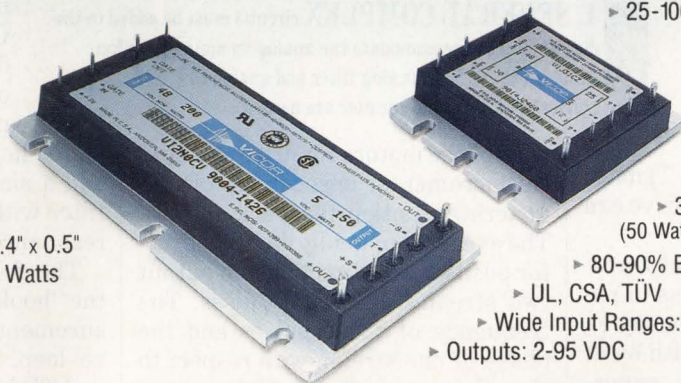


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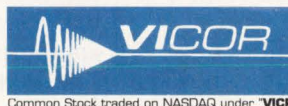
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digital mode.

More insight into this mixed-signal system can be gained by deriving its theoretical OL expression. Because this is a sampled system, its transfer function is in the z domain. So to analyze the system, all blocks must be converted to functions of the continuous frequency variable s in the starred transform. First, $G_C^*(s)$, the starred transform of $G_C(z)$ is found:

$$G_C^*(s) = G_C(z) \Big|_{z=e^{sT}} \quad (4)$$

The DAC is assumed to be a zero-order hold type with the transfer function $(1 - e^{-sT})/s$.

By again using averaging to reduce $R(s)$ to zero, C becomes

$$C = S^*(HG_P) - Y^*(HG_P) \quad (5)$$

where $H(s)$ is $H = [(1 - e^{-sT})/s]G_C^*$

Taking the starred transform of both sides of Equation 5—that is, sampling $C(s)$ to get $C^*(s)$ —gives:

$$C^* = S^*(HG_P)^* - Y^*(HG_P)^* \quad (6)$$

Because $C^* = Y^*$, the closed-loop response Y^*/S^* can be solved:

$$\frac{Y^*}{S^*} = \frac{(HG_P)^*}{1 + (HG_P)^*} \quad (7)$$

By using the DSA's $T/(1 - T)$ math key, HG_P^* for the open-loop curve can be found from Equation 7.

In many systems, the plant transfer function $G_P(s)$ is low-pass in nature and the sampling frequency F_S can exceed the loop bandwidth by at least tenfold. In these cases, $(HG_P)^*(s)$, the sampled version of $H(s)G_P(s)$ doesn't contain alias components and

$$(HG_P)^* = HG_P = [(1 - e^{-sT})/s]G_C^*G_P \quad (8)$$

over the frequency span from 0 to $F_S/2$.

Equation 7 then simplifies to

$$\frac{Y^*}{S^*} = \frac{HG_P}{1 + HG_P} \quad (9)$$

from which the OL gain $H(s)G_P(s)$ can be calculated.

For systems with a high sampling rate, Equation 8 indicates that the effect of the DAC is to add a linear phase shift to the product $G_C^*(s)G_P(s)$ corresponding to a small constant delay of $T/2$.

The example high-speed drafting plotter employs two identical digital servo loops to control the movement and position of the pen carriage and the paper. The servo systems use re-

closed-loop performance, the microcontroller also uses the feedback signal to perform the digital compensation and to estimate velocity.

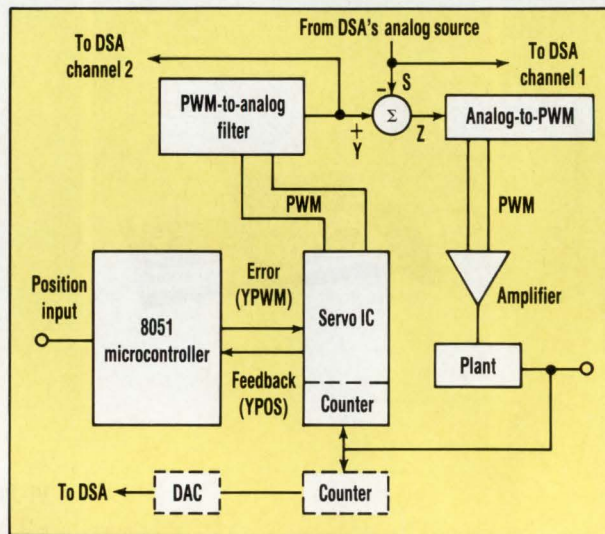
The microcontroller's 8-bit output represents the error between the desired and current position of the appropriate axis (X for paper control and Y for pen control). This output word goes to a custom servo IC that creates PWM signals for each motor. The word's sign bit causes the appropriate output line (MOTA or MOTB) to pulsate, directing the motor to move in the right direction. The word's magnitude sets the width of the pulses on the servo IC's pulsating

output. This width determines the on-time of the half-bridge drivers, thereby creating a path for current flow through the motor.

It turns out that the pen axis is tougher to control in high-speed plotters than the paper axis. This is due to the resonances in the pen carriage-belt system, which can be modeled as a spring-mass system. These resonances are caused by an uncontrolled pen-axis vibration and exhibit themselves as small wiggles when the plotter draws a straight diagonal line at high speed. By using a DSA to measure the OL gain of the servo loop, designers can find these resonances and create a compensation algorithm to eliminate them. A typical solution is to add a simple third-order FIR notch filter with a center frequency at the resonance frequency.

The following examples describe the "hooks" needed to make OL measurements of the plotter's Y-axis servo loop. Both the analog injection and digital summing junction techniques are used. In order to show the resonance in the OL curve, the measurements were made without the "wobble" notch filter.

In the first example, an analog injection setup obtains the Y/S closed loop curve. The OL gain is then calculated from the curve. Because the system has PWM control signals, the



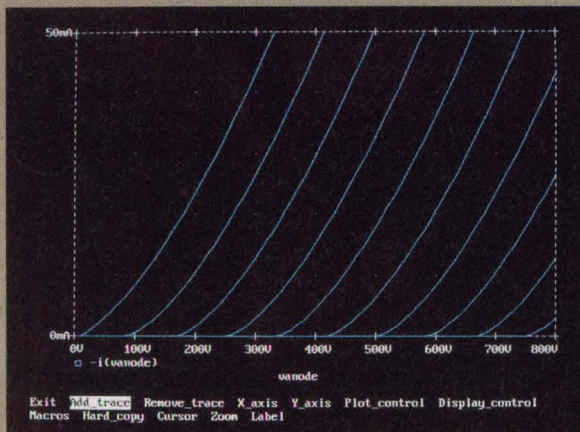
4. SEVERAL COMPLEX circuits must be added to the digital loop to accommodate the analog summing junction. Besides the PWM-to-analog filter and analog-to-PWM converter, a DAC and counter are needed.

versible dc motors for drive and optical incremental encoder circuits to generate position feedback signals. The encoders optically detect the motor position and direction and output two streams of digital pulses. The frequency of these pulses and the phase of one stream with respect to the other convey information about the motor speed and direction.

The pulse stream is fed into an 8-bit up/down binary counter whose contents represent the motor's position (Fig. 3). An Intel 8051 microcontroller periodically reads this position feedback signal and compares it to the reference input to produce an appropriate error signal. To improve



The Standard for Circuit Simulation



I-V curves of a triode vacuum tube

Analog Behavioral Modeling

The Analog Behavioral Modeling option for the PSpice Circuit Analysis package allows you to describe analog components, or entire circuit blocks, using a formula or look-up table. Linear blocks may be described using either a Laplace transform or a frequency response table. Once defined, you can use these blocks in all PSpice analyses, including DC, AC, and transient.

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DIGITAL OPEN-LOOP MEASUREMENTS

measurement setup needs complex circuits in addition to the op-amp summer.

Analysis of the loop reveals that the output of the servo IC, where the control signal is in PWM form, is the only practical place to inject an analog stimulus. Consequently, an analog filter that converts PWM to analog signals is needed in front of the op-amp summer (Fig. 4).

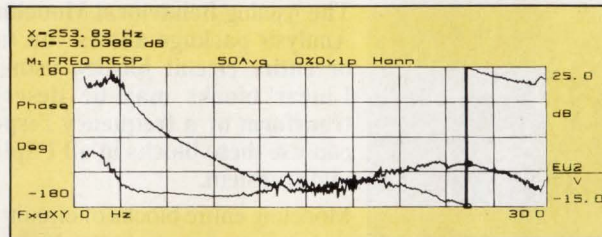
Then the output of the op amp must be converted back to PWM to drive the half-bridge circuits. The bandwidth of these two nonlinear circuits must be large with respect to the loop bandwidth so as not to alter the loop's characteristics.

OTHER ERRORS INTRODUCED

Even with bandwidth considered, the analog injection scheme introduces other sources of errors into the Y/S measurement, such as phase distortion and gain error. The latter results from the difference in units of measurement between the DSA (volt) and the servo loop (pulse width in seconds). The designer must accurately determine the gains of these added circuits, which isn't a simple task. Then the nonlinear gains can be removed from the measurement using the DSA's waveform-math feature. Otherwise, the resulting CL and OL curves' absolute readings will be inaccurate.

However, the OL curve obtained from this analog technique does indicate the cause of the wiggle problem: small resonances at around 260 Hz (Fig. 5). In this case, the OL result was calculated from an averaged Y/S measurement with the DSA in the FFT mode. The result is quite noisy due to the operating mode of the DSA. In this setup, the preferred measurement mode is the swept-sine mode, which offers a better signal-to-noise ratio, although at the expense of longer measurement time.

The difficulties with the



5. THE OPEN-LOOP MAGNITUDE and phase curves calculated from the closed-loop Y/S measurement setup in Figure 4 indicate small resonances at about 260 Hz.

analog injection scheme stem from the fact that it uses the DSA to sample a sampled-data system. A better method is to excite the loop with a digital source. Then the setup can periodically latch two streams of digital words at the nodes of interest into the DSA's two channels. This technique, which is basically how the software summing junction works, is more straightforward and accurate.

A software summing junction typically consists of a few lines of 8051 assembly code. The code reads in a digital word from the DSA source (S), performs a subtraction ($Y - S$), and outputs the result to the loop. Even though the loop characteristics depend on T —the controller's computation rate—the new code segment is short enough that it won't noticeably affect the measurement.

Unlike the analog approach, this

method doesn't restrict the location of the summing node. In fact, designers can sum the stimulus and the operating signal $R(t)$ at the existing reference node. They can also create a node at the input of the routine that does the digital compensation and have the DSA probe the output of that routine. This latter location enables designers to study the transfer function of the digital compensation by itself.

For the example pen controller, half a dozen lines of assembly language create the summing node (Fig. 6). The node is inserted in front of the instruction line that updates the Y-axis PWM error signal (YPWM).

Compared to the analog injection approach, which requires adding several complex circuits, this digital technique adds only an 8-bit latch (Fig. 7). Because the DSA expects the qualifier inputs (that is, address signals) and the data to be present simultaneously, the latch is needed to hold the address information from the microcontroller's multiplexed address/data bus. Of course, systems using processors with separate address and data buses don't need a latch.

Digital summing also offers a significant advantage over the analog approach if the designer wants to probe other nodes in the loop. For example, the designer may be interested in the step response of the Y axis at the feedback node (YPOS). The analog technique would require the addition of a DAC and an up/down binary counter to count the feedback position pulses (Fig. 4, again). Moreover, the antialiasing filter in front of the ADC in most FFT-based analyzers will distort the measured step response. With the digital approach, the designer simply uses the 8051's Read signal as the data clock and qualifies it

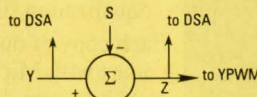
```

CPL      A
INC      A
          ;A contains the Y PWM info

YSUM    EQU      $
MOV      R0,#1000000B ;address of DSA at Y and S
MOVX     @R0,A
          ;I- WRWY (Write to DSA at Y)
MOV      B,A
MOVX     @R0,A
          ;II- Read DSA's Source
CPL      A
INC      A
ADD      A,B
          ;A contains Y-S
MOV      R0,#S_YPWM ;address of Servo IC's Y PWM register and DSA at Z
MOVX     @R0,A
          ;III- WRWZ (Write to DSA & to YPWM)

```

(a)



(b)

6. SEVERAL LINES OF 8051 assembly language code create the digital summing junction for the pen control loop (a). The junction is inserted in front of the instruction line that updates the Y-axis PWM signal (YPWM).

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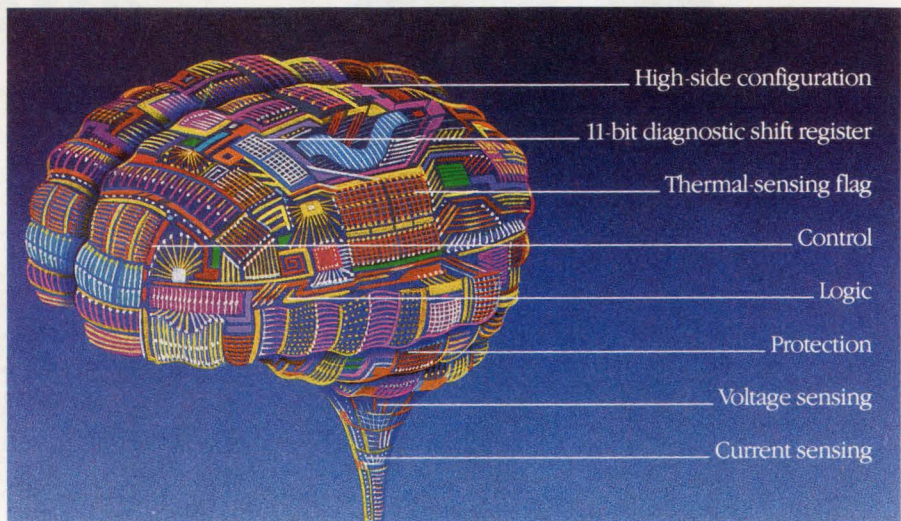
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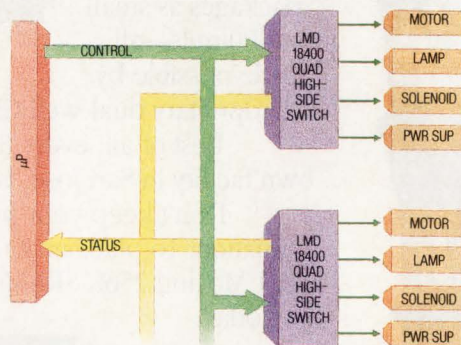
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DIGITAL OPEN-LOOP MEASUREMENTS

when the microcontroller addresses the YPOS port.

With the DSA in the swept-sine mode, the Y-axis OL gain characteristics were measured using both the direct (Y/Z) and calculated (Y/S) methods. Both curves have small peaks around a phase crossover frequency of 260 Hz (Fig. 8). Markers at the gain and phase crossover frequencies display a phase and gain margin of about 34 degrees and -20 dB, respectively.

CLEANER MEASUREMENTS

The measurements in the swept-sine mode are significantly cleaner than those made in the FFT mode (Fig. 5, again). The reason is that the FFT mode's random noise stimulus distributes its energy over a wide bandwidth. On the other hand, the swept-sine stimulus concentrates its power at one discrete frequency, so a better signal-to-noise ratio is obtained without any signal processing. In noisy systems, this is a major advantage.

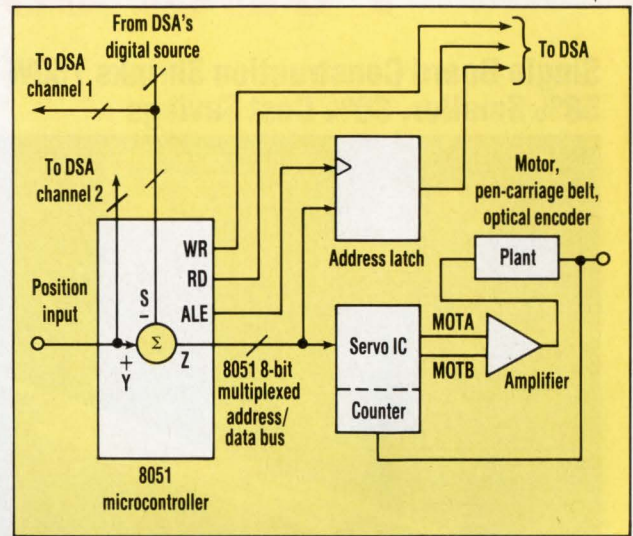
An important consideration in this digital measurement is supplying the DSA with a common clock, which requires a thorough understanding of the system's timing. For the plotter, the 8051 microcontroller reads the Y feedback position information

(YPOS) from the servo IC, processes it, then outputs the YPWM error signal back to the servo IC. The 8051 then repeats the process for the X axis before getting back to Y. This entire cycle results in a servo-loop sampling rate of 1.67 kHz, which is used as the common clock rate for the DSA. This is the rate at which the DSA source updates its output and the analyzer's two channels latch in their data.

It's important to note that although there's one common sampling clock for the DSA, the latching clocks for the source and the two input channels occur at different times. For instance, in a Y/Z measurement using the example setup, the data latching clocks for channel 2 (Y) and channel 1 (Z) occur at lines I and III, respectively (during 8051 Write cycles) (Fig. 6, again). The DSA source is enabled to output the stimulus data onto the 8-bit bus at line II (the 8051 Read cycle). Any one of these three events occurs at a rate of 1.67 kHz and can be used as the DSA's common sampling clock, F_s .

Because events I and III both occur during 8051 Write cycles, the DSA uses a "qualifier" input pod to decode the 8051 address signals. This ensures that the data streams (Y or Z) are routed to the correct channels.

Although designers can select any repetitive signal from the system to be the DSA's sampling clock, they must be wary of introducing processing delays into the measurement. For example, selecting the rising edge of the 8051's Write Y pulse (event I in



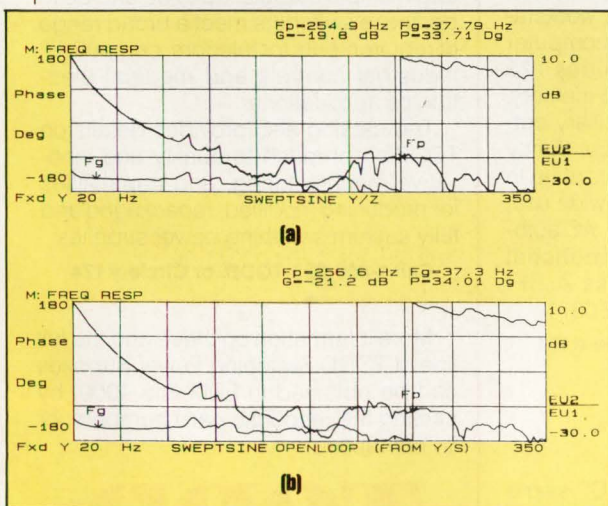
7. THE DIGITAL SUMMING junction is much simpler than the analog version, requiring only an address latch to hold the address information from the microcontroller's multiplexed address/data bus.

the code listing) as the DSA's sampling clock adds a processing delay of $1/F_s$ as seen by DSA channel 1. Consequently, at each sampling point, the DSA associates the data latched in during the previous cycle as the data for that sample. The net effect is that the transfer function result has a positive phase offset. This offset can be removed by entering the known artificial delay into the DSA. Another solution is to select the rising edge of the Write Z or falling edge of the Write Y signal as the sample clock. □

Hoang Nhu is an R&D hardware engineer at Hewlett Packard's Lake Steven Instrument Div. Nhu received his BSEE from California Polytechnic University in Pomona and his MSEE from the University of Washington in Seattle.

Reference:

1. Control system development using dynamic signal analyzers. Hewlett-Packard Application Note 243-2.

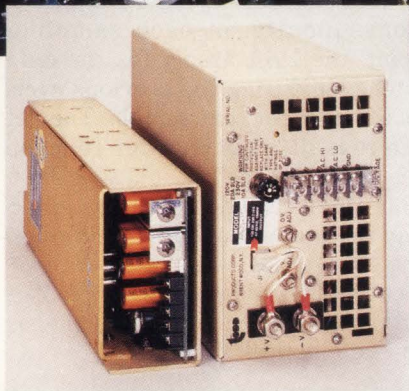
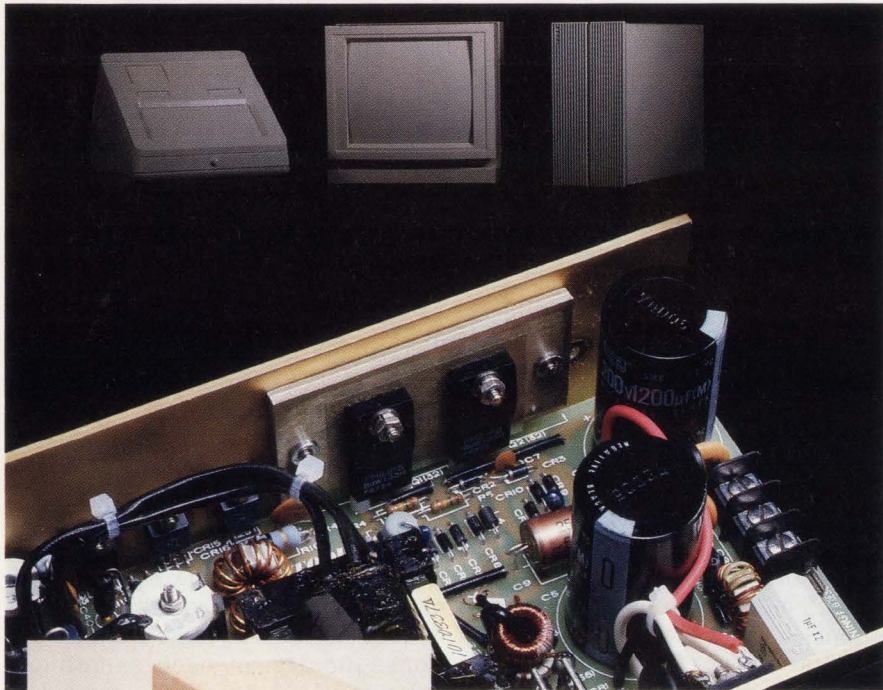


8. THE Y-AXIS open-loop characteristics obtained with the DSA's swept-sine mode are less noisy than those made with the analyzer's FFT mode. The direct measurement (a) and the calculated curves (b) both show small peaks around a phase crossover frequency at 260 Hz.

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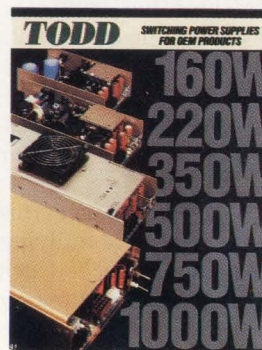
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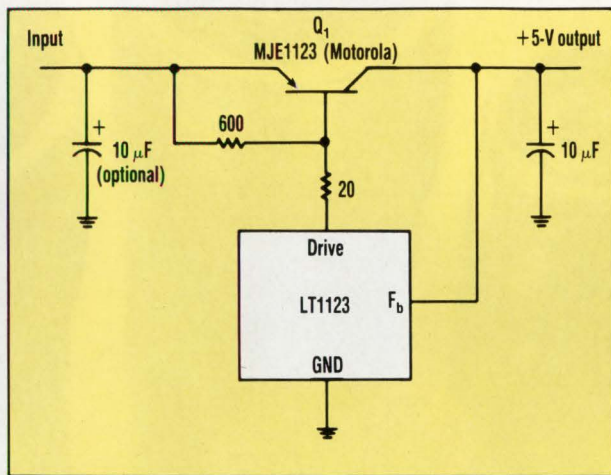
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Switching-regulator post regulators, battery-powered apparatuses, and other applications often require low-dropout linear regulators. Frequently, battery life is significantly affected by the regulator's dropout performance. This simple circuit offers a lower dropout voltage than any available monolithic regulator (Fig. 1). Dropout is below 50 mV at 1 A,

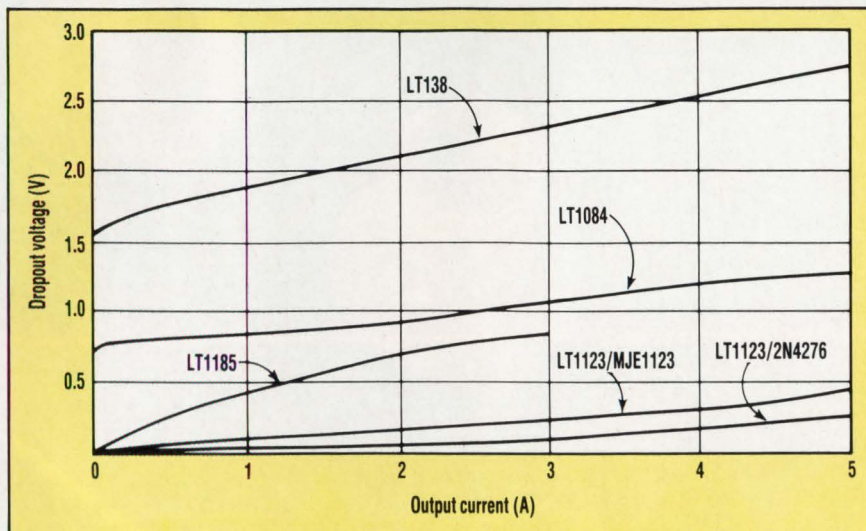
increasing to only 450 mV at 5 A. Line and load regulation are within 5 mV and initial output accuracy is inside 1%. In addition, the regulator is fully short-circuit protected and has a no-load quiescent current of 600 μ A.

The circuit's operation is straightforward. The three-pin LT1123 regulator servo (TO-92 package) controls Q_1 's base to keep its feedback pin (F_b)

at 5 V. The 10- μ F output capacitor supplies frequency compensation. If the circuit is located more than 6 in. from the input source, the optional 10- μ F capacitor should bypass the input.

Configurations of this type normally offer unpredictable short-circuit protection. In this circuit, the MJE1123 transistor is specifically designed for use with the LT1123. Because of this, beta-based current limiting is practical. Excessive output current causes the LT1123 to pull down harder on Q_1 until beta limiting occurs. Under these conditions, the controlled pull-down current combines with Q_1 's beta and safe-operating-area characteristics to supply reliable short-circuit limiting.

Even at 5 A, dropout is about 450 mV, decreasing to just 50 mV at 1 A (Fig. 2). Monolithic regulators can't approach these figures, primarily because monolithic power transistors don't offer Q_1 's combination of high beta and excellent saturation. For comparison, this circuit's dropout is ten times better than 138 other regulators, and significantly better than the other types shown in the plot. Because of Q_1 's high beta, base-drive loss is only 1 to 2% of output current, even at a full 5-A output. This maintains high efficiency under the low $V_{in}-V_{out}$ conditions the circuit will usually encounter. As an exercise, the MJE1123 was replaced with a 2N4276 Germanium device. This combination supplied even lower dropout performance, although current-limit characteristics couldn't be guaranteed. \square



2. THE LT1123/MJE1123 COMBINATION offers a much lower dropout than other regulators—only the LT1123/2N4276 combination is better. However, current-limit characteristics can't be guaranteed for that regulator pair.

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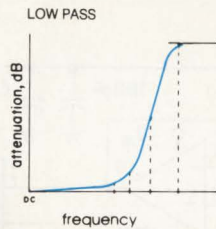
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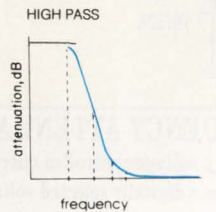
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PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
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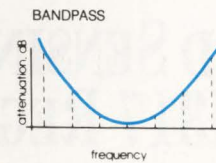
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PHP-600	600	1600	545	440	350	2.0	17	14.95
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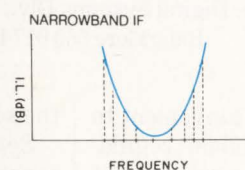
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F132-2 REV. ORIG.

CIRCLE 522 CONTROL RF SIGNALS DIGITALLY

MICHAEL A. WYATT

SSO Honeywell Inc., Clearwater, FL 34624; (813) 539-5653.

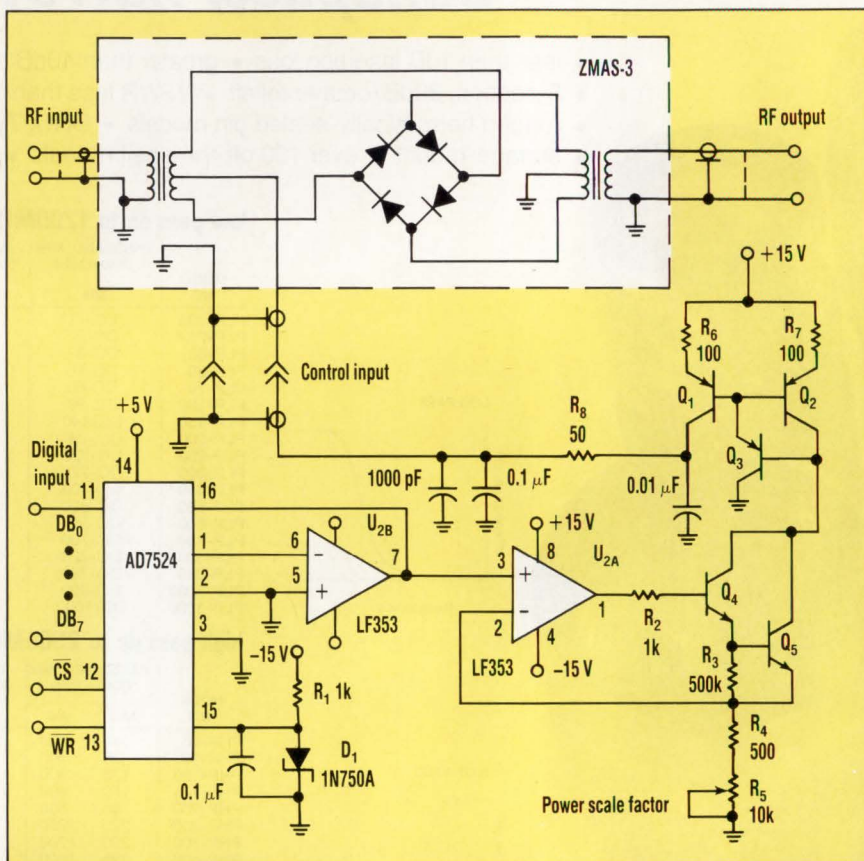
high and the attenuation needed. This can be used in a lookup table or curve-fit to an equation. If a greater attenuation range is required, the attenuator sections should be cascaded and a dual DAC, such as the AD7528, should be used. □

By combining a balanced mixer, voltage-controlled current source, and a digital-to-analog converter, a digitally controlled radio-frequency attenuator can be produced (see the figure). The mixer (ZMAS-3), specifically designed for attenuator operation, acts as a current-controlled transmission gate between the RF input and output ports. Current enters the control input and forward biases the quad diode array within the mixer. Because the diodes' conductance is proportional to forward current, the transmission of RF energy from the RF input to the output flows through the diode array and is thus controlled by the diode array's forward current. The mixer's control range is over 40 dB within a frequency range of 1 to 200 MHz. Other ranges are available from its manufacturer, Mini-Circuits, Brooklyn, N.Y.

Transistors Q_{1-5} , along with op amp U_{2A} , form a voltage-controlled current source. These transistors can be any general-purpose devices, such as 2N3904s, 2N3906s, or part of an array, such as the CA3096. Potentiometer R_5 sets the attenuator's scale factor by establishing the voltage-to-current transfer ratio.

The AD7524 8-bit DAC from Analog Devices, Norwood, Mass., supplies the overall digital control by producing a digitally selected voltage that drives the voltage-controlled current source. The digital input is an 8-bit word that uses \overline{CS} and \overline{WR} to latch the data into the DAC.

To calibrate, R_5 is adjusted with the DAC at its maximum value (all bits high) to establish the minimum attenuation. Then, the DAC is set to its minimum value (all bits low) to establish the maximum attenuation. The difference between the maximum and minimum attenuation is the attenuator's control range. Each DAC bit can now be sequentially set



THIS RADIO-FREQUENCY ATTENUATOR, which is digitally controlled, combines a balanced mixer, a voltage-controlled current source, and a digital-to-analog converter. The DAC produces a digitally selected voltage that drives the current source. R_5 sets the attenuator's scale factor.

CIRCLE 523 ADD SENSING TO LM317 REGULATOR

M. S. NAGARAJ

ISRO Satellite Centre, Digital Systems Div., Airport Rd., Vimanapura P.O., Bangalore 560 017 India.

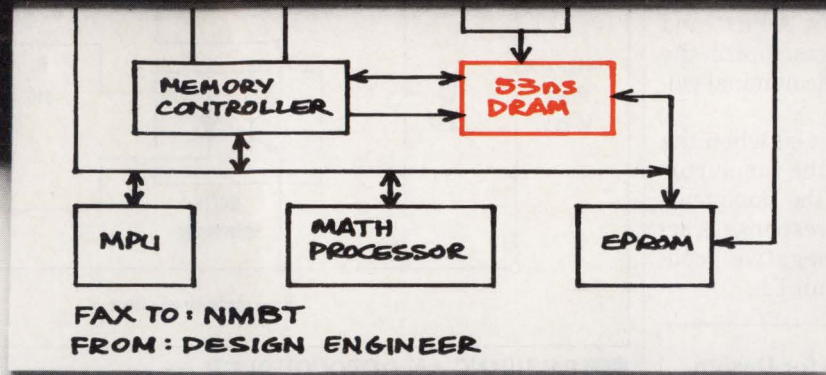
Though they're convenient to use, three-terminal regulators can't sense and correct for a voltage drop across the conductors carrying the load current. An optocoupler helps perform

the sense function (see the figure).

Setting R_1 to 240 Ω causes a 5-mA constant current to flow through the optocoupler's transistor. R_3 is adjusted to achieve the desired 12 V across the load. A voltage drop

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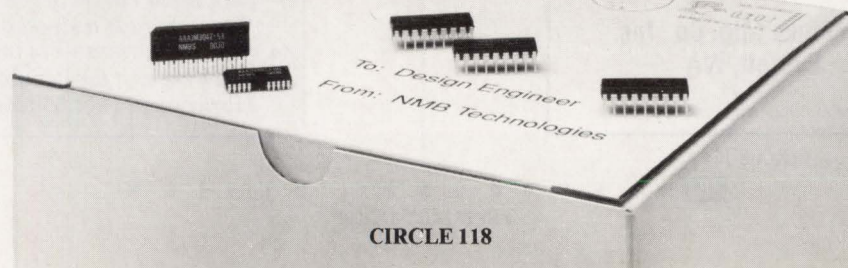
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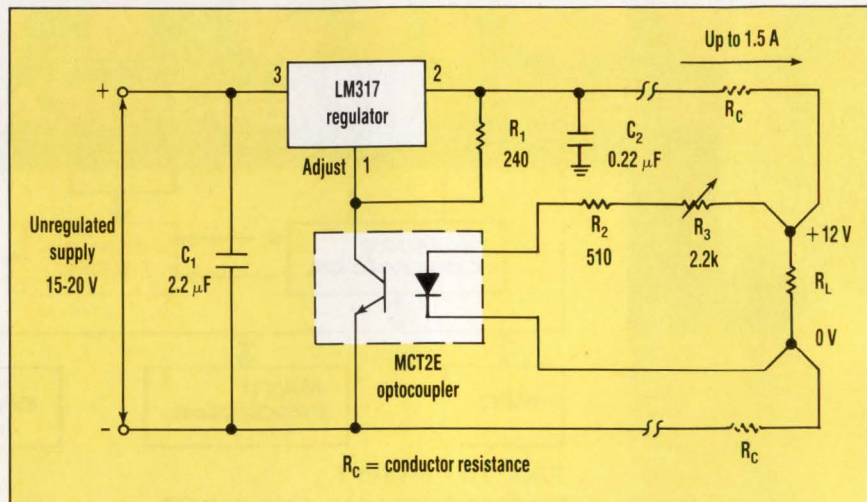
IDEAS FOR DESIGN

across the load caused by a larger drop in the conducting path lowers the current through the optocoupler's light-emitting diode. This action drives the transistor toward its "off" state and increases its V_{CE} . Hence, the regulator's Adjust and output voltages increase until the load voltage reaches the nominal value of 12 V.

The process is reversed when the voltage drop across the conductor decreases. Note that the nonlinearity in the optocoupler response is accounted for by the negative feedback built into the circuit. □

Send in Your Ideas for Design

Address your Ideas-for-Design submissions to Richard Nass, Ideas-for-Design Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604.



BY USING AN OPTOCOUPLER with a three-terminal regulator, this circuit corrects for voltage drops across the conductors carrying the load current. When the load voltage falls due to an increased I_R drop through the conductors, the current through the optocoupler's light-emitting diode is reduced, driving the transistor toward cutoff and increasing its V_{CE} voltage. This raises the LM317's Adjust voltage, which keeps the load voltage steady at 12 V. Should the I_R drop across the conductors decrease, the opposite action takes place.

Advertisement



PENTON'S VIDEO LIBRARY



How To Choose A Digital Storage Oscilloscope

Many of the questions most often asked about DSOs are answered in this 26-minute video. The video serves as a valuable DSO performance tutorial, while introducing the company's line of medium and high-frequency DSOs. You'll learn how DSOs use digital sampling to capture a wide variety of signals—both single-shot and repetitive, and also how the combination of signal acquisition power and measurement/analysis facilities extract out hidden details. The presentation is divided into two parts. The first covers signal acquisition and digital sampling techniques, while the second illustrates the powerful signal analysis capabilities of DSOs. **Free Video**

John Fluke Mfg. Co., Inc.
Everett, WA

CIRCLE 154

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Here's one reason that over half of all SCSI devices sold are NCR.

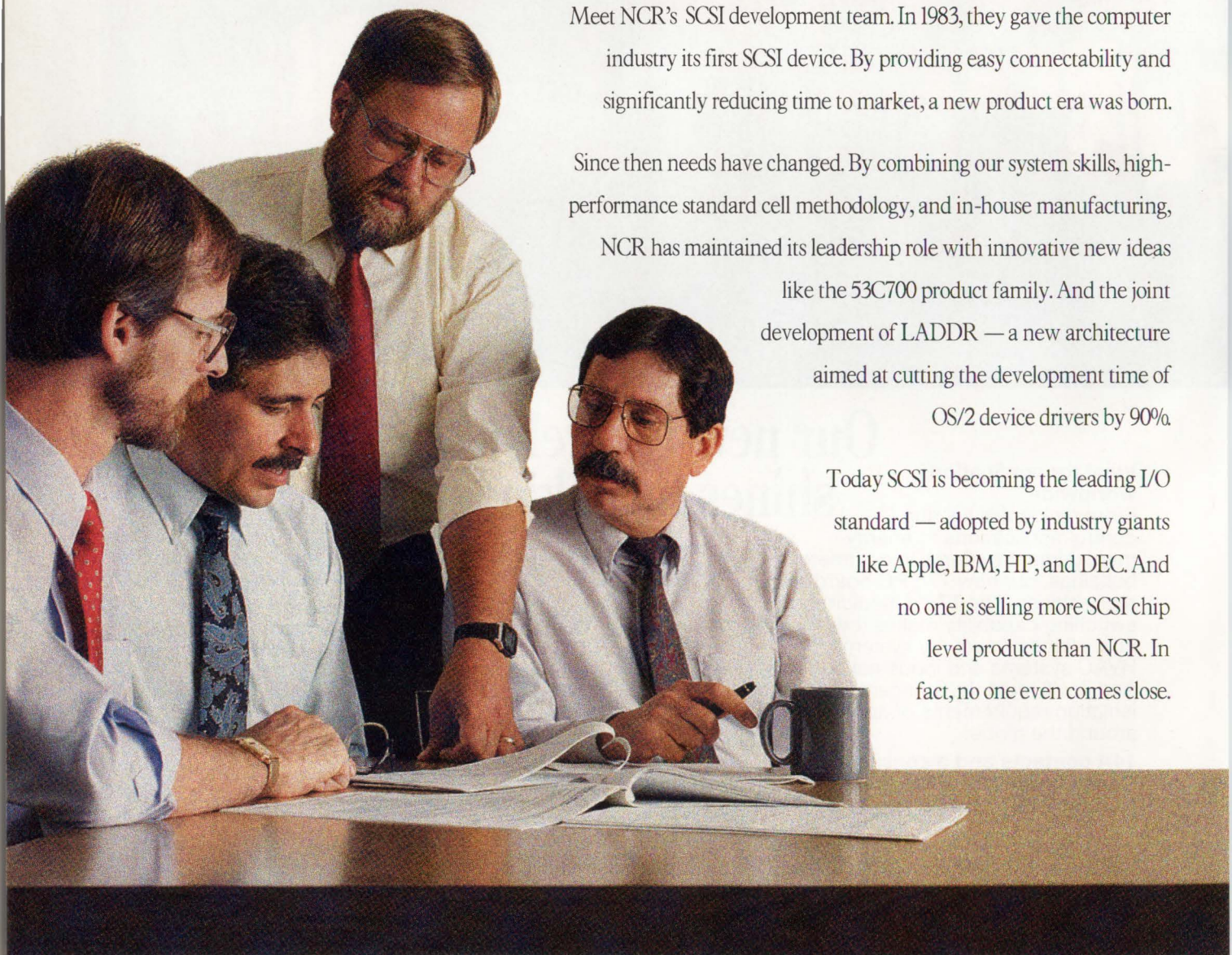
We created the market... and we still lead the way.

Meet NCR's SCSI development team. In 1983, they gave the computer industry its first SCSI device. By providing easy connectability and significantly reducing time to market, a new product era was born.

Since then needs have changed. By combining our system skills, high-performance standard cell methodology, and in-house manufacturing, NCR has maintained its leadership role with innovative new ideas

like the 53C700 product family. And the joint development of LADDR — a new architecture aimed at cutting the development time of OS/2 device drivers by 90%.

Today SCSI is becoming the leading I/O standard — adopted by industry giants like Apple, IBM, HP, and DEC. And no one is selling more SCSI chip level products than NCR. In fact, no one even comes close.



Part of the NCR SCSI Development Team: (left to right)
Jerry Armstrong, Sr. Software Engineer; **Harry Mason**, Strategic Marketing Manager; **John Lohmeyer**, NCR Sr. Consulting Engineer and Chairman of the ANSI X3T9.2 Committee and **Dave Skinner**, SCSI Product Manager.



North American Sales Headquarters
1731 Technology Drive, Suite 600
San Jose, CA 95110
(408) 453-0303

Here's another.

The NCR 53C700 SCSI I/O Processor...
So good, *Electronic Design* named it the
product of the year.

"You can't tell a good SCSI chip just by looking at it..." and according to *Electronic Design*, NCR's 53C700 is the best there is.

The only third generation SCSI device on the market today, it concentrates all the functions of an intelligent SCSI adapter board on a single, smart and extremely fast, chip... for about 15% of the cost.

As the first SCSI I/O processor on a chip, the 53C700 allows your CPU to work at maximum speed while initiating I/O operations up to thousands of times faster than any non-intelligent host adapter. DMA controllers can burst data at speeds of up to 50 Mbytes/s. This new chip cuts down system time hookup to a fraction of what it has been.

Those are just a few of the reasons *Electronic Design's* "Best of the Digital IC's" award went to NCR's 53C700 last year.

And now the NCR 53C710!

For the complete story on the NCR SCSI product line featuring the new 53C710, as well as the upcoming SCSI seminars with the NCR SCSI Development Team, please call:

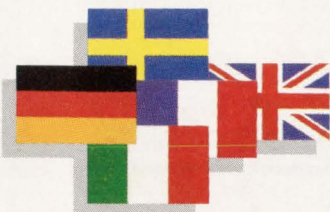
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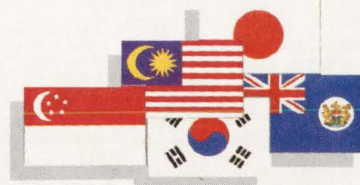
NCR

Creating value

CIRCLE 140

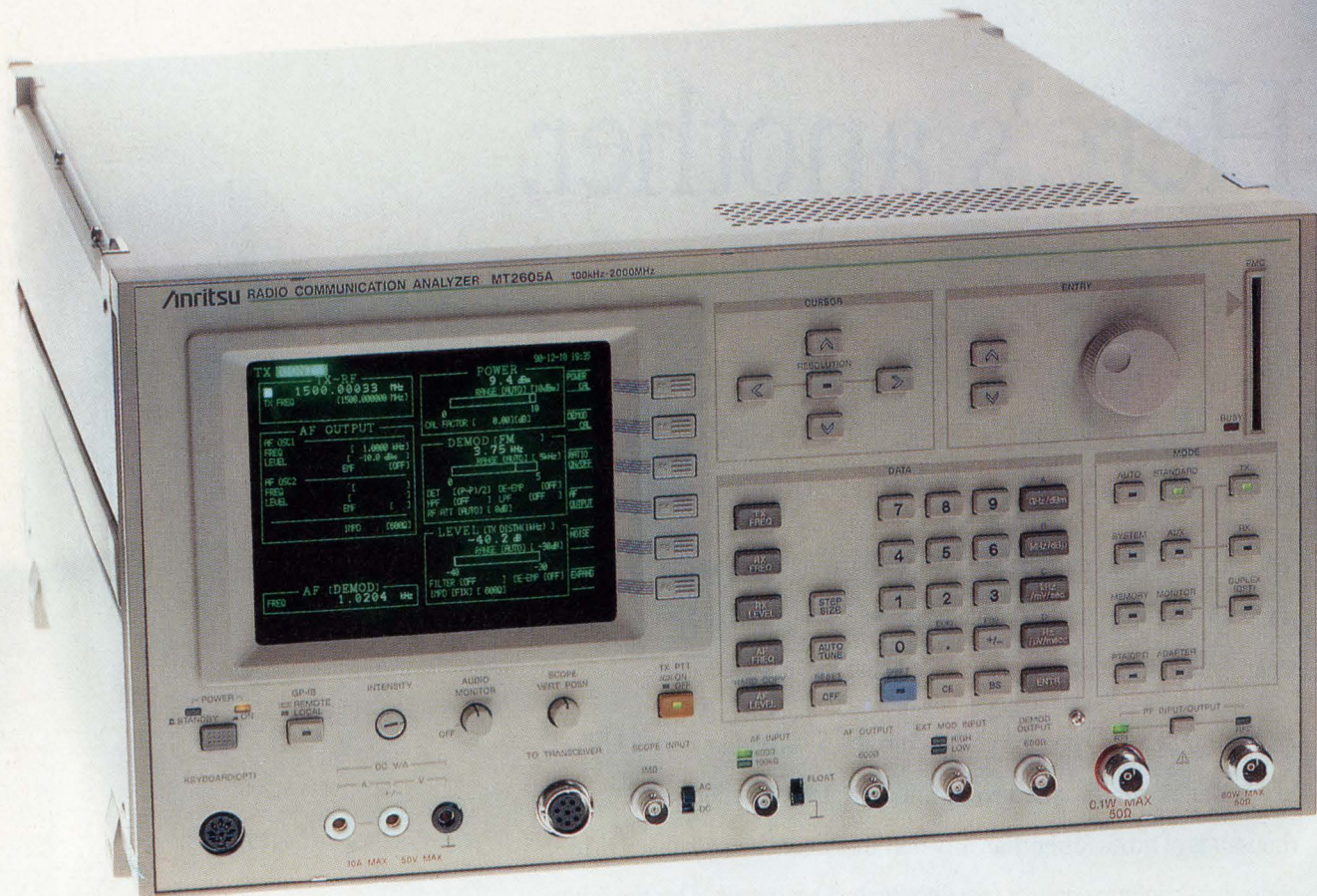


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Greater Range and Total Ability 100kHz to 2GHz



Anritsu's new MT2605A Radio Communication Analyzer is all you need for comprehensive radio testing. This single instrument can perform 14 separate tests in just 2 minutes. Plus, it covers the wide range from HF and VHF to UHF, and up to quasi-microwave spectra.

In fact, it's like 10 pieces of equipment in one.

The MT2605A is a signal generator, AF generator, frequency counter, power meter, modulation meter, AF

Features

- Frequency range: 100kHz to 2GHz
- Digital system testing:
 - Burst measurement
 - Bit error measurement (option)
 - Digital modulation measurement (separate unit)
- Accurate, high-stability signal generator
 - Setting resolution: 10Hz (available for narrow band systems)
 - Signal stability: $\leq 2 \times 10^{-8}$ per day

level meter, distortion meter, oscilloscope, DC voltmeter and DC ammeter, all in one easy-to-use instrument.

Digital test capabilities include burst measurement.

In addition, the Personal Test Automation (PTA) software option even allows users to create custom test programs and store them on convenient Plug-in Memory Cards (PMC).

Anritsu

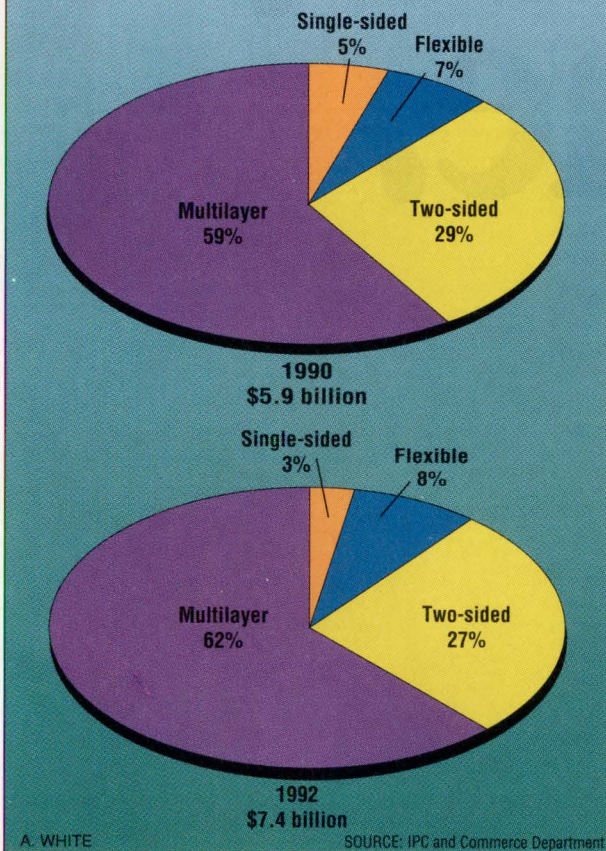
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ELECTRONIC DESIGN

QUICK LOOK

EDITED BY SHERRIE VAN TYLE

PC BOARDS SHOW STEADY GROWTH



MARKET FACTS

With electronics at the heart of more and more equipment and vehicles, the market for manufacturing pc boards is burgeoning. The U. S. market is expected to grow from \$5.9 billion last year to \$7.4 billion in 1992. The compound annual growth rate is expected to be about 6.3%. The growth picture has several clouds on the horizon, though.

For one thing, in economic downturns demand for electronic systems slackens and sales of pc boards decline. For another, the fragmented pc-board industry is undergoing consolidation. There were 200 pc-board outfits in the U. S. in 1989, compared with 2000 five years ago.

The biggest market segment is that for advanced boards of 6 to 22 layers and 3 to 8-mil lines. These boards go into computers and peripherals, telecommunication products, along with military and aerospace equipment. The next biggest sector is that for simple boards, a segment that amounted to \$2 billion in revenues last year. Mostly for consumer products, these boards have two to six layers and 8- to 12-mil lines. Last year, flexible boards made up the smallest slice of the board market, with sales of \$400 million.

Manufacturers of pc boards are divided into captives (operated by original equipment manufacturers) and independents, which supply OEMs that lack in-house manufacturing.

As pc-board designs call for lines/spaces of under 5 mils, manufacturers are turning to new ways to make the inner board layers. Also pressing pc board makers are the demands of surface mounting. SMT, delayed in the U. S. by lack of standards and lack of components, seems finally to be catching on. SMT is expected to snare two-thirds of the IC packaging market by 1994, according to Electronic Trend Publications, a Saratoga, Calif., market research company. Designers working with SMT boards have to deal with blind or buried vias, smaller line widths, and components on both sides of the board.

1-MINUTE OPINIONS

What do you think about the education that young engineers are getting these days?

I find it truly amazing that many people these days want more humanities courses included in the curriculum of engineering programs. Young prospective engineers need more technical, mathematical, and specialization courses so that they can compete in the highly competitive and technical job market. Employers are not interested in your extensive knowledge of history and art and your ethics, which have been molded from day one by your upbringing.

The idea of well-rounded is more suited to the pocketbooks of college administrators, who set fees of \$500 to \$1,000 per three-credit course, than to students. **Richard Sellars, Middletown, Conn.**

The education of any individual must be well-rounded. All people who attend institutions of higher learning should be exposed to not only the humanities but also to the technologies. I have respect for

graduates in all fields because I took classes in the various branches of knowledge available. I see that the stream does not flow in both directions. People who study in other branches of knowledge seldom understand even the most elemental scientific or technological fundamentals. Yet there is a large body of them that tells us that we must understand what they are doing and why.

The education of every person must also include science and engineering. Five years is too long to expect someone to stay in school who will emerge in an ill-respected profession where you can be thrown out of work on the whim of Congress or a market glitch. **David Lieby, Boulder Creek, Calif.**

What's your opinion on the education of today's young engineers? Mail your responses to Electronic Design, Reader Opinions, 611 Route 46 West, Hasbrouck Heights, NJ 07604 or fax them to (201) 393-0637.

Memory lane.



Faint, illegible text in the bottom left corner, possibly bleed-through from the reverse side of the page.

Faint, illegible text in the bottom right corner, possibly bleed-through from the reverse side of the page.

Introducing the complete line of non-volatile memories from Fujitsu.

Talk about fond memories. With Fujitsu's full line of CMOS and bipolar non-volatile memories, you've got a choice that includes ROMs, EPROMs, EEPROMs and PROMs. Plus all the packaging options you can think of. Now that's worth remembering.

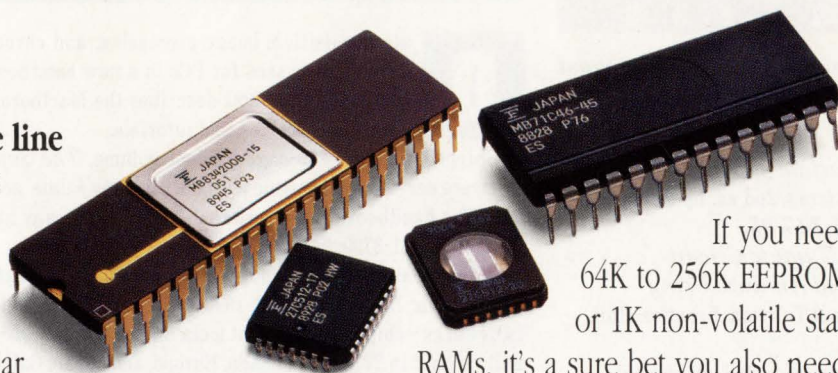
Take our low-power CMOS ROMs, for example. You get densities up to 16Mbits. Plus we're also developing a very high-density 32Mbit device.

But density alone isn't enough. Which is why our ROMs also come in both standard and high-speed versions as fast as 150ns. With blazingly fast 100ns devices just around the corner.

When it comes to EPROMs, we've got the broadest selection in the industry. With densities ranging from 64K to 4Mbits. And speeds up to 150ns.

But the future is always faster. Which is why our 1Mbit device will soon operate at speeds of 55ns and 100ns.

What's more, our 1Mbit and 4Mbit devices are available in x8 and x16 configurations for your most advanced applications.



If you need 64K to 256K EEPROMs, or 1K non-volatile static RAMs, it's a sure bet you also need reliability. Which makes Fujitsu the one supplier to always keep in mind.

We've utilized thin-oxide and CMOS technologies in our entire EEPROM product line to provide you with the highest quality and reliability.

Just take a look at the numbers. A failure rate of less than .0004% per 1000 hours. And erase/write cycles of 10,000 minimum and over 100,000 typical. That's reliability.

As for PROMs, it's no secret that Fujitsu devices range from 256 bits to 128K. But now our PROMs are even better. Because our unique new BiCMOS technology increases speed and densities and lowers power consumption.

Both the 128K device, which clocks in at 35ns, and our soon-to-be-announced 256K device, which will run at 25ns, are the fastest PROMs on the market in these densities.

All in all, when it comes to non-volatile memories, only Fujitsu gives you the choice.

If you'd like to know more, call 1-800-642-7616. And take a stroll down memory lane.

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QUICKLOOK

OFFERS YOU CAN'T REFUSE

BEST SELLERS

Which technical books are the most popular in Silicon Valley?

ELECTRONICS:

1. *Noise Reduction Techniques in Electronic Systems*, 2nd ed. by Henry W. Ott. Wiley, 1988. **\$47.95.**
2. *SPICE: A Guide to Circuit Simulation and Analysis Using PSPICE* by Paul Tuinega. Prentice-Hall, 1988. **\$20.60**
3. *Art of Electronics*, 2nd ed. by Paul Horowitz and Winfield Hill. Cambridge University Press, 1989. **\$49.50.**
4. *Microchip Fabrication*, 2nd ed. by Peter Van Zant. McGraw-Hill, 1990. **\$49.50.**
5. *Radargrammetric Image Processing* by Franz W. Leberl, Artech House, 1990. **\$88.**

COMPUTER SCIENCE:

1. *Object-oriented Design with Applications* by Grady Booch. Addison Wesley, 1990. **\$37.25.**
2. *Postscript Language Reference Manual*, 2nd ed. Adobe Systems Inc. Addison-Wesley, 1990. **\$28.95.**
3. *Object-oriented Analysis*, 2nd ed., Peter Coad and Edward Yourdon. Prentice-Hall, 1990. **\$31.**
4. *Computer Architecture: A Quantitative Approach* by John Hennessy and David Patterson. Morgan Kaufman, 1990. **\$54.95.**
5. *The Age of Intelligent Machines* by Raymond Kurzweil. MIT Press, 1990. **\$29.95.**

This list is compiled for *Electronic Design* by Stacey's Bookstore, 219 University Ave., Palo Alto, CA 94301; phone (415) 326-0681; fax (415) 326-0693.

HOT PC PRODUCTS

An interactive command shell for Apple's Macintosh gives users the ease of windowing as well as the directness of DOS and Unix command lines. Envyre, from Appropriate Solutions, enables users to manage directories, view source code, and view hexadecimal listings of object files.

Envyre allows users to move among DOS, Unix, and Macintosh environments. It also supports any printer that connects to the Mac. The program lists for \$99.95. Contact Appropriate Solutions, P.O. Box 458, Peterborough, NH 03458; (603) 924-6079.

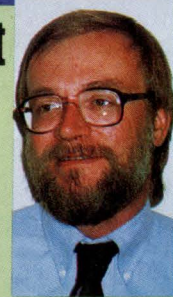
Data-acquisition, image-processing, and chromatography products are among the devices discussed for PCs in a new handbook. Data Translation's *New Product Handbook* for 1991 describes the Marlboro, Mass., company's 300 products with data sheets, tables, and tutorials.

Shipped with the 275-page product volume, *The Source Handbook* lists hardware and software services compatible with the company's data-acquisition and image-processing products. The handbooks can be ordered from the company at 100 Locke Dr., Marlboro, MA 01752-1192; (508) 481-3700; fax (508) 481-8620.

A free seminar is being offered on designing with Echelon Corp.'s LON control technology [*Electronic Design*, Dec. 13, 1990, p. 139]. Topics include intelligent distributed control, the LONworks—chips, development tools, and hardware aids—and application examples. Seminars will be held in 27 states, Canada, Europe, and Japan. Call (800) 258-4LON.

K M E T S K O R N E R

...Perspectives on Time-to-Market



BY RON KMETOVICZ

President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458

While doing too little planning is somewhat of a problem, doing too much is often the offsetting error made by many new-product-development teams and their managers. It turns into planning and replanning and planning and... The cycle never lets the planning phase end and the execution phase begin. It can be an indication that the planning process needs to be improved. Or it can forecast serious problems with the stability of the definition that is driving the plan.

In either case, an understanding of the problem must be reached and the cause eliminated. It's usually easy to determine if a changing definition is at the heart of the problem by asking those involved in the continuous planning process for their feedback. Besides this action, reviewing the external reference specification (ERS) revision log will help develop added insight. The mere fact that the planning phase can expose such a serious fundamental problem is reason enough to take the planning activity very seriously. Clearly, the only right action to take is one that will stabilize the definition to allow for the planning phase to be completed successfully.

Problems with the planning process itself are the other major contributing factors to this problem. Most of the time the problems can be grouped into technique and tools categories. From the technique perspective, the most frequently made error is that of trying to accomplish all planning activities through a "super planner." This individual tries to do it all. No shared and distributed planning techniques to worry about here. All plans are done by one person. Do you think that those who have their work planned for them really care about what's in the computer system?

A second pitfall to avoid is placing too much detail into the project's master plan. It is necessary to have individuals manage their own work affairs while providing summary task information at the project level. Where possible, individuals should be encouraged to generate task information that is two to four weeks in duration for tracking at the project level. It is assumed that individuals will maintain detail with greater resolution at the local level.

Third, individuals need to understand fundamental planning concepts. If your work group knows how to produce a hierarchical decomposition of a project, a milestone sequence, a task list, task-duration estimates, task resource assignments, and task networks, then you have the basic planning skills in place. If not, you should give consideration to developing these skills in a timely fashion. Problems with tools are usually associated with software, hardware, and utilization techniques that cannot move at the speed of the project. We'll look at this topic in the next column.

QUICKLOOK

TIPS ON INVESTING

If you choose to roll over your CDs, you may wish to shop around, comparing CD rates at local banks and savings and loans. Another way to obtain CD rates is through financial services firms. These firms search the country for the highest rates available from banks and savings and loans and, in turn, "broker" them to their clients. The interest rates to investors are usually higher than those the local banks are offering and, best of all, some firms offer these fully insured, higher yield bank CDs without charging you a commission.

You may also consider other fixed-income investments that offer higher rates of return than CDs. The diverse fixed-income markets offer a potentially confusing array of investment alternatives. However, although interest rates have declined in recent months, income, safety and liquidity remain paramount. You must understand the difference between each of the products. For example, CDs are federally guaranteed and offer a fixed rate of return whereas with other fixed-income products both principal and yield may fluctuate with changes in market conditions.

If you are an income-oriented investor, consider the following alternatives:

•Government securities. United States Treasury issues—bills, notes, and bonds—are the safest securities available: They are backed by the full faith and credit of the U. S. government. They range in maturities from three months to 30 years and have a large secondary market (exchanges and over-the-counter markets where securities are bought and sold subsequent to original issuance) which offers engineers a high degree of liquidity. Income from Treasuries is also exempt from state and local taxes.

If you are a traditional Treasury security buyer, you should also consider investing in government agency bonds. They offer higher yields than Treasuries without sacrificing quality. Issued by various agencies of the U. S. government, they are not direct obligations of the government. But they are considered "moral obligations" and their quality is considered second only to that of direct U. S. Treasury instruments. Treasuries are subject to market fluctuations.

•Collateralized mortgage obligations. CMOs offer superior quality as well as yields that surpass those of Treasury and agency

securities. CMOs are backed by pools of mortgages and principal and interest from these underlying mortgages are passed through from the homeowners to the CMO investor. Since CMOs are collateralized by mortgages, they are usually rated AAA by Standard and Poor's. (Moody's Investors Service and Standard and Poor's are investment services that classify securities according to risk.)

•Corporate bonds. The corporate bond market offers an unparalleled diversity of ratings, quality, maturities, and coupons (income). Besides investment-grade bonds (rated Baa or better by Moody's and BBB by Standard and Poor's), high-yield securities are available for investors willing to take on the additional risk commensurate with a higher yield.

•Tax-free municipal bonds. My most often recommended investment for engineers looking for higher after-tax income is municipal bonds. Income from municipal bonds is exempt from federal taxes, and if you are a resident of the state of the issuer, income is also exempt from state and local taxes. Municipal bonds may be subject to state or local taxes or alternate minimum tax, however. An abundance of new tax-free issues has managed to keep yields in the municipal bond marketplace at relatively high levels. As a result, municipal bonds offer the individual investor an attractive opportunity.

You can also participate in the fixed-income markets in ways other than through direct investment. Consider mutual funds and unit investment trusts. By investing in a mutual fund, you can choose from a portfolio of government securities, corporate bonds or tax-advantaged municipal bonds, among others. You benefit from the expertise of professional portfolio managers who select and monitor a variety of securities, diversified by coupon rate and maturity.

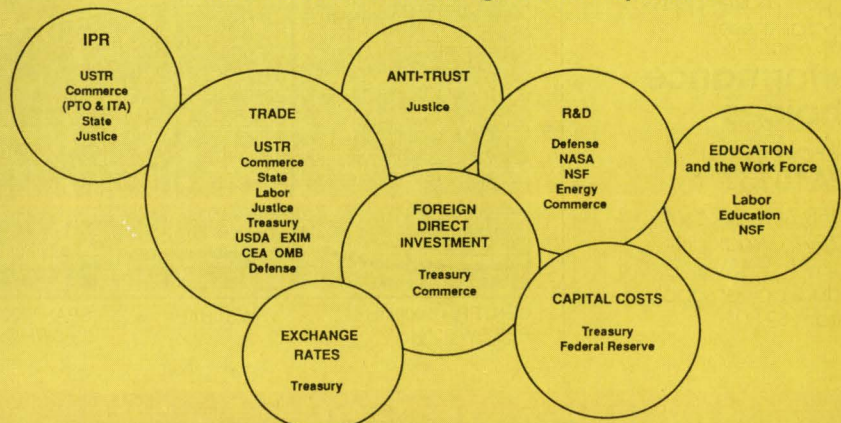
A unit investment trust (UIT) is a fixed portfolio of securities. Fixed-income UITs provide monthly income and are one of the most convenient ways to own bonds.

Henry Wiesel is financial consultant with Shearson Lehman Brothers, 1040 Broad St., Shrewsbury, NJ 07702; (800) 631-2221 (U. S.) or (800) 221-0073 (N. J.) He is also a qualified pension coordinator. Wiesel invites questions and comments, which should be addressed to him c/o the news editor.

EYECATCHER

When agencies and issues overlap: A chart from the U. S. Commerce Department's International Trade Administration shows the many issues facing the electronics industry and the various federal agencies responsible. Areas that once were distinct now are intertwined. More coordination of policies is needed, says the ITA. The chart appears in the ITA's report *The Competitive Status of the U. S. Electronics Sector*. (IPR: intellectual property rights.)

Competitiveness Issues and U.S. Government Agencies Responsible



Source: U. S. Commerce Department, Science & Electronics

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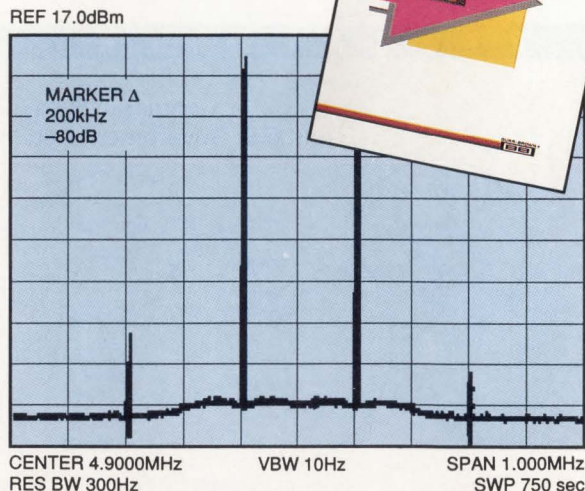
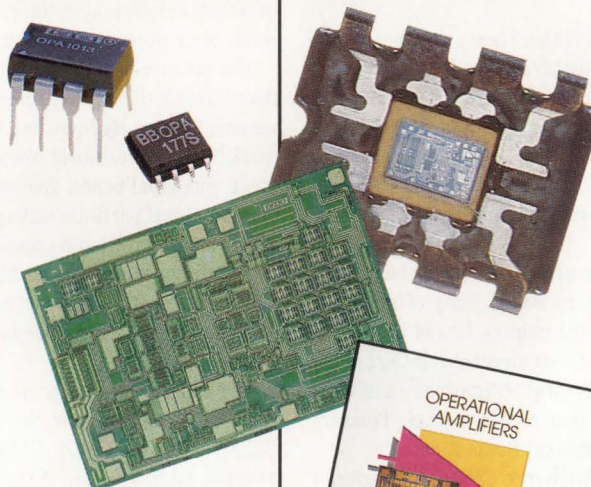
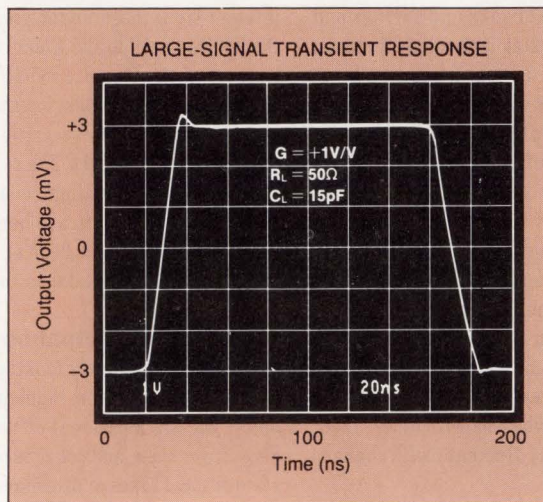
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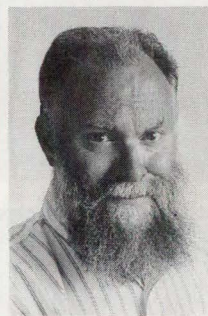
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BB

WHAT'S ALL THIS TEFLON STUFF, ANYHOW?

Once upon a time, a long time ago, a friend of mine, Arnie Liberman, designed a really good operational amplifier with a very low bias current—less than 0.1 pA. Now, when you want to measure and test a current as small as that, you don't just measure the $I \times R$ drop across a resistor, because even with a 100,000-M Ω resistor, it's hard to get resolution or accuracy. (0.1 picoamperes \times 100 kM Ω = just 10 mV). So Arnie set up a test with an integrator. If this amplifier had an output drift rate (or ramp rate) of 5 mV/s with a feedback capacitor of 10 pF, that would prove that the amplifier's input current was 5 milli \times 10 pico, or 50 femtoamperes.



BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

But you can't just run an integrator without resetting it occasionally. And Arnie knew you could not easily find a relay that would short out the feedback capacitor without introducing lots of leakage and a bad jump when you turned off the drive to the relay's coil. So he made up a "relay" by applying a lever to a long push-rod which reached into the sealed box where the test was going on. The push-rod would close the contacts and short out the capacitor. Then when you backed off on the push-rod, the integrator would integrate the current, and all you have to do is measure the output's dV/dt to tell if the input current was within spec. And this worked fine, even at the level of

small femtoamperes.

It worked fine in 1971...it worked okay in 1972...it worked in 1973. But after you started the test, you had to wait many seconds for the output dV/dt to stabilize to the point where you could get the right answer. Later, in 1973, you had to wait almost a minute to get the right answer.

In 1974, when you had to wait 3 or 4 minutes to get any valid reading, somebody in Production Test finally complained to Arnie that you couldn't get very many units tested in a day. So Arnie went to troubleshoot the test fixture. And he was puzzled for a while. What could cause such an erroneous reading? Soon, he realized that the push-rod was the culprit. If you pushed it back and forth, just a tiny bit, the integrator went berserk. But how could that be? The push-rod was made of Teflon. And it slid in Teflon bushings. How could there be a big error caused by the push-rod?

But as it turned out, that was indeed *exactly* the problem. When the push-rod slid in its bushing, it generated thousands and thousands of volts of static electricity. Now, on most ordinary insulators, those charges would drain off shortly. But because Teflon is such a good insulator, the charges would bleed off over a long, *long* time (through the air). Some of this charge would go into the summing point of the amplifier—for many seconds.

As the Teflon got drier with time, the time constant got longer and longer until he had to fix it. Arnie replaced the Teflon push-rod and Teflon bushing with a grounded metal push-rod, in a grounded bushing, with just a tiny sliver of Teflon insulator on the end that pushed against the switch contacts. The problem was banished. It just goes to show that if you have the *best* materials,

and the *finest* concept, and you misapply things just a *little*, you can get some *terrible* results.

Recently, I was testing some of my operational amplifiers, LPC662's, with MOSFET inputs. The bias current was consistently down in the 2- or 3-fA area. It was so small that it really was hard to measure. I had a 10-pF integrator running, similar to Arnie's, but I was trying to get 20 times greater resolution. The resolution was marginal, as there were some jumps in the signal. The signal had long tails and additional errors if you tested a good amplifier after a bad one had pegged. And the switches didn't always give zero error on a damp day. So I wrote down a list of the fixes I needed, and I set my new technician Paul to work on them.

Paul made some imaginative and bold improvements. I had suggested that he should plot the ramp on a strip-chart recorder. Paul set up a digitizing scope and programmed it to spit out the answer scaled directly in femtoamperes.

I asked Paul to set up a simple circuit to drive a 6-V reed relay so there wouldn't be much charge coupled into the circuit from the voltage that drives the coil. Paul set up a clever adaptive circuit to take advantage of the small difference between the relay's pull-in and drop-out current, so that he fed the coil 2.6 V all of the time. You only had to hit the coil with a small pulse of voltage, positive or negative, to close or open the contacts, respectively.

I cautioned him that if the wires wiggle, they can couple a lot of charge and noise into the input. Paul strung the whole circuit up on rubber bands, as a shock mount, so that people walking on the floor nearby would not ruin the measurement.

Also, I cautioned him that we would soon need a good, low-leakage socket, guarded with Teflon insulation. Again, Paul gave me better than I asked for, with a big slab of Teflon for all of the components to be mounted on or above.

I explained to Paul that the slow recovery from overload was caused by the silver-mica feedback capaci-



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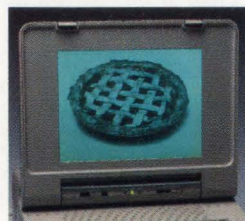
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PEASE PORRIDGE

tor which had poor dielectric absorption. I gave him a capacitor that I had made—filled with air—about 0.5-in.-by-2 in.-by-4 in. of air, to make a 5-pF capacitor. It had copper plates and guarded copper side-frames.

Now, first of all, why am I telling you all of these details? If I design a tester with greatly improved performance to help me test a really high-performance product, why should I tell all our competitors so that anybody in the world can test their products using the improved tester? Why should I give away all of these hard-earned secrets?

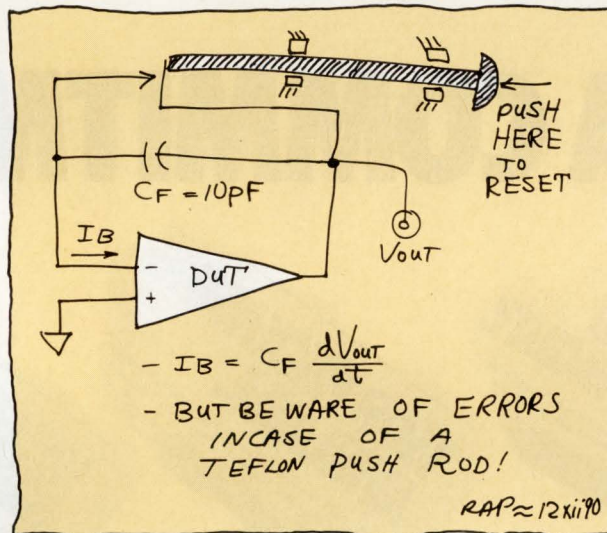
Here's a preliminary answer: It's probably true that some competitors might learn how to test better and faster if I give them my techniques. But my customers will also learn faster. There are more of them, and it's more important to teach them, because they're still trying to come up the learning curve. There's not much point in keeping secrets about testing if our customers are kept in the dark. It's just not fair to make your customers guess what is a good way to test your products.

Note that that is *not* the same as telling the customer exactly how we test it (we have testers, big expensive Teradyne setups, with monstrous interface boxes and complex software, and it would be much too complicated to tell everybody exactly how we run each test). But we do feel obligated to give any customer a good, valid test circuit that gives the same data as our production tests.

Okay. Paul set up this fixture. But there were a few little problems. For one, the output ramp would occasionally give a jump at random times. This jumping seemed worse than previously. Also, I asked Paul to test a whole group of parts, and he said, well, it would take longer than one day to test those parts.

OH?? I knew Paul could test those parts in less than a day—unless there was something wrong. I asked, *well*, why can't you test a part in a

minute or two? He replied, "The output is off-scale and doesn't even come on-scale for 2 minutes." That didn't seem right. It wasn't until 3 days later that I slapped myself on the forehead at 6 A.M.—it was the Teflon factor. Paul had added lots of Teflon around the circuit, and the charge stored on its surface was the major cause of the long tails. When I got to work, I asked Paul to cover up as much of the Teflon as he could with aluminum foil—and ground it. He said the settling got a *lot* better. So he then removed all of the Teflon, and the slow settling went away. Just like Arnie's problem and Arnie's solution, 16 years earlier!



The next problem was with those darn jumps. Now, we could program the tester, not just to test the ramp for 60 seconds, but to test for six 10-second segments. If the answer was the same for 3 or 4 of the segments, then that is probably valid data and we should just ignore segments where the data had a big JUMP. Yes, we could do that. But, where did these jump errors come in?

The jumps were only 10 mV or so, always in the same direction, and at random times. Older fixtures did not have as many jumps. Why? The answer seemed to be related to that nice big feedback capacitor I had made. The circuit *did* have fast settling—not such a long tail as the older silver-mica feedback caps. But Paul spotted some literature—some

Keithley data sheets—and some notes in Jiri Dostal's book* about cosmic rays and charge.

Dostal observed that when a cosmic ray or alpha particle or other energetic subatomic particle passes through matter, it often causes a discharge of electrons. If there's a sensitive detector nearby, some charge may come through the air and cause several thousand electrons to arrive at the detector.

Not just one electron, but several thousand—hey, that was the size of the jumps we were seeing—5 pf × 10 mV is about 50 femtocoulombs, equal to 300,000 electrons. So we researched a little more and realized

that if we made a smaller volume of air adjacent to the delicate summing point of the amplifier under test, we should be able to cut down on the rep rate of these little jumps. So we're now preparing two feedback capacitors. We're not sure which one we will use, but they should both work quite well.

One has an air dielectric, but it's only 1 in. by 1.2 in. with 0.080-in. spacing between the plates. It will have less than 1/10th of the volume of the old air capacitor. The other feedback capacitor will use about 5 inches of twisted pair, using one

piece of bare bus wire, and another wire with sleeving made of...Teflon. If you put it in the right place, Teflon is really *good* stuff. Some time I will tell more about which capacitor we used, and the other details we need to test for femtoamperes. Sockets?? Relays?? Ha!!

All for now. / Comments invited! / RAP / Robert A. Pease / Engineer

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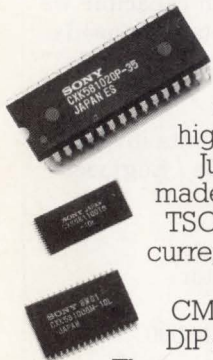
*Jiri Dostal, *Operational Amplifiers*, Elsevier Scientific, 655 Avenue of the Americas, New York, NY 10010; (212) 989-5800. About \$113.

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CXK581100YM*	128K x 8	100/120	TSOP (reverse)	L, LL
CXK581001P	128K x 8	70/85	DIP 600 mil	L
CXK581001M	128K x 8	70/85	SOP 525 mil	L
CXK581020SP	128K x 8	35/45/55	SDIP 400 mil	
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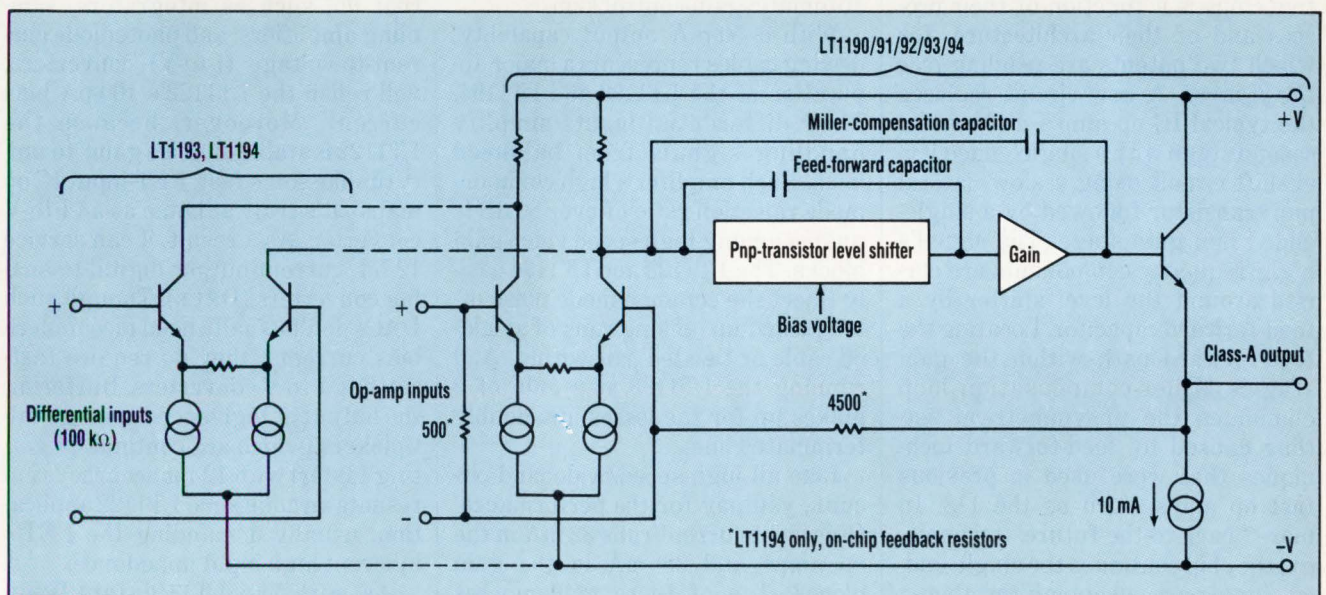
OP AMPS FROM 18-V, STANDARD BIPOLAR PROCESS CHALLENGE SPEED/BANDWIDTH OF COMPLEMENTARY-PROCESS DEVICES.

FRANK GOODENOUGH

Over the past few years, devices built on complex and expensive complementary-bipolar processes have dominated the high-speed/wideband IC op-amp arena (ELECTRONIC DESIGN, April 12, 1990, p. 45). The one exception to that, of course, is fast-settling devices with JFET input stages. But even several FET-input op amps are now built on these complementary processes. Nonetheless, process and circuit designers at Linear Technology Corp. (LTC) felt there was lots of life left in the fast lane for op amps from non-complementary processes. Their goal: Challenge the performance of today's fastest IC op amps, but beat them on cost. To achieve it, build them on processes that do not own the fast vertical pnp transistors of a complementary process.

The development process at LTC took two tacks. One produced the LT1190 family containing three video-bandwidth op amps and 2 video-bandwidth gain blocks with high-impedance differential inputs. The second approach produced the LT1122, one of the fastest-settling IC op amps with a JFET input. The 1190 family is built on a conventional (non-complementary) 18-V bipolar process. The LT1120 FET op amp is constructed on LTC's conventional 40-V bipolar process, which builds unique, polysilicon, FET gates (JFETs can be added to virtually any bipolar process). These are maximum voltage ratings. Unless noted, all other specifications for the LT1190 family are typical, but maximum and minimum ratings will be available by March. Specifications for the LT1122 are maximums or minimums for the lowest-grade units.

Aimed at a wide range of video-signal applications, the



A SINGLE-ENDED SECOND STAGE in members of the LT1190 IC amplifier family put feedforward circuitry around a slow pnp level shifter located inside a Miller-compensation loop. The circuit cuts the settling time of older designs yet slews and settles symmetrically. The LT1193/94 video gain blocks add a second differential stage on the front-end to provide 100 kΩ of resistance at both inputs.

FAST-SETTLING IC OP AMPS

five members of the LT1190 family have much in common, plus a few important differences. The three op amps—the LT1190, LT1191, and LT1192—offer minimum stable closed-loop gains of +1, +1, and ± 10 ; gain-bandwidth products of 50, 90, and 400 MHz; and open-loop gains of 85, 90, and 100 dB, respectively. Driving 1000 Ω , all five slew at 450 V/ μ s, which translates into a full-power bandwidth of 24 MHz for a 6-V pk-pk output swing from a ± 5 -V supply.

SPEEDY SETTLERS

The LT1190/91/92, which are true op amps, fill applications from conditioning and processing wideband signals to driving flash analog-to-digital converters (ADCs). In addition, because the LT1190 and LT1191 are stable at a gain of one, they lend themselves to fast integrators and active filters. Though their primary use isn't handling fast pulses with precision, their settling time to within 0.1% (10 bits) for a 3-V step is still a mere 100 ns. Settling is symmetrical (both positive- and negative-going signals settle in similar times and with relatively similar waveforms) without a thermal tail, and the high open-loop gain ensures accuracy.

The speed and bandwidth of all five chips is a function of their process and of their architecture, for which two patents are pending (*see the figure*). A new circuit replaces the typical IC op amp's differential second stage with a single-ended level-shift circuit using a slow, lateral pnp transistor followed by a single-ended npn gain stage. The signal's high-frequency components are carried around the level shifter by a feed-forward capacitor. Locating the feed-forward path within the gain stage's Miller-compensation loop eliminates the unsymmetrical settling caused by feed-forward techniques that were used in previous fast op amps, such as the 118. In more "back-to-the-future" technology, the chip continues the single-ended signal path, swapping the almost universal complementary output stage for a class-A emitter-follower circuit.

A major feature of each family member involves providing the necessary current—up to 50 mA—to drive highly capacitive loads and 50-to-100- Ω matched transmission lines. Operating from ± 5 -V supplies, the op amps can put ± 3.8 V across 1000 Ω . From ± 8 -V rails, the output rises to ± 7 V, dropping to only ± 6.5 V for a 100- Ω load. All five can also operate from a single 5-V supply, producing an output swing of 3.75 V, albeit with somewhat reduced speed and narrower bandwidth.

The LT1193 and LT1194 differential video gain blocks have the same basic core circuitry as the op amps. However, an additional differential stage has been added on the front-end. The inputs for both deliver an input resistance of 100 k Ω . The input voltage generates a differential current in the input npn transistors, a current that's matched by the second, and identical, stage connected to the feedback resistors. These internal thin-film devices set the LT1194's gain at 10. They're added externally by users of the LT1193 to create gains between two and several hundred. Bringing the LT1194's balance pins high, which can be done in a few nanoseconds, cuts the gain to as low as unity to limit gain under over-signal conditions, or within an automatic-gain-control loop.

With a 50-mA output capability, driving cables represents a major application of the LT1193 and LT1194. Their differential inputs simplify handling signals from balanced lines. Each amplifier's high common-mode rejection ratio of over 80 dB is unique among high-speed video gain blocks. The LT1193 and LT1194 easily reject the common-mode noise often picked up on long runs of shielded cable or twisted-pair wiring. And running the LT1193 at a gain of 2 makes up for the losses in a doubly terminated line.

Like all high-speed/wideband circuits, you pay for the performance. Quiescent current runs 32 mA in the op amps and 35 mA in the gain blocks. Ten of those milliamperes flows in the class-A output stage. However, bringing the ICs' shutdown pin to the minus supply rail

drops the current to just 1.2 mA.

Aside from the fact that it's a fast/wideband op amp, the FET-input LT1122 has little in common with the LT1190 family. Its venue is handling fast pulses accurately. All grades not only settle plus and minus 10-V output steps to within 0.01% of final value in under 540 ns, but that specification is guaranteed. Moreover, every A- and C-grade device coming off the line is tested for it. In the past, measuring this parameter (to 12-bit/0.01% accuracy) on a production basis has been time-consuming and thus "expensive." Even when this parameter was guaranteed, testing was usually performed on a sampling basis.

NEW TEST CIRCUIT

To cut costs, test engineers at LTC developed a new test circuit using two poles of the LTC201A, their high-speed quad analog switch, as a flat-topped, ± 10 -V signal generator. Slew rate runs 50 V/ μ s, which translates into a typical full-power bandwidth of over 1 MHz. Unity-gain bandwidth typically runs 13 MHz (all LT1022 specifications are for the lowest-grade devices).

Many high-speed applications don't need the low bias current of a FET-input op amp. However, those that do, such as integrators, sampling amplifiers, and photodiode current-to-voltage (I-to-V) converters, will relish the LT1122's 100-pA bias current. Moreover, because the LT1122 is stable at noise gains to unity (unlike some fast, FET-input IC op amps), it's truly at home as an I-to-V converter. As a result, it can service 12-bit, current-output digital-to-analog converters (DACs). Though such DACs don't usually need picoampere bias currents, they do require fast-settling I-to-V converters. Buffering the output of high-speed analog multiplexers (which are continually getting faster) with 12-bit accuracy represents an additional LT1122 application, usually demanding the FET's inherent high input impedance.

As with the LT1190-family op amps, the LT1122 also combines high open-loop gain (103 dB driving 1 k Ω , which is very high for a FET-input IC

FAST-SETTLING IC OP AMPS

op amp) with symmetrical slewing and settling. The result is total typical harmonic distortion of 0.001% (for a 7-V rms output and a 5-k Ω load, over 20 Hz to 20 kHz). With such low distortion and a 1-MHz power bandwidth, the LT1122 should find wide acceptance in the audio community. Even when driving 600- Ω , open-loop gain is still above 100 dB.

Offset voltage, while not in the OP-07 class, is under a millivolt (900 μ V) and common-mode rejection ratio is 80 dB—numbers that are superior to those of most FETs. Driving 600 Ω and operating from \pm 15-V rails, the LT1022's output swings \pm 11.5 V and its supply current is 11 mA. It should be noted that like most FETs, the FET-input op amp needs split supplies. It can operate, however, from \pm 5-V supplies even though performance is reduced.

Only marginal differences separate the premium A and B grade devices from the lower C and D grades. For example, the offset voltage, slew rate, settling time, and open-loop gain of the premium units run 600 μ V, 60 V/ μ s, 540 ns, and 105 dB, respectively. Under similar conditions, these specifications for the lower-grade units run 900 μ V, 50 V/ μ s, 590 ns, and 103 dB, respectively. Both grades are available tested (and untested) for the settling-time specification. \square

PRICE AND AVAILABILITY

Members of the LT1190 family come in plastic (commercial) and ceramic (military) 8-pin DIPs and SOICs (commercial). In quantities of 100, the plastic DIP versions cost \$2.25 each for the LT1190, \$2.40 each for the LT1191 and LT1192, and \$2.95 each for the LT1193 and LT1194. The LT1122 comes in similar packages and temperature ranges. In quantities of 100, the LT1122DCN (low grade, plastic DIP with settling time not 100%-tested) goes for \$2.50 each. The LT1122CCN, the same op amp that's 100%-tested for settling time, goes for \$2.95 each in 100s. Small quantities of all devices are in stock.

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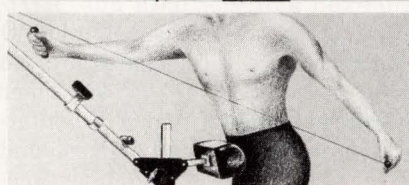
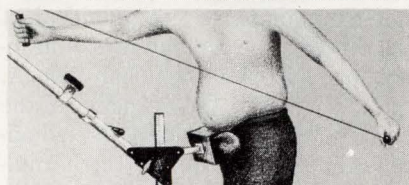
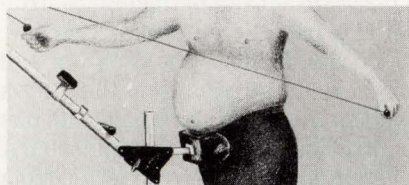
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CIRCLE 106

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EMBEDDED CONTROLLER BOARD OFFERS IN-SYSTEM RECONFIGURABILITY

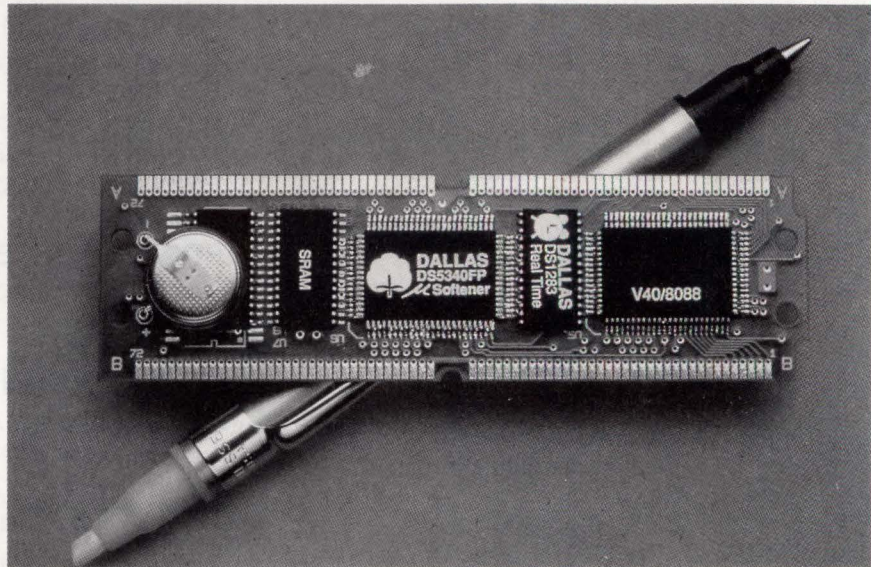
DAVE BURSKY

A compact circuit-card assembly, which is about the size of a large stick of chewing gum, can give designers a reprogrammable, embedded CPU to tackle demanding control tasks. The assembly combines a high-integration processor and up to 256 kbytes of battery-backed static RAM. The first version of the Flip-Stik module from Dallas Semiconductor—the DS2340—employs the NEC V40 processor, an 8086 software-compatible CPU with many on-chip features, including a serial port, interrupt controller, timer-counter, and DMA controller. Also included on the mini circuit card are up to 256 kbytes of CMOS SRAM, a lithium battery, and the recently released DS5340 Micro Softener chip, which ensures crash-free recovery due to unstable power.

The DS5340 replaces more than half-a-dozen other circuits to implement a power monitor, a watchdog timer, an address decoder, a dual-port register file, and parallel I/O ports. To aid in systems startup, there's a clock oscillator, a bootstrap ROM, a bootstrap loader, and the ability to turn blocks of RAM into nonvolatile memory by powering the RAM in the low-voltage backup mode from the 3-V lithium cell.

An option—can be included on the module—is Dallas' DS1283 real-time clock; with the option, the module's part number becomes DS2340T. The 1283 is a permanently powered clock and calendar circuit that keeps track of hundredths of seconds, seconds, minutes, hours, days, date of month, months, and years.

The Flip-Stik module has the same physical size as the 72-contact high-capacity single-in-line memory modules typically used in computer systems. However, rather than one row of contacts, the card has two rows of 72 contacts each—one row on each of the long sides of the small pc card. Side A is intended for single-board systems and provides three byte-wide bidirectional I/O ports. One of



those ports can alternatively serve as eight interrupt inputs. The two other ports can be configured as a high-speed interface to allow the DS2340 to act as a peripheral controller to a host microprocessor system.

On the B-side of the SIMM are all of the address lines from the V40 as well as the DMA handshake and bus control lines for system expansion. A system could thus be converted from non-expandable to expandable just by flipping the module over and inserting side B rather than side A. Signals common to both edges of the card include the nonmultiplexed address lines A15-A8 as well as the multiplexed address/data bus, AD7-AD0, as well as the memory and I/O control lines. Also included are the V40's serial port and counter-timer I/O lines and all of the CPU's interrupt input lines except for lines 5 and 7, which are dedicated for the time-keeper chip and the softener chip, respectively. Both sides of the card also bring out three lines for the DS5340's Port A, as well as the crystal inputs, the Reload control pin, several Chip Enable signals for off-card memory, and a latched A16 Address line from the V40.

On-card Memory options for the DS2340 include 16, 64, 160, or 256

kbytes of nonvolatile static RAM, which can be controlled by the five operating modes of the Flip-Stik. The modes set up various control lines to serve as memory control signals and determine whether the signals are intended for a closed, non-expandable system or for an expandable, more flexible system.

Because the processor on the Flip-Stik is software compatible with the 8086, software can be developed directly on an IBM PC or compatible. That also gives users many development tools to choose from.

Furthermore, software designers for the Flip-Stik can take advantage of many software tools that already run on PCs for native-language code development. Because the V40 can run 8086-based software, a PC-type BIOS for the V40 Flip-Stik will be developed; it's scheduled for release in the second quarter of this year. Once that's available, the Flip-Stik will be able to run many of the DOS-compatible application packages.

Prices for the DS2340 start at \$53.40 in 1000-unit quantities. Delivery is from stock.

Dallas Semiconductor Corp.,
4350 South Beltwood Pkwy., Dal-
las, TX 75244-3292; Don Folkes,
(214) 450-0400. **CIRCLE 301**

NEW PRODUCTS

DIGITAL ICs

PC PRODUCTS SIMPLIFY LAPTOP DESIGNS

A host of PC products from VLSI Technology Inc. aims at designs ranging from low- to high-end PC/AT-compatible systems, including laptop and notebook PCs. The products include the VL82C325 and VL82C335 cache controllers, the VL82C107 combination chip, and the VL82C312 power-management unit (PMU). The latter two parts combine with the recently announced VL82C310 Scamp-LT PC/AT controller to form a three-chip notebook PC chip set. The cache controllers can operate with the company's Scamp or Topcat chip sets using either 80286 or 80386 microprocessors.

The VL82C325 SX cache controller contains all of the cache control that's needed to implement 80386SX cache subsystems with one or two external cache data RAMs for data memory. Memory configurations of up to 16 Mbytes can be supported. The VL82C335 DX chip uses two or four external cache data RAMs in 80386DX systems, supporting up to 64 Mbytes of memory. The two controllers feature a lookaside architecture that allows the cache and main memory to be accessed in parallel. Just one external AND gate is required and no other glue logic is needed in the system. Both parts can operate in pipelined and nonpipelined modes. Also, both contain a built-in test feature and cache data RAM testability. The parts are housed in 100-lead plastic quad flat packs. The VL82C325 and VL82C335 cost \$70 and \$85, respectively. Samples are available now, with volume production expected to begin in the second quarter.

The VL82C107 combines a keyboard, mouse controller, and real-time clock



with address latches, buffers, DMA acknowledge decoders. This combination is required by the Scamp-LT controller. The part also contains the circuitry necessary to link PC memory cards to the system. It's available now in sample quantities in a 128-lead plastic quad flat pack. Production will start in the second quarter. Single-unit prices are about \$25.

The PMU chip reduces overall system power consumption and adds a few features necessary for laptop and notebook PCs. The power reduction is done with activity monitors that detect system inactivity. Upon detection, the CPU clock frequency is slowed down and power is removed from peripheral devices. The chip also integrates some of the ordinary glue logic found in portable systems. This includes chip-select and interface logic for floppy-disk controllers, IDE hard-disk interfaces, serial and parallel ports, and display devices. It's available now in sample quantities. Production will start in the second quarter. Single-unit prices will run for around \$40.

VLSI Technology Inc., 8375 South River Pkwy., Tempe, AZ 85284; (602) 752-6200. **CIRCLE 302**

RICHARD NASS

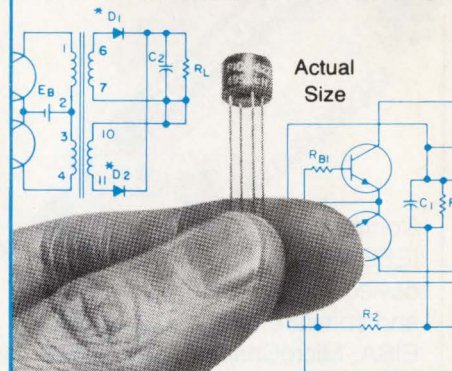
IMAGING CHIP SCALES, ROTATES IMAGE DATA

The Bt710 scaling and rotation chip manipulates monochrome images many times faster than standard graphics and general-purpose processors. It has a unique scaling algorithm that scales bi-level images to produce a gray-scale result. Two on-chip DMA channels, which support autonomous operation, manage reads from source-image buffers and writes to destination buffers. The channels translate addresses for image rotations and transfer bit-

aligned blocks to window or frame-buffer pixel boundaries. Scaling can be down to 6% or up to 750% of the original image. The PixelVue software package lets you manipulate images in a PC or workstation. The Bt710 comes in a 132-lead PGA package and costs \$132 in 100s. An evaluation kit that includes the Bt710 on an AT-compatible plug-in card costs \$995. PixelVue development kits start at \$1990 for the Windows 3.0 DOS environment.

Brooktree Corp., 9950 Barnes Canyon Rd., San Diego, CA 92121; Tom Kovanic, (619) 452-7580. **CIRCLE 303**

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PCB TOOLS CONFORM TO MILITARY STANDARDS

Two new tools from Valid Logic Systems, a pc-board reliability analyzer and a documentation tool, comply with military and international standards that include MIL-HDBK-217E, CNET, and Computer-aided Acquisition and Logistics Support (CALS). Viable is a pre- and post-layout analysis tool that lets users predict reliability at the component, board, and system levels. Viable makes its predictions based on device operating voltage, current, power, temperature, duty cycle, and manufacturing processes. CALS-Out is a software package for generating release and process documentation that meets CALS requirements. Users can produce assembly drawings, fabrication drawings, and other documentation in standard formats. In addition, it delivers data files electronically in the International Graphics Exchange Specification (IGES) 4.0 format. Both tools will be available this month. Viable and CALS-Out run on DEC, IBM, and Sun workstations, and cost \$12,000 and \$6000, respectively.

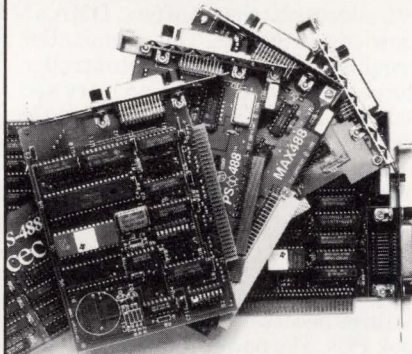
Valid Logic Systems Inc., 2820 Orchard Pkwy., San Jose, CA 95134; (408) 432-9400. CIRCLE 304

TIMING-DIAGRAM TOOL TACKLES LARGER DESIGNS

The newest version of the dV/dt timing-diagram software, called dV/dt Plus, uses extended memory to handle larger and more complex timing diagrams. The software automates the manual and tedious task of drawing timing diagrams and supporting documentation. As an analysis tool, it lets designers set propagation delays, verify requirements, and measure time be-

tween edges. In addition, users can perform trade-off analysis before schematic capture with the tool's "what-if" capability. An IBM PS/2, PC/AT, or compatible is required with dV/dt Plus. There must be 640 kbytes of RAM plus a minimum of 1 Mbyte of extended memory. The product is shipping now for \$795. The original DOS version and the Macintosh version of dV/dt cost \$695. Designers can obtain a free demo disk by calling the company.

Doctor Design Inc., 5415 Oberlin Dr., San Diego, CA 92121-1716; (619) 457-4545. CIRCLE 305



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MCM TOOLSET MASTERS FRONT-TO-BACK DESIGN

A number of stand-out features support MCM Engineer, a multichip-module (MCM) design system. The features include component placement, timing-driven routing, high-speed layout analysis, thermal analysis, design verification, and manufacturing integration—all under one user interface. It's tied into schematic entry and logic simulation at the front end, a suite of layout simulation tools in the middle, and manufacturing interfaces on the back. MCM-L, MCM-O, and MCM-C technologies are supported. In addition, MCM Engineer can handle a resolution of 0.001 μm for small thin-film MCMs, and up to 120 layers for co-fired MCMs. Users can choose from three common chip-mount techniques: flip chip, tape-automated bonding, and wire bond.

MCM Engineer runs on Intergraph workstations, and will be available sometime this quarter. Including all functions, it costs \$85,000 per seat.

Intergraph Corp., Electronics Div., Huntsville, AL 35894-0001; (800) 826-3515 or (205) 730-2700. CIRCLE 306

PCB TOOL CALCULATES TRACE IMPEDANCES

Support for two more board-trace geometries—buried microstrip and asymmetric stripline—are the latest additions to the LineSim transmission-line simulator from HyperLynx Inc. With the additions, LineSim version 1.42 can calculate the impedance of almost any digital pc-board trace from basic parameters, such as width, thickness, distance from power planes, and board dielectric. Rather than surveying a printed-circuit board after layout, LineSim is intended for design of critical traces before layout begins. With LineSim, the circuit to be simulated is specified in a "push-button" schematic: circuit elements are clicked in and out with a mouse. The simulation itself is shown on the screen in an oscilloscope-like display, and is completely interactive. Compilation isn't necessary to resimulate the circuit when a parameter is changed. LineSim 1.42 is shipping now for \$595. It comes with both a hard-copy and on-line manual.

HyperLynx Inc., P.O. Box 3578, Redmond, WA 98073-3578; (206) 869-2320. CIRCLE 307



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Capital Equipment Corp.
Burlington, MA. 01803

CIRCLE 99

DUAL PWM-CONTROLLER IC FIXES AC POWER FACTOR, REGULATES DC OUT

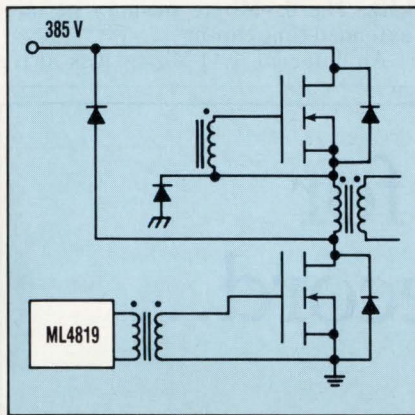
FRANK GOODENOUGH

Until now, if you wanted to build an off-line switching power supply sporting power-factor correction (PFC), two separate pulse-width-modulation (PWM) controller ICs had to be employed. One ran the boost converter that corrects for power factor. The other ran the more conventional buck converter that followed it, changing the high voltage output of the PFC circuit to regulated, isolated, system supply rails. Micro Linear's ML4819, aimed at 100- to 400-W supplies for PCs, instruments, and peripherals, does both jobs.

The IC contains two PWM controllers that share a common oscillator, voltage reference, and UVLO (undervoltage lockout) circuit. The common circuits eliminate external components, significantly saving both cost and pc-board space. In addition, because the oscillator is shared, there's no need for special circuits to prevent beat notes.

Why power-factor correction? The line current drawn by a typical capacitor-input full-wave rectified-power supply is a spike of current that flows at the sine-wave peaks for about 1/5 of each half cycle. Such a load on an ac line represents a power factor of no more than 0.65. It not only limits the power drawn from a given ac line to about 65% that of a resistive load, but it's rich in harmonics that can cause dangerous heating in the neutral wires of power distribution systems. By the end of the decade, half of the load on the power grid is expected to be electronic: switching power supplies. As a result, by 1992, Europe is expected to have strict legal limits on power factor, with the U.S. probably on its heels. Moreover, while most 115-V ac lines can provide no more than about 700-800 W to a load with a power factor of 0.65, high-end workstations and even today's PC-based systems push a kilowatt.

A power-factor-correcting boost converter using the ML4819 pro-



duces 385 Vdc from ac lines between 90 and 260 V. As a result, it handles the low to high limits of both U.S. and international ac mains. Like most PFC controllers, it employs current-mode control and senses the sinusoidal ac-line voltage. This sinusoidal voltage is multiplied by the output of the error amplifier (the difference between the output voltage and the reference voltage). The multiplier's output becomes the reference for the PWM comparator, which senses the current in the external power-factor-correcting power MOSFET. Thus, the on-time of the MOSFET is a function of both the 385 V output and the input sine wave, forcing the ac line current to a sinusoidal shape.

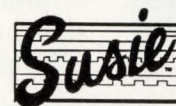
The output PWM controller is a conventional current-mode circuit with several added features: a maximum duty-cycle clamp, slope compensation, and cycle-by-cycle current limiting. The controller is recommended for use in the "two-switch forward converter" topology (see the figure). This circuit offers the distinct advantage of clamping the voltages across the external MOSFETs to a value of 380 V (the output of the PFC converter). Conventional single-switch designs demand MOSFETs rated at twice that voltage, plus a safety factor to allow for the effects of leakage-inductance spikes. One higher-voltage power FET costs more than twice as much as two lower-voltage devices, and its

higher on-resistance yields a supply with lower efficiency—unless a costlier FET is used.

A 15-A, 12-V 88-kHz supply running off rectified 120 V ac, built with the ML4819 in the two-switch topology, sports a full-load efficiency of 85%. Power factor runs 0.996 at 15 A off a 120-V line, 0.994 off a 220-V line. Total harmonic distortion (THD) ranges from 2% with a 7.5-A load off a 90-V line to 33% with a similar load off a 240-V line. Similar THDs at 15 A are 6% and 14%, respectively.

The ML4819 comes in a 20-pin DIP and goes for \$3.95 each in quantities of 100. Small quantities are in stock.

Micro Linear Corp., 2092 Concourse Dr., San Jose, CA 95131; Jon Klein (408) 433-5200. CIRCLE 323



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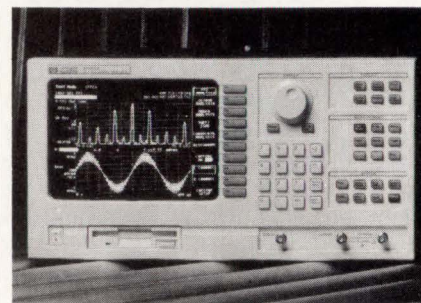
CIRCLE 176

SPECTRUM/NETWORK ANALYZER COMBINES FUNCTIONS

The dual-channel HP 35665A spectrum/network analyzer combines the functions of several instruments in one unit to offer a broad range of high-performance mea-

surement options. The analyzer makes spectrum measurements to 102.4 kHz and network measurements to 51.2 kHz. The 6.4-Mbyte memory permits extended-time capture.

An internal 1.44-Mbyte disk drive



compatible with HP 9000 Series 200 and 300 workstations and MS-DOS computers, stores traces, instrument states, limit tables, and HP Instrument Basic programs. The unit is protected against aliasing and offers 400-line frequency resolution and digital-zoom capability.

Options that expand the instrument's basic analyzer capabilities include computed order-tracking, ANSI-compliant real-time octave measurements, swept-sine measurements, curve fitting and synthesis, arbitrary source capability, and the ability to run HP Instrument Basic programs.

With advances in signal-processing techniques, the HP 35665A can make 10 measurements per second with the display on and up to 30 per second in the fast-average mode (a 12.8-kHz real-time rate). Signals can be recorded to a waterfall display at more than 10 updates per second.

The HP 35665A analyzer starts at \$12,500. Delivery is estimated at 12 weeks after receipt of order.

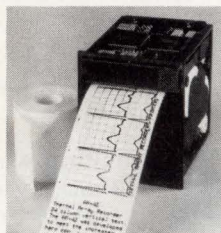
Hewlett-Packard Co., Lake Stevens Instrument Div., 8600 Soper Hill Rd., Everett, WA 98205-1298; (800) 348-0033 or (800) 752-0900.

CIRCLE 319

JOHN NOVELLINO

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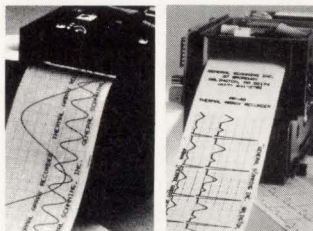


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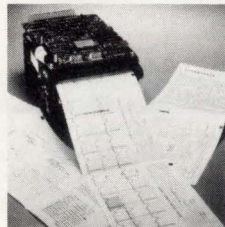
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CIRCLE 175

ASSEMBLY CONVERTS 28-PIN DIP PLUG TO PLCC

Emulators designed for 28-pin DIP devices can be converted to work with PROMs in 28-pin PLCC packages using the SOCON 28DIP6/PLCC converter. The assembly consists of a pc-board with a female production-style DIP socket on top. The board is mounted on a PLCC plug with 50-mil-space, gold-plated round contact pins. The pins are wired one-to-one. The 28DIP6/PLCC costs \$165 in single-unit quantities; quantity discounts are available. Delivery is stock to 5 days after receipt of an order.

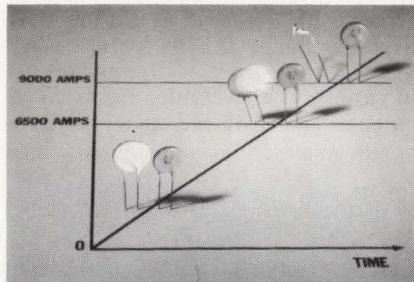
EDI Corp., P.O. Box 366, Patterson, CA 95363; (209) 892-3270. CIRCLE 324

SMALL METAL-OXIDE VARISTORS SOAK UP BIG TRANSIENT CURRENTS

Peak transient currents of 9000 A are within the capabilities of the Sanken Super S series of metal-oxide varistors from World Products. The disk-shaped components meet the increasing challenge of protecting sensitive circuitry from the destructive effects of transient voltage surges. Not only do the Super S varistors handle more current, but they do so in a smaller-than-standard package that measures 17 mm in diameter compared with the usual 20 mm.

In extensive testing, the Super S varistors outperformed others from competitors by handling up to 30 times the number of 6500-A surges before the varistor voltage varied by more than 10%. That's the generally accepted standard for device failure. In addition, the Super S varistor was the only device that withstood pulses of 9000 A and remained within spec. Furthermore, the varistors display better temperature stability and a higher energy rating (120 joules) than competing devices.

The improved performance in a smaller package isn't a matter of improved materials, but rather of process advances. Sanken slightly changed the material mix in the varistor disks, and



changed their production process to yield more consistent grain barriers in the finished product. The result is higher thermal resistance, which aids in temperature stability.

The Super S series ranges from 130 to 680 V ac rms ratings. Devices are offered in all standard lead spacings and can be taped and reeled for automatic insertion. Epoxy length on the leads is tightly controlled to a maximum of 3 mm to guarantee excellent solderability. Pricing in quantities of 1000 is \$0.25. Delivery is from stock to eight weeks.

World Products Inc., Protection Products Group, P.O. Box 517, Sonoma, CA 95476; (707) 996-5201.

CIRCLE 313

■ DAVID MALINIAC

4-MM SURFACE-MOUNTED TRIMMER WITHSTANDS ALL PROCESSING

A surface-mounted trimmer is being claimed as the industry's smallest 4-mm multiterm trimmer. The model 3224 from Bourns Inc. offers superior setting accuracy and long-term reliability. In addition, the device is sealed for compatibility with all surface-mounting placement, soldering, and cleaning processes.

The 11-turn device boasts a rotational life of 200 cycles, which is particularly important in applications where frequent and accurate adjustments are needed. Such capabilities in a 4-mm package make the model 3224 trimmer useful in precision instruments, telecommunication-switching equipment, and industrial-automation controllers and sensing equipment.

Many manufacturing obstacles associated with using electromechanical devices in surface-mounted assemblies are leapfrogged by the trimmer. Some

features that aid in this respect are a smooth-top surface and a flush side-adjustment screw that permits high pick-and-place throughput and yields. Designers will appreciate its industry-standard footprint layout.

The trimmer comes in a broad range of resistance values ranging from 10 Ω to 2 M Ω . Other electrical-performance values include a contact-resistance variation of 1%, temperature coefficient of 100 ppm/ $^{\circ}$ C, and resistance tolerance of 10%.

Pricing begins at \$1.98 in quantities of 1000 to 4999. The trimmers are packaged on 12-mm-wide tape reels that meet EIA standards. A 7-in. reel holds 500 pieces and a 13-in. reel carries 3000. Availability is in eight weeks after receipt of order.

Bourns Inc., 1200 Columbia Ave., Riverside, CA 92507; (714) 781-5071. CIRCLE 314

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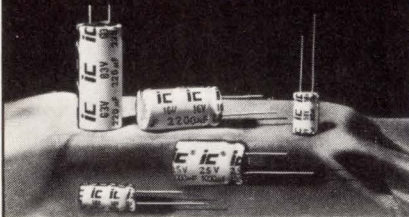
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CIRCLE 102

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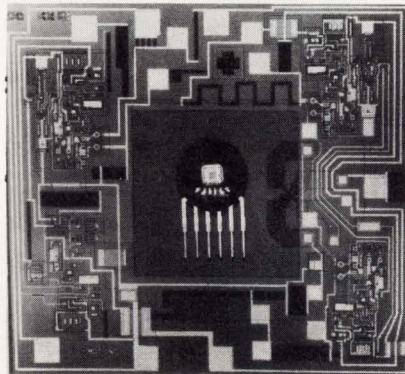
An LED, bright enough to be seen at 1500 ft. in all ambient-light conditions, is available from ROHM Corp. The SLA-580 Series LEDs feature a 12° viewing angle that's well suited for use in various transportation-safety applications. The LT3F red model produces



1.75 to 2.5 cd (candlepower) at 20 mA. The MT3F green unit produces 0.4 to 0.6 cd at the same current. In million-piece quantities, the red LEDs cost under \$0.50 and the green types under \$0.10. Delivery is in 10 weeks.

ROHM Corp., 8 Whatney, Irvine, CA 92718; (714) 855-2131. **CIRCLE 315**

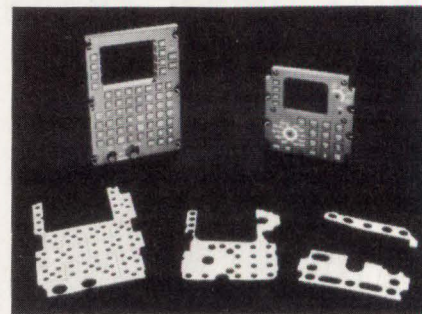
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Now there's a monolithic 0-to-15-psi pressure sensor with a fully signal-conditioned output. The MPX5100D sensor integrates the sensing element, offset calibration, temperature-compensation circuitry, and signal amplification. Because its output scale is calibrated from 0.5 to 4.5 V, the device is well suited for microprocessor-based systems with analog to digital inputs. Temperature compensation is from zero to +85°C. The sensor costs \$45 in lots of 100. Samples are from stock, and production quantities have lead times of 6 to 8 weeks.

Motorola Inc., 5005 E. McDowell Rd., Phoenix, AZ 85008; (602) 244-4556. **CIRCLE 316**

MIL-SPEC EL LAMPS MEET NVIS NEEDS



Guaranteed compliance with MIL-L-85762A for night-vision imaging-systems (NVIS) applications is offered by the 10G/NVIS electroluminescent lamps from ELtech. The lamp is designed for military avionics applications, such as MIL-7788E Type IV cockpit panels, as well as LCDs and floodlights. The key to the lamp's compliance is its filter design, which is just 0.010-in. thick and is made from a polycarbonate material. Pricing depends on lamp configuration and quantity. Delivery is in from 10 to 12 weeks from receipt of order.

ELtech, 181 Gibraltar Rd., Horsham, PA 19044; (215) 441-0404. **CIRCLE 317**

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standard 250 for Type 4X enclosures. The Weather Ready Series of Minikey devices hold up in many industrial applications. A broad range of designer colors, double-shot key legends, and standard or custom output codes is available. Call for pricing and delivery.

XCEL Corp., 4290 E. Brickell St., Ontario, CA 91761; (714) 391-4321.

CIRCLE 318

That Was Then...

Quality Comes Through

Company Delivers On Its Promise Of 12-ns SRAMs

By Hugh G. Willett

SANTA CLARA, CALIF. — Silicon Valley start-up Quality Semiconductor Inc. this week will fulfill its plan to move into high-performance static RAMs. Quality Semiconductor will introduce a line of five 16-kilobit \times 4 SRAMs, implemented in 1-micron CMOS, capable of access speeds as fast as 12 ns. The SRAMs follow by one month the debut of

the company's first product line of standard logic devices, and by two weeks its introduction of high-speed first-in first-out (FIFO) memories.

The new SRAMs are designed for the fast-access primary and secondary cache requirements of high-performance RISC- and CISC-based systems, said Sunneel Rajpal, director of marketing at Quality Semiconductor, Santa Clara, Calif. "These SRAMs are targeted at systems with clock rates of at least 25 MHz," he said. "Our fast CMOS process lets us add value through performance

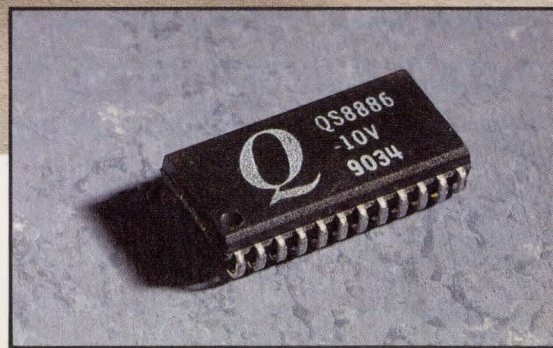
[to page 22]

...This Is Now!

Remember last May when 33-MHz seemed incredibly fast? That's when Quality delivered 12ns 16Kx4 SRAMs for ultra-fast cache designs.

Today the real action starts at 40-MHz, and you'll be glad to know we're not just talking about 10ns devices—but *shipping* in production quantities *right now!*

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And because you need more than fast cache to complete your system, ask about our 15ns FIFO memories and QSFACT™ logic family in FCT/A/B/C speeds.

To order 10 or 12ns SRAMs, call 408-986-1700. Ask about our latest High-Performance CMOS data book with logic, cache and specialty memories designed to help you keep pace in the megahertz race. After all, that was then... this is now!



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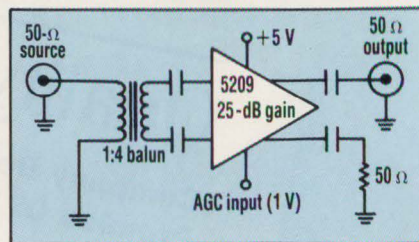
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Article shown was published in Electronic Buyers News, May 7, 1990

ANALOG MULTIPLIER IC HANDLES SIGNALS TO 1 GHz

The NE5209 from Signetics aims at applications ranging from automatic gain control (AGC) in cellular telephones or CATV systems to amplitude modulating UHF carriers with video. The NE5209 is basi-

cally an analog multiplier (variable gain amplifier). With its control voltage at 1 V, it supplies a minimum of 23 dB, ± 0.4 dB of gain, from dc to 400 MHz. The 3-dB bandwidth is a minimum of 600 MHz. Typically, 5 dB of gain is still



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CIRCLE 105

available at 1 GHz. Dropping the control voltage linearly to 0 drops the gain linearly to about -40 dB, a gain change of 60 dB. The 3-dB bandwidth of the chip's control voltage is 20 MHz. In an IF strip, three cascaded NE5209s can provide over 60 dB of fixed or variable positive gain. For fixed-gain operation, an on-chip bandgap reference (typically 1.3 V) can set the control voltage and thus the gain.

Remotely, from a panel, manual gain control of one or more wideband video or RF signals represents another typical application. Alternatively, a host computer can provide the control signal via a low-cost DAC.

Unlike other RF amplifier ICs, the NE5209 is internally compensated, eliminating the need for external networks to tune the circuit for a particular operating frequency. Again, relative to other variable-gain amplifiers, noise increases slowly as gain drops. In most amplifiers, every dB drop in gain adds 1 to 2 dB of noise. However, the NE5209's noise only increases 0.6 dB for each 1-dB drop in gain.

Signal inputs and outputs are both differential, permitting use with baluns in RF applications for impedance matching. The differential output simplifies the job of driving balanced lines. Gain is peaked by matching a 50-ohm source impedance to the chip's 1-k-ohm resistance at each input (see the figure). Output resistance typically runs 50 ohm, so impedance matching isn't required. Operating from a 5-V supply rail and driving 50 ohm, the output swings 400 mV pk-pk. The output swings 1.9 V pk-pk when driving 1 k-ohm.

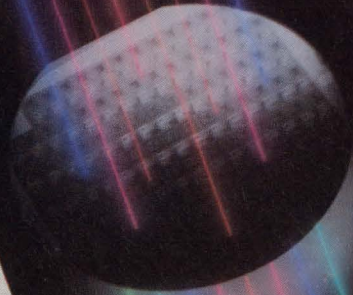
In its 16-pin plastic DIP, the commercial-grade NE5209 runs \$14.24 each in hundreds. The extended-industrial temperature range SE5209 goes for \$17.08 each in hundreds. The analog multiplier IC is available from stock.

Signetics Co., Div. of North American Philips Corp., 811 Arques Ave., P.O. Box 3409, Sunnyvale, CA 94088-3409; Michael Sera, (408) 991-4544. **CIRCLE 312**

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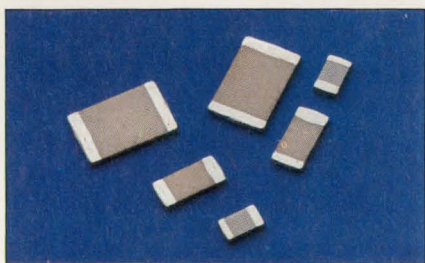
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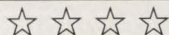
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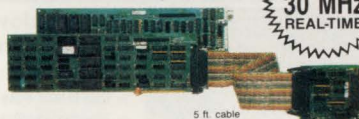
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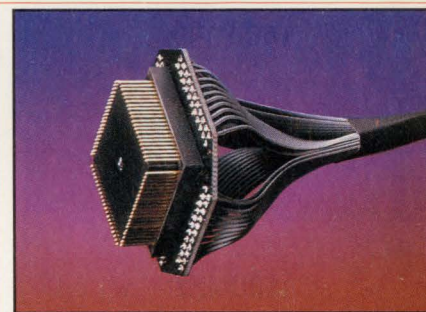
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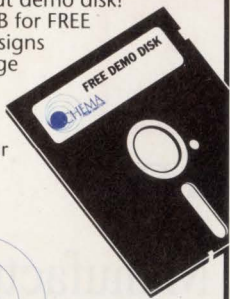
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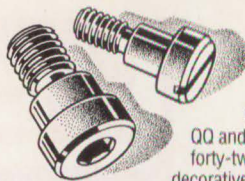
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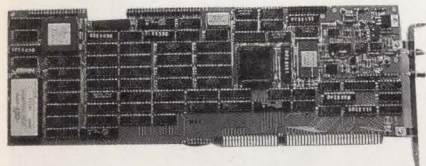


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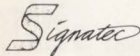
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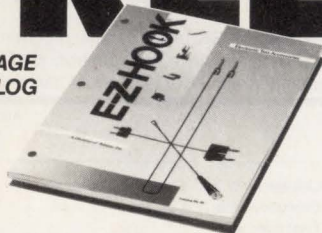
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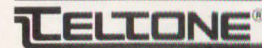
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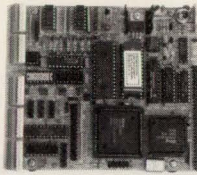
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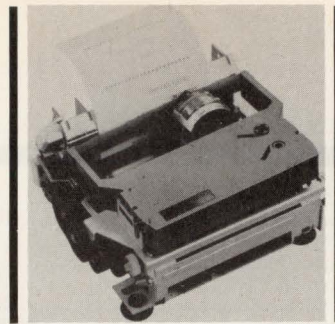
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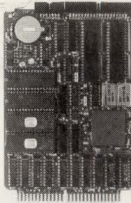
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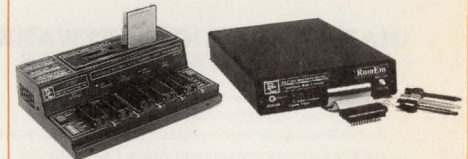


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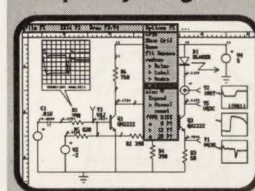
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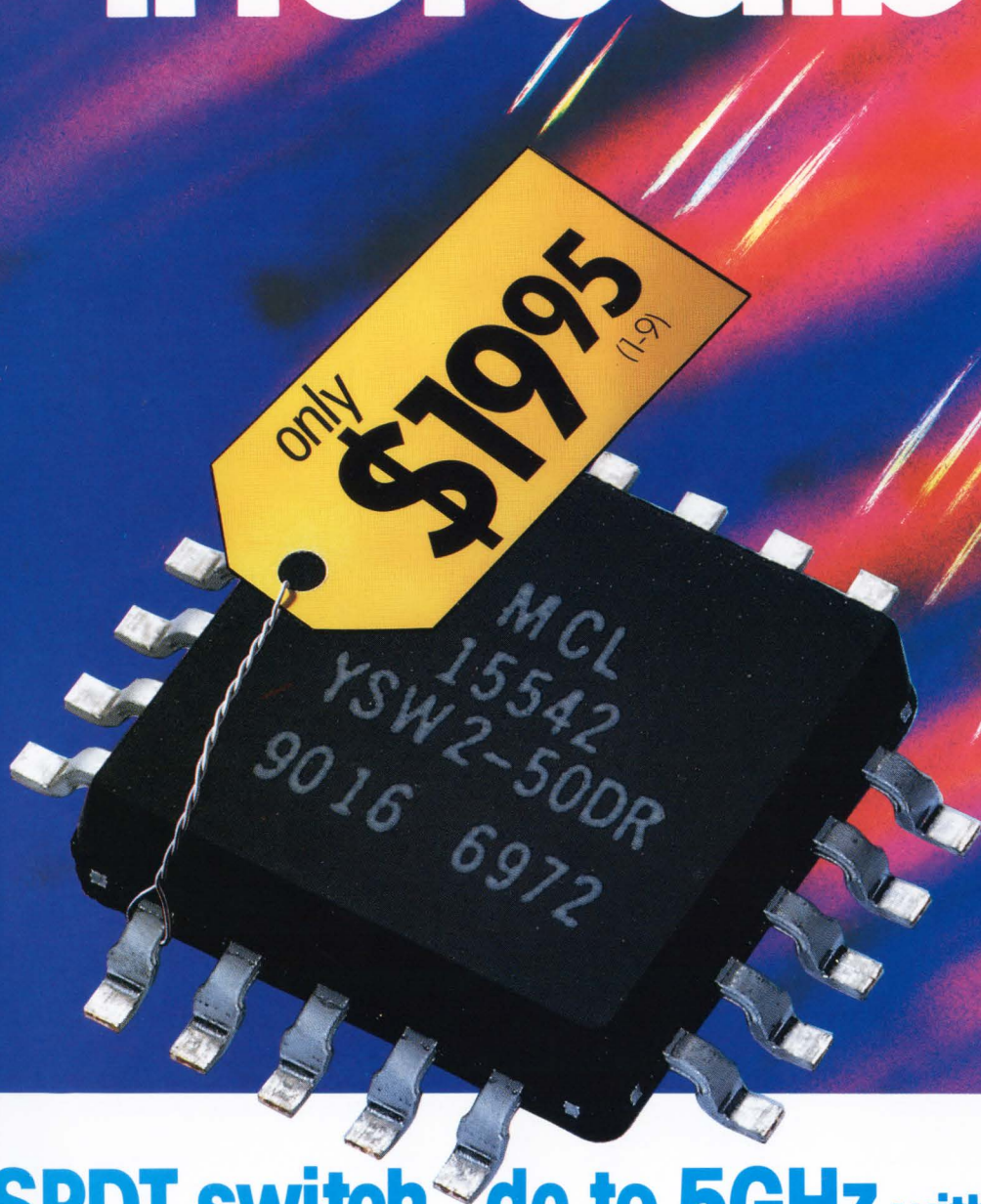
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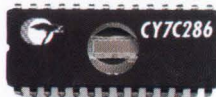
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