

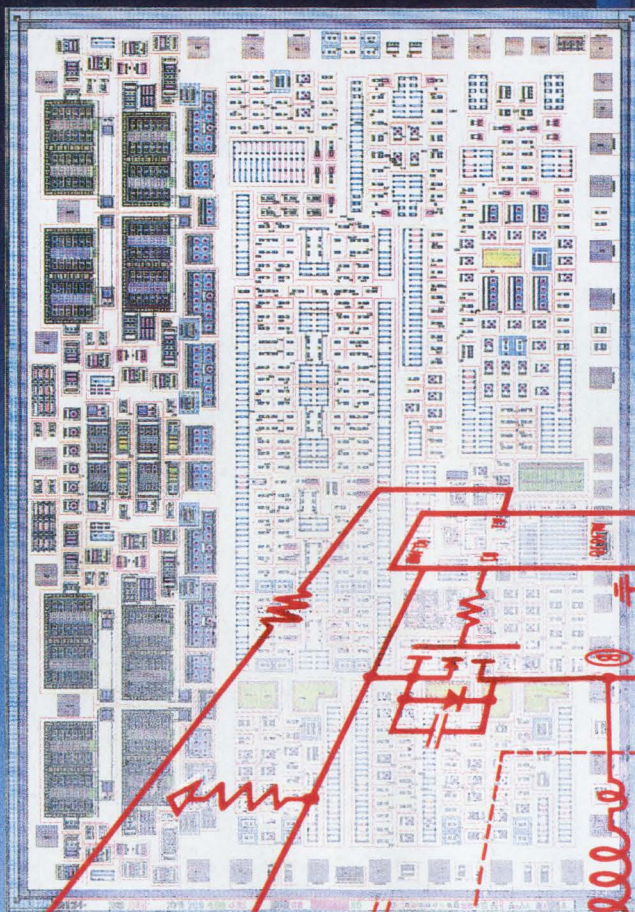
**CONNECTING NON-ISDN TERMINALS TO ISDN  
DELTA-SIGMA ADCs CHALLENGE INTEGRATORS**

FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE

# **ELECTRONIC DESIGN**

A PENTON PUBLICATION U.S. \$5.00

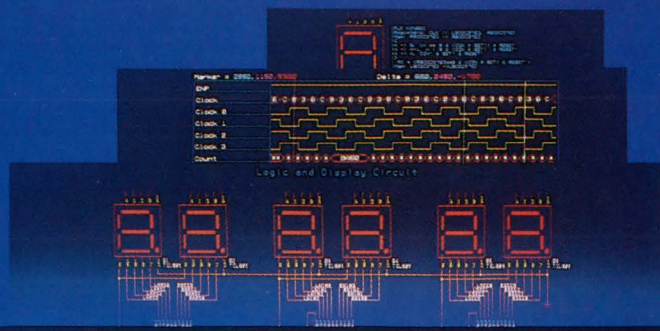
APRIL 25, 1991



**PHASE  
MODULATION  
CUTS  
SWITCHER  
SIZE**

- **SPECIAL REPORT: THE WIDE WORLD OF DYNAMIC RAMs**
- **DESIGNERS' GUIDE TO PACKAGING AND MATERIALS**

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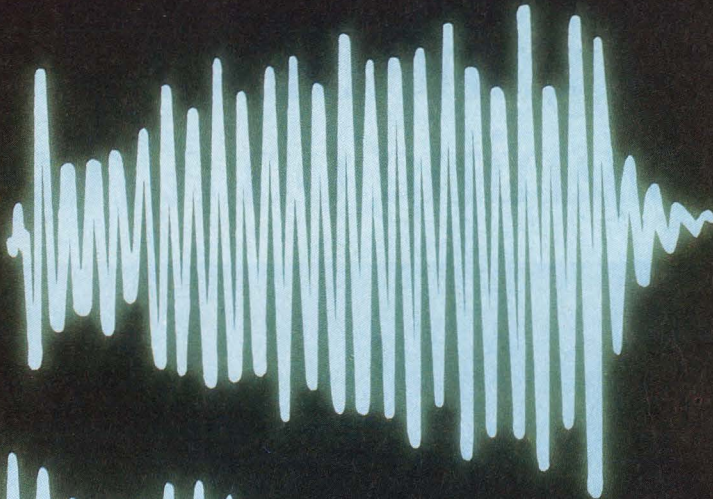
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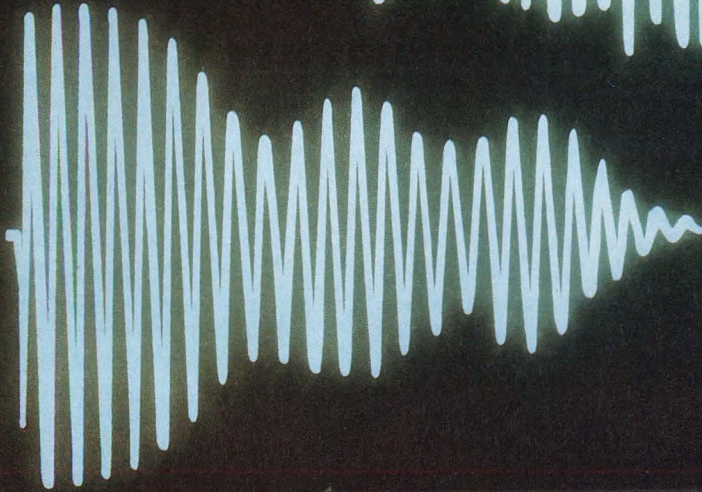
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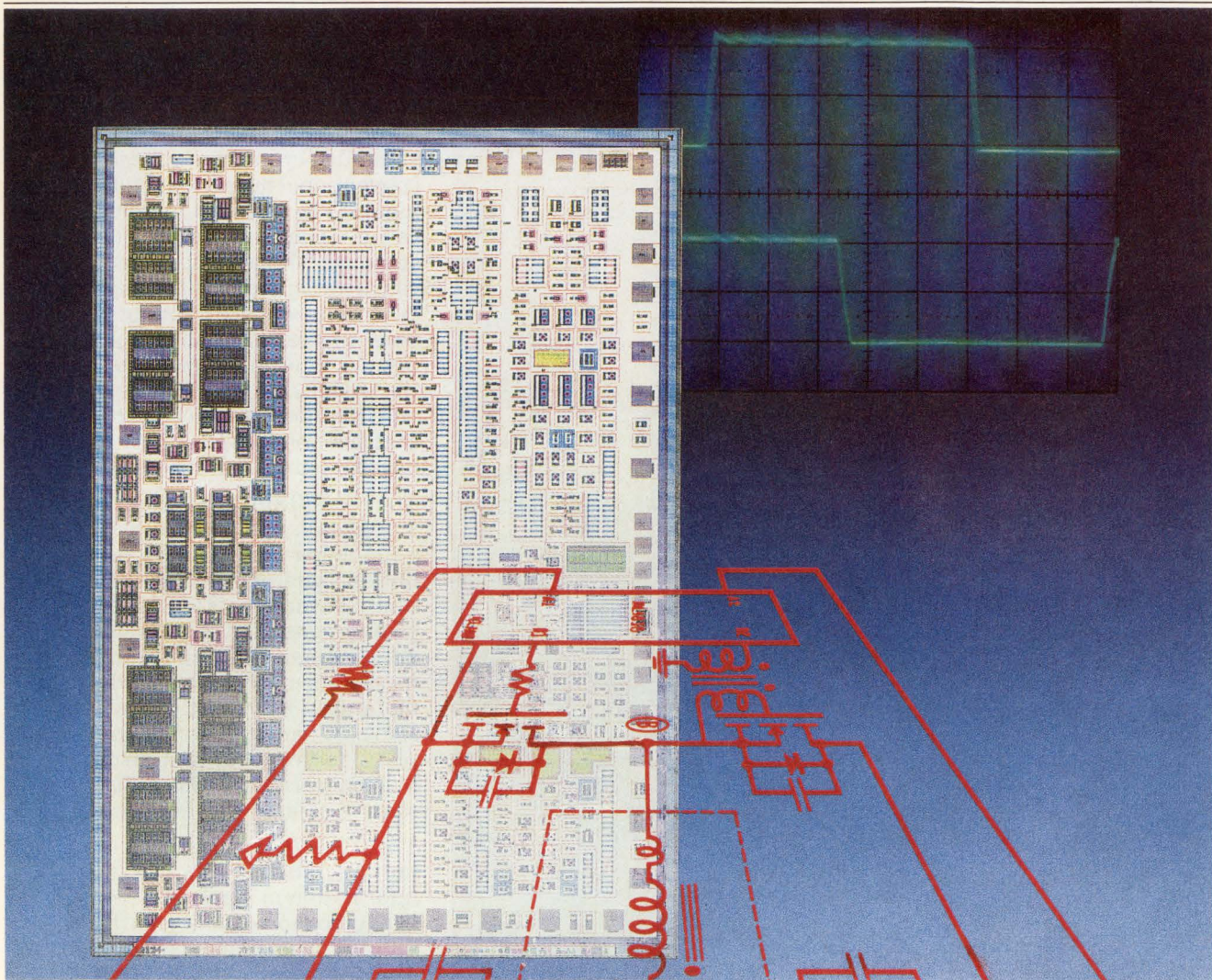


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CIRCLE 115

# ELECTRONIC DESIGN



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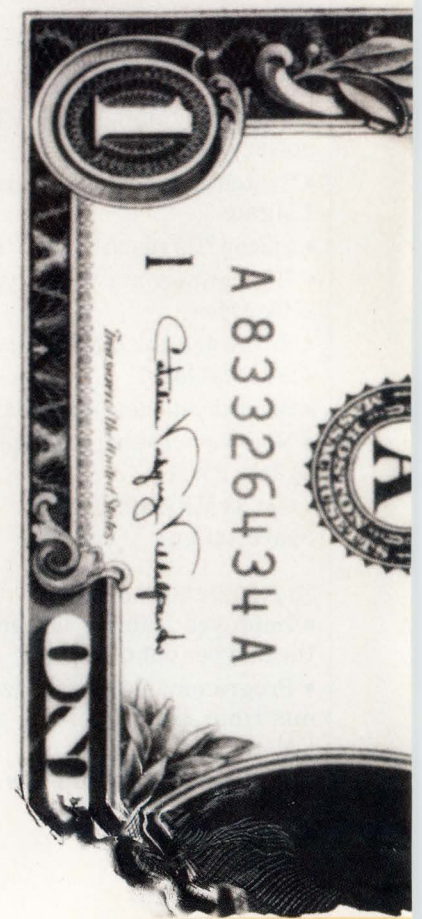
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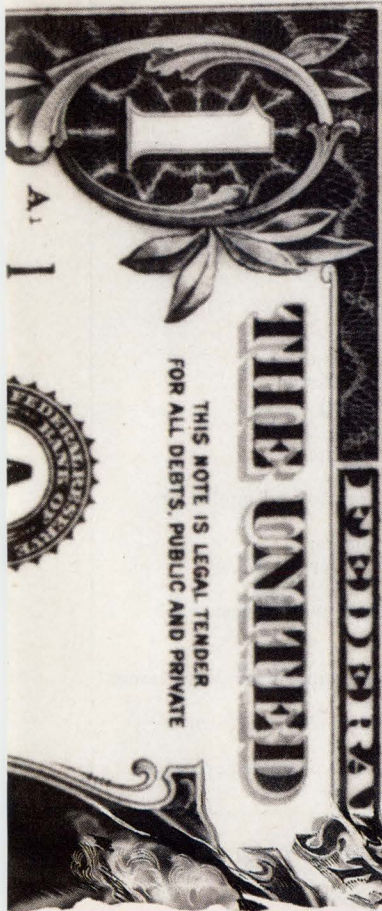
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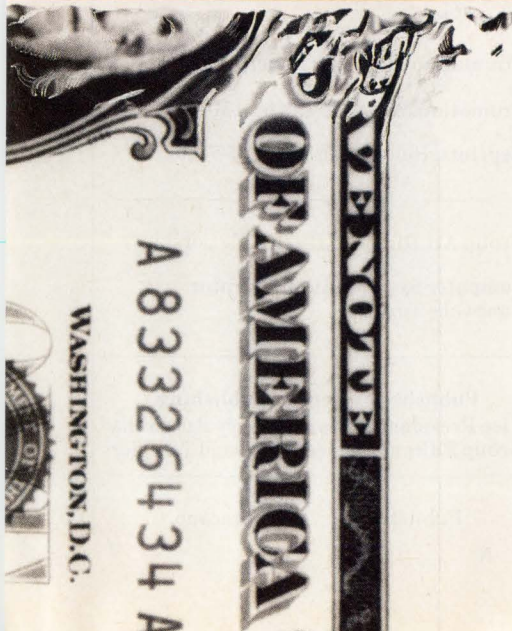
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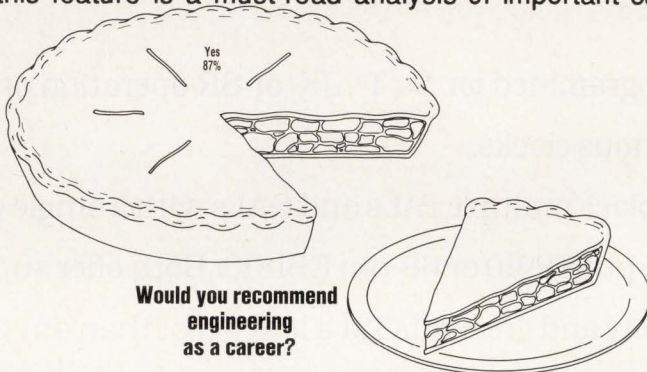
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## Engineers: Are you getting your share of the pie?

The challenges in engineering have never been easy to swallow. But designing in the 1990s will be tougher than ever before as growing competition creates the need for higher quality products and *design-for-manufacturability*.

In the June 13 issue of *Electronic Design*, we survey our readers to find out how engineers are coping with these increased challenges and how satisfied they are with their careers.

Our annual reader study also examines the issues that are uppermost in the minds of design engineers, from time-to-market pressures to designing with components of greater complexity. Presenting data gathered from a survey of our 130,000 domestic readers, this feature is a must-read analysis of important career issues.



Will designing in the 1990s leave you hungry? Find out June 13.

**ELECTRONIC DESIGN: LEADER OF THE PACK  
SINCE 1952**

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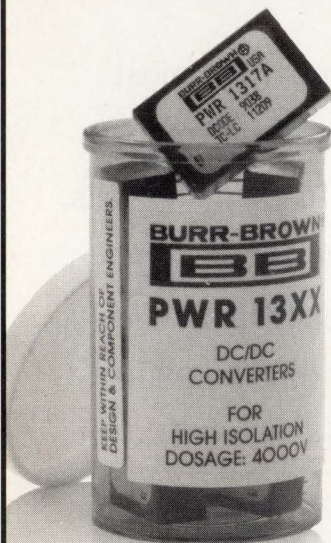
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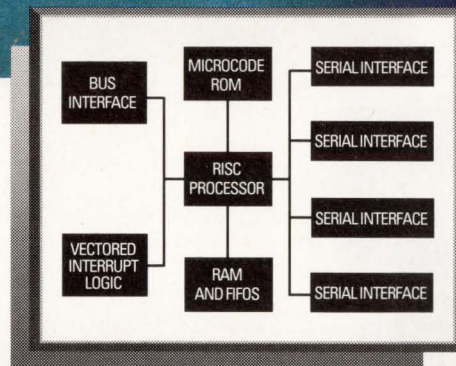
All five types of UNIX-specified parity and error handling. And more.

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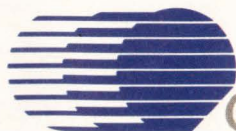
The CL-CD2400 adds synchronous capabilities. It offers 4 independent, multi-protocol channels, plus an on-chip DMA controller for fast, efficient I/O.

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## EDITORIAL

### RICE IS NICE, BUT...

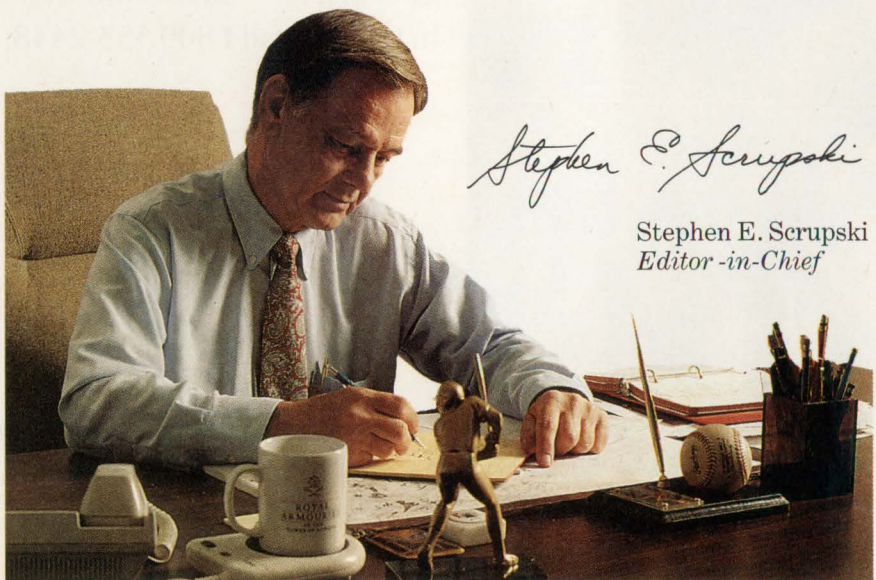
**I** read in the papers where President Bush has been talking to Japanese Prime Minister Kaifu about Japan's barriers to the importation of U.S. rice. Now, don't get us wrong. We're all for U.S. farmers making a buck or two out of the export of their products. And we think it's great that our elected leader is laying it on the line with one of our country's major trading partners. However, we hope he's also thinking about the electronics industry. Our industry is not only the U.S.'s largest employer, its products are the key to the nation's future prosperity as well as its security.

A group called the Council on Competitiveness, headed by retired Admiral Bobby Inman, recently issued a report aimed at President Bush that detailed the areas of technology where the Council feels the U.S. stands strong and where it has lost or is losing badly. Some of the "strong" categories include CAE, systems engineering, microprocessors, applications software, graphics hardware and software, processor architecture, and software engineering. Several areas where the Council feels the game's already over include display materials, gallium arsenide materials, IC fabrication and test equipment, displays, multichip packaging systems, memory chips, and optical information storage.

Looking at these two lists, it's clear that the U.S.'s strengths are in higher, systems-level technologies. Unfortunately, there's a tight linkage between component advances and new system concepts, and implementing these system concepts requires hardware.

Nobody wants the big brother in Washington running our industry. We've already seen how government has mishandled the savings and loan industry and our educational system. Maybe we haven't found the right formula yet—the right combination of government and industry. But sooner, rather than later, the government is going to have to play a part in revitalizing the U.S. electronics industry as it prepares to enter the 21st century. That will mean giving the industry the ability to obtain the capital it needs (and with growing complexity, capital needs grow more exorbitant every day), and putting the nation's best horse-traders to work on international trade negotiations.

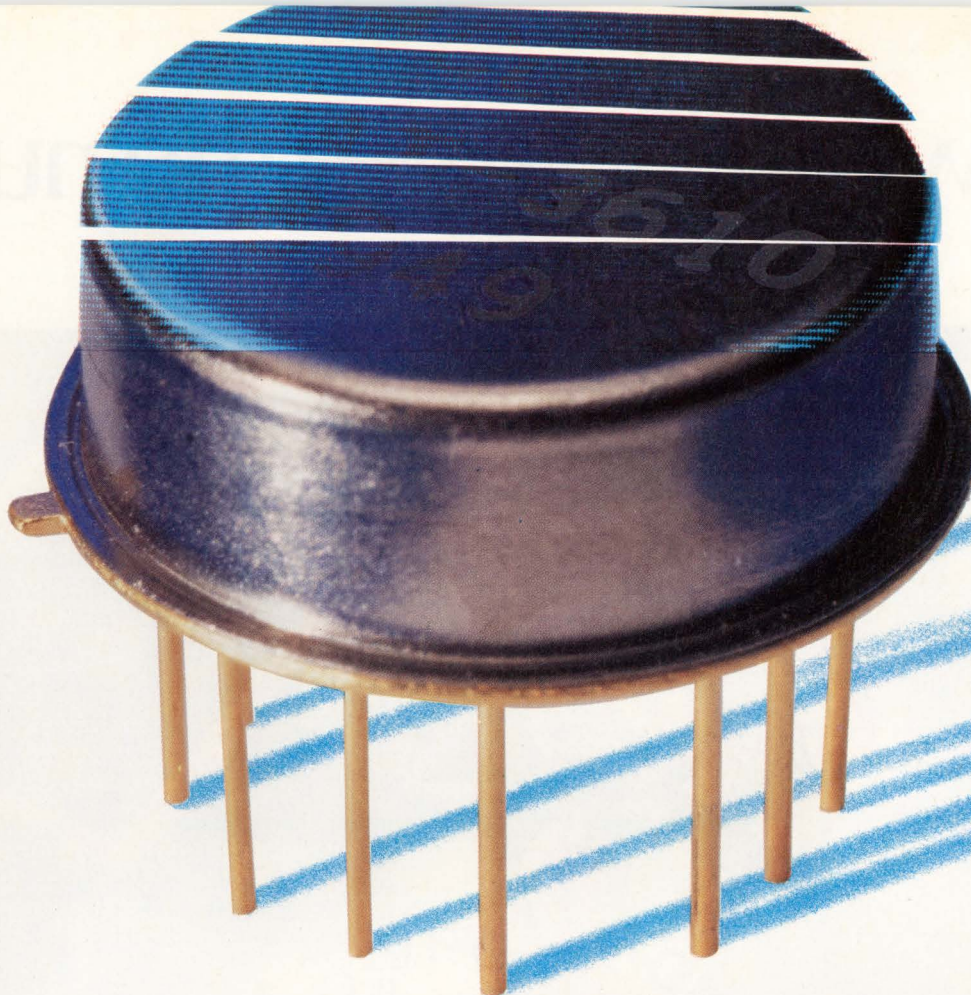
The U.S. and its allies were eminently successful in the recent Gulf conflict. But those laser-guided bombs and Patriot missiles were using years-old hardware. The industry has plenty of ideas and systems expertise for future systems, but you're not going to knock any FutureScuds down with only a concept, any more than you can knock them down with bags of rice.



*Stephen E. Scrupski*

Stephen E. Scrupski  
Editor-in-Chief





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<b>1.0</b>	<b>0.2</b>	<b>2.0</b>	<b>0.2</b>	<b>6.0</b>	<b>0.3</b>	<b>10.0</b>	<b>0.3</b>
1.5	0.32	3.0	0.4	9.0	0.6	15.0	0.6
<b>2.0</b>	<b>0.2</b>	<b>4.0</b>	<b>0.3</b>	<b>10.0</b>	<b>0.3</b>	<b>20.0</b>	<b>0.4</b>
2.5	0.32	5.0	0.5	13.0	0.6	25.0	0.7
3.0	0.4	6.0	0.5	16.0	0.6	30.0	0.7
3.5	0.52	7.0	0.7	19.0	0.9	35.0	1.0

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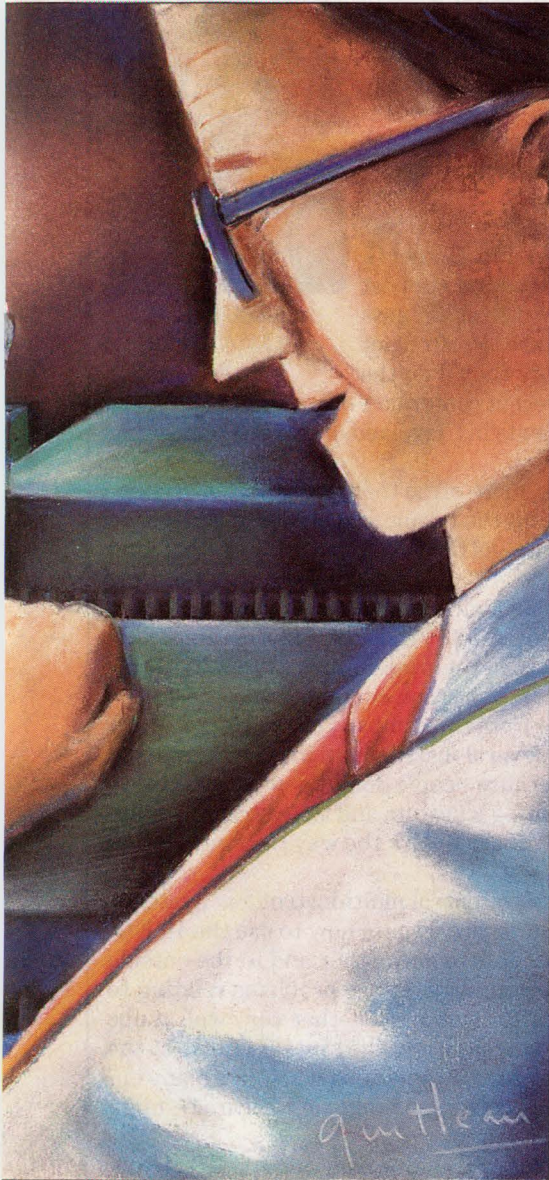
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in a 32-bit design. Which means more engineers to write it, often within very different, even mismatched environments.

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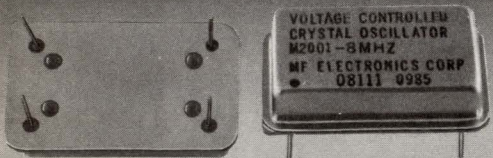


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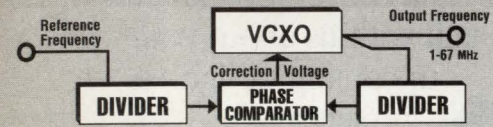
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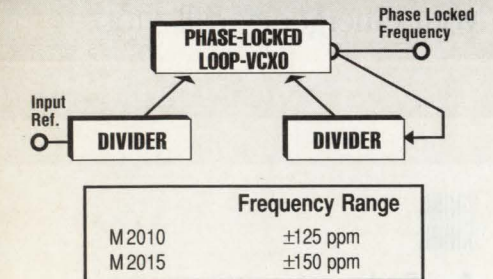
With MF VCXO's, since the specification is computer-tested over the full operating temperatures, you can be assured that the specified frequency- deviation is what you get for capture range.

	Control Voltage	Deviation
M 2001	0.3 to 10V	±175 ppm
M 2002	0.3 to 4V	± 75 ppm
M 2003	0.3 to 10V	±175-300 ppm
M 2004	0.3 to 4V	±125 ppm
M 2005	1.0 to 4V	± 75-300 ppm
M 2006	0 to 5V	±150 ppm
M 2007	0.5 to 4.5V	±125-250 ppm

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### Series M2010, M2015

This is the complete loop, including the phase-comparator and the VCXO, in just one package. Add the dividers to match the frequencies. Oscillators from 10 to 30MHz.



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## PUMP UP THE T&M LEARNING CURVE

It's about time the electronics industry started to think about more formal training in test and measurement techniques. Today's designs are too complex to continue the ad-hoc test practices still found in many companies. Engineering schools have never really taught students to become test engineers. And with curriculums as crowded as they are, the schools aren't likely to improve their T&M instruction.



JOHN NOVELLINO  
TEST & MEASUREMENT

Part of the problem is that some companies see test engineering as an entry-level training ground. Homer G. Hurlbut, Jr., manager of the characterization support branch in Texas Instruments' semiconductor process and design center, feels new engineers are too often put into the test arena because that's where they'll do the least damage. Hurlbut, a panelist at a recent conference on measurement technology sponsored by Keithley Instruments in Cleveland, has some interesting thoughts on the subject.

"Test engineering is a learning track, more often than not, where new engineers learn what the company does, learn the people and the faces and where they come from, and what wafers look like and the variations in them—that kind of thing," says Hurlbut. "By the time we get a fairly competent test engineer who's digging right into it, we turn around and say, 'Wouldn't you like to be a circuit designer? Or wouldn't you like to get into production engineering?'"

John Pesec, Keithley's manager of customer service, confirms the need to provide more training in T&M. Pesec's four application engineers take 400 calls a week, mostly from customers, but also from the company's sales force. Many calls result from attempts to connect several instruments into an automated setup. "We get a lot of general calls because people don't know where else to turn," says Pesec. "They are implementing a system and they hook up equipment from five different vendors, but it doesn't work the way the five vendors said it should."

Because PCs are used more and more to control multi-instrument systems, the fastest growing area of concern is interface issues—how to use the IEEE-488 bus to connect multivendor instruments to each other and to the outside world. But software questions are also abundant, as are problems relating to computer speeds. A group of instruments may work together very well at one speed, but users then upgrade their controllers and the system falters at the higher speed. Properly grounding a test setup is another area where many engineers are left clueless, especially when they're making high-accuracy, high-resolution measurements at low levels.

Because we can't expect much help from the engineering schools, T&M vendors will have to take an active role in educating their customers, and prospective customers. Hurlbut cites the Japanese practice of extended support and training that comes with major equipment purchases.

"One of the things that the Japanese do better than we do, and they do a lot better than we do, is they support their equipment until the user knows everything about it," says Hurlbut. "The people who supply the equipment come in, gown up, go into the clean rooms, and spend as much as six months to a year with that equipment on the customer's site. When they get through, that piece of equipment works in the environment that it needs to work in."

He acknowledges that "the first 50 things that go wrong are probably my folks trying to understand the equipment." But that's all the more reason the vendor should make available someone who can work with his people and answer questions that arise in the unit's operating environment. Besides, the communication is bidirectional, also helping the vendor's representatives. "They get the feedback that helps them understand what the user needs and what the user wants in the user's environment," notes Hurlbut.

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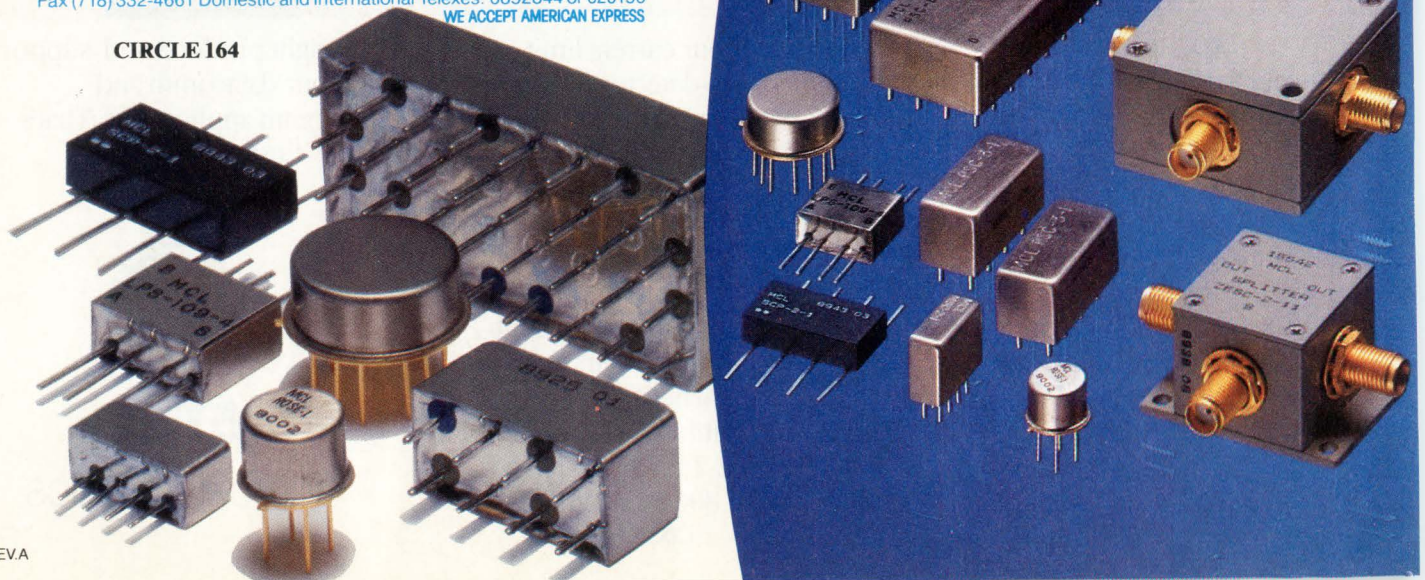
For detailed specs and performance data, refer to the *MicroWaves Product Directory*, *EEM* or *Mini-Circuits RF/IF Signal Processing Handbook, Vol. II*. Or contact us for our free 68-page *RF/IF Signal Processing Guide*.

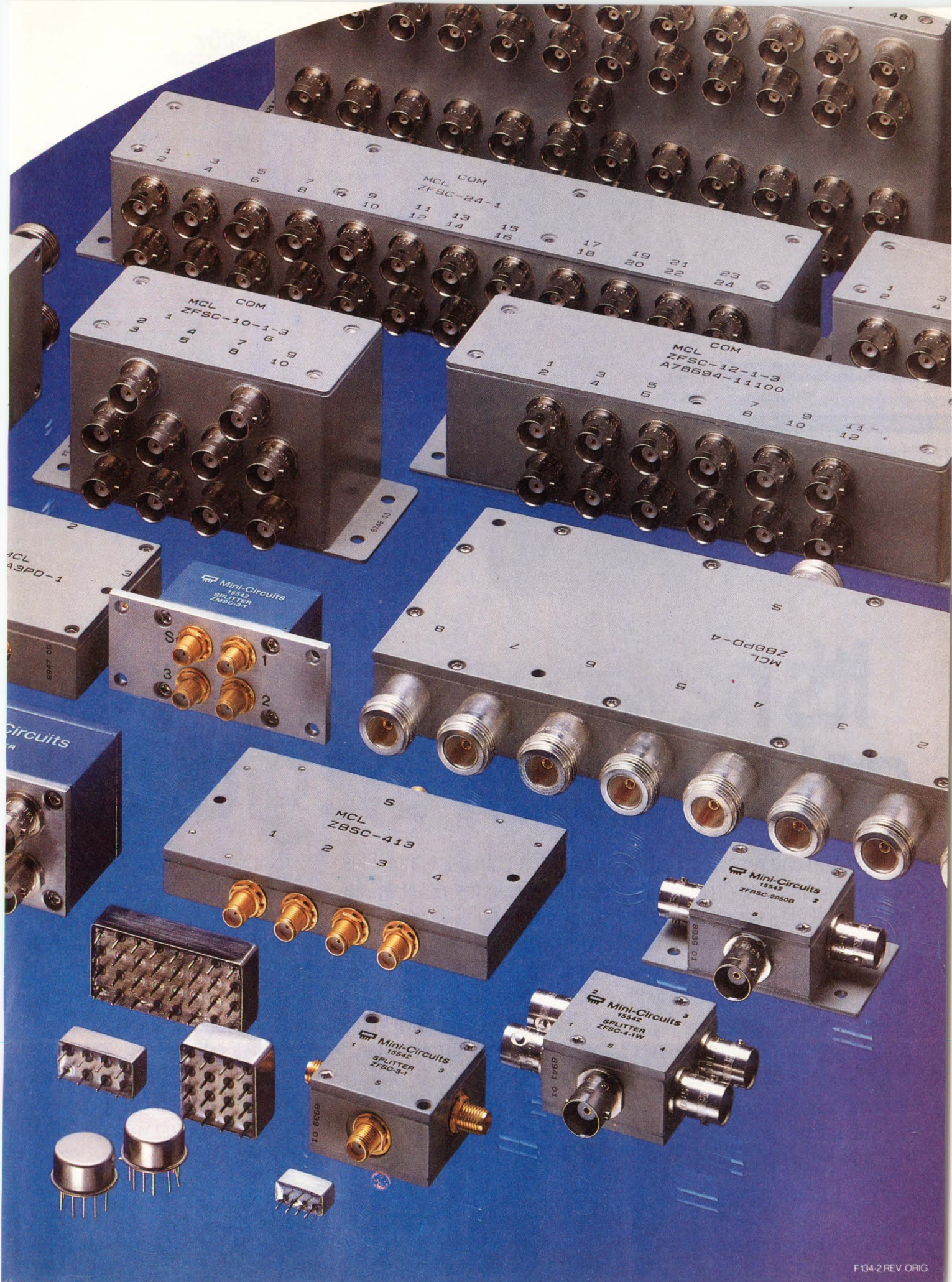
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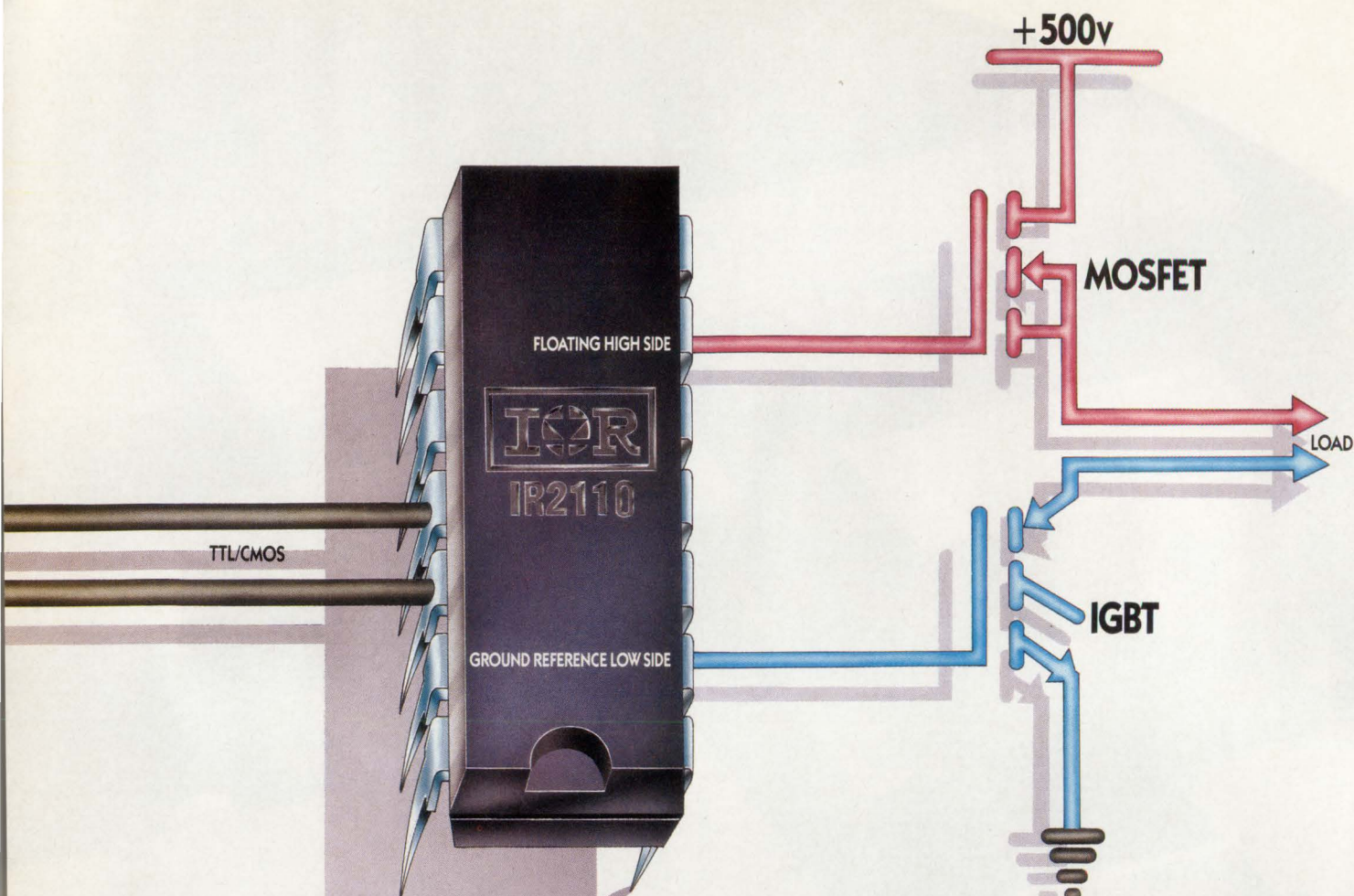
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**PHASE MODULATION RUNS  
PWM POWER SWITCHERS**

Full-bridge, switch-mode power supplies larger than about 500 W, which moved from PWM to resonant-mode topologies early on, are now switching to a new topology. The topology's name is undecided so far—Unitrode Corp., Merrimack, N.H. calls it phase-controlled PWM; Micro Linear Corp., San Jose, Calif., simply dubs it phase modulation (see "Phase Modulation Cuts Large Switcher Losses," p. 39). Both companies are announcing IC controllers for the topology. The technique combines the advantages of resonant mode (low-loss zero-voltage switching at high frequencies) with those of PWM (high-power-per-pulse, constant-frequency, square-wave switching). It eliminates peak voltage and current stress on the DMOS power switches, permitting minimum-rated FETs, thus reducing cost. Unitrode points out that phase-controlled PWM actually employs resonant-mode techniques to achieve its zero-voltage switching. The controller can run voltage or current mode at frequencies to 2 MHz. In general, the larger the supply the lower the operating frequency. The chip's 2.5 V  $\pm 1\%$  reference holds within  $\pm 0.8\%$  over input voltage change and temperature. In quantities of 1000, the commercial-grade UC3875 controller runs \$4.50 each. For additional information, call Joe Papalardo (603) 424-2410. *FG*

**SWITCH EXPANDS ASIC  
EMULATORS TO 1 MGATE**

A switching matrix that routes the 4000-plus signals between multiple ASIC emulation systems will make it possible for circuit emulations to reach 1 million gates. Up to 20 of Quickturn Systems' emulators (the RPM series), each with capacities from 10,000 to 50,000 gates, can be tied together and operated as one large emulator. Each RPM emulator from the Mountain View, Calif. company basically consists of a group of Xilinx field-programmable RAM-based logic arrays onto which any circuit pattern can be mapped for emulation purposes. Another modular RPM enhancement is the software package called OneView. It controls the emulation activity and displays the emulation data through one workstation window. The OneView software also helps a designer partition large net lists across several RPM systems. To handle the switching of over 4000 signal paths, Quickturn engineers employ, again, the RAM-based reprogrammable arrays from Xilinx. Switch programming details are downloaded through the RPMs, which are attached to the interconnection module that holds the crosspoint switch. The OneView software runs on Sun workstation families. Contact Quickturn at (415) 967-3300. *DB*

**SILICON ICs REACH  
24 GBIT/S SPEEDS**

To demonstrate silicon's usefulness in high-speed integrated circuits, researchers at the Ruhr University in Bochum, Germany, designed a number of basic ICs operating at data rates up to 24 Gbit/s. According to Hans-Martin Rein, a professor in the school's electrical-engineering department, this is the highest speed reported so far for silicon-based ICs. The devices were fabricated at Hewlett-Packard, Palo Alto, Calif., using the company's advanced silicon bipolar technology called HP 25. Some of the experimental circuits developed include a time-division multiplexer and a regenerating demultiplexer, both operating at up to 24 Gbit/s. A combination of these two ICs resulted in a parallel-operating decision circuit that ran at 23 Gbit/s. In addition, a data rate of 15 Gbit/s was achieved for a standard decision circuit. All devices were designed with a view toward applications in optical-fiber transmission systems and measuring equipment. Only devices using gallium arsenide material have matched or surpassed these rates. "There's no doubt that the records achieved are still far from the speed limits for silicon," says Rein. "They will be improved upon in the near future by using more advanced silicon technologies." *JG*

**HIGH GATE-COUNT ARRAYS  
YIELD UP TO 250K GATES**

Combining 0.8- $\mu$ m minimum feature sizes with sea-of-gates architectures, two families of CMOS gate arrays pack some of the highest gate counts in the industry—between 302,000 to 400,000 total gates. One family, the M6008X series from Mitsubishi Electronics America Inc., Sunnyvale, Calif., also claims the highest I/O count—576 pins—thanks to tape-automated bonding on a special quad-sided flat package. The other family, the TC160G series from the ASIC Div. of Toshiba America Electronic Components Inc., Sunnyvale, Calif., offers as many as 416 I/O pins.

Mitsubishi employs a triple-level metal process that pushes the utilization to about 60%, yielding nearly 250,000 usable gates on the largest chip. The small features enable the gates to operate at frequencies of up to 100 MHz. However, with so many active gates on a chip, even CMOS power levels start to climb. Consequently, Mitsubishi designers allowed for an optional heat sink, so that the high-pin-count packages could dissipate as much as 22 W. One way that

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the company tries to compensate for the higher power is by giving the designer four speed/power options for most cells in the library. Thus, designers can optimize for gate delays as short as 215 ps for lightly loaded gates or power dissipations as low as  $6 \mu\text{W}/\text{MHz}/\text{gate}$ . A double-metal process currently used by Toshiba on its arrays limits gate utilization to approximately 40% of the total gate count, yielding about 120,000 usable gates from the 302,000-gate chip. The company is developing a triple-level-metal process to improve the on-chip interconnection ability. Typical gate delays are about 300 ps for a lightly loaded gate. For details, contact Mitsubishi at (408) 730-5900, and Toshiba at (408) 733-3223. *DB*

## SOFTWARE AUTOMATICALLY INSERTS JTAG TEST LOGIC

Once a design is completed, designers can typically insert boundary-scan logic, such as that defined by the JTAG standard (now IEEE 1149.1). However, it's often difficult to backtrack and add that logic in. The release of a software package, NetTag, by Gould AMI Semiconductors Inc., Pocatello, Idaho, now eliminates the retrofitting headache. It claims to be the first commercial package (used with the company's own ASIC cell library) to automate the insertion of boundary-scan circuitry, the test-access-port controller, and the four or five dedicated test pins. The software can also automatically serialize the parallel functional-test patterns. By automating the scan insertion, substantial time can be saved in bringing a chip to market. It also simplifies the "design-for-test" issues during chip development. The NetTag package is part of the company's expert system design environment that includes the established NetTrans package, a universal net-list translator, and NetScan, a scan-path insertion and test-generation tool. All three tools can be used together to import a design from another library, insert internal scan-path logic, and then add 1149.1 boundary-scan logic. Contact Mark Alexander at (209) 586-7422. *DB*

## SCHOTTKY DIODES OF GERMANIUM?

A series of germanium Schottky diodes that operate reliably at 125°C has been developed by Germanium Power Devices, Andover, Mass. These diodes have lower voltage drops than silicon Schottky diodes. At 25°C, a typical germanium device has forward drops of 0.28, 0.36, and 0.42 V at forward currents of 20, 60, and 100 A, respectively. In comparison, equivalent silicon rectifiers at the same currents show forward drops of 0.4, 0.54, and 0.65, respectively. What's more, at 100°C, the diodes' forward-voltage drop decreases by another 0.1 V, while silicon's forward drop changes little at elevated temperatures, according to Germanium Power Devices president Oliver Ward. The low forward drop is the result of germanium's lower bandgap, as well as the company's advanced processing techniques. The diode chips, which measure 200 mils on a side, will find homes as the output rectifiers in high-current, low-voltage (5 V and below) switching power supplies, as well as in the "ORing" circuits used when the supplies are paralleled. For additional information, call Rick Kassiotis at (508) 475-5982. *FG*

## NON-WOVEN SUBSTRATE MAKES LIGHTER PWBs

A non-woven, paper-based substrate made from 100% aramid fiber promises significant performance advantages compared with existing fiber-glass substrates for printed-wiring boards. Lower dielectric constants, a smoother mounting surface, uniform thickness, and lighter-weight boards can be made with the Thermount reinforcement material from DuPont Electronics, Wilmington, Del. Now in its final development stage, the material will particularly suit boards with high circuit and package densities, using fine-pitch surface-mounted devices or direct-chip-attach assemblies. Call DuPont at (800) 453-8527, ext. 10. *DM*

## GET 33 MFLOPS FROM A SPARCSTATION

The arrival of an enhancement board will help users upgrade their SBus-compatible computers. The Spirit-30 DSP boards developed by Sonitech International Inc., Wellesley, Mass., can perform up to a 33 MFLOPS for real-time signal processing or application acceleration. Without the board, a Sparcstation 2 typically processes about 4 MFLOPS. The Spirit-30, designed around Texas Instruments' TMS320C30 DSP chip, plugs into one SBus slot. Up to eight Spirit-30 boards can be daisy-chained together to further increase performance. Each board transfers data over the SBus through its 32-bit interface at 25 Mbytes/s, and they carry from 256 kbytes to 2 Mbytes of zero-wait-state static RAM. It also dissipates 8 W of power. Application-specific modules are accepted to link with audio and video sources. The company's next generation of boards, due out in about three months, will upgrade to TI's TMS320C40 processor. *RN*

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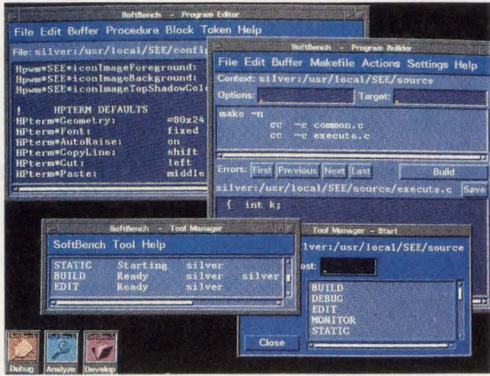
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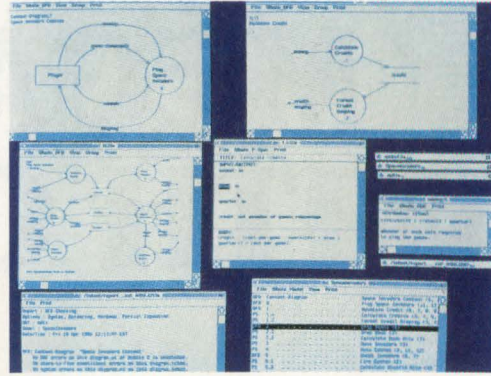


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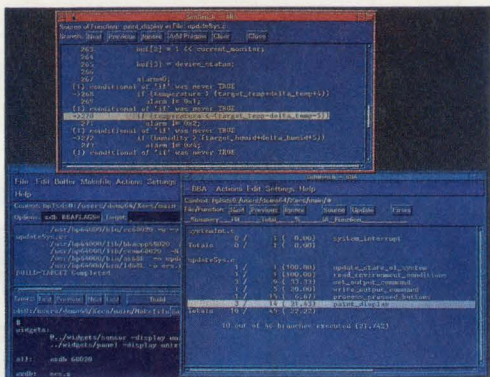
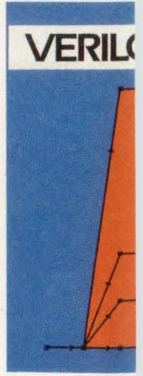
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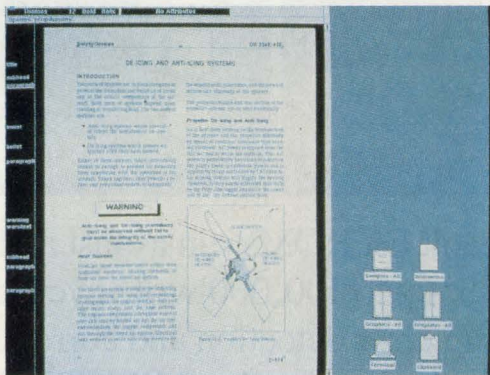


Cadre Teamwork: A family of tools that implement system analysis and software design methodologies.

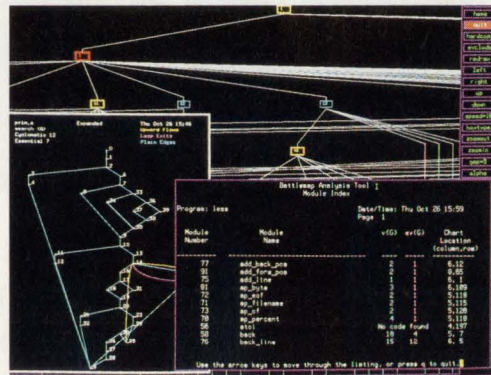


HP Branch Validator: Provides accurate branch information quickly and easily, reducing software test time while increasing confidence.

# Best CA

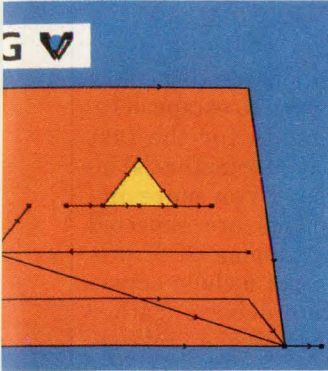


Interleaf Technical Publishing Software: A documentation software and management system that features integrated text and graphics.

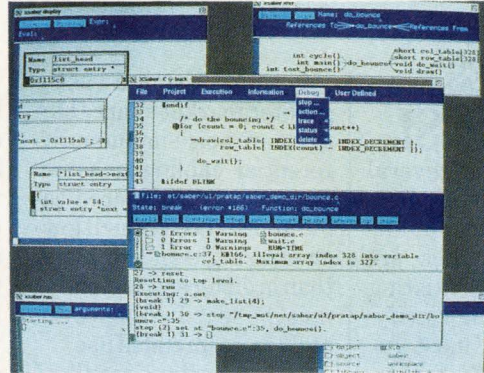


McCabe Test Tools: An automated software testing and reverse engineering application.

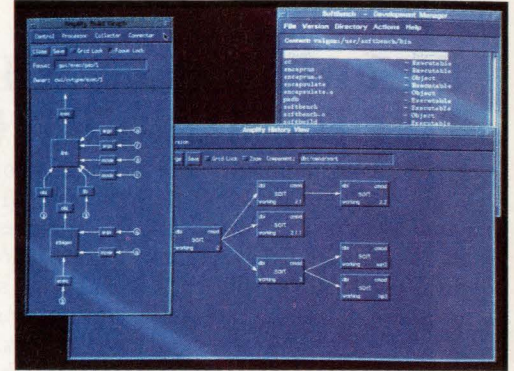




**Verilog LOGISCOPE:**  
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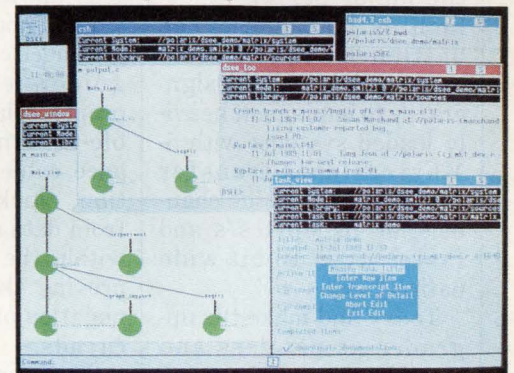


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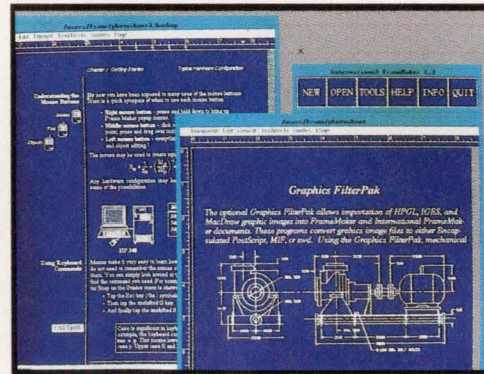
# SE scenario.



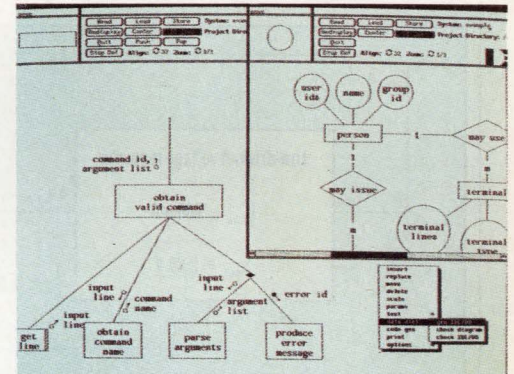
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## IMPROVED CABLING SCHEMES TAKE THE MAYBES OUT OF SCSI

The least-controllable portion of the Small Computer Systems Interface (SCSI) standard—the cables that connect the drives to the system or host adapter—has been showered with much attention lately. This is because those cables now are the major performance-limiting bottleneck. The bottleneck has become more apparent as designers try to implement heavily loaded systems with 5-Mbyte/s data-transfer rates over byte-wide channels, or 10 Mbytes/s and faster over 16-bit-wide paths.

To try and make the upgrades as painless and smooth as possible, members of the X3T9.2 task group within the SCSI standardization committee

recently completed several theoretical and experimental studies on cable designs. Those studies are changing several existing conceptions, while clarifying others. But most important, the study has resulted in a set of cabling guidelines to help companies implement reliable, longer, higher-speed single-ended connections. The guidelines include the proper relationship of cable-to-terminator impedance, cable signal attenuation, clock line isolation from data and parity lines within the cable, and improving the active signal negation of the line-driver circuits.

Single-ended cabling has been a focal point of the committee. Its lower cost, lower power, and reduced

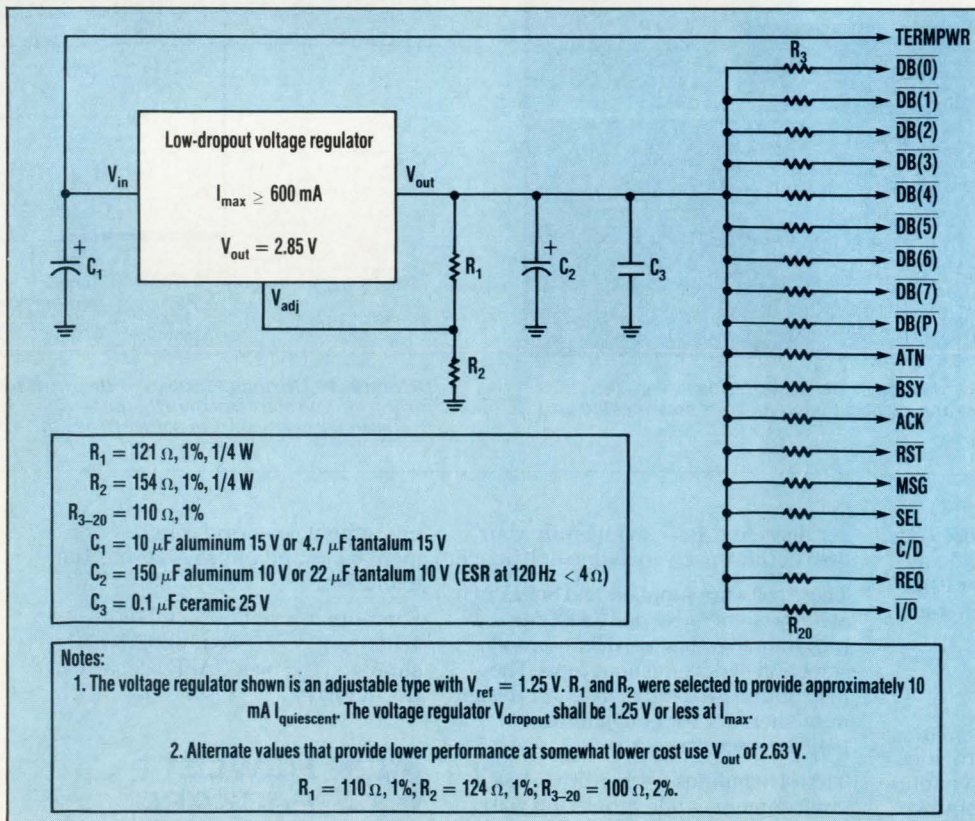
chip count give it a vastly greater market share than the more noise-immune differential cabling scheme. Because the measured cable impedance is much lower in single-ended mode than in differential mode, it must be specified appropriately to its intended use.

One important result of the studies is a “standard” or recommended design for a shielded, twisted-pair cable that meets most needs of both single-ended and differential SCSI systems. That cable, which is also practical for customized assemblies, is reasonably economical and widely available from quality cable suppliers. With such a cable, good operation of fully loaded single-ended SCSI buses can be obtained for cable lengths well above 6 meters in both the asynchronous or synchronous modes.

Additional testing is now being done to establish requirements for the fast SCSI (10 Mtransfers/s) interface. Even more improvements are expected as forthcoming SCSI protocol chips include active-negation drivers (rather than the prevalent release-on-negation drivers). Extensive use of controlled-rate ramping in the drivers will also improve bus performance by reducing overshoot and ringing. Furthermore, similar benefits may come from using clamp diodes in the terminators, a scheme that IBM has proposed at the most recent committee meeting.

One of the major problems with the single-ended SCSI is the double-clocking of the Request or Acknowledge signals due to noise coupled from data-line switching. One recommended solution provides crosstalk isolation within the cable by placing the REQ and ACK signal pairs in the core of the cable, and the data and parity pairs in the outer layer. That allows for a buffer layer of inactive-signal pairs during data transfers in between the data and parity signals and the REQ and ACK signals. However, to build such cables requires a level of assembly control that’s not widely employed in the industry today. It also requires an 18-pair outer layer in the new “P” cable standard (the P cable is a 16-bit single-cable interface defined by the X3T9.2 committee).

The biggest problem, though, is the large asymmetry of received signals in single-ended cabling schemes. It turns out that such problems are best





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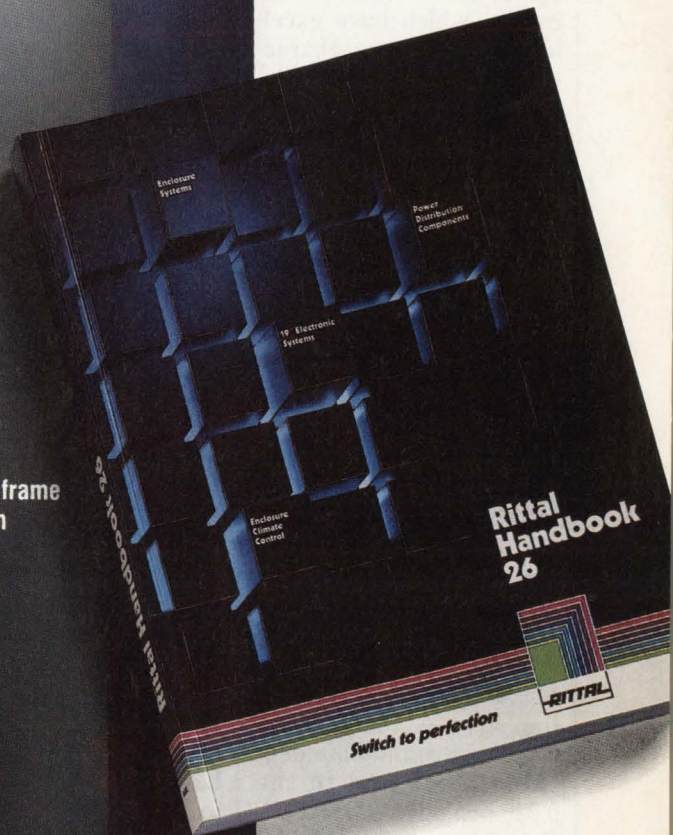
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dealt with if the single-ended cable impedance is less than the impedance of the terminator by about 25%. The original 220/330- $\Omega$  resistor-network terminators, with an impedance of 132  $\Omega$ , work best with cables whose single-ended impedance is in the range of 100  $\Omega$ . The only widely used cable of that type is the 0.050-in. pitch AWG 28 PVC coated ribbon cables. But buses employing the AWG 28 PVC coated cables are typically so short that they don't require optimized terminator impedance matching.

For longer buses, shielded twisted-pair cables can be had with impedances of up to 90  $\Omega$ . Most of these cables, which have excellent performance characteristics (low loss, low delay), typically employ foamed dielectrics (100  $\Omega$  if AWG 30 conductors are used). The foam dielectric, however, may be difficult to handle for many cable assemblers who prefer the solid-dielectric cables.

To create the best solution, the committee developed a way to take advantage of the lower impedance and better control of open-circuit voltage of the 110- $\Omega$  regulated terminator (see the figure). The control scheme is being introduced as part of the SCSI-2 standard and now in full commercial production. It's ideally matched to the so-called 80- $\Omega$  SCSI-standard-round-shielded-cable stock and to the 0.025-in pitch AWG 30 PVC flat-ribbon-cable stock preferred for the high-density SCSI connectors. And, unlike the original 220/330- $\Omega$  terminators, its performance doesn't change if the Terminator Power line

voltage changes on the SCSI bus.

The 110- $\Omega$  terminator also works well with the 90- $\Omega$  cables. Several companies have successfully used that combination. For better impedance matching of the 110- $\Omega$  terminator and the 0.050-in.-pitch ribbon cable, PVC insulation and AWG 26 conductors can be specified. But in long twisted-pair round shielded cables, PVC insulation produces unacceptably low impedance and high attenuation cables.

The previously mentioned 80- $\Omega$  SCSI standard cable incorporates 25 twisted pairs of AWG 28 conductors, 7/36 stranded, with solid polyolefin (poly-

propylene or polyethylene) insulation to 0.033-to-0.025 diameter. That bundle of cables is wrapped in a polyolefin-based tape buffer layer, which provides a low-capacitance isolation of the outer pairs from the overall shield layers.

Examples of such cables include the Astro model 52-107-C, Berk-Tek 271212, C&M C801/25, Hitachi 8213, Madison 4099 and 4179, Montrose 7251, and NEK J0517-1. They have single-ended impedances of about 80  $\Omega$  and differential impedances of 120  $\Omega$ , and their attenuations of the SCSI signals are acceptably low. The cable performance can still be poor if the cable manufac-

turer doesn't pay attention to small details, such as making sure the twist pitch of the twisted-wire pairs is uniform so that signal skew down the cable is minimized.

The new cabling information will be included in the upcoming SCSI-3 parallel interface draft document that's scheduled to be available in June from Global Engineering Documents (800) 854-7179, or (714) 261-1455. For details about participating on the SCSI-3 project, contact John Lohmeyer of NCR Corp., Wichita, Kans., chairman of the X3T9.2 committee, at (316) 636-8703.

DAVE BURSKEY

## PROGRAMMABLE TO 15 MHz, CONTINUOUS-TIME Gm/C FILTERS MOVE TO CMOS

**V**oltage-programmable, continuous-time IC filters have been built by academia, and described at conferences like ISSCC, for at least 10 years. However, the first commercial devices appeared just last year from International Microelectronic Products (IMP), San Jose, Calif., and Silicon Systems Inc. (SSI), Tustin, Calif. (ELECTRONIC DESIGN, Feb. 8, 1990, p. 43). Now it looks like their time has come. At next month's Custom IC Conference (CICC) in San Diego (May 12-15), SSI will describe a new bipolar IC filter that has cutoff frequencies programmable between 2 and 10 MHz. The company recently announced another four frequencies between 1.5 and 8 MHz. IMP, on the other hand, has now built a new one in CMOS.

To date, all of these fil-

ters aim at the read-channel circuits for signals coming off magnetic media, particularly from hard disks employing constant-density (zone-bit) recording. However, IMP feels that the architecture of its latest device (the first of a family) lends itself to general-purpose applications including image enhancement, antialiasing, and telecommunications. The filter uses a Gm/C architecture, and the cutoff frequency of its biquads can be digitally programmed from 1.5 to 15 MHz.

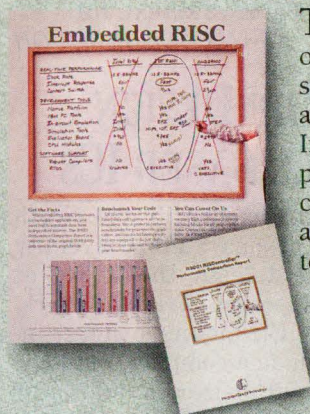
A Gm/C filter starts with a transconductance (Gm) amplifier, adds an integrating capacitor (C) to the output, and provides feedback from output to input. A filter pole is created at -Gm/C. Changing the amplifier's transconductance by changing its dc bias, or changing the load

capacitance, changes the filter's cutoff frequency. Low-, high- and all-pass filters can be built and individual stages cascaded to provide additional attenuation, and/or to create band-pass or band-reject responses. Virtually all common filter topologies (Butterworth, Chebyshev, Bessel) are practical.

IMP's IMP4255 contains a sixth-order low-pass Bessel section, a fourth-order all-pass section, and a pulse-slimming section that can be looked upon as an adjustable high-frequency boost stage capable of providing up to 9 dB of gain. Bessel filters are known for their slow, smooth roll-off, which results in minimum overshoot when handling pulses and linear-phase response in the frequency domain. The latter can also be expressed as minimum,

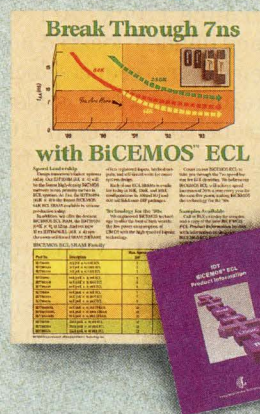
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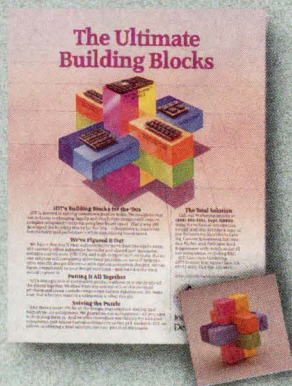
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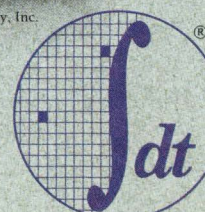
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differential group delay. It runs just 1 ns maximum from 1.5 to 15 MHz with the all-pass section (which can add phase correction) disabled. Coarse cutoff-frequency adjustment is made by switching the capacitance at the output of each Gm/C stage. For fine adjustment, each stage's dc bias is altered.

At the heart of the chip is a digital phase-lock loop (PLL). Its tuning element is a Gm/C biquad, identical to those forming the filter. The PLL tracks a reference clock from the host. The dc output of the PLL is applied to the bias inputs of the Gm/C amplifiers and the output of the up-down counter in the PLL switches their load capacitors as

it switches the capacitors in its biquad to track the reference clock. A frequency divider, located between the reference-clock input and the PLL, is also controlled by the serial I/O to further program the filter's cutoff frequencies. Each section's response is independently variable from 0.12 to 1.5 times the reference-clock frequency. The PLL ensures that changes in amplifier Gm or load capacitance, with temperature, time, or supply voltage, will not change performance—particularly cutoff frequency.

The IMP4255 runs off a 5-V rail and comes in a 16-pin SOIC and a DIP. In lots of 1-99, pricing starts at \$15 each. An evaluation sys-

tem for the filter (and future family members), and filter-synthesis software, will soon be available. Call

Michele Drgon at IMP, (408) 434-9100, or SSI at 1-(800) 624-8999 ext. 151.

FRANK GOODENOUGH

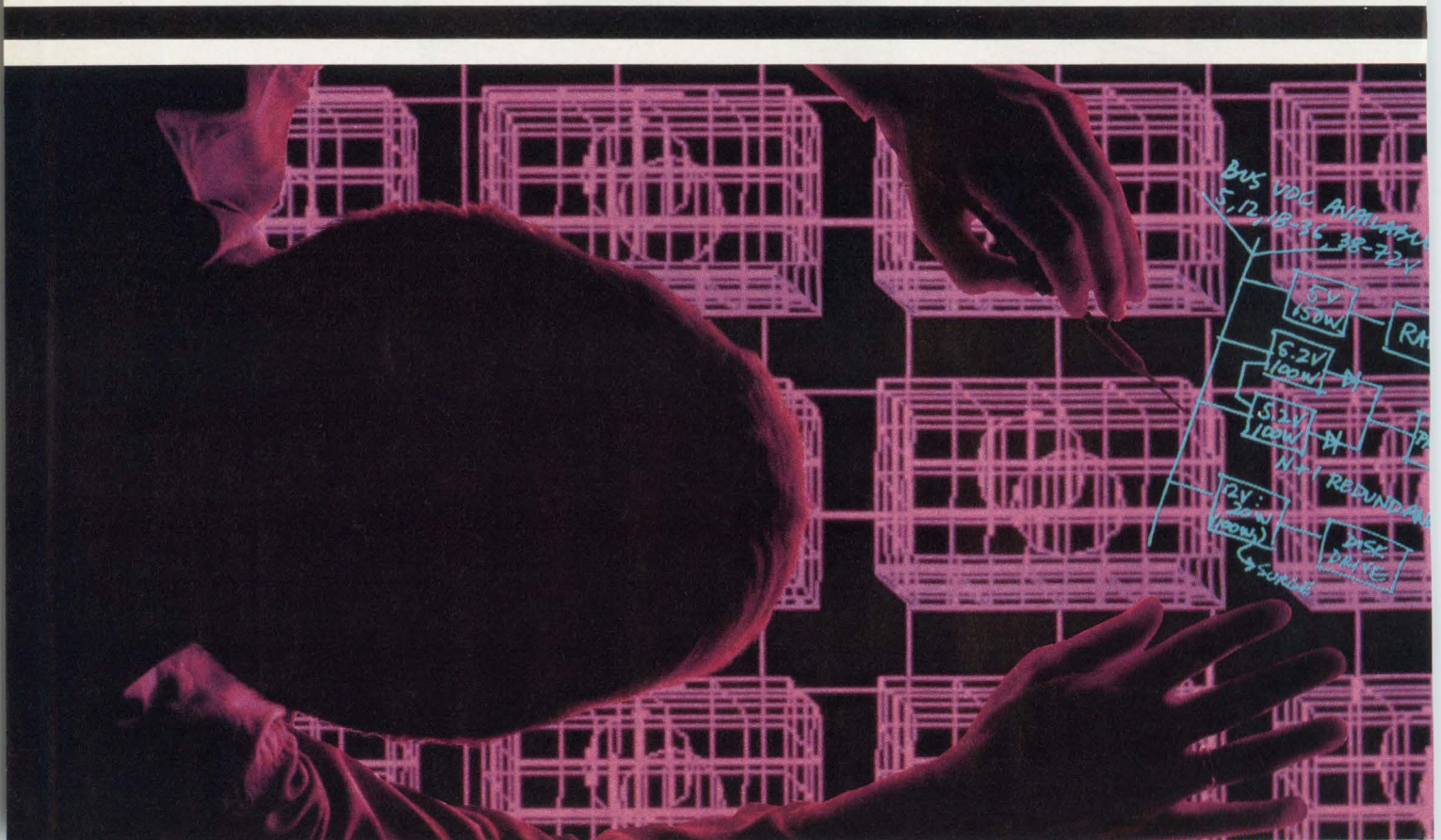
## BUDGET-PRICED CHIP DESIGN TOOLS TACKLE CELL-BASED ICs

Designing semicustom chips usually requires a budget of many tens of thousands of dollars for CAE software. Now a combination of university research and development efforts has yielded a low-cost software-tool package, called Oasis, that can perform cell-based chip designs using a top-down methodology with synchronous circuitry. The tools, developed at the University of North Carolina

at Chapel Hill, the North Carolina State University at Raleigh, the MCNC at Research Triangle Park, N.C., among others, include a compiler and logic synthesizer, a simulator and verifier, an automatic-test-pattern generator, and an automatic layout generator.

Offered on a site license for just \$3000, and a \$2000/year maintenance contract (maintenance price is for four seats; support for ad-

# Helping you design power in without risking



ditional seats costs \$500 per seat), the software allows designers with little design experience to create CMOS chips with complexities from a few thousand transistors to over half a million devices. Typical designs implemented in 1.25- $\mu\text{m}$  technology are a 137,000-transistor chip that runs at 25 MHz, and in 0.8- $\mu\text{m}$  technology, a 594,000-transistor chip that runs at 40 MHz.

Included in the bundle of tools is a design-flow manager, Decol, that provides a template-driven user interface. Six packages for compilation and logic synthesis include: Logic3, a compiler and linker of synthesized blocks; Diet, a state-assignment optimiz-

er; Espresso2.3, a minimizer of two-level logic; Decaf, a synthesizer and optimizer of multilevel net lists; Crisp, an identifier and remover of redundancies; and Memap, a technology mapper for area or delay.

Once the logic is ready, another bundle of tools takes over. They include rule checkers, testability predictors, fault simulators, test-pattern generators, and test-pattern weight optimizers. Mixed-level simulation and verification tools handle critical-path timing analysis, layout extraction, and verification of hardware descriptions before final layout is done with a quadrisection-based cell placer and router.

The design can be captured with Logic-3, a Pascal-like programming language that combines functional and structural descriptions. The functional description specifies finite-state machines and decoding logic that can be synthesized into circuit structures with logic-synthesis software. Scan-path logic can be inserted into every synthesized block.

In addition, the system can accept logic blocks designed on other software systems. Such blocks, however, must be manually interconnected to the rest of the logic. Data-path logic can also be synthesized hierarchically from parameterized structural and functional descriptions of

subcomponents.

Following design verification, test-generation tools determine the fault coverage at the gate level. Automatic placement and routing are performed after the circuit meets the design specifications, and final performance verification is based on the circuit extracted from the mask data. The Oasis 1.0 software runs under Unix 4.3 BSD; SunOS, the Sun operating system; and Ultrix. It can be installed on VAX8650, DEC3100, Convex-C1/2, Sun 3, and Sun 4 platforms. Software licenses can be obtained from the Software distribution office at MCNC. Call (919) 248-1969.

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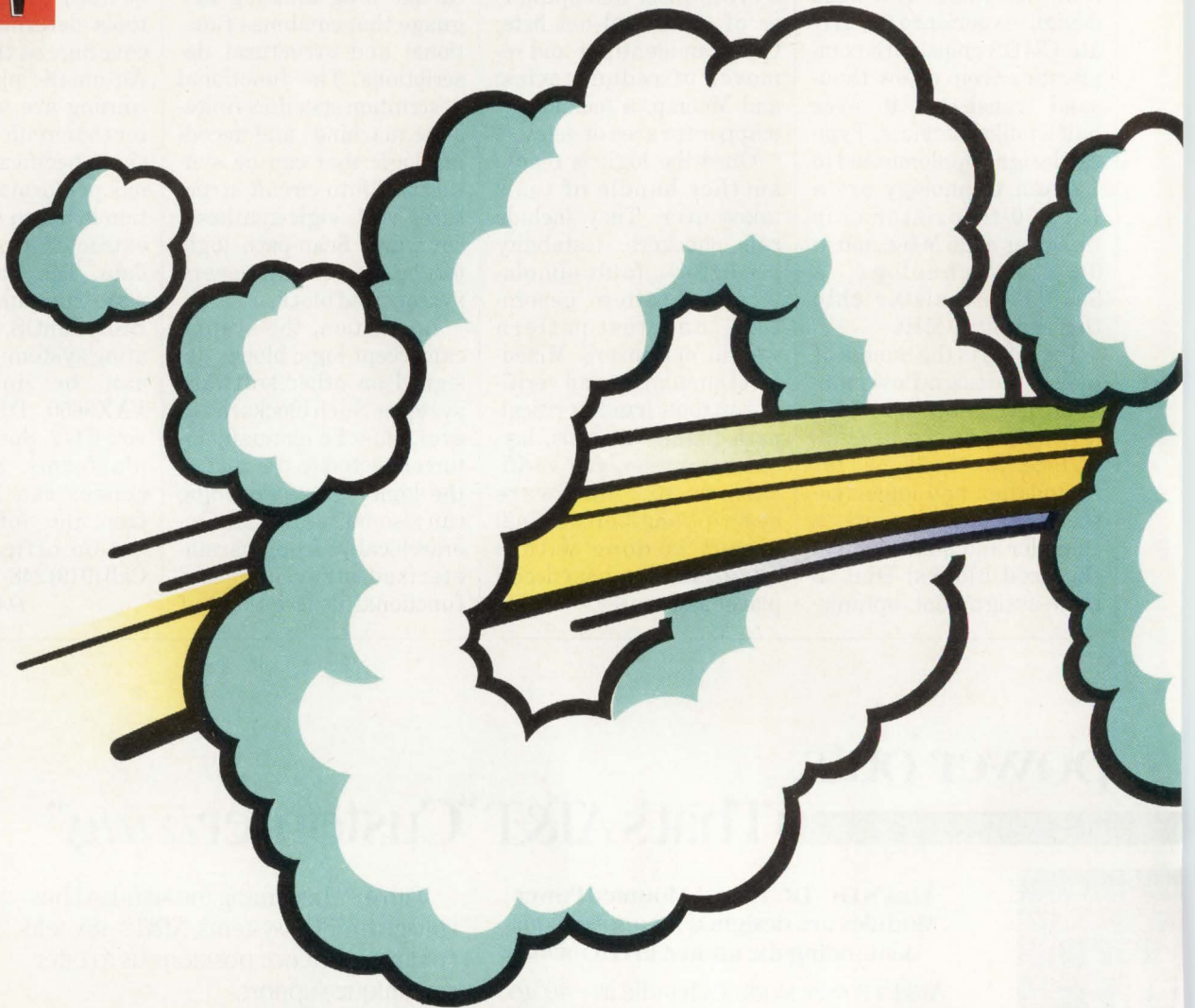
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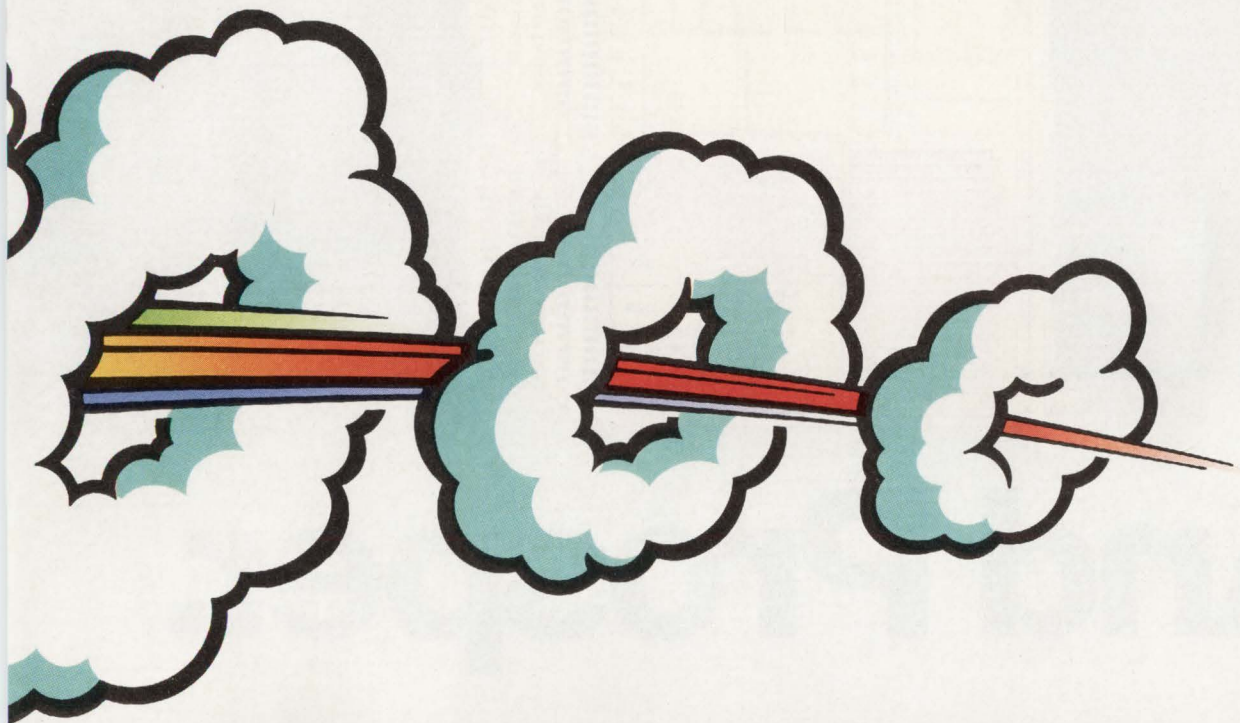
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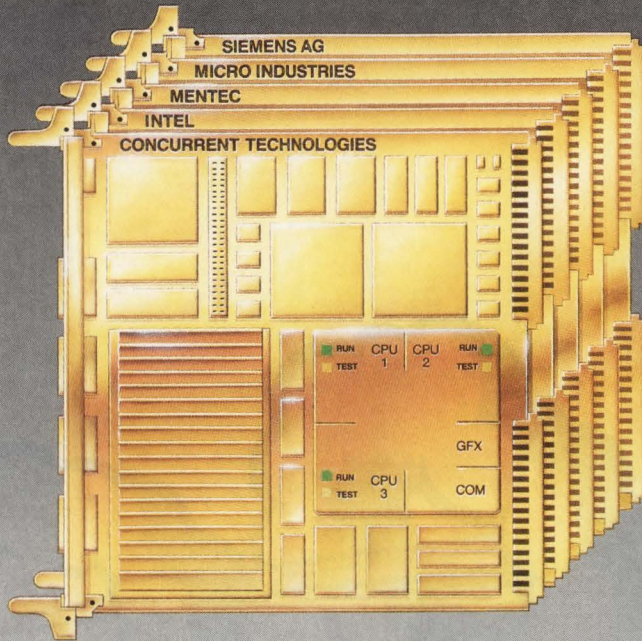


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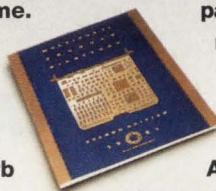


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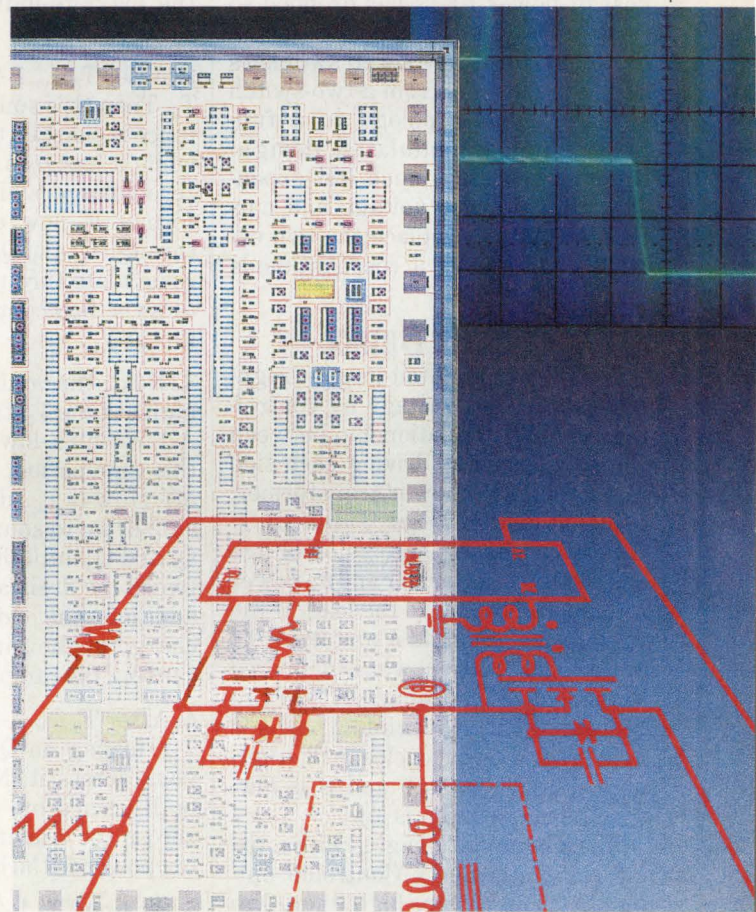
# PHASE MODULATION CUTS LARGE-SWITCHER LOSSES

FRANK GOODENOUGH

Over the last several years, resonant-mode operation has been the preeminent innovation in switching power supplies. By offering zero-voltage and zero-current switching topologies, the technique cut switching losses, thus creating high-density supplies. Reducing these switching losses eased the job of building higher-frequency switchers, which raises power density by cutting the size of magnetic and capacitive components.

But as total output power climbs above 400 W, many supplies employ a full-bridge pulse-width-modulated (PWM) design with four MOSFET switches instead of using one or two switches (*Fig. 1*). To date, most of these supplies operate below 100 kHz. And while low-loss full-bridge resonant-mode topologies have appeared, their operation has been limited in designs above 200 W. This is where phase modulation enters under the aegis of Micro Linear's controller IC, the ML4818.

Phase modulation is a new topology that features zero-voltage switching. In other words, the drain-to-source voltage of the MOSFET switch is zero when the gate of each n-channel FET is driven positive to turn it on. Phase modulation couples the low switching losses of resonant-mode designs with the efficient power transfer and constant-frequency operation of pulse-width modulation (PWM). It's often called soft switching because the transitions are resonant, but the power-transfer waveforms are basically square waves with flat tops. Phase modulation will find its major applications in high-density switching power supplies with output power between 250 and 2500 W.



The ML4818, which can operate to over 1 MHz, typically increases the power density of today's switchers by at least 50%. By changing topologies, for example, a 400-W supply now switching at 100 kHz can move to 500 kHz. A move to phase modulation can also cut material cost, as well as design time.

Unlike resonant-mode operation, phase modulation doesn't demand the use of MOSFETs with peak voltage and current ratings

# PHASE-MODULATED CONTROLLER IC

as much as four times those used in conventional square-wave PWM designs (see the table). Low-power switchers, which typically use one 50-cent switch, may be able to accept the added cost of resonant-mode operation (a \$1.25 switch) to gain the smaller size offered by the topology. However, because most 250-W or larger supplies use a full-bridge topology, the compromise is more difficult at higher power. In these supplies, four FETs, rather than one that's initially more expensive (higher-power), would have to be replaced with still more expensive devices.

On the other hand, because the cost of power FETs has dropped so dramatically, it may now be economical to move lower-power switchers (less than 200 W) from a two-switch resonant-mode topology to a full-bridge phase-modulated design. That is, use four much less-expensive FETs (lower voltage and current ratings) to replace the two devices required by a resonant-mode design.

## CROSS A BUSY BRIDGE

A phase-modulated supply regulates its output voltage by controlling the phase relationship between the square waves driving each side of the supply's power transformer, points A and B (Figs. 1 and 2). If they're in phase, there's no voltage across the transformer and no power is delivered to it or to the load. If the waveforms at points A and B are 90° out of phase, 50% power is delivered to the load (Fig. 2, again). If they're 180° out of phase, maximum power is delivered. Power cycles will alternate: First A is high and B is low, then B is high and A is low.

The power cycle begins with a rising ramp at time  $T_0$ . Controller outputs A-2 and B-1 are high, therefore FETs  $Q_2$  and  $Q_1$  are on. When power is delivered through the transformer to the load, the following sequence of events takes place:

1. At time  $T_1$ , the controller's phase-modulation comparator trips due to the rising ramp on its plus input, or the current-limit comparator trips first due to a fault. The B-1 line goes low, turning off  $Q_2$ . With  $Q_2$  off, the

## SWITCHING-POWER-SUPPLY TOPOLOGY COMPARISON

Feature	Topology			
	Square-wave PWM (full bridge)	Resonant mode		Phase modulation
		Zero-voltage switching	Zero-current switching	
Usable to $f_{MAX}$ of:	200 kHz	3 MHz	1 MHz	2 MHz
Major switching-loss mechanism	$1/2 LI^2f$ $1/2 CV^2f$	None	$1/2 CV^2f$	None
Switch peak-current rating	$1.1 \times I_{AVG}$	$1.5 \times I_{AVG}$	$3 \times I_{AVG}$	$1.2 \times I_{AVG}$
Switch peak-voltage rating	$V_{IN}$	$4 \times V_{IN}$	$2 \times V_{IN}$	$V_{IN}$

drain-to source parasitic capacitances of  $Q_2$  and  $Q_3$  are charged to  $V_{in}$  (which may be hundreds of volts) by the leakage-inductance's current,  $I_{leakage}$ .

2. After  $T_{delay}$ , B-2 goes high at time  $T_2$ . Then  $Q_3$ 's source-to-drain capacitance is charged to  $V_{in}$ , turning on  $Q_3$  while it has zero voltage across it—zero-voltage switching. The transformer is now effectively shorted through  $Q_1$  and  $Q_3$ , enabling  $I_{leakage}$  to recirculate through the two transistors via their common source connection at  $V_{in}$ .

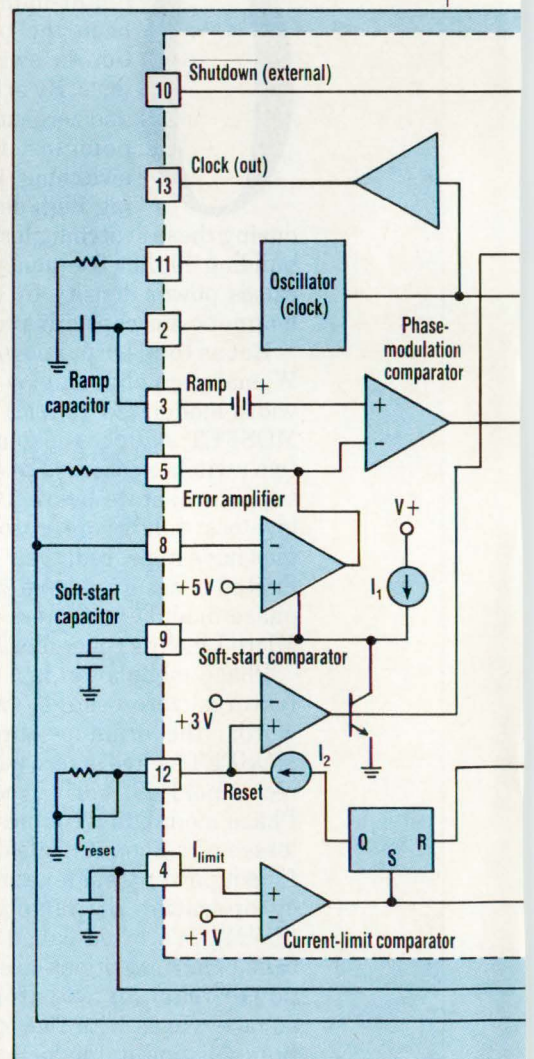
3. Next, the controller's Clock goes high at time  $T_3$ , taking A-2 low. Line A-1 remains low for  $T_{delay}$ . During this time period, both  $Q_1$  and  $Q_4$  are off. Now  $I_{leakage}$  discharges the parasitic drain-to-source capacitances of  $Q_1$  and  $Q_4$  until there's zero volts between the drain and source of  $Q_4$ . In addition, the clock starts the discharge of the ramp capacitor at  $T_3$ , causing the ramp to start falling.

4. After  $T_{delay}$ , A-1 goes high at time  $T_4$ , turning on  $Q_4$  while it has zero volts across it. Now  $Q_4$  and  $Q_3$  are both turned on, creating a voltage across the transformer and delivering power to the load.

5. At time  $T_5$ , B-2 goes low and the sequence of events is repeated, except that the polarity of each output and the direction of each transition are reversed.

With an understanding of how phase-modulated switching regulators work, the features of the topology and the ML4818 should be explored. To start with, the MOSFET switches are fully clamped. That is,

they need only be rated at  $V_{in}$ . Moreover, they don't require snubbers. Constant-frequency operation, impossible with resonant supplies up to now, not only simplifies filtering, but can also synchronize multiple sup-



# PHASE-MODULATED CONTROLLER IC

plies. Potential beat notes, which can cause havoc with analog signals and even with data, are thus eliminated.

The lossless switching at zero volts represents one of those rare occasions where you get something for nothing. The usually wasted energy stored in the transformer's leakage and magnetizing inductance drives the voltage across each switch to zero before the next switch is even allowed to turn on. As a result, there's no charge dumping, and losses due to Miller-capacitance turn-on delays are reduced.

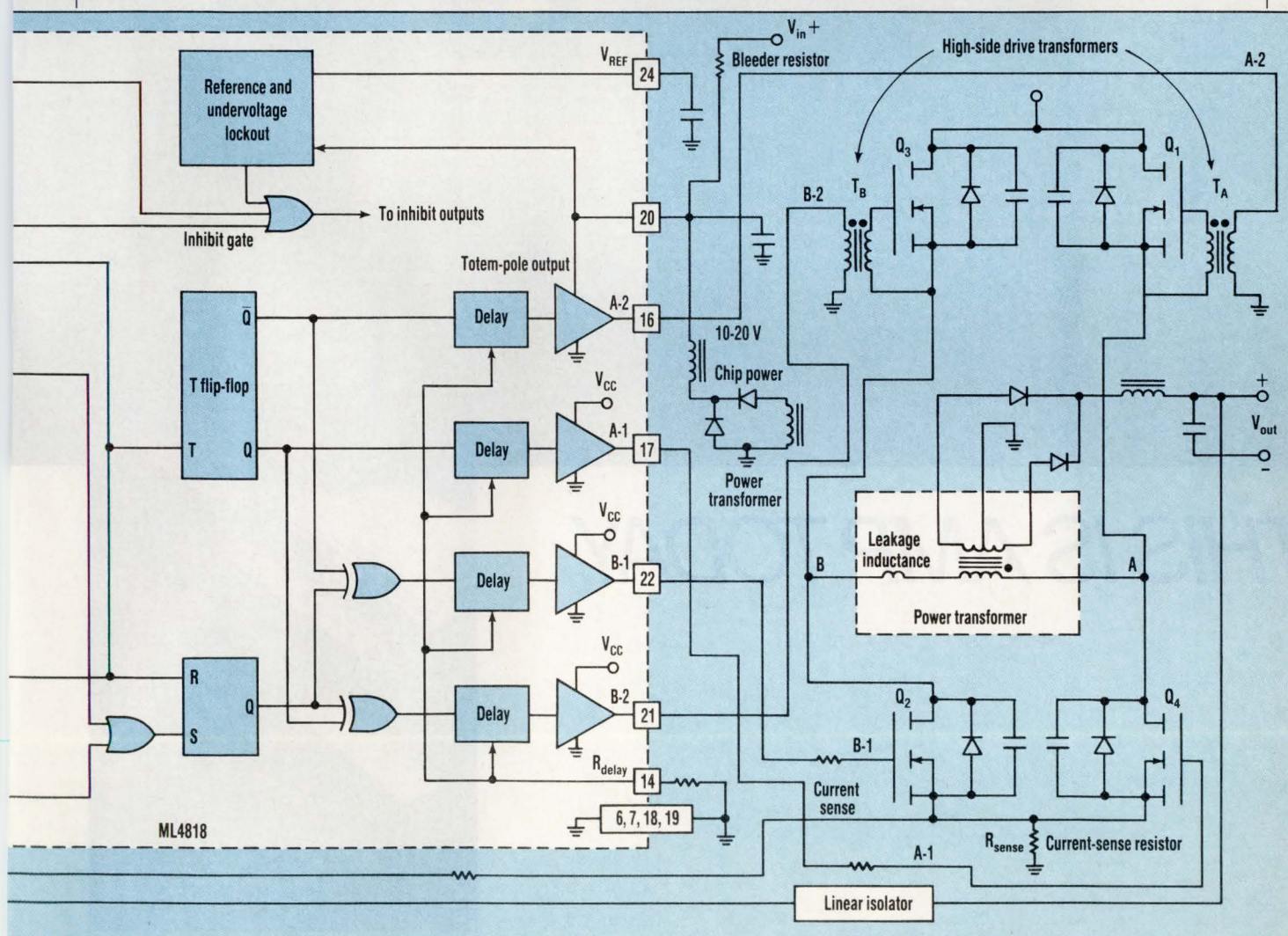
Charge dumping is caused by the MOSFET's output capacitance  $C_{out}$  (Fig. 3). The power lost with non-zero-voltage switching equals  $C_{out} V^2 f$ , where  $V$  is the supply volt-

age  $V_{in}$  and  $f$  is the switching frequency. This power loss can be significant in supplies with high input voltages, such as off-line switchers operating at high frequencies. Running one standard IRF450 MOSFET at 350 V while switching at 500 kHz results in a charge-dumping loss of 20 W, which becomes 40 W switching at 1 MHz.

In most MOSFET switching circuits, the FET's drain-to-gate or Miller capacitance must be fully charged to get the FET fully into saturation. This charging current (power) comes from the gate-drive circuit. The time needed to charge the Miller capacitance slows FET turn-on, raising switching losses. However, during zero-voltage switching, the FET

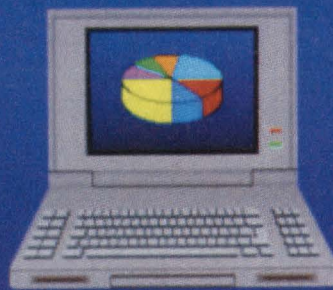
turns on with a drain-to-source voltage of zero. None of the gate drive is wasted charging Miller capacitance.

Because resonant supplies shuttle more current through their passive parts than they transfer (dissipating power in the process), internal rms and peak currents run substantially higher than the dc currents delivered to the load. Phase modulation, on the other hand, offers energy transfer similar to PWM designs. In addition, whereas resonant-mode supplies generally require a minimum load (often as much as 10% of full load), phase-modulated switchers can always run at zero load. Finally, unlike some topologies, this new one doesn't limit designers to just voltage-mode operation. It also handles



**1. A PHASE-MODULATED** switching-regulator controller, Micro Linear's ML4818 modulates the relative phase of square waves applied across the power transformer (points A and B). The modulation regulates the output voltage of the full-bridge switching power supply.

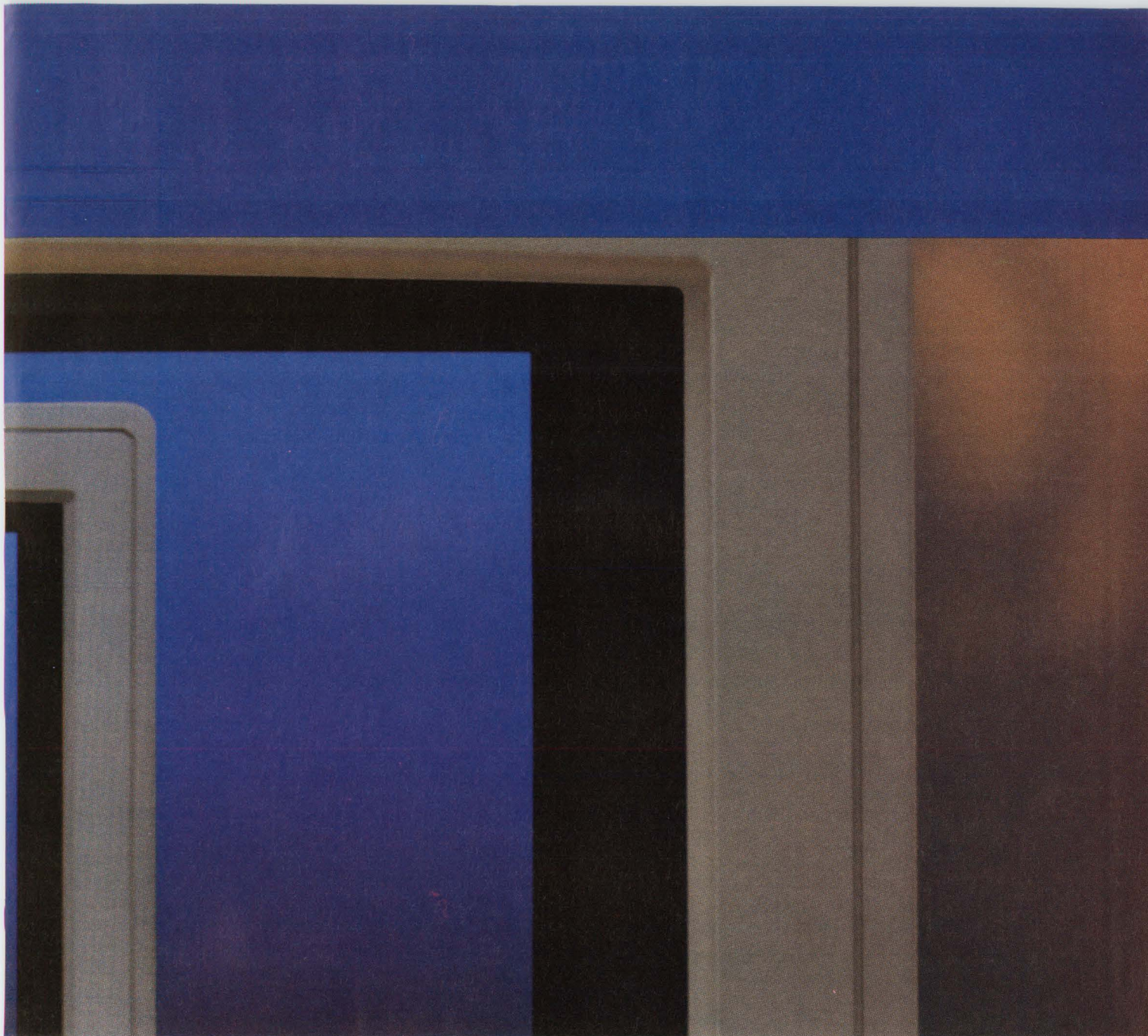
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# AMP

CIRCLE 180

# PHASE-MODULATED CONTROLLER IC

current-mode switching as well.

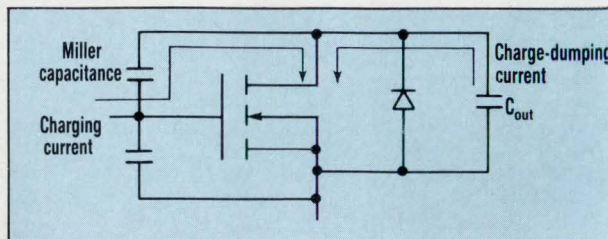
The ML4818 takes full advantage of what the phase-modulation topology offers, and provides all of the safety features expected from today's controllers. To start, the ML4818's four totem-pole outputs are rated at minimum peak currents of 1.5 A (500 mA continuous). They easily charge a FET's 1000-pF input capacitance to 12 V in just 60 ns maximum. Because the topology handles both voltage and current modes, the controller is equipped to do likewise. For the voltage mode, pin 3 (the ramp pin) should be connected to the current source from the oscillator (pin 2). The current source charges the ramp capacitor (Fig. 1, again). Alternatively, the ramp pin should be connected to a voltage proportional to switch current for current-mode operation. Such a voltage can be obtained across the current-sense resistor with current transformers in series with the FETs, or from sense-FETs if available in the voltage and current ratings required.

There are several safety features to protect the switches. They include cycle-by-cycle current limiting with integrating fault detection, soft start, undervoltage lockout, and the ability to shutdown the controller

and supply in microseconds with an external signal (for example, if the system catches fire).

Current limiting starts when the current sensed on pin 4 (the current-limit comparator's plus input) reaches 1 V. The comparator fires, thus terminating the power cycle through QRS flip-flop #1. QRS flip-flop #2 then turns on current source  $I_2$  to charge  $C_{RST}$  (pin 12).  $I_2$  stays on for the duration of the clock period. When charged to 2.3 V, the soft-start comparator triggers and initiates a soft-start reset. The number of times the cycle is terminated due to over-current conditions is "remembered" on  $C_{RST}$ . Over time, if not continuously charged, the capacitor is discharged by the parallel resistor.

Because the per-power-cycle charge on  $C_{RST}$  is directly proportional to how early the reset takes place in the power cycle, a reset is triggered more quickly under short-circuit conditions than during a load surge. This technique is the way most circuit breakers work, and is



**3. PHASE-MODULATED CONTROL** of a switching regulator increases switching efficiency by reducing charge dumping and Miller-capacitance losses.

called Integrating Fault Detection.

When soft-start reset occurs, the soft-start comparator's output goes high, which inhibits the totem-pole outputs (via the line to the inhibit gate) and turns on the npn transistor connected to the comparator's output. The npn transistor discharges the soft-start capacitor (which was charged by current source  $I_1$ ). The output remains off until  $C_{RST}$  discharges to 1.1 V, through its parallel resistor, supplying a reset delay. When the circuit starts up, the error amplifier's output voltage is limited to the voltage at pin 9, effectively limiting the duty cycle.

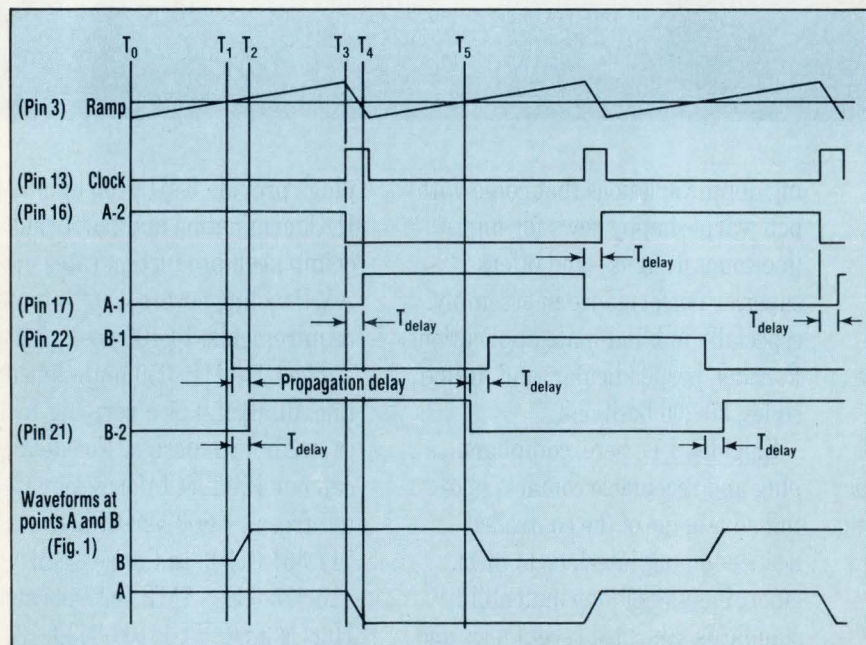
At power-up, the undervoltage-lockout circuit keeps the reference disabled and the controller draws less than 1.1 mA through the bleeder resistor from pin 20 to  $V_{in}$ . Current through the bleeder also charges the capacitor tied to the pin. When the capacitor is charged to 9.2 V, the circuit wakes up, the reference is enabled, and the circuit runs until the voltage drops to 8.4 V. □

## PRICE AND AVAILABILITY

The ML4814 comes in a 24-pin "power" DIP. A heavy copper leadframe is used, which connects to pins 6, 7, 18, and 19, the middle pins on each side; these pins are the ground pins and conduct heat to the pc board's copper foil. The device is rated for the commercial operating-temperature range. In quantities of 1000, it goes for \$7.19 each. Small quantities are in stock.

Micro Linear Corp., 2092 Concourse Dr., San Jose, CA 95131; Jon Klein, (408) 433-5200.

CIRCLE 511



**2. IN A FULL-BRIDGE** phase-modulated switching regulator, power is delivered to the load (shaded areas) when waveform B is high and waveform A is low, and vice versa.

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HOW VALUABLE?	CIRCLE
HIGHLY	535
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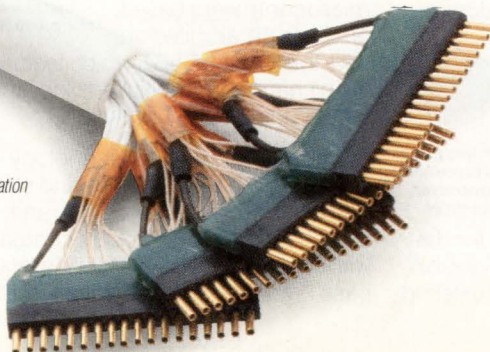
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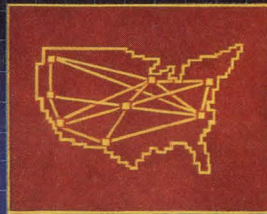
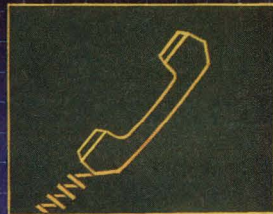
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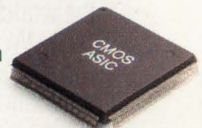
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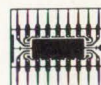
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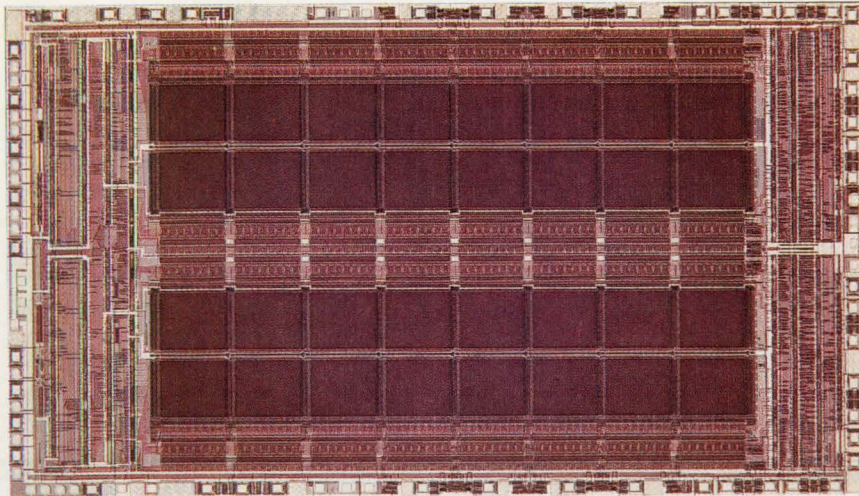


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TRIPLE-PORT DRAM PHOTO FROM MICRON TECHNOLOGY

# DRAM DIVERSITY YIELDS A MEMORY TO SUIT ANY SYSTEM

**I**n its 20 or so years of its existence, the dynamic RAM has evolved considerably to keep pace with the performance needs of the system architect. Today, there are over a dozen architectural and feature variations that memory manufacturers offer to the system designer. With the wide range of choices, designers can optimally tailor the system to match the performance, capacity, cost, and expansion granularity requirements demanded by the end application.

Today's designers are free to work with DRAMs that have 1-, 4-, 8- and even 16-bit-wide data paths, with 9- and 18-bit parity options coming soon from most suppliers. Memory capacities continue to increase by factors of four. As a result, most DRAM suppliers are now entering mass production of 4-Mbit chips. Some of these companies are already giving their best customers samples of 16-Mbit chips and expect to start large-scale sampling of 16-Mbit chips by the end of 1991. Foundation work and processing refinements are well under way at those same companies to develop the memory-cell structures needed for the ensuing generations of 64- and 256-Mbit chips (see "Making DRAMs denser," p. 52).

Not only do designers have a choice of DRAM word widths, but they also have a choice of system features. The standard DRAM can now be had with access times of less than 55 ns. And special operating modes—static col-

DAVE BURSKY

MANY DATA-PATH OPTIONS AND SYSTEM-CONTROL CHOICES LET DESIGNERS OPTIMIZE THE SYSTEM AND EXPLOIT DRAMS.

umn, page, and fast-page—enable the chips to deliver a burst of data at a much higher rate than the standard row-and-column addressing mode. Some of those modes can bring the subsequent accesses after the first one in the series to less than 25 ns.

The need for diversity and high-performance graphics systems also created the need for a new memory type in the early 1980s—the video RAM. First offered by Texas Instruments as a 64-kbit chip, the architecture has been through several iterations, with densities now reaching 1 Mbit. Some versions even include image-processing logic. In addition to the standard DRAM functionality on the chip, the basic VRAM offerings contain a 4- or 8-bit-wide serial-access port that allows the chip to deliver an entire row of data to a video subsystem at speeds comparable to the more-costly high-speed static RAMs. On the host-system side, the chips appear as standard DRAMs and offer the typical 60-to-100-ns access times. On the video side of the chips, however, the output looks like a fast shift register, able to shift out from 256 8-bit or 512 4-bit words at clock rates as fast as 15 ns/word.

Even more diversity has started evolving in DRAM architectures. Last year saw Micron's introduction of the MT43C4257, a triple-port 1-Mbit memory that contains the standard DRAM port plus two video-RAM-like 512-by-4 serial-access ports (ELECTRONIC DESIGN *May 24, 1990, p. 37*). A slightly different organization can be seen in the MT43C8128, which has its main port appearing as a 128-k-by-8 DRAM and the two serial ports looking as dual 256-by-8 ports (*Fig. 1*). High-density pseudo-static RAMs based on a DRAM core have also started to arrive. They offer the high density of DRAMs with close to



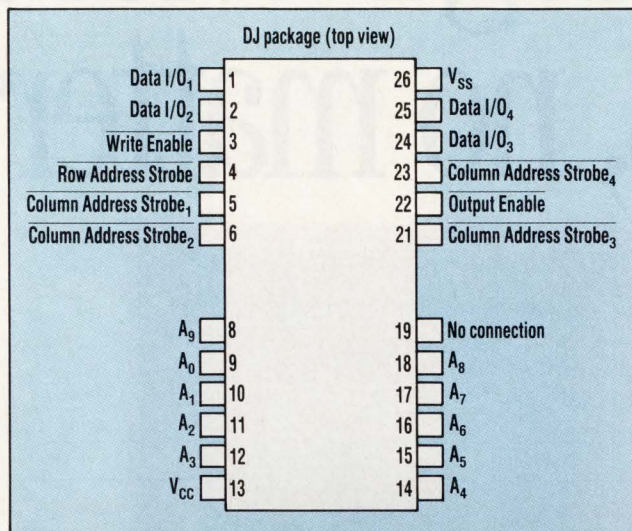
## FLEXIBLE DRAMS

eventually byte-wide and 16-bit architectures will dominate in the mid-to-late 1990s. Furthermore, designers expect 16-bit-wide chips to make some significant application inroads at the 64-Mbit level. For instance, a pair of 16- or 18-bit-wide 16-Mbit chips could form the entire memory of a base-model desktop computer (2 Mbytes). NEC, for instance, plans to have an entire family of 16-bit-wide, 4-Mbit DRAMs released before the end of this year, and will follow those chips with 16-Mbit versions in late 1992.

As graphical-user-interfaces and application programs become more complex, similarly organized

64-Mbit chips could eventually form the memory subsystem (8 Mbytes). Proving such a memory is possible, designers at the Semiconductor Research Center of Matsushita Electric Industrial Co. Ltd. in Osaka, Japan, developed a 4-M-by-16 version of a 64-Mbit DRAM. They unveiled the chip earlier this year at the International Solid-State Circuits Conference (ISSCC). By paying careful attention to power and ground busing, the 16-bit-wide I/O bus was kept relatively free of noise.

Most DRAM vendors are already mass-producing 1-bit- and 4-bit-wide versions of the 1- and 4-Mbit CMOS DRAMs. Access times are as short as 70 ns for the newer 4-Mbit chips, and companies are promising 60-ns samples before year's end. Fine-tuning is already in place for most 1-Mbit production lines so that 60-ns devices are readily producible. At least one supplier, NMB Technologies, has specified a 53-ns standard-speed grade. Some designers, though, question the need for such a high-speed grade—most high-speed systems usually have an intermediate cache memory that doesn't demand such short access times for the main memory. In some cases, of course, the main memory's speed may be fast enough using these fast



**2. WITH FOUR CAS LINES** rather than one, the TMS44460 from Texas Instruments can replace four 1-M-by-1 DRAMs, which are typically used to handle the parity bits on a 1-M-by-36 memory in a SIMM package.

DRAMs, thus the cache may not be needed.

For users that have the most stringent speed requirements for main memory, designers at Hitachi may have the best product—a biCMOS DRAM that offers access times as short as 30 ns. However, such memory speeds don't come free. The biCMOS DRAMs will sell for close to double the price of the fastest CMOS chips. Hitachi currently has a 1-Mbit biCMOS DRAM it offers as a commercial product, and is developing a 4-Mbit version it hopes to release in late 1991 or early 1992. An early prototype of the 4-Mbit chip was unveiled earlier this year at ISSCC.

If that solution isn't quite what's needed, perhaps some research work by designers at Mitsubishi will lead to the answer—a cache-DRAM chip that combines DRAM and static RAM on the same piece of silicon. Although it's not yet a commercial product, the concept has its appeal. This is because a very wide bus can be formed between the two memory blocks so that many bytes can be transferred from the DRAM to the cache blocks during one cycle whenever a cache line must be refilled.

Further solutions to the speed issue led to an experimental DRAM developed by Toshiba's research lab-

oratory described earlier this year at ISSCC. The chip replaces the standard, multiplexed, row and column address signals with a direct-input address, eliminating the setup and timing delays associated with demultiplexing the address. In a laboratory setting, the CMOS chip accessed data in about 17 ns—the same speed as the experimental 4-Mbit biCMOS DRAM Hitachi described at the same conference.

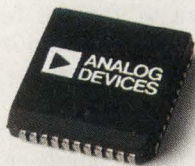
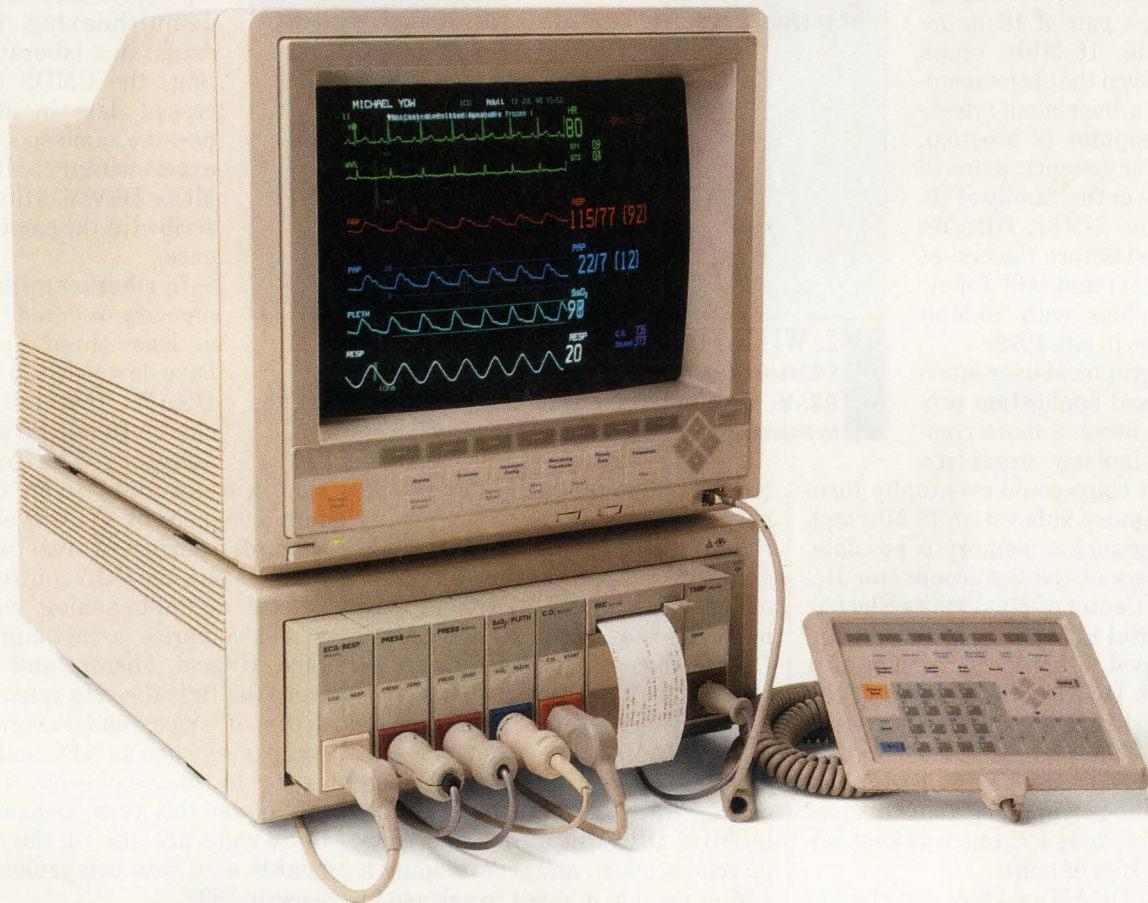
In addition to the main-memory-oriented DRAMs, at least three companies have developed 16-bit-wide DRAMs that reduce the chip clutter on PC graphics adapters. The first ver-

sion, a 64-kword-by-16-bit chip, offers designers of VGA-level graphics cards a perfect fit. Just two of the DRAMs plus the VGA controller and palette digital-to-analog converter would comprise a minimum interface. Hitachi, Micron, and Toshiba were the first three to release these types of chips, and several other companies, such as NEC and Vitelec, expect to release pin-compatible devices later this year. Denser, 256-k-by-16 chips are also on the drawing boards at a few companies for release in 1992.

Unlike the main-memory arena in which densities traditionally increased by factors of four, a few companies in the video-support-memory area feel that designers need a 2-Mbit memory, organized as 128 kwords by 16 bits. The memory would make the "ideal" single-chip memory for low-end VGA displays, which require 256 kbytes of storage. Hitachi, as well as other Japanese memory suppliers, are planning such chips for late 1991 release.

Several options exist with these DRAMs that can simplify video-subsystem design. Control signals on the chip in one version can offer upper or lower byte control with a fast-page-mode access mode available to move data quickly. A similar version

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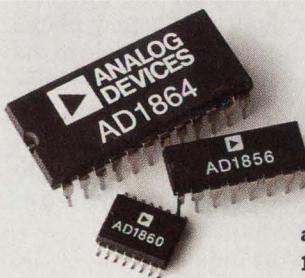
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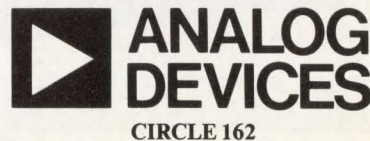
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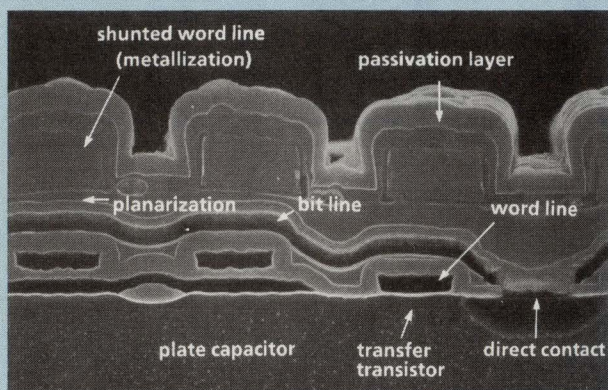
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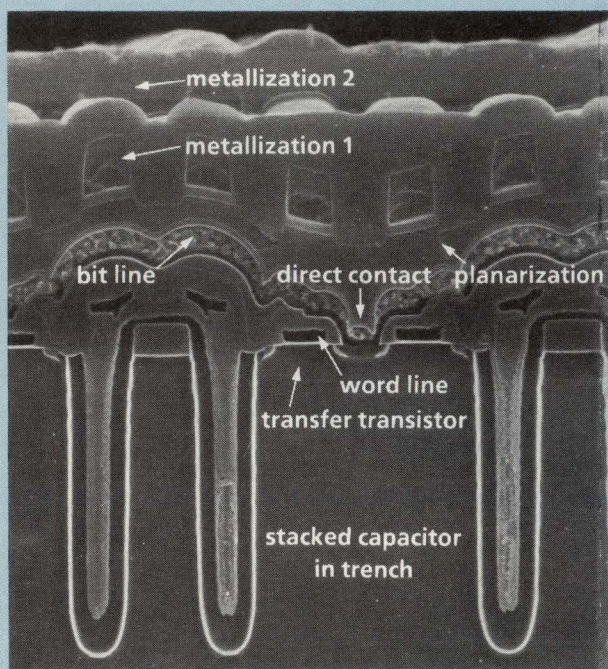
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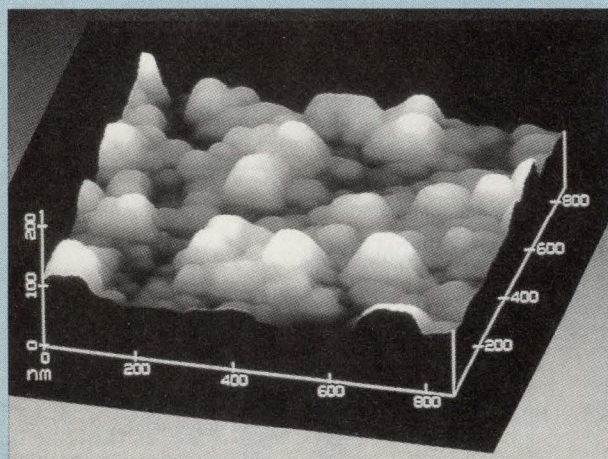
## MAKING DRAMS DENSER



a



b



c

Since their inception, dynamic-RAM processes and circuit structures have undergone many engineering changes. These changes aim to reduce the size of the chip, packing more cells on the chip, improving the access time, and reducing chip cost. Starting with the first-generation DRAMs and up through the 256-kbit level, chip designers have used a lateral structure for the capacitive storage cell, which contains the charge that represents the bit condition. If there's too little charge, the bit value fades or it can be upset by an alpha-particle strike. Too much charge and the memory chip is too slow or too large to be profitable.

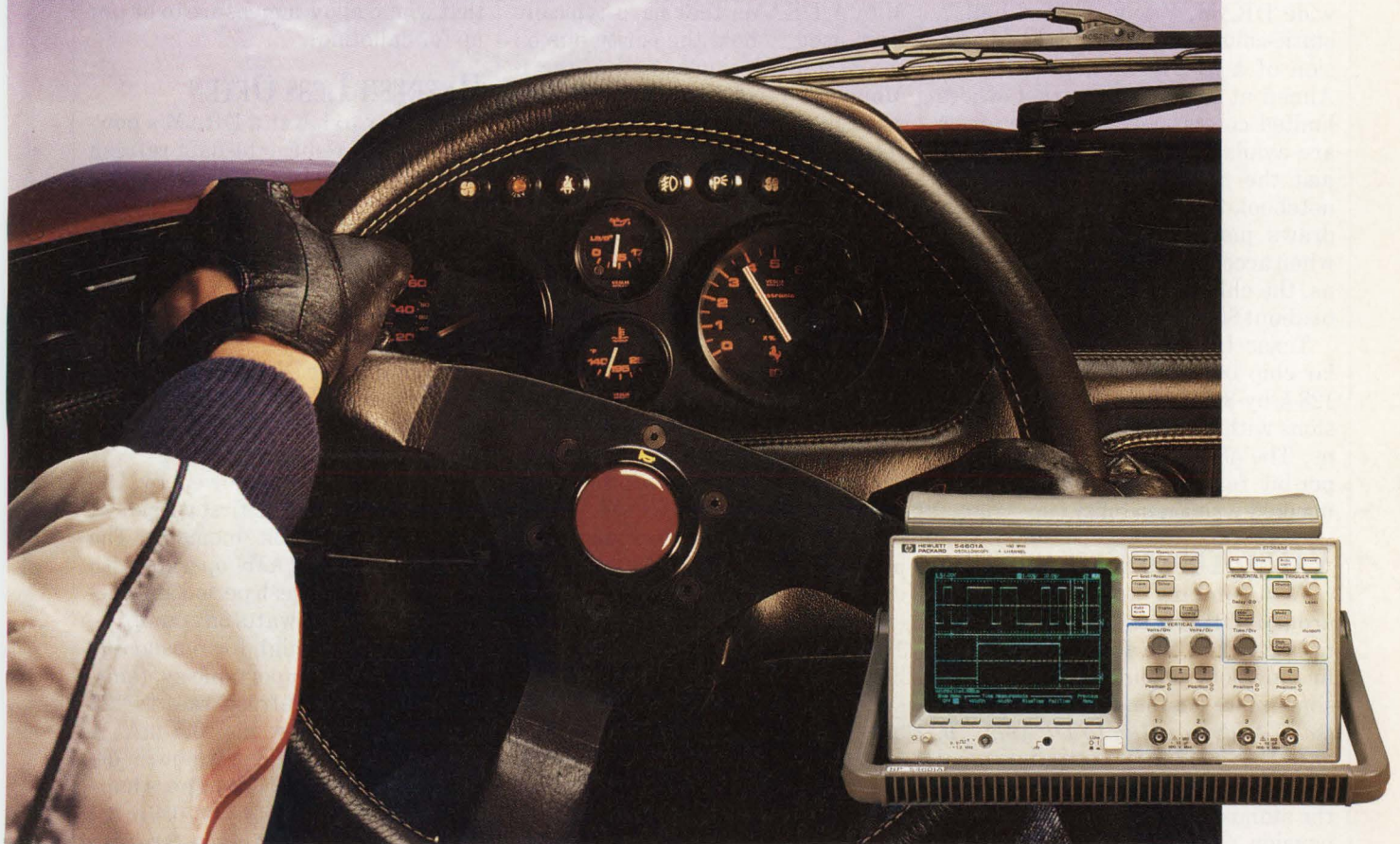
DRAMs have employed a single-transistor/single-capacitor storage cell since the second-generation 16-kbit chips' introduction in the late 1970s. However, that lateral cell structure isn't dense enough for generations beyond 1 or 4 Mbits because the transistor and capacitor are side-by-side to each other. Even though feature sizes dropped from the 5- $\mu\text{m}$  range used in the late 1970s to the deep-submicron range of 0.4  $\mu\text{m}$  for the prototype 64-Mbit parts, scaling limits have been reached for some aspects of the chip.

As the capacitor's area shrinks, so does the capacitance value. Once that value drops below about 25 fF, most memory designers would not recommend using the cell for storage. Consequently, the capacitance has apparently reached the minimum reliable value. The value dictates the area of a lateral-cell capacitor. Chip designers are, of course, looking at ways to further improve the lateral cell as well as come up with new structures that pack more capacitance per unit area.

In the effort to construct a more efficient cell, DRAM makers find themselves in two opposing cell-design camps. The first camp employs a stacked-cell structure that builds the capacitor above the control transistor using wing- or cylindrical-shaped plates (Fig. A). The other uses minute etched trenches in the silicon and forms the capacitors in those trenches (Fig. B). Both cell types have their manufacturing pros and cons. Nonetheless, both work and are manufacturable. As a result, it will be up the chip makers to answer questions about long-term reliability and cost-to-manufacture of the storage cell.

To increase the capacitance by almost 35% over the value expected from the lateral area, designers at Micron Technology Inc., Boise, Idaho, developed a roughened silicon-nitride dielectric layer in a lateral cell to increase the plate surface area; the rough surface is clearly visible through the eye of an atomic-force microscope (Fig. C). The increased surface area is approximately 35% higher than that of a smooth cell. That larger area translates into a higher storage capacitance. Micron and a number of other companies reported on their experimental findings at the 1990 IEEE International Electron Devices Meeting.

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with static-column access is also available. For more selective write requirements, a version with write-per-bit capability makes it possible for the video controller to handle more detailed image control.

One of only several companies to offer a fast, moderate-density byte-wide DRAM, Vitelic created both a static-column and a fast-page version of a 64-k-by-8 image memory. Aimed at the laptop market where limited colors and gray-scale levels are available, this memory may be just the right size for pocket and notebook-type computers. The chip draws just 1 mA on standby, but when accessed at its best speed of 70 ns, the chip's power drain increases to about 65 mA.

Texas Instruments offers a similar chip but at the 1-Mbit level. Its 128-k-by-8 TMS48C128 comes in versions with access times as short as 70 ns. The 48C138, which has a write-per-bit feature, also comes with a masked-write capability.

## VALUE-ADDED PACKAGING

A secondary business evolves around DRAM chips—value-added packaging in the form of single-inline memory modules (SIMMs), and some more custom-oriented hybrids (see "Adding value to DRAMs," p. 56). For personal computers and workstations, SIMMs have become the standard format for memory expansion, especially when that memory resides on the system motherboard.

The growing popularity of SIMMs has enticed TI to develop a specialty

1-M-by-4 DRAM with four Column-Address-Strobe lines (Fig. 2). By having four CAS lines, each of the four I/O bits can be read or written individually—an ideal adjunct for a 1-M-by-36 SIMM already employing standard 1-M-by-4 DRAMs. One TMS44460 could then replace four 1-M-by-1 DRAMs that have typically been used to hold the parity bits on the SIMMs. A similar chip at the 1-Mbit level, the TMS44C260, is also organized as 256-k-by-4 and has four CAS lines plus all of the standard control lines.

In addition to architectural variations, new-generation DRAMs are coming with new options—special low-power modes for use in battery-powered systems and a test mode to simplify functional testing. Furthermore, as the lithography requires deep submicron features to achieve the high densities, internal electrical stresses require that the power-supply level be reduced. Both the 4- and the 16-Mbit generations will probably still use a 5-V external power supply and on-chip voltage-reduction circuits to drop the internal voltages to less than 4 V (3.3 V in many cases). That lower supply voltage will also help to reduce the chip's power consumption. Most DRAM manufacturers expect the 16-Mbit chip to be a pivotal chip for system designers. They plan to offer a version that accepts either 3.3 or 5 V externally, or in two separate options, one bonded for a 5-V supply and the other for a 3.3-V supply.

Beyond the 16-Mbit chip, most memory manufacturers expect to

use only a lower supply voltage than today's 5-V level (most likely is the 3.3-V standard). There are some proposals wending their way through the Joint Electron Device Engineering Council (JEDEC) committees for a sub-3-V standard, but there has yet to be an industry-wide consensus that would allow a measure to be put up for balloting.

## REFRESH LESS OFTEN

One way to lower a DRAM's power drain is to reduce the data-refresh rate. However, by slowing the refresh rate, more charge can potentially leak off the memory cell's storage capacitor, thus causing a bit to inadvertently change value. Rather than create a special memory chip designed specifically for a slower refresh rate, most DRAM vendors can just test chips for their leakage currents and sort out those that test extremely low.

This practice is followed by Oki Semiconductor for its first version of a low-power 4-Mbit memory. The normal-power DRAMs operate with an 8- or 16-ms refresh period and consume tens of milliwatts on standby—a level much too high for reasonable battery backup in portable systems. By slowing the refresh rate to 128 ms, the chips draw just 0.5 mA. A more optimized version is now in development, and Oki's designers hope to reduce the drain to just 0.4 mW/chip. Many other companies are also working on low-power, slow-refresh DRAMs, with Toshiba probably leading the pack in that research.

It may not come as a surprise to

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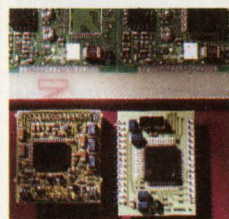
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most designers, but it's a little known fact that the 4-Mbit chips all have a built-in functional-test mode that's activated by pulling the Write line low and reversing the timing on

the CAS and Row-Address-Strobe (RAS) lines—CAS before RAS with Write Enable low. That sequence places the memory chip into a wide-word test mode, which internally

checks 8 or 16 bits at a time. If a bad bit is found, the output bit pattern alerts the tester that a more thorough test must be done on that chip. Although this mode can be activated when the chip is in a computer system, no system manufacturers have incorporated this test mode into the basic boot-test of a system for self-correction.

Designers at Micron, though, are warning some system designers to be careful about upgrading their boards from 1-Mbit chips to 4-Mbit chips. On the 1-Mbit-generation chips, pin 1 is a "don't care" pin and reversing the CAS and RAS timing has no effect—the test mode is controlled by a super-voltage level applied to pin 1. At the 4-Mbit level, the pin must be pulled low prior to the reversed CAS-before-RAS timing applied to the chip, to initiate the test action.

When designing 1-Mbit-based systems, special attention should be paid to the state of pin 1. It should not be tied low because if a 4-Mbit device is substituted, the pin could accidentally cause the chip to go into its self-test mode.

There are yet other slight differences between the 1-Mbit and 4-Mbit-generation DRAMs. Those differences have to do with power-up sequencing and the number of allowed refresh cycles.

The 1-Mbit chips typically require a 0.1-ms delay followed by any 8 RAS cycles. The 4-Mbit specifications are somewhat more restrictive and permit a chip to respond to 8 RAS-only or Write-with-CAS-before-RAS refresh cycles. This restriction is needed to also prevent the memory from entering the test mode. To partially solve the incompatibility issues, designers at Micron offer a second version of their 4-Mbit chip that requires a super-voltage signal to switch into the test mode, instead of requiring the Write-Enable line to be pulled low. □

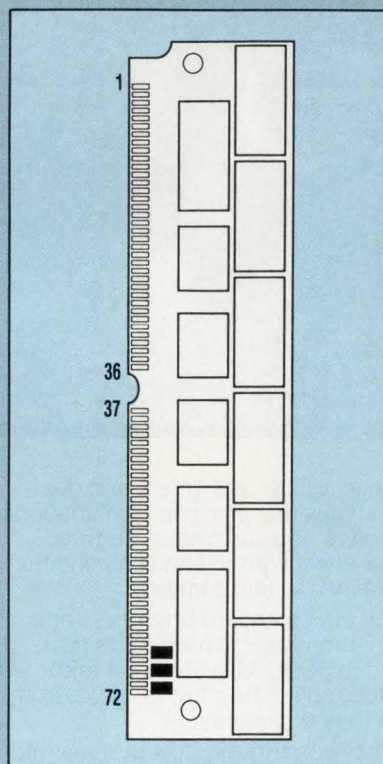
## ADDING VALUE TO DRAMS

For a long time, the DRAM was only available in the familiar 16-, 18-, and 20-pin DIPs. However, as designers tried to push the memory capacity of their boards to new highs, DRAM manufacturers shoehorned the new-generation chips into J-leaded plastic flat packages, zig-zag vertical in-line packages, and most recently into the very-low-profile thin-small-outline packages (TSOPs). With these package options, designers have enough choices when dealing with individual memory chips. But, because many memory subsystems now pack megabytes of storage, laboring at the chip level is time lost for most designers.

One surging approach involves using single-in-line memory modules (SIMMs). The SIMM concept started during a period when 256-kbit DRAMs were in short supply. At that time, system manufacturers examined ways to build systems with user-installable memory that was more rugged than the venerable DIP. If they could create such a format, they could get systems out to market faster because the systems could be sold without DRAM. But then users would have to expend the cost and time to find the scarce DRAM supplies actually in the market.

As most computer-system makers adopt the SIMM format, many of the DRAM and non-DRAM makers have started offering 8- and 9-bit (byte-wide) SIMMs and the 32- and 36-bit word-wide versions. Capacities range from 256 kbytes for the older SIMMs up to 8 Mbytes for the largest commercial offerings.

The chewing-gum-stick-sized SIMM is a good compromise (see the figure). It offers a rugged for-



mat that most users can deal with, and its size gives most users a reasonable level of granularity for each storage-capacity increment. Furthermore, the small SIMM card is easier to remove than individual chips when system memory must be replaced with next-capacity generation DRAMs.

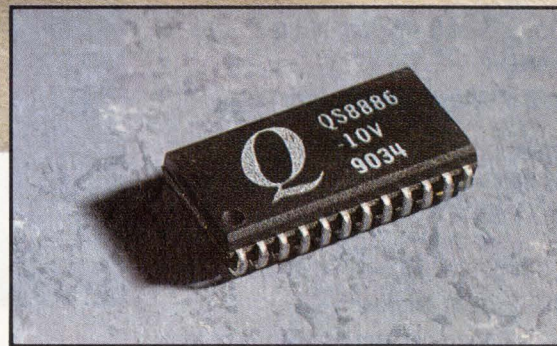
SIMMs have since caught on in a big way, with most system makers employing SIMMs for their hardware, even though the memory shortages have abated. Quantity pricing for the SIMMs isn't much higher than that for individual chips for 1-Mbyte units. Quantity prices for 1-Mbit DRAMs are now between \$3.50 and \$6.00, and SIMMs containing 8 or 9 chips are typically selling for about \$40 in large quantities and about \$50 to \$80 at the retail level.

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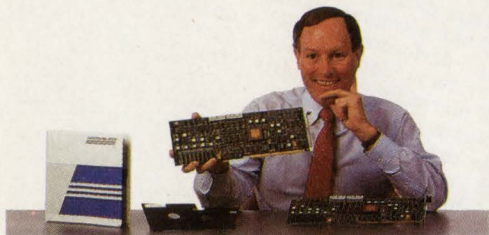


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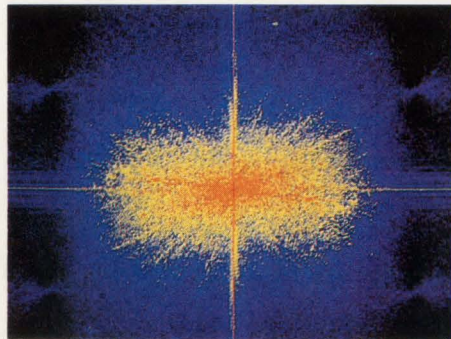
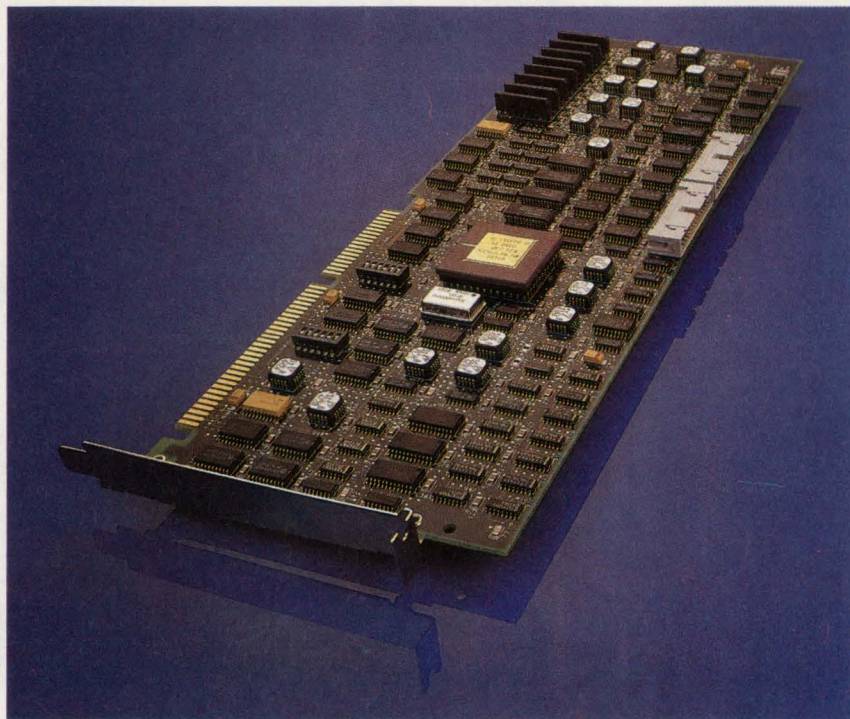
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# ADAPT NON-ISDN TERMINALS To ISDN DATA RATES

A MULTIPROTOCOL PROCESSOR WITH A 68000  
CORE IMPLEMENTS V.110 OR  
V.120 RATE ADAPTION.

ROBERT W. O'DELL  
AND MOTI KURNICK  
Motorola Inc.,  
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# T

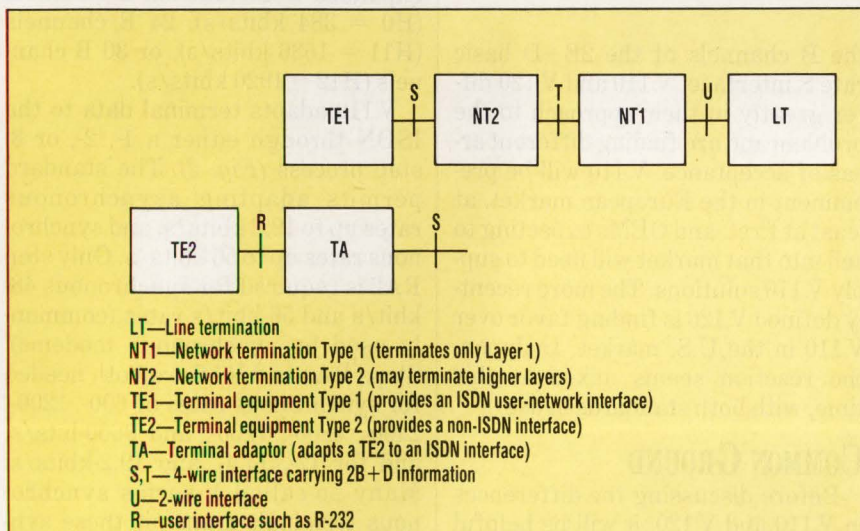
he emergence of the Integrated Services Digital Network (ISDN) raises a problem: How can vast quantities of older, non-ISDN compatible equipment be used with ISDN? Addressing this issue, the CCITT (Consultative Committee for International Telegraph and

Telephone) proposed the V.110 and V.120 interface standards, which solve this problem in two different ways. These standards are usually referred to as Rate Adaption methods, because a large part of their content is devoted to adapting the data rates of various terminal equipment (50 bits/s to 56 kbits/s) to the 64-kbit/s basic rate of ISDN.

The MC68302 Integrated Multiprotocol Processor from Motorola integrates

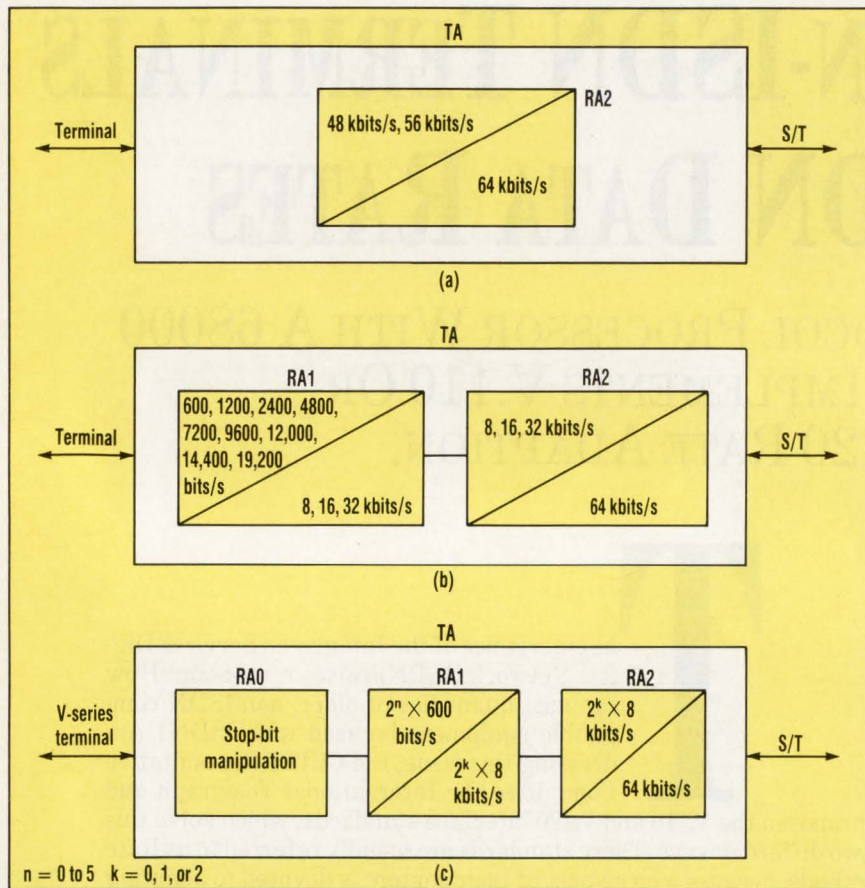
the well-known 68000 core with three serial communications controllers and other peripherals, making it ideal for implementing many communications protocols in both general-purpose and ISDN environments (See "Inside the 68302," p. 66). This article shows how the 68302's features can be used in ISDN to implement V.110 or V.120.

Basic-rate ISDN uses two 64-kbit/s channels to transmit some combination of voice or data information. These two channels are called bearer channels, or B channels. Configuring the B channels requires using an additional 16-kbit/s channel, called the D channel. These three channels extend from the terminal de-



**1. BASIC ISDN** components include TE1 (ISDN) and TE2 (non-ISDN) terminals. The R interface is defined by users and is often a common interface, such as RS-232. The TA, or terminal adaptor, block (the subject of this article) interfaces non-ISDN terminal equipment to the network. The LT box is the line termination at the central office. Between the terminal and the LT box may be a network termination device, such as a PBX. The S and T reference points are physically 4-wire interfaces, while the U interface is 2-wire.

**DESIGN APPLICATIONS**  
**MULTIPROTOCOL**  
**ISDN CONTROLLER**



**2. ADAPTING A SYNCHRONOUS 48-kbit/s or 56-kbit/s terminal to the 64-kbit/s B channel requires only step RA2 (a). Adapting lower synchronous data rates requires two steps (b). Asynchronous terminals require a stop-bit shaving function in addition to the two-step adaption process (c).**

vice (such as an ISDN phone or ISDN card in a personal computer) to the central office through a set of interfaces and functions defined by the ISDN reference model (Fig. 1). The S and T interfaces are physically the same 4-wire interface, while the U interface is a 2-wire interface.

If a terminal device is ISDN-compatible, it can directly access the 2B+D channels of ISDN, as shown by the TE1 box in the figure. If the terminal device isn't ISDN-compatible (as in a TE2, for example), it must be adapted with a box that can access the 2B+D channels. This is where V.110 and V.120 step in.

The V.110 and V.120 standards implement the Terminal Adaptor (TA) function as shown in the ISDN reference model (Fig. 1, again). They link non-ISDN terminal equipment (terminals and computers) into one of

the B channels of the 2B+D basic rate S interface. V.110 and V.120 differ greatly in their approach to the problem and are finding different areas of acceptance. V.110 will be pre-eminent in the European market, at least at first, and OEMs expecting to sell into that market will need to supply V.110 solutions. The more recently defined V.120 is finding favor over V.110 in the U.S. market. In Japan, the reaction seems mixed at this time, with both standards in use.

### COMMON GROUND

Before discussing the differences in V.110 and V.120, it will be helpful to discuss what they share in common. First, both standards offer the ability to transmit data from non-ISDN terminal equipment over one of the B channels, through an ISDN to other non-ISDN terminal equip-

ment. Both can rate adapt slower equipment up to the 64 kbit/s B-channel rate. Both accept data from this terminal equipment over standard R interfaces such as RS-232 or RS-244. Finally, both require a call to be established on the D channel before this data transfer can begin. Data is transferred on the D channel using an HDLC (high-level data-link control)-type protocol called Link Access Procedure D, or LAPD.

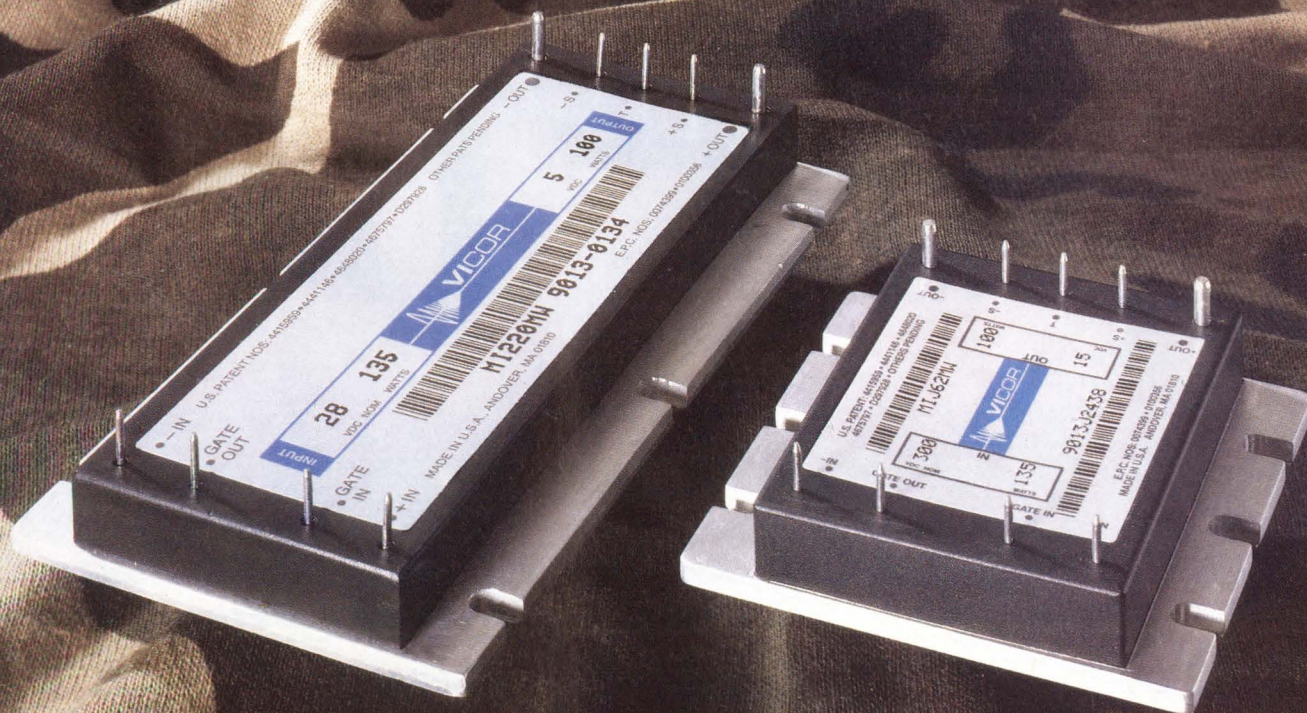
What are the major differences? V.110 sends all information received over the R interface onto selected bits of a B channel, similar to a virtual circuit. The negotiated bits of the B channel are permanently assigned to the terminal for the duration of the transfer. All V.110 data is sent over the B channel in an 80-bit frame.

V.120, on the other hand, extracts data from the R interface, packetizes data into LAPD-type frames, and sends it over the B channel using LAPD techniques. As a result, data packets need not be received in a regular, periodic fashion, as with V.110. This characteristic enables data from multiple terminals to be statistically multiplexed over a B channel using V.120, or if properly negotiated, over more than just one B channel. The V.120 data rate may also be expanded to include six B channels (H0 = 384 kbit/s), 24 B channels (H11 = 1536 kbit/s), or 30 B channels (H12 = 1920 kbit/s).

V.110 adapts terminal data to the ISDN through either a 1-, 2-, or 3-step process (Fig. 2). The standard permits adapting asynchronous rates up to 19.2 kbit/s, and synchronous rates up to 56 kbit/s. Only step RA2 is required for synchronous 48-kbit/s and 56-kbit/s rates (commonly used by synchronous modems). Steps RA1 and RA2 are both needed for synchronous rates of 600-, 1200-, 2400-, 4800-, 7200-, and 9600-bits/s, and for 12-, 14.4-, and 19.2-kbit/s. Many so-called V-series synchronous terminals transmit these synchronous rates. The terminals are widely available in Europe.

Adapting asynchronous terminals with up to 19.2-kbit/s data rates to ISDN requires all three steps. This is because the process of rate-adapting

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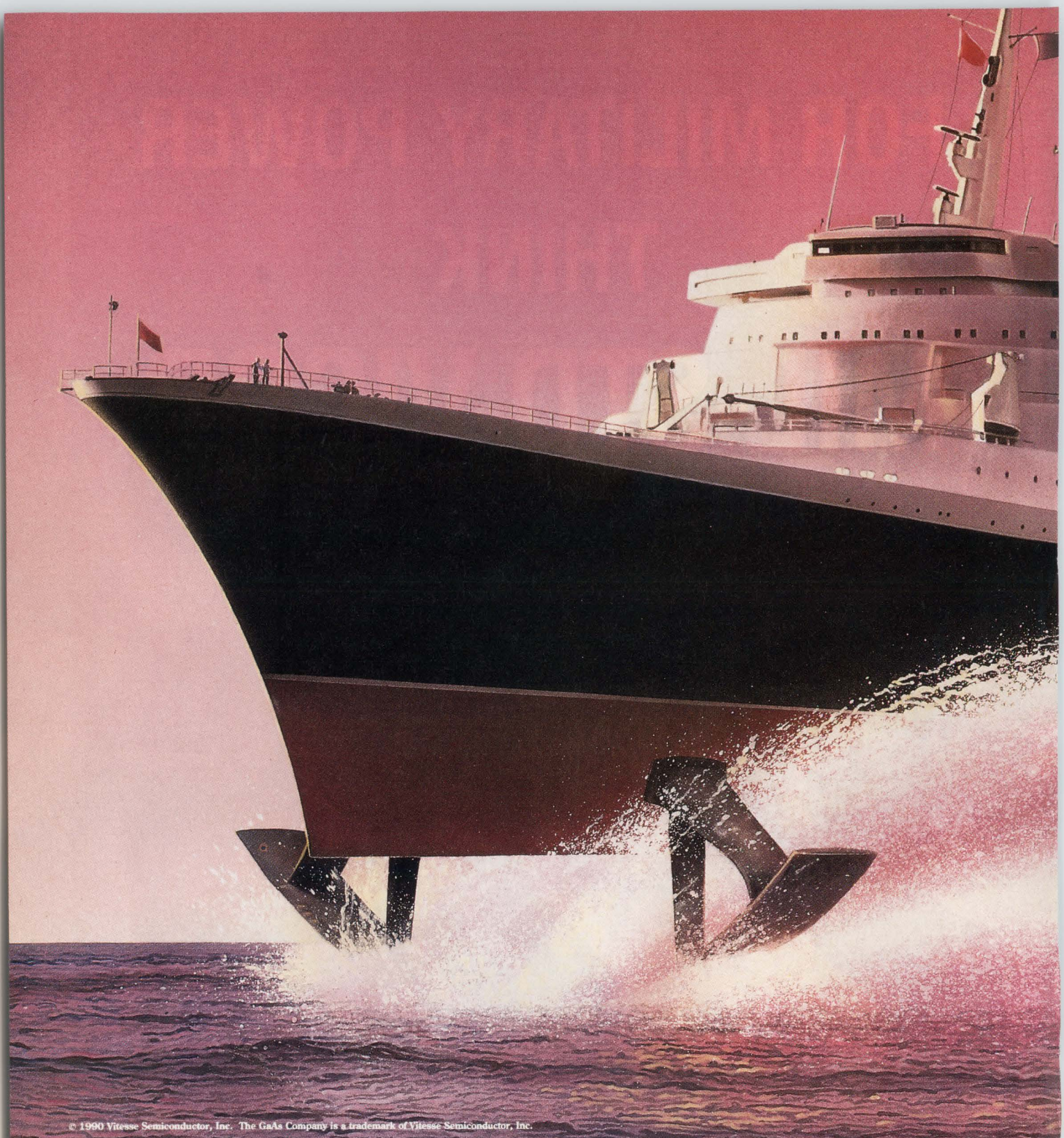
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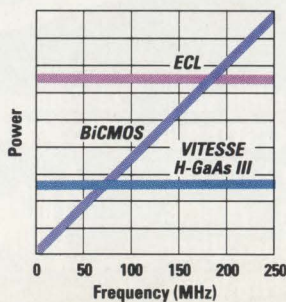


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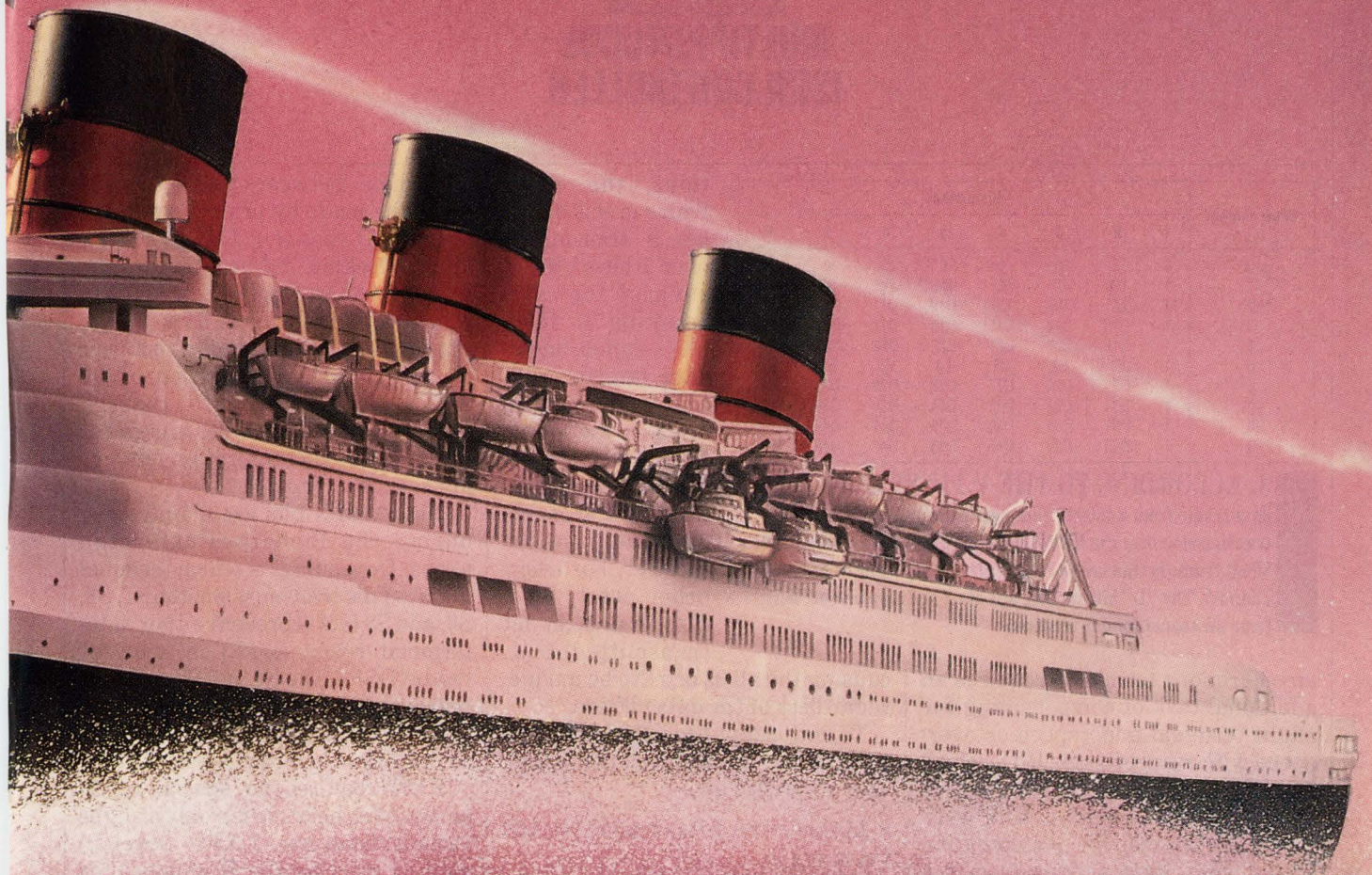
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# MULTIPROTOCOL ISDN CONTROLLER

Octet number	Bit number							
	1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0
1	1	D1	D2	D3	D4	D5	D6	S1
2	1	D7	D8	D9	D10	D11	D12	X
3	1	D13	D14	D15	D16	D17	D18	S3
4	1	D19	D20	D21	D22	D23	D24	S4
5	1	E1	E2	E3	E4	E5	E6	E7
6	1	D25	D26	D27	D28	D29	D30	S6
7	1	D31	D32	D33	D34	D35	D36	X
8	1	D37	D38	D39	D40	D41	D42	S8
9	1	D43	D44	D45	D46	D47	D48	S9

**3. ACCORDING TO THE V.110 STANDARD, a data frame from a 4800-bit/s source is formatted for transmission over the ISDN B channel in ten 8-bit octets. This 80-bit frame is transmitted over only one bit of the 64-kbit/s B channel. The "D" bits include any start and stop bits present from an asynchronous terminal.**

asynchronous terminals requires an additional task of compensating for slight terminal underspeed or overspeed with respect to the ISDN clock rate. Thus, the RA0 function refers to stop-bit manipulation. The difficult case in stop-bit manipulation arises when data arrives from the ISDN into the terminal adaptor slightly faster than it's sent from the terminal adaptor to the terminal. If this situation goes uncompensated, data can build up until it overflows the buffers in the terminal adaptor. To avoid this problem, stop bits may be "shaved" by up to 12.5% for most data rates, and up to 25% for data rates less than or equal to 300 bits/s.

In addition, the data rate itself must be mapped into one of six synchronous rates. In the asynchronous case, data from terminals with data rates as low as 50 bits/s can pass through the RA0 function mapped into the nearest ( $2^n \times 600$ )-bit/s data rate (where  $n = 0$  to 5).

The reference model diagram for the RA2 function doesn't clearly show that if slower rates are adapted to the ISDN, then only 1, 2, or 4 bits of the B channel may be required to transmit V.110 data. In this case, it's possible for other terminals to use remaining B-channel bits for other V.110 transmissions.

A typical 80-bit frame contains synchronization information (0s and 1s), data (D bits), signalling rate and clocking information (E bits), and S and X channel-control bits (Fig. 3). To perform the RA1 and RA2 func-

tions, the 80-bit frame in this example is transmitted over 1 bit of the B channel for rate-adapting a 4800-bit/s synchronous data rate to an 8-kbit/s data rate. Each 80-bit frame begins with an all-0s octet, which is used for frame synchronization by the receiver. For every other octet, bit 0 (the first octet bit transmitted) is 1,

causing the all-0s octet to be unique, regardless of the data pattern.

To rate adapt the 4800-bit/s rate, 48 data bits are included per frame. This is verified as:

$$8 \text{ kbits/s} / (80 \text{ bits/frame}) = 100 \text{ frames/s}$$

$$48 \text{ bits} \times 100 \text{ frames/s} = 4800 \text{ bits/s}$$

One common area of confusion in the V.110 standard relates to the definition of the D bits. Although they're termed data bits, they can also transmit start bits and stop bits for asynchronous terminals. The idea is simply to transmit *all* information from the terminal through the ISDN, as if the channel were a transparent line.

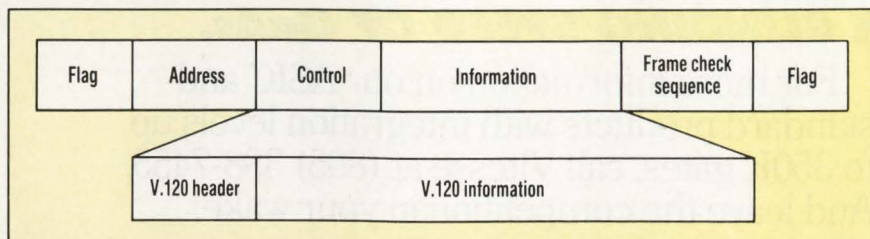
The E1-E3 bits define the format of the 80-bit frame. For instance, the pattern would be 011 with this frame. It would designate either 4800-bit/s rate adaption to an 8-kbit/s rate using one B-channel bit, 9600-bit/s rate adaption to a 16-kbit/s rate using two B-channel bits, or 19.2-kbit/s rate adaption to a 32-kbit/s rate using four B-channel bits (the

distinction between these 3 types would be made by prior negotiation over the D channel). The E4-E6 bits allow clocking information to be transmitted through the ISDN to other user equipment. This allows phase information relating to a user clock, which is within 100 ppm of the ISDN clock rate, to be passed through the ISDN. Bit E7 is used for multiframe synchronization for very low terminal rates.

The S and X bits are mainly used during the B-channel call-setup phase. Depending on which terminal initiated the transmission, the S1, S3, S6, and S8 bits represent either data-terminal ready (DTR) or data-set ready (DSR). The S4 and S9 bits represent ready to send (RTS) or carrier detect (CD), and the X bits represent a frame sync or clear to send (CTS).

V.120 requires no special reference model, because it's only a slight variant from the LAPD (level 2) method used on the D channel for call setup. It doesn't need to distinguish between various speeds and terminal clocking methods. The frame structure for V.120 is an enhancement of LAPD (Fig. 4).

The differences between V.120 and LAPD are worth noting. First, no distinction between the user and the network exists as in LAPD. This is because the transfers are sent to terminal equipment, not to the network for call control. Second, information frames may be sent as response frames, rather than just the standard receiver ready (RR), receiver-not-ready (RNR) type responses. This increases efficiency in an environment where information frames are the rule rather than the exception. Third, the frame reject (FRMR) message may be sent as a response.



**4. A LAPD + PROTOCOL for B-channel V.120 transmission is an extension of the common LAPD protocol. V.120 field information contains data directly sent from the terminal. The remaining frame space is allotted to LAPD + protocol overhead.**



# MULTIPROTOCOL ISDN CONTROLLER

the 68302 arrive at priority-level four, with an individual vector internally supplied for each source.

The IDL interface is implemented with pins L1RQ, L1GR, L1SY0, L1RXD, L1TXD, L1CLK, and L1SY1 of the 68302. From this one physical interface, the D-channel and B-channel are extracted and routed to SCC1 and SCC3 on the 68302. The SCPTXD, SCPRXD, SPCLK, PA7,

and PA8 signals from the 68302 make it possible for commands to be sent to the 145475. This is done through the separate SCP channel on the 68302.

In this example, the devices are clocked with separate crystal frequencies. However, it is possible to clock the 68302 at speeds from 8 to 16.67 MHz. With a 16.67-MHz clock, the SCCs use only 1% of the 68302

bus bandwidth. Therefore, there's ample time to execute the higher layer LAPD protocol on the D channel, and to format V.110 or execute the LAPD+ protocol for the B channel, plus terminal control. Results taken from actual Motorola-developed LAPD software show that an entire V.120 application would require less than 50% of the 68302 performance bandwidth. Port SCC2 is connected

## INSIDE THE 68302

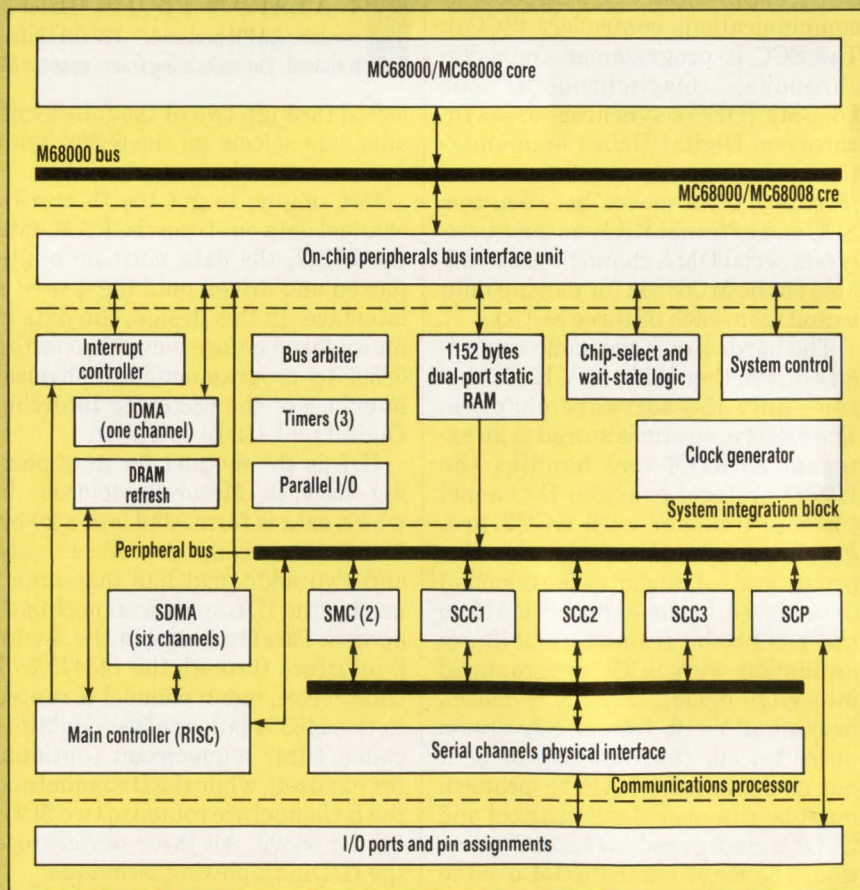
**T**he MC68302 Integrated Multiprotocol Processor (IMP) combines the benefits of the 68000 microprocessor with a flexible communications architecture (see the diagram). The CMOS device incorporates a 68000 core processor (16.67 MHz), a communications processor with associated peripherals, and a system-integration block.

The 68000 core processor is instruction-set and timing compatible with the 68000 microprocessor (16-bit) version of the 68000 family. It differs from the 68000 microprocessor in just a few of its external signals. First, a BUSW signal has been added, which selects whether the device supports the 16-bit 68000 or the 8-bit 68008 data-bus widths. This option is chosen during reset. Second, an RMC signal may be used as a bus lock. RMC is asserted externally during instructions with read-modify-write cycles. Third, an internal IPEND signal has been added to support a low-latency interrupt mechanism. Finally, the 68000 core processor on the 68302 differs in that it doesn't support the older 6800-family of peripherals. As a result,  $\overline{VMA}$  and  $\overline{E}$  signals are eliminated, and  $\overline{VPA}$  is retained simply as the autovector input AVEC.

The communications processor consists of a RISC processor, three SCCs (serial communication controllers), six DMA channels for the three SCCs, a programmable physical interface, a serial communication port (SCP), and two serial management control-

lers (SMCs). The RISC processor is a separate processor from the 68000 core, and is dedicated to the service of the SCCs, SCP, and SMCs. It works with these channels to implement the user-chosen protocol, and to manage the six DMA channels that transfer data between the SCCs and memory. It also executes commands issued by the 68000 core and generates interrupts to the on-chip interrupt controller. The 302 supports three full-duplex independent SCCs

that support the following protocols: HDLC/SDLC, UART, BISO, DDCMP, V.110, and fully-transparent operation. Two DMA channels, which are dedicated to each of the three SCCs, transmit data between the SCCs and internal dual-port RAM, or directly between the SCCs and external memory. Data from each SCC may be received into (or transmitted out of) as many as 8 buffers, without intervention from the 68000 core.



## MULTIPROTOCOL ISDN CONTROLLER

to a terminal device through the 145407 RS-232 driver device. In this design, an asynchronous (UART) mode is chosen for SCC2. To perform the stop-bit manipulation function in V.110 applications, the SCC in its UART mode is configured to shave stop bits by 12.5%. This function is handled automatically by the SCC and can be enabled and disabled dynamically. The internal clock is gen-

erated from SCC2's baud-rate generator, which can generate baud rates from 150 baud to 347-kbaud using the internal 16.67-MHz clock.

The SCC2 port is operating as a DCE (data-communication equipment, such as network line card) rather than a DTE (data-terminal equipment, such as a handset). Therefore, the TXD2 and RXD2 pins are connected to the terminal's RXD

and TXD pins, respectively. The terminal's CD and CTS lines are driven by parallel ports PA2 and PA5 on the MC68302. These two I/O pins were reassigned from SCC2's RTS2 and RCLK2 pins, which aren't needed for this design.

The 68302 receives the terminal's RTS and DTR lines through its CD2 and CTS2 pins, respectively. These pins may be configured to automati-

The physical interface supports a standard nonmultiplexed interface for each of the three SCCs (TXD, RXD, TCLK, RCLK, CTS, RTS, and CD), as well as several multiplexed modes. In the multiplexed modes, up to three SCCs can be time-multiplexed onto the same serial channel. The multiplexed modes include IDL, GCI, and PCM Highway. IDL and GCI are alternative standards for moving 2B+D data between ISDN devices. IDL was developed by Motorola, and GCI was defined from IOM-2 in Europe. PCM Highway is commonly used with T1 or CEPT lines, carrying 24 8-bit channels at 1.544-Mbit/s or 32 8-bit channels at 2.048-Mbit/s data rates, respectively.

The SCP is a full-duplex, synchronous, character-oriented channel that provides a three-wire interface. It's used as a control channel for IDL, or as a means to communicate with other serial-peripheral-interface-type (SPI) devices. The SCP implements a subset of Motorola's SPI interface. The two SMCs transmit and receive local control information multiplexed with the 2B+D data in the IDL or GCI buses.

The systems-integration block incorporates general-purpose peripherals that eliminate the glue logic used in most 68000 systems. It includes an independent DMA controller (IDMA), an interrupt controller, parallel I/O ports, an 1152-byte dual-port RAM, two timers, and a watchdog timer. The systems-integration block also has chip-select lines, wait-state-

generation logic, a bus arbiter, low-power modes, core-disable logic, an on-chip clock generator, and a hardware watchdog.

The IDMA controller can transfer data at up to 4-Mbytes/s. It performs data packing and unpacking for odd address transfers. The controller can transfer both 8- and 16-bit quantities, and supports peripherals with DREQ, DACK, and DONE lines. Requests may be generated internally with limited or full bandwidth, or externally by a peripheral.

The interrupt controller supports a total of 15 internal sources and 3 external sources. It can supply vectors for all sources, and can also supply dedicated interrupt-acknowledge signals to the external sources.

A total of 28 I/O lines are multiplexed with the three SCCs and SCP. Regardless of the way the on-chip peripherals are configured, at least five I/O lines are always available, four of which can interrupt the 68000 core.

The dual-port RAM offers 576 bytes of additional system RAM for general use, such as data buffer storage, and 576 bytes of parameter RAM used to initialize, configure, and control the communications processor. It supplies zero wait states to the 68000 core, regardless of whether the communications processor is currently accessing this RAM. If necessary, the communications processor is held off by one clock cycle to avoid contention.

Two general-purpose 16-bit timers support capture and output

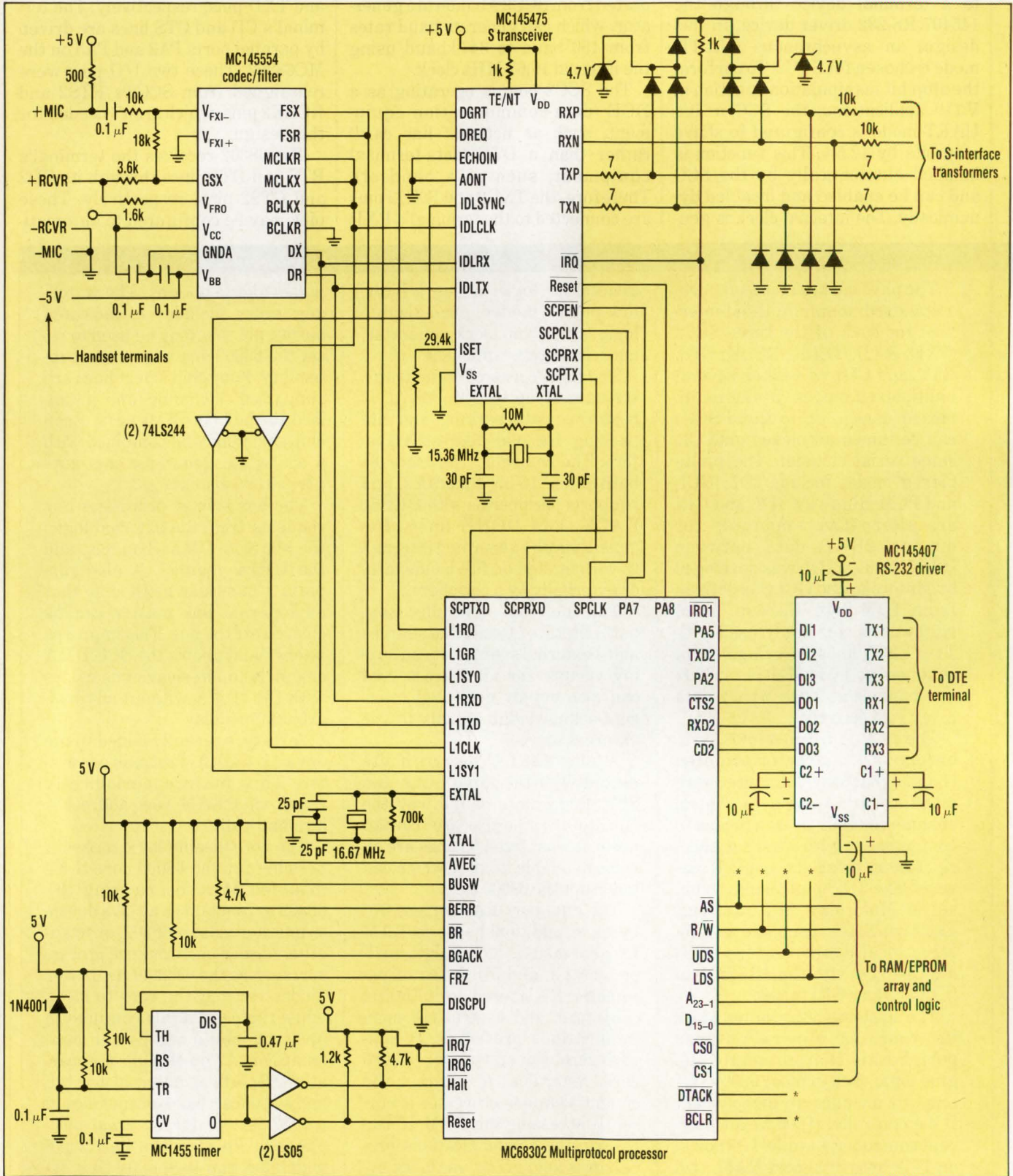
pulse/toggle options. The watchdog timer includes a dedicated output pin that may be used to reset the 68302 and an interrupt capability. Four chip-select lines are supported, including one initialized to the boot-ROM area. Each chip select may be combined with a wait-state generator that supports 0 to 6 wait states.

The bus arbiter prioritizes bus requests from the external logic, the six SCC DMA channels, and the IDMA channel. It also supports a bus-clear method so that an external bus master can be cleared off the bus. This improves latency and allows the SCC DMA channels to interleave bus cycles with the IDMA without any bus-arbitration delay.

A feature recently added to the device is a DRAM refresh controller. This feature periodically reads all DRAM row addresses automatically.

The core-disable logic makes it possible for the 68000 core to be disabled at reset, causing the 68302 to function as a slave device to another master 68302, or to another higher-performance processor, such as the 68020. Low-power modes can put the core to sleep while the peripherals continue to operate, reducing power consumption. An on-chip clock generator supports an external crystal, and supplies a clock-output signal to the rest of the external peripherals. Finally, the hardware watchdog can terminate bus cycles when no peripheral responds to a read or write cycle from the 68302.

# MULTIPROTOCOL ISDN CONTROLLER



6. THE DESIGN OF A V.110/ V.120 terminal adaptor uses all three SCCs on the MC68302, including the additional SCP port. The 68000 core on the MC68302 is the only processor required in the design. Control lines marked with an asterisk (\*) connect to the 5-V supply through 10-kΩ pull-up resistors.

## MULTIPROTOCOL ISDN CONTROLLER

cally enable transfers of data to or from the terminal. Consequently, the SCC mode register configures SCC2 in the automatic mode.

The MC1455 timer generates the output pulse to satisfy the power-on reset requirements of the 68302. This application example uses 64-kbytes of EPROM and 64-kbytes of static RAM. The chip-select and wait-state-generation logic on the 68302 contribute to memory-design simplicity. The Chip Select 0 signal to the ROM only activates for read cycles, while Chip Select 1 is activated for both read and write cycles.

Chip Select 0 has the added property of coming up enabled after reset for the first 8 kbytes of the address space. This is enough space for configuring the rest of the chip selects. The 68302's six SDMA channels will move data between the three SCCs and external RAM. These DMA cycles are identical to the 68000 core cycles, and may occur with wait states. The wait-state-generation logic provides DTACK automatically after the programmed number of wait states (0 to 6).

The crystal circuit is a typical configuration (Fig. 6, again). Of course, an oscillator could replace the crystal circuit. The AVEC pin is pulled high because autovectoring for external interrupts isn't needed. If external devices were added (not shown), the MC68302 interrupt controller could handle the interrupt vector generation. The BUSW pin is pulled high for 16-bit operation and may not be modified dynamically. Two memory chips (EPROM and RAM) are required for 8-bit operation. Another pair of devices is needed for 16-bit operation.

Pin BERR is pulled high because it's an open-drain connection. It will be asserted low by the MC68302 if the on-chip hardware watchdog timer terminates a stalled bus cycle. Pin BR is tied high because no external bus masters exist in this design. Pin BGACK is pulled high (inactive) and is asserted low during an IDMA or SDMA bus cycle. The FRZ pin is tied high since the MC68302 freeze-debugging logic is not used in this design. Pin DISCPU is tied low so that

the M68000 core on the 68302 can function normally. Tying this pin high causes the part to enter the Disable CPU mode and become an intelligent peripheral. This mode would be useful if more than three SCCs were required, but only one 68000 core needed to be operating.

Arbitration is handled by the Bus Arbitration Unit in the following priority: External Bus Master (not required in this application), SDMA channels, IDMA channel, and 68000 core cycles. Consequently, the SDMA channels have the highest priority. If the Independent DMA were required, the SDMA channels can cycle-steal from the IDMA, without any wasted time for external bus arbitration. This arbitration is handled internally. The BGACK pin is asserted externally by the IDMA or SDMA when the arbitration is complete.

The 68302 timers may be used as LAPD protocol timers, generating interrupts to the 68000 core. In addition, the watchdog timer can generate an interrupt, or use the WDOG output signal to assert a chip reset whenever an unexpected system state is encountered.

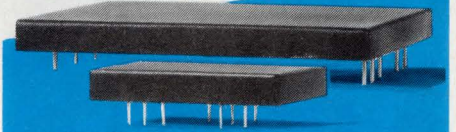
The 68302 combines a large number of peripherals with a low power, high performance 68000 core for implementing many complex control functions. The multiprotocol processor is ideal for ISDN-based systems and many other communications applications. Both V.110 and V.120 rate-adaption applications can be implemented with the hardware configuration discussed in this article. □

*Robert O'Dell, senior applications engineer in Motorola's 68000 Operations Group, has a BSES from the University of South Florida and an MSCS from the University of Texas at Austin.*

*Moti Kurnick, design engineering manager for the MC68302, holds a BSEE from Beer-Shave University.*

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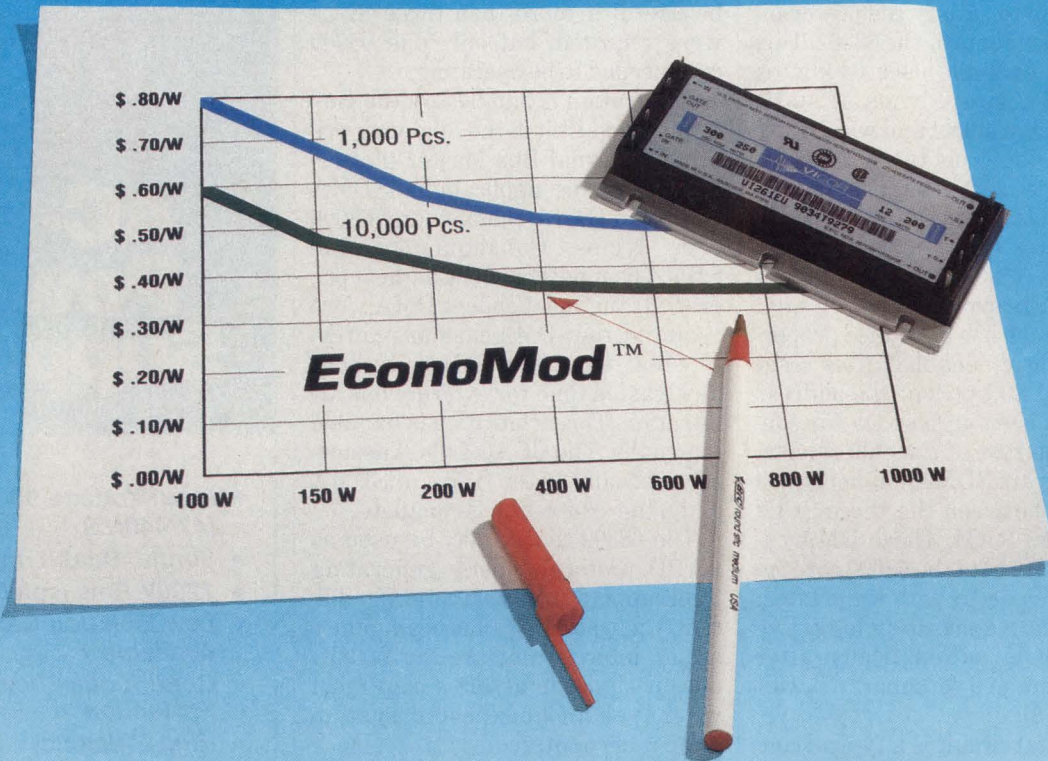
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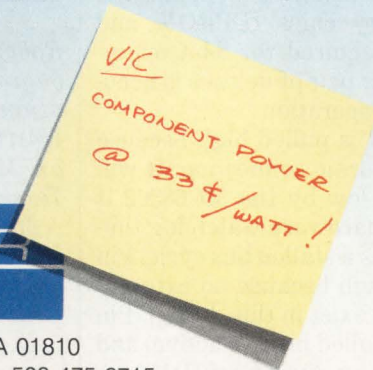


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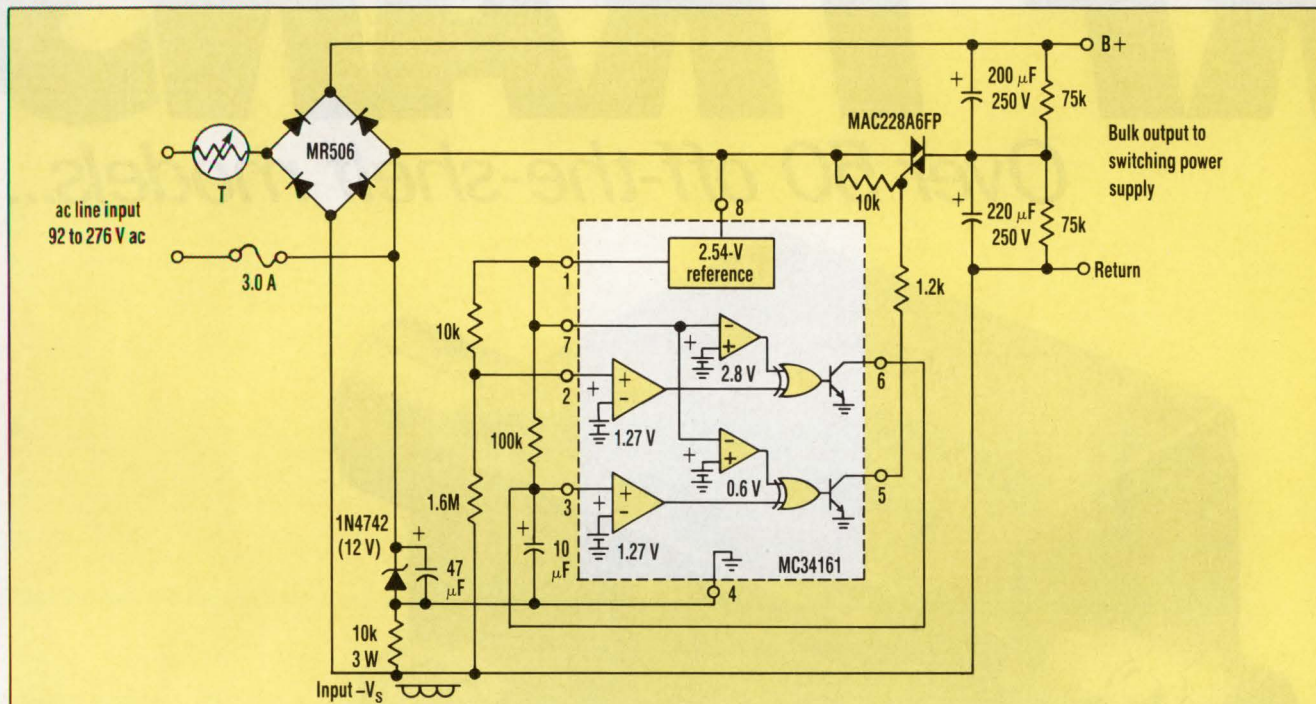


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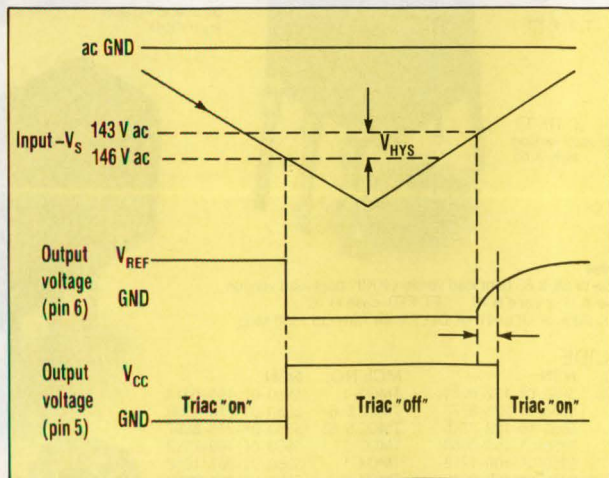
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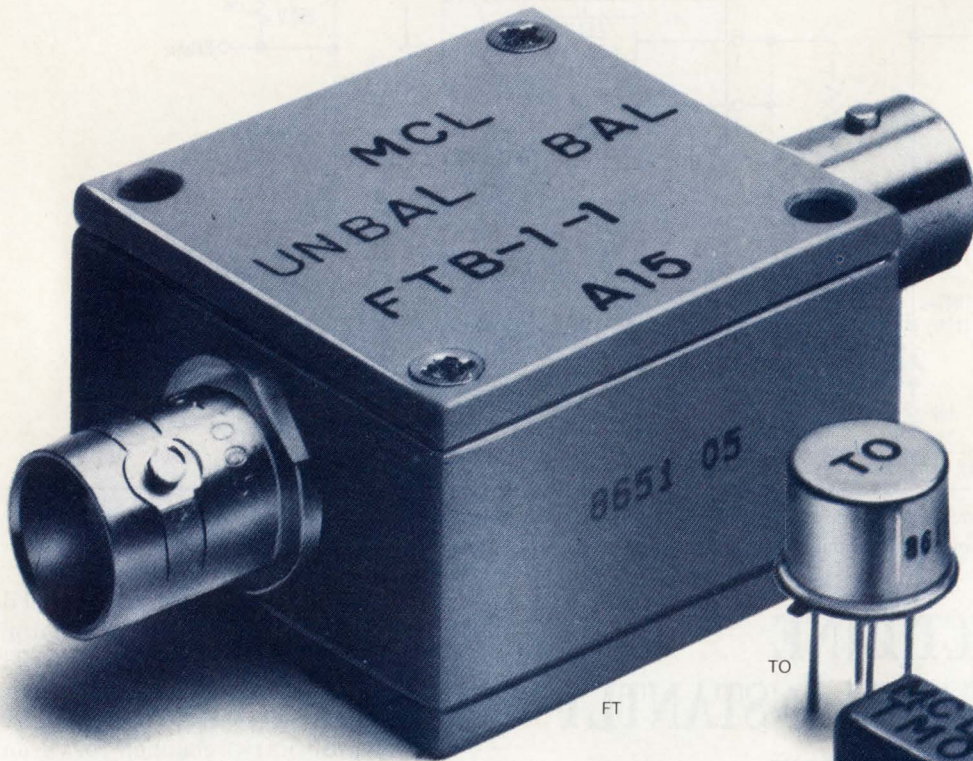
This highly flexible dual-channel device can be configured to monitor a wide range of input voltages. The chip's flexibility is achieved by using a Mode Select input that lets users program its two channels for various voltage-sensing applications. In this application, the Mode Select input is tied to  $V_{REF}$ , allowing one channel to sense overvoltage and the other undervoltage.

When the circuit's input voltage is less than 146 V ac, the triac is gated continuously, causing the input diodes to double the ac line voltage. When the input is greater than 146 V ac, the triac is off, causing the input diodes to act as a full-wave bridge rectifier. In either case, the switching power supply's input receives an input voltage that's equal to operation at 240 V ac.

The MC34161's first input (pin 2) is set for undervoltage sensing. This channel senses the negative half cycles of the ac line voltage. The 1.6-M $\Omega$  and 10-k $\Omega$  resistors set up a divider network to trip at 146 V during power up and 143 V during power down. If the ac line voltage is less than 146 V, this channel's output will be off, allowing the 10- $\mu$ F capacitor

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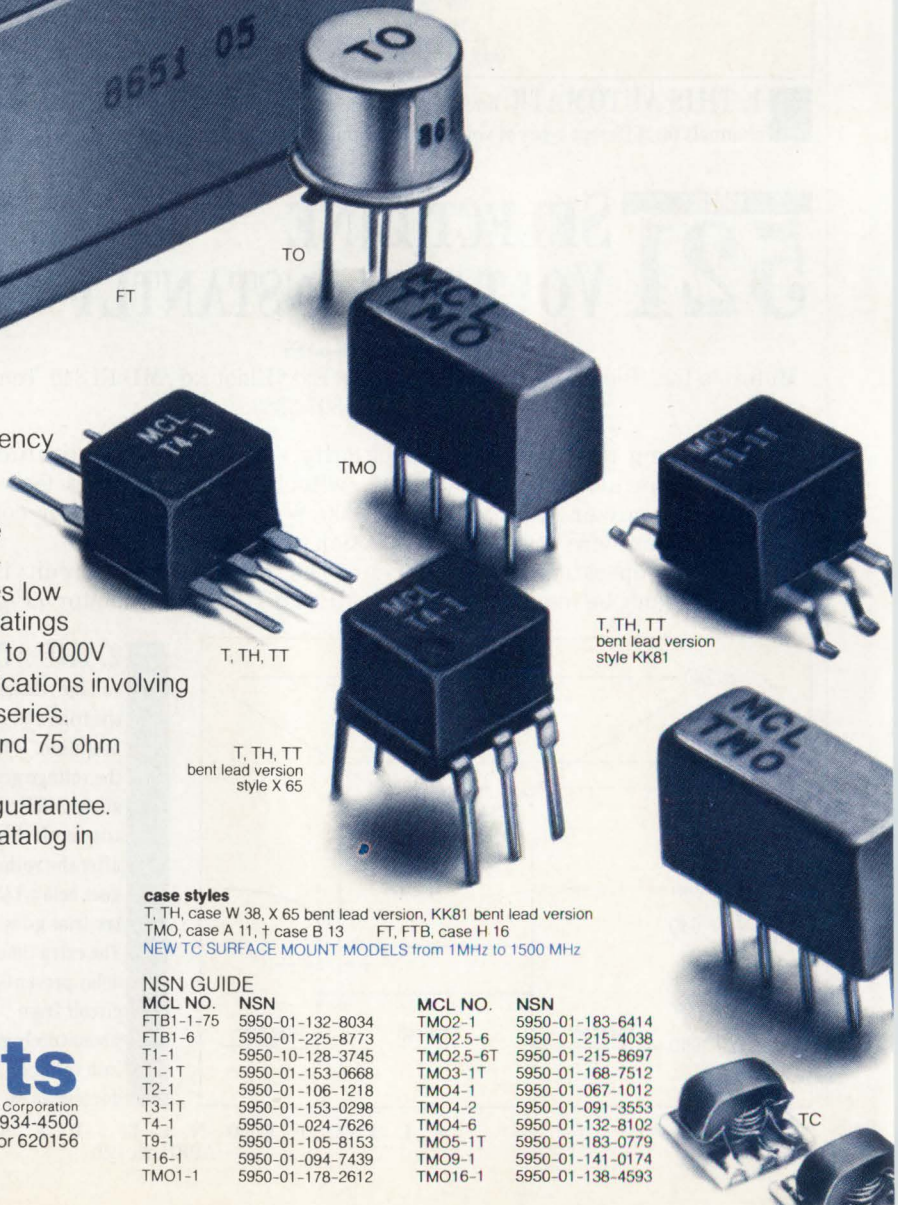


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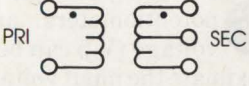
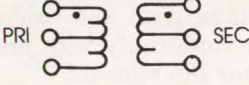
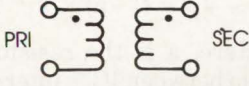
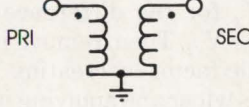
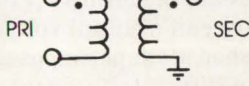
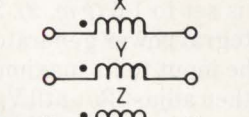
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		T2.5-6T	2.5	.01-100	.01-100	.02-50	50-20	4.95	
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		T4-1	4	2-350	2-350	.35-300	2-100	3.25	
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		TMO2-1T	2	.07-200	.07-200	1-100	5-50	8.45	
		†TMO2.5-6T	2.5	.01-100	.01-100	.02-50	05-20	8.45	
		†TMO3-1T	3	.05-250	.05-250	1-200	5-70	7.95	
TMO4-1	4	2-350	2-350	35-300	2-100	6.25			
TMO5-1T	5	3-300	3-300	6-200	5-100	8.45			
TMO13-1T	13	3-120	3-120	7-80	5-20	8.45			
<b>B*</b> 	TT	TT1-6	1	.004-500	.004-500	.02-200	1-50	6.95	
		TT1.5-1	1.5	.075-500	.075-500	2-100	1-50	5.95	
		TT2.5-6	2.5	.01-50	.01-50	.025-25	05-10	6.45	
		TT4-1	3	.05-200	2-50	2-50	1-30	5.95	
		TT4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	6.95	
		TT25-1	25	.02-30	.02-30	.05-20	1-10	9.95	
		TTMO25-1	25	.02-30	.02-30	.05-20	1-10	11.95	
		TTMO1-1	1	.005-100	.005-100	.01-75	05-40	11.45	
		TTMO4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	13.95	
		<b>C</b> 	T	T1-1	1	.15-400	.15-400	.35-200	2-50
T1.18-3	1.18			0.01-250	0.01-250	0.02-200	0.03-50	5.65	
T1-6	1			.01-150	.01-150	.02-100	05-50	5.65	
T1.5-1	1.5			.1-300	.1-300	2-150	5-80	4.45	
T1.5-6	1.5			.02-100	.02-100	.05-50	0.1-25	5.65	
T2.5-6	2.5			.01-100	.01-100	.02-50	05-20	4.45	
T4-6	4			.02-200	.02-200	.05-150	1-100	4.45	
T9-1	9			.15-200	.15-200	3-150	2-40	3.95	
T16-1	16			3-120	3-120	7-80	5-20	4.45	
T36-1	36			.03-20	.03-20	.05-10	1-5	6.95	
TO-75	1		10-500	—	10-500	40-250	6.95		
T1-1H	1		8-300	8-300	10-200	25-100	5.95		
T9-1H	9		2-90	2-90	3-75	6-50	6.45		
T16-H	16		7-85	7-85	10-65	15-40	6.45		
TMO1-02	1		1-800	1-800	2-500	—	9.45		
TMO1-1	1		15-400	15-400	35-200	2-50	6.25		
TMO1.5-1	1.5		.1-300	.1-300	2-150	5-8	8.45		
†TMO2.5-6	2.5		.01-100	.01-100	.02-50	05-20	7.95		
†TMO4-6	4		.02-200	.02-200	.05-150	1-100	7.95		
TMO6-1	6		3-200	3-200	5-150	5-50	7.95		
TMO9-1	9	.15-200	.15-200	3-150	2-40	7.95			
TMO16-1	16	3-120	3-120	7-80	5-20	7.95			
<b>D</b> 	T	T2-1	2	.050-600	.050-600	.1-400	5-200	3.95	
		T3-1	3	5-800	5-800	2-400	—	4.45	
		T4-2	4	2-600	2-600	5-500	2-250	3.95	
		T8-1	8	.15-250	.15-250	25-200	2-100	3.95	
		T14-1	14	2-150	2-150	5-100	2-50	4.95	
		TMO2-1	2	.050-600	.050-600	1-400	5-200	7.95	
	TMO3-1	3	5-800	5-800	2-400	—	8.45		
	TMO4-2	4	2-600	2-600	5-500	2-250	7.95		
	TMO8-1	8	.15-250	.15-250	25-200	2-100	7.95		
	TMO14-1	14	2-150	2-150	5-100	2-50	8.45		
	FT	FT1.22-1	1.22	.005-100	.005-100	.01-50	05-25	35.95	
		FT1.5-1	1.5	.1-400	.1-400	5-200	1-100	35.95	
	<b>E</b> 	FTB	FTB-1	1	2-500	2-500	.5-300	1-100	36.95
			FTB1-6	1	.01-125	.01-125	.05-50	1-25	36.95
■FTB-1-75			1	.5-500	5-500	5-300	10-100	36.95	
<b>F</b> 	T	T-622	1	0.1-200	0.1-200	0.5-100	5-80	3.25	
		T626	1	0.01-10	0.01-10	0.2-5	0.4-2	3.95	

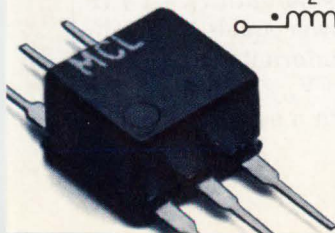
■ Denotes 75 ohm models

\* FOR A AND B CONFIGURATIONS

Maximum Amplitude Unbalance  
0.1 dB over 1 dB frequency range  
0.5 dB over entire frequency range

Maximum Phase Unbalance  
1.0° over 1 dB frequency range  
5.0° over entire frequency range

CIRCLE 165



to charge through the 100-kΩ resistor. Once the capacitor charges past the threshold voltage of the second input (pin 3), the triac is activated. This enables the circuit to act as a voltage doubler.

If the ac line voltage is greater than 146 V ac, the output of channel 1 (pin 6) is activated, pulling channel

2's input below its threshold. The triac is then turned off, making it possible for the input diodes to perform as a full-wave bridge (Fig. 2).

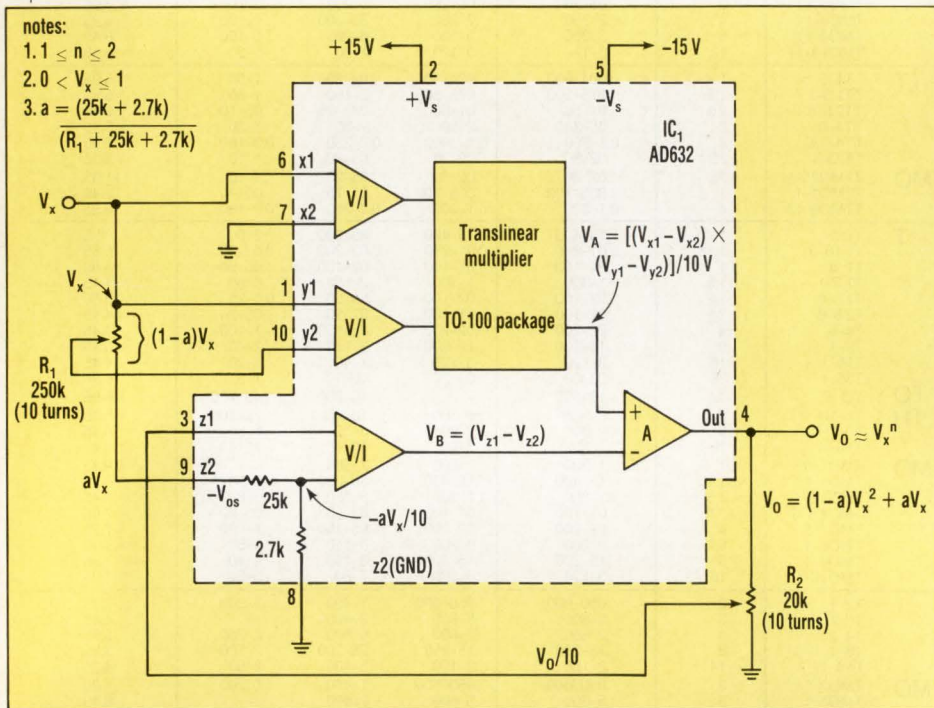
This circuit has two unique features. First, the circuit is powered by negative supply. This enables the triac to be activated in two of its more sensitive quadrants (quadrants 2

and 3), thus lowering the current requirement of the circuit. Second, only the negative half cycles are sensed, which could create a problem. However, because a delay is needed during power up to prevent the circuit from prematurely going into voltage-doubler mode, a time delay already exists. □

## CIRCLE 522 IC GENERATES NONINTEGRAL POWERS

ROBERT S. VILLANUCCI

Wentworth Institute of Technology, 550 Huntington Ave., Boston, MA 02115;  
(617) 442-9010.



By using a circuit built with an analog multiplier and two potentiometers, an output voltage ( $V_0$ ) can be made to approximate the input voltage raised to the power of  $n$  ( $V_x^n$ ) (Fig. 1). The value of  $n$  can be any nonintegral power between 1 and 2. The circuit comes in handy when a nonlinear sensor's output requires algebraic curve fitting. In addition, it can be scaled for the correct output-voltage level and calibrated for law conformity with just two resistor adjustments.

The circuit implements a series approximation that states:

$$V_0 \approx V_x^n = (1-a)V_x^2 + aV_x$$

Here,  $a$  is the resistor-divider ratio between  $IC_1$ 's internal 2.7- to 25-kΩ network and  $R_1$ 's setting. To create the approximation, start with the transfer function for the IC:

$$V_0 = \frac{(V_{x1} - V_{x2}) \times (V_{y1} - V_{y2})}{10V} = 10V \times (V_{z1} - V_{z2})$$

Substitute 0 V for  $V_{x2}$  and  $(1-a)V_x$  for the difference voltage,  $V_{y1} - V_{y2}$ . Then, remove  $IC_1$ 's 10-V scale factor by creating  $V_0/10$  on  $R_2$ 's wiper and applying it to the  $z1$  input. The approximation is completed by using the internal network at  $z2$  to create the term  $aV_x/10$ .

The circuit's output voltage can be seen when it's superimposed on a 1-V peak positive triangle-wave input, and  $n$  is set to 1.6 (Fig. 2). Scale the nonintegral power generator by setting the input to its maximum value (1 V), then adjust  $R_2$  until  $V_0 = 1$  V (1 raised to any power equals 1). To calibrate for law conformity, raise a convenient value of  $V_x$ , say 0.4 V, to the value of  $n$ . With  $n$  set to 1.6 in this

**1. WITH JUST** an analog multiplier and two potentiometers,  $V_0$  can approximate  $V_x^n$ , where  $n$  equals any nonintegral power between 1 and 2. The circuit can be scaled for the correct output voltage and calibrated for law conformity by adjusting  $R_1$  and  $R_2$ .

n	a	R <sub>1</sub> (setting)
1.0	1.00	0
1.2	0.72	38.47k
1.4	0.45	61.56k
1.6	0.30	92.34k
1.8	0.16	173.13k
2.0	0.00	∞

← Short  $R_1$

← Remove  $R_1$

**2. THE** circuit's output waveform is superimposed onto its input. In this case,  $n$  is set to 1.6. It shows that  $V_x^n \approx V_0$ .

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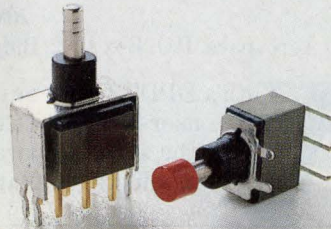
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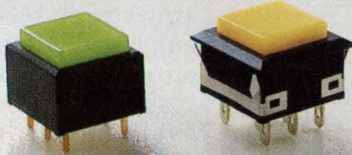
# 40<sup>TH</sup> YEAR of Innovation

### WORTH A MILLION



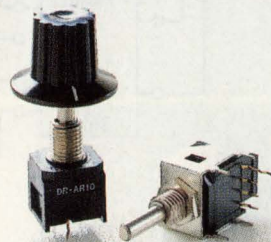
Million operations from unique LED illuminated JB keypad switch. Red, green or yellow LED options.

### DOUBLE DUTY



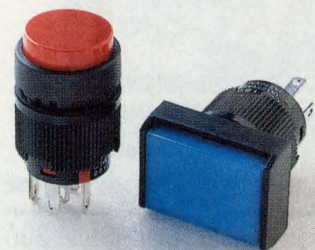
Logic-level for PCB or power rating for snap-in panel mounting, from very low-profile UB pushbuttons with full-face LED illumination.

### TURNING POINT



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CIRCLE 121

## IDEAS FOR DESIGN

circuit,  $V_o \approx 0.4^{1.6} \approx 0.231$  V. Adjust  $R_1$  until the output equals 0.231 V. The values of  $R_1$  vary from 0, when  $n = 1$ , to infinity, when  $n = 2$  (see the table). □

Reference:

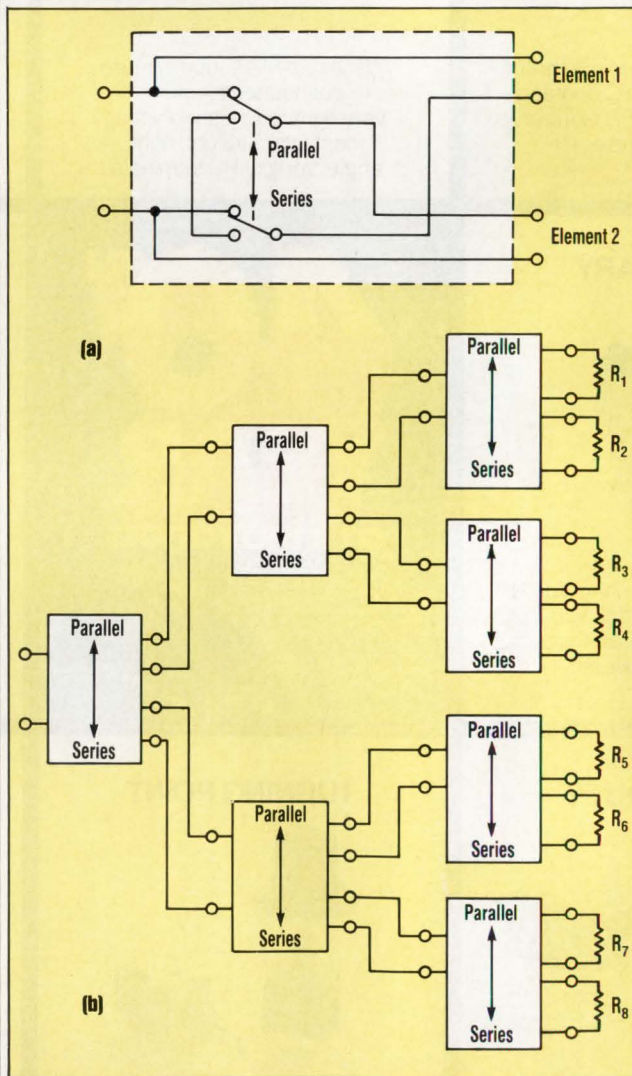
Analog Devices Inc. "AD632 Internally Trimmed Precision IC Multiplier" data sheet. Norwood, Mass., July, 1982.

# CIRCLE 523 SELECT SERIES OR PARALLEL COMBO

JON VICKLUND

Ball Aerospace, P.O. Box 1062, Bldg. FA-2, Boulder, CO 80306; (303) 939-4496.

**W**ith a DPDT switch or relay, users can select either the series or parallel combination of any two elements (see the figure, a). The elements used in the circuit can be any two-terminal device, such as a resistor, a capacitor, an inductor, or a battery or solar cell. Polarized as well as nonpolarized elements can also be used. The direction of the current within the element is the same regardless of which position the switch occupies.

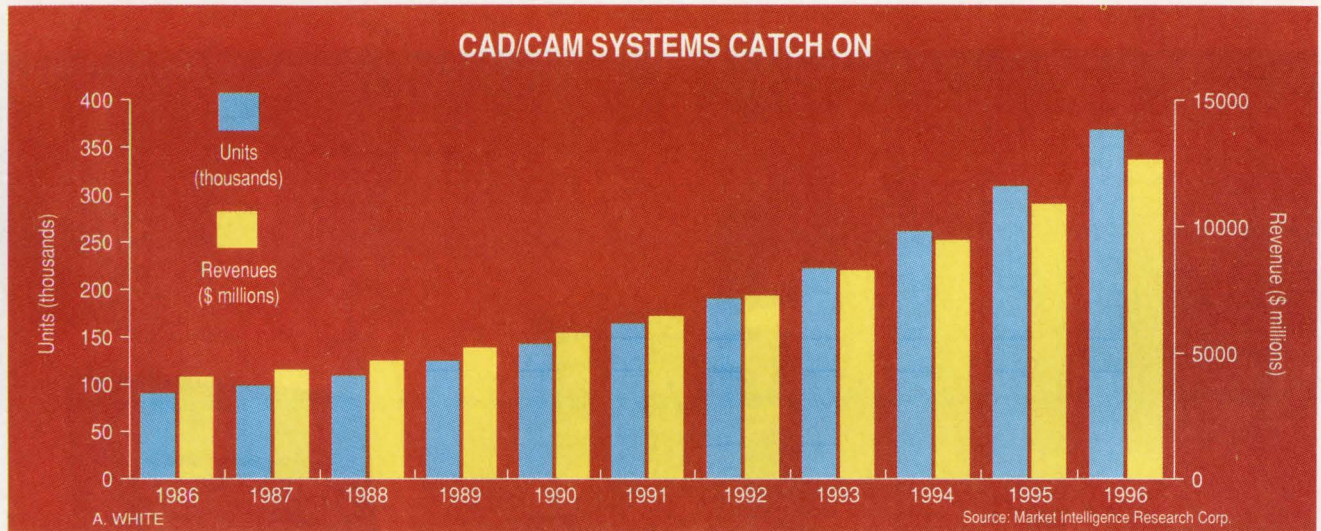


If several switches are ganged together, a load box is created (see the figure, b). This load box is very flexible, supplying loads for high-voltage, low-current sources when all the switches are in series or low-voltage, high-current sources when all the switches are in parallel. There are  $2^n$  combinations of loads, where  $n$  equals the number of DPDT switches or relays employed. Using different values for resistors  $R_{1-8}$  will avoid having repetitive combinations. □

**EITHER A SERIES OR A PARALLEL combination of any two, two-terminal devices can be selected by correctly configuring this circuit (a). By ganging several of the switches together, a load box can be created (b). The box supplies the loads for high-voltage, low-current sources (series) or low-voltage, high-current sources (parallel).**

# ELECTRONIC DESIGN QUICKLOOK

EDITED BY SHERRIE VAN TYLE



## MARKET FACTS

**C**omputer-aided design and manufacturing systems have changed the way engineers work. Apparently, engineers want more of the same. World revenues for CAD/CAM systems, which amounted to \$5.2 billion in 1989, should top \$12 billion by 1996. Growth in that period should average nearly 14%. So forecasts the Market Intelligence Research Corp.,

a Mountain View, Calif., market watcher.

Most CAD/CAM systems find use in the defense/aerospace industry. But while demand for CAD/CAM systems in the aerospace industry is expected to stay strong, the U. S. government will shift from defense spending to funding space programs, where CAD/CAM systems are called for as well.

Engineers can expect to pay less for the systems. As hardware costs decline, system prices will drop 2 to 4% a year, market researcher MIRC predicts. Prices for software,

though, will edge up. Makers of systems are turning to the Unix operating system, which should mean easier linking of diverse systems and better networking.

As for future growth, vendors of CAD/CAM systems are setting their sights on Europe. In 1989, European CAD/CAM revenues amounted to 44% vs. 43% for the U. S. By 1996, Europe's share should reach 49% vs. 37% for the U. S. The remaining 14% share falls to Asia, whose market share is expected to remain about the same.

## QUICK REVIEWS

**B**oth a refresher course on laser-printer technology and an in-depth look at the Hewlett-Packard Laserjet IIP, *LaserJet IIP Essentials* addresses most laser-printing issues in its 374 pages. The book, from Peachpit Press Inc., Berkeley, Calif., covers printer setup and configuration, hardware upgrading, Postscript cartridges, along with other enhancements. Several chapters deal with the technical and aesthetic aspects of using laser fonts. These chapters also supply the rudiments of typography and tips on using fonts with the IIP.

A companion book, *The LaserJet Font Book*, supplies more than 1000 samples of fonts available from a dozen font companies in its 368 pages. Both books will help the reader to fine-tune documents and presentation materials for that "just-right" look.

*LaserJet IIP Essentials* sells for \$21.95; *The LaserJet Font Book*, for \$24.95, in bookstores. They can be ordered from Peachpit (ISBN 0-938151-18-5 for the printer text and 0-938151-06-1 for the font book) by calling (415) 527-8555.

**A** book for designers on using Verilog hardware description language shows how it works through examples. Verilog's HDL is put to work in designing a pipelined processor, a cache-memory system, a UART chip, and a floppy-disk subsystem. *Digital Design with Verilog HDL*, written by Eli Sternheim, Rajvir Singh, and Yatin Trivedi, not only gives engineers an overview of Verilog but also has a chapter on tips and techniques in Verilog modeling.

Published by Automata Publishing Co., *Digital Design with Verilog HDL* is being used in classrooms at North Carolina State University, Santa Clara University, and at the University of Illinois at Urbana-Champaign. The book includes a disk with 5000 lines of example Verilog models.

The book's list price is \$49.95. However, volume discounts and site licenses are available for companies. To order, contact the company at 10487 Westacres Dr., Cupertino, CA 95014; (408) 255-0705; fax (415) 855-9545. Refer to ISBN 0-9627488-0-3.

# Motorola's In Real



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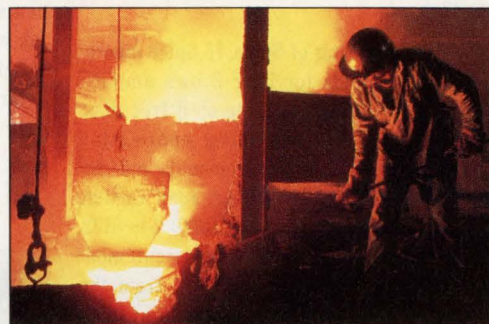
One reason is our long-time experience with real-time technology, beginning with our pioneering work back in 1980. Another is the broad spectrum of our product line, which includes ICs, boards, systems, and software. In short, Motorola has everything you need to build real-time applications ranging from simulation to industrial automation to imaging and more.

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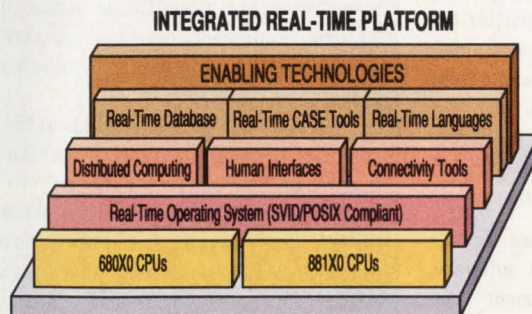
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as for development. Several human interfaces are available for UNIX, including Motif, X.11 and DeltaWINDOWS.<sup>™</sup> As for networking, Motorola supports all popular protocols, including TCP/IP, NFS, SNA, OSI, and X.400. We also offer database and CASE tools, and you can work in C, LISP, FORTRAN, ADA, BASIC, COBOL, and PASCAL. Put it all together, and you will discover only one company gives you the full story on real-time, and that's Motorola.



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# QUICKLOOK

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**A** free disk has Spice models of Analog Devices' amplifier ICs. The 176-model library includes current and voltage-noise models for some devices and models of two instrumentation amplifiers. Contact the company at One Technology Way, Norwood, MA 02062; (617) 329-4700.

**S**peaking of Spice, 75 Spice macro-models for Burr-Brown amplifiers are available on a free disk. An accompanying application bulletin describes the macromodels and circuit models in detail. Contact John Conlon, Applications Engineering at (800) 548-6132. The macromodels and simplified circuit models also may also be downloaded from the company's electronic bulletin board at (602) 741-3978 (300/1200/2400 8,N,1).

**A** free disk demonstrates software that helps root out electromagnetic interference problems in systems. Atkinson Engineering, of Warrenton, Va., has developed a graphical EMI modeling spreadsheet for IBM PCs and compatibles as well as for the Apple Macintosh. With the GEMS package, EMI can be modeled as a set of sources, coupling paths, and fixes that are interconnected and then interrelated like numeric cells on a spreadsheet. Cells can be added, copied, moved, deleted, or changed. The system must have Microsoft Windows 3.0 installed. Contact Kenn Atkinson, (703) 347-5716.

**S**witched capacitor filters are becoming faster, quieter, and lower in distortion. But many system designers still are unfamiliar with their use. Enter Linear Technology's application note, "AN40: Take the Mystery Out of the Switched Capacitor." The 28-page note discusses how to use switched capacitor filters to replace active RC filter types along with power-supply effects, input and output considerations, and filter response.

Contact the company at 1630 McCarthy Blvd., Milpitas, CA 95035-7487; (800) 637-5545 or (408) 432-1900; fax (408) 434-0507.

**A** free disk demonstrates Testniques' Test Executive software, which trims development time for VXI and IEEE-488 ATE systems, benchtop test systems, and customized instrumentation systems, the Minneapolis company says. Versions are available for Microsoft C and LabWindows. Contact the company at (612) 533-4107.

HOT PC PRODUCTS

**W**ould you rather give commands to your PC in English than in DOS? Using artificial intelligence techniques, PC-IQ from A. I. Solutions prompts PC users with "Do you want me to perform a command or run a program?" Users then enter a request such as "make a file" and can add their own commands to the program's vocabulary. PC-IQ, which runs on PCs, XTs, ATs, PS/2s, and compatibles, needs 640k of RAM, DOS 2.0, and a hard disk. The software lists for \$99.95. Contact A. I. Solutions, 58 Creekview Dr., P. O. Box 128, West Seneca, NY 14224; (800) 677-6670 or (716) 675-5311.

**A**imed at keeping engineers abreast of technical information, a database on CD-ROM has information from 3000 engineering journals and conference proceedings. Ei Page One, from Ei/Engineering Information Inc., is updated monthly and is arranged in table of content format. Page One also has 60% more conference coverage than the company's other electronic publication, Compendex Plus, in print as *The Engineering Index*.

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K M E T S K O R N E R

## ...Perspectives on Time-to-Market

**BY RON KMETOVICZ**

President, Time to Market Associates Inc.  
Cupertino, Calif.; (408) 446-4458; fax (408) 253-6085



**T**ask network models are formed by connecting tasks to one another either in series, parallel, or a combination of the two. The most important item to remember about building the network model is to make network connections based only on considering how the tasks relate to one another. Use a series connection only if activity B cannot start until activity A is finished. Use parallel arrangements in all other cases. Question all series connections and look for ways to remove them or decompose them into short work content structures. From a time-to-market perspective, serial relationships slow down the new product development process.

Once you have produced a network with a minimum of serial connections and it's entered into your computer system, you can then, to the best of your team's ability, begin estimating the work content in each activity within the network model. Please avoid confusing work content with task duration. Work content is simply the number of hours, days, or weeks of work that are needed to do the activity. It's expressed as person-hours. Knowing work content makes it possible to compute the time duration required to complete a given activity once a resource is committed to work on the task at a given rate. For example, a task with a 30 person-hour work content that is worked on at 2 hours/day takes 15 work days to complete. Each activity in your database should have a work content number in its associated data field.

Now that data is assembled about the new product development effort, you can determine time to market as a function of the resources applied to realizing the product. To do this, you assign resources to each activity and commit the assigned resource to work on the assigned activity at a given rate. The computer tool then computes the task duration from the information available and begins to provide detailed feedback about the effort's time to market. After committing all your available resources, you'll want to use leveling and constraining algorithms to ensure the resource commitments you have made are within the typical daily limits of your organization.

Most often, a development team that follows these steps finds, after consuming all its assumed-to-be-available resources that it is still short of meeting its time-to-market goals in time. If front-end work has been done correctly, the exercise becomes one of adding resources in critical areas until time to market objectives are realized.

# QUICKLOOK

## TIPS ON INVESTING

**A**s the saying goes, taxes are inevitable. And income taxes play an important role in an engineer's investment decisions, particularly during the transition between working life and retirement. This transition has three phases, each with its own tax-planning issues.

Pre-retirement, your tax-planning strategies do not change much since you are still working and your tax rate probably hasn't changed. You want to maximize after-tax investment returns and begin to reposition your portfolio to reduce risk and generate additional income for your retirement. You should begin to clarify your retirement goals and needs. If your portfolio has a large amount of stock in the company you work for, consider diversifying into more conservative investments. A financial consultant can review your portfolio and suggest appropriate investment allocations to help you meet and maintain your current lifestyle once you retire.

Of uppermost concern during the point of retirement is how and when to take distributions from employer-sponsored retirement plans. If you're receiving a lump-sum distribution, you must decide either to roll the distribution into an IRA or Keogh or take advantage of a favorable tax treatment on an immediate distribution. If you were 50 years old by Jan. 1, 1986, you can use five-or ten-year forward averaging for a lump-sum distribution (with any pre-1974 amounts eligible to be taxed at a flat 20% capital gains rate, if elected). Otherwise you can use five-year averaging only once, after you reach 59 1/2. A lump-sum distribution typically represents the most money you will receive at any one time.

Post retirement involves tax planning in many different areas. Many taxpayers sell their home to move to smaller residences or retirement communities and face a large tax liability on the resulting capital gain. You are permitted a one-time exclusion of up to \$125,000 of profit on your primary residence. To qualify, your home must have been your primary residence for at least three of the last five years and either spouse must have reached age 55.

Once you have retired, some of your Social Security benefits may be taxable. If your adjusted gross income plus tax-free interest plus one-half of your Social Security benefit exceeds a limit (\$25,000 for singles, \$32,000 for couples), up to one-half of the benefits will be added to taxable income. You also face a loss of benefits if you continue to work during retirement. Depending on your age, Social Security recipients lose \$1 for every \$2 or \$3 of earned income above a ceiling amount. However, no benefits are lost if you are at least 70 years old.

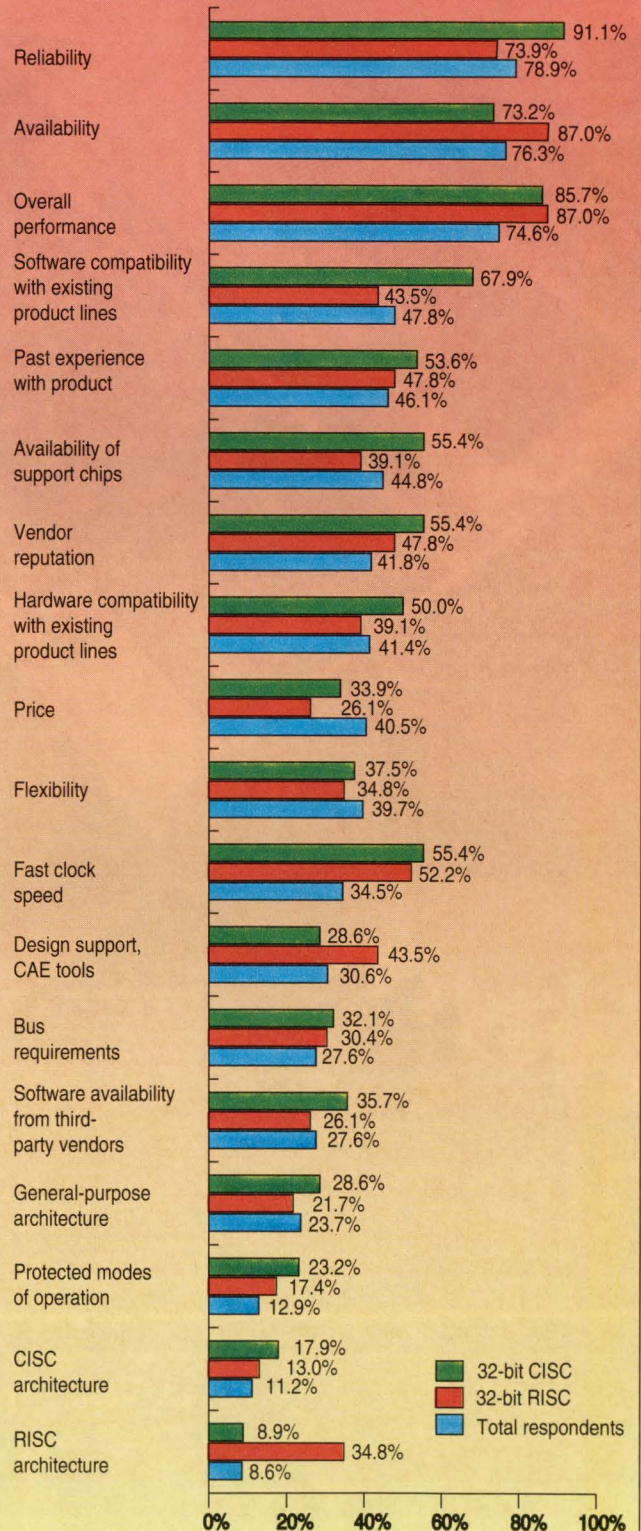
Your retirement years can be the most enjoyable time of your life. You may be "retired" almost as many years as you worked, so a careful analysis of your needs and goals is important. The closer you are to retirement, the more important it is to review your financial portfolio often. For a free copy of *The Changing American Dream: The Real Definition of Retirement*, a Shearson Lehman Brothers publication, call or write me.

Henry Wiesel is a financial consultant with Shearson Lehman Brothers, 1040 Broad St., Shrewsbury, NJ 07702; (800) 631-2221 or (800) 221-0073 in N. J. Wiesel is also a qualified pension coordinator with The Private Client Group. He invites questions and comments.



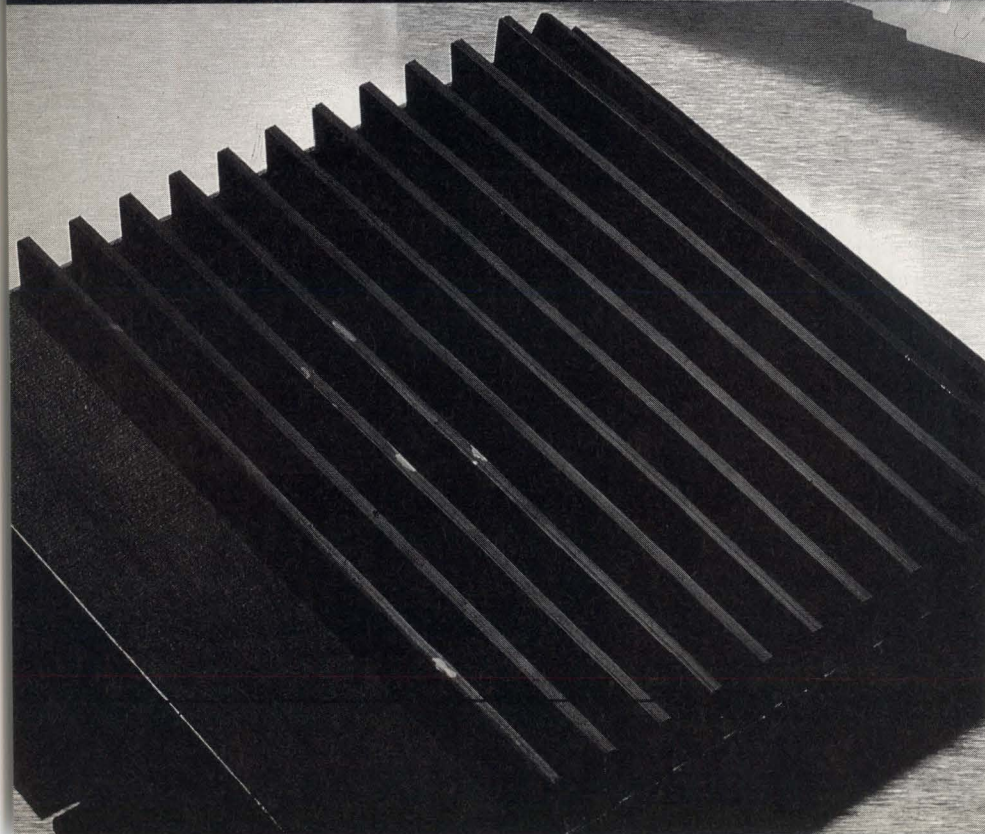
## MICROPROCESSOR SURVEY

### WHAT'S IMPORTANT WHEN YOU SELECT A MICROPROCESSOR FOR A DESIGN?



Source: a survey of Electronic Design readers conducted by the Adams Co., Palo Alto, Calif.

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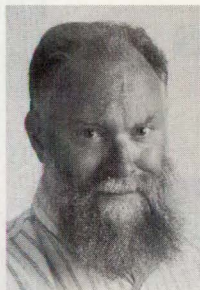
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CIRCLE 116

# WHAT'S ALL THIS MENTORING STUFF, ANYHOW?

Once upon a time, a new engineer came to work in our group. A woman. Now, in some areas, it's really not a surprise to have a new engineer or a woman engineer, but in our group, that did not happen very often. So when Jane arrived, we all tried to be polite and cheerful, for a change, and not just scream at her and give her a hard time, as newcomers are sometimes treated. Now, Jane was a bright young woman, but there were a lot of things that she had to ask questions about, so she would ask various people. Sometimes she would ask me, and sometimes she would ask Andy,



**BOB PEASE**  
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

another of the old-time experienced engineers. We didn't just fall over ourselves to help this bright young engineer. But we did realize that the more questions we answered, and the faster we could bring her up the learning curve, the quicker we could get a lot of help out of her and turn her into a *real engineer*. So we were reasonably cheerful at answering some of her dumb questions (like where do you find things that aren't filed or indexed rationally?), and some of her very thoughtful questions (why do we keep telling customers this or that when it's not true??). And we tried not to just throw answers at her, but to explain the rea-

sons behind the answer.

One day, I wandered over to get some info out of a book, and Jane asked me a question. Andy had the answer quicker than I did, and I was standing around reading the book, while Andy explained the answer to Jane. When he was finished, I said, "Hey, Andy, you know, Jane is your protégée, right?" Andy agreed. I continued, "And Jane is my protégée, too, right?" Andy agreed. I then said, "And, Andy, do you know what that makes us?" Andy could not think of the correct word. I said, "That makes us dirty old men." And all *three* of us broke up into laughter. Around here, no-one and nothing is taken very seriously....

Actually, there *is* a word that applies, so if a person is my protégé (male) or protégée (female), then I am a Mentor. I attended a nifty conference on Bipolar Circuits and Technology in Minneapolis in September. I must say, although it doesn't get *nearly* as much publicity as ISSCC, it's getting to be nearly as good as ISSCC, so long as you are really interested in bipolar circuits (if you're a hard-core MOS enthusiast, there's no reason for you to come to Minneapolis in September). The after-lunch speaker this past year was Jim Williams of Linear Technology Corp., Milpitas, Calif. Jim talked about several topics, but his most serious pitch was that we must do a lot of mentoring. We can't just hire a bunch of kid engineers, ignore them, throw garbage at them, and then chew them out. We probably never *could* do that. But in the 1990s, it's reasonably easy to see that the nurturing of new or young engineers is a major part of our jobs.

When I was a kid engineer at Philbrick, I had a number of excellent teachers, engineers who taught me

many different aspects of the profession. I must say, though, I was a rather *green* engineer, because I never had a hobby of ham radio, as many engineers did. In fact, I only transferred from the Physics department to become an EE in the fall of my senior year.

At Philbrick, Dr. Achard helped me appreciate technical writing. Bruce Seddon taught me a lot about worst-case design. Al Pearlman answered lots of my questions about transistors. Bob Malter did not have much time for dumb questions, but I studied his designs and asked a few questions that were not *too* dumb. I mean, learning how to ask questions that are not *too* dumb is a significant part of every student's education. After studying and learning from a whole bunch of people for over a year, I was just barely able to design my way out of a paper bag with a little help. It took me a few more years before I understood the whole picture, well enough that I could design amplifiers without too many fatal flaws, or latch-up modes, or features that did more harm than good.

So if we also want to hire good engineers to work on linear or analog circuits, we can't just find them in thin air, and we can't just hire them from our competitors. And we *certainly* can't just find them coming out of colleges. I mean, when a student graduates from a good engineering school, the best I can hope for is that the student has learned some good study habits, some good attitudes toward work, and some ability to analyze several kinds of circuits. But not everything. Can I hope that the student really knows how to design an op amp? Well, I hope that an engineer I am interviewing knows a little bit about designing *something*. If he (or she) can design and analyze some things pretty well, there's good hope I can teach them enough to come up the learning curve quickly. That's only fair. If I can make *them* look good, then they can make *me* look good.

So I should try to avoid the "mushroom treatment," not heap manure on them and leave them in the dark. I should teach them sometimes, throw problems at them other times, challenge them, and try to set a good example. I should avoid letting them get

## PEASE PORRIDGE

stuck, or hung up, or discouraged. I may not be able to answer every question. I may demur, or duck certain questions, and tell them to go figure it out for themselves. It's a little bit like when you have kids. You can't teach your own kids everything, but you try to steer them in a course where they can learn what they need.

I remember when our sons were just learning to read. For a while, my wife and I agreed that *each* of us read everything that Benjamin read. After about a month, we agreed, well, one *or* the other would try to read everything Benjamin read because he was just too omnivorous for each of us to fit in the time to read everything. A month after that, we sort of gave up, as we could not possibly keep up with his appetite for reading. We tried to read samples of what he was reading. But, we had gotten him turned on and he was off to the races, devouring every kind of book and magazine that was suitable

for young people, and many grown-ups' topics as well. Now that both my sons are taller than I am, they throw me an occasional bone, some good things for me to read that they can recommend. Turnabout is fair play.

Now, when we assign projects to engineers at work, I can't keep up with all of the details, and I can't know all of the answers. But I have to keep in touch, to tell if there's trouble, to facilitate the search for answers, and to prevent the guy from getting discouraged. This is even necessary for an experienced engineer! Because there really aren't many easy projects that our customers want us to do, every engineer gets some very challenging projects. Challenges are great for young engineers, but mentoring would advise you against loading on an unfairly heavy load. Similarly, I have to keep an eye on the project, to make sure the engineer doesn't make a false assumption and go barreling down a path that

is dead-end. Everybody recognizes that after it has happened, but it's a little harder to see it in advance.

Wow, Pease, it sounds like you really are in charge of a big group. How many people does Mr. Super-manager Pease have working for him? Well, about 2 engineers, 2 technicians, and one guy who is half-way up from technician to engineer. But, I must say, by default, I have given some of my technicians a lot of liberty, and they have responded by coming up with some brilliant moves, interspersed with a few occasional marvelous blunders. So, I have 2 boys at home, and 5 boys at work, and, oh boy, do we have fun.

All for now./Comments invited!/RAP  
Robert A. Pease / Engineer

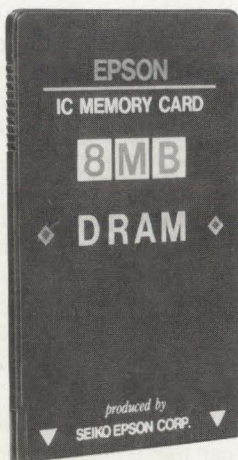
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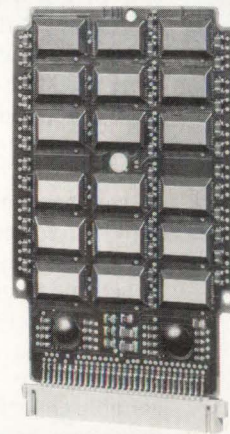
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CIRCLE 122

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Model	Speed (ns)	Packaging	Data Retention Current	Special Features	Availability
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— CXXK581000M	100/120/150	SOP 525mil	L/LL	B/X	Now
— CXXK581100TM	100/120/150	TSOP	L/LL	B/X	Now
— CXXK581100YM	100/120/150	TSOP (reverse)	L/LL	B/X	Now
— CXXK581001P	70/85	DIP 600mil	L/LL		Now
— CXXK581001M	70/85	SOP 525mil	L/LL		Now
— CXXK581020SP	35/45/55	SDIP 400mil			Now
— CXXK581020J	35/45/55	SOJ 400mil			Now
128Kx9 — CXXK77910J	20	SOJ 400mil		Sync ASM	2H '91
256Kx4 — CXXK541000J	25/30/35	SOJ 400mil			2H '91

L = Low LL = Low, Low B = 3 Volt X = Extended Temperature

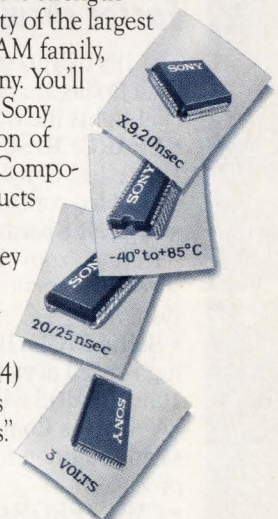
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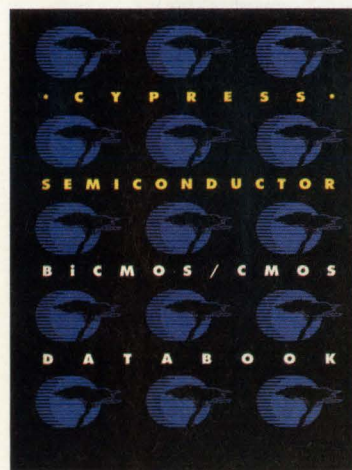
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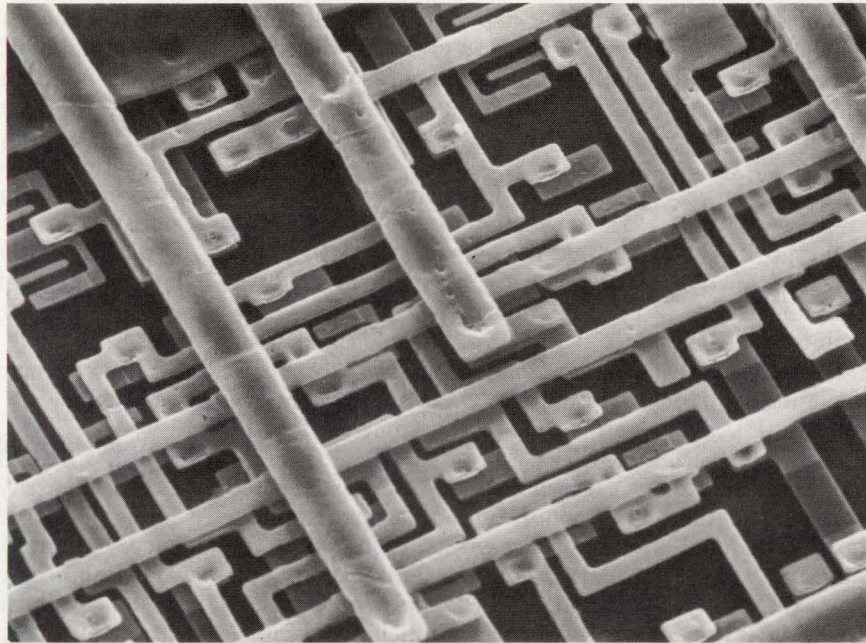


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**THREE LAYERS OF METAL**, as shown in this microphotograph from a scanning-electron microscope, allow up to 70% of the gates to be utilized on one chip. The new channelless sea-of-gates arrays are from Motorola.

# GATE ARRAYS CHALLENGE STANDARD-CELL ASICs

CHANNELLESS SEA-OF-GATES ARRAYS WITH UP TO  
318,000 GATES USE TRIPLE-LAYER METAL FOR POWER  
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**T**raditionally, gate arrays are used as “glue logic” to integrate the miscellaneous logic in systems. However, a new family of submicron CMOS arrays with up to 318,000 gates can be loaded with huge blocks of memory—up to 256 kbits of fully diffused RAM—making them applicable for true system integration. In the past, such applications required standard-cell-based ASICs. The new gate arrays not only significantly extend the size range of gate arrays, but they blur the application lines between gate arrays and standard-cell-based ASICs.

The first sea-of-gates array family to cross the 300k-gate barrier, the H4C Series from Motorola’s ASIC Div., Chandler, Ariz., has an effective channel length of 0.7  $\mu\text{m}$  and a power dissipation of 3  $\mu\text{W}/\text{MHz}/\text{gate}$ . Based on a triple-layer-metal single-polysilicon process, the arrays offer embedded boundary scan logic and 180-ps typical gate delay (see the figure). They operate fast enough to support the

# HIGH-DENSITY GATE ARRAYS

speed requirements of 60-MHz processors. According to the company, customers can achieve a 70% typical gate utilization in most applications.

The arrays incorporate an internal core-cell architecture identical to the company's 105,000-gate HDC Series. As a result, the new gate arrays can utilize any of the cells in the HDC library. CAD support is an extension of that used for the HDC Series.

The series will be introduced in two phases. The first phase, available now, will offer densities of up to 195,000 available gates and I/O signal density up to 256 pins. In the second phase, scheduled for the late third quarter of this year, densities of up to 318,000 gates will be available, and I/O signal density will exceed 500 pins.

Also beginning in the late third quarter, users will be able to embed blocks of fully diffused RAM and implement CAD-controlled boundary-scan configurations. The library will be expanded to include phase-locked-loop (PLL) clock-skew control macros. In addition, the CAE software will be extended to support the company's Customer Defined Array (CDA) architecture, a fully configurable RAM-cell generator, embedded boundary scan in I/O cells, and power calculation.

## ARRAY ARCHITECTURE

The H4C Series can be implemented in either a conventional gate array or a CDA—an architectural hybrid that includes features of gate arrays and standard cells. As in standard-cell implementations, embedded blocks or megafunctions are used in a CDA to provide performance unattainable in a conventional gate array. However, the CDA takes advantage of the low cost of manufacturing a gate array by using a fixed I/O and die size.

Market demand for gate arrays with considerably higher numbers of gates led Motorola to develop the new series. The company worked with several "technology partners," such as Apple Computer, Hewlett Packard/Apollo, and NeXT Computer, to define the features designed into the new series. By universally

shrinking array features, the number of gates in a given size die essentially doubled, compared to the HDC series. And by using reduced gate-oxide thickness, performance improved 30%.

Because the array features of the HDC Series were universally shrunk, the new H4C Series can utilize any of the over 270 internal macrocells (over 150 different functions) and over 400 periphery cell combinations in the HDC library. In addition, the CAD support for the new series is the same as for the HDC Series.

Design development is supported on Apollo/Mentor Graphics and Sun engineering workstations using Motorola's Open Architecture CAD System (OACS). The OACS framework supports multichip and multi-level simulation, logic synthesis, static-timing analysis, triple-layer metal routing, and automatic test-pattern generation.

While the HDC cells include a number of moderate-size preconfigured metallized static-RAM cells, the H4C Series adds the capability of integrating large, high-speed, high-density RAMs within the gate array. These fully embedded synchronous single or dual-port static memories can be as large as 256,000 bits. A custom SRAM compiler can generate over 200,000 different physical single- and dual-port SRAM configurations in sizes up to 256,000 bits. Each RAM can be customized to the exact desired configuration.

The SRAM compiler is fully integrated into the ASIC design system. SRAMs can be generated, characterized, and modeled without engineering intervention, and are ready for immediate use in schematic capture and gate-level simulation on a user's workstation. The characterization methodology offers users different levels of simulation, depending on desired accuracy versus CPU time trade-offs. Compiled memories are placed automatically within the gate-array structure. Other megafunctions now under development by the company include a CPU and many commonly used arithmetic and peripheral functions.

ASICs communicate frequently with a number of other chips, including other ASICs, microprocessors, and RAMs. Optimizing such system performance requires that the communication between chips using synchronous interfaces be maximized. Control and distribution of clock skew both on the chip and between chips in the system is critical. The new gate arrays offer balanced clock trees for on-chip clock-skew control, and PLLs to manage clock skew between chips.

## CLOCK-TREE SYNTHESIS

The gate arrays support Gate-Ensemble clock-tree synthesis from Cadence Design Systems, San Jose, Calif. Balanced clock-tree networks can be synthesized during layout with little effect on design routability. The clock trees have minimal interference with critical data paths and make it possible to use embedded megafunctions, such as SRAMs. These clock trees minimize both clock skew across the chip and clock insertion delay.

Several proprietary macrocells supply PLLs to control clock skew between chips. The PLLs compensate for insertion delays and process variation by synchronizing internal storage elements with the external system clock.

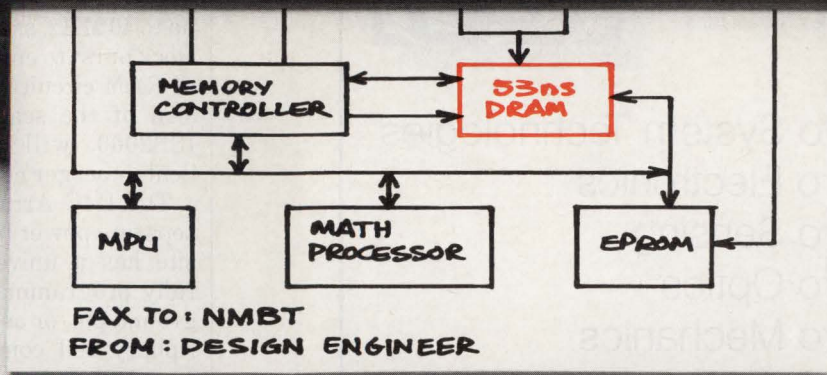
The company has developed a fully integrated test strategy for the H4C Series, which it says will be implemented across all future ASIC technologies. The H4C library provides all D and JK flip-flop macros in scan versions, as well as special level-sensitive scan-design (LSSD) macros. A scan macro, which has been licensed from Storage Technology, Denver, Colo., eliminates the additional propagation delay usually associated with scan circuitry.

JTAG (1149.1) boundary-scan macrocells include specially designed I/O and internal macrocells. The JTAG I/O macrocells reduce silicon overhead by placing all sequential logic in the periphery region of the array. The internal macrocells supply registers and control to the test-access port (TAP).

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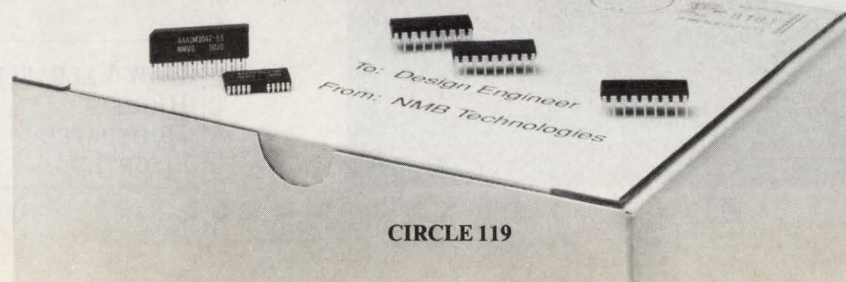
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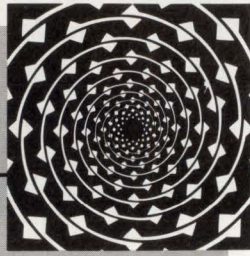
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CIRCLE 119

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## HIGH-DENSITY GATE ARRAYS

based tester for ASICs, is being developed jointly by Motorola and the ATE Div. of Schlumberger Technologies, San Jose, Calif. It features up to 1024 signal pins with 64 scan channels. The tester supports scan rates up to 40 MHz, as well as a high-speed clock burst to enable built-in self test of RAM circuits. A commercial version of the scan-based tester, the ISS2000, will be announced by Schlumberger next month.

The H4C Arrays each have four separate power buses. Each I/O cell site has a universal buffer that's fully programmable as a power or ground pin, or as one of over 400 periphery cell combinations. The arrays have a set of fixed power and ground pads. All non-JTAG I/O cells are programmable for drive currents of 2, 4, or 8 mA. Up to six cells can be paralleled internally to deliver up to 48 mA of output current through one pin.

Available packaging includes JEDEC and EIAJ quad flat packages (QFPs) and tape-automated bonding (TAB) packages, as well as JEDEC pin-grid arrays (PGAs). Pin counts range from 128 to over 500. □

### PRICE AND AVAILABILITY

Three arrays—the H4C057 with 57,000 raw gates, the H4C123 with 123,000 gates, and the H4C195 with 195,000 gates—are available now. Five other arrays planned for the late third quarter include the 27,000-gate H4C027, the 35,000-gate H4C035, the 86,000-gate H4C086, the 161,000-gate H4C161, and the 318,000-gate H4C318. Nonrecurring engineering cost ranges from \$35,000 to over \$200,000, varying with gate equivalency. Arrays using diffused and embedded functions will also entail an engineering charge based on design-support requirements.

As a typical production pricing example, an H4C057 array (up to 40,000 usable gates) in a 160-lead QFP will cost approximately \$27 each, in 10,000-unit quantities per year. Prototype cycle time is 4 weeks for standard arrays (without fully diffused embedded functions) and 6 to 8 weeks for CDAs (with full-diffusion options).

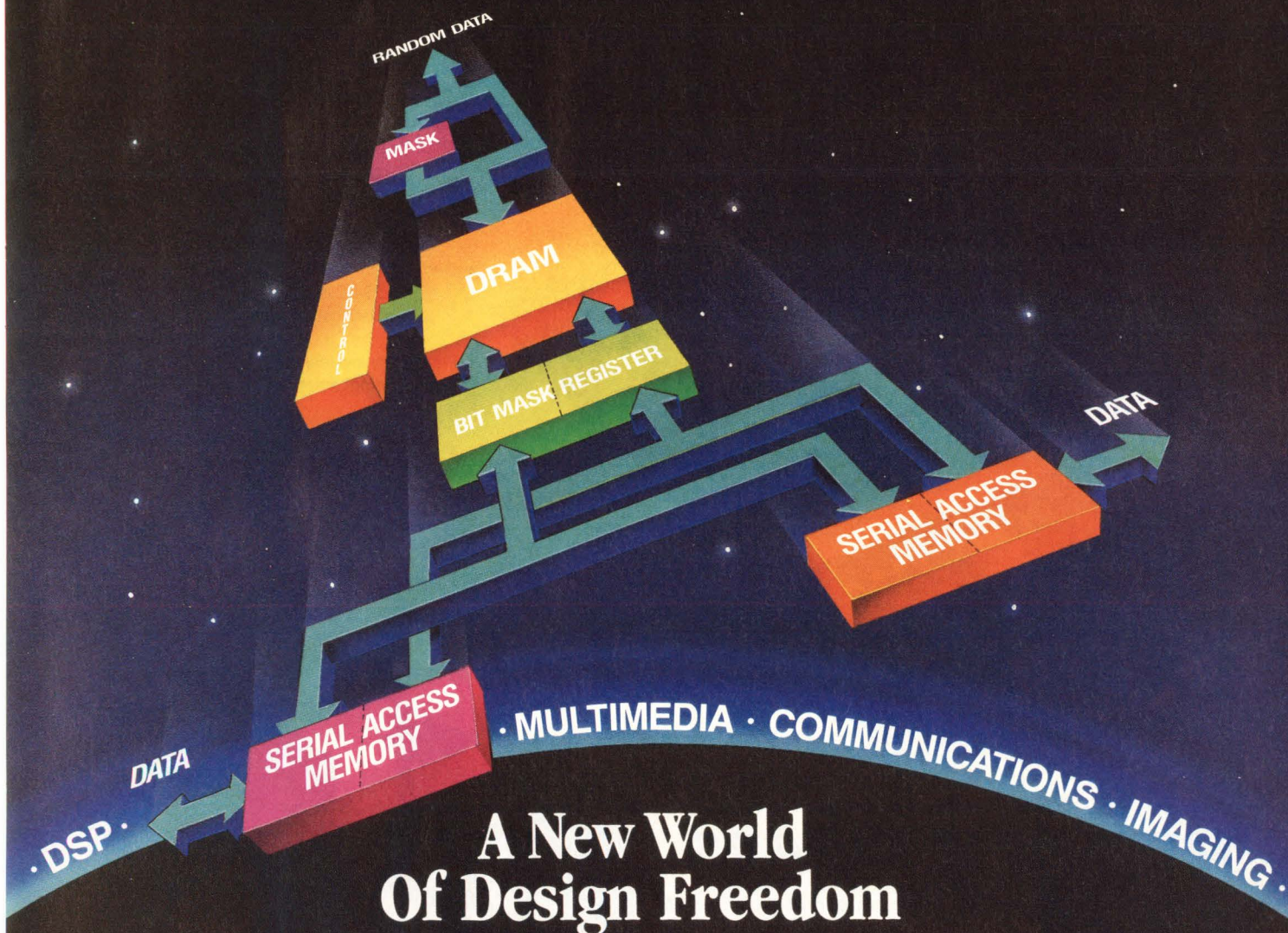
Motorola Inc., Semiconductor Products Sector, ASIC Div., 1300 North Alma School Rd., Chandler, AZ 85224; (602) 821-4406.

CIRCLE 514

### HOW VALUABLE?

HOW VALUABLE?	CIRCLE
HIGHLY	544
MODERATELY	545
SLIGHTLY	546

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MT43C4258*	256K × 4 DRAM	80,100,120	40-Pin SOJ	Samp: Now Prod: Mar 91
	512 × 4 SAMs	25,30,35		
MT43C8128	128K × 8 DRAM	80,100,120	52-Pin PLCC	Samp: Now Prod: 2Q91
	256 × 8 SAMs	25,30,35		
MT43C8129*	128K × 8 DRAM	80,100,120	52-Pin PLCC	Samp: Now Prod: 2Q91
	256 × 8 SAMs	25,30,35		

\*Provides SAM stop address input \*\*Call for military availability

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CIRCLE 125

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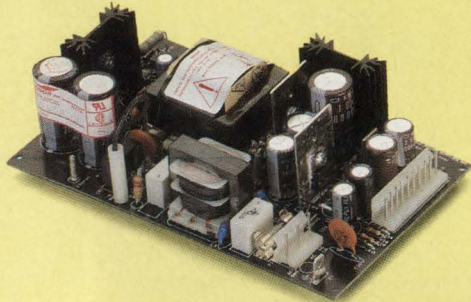
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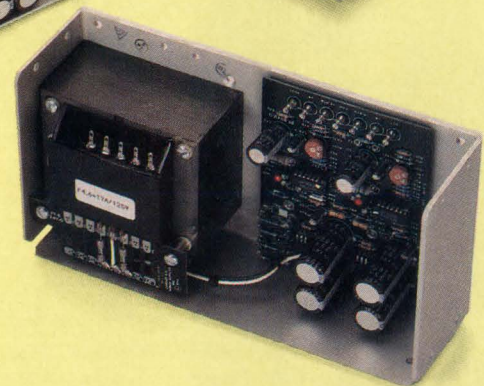
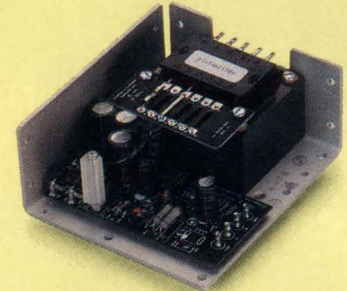
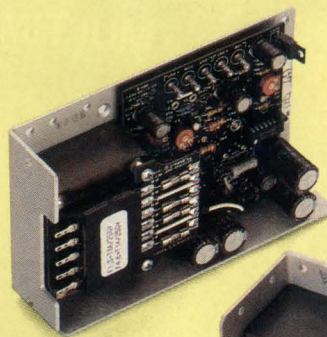


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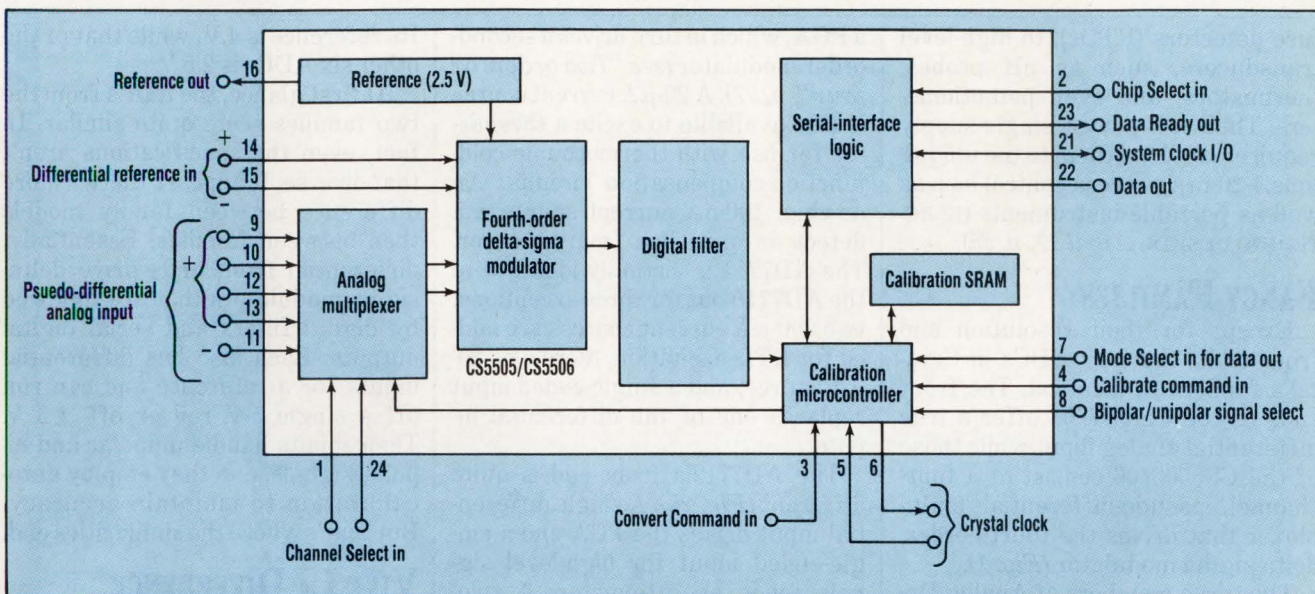
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CIRCLE 113



**1. SPORTING AN INPUT MULTIPLEXER** and a convert command input, Crystal's 16-bit CS5505 and 20-bit CS5506 delta-sigma ADCs look and act like conventional sampling analog-to-digital converters.

# 20-BIT DELTA-SIGMA ADCS VIE FOR INTEGRATOR JOBS

FRANK GOODENOUGH

**T**he first delta-sigma analog-to-digital converters (ADCs) aimed at dc instrumentation jobs—Crystal Semiconductor's 16-bit CS5501 and 20-bit CS5503 with 10-Hz bandwidths—were a nice fit for converter-per-channel applications. However, the 130-ms delay through their digital filters made their use at the output of an analog multiplexer impractical. In addition, they needed a reference, four power supplies, and dissipated 40 mW, which didn't lend them to for battery-powered or control-loop applications.

Now Crystal Semiconductor and Analog Devices, a newcomer to the delta-sigma arena, have each come up with a family of delta-sigma converters for classic dc-measurement applications that can handle multiplexed inputs. With a convert command, Crystal's 16-bit CS5505/07 and 20-bit CS5506/08 delta sigmas even look like conventional ADCs. On the other hand, Analog Devices converters, the 20-bit AD7710/11/12, have added signal conditioning in the form of a programmable-gain amplifier and current sources for sensor excitation. Both easily provide sampled-data rates of 20 Hz.

These converters offer performance undreamed of a few years ago at any price, challenging IC integrating converters, as well as modules, boards, and even instruments. Yet they cost from just \$9 to \$23 each in 1000-unit lots.

Application areas for the converters range from process control to laboratory and medical instrumentation to automatic test equipment and weigh scales (from supermarket-deli scales to roadside truck scales). They link easily with low-level sensors from thermocouples, strain gages, and resistance-tempera-

# 16/20-BIT DELTA-SIGMA ADCs FOR DC INSTRUMENTATION

ture detectors (RTDs), to high-level transducers, such as pH probes, thermistors, and even potentiometers. Their low-power, single-supply requirement lend them to the ubiquitous 4-20-mA process-control loop as well as portable instruments (ELECTRONIC DESIGN, April 11, p. 65).

## FANCY FAMILIES

Except for their resolution and front ends, the four ADCs in Crystal's family are identical. The front ends of the CS5507/08 offer a true differential analog input while those of the CS5505/06 consist of a four-channel, pseudo-differential multiplexer that drives the fourth-order, delta-sigma modulator (Fig. 1).

The three members of Analog Devices' family are also basically differentiated by their front ends (Fig. 2a). The AD7710's front end consists of a two-channel, true-differential multiplexer. The multiplexer drives

a PGA, which in turn drives a second-order modulator (see "Two orders or four", p. 97). A 20- $\mu$ A current source is also available to excite a thermistor for use with thermocouple cold-junction-compensation circuits. An on-chip, 100-nA current source can detect an open line from a sensor. The AD7711 is virtually identical to the AD7710 but for three exceptions: two 200- $\mu$ A current sources are added for RTD excitation, there's no 20- $\mu$ A source, and a single-ended input replaces one of the differential inputs.

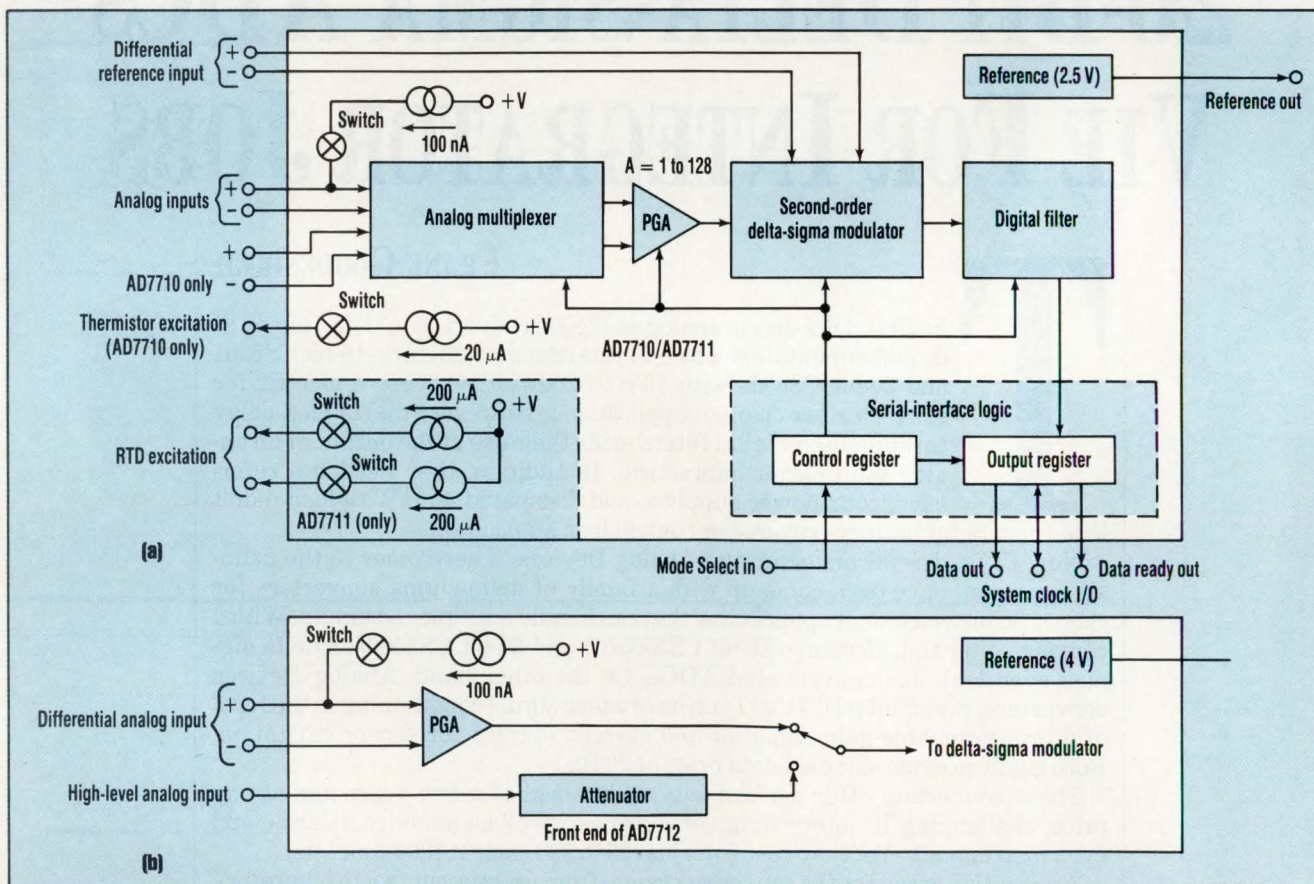
The AD7712's front end is quite different (Fig. 2b). A single differential input drives the PGA and a single-ended input for high-level signals feeds an attenuator. A two-channel, single-ended multiplexer selects the output of the PGA, or the attenuator, for the delta-sigma modulator. The AD7712 has only the open-line-detecting current source.

Its reference is 4 V, while that of the other six ADCs is 2.5 V.

At first glance, the ADCs from the two families seem quite similar. In fact, even the specifications aren't that diverse. It appears there's more difference between family models than between families. Essentially, differential front ends drive delta-sigma modulators that are followed by digital filters and serial digital outputs. Each also has differential inputs for a reference and can run off a single 5-V rail or off  $\pm 5$  V. Their inputs handle unipolar and bipolar signals, and they employ auto-calibration to maintain accuracy. But that's where the similarities end.

## VIVE LA DIFFERENCE

Crystal's CS5505/6/7/8 ADCs, as noted earlier, are designed to "look like" conventional converters. Unlike any other delta-sigma ADC, a convert command (bringing pin 3



**2. INPUT MULTIPLEXERS** on Analog Devices' AD7710/AD7711 ADCs enable them to act as conventional sampling ADCs. The converters also have current sources for exciting sensors (a). Their cohort, the AD7712, lacks the multiplexer and current source. It does, however, offer a high-level input followed by an attenuator and switches to a 4-V reference (b).



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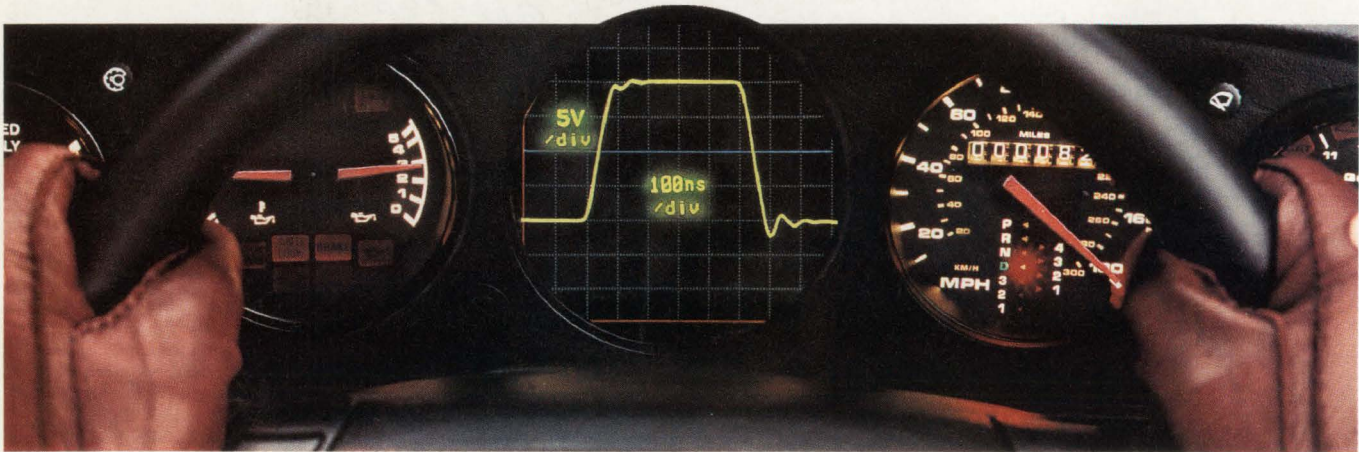
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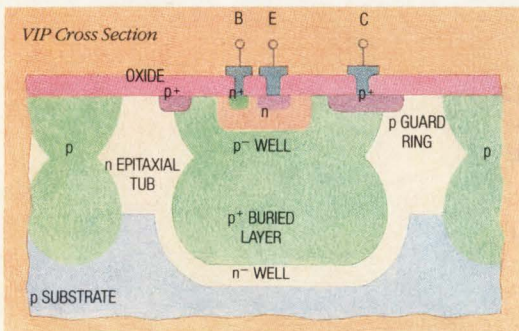


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# 16/20-BIT DELTA-SIGMA ADCs FOR DC INSTRUMENTATION

high) starts a conversion. Again, as with most common converters, a data-ready output (pin 23 goes low) indicates conversion is complete and is ready at the serial-output port (pin 22). If the convert pin is high at the end of the conversion, the ADC starts a new conversion. In the CS5505/06, the convert command also latches the 2-bit address of the four-channel input multiplexer.

The chips are designed to operate with a low-cost (19 cents each in volume quantities) 32.768-kHz watch-crystal clock. With it, the converters spit out new 16- or 20-bit digital words every 50 ms, or 20 sampled conversions/s. Unlike earlier delta sigmas, the digital filters in the new converters settle to within 1/2 least-significant bit in 50 ms. A fast-settling filter is obtained by switching from the low-pass circuit in earlier instrumentation delta sigmas to a comb topology in which only one convolution (instead of several) is occurring at one time. Running at 32.768 kHz, the filter produces zeros, and thus deep, normal-mode, power-line-noise-rejecting notches (typically -120 dB) at 50, 60, 100 and 120 Hz. Minimum attenuation at these frequencies runs -48, -53, -62 and -69 dB, respectively.

## RETURN TO REALITY

The interrelationships among analog input-voltage, reference-voltage, and power-supply-voltage ranges add to the versatility of each of these converters. Like an op amp, there's no analog ground within the chip. All signal and reference inputs are floated. The digital supply is +5 V, the positive analog supply can lie between +5 and +10 V, and the negative analog supply can lie between 0 and -5 V. The absolute difference between the plus and minus analog supply rails must not exceed 12 V. Both the input voltage and reference can lie anywhere between the two analog rails. Crystal, however, recommends a reference voltage between 1 and 3 V. In addition, the maximum span of the input voltage should be within the maximum span of the reference.

The on-chip reference is 2.5 V with

## TWO ORDERS OR FOUR

Crystal uses a fourth-order delta-sigma modulator in its converters, while Analog Devices uses a second-order modulator. Crystal's approach was dictated by its need to achieve 20-bit performance. Analog Devices, on the other hand, felt it could meet the performance with a less complex design (and hence lower-cost unit), using a second-order approach. The key to reaching 20-bit performance with a second-order modulator is a 10-MHz clock, which represents a high oversampling ratio, compared with Crystal's low-cost 32.768-kHz low-frequency clock. A second-order design is simpler, uses less silicon, and potentially cuts IC design time.

a 5-V supply that's referenced to the plus rail. Consequently, the reference-out point (pin 16) sits at +7.5 V if the plus rail is at +10 V. The reference's typical accuracy to within 4% and drift of 60 ppm/°C are both sufficient for ratiometric applications in which sensor excitation is a reference-voltage function. For non-ratiometric jobs, a precision off-chip reference should be used.

Though the Crystal and Analog Devices converters are specified as 16- and 20-bit devices, the prime applications for these ADCs don't demand 20-bit accuracy, and most not even 16-bit accuracy. Nevertheless, because all delta-sigma converters are inherently monotonic, their prime specifications are differential nonlinearity. These are specified as "no-missing codes" (NMCs) to some number of bits. Integral linearity, and gain and offset errors are similarly specified—after calibration.

The 16-bit Crystal units guarantee NMCs to 16 bits; their 20-bit converters to 18 bits. Some codes may be missed at 20 bits due to truncation errors in the output word's digital computation, rather than as a result of analog circuits. Only a few codes are missed at 19 bits, the typical NMC specification.

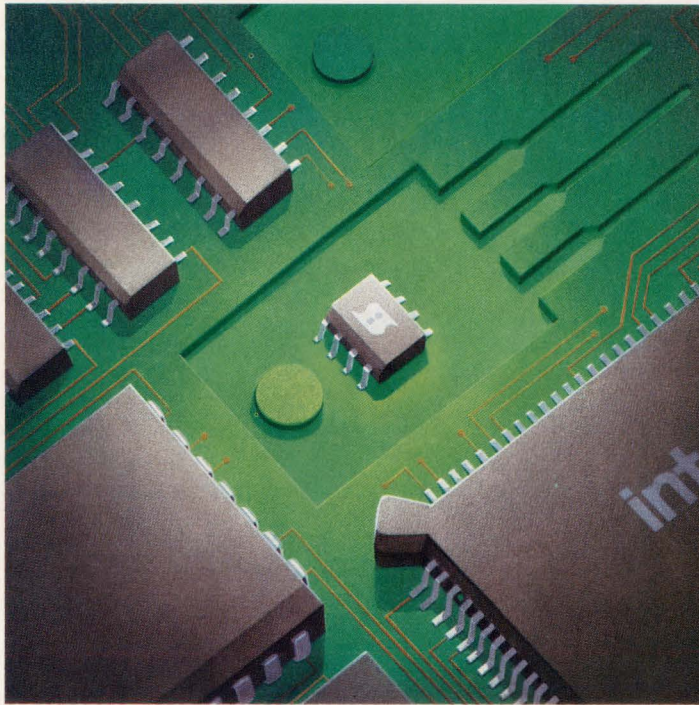
Integral linearity of the top-grade Crystal units is guaranteed to be within 0.0015% (16 bits). Full-scale and offset error after calibration, at any temperature, runs a maximum of  $\pm 24$  and  $\pm 64$  LSBs, respectively, for the 20-bit converters;  $\pm 1.5$  and  $\pm 4$  LSBs, respectively, for the 16-bit devices. The chips take just 4.5 mW of power operating from a 9-V battery, and a mere 25  $\mu$ W when asleep. They should find many homes in handheld instruments of all types, as well as in 4-20-mA current loops.

## ANOTHER DRUMMER

Beyond the front end, the architecture of Analog Devices' converters bears little resemblance to Crystal's (Fig. 2, again). Two major differences stand out: The Analog Devices units include a PGA and a bidirectional serial I/O for host control of chip operation, and for shipping data words to the host. A 24-bit control word performs several tasks. They include selecting the input channel; activating the current sources; setting signal bandwidth, word rate, and PGA gain; activating calibration; and selecting the operating mode. Other tasks involve calling for data and calibration coefficients to be sent to the host, activating the sleep mode, and selecting between bipolar and unipolar input signals. Like Crystal's ADCs, these have a data-ready output that goes low when a new data word is ready for the host and after completing a calibration step.

The master clock should run at 10 MHz and can be implemented with a crystal between two pins. As programmed by the host, the performances of the PGA and digital filter are interrelated, with both elements determining effective resolution. The PGA can be given any one of eight gains in binary increments from 1 to 128. The data rate, and the first notch of the filter, can be set at 10, 25, 30, 50, 60, 100, 250, 500 and 1000 Hz. The -3-dB frequency can range from 2.62 to 262 Hz. For a 10-Hz data rate, resolution is 21.5 bits at a gain of one, and 16.5 bits at a gain of 128. At the maximum data rate of 1000 Hz, resolution is 8.5 bits regard-

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The Analog Devices converters guarantee no-missing-code performance to 21 bits with no truncation errors. Like Crystal's units, integral nonlinearity is within 0.0015%; the filter notch is at 60 Hz. After calibration, maximum gain error runs within  $\pm 0.5$  LSB, and maximum offset error is 10  $\mu$ V.

The converters' 2.5-V reference is with respect to ground. Its accuracy is within 1% maximum and drift rate is 25 ppm/ $^{\circ}$ C typical. Power drain, however, is significantly higher than the Crystal units—45 mW maximum in the operating mode and 100  $\mu$ W while asleep. But the values and relationships between supply-rail, signal, and reference-input voltages of the two families are virtually identical. The Analog Devices' units need a 5-V digital rail while the analog rails can run from  $\pm 5$  V to 0 and 5 V, and to 0 and 10 V.  $\square$

### PRICE AND AVAILABILITY

The 16-bit Crystal CS5505 and 20-bit CS5506, with their four-channel multiplexer front ends, come in 24-pin plastic DIPs. The single-channel 16-bit CS5507 and 20-bit CS5508 come in 20-pin plastic DIPs. Both are rated for the extended-industrial-temperature range. In quantities of 1000, pricing ranges from \$9.30 to \$22.70 each. Military grades are also available. Small quantities are available from the factory.

Analog Devices' AD7710, AD7711, and AD7712 come in 24-pin plastic packages and are rated for the extended-industrial-temperature range. In quantities of 1000, they go for \$12.75, \$13.60, and \$11.90 each, respectively. Military grades are also available. Small quantities can be had from the factory.

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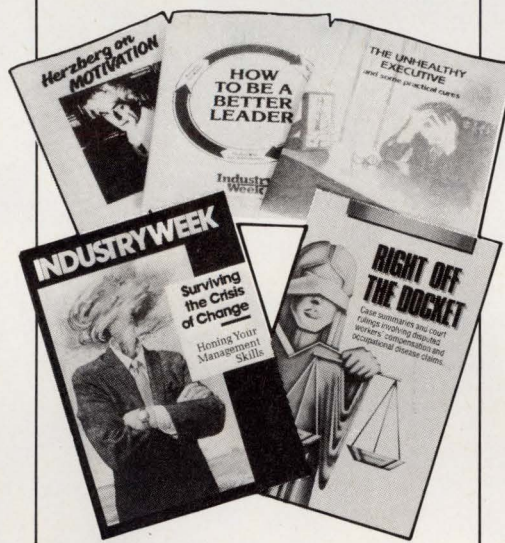
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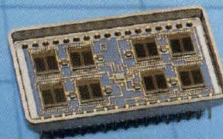
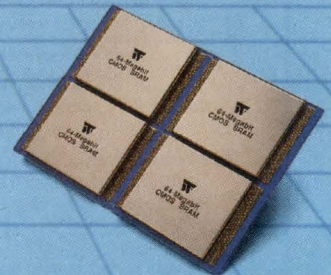
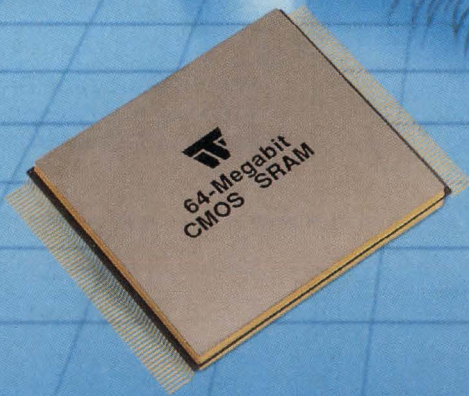
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## The Packaging Hurdle

*Not all exotic alloys and composites go into stealth fighters or race cars. Advances in electronic gear will increasingly depend on innovative material technology.*

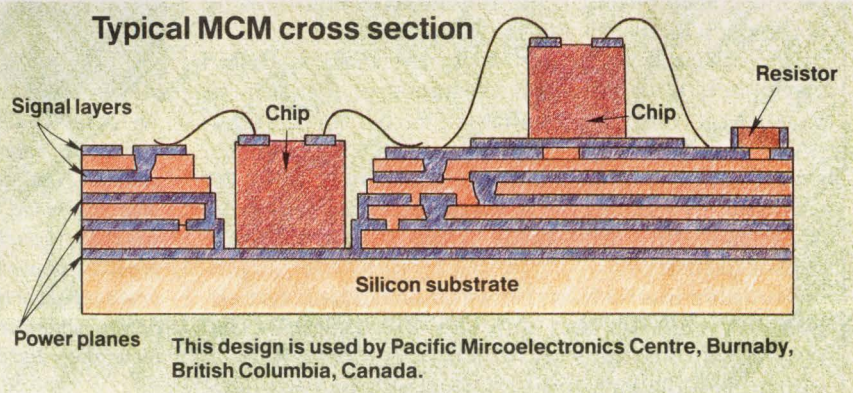
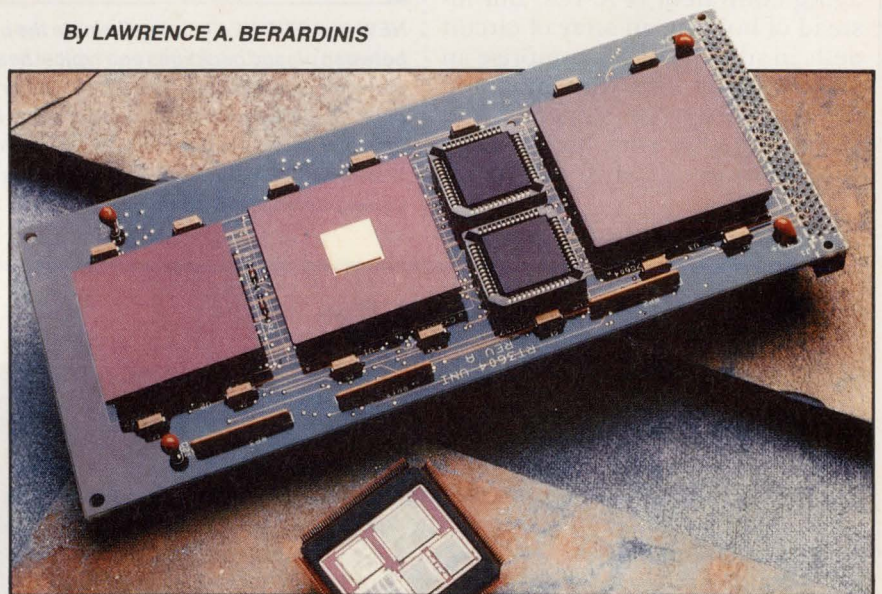
By LAWRENCE A. BERARDINIS

**P**ACKAGING ONCE was little more than an afterthought in the design of many electronic products. But no more. Today, the packages that house IC chips and modules are becoming as sophisticated as the microcircuits they contain.

The reasons are easy to understand. Thermal management problems become huge as microprocessors approach the 100-MHz region and memory chips hit 64M bits. As the number of on-chip I/Os reach the hundreds, designers must resort to complicated schemes just to make connections between closely packed circuits.

The response to these problems has been a dramatic push in materials and packaging technologies. Massive research efforts are underway in Fortune 500 companies, firms that include AT&T Co., Boeing Co., Digital Equipment Corp., General Electric Co., Hewlett-Packard Co., Hughes Aircraft Co., IBM Corp., Intel Corp., Motorola Inc., Rockwell International Corp., and Texas Instruments Inc., as well as at other companies and in Japan.

The research consortium MCC (Microelectronics & Computer Technology Corp.) is also involved,



**HIGH-DENSITY** interconnect boards based on multichip modules (MCMs) are today's most sophisticated electronic packaging technique. Within a few years, the technology will migrate into everything from PCs to automobiles. The idea behind MCMs is to mount multiple chips on a common substrate to save space and reduce interconnect length. MCMs built on silicon substrates, such as those made by nChip, San Jose, Calif., are in many ways more advanced than the chips they connect.

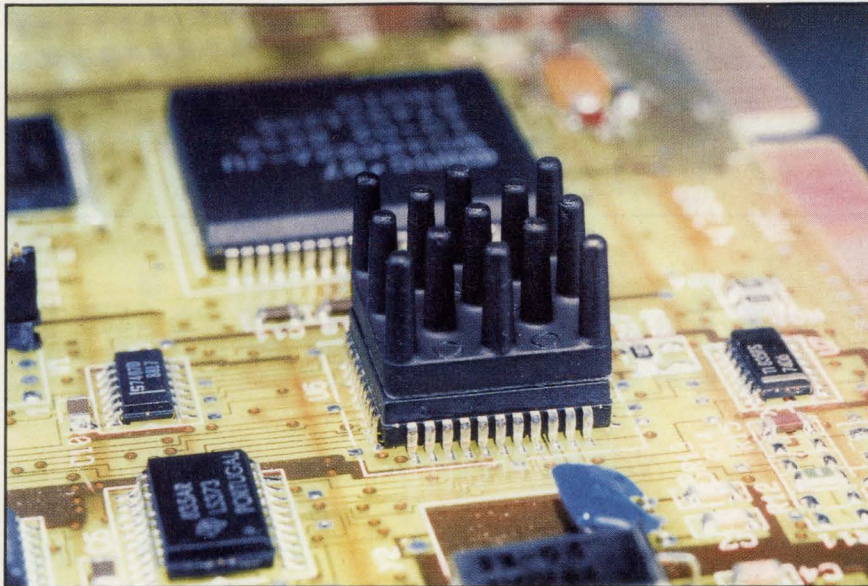
# ELECTRONICS

## PACKAGING AND MATERIALS

developing CAD tools to support the design of advanced chip and hybrid packages. Moreover, the technology is important enough to attract funding from DARPA (Defense Advanced Research Projects Agency), which is starting to work on a high-density circuit packaging initiative. Commercial vendors are working in this area as well.

### ALMOST-INTEGRATED CIRCUITS

The packaging technique which is attracting the most attention in electronics today is multichip module. Multichip modules (MCMs) are said to be the packaging equivalent of ASICs. But instead of holding an array of circuit cells in silicon, MCMs comprise an assortment of bare dice mounted on an appropriate substrate and strung together with high-density interconnect. Using thin-film



**NEW PLASTIC HEAT** sinks eliminate the problem of thermal-expansion mismatch between plastic packages and typical heat sinks made of aluminum. The metal-filled polymer, called Deltem, has a CTE similar to that of materials commonly used to enclose PLCCs and PQFPs, yet conducts heat more readily. It also weighs 40% less than aluminum, placing less stress on solder joints. Deltem heat sinks from EG&G Wakefield Engineering are available in sizes from 0.650 to 0.950 in. per side, corresponding to IC packages from 44 to 168 pins.

## An Interdisciplinary Art

LOOK AT A team designing advanced packaging today and you're likely to find physicists, polymer chemists and material specialists, as well as crack mechanical and electronic engineers. The reason is that packaging poses tough mechanical and materials problems that can frustrate the most carefully planned circuit designs.

To understand why, consider what can happen on an integrated circuit if the mechanical engineering of the package is less than first rate. Stresses induced by factors such as bond wires or thermal expansion can change the inherent resistance of the silicon, causing circuit behavior that is nearly impossible to predict. (In fact, some industry veterans claim that poor chip packaging led to the accidental discovery that silicon can act as a variable-resistance transducer, and thus gave birth to the silicon pressure sensor industry.)

Complex interactions between packaging and circuit elements demand innumerable trade-offs that cross the boundaries of ordinary engineering disciplines. Mechanical and electrical simulations must treat each material or structure in an electronic package as a dynamic subsystem in its own right which must be described in terms of coefficient of thermal expansion, Young's modulus, dielectric constant, thermal conductivity, impedance, signal frequency,



**AN EXAMPLE OF** how packaging teams have become interdisciplinary: One effort to win a multimillion-dollar DARPA contract in MCMs will be led by these professionals at Texas Instruments Inc. From left to right, physicist Howard Test, a specialist in package design for power-specific applications; physicist Dr. Walter Schroen, in charge of packaging and interconnect of high lead-count ICs and ultradense boards; and polymer chemist Gail Heinen, specializing in a die-attach technology and computer simulation.

and other parameters. Rigorous testing must also gauge effects that are hard to simulate by computer. Typical tests check factors such as corrosion between two materials; ingress of moisture through seals, and fracture mechanics.

technology, these modules are smaller and support higher signal speeds than printed-circuit boards and even hybrid assemblies.

Potential applications for MCMs include CPUs, memories, graphics subsystems, networking nodes, and embedded controllers. In general, any large circuit running faster than 40 MHz or which must occupy limited space is a strong candidate for multichip design.

MCMs support high speeds with interconnect lengths that are 10 to 100 times shorter than on standard circuit boards. Die spacing can be as low as 10 to 20 mils. Also, MCMs eliminate an entire level of packaging and the corresponding propagation delays. In a 40-MHz system, for example, chip-to-chip transmission times can be cut by 4 to 6 ns, a savings of about 20% with respect to the 25-ns clock cycle.

Although multichip technology solves two major problems for system designers, it creates several new ones for packaging engineers. The challenge is to cool a dozen or more chips operating at 50 to 100 MHz inside a small package. A Risc-based computer, for example, consisting of several VLSI chips, can dissipate up to 70 W. Air-cooled modules can handle about 15 W, but manufacturers claim that exotic heat sinks will allow MCMs to take on circuits that generate from 50 to 75 W.

The trick to designing multichip modules — which also applies in hybrids and printed-circuit boards — is finding and assembling materials with the right blend of electrical, mechanical, and thermal properties. Trade-offs are almost always required and depend on the application. Although each MCM manufacturer seems to have a different recipe, the construction of these packages can be broken into three basic elements: substrate, dielectric, and interconnect method.

**Substrate:** One approach to multichip modules is to use familiar circuit-board technology such as FR-4. Chips are typically wire bonded and covered with an

opaque epoxy. These assemblies are called chip-on-board and can be enclosed to customer specifications. Although the packaging method costs relatively little, it is generally limited to applications where speed and size are not at a premium.

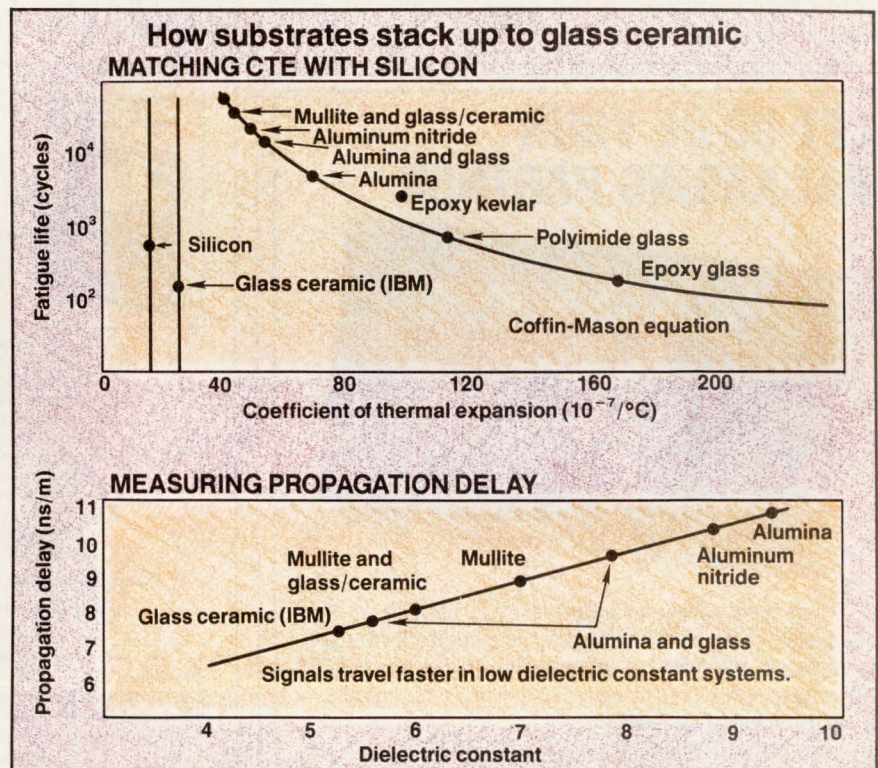
Ceramics are also commonly used to make MCMs. Alumina substrates, for example, date back more than 20 years in thick-film hybrids and power modules. Compared to conventional organic laminates, they are more thermally conductive, provide increased mechanical support, and allow line width and separation to be reduced by one to two orders of magnitude.

Alumina falls short, however, because it has a high dielectric constant and does not expand at the same rate as silicon over temperature variations. With twice the dielectric constant of FR-4, it tends to limit signal speed and offset the

gains of shorter connections. Parasitic capacitance inherent to substrate/conductor interface is to blame. But help is available from glass ceramics that have dielectric properties similar to those of standard circuit boards.

One of the biggest advantages of cofired glass-ceramic, a substrate that IBM engineers are having success with, is that its coefficient of thermal expansion (CTE) closely matches that of silicon. Glass ceramic has a CTE of  $30 \times 10^{-7}/^{\circ}\text{C}$ , compared to  $26 \times 10^{-7}/^{\circ}\text{C}$  for silicon and about  $60 \times 10^{-7}/^{\circ}\text{C}$  for alumina. This translates into a better fatigue life for solder connections because it equalizes thermal expansion and contraction cycles between the chip and substrate.

Other new ceramics, including aluminum nitride and silicon carbide, trade off dielectric properties for higher thermal conductivity. Thermal conductivity is also



**GLASS CERAMIC** has thermal-expansion properties closer to those of silicon than many other substrate materials. The closer the match, the less stress placed on solder bonds, and the higher the fatigue life of the joint. Glass ceramic also offers one of the lowest dielectric constants, which translates into shorter propagation delays for signals.

# ELECTRONICS

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a major selling point for metal substrates such as molybdenum-copper. Unlike low-dielectric-constant ceramics, these materials allow heat to dissipate from the substrate rather than the surface of the chip itself.

An edge that silicon carbide has over other new ceramics is that its thermal-expansion properties are similar to those of a silicon die. Mixed with aluminum in a reinforced matrix, composites of silicon carbide are also easy to tool. The best CTE match, however, is provided by single-crystal silicon substrates.

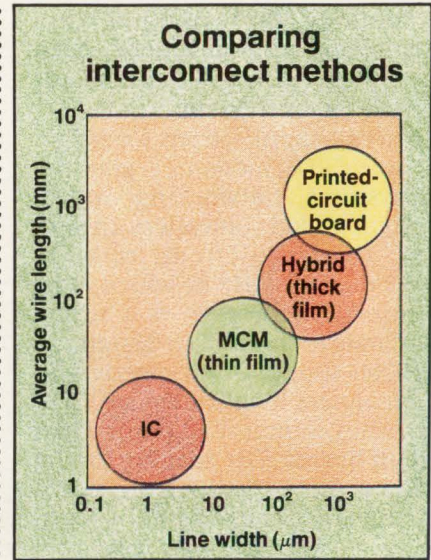
Silicon may be the ideal substrate material for multichip modules. In addition to having an identical coefficient of thermal expansion, it offers high thermal conductivity and a low dielectric constant. It also allows passive elements such as terminating resistors and decoupling capacitors to be integrated into the substrate.

One firm's answer to the question of substrate material is the

"no-substrate" module. Chips are flip mounted directly to a tape film stretched across a frame. Connections are made using reach-through vias, a solderless process that eliminates the need for bumps.

Pioneered by Polyolithics Inc., Santa Clara, Calif., the method recently won an endorsement from the Air Force, which awarded the firm a Small Business Innovative Research contract. The contract is part of the Air Force's new Electronic Packaging and Interconnect Initiative under the direction of Wright Research and Development Center, Wright-Patterson AFB, Ohio.

**Dielectrics:** Dielectrics provide MCMs with passivation and insulation, just as in ICs. Packaging engineers are experimenting with several materials. Not surprisingly, silicon dioxide is a frequent choice. Others report success with organic polymers such as polyimide and BCB (benzocyclobutene). Though most di-



**INTERCONNECTS ARE shorter on multichip modules than on hybrids or printed-circuit boards, giving MCMs a distinct advantage where circuit speed and small size are important. And because MCMs use thin-film metallization techniques, they have line widths approaching those of ICs.**

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## Advances In Soldering

THE SOLDERING of leadframes to circuit boards is part of the critical path in electronic packaging. Slowdowns here cannot be tolerated. But as lead spacings become finer — some are only 10 mil apart — the limitations of conventional solder technology are beginning to cause problems. The biggest barrier seems to be the minimum resolution that the reflow process can provide without forming solder bridges.

With lead spacings smaller than 20 to 25 mils or so, standard infrared (IR) and vapor-phase reflow soldering techniques are inefficient. Instead, manufacturers are using a new soldering method called hot-bar reflow. The bar, called a thermode, is positioned over the leads and is pulse-heated to the reflow temperature of the solder. Because the thermode comes down cold it can also be used to press the leads to the bond pads.

Another advantage of hot-bar reflow is that it allows circuit-board bond pads to be plated rather than screened with solder. Higher resolution (finer lead pitch) and fewer cleaning steps are among the benefits of bond-pad plating.

Leads are also being preplated to improve the resolution of the soldering process. Inner leads on 8-mil-pitch TAB frames, for example, are plated with a gold/tin alloy and soldered by thermode to the IC. Once the hot bar heats to the eutectic point, about 550°C, the alloy reflows and forms a strong bond with a pull

strength of up to 25 g.

Other preplating materials include solder and palladium, but solder can only be used when subsequent thermal steps such as chip attachment and wire bonding are kept under 200°C. As new soldering methods mature, such as laser soldering, more and more preplating materials will be feasible. Laser heating is said to provide the tightest control over solder profiles.

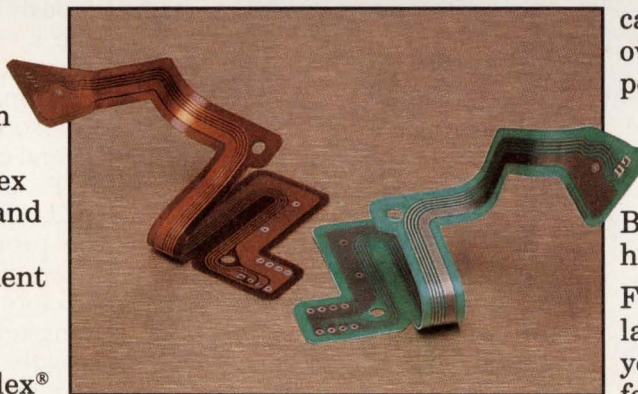
Patternable fluxes and pastes are also beginning to emerge. These fluxes minimize bridging and provide adhesion for package leads. In addition, solder suppliers are developing alcohol and water-based fluxes, some of which require no cleaning steps. Low-halide fluxes that reduce oxides and enhance wettability and low-melting point mixtures of indium and bismuth hold promise as well. Another trick is to use peel-away preform tapes that break solder bridges when removed.

Researchers at Texas Instruments, also working on the solder-bridge problem, have developed a new way of soldering called delayed reflow. Reflow is delayed because the solder is applied in a form where the tin and lead are not fully mixed. By the time board temperatures stabilize, the alloy mixes and temperature distribution is nearly uniform at the instant of reflow. This prevents bridging because of optimum solder profiles and better wetting of the parts to be connected.

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electronics are applied using thin-film deposition techniques such as sputtering, spin-on, and spray-on, some manufacturers employ tape-based delivery systems.

Polyimide is the most widely used dielectric for MCMs because it can be easily applied to both silicon and ceramic substrates. In either case, conductive traces normally consist of polyimide on copper, a combination that causes minimal propagation delay. Experts claim that low-stress and acetylene-terminated polyimides are best suited for these applications. In contrast, BCB is typically used to insulate conductors on copper-clad silicon carbide and aluminum nitride.

A few manufacturers, such as nChip Inc., San Jose, Calif., employ silicon dioxide as an insulator for MCMs. Users say that it is less expensive, requires fewer processing steps, and absorbs less moisture than polyimide. And because it is more thermally conduc-

## New Packages Blur Chip Boundaries

SEMICONDUCTOR MAKERS say that their products may someday be differentiated more by packaging options than by anything else. One example: A new 16M-bit DRAM. On the outside, the chip carrier looks like a standard Jedec SOJ (small-outline J-leaded) package. On the inside, both the lead frame and IC itself sport clever designs.

Instead of using perimeter bond pads, the rectangular die has only one row of pads that run along the center. The leadframe fastens to the chip with double-sided adhesive tape and is conventionally bonded with short gold wires. Called the LOCCB (lead-on-chip with center bond), a joint development of Texas Instruments Inc. and Hitachi Ltd., the package is also being considered for high-speed SRAMs, 64M-bit DRAMs, and ECL circuits.

Center bonding improves on edge bonding by saving die space, reducing interconnect length, increasing speed, and by providing uniform lead capacitance. In contrast, lead capacitance in standard SOJ packages can vary by over 20%, causing major timing problems.

LOCCB is representative of a new design approach that optimizes the IC and its carrier as a single unit. For example, chips packaged this way need one less metal layer because the leadframe distributes power over two buses that run the length of the chip. The scheme not only eliminates one mask step, but also provides 10 times more immunity to electrical noise than where an embedded metal layer delivers power.

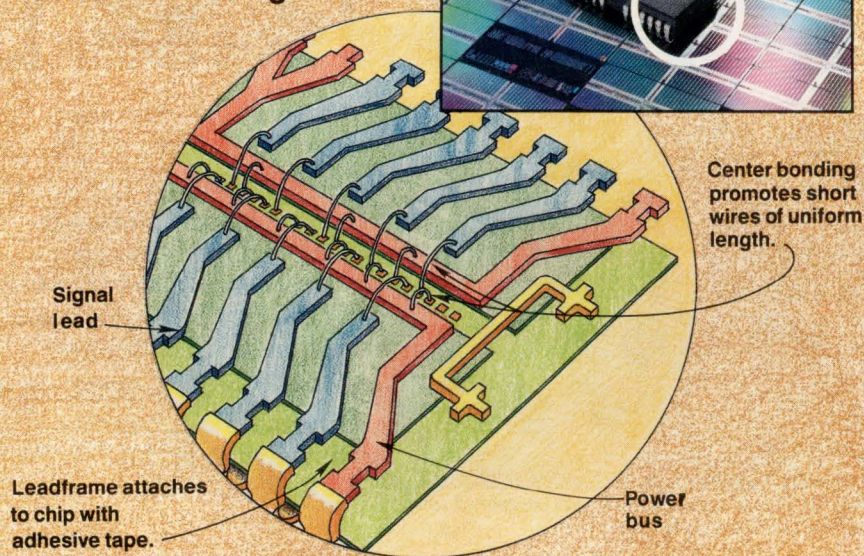
Although the first release of the LOCCB is wire bonded, future versions could be TABed or attached directly to copper leadframes. Copper leadframes, 2 to 3 mil thick, can be coated with gold or

palladium and bonded to the chip through thermocompression. Leads can attach directly to on-chip aluminum bond pads or through plated gold or copper bumps.

Thermocompression combines heat and pressure to fuse metals at lower temperatures than previously possible. Experts say that the method can produce bonds up to 10 times stronger than conventional gold-wire connections. It also requires less vertical and lateral clearance than wire loops.

To attach to aluminum bond pads, the surface metal must first be protected. Packaging engineers do this by sputtering a refractory metal such as titanium or tungsten, then a noble metal such as gold or palladium. The refractory provides mechanical protection, while the noble metal prevents corrosion.

### An inside look at center bonding

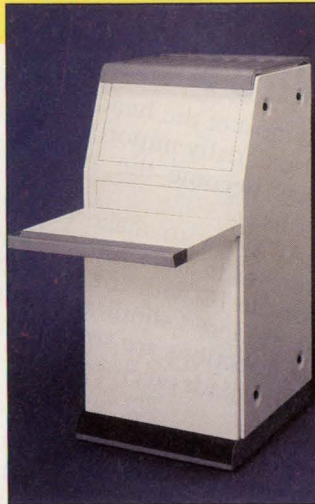


**A NEW CHIP package called the LOCCB (lead-on-chip with center bond) from Texas Instruments and Hitachi enhances the performance of DRAMs and other circuits. It accommodates chips having bond pads along the center, a configuration that reduces chip size, wire-bond length, and timing skews.**

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tive, it eliminates the need for thermal pillars that normally cool polymer-insulated substrates. These structures generally lie under the die to shunt heat to the back of the substrate, but consume valuable space that otherwise could hold interconnects.

Multichip designers have avoided silicon dioxide because they cannot grow layers thick enough to isolate conductors. A newly developed plasma process, however, makes it possible to deposit up to 20  $\mu\text{m}$  of high-integrity oxide. The material is sputtered under controlled compression to cancel tensile stress and prevent cracks and warpage.

**Interconnect:** What sets MCMs apart from printed-circuit boards and hybrids is the ratio of die-to-substrate area. This important figure of merit is determined chiefly by the interconnect system. In circuit boards and hybrids, die-to-substrate area is about 15% tops. But using thin-film photolithography — the same technology used to make ICs — multichip modules are hitting ratios as high as 90%. The reason is that MCM designers can apply almost any conductor (Cu, Al, Au) to almost any substrate with resolution of about 10  $\mu\text{m}$ .

There are two basic approaches to interconnecting dice in multichip modules. One is a "chips-first" approach, used by General Electric, Texas Instruments, and others, in which dice are placed face-up in cavities milled into ceramic substrates. Polyimide tape is laminated over the top of the chips, forming a planar surface. High-density interconnect, usually copper, is then deposited over the polyimide. Laser-drilled holes create vias and open passages for I/Os. Additional layers are built up with spun-on or sprayed-on polymer films.

The alternate way of synthesizing MCMs, a "chips-last" approach, is compatible with both silicon and ceramic substrates. Here, aluminum or copper interconnect is deposited on the substrate before the chips are at-

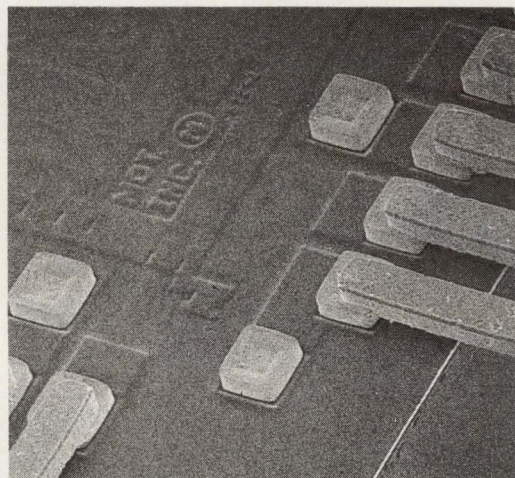
## Tab Untangles Wire Nests

THOUGH MCMs are grabbing most of the headlines, other advanced packaging technologies may be equally important. In particular, TAB (tape-automated bonding) has become the attachment method of choice in fine-pitch applications.

Tape-automated bonding is a way to make chip connections en masse, rather than one at a time as is done with a wire bonder. A rigid leadframe is positioned over the IC with inner leads aligned to the bond pads. Connections are soldered simultaneously, often by a hot-bar reflow process. These connections are stronger, pose less impedance, and accommodate smaller pads on closer centers than wire-bond attachments.

TAB leadframes are formed from various materials, ranging from multilayer tapes to copper film. Lately, TAB tapes are becoming more and more sophisticated and are assuming functions beyond mere interconnection. New tapes are going to two and three layers of metal to provide shielding, impedance matching, and the distribution of power and ground. And advanced dielectrics such as polyimide are providing dual functions of mechanical support and electrical insulation.

Signal planes, which contain up to 360 traces, are typically 1-oz. copper with a nominal thickness of 1.4 mil. Ground planes consist of



**TAPE-AUTOMATED BONDING (TAB) replaces wires with flexible beams 1 × 2 mil in cross section. The beams are tin-plated copper and are part of a rigid frame supported by polyimide tape. Inner leads, shown at 170× in this SEM close up from Motorola Inc., solder to gold-bumped bond pads on 4-mil centers, providing 360 pin outs for the IC.**

copper as well and are electrolessly plated with a thin layer of tin 10 to 30  $\mu\text{in.}$  thick. Plating thickness determines how easy or difficult the inner lead bonding will be. Excess tin tends to cause lead-to-lead bridging, while too little tin may leave solder joints open.

Another mass-bonding technique rapidly gaining acceptance is called flip chip or bump bonding. Dice are placed face down on the mounting substrate over a matrix of soft metal bumps. Because interconnections to the IC are only a few thousandths of an inch long, signal delays and degradation are minimized. Flip chips have the smallest possible footprint because there are no connections outside the perimeter of the die.

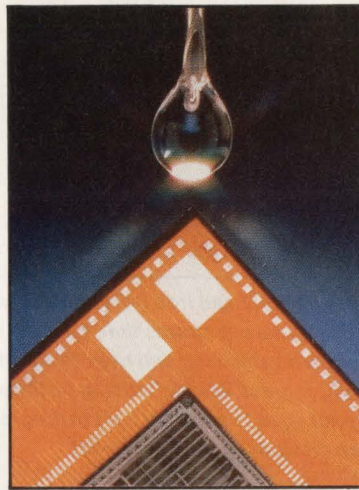
Bump-bonded dice have a large capacity to dissipate heat. Heat shunts away from the active circuits through the metal bumps in one direction, and to the exposed back surface of the die in the other direction. Cooling gels and heat sinks are often applied to accelerate heat transfer from the chip. Cooling can also be enhanced by an "integrated cold plate," a novel technique in which grooves are etched into the back of the silicon to increase surface area.



## New Materials Cure Packaging Headaches

ADHESIVES AND COATINGS are among the most critical elements in electronic packaging because they frequently come into contact with the silicon. These materials must be thermally conductive, easy to apply and cure, safe for the environment, and similar to silicon with respect to thermal expansion.

One promising new material to provide adhesion and coating in electronic packages is silicone. General Electric's GE Silicones, Waterford, N.Y., for example, offers a wide assortment of silicones for everything from coating semiconductor junctions to encapsulating power IC modules. Silicone is a solventless material that needs no primer for adhesion and eliminates the risk of ionic contamination. It can be formulated in both soft gels and hard molding compounds, and the different mixtures can be layered to suit the application.



**SILICONES ARE SAFE** enough to use in direct contact with silicon junctions and are safe for the environment as well because they require no solvents. They can also be used as conformal coatings on conventional circuit boards and to seal chip-on-board and power hybrid assemblies.

tached. Depending on the substrate, silicon dioxide or polyimide serves as the dielectric. Dice are then bonded through flip-chip or TAB connections. E-Systems Inc. of Dallas, Tex. and nChip are using this method.

To prevent polyimide from oxidizing copper and raising the dielectric constant of the interface, a protective coating of chromium, nickel, or titanium can be applied. Sputtered aluminum can also be used in place of copper.

One of the advantages of depositing copper or aluminum on silicon dioxide is that surface conductors can be isolated on rails of oxide. This reduces interconnect capacitance by a factor of two and cuts propagation delays in half with an effective dielectric constant of 1.9.

Embedding metal in silicon dioxide also opens the door to multifunctional structures. For example, the dielectric that separates the ground and power planes forms an integral decoupling capacitor, distributed over the metal-oxide-metal sandwich. It also sets up a resistive layer that can replace discrete components to terminate 50 to 100- $\Omega$  lines.

MCM manufacturers are currently trying to exploit these and other novel features. For one

thing, they are developing "generic substrates" that can be mass-produced and stored for future use. These substrates — having ground, power, and  $x-y$  signal layers — can be quickly customized

when needed. Interconnect is mask programmable, and ultimately will be programmed by the user on-site. Spearheaded by MCC Corp., QTAI (quick-turn-around interconnect) is being produced

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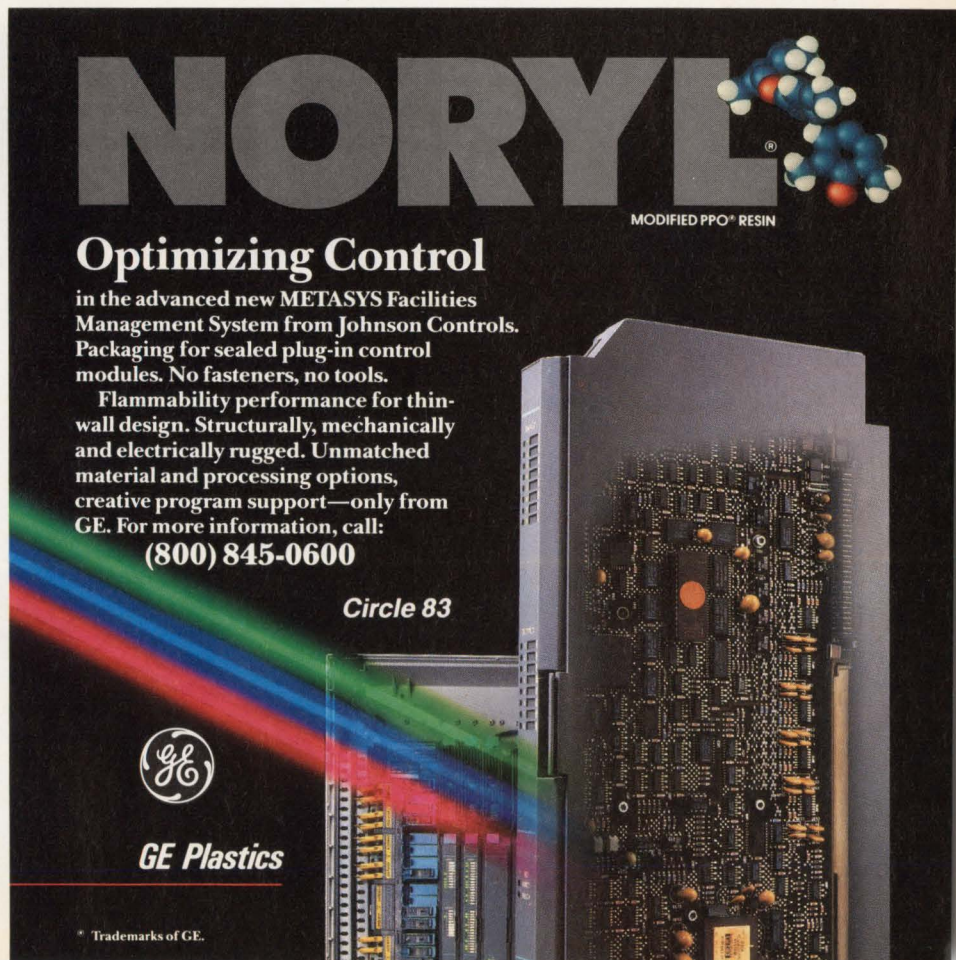
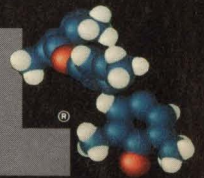
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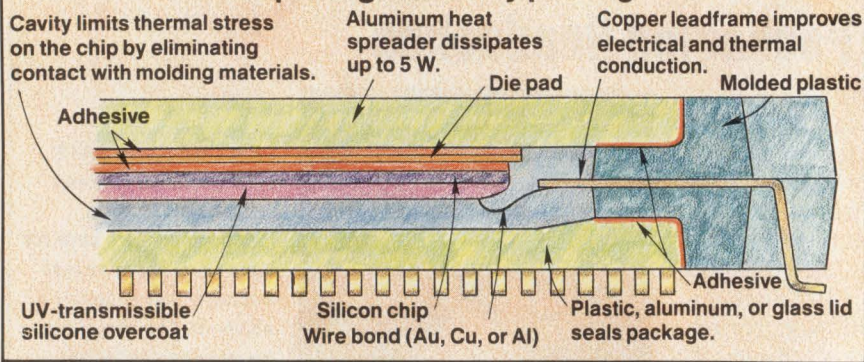


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### Exploring the cavity package



**CAVITY PACKAGES** allow chips to be enclosed free from contact with molding materials. Dice mount on plastic or metal substrates that, besides providing mechanical support, contribute to electromagnetic shielding and heat dissipation. The packages are sealed with plastic, aluminum, or glass lids, depending on the application. Glass lids, for example, seal EPROM packages to allow UV light to program chips, while aluminum-topped packages can dissipate up to 5 W of heat.

by Harris Corp. and Eastman Kodak Co., both MCC shareholders.

Researchers say the next step will be to redesign standard ICs to take advantage of special conditions in MCMs. Because chips are closer together, for example, out-

put buffers can be smaller since they need not drive as large a load. It also stands to reason that static-discharge and surge-protection cells can be eliminated because package I/Os are typically protected. And in MCMs with active

substrates, power distribution and communication circuits can be moved off chip. In all, module/chip synergy will make the entire assembly faster, smaller, and less expensive.

### HIGH-LEVEL PACKAGING

Electronic packaging is divided into several functional levels with respect to the chip. For reference, the chip is said to be at level zero. Chip packages — DIPs, carriers, flatpacks, and PGAs — are level one. Electrical and mechanical support of level-one components is second-level packaging, circuit boards in the classic sense.

Like everything else in electronics, printed-circuit boards are getting smaller, faster, and denser. So much so, in fact, that the delineation between multichip modules and circuit boards is beginning to fade. As a result, circuit-board designers face many of the same tough problems that plague MCMs, but they can also draw from a wealth of new materials, processes, and assembly methods developed by semiconductor and module suppliers.

To combat heat-dissipation problems, for example, board designers are turning to copper heat shunts or "thermal vias" similar to those used in MCMs. On another front, TAB (tape-automated bonding), flip chip, and aluminum wire bonding are employed in various combinations to shrink circuit boards or free up board space.

Other circuit board problems are solved by mounting TAB leadframes to the board to absorb thermal-expansion mismatch between the die and the substrate. Multilayer tapes can also provide impedance matching between silicon and board contacts. Called chip-on-tape, this mounting method offers the small footprint of a bare die, yet circumvents the testing dilemma through lead fan-out. Chips can be bumped or wire bonded to the tape.

To handle flip chips on circuit boards, new bump-bonding methods have been developed that withstand significant electrical

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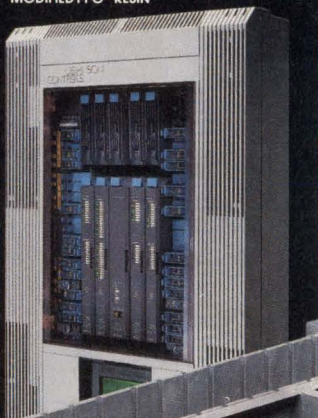
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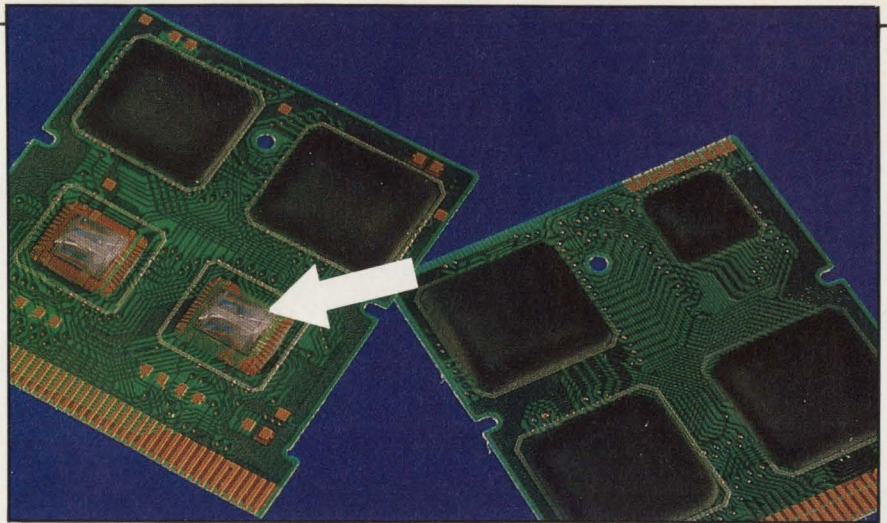
and mechanical abuse. In one method, die are bumped with copper "studs" to improve the electrical and thermal interface. The solder-capped studs are aligned to aluminum bond pads, often protected by a thin-film system of refractory and noble metal. Special techniques are used to protect the silicon with either polyimide or silicon nitride dielectrics.

Advances in soldering technology are also migrating from modules to boards. Hot-bar soldering, for example, developed for tightly spaced inner leads on TAB frames, is now being used to make outer-lead connections to circuit-board substrates.

Through technology transfer, circuit boards are looking more and more like multichip modules every day. In fact, some predict that one-third of all semiconductors will be housed in MCMs by the end of the decade. The few functions left to circuit boards will be provided by other levels of packaging, and MCMs will have fulfilled their purpose: to eliminate a level of packaging and bring chips closer together.

The year 2000 is likely to see modules and hybrids plugged into backplane-like structures. MCM packages, conforming to quad flat-pack standards, will insert into surface-mount sockets with zero-insertion force connectors. These packages are already available in ceramic and aluminum nitride, and plastic versions are expected to be out soon. Called cavity-down packages, they allow heat to escape through the top of the module and even include integral metal shielding.

Packaging experts believe that connection systems that link MCMs, discretives, and passives will start to grow in the "z-direction" orthogonal to the substrate. This is already under way with three-dimensional packaging schemes that stack 50 to 75 bumped chips in the form of a cube. Multilevel TAB structures also allow several chips to be stacked. By standing dice on end, single in-line packages (SIPs) and zigzag in-line



**CHIP-ON-BOARD assemblies are becoming more uniform and reliable because of improved encapsulants and application equipment. The clear encapsulant, a UV-transmissible epoxy from Dexter Corp., Industry, Calif., seals unpackaged EPROMs on a board made by Sharp Electronics Corp. for its "pocket planners".**

packages (ZIPs) make use of the third dimension as well.

These developments are revolutionizing design. Because of MCMs and multifunctional interconnect, electronics are increasingly located at the spot where

they are needed rather than linked over a cable. Disk-drive chips, for example, are often mounted on the read/write head, and in anti-lock braking systems, control circuits are often fastened to the brake caliper itself.

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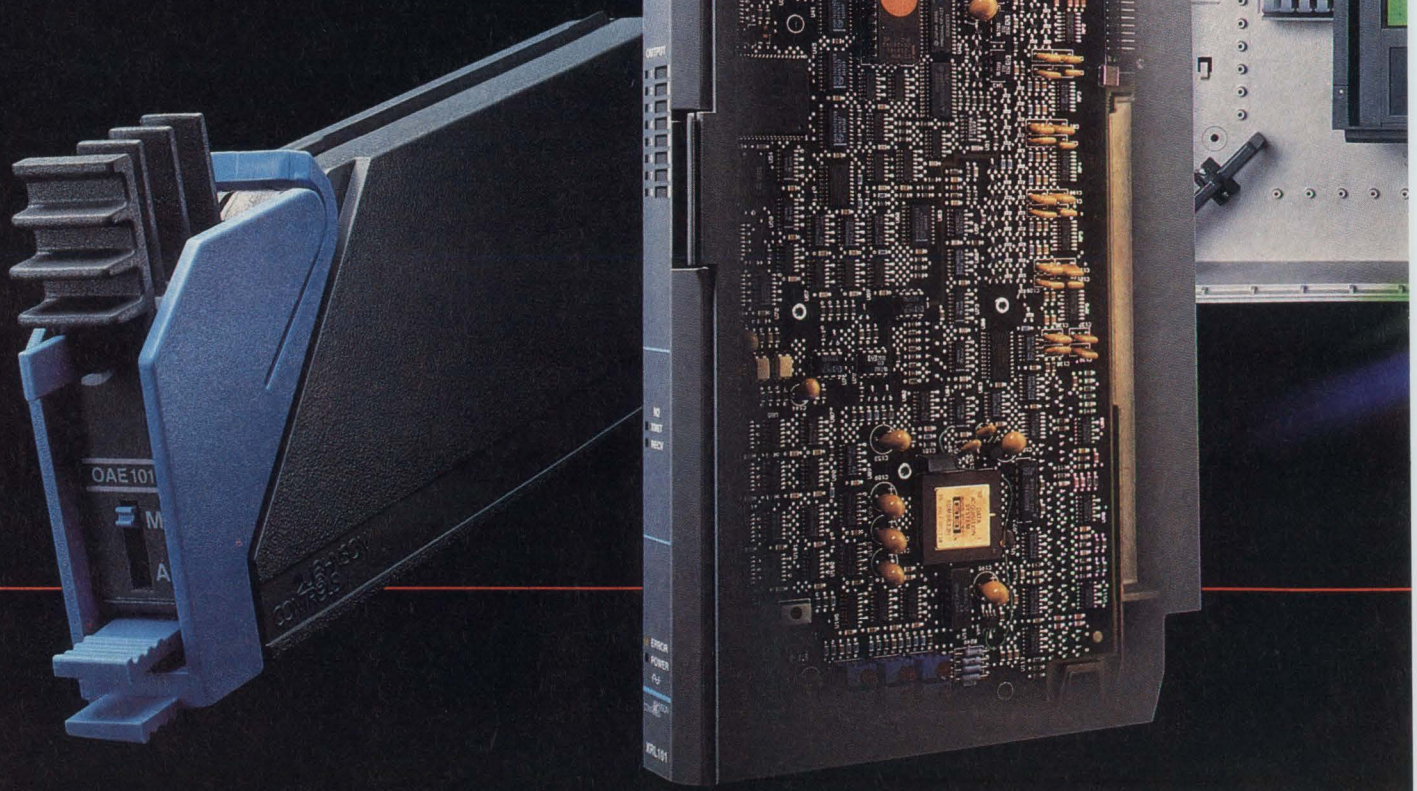
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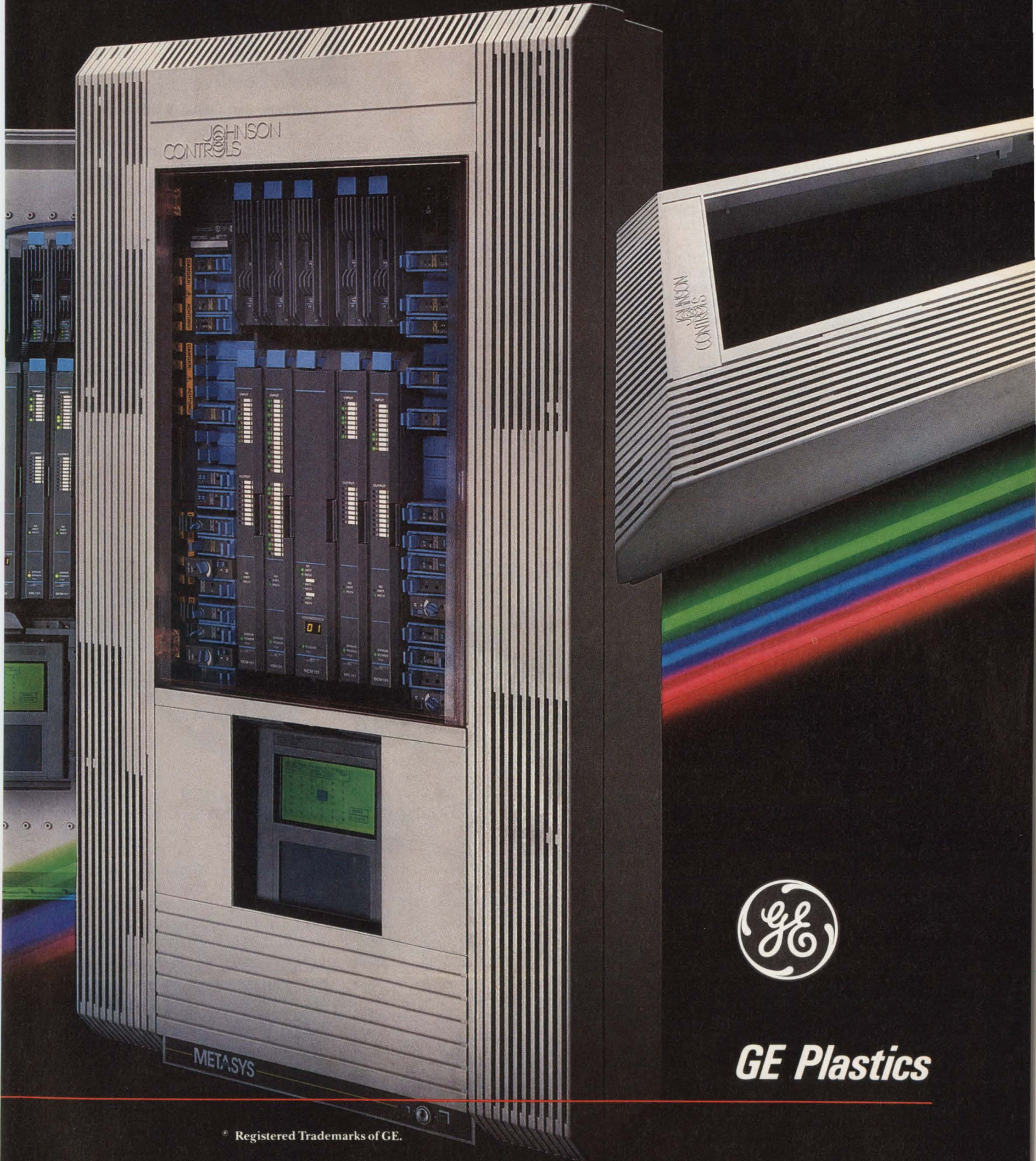
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# ELECTRONICS PACKAGING AND MATERIALS Resource File

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This 40 page catalog contains a wide selection of standard products that can be shipped in a matter of days after the order is placed. Zero is one of the nation's largest manufacturers of cases, cabinets, enclosures and related hardware. The catalog provides nearly 30 product groups.

Zero Corp., Burbank, CA (818)846-4191

**CIRCLE 84**

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Rogers Corp., Rogers, CT (203)774-9605

**CIRCLE 85**

## AUTOMATED PACKING SYSTEM'S



### H-75B

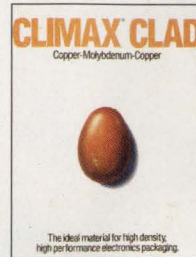
The H-75B is an improved tabletop bagger that works more quietly and efficiently than ever before. The H-100 is an all purpose high-speed plastic packager that bags up to 45 bags per minute. (800)331-4414

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## COPPER CLAD MOLY



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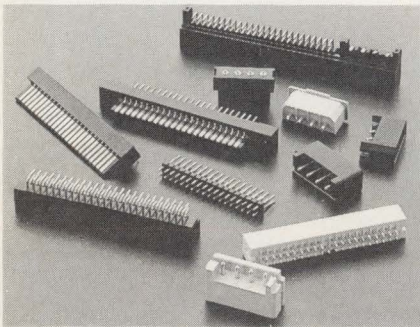
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## ELECTRONICS PACKAGING AND MATERIALS

### PLASTIC FOR SMT CONNECTORS



ENGINEERING thermoplastic, Stanyl 46 nylon, has high-heat distortion temperature of 545°F, high modulus and low creep at elevated temperatures, and high fatigue and chemical resistance. The nylon material is for electrical/electronic components, especially close-tolerance surface-mounted connectors and terminal-block housings where products with-

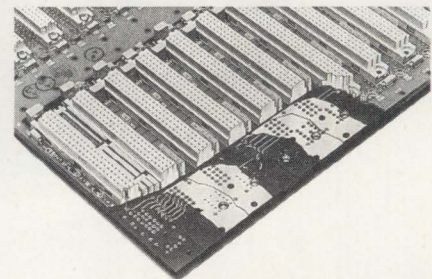
## PACKAGING MATERIALS FOR ELECTRONICS

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**Circle 89**

stand demands of IR, wave, and vapor-phase soldering. Product is said to provide three times the dry impact strength of conventional nylons. *DSM Engineering Plastics, 501 Crescent Dr., Reading, PA 19612.*

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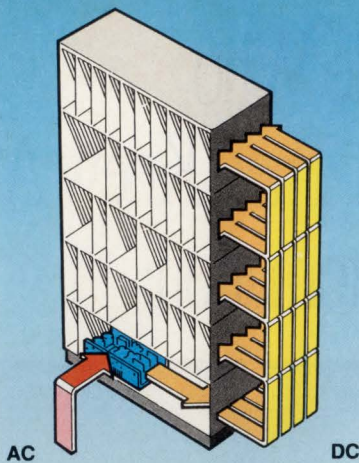
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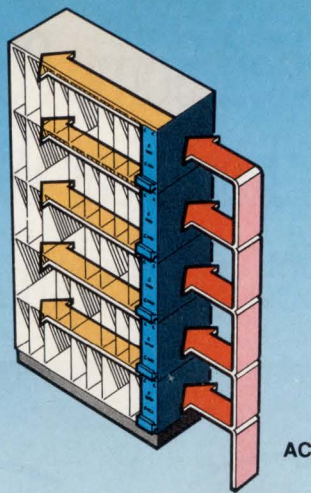
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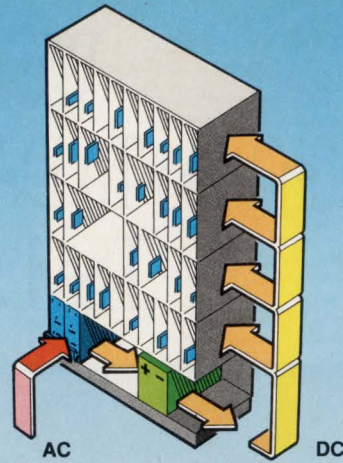




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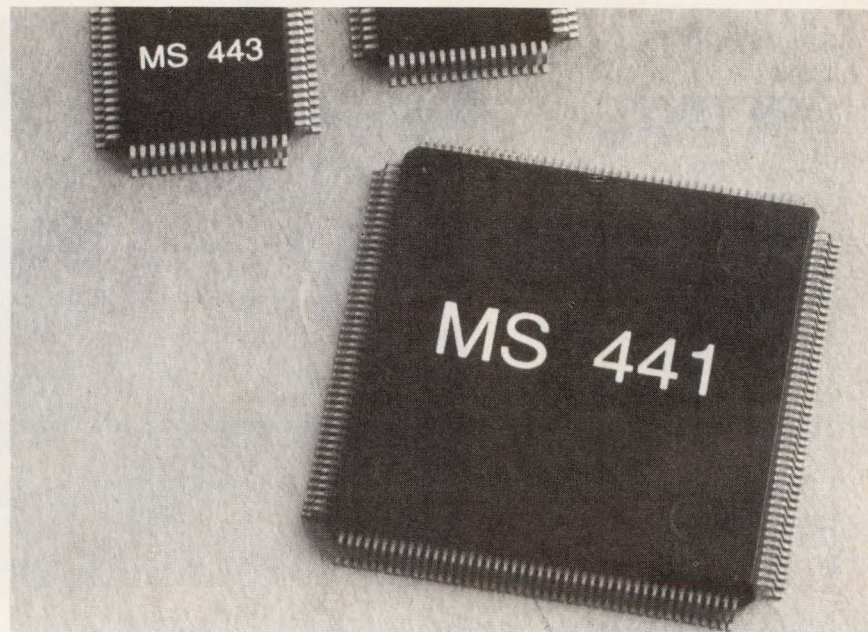
DAVE BURSKY

**W**ith custom static RAMs that support a new cache architecture called concurrent write-back, system designers can achieve write hit rates of 99.8% and read hit rates of 96% for 80386- or 80486-based systems. The Simulcache chip set from Mosel achieves such high hit-rate levels by optimizing for zero-wait-state performance on CPU writes as well as on CPU reads. Concurrency enables the CPU to read and write back to the cache while the cache simultaneously performs "housekeeping" tasks in the background. Thus, in 99.8% of the write cases, the CPU can send data to the cache without waiting. The high write-rate hit is particularly valuable in 80486-based systems, which typically have about 75% of their bus activity composed of writes.

The Simulcache chip set, which consists of a controller chip and dedicated cache-RAM chips, ties into either the 80386 to form a primary cache subsystem or the 80486 processor to form a secondary cache. Initial versions of the chip set will support CPUs running at 25 to 33 MHz with zero-wait-state memory access. The MS441 concurrent write-back cache controller manages all of the data transfers between the CPU, the MS443 dual-ported cache-memory chips, and the system logic chip set and main memory.

On the controller chip are two bus controller subsections, one to manage the CPU interface and the other to manage the logic chip-set interface. Also included are the cache-tag array, a data-path control unit, and the concurrent bus control unit. The tag block holds 2000 entries and is two-way set-associative. Users can configure the controller to set up four programmable cache regions, each with noncacheable, cacheable, and cacheable-write-protect modes.

The supporting dual-port SRAMs include special data-path registers that hold hit and miss addresses, and



read and write registers that hold data. Two banks of memory cells on the chip, both organized as four planes with each plane holding 2-words-by-9-bits, give the chip a total capacity of 144 kbits, including parity bits. Data can be loaded or read with standard address-access modes, or when trying to quickly transfer data. During a cache update, the memories can be switched to their "turbo" mode, which allows burst data transfers at up to 256 Mbytes/s.

Unlike the 80486, which only does burst reads, the chip set supports both burst reads and writes. As a result, cache write-back operations can be done at twice the speed of ordinary writes, improving system throughput. Although the off-chip peak transfer rate is 256 Mbytes/s over dual 36-bit data buses, the cache RAMs internally transfer data at more than twice that speed—533 Mbytes/s.

Each RAM has an internal 32-bit data bus, so four RAM chips can be cascaded to form a 64-kbyte cache with a 128-bit line width. The cache RAM can simultaneously latch up to 16 bytes in a single clock, to lock data

in for a full line replacement. The cache subsystem employs an internal data path similar to that used inside the 80486 CPU. The on-chip data path registers channel data into, out of, and around the memory array in single-clock increments.

Besides serving as a cache, the chip also has a bypass mode that allows fast data streaming directly between the system port and the CPU port of the MS443, while imposing only a 5-ns delay. That mode is particularly useful when a Read Miss occurs. Also, the internal pipeline of the memory chip makes it possible for the chip to implement self-timed write operations to make the most of available timing overlaps.

The MS441 cache controller comes in a 184-lead plastic quad-sided flat package, while the MS443 cache RAMs are housed in 64-lead PQFPs. In quantities of 10,000, the MS441 sells for from \$65 to \$114, depending on CPU type and speed grade. The MS443 sells for \$9 in similar quantities. Delivery of samples is from stock.

*Mosel Corp., 914 W. Maude Ave., Sunnyvale, CA 94086; Bert McComas, (408) 733-4556.* **CIRCLE 320**

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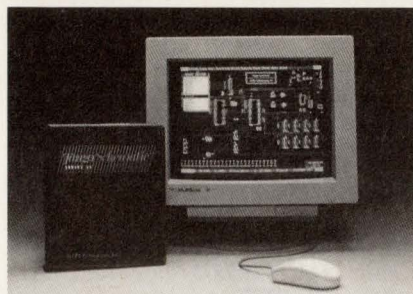
COMPUTER-AIDED ENGINEERING

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**Quickturn Systems Inc., 325 E. Middlefield Rd., Mountain View, CA 94043; (415) 967-3300. CIRCLE 321**

### SCHEMATIC CAPTURE HAS KEYBOARD MACROS



Version 1.20 of the Tango-Schematic schematic-capture software enables users to create their own keyboard macros. Other new features include support for PSpice and P-CAD net lists, autopanning, wildcard searching in the browse mode, the ability to display parts in the list box, and automatic placement of wire and bus names. Tango-Schematic comes with component libraries totalling 10,500 parts. Every logic gate also comes with its DeMorgan equivalent symbol. Library man-

agement facilities perform on-line listing and browsing of components, merging, and renaming. Tango-Schematic Version 1.20, which runs on PCs, is shipping now for \$495.

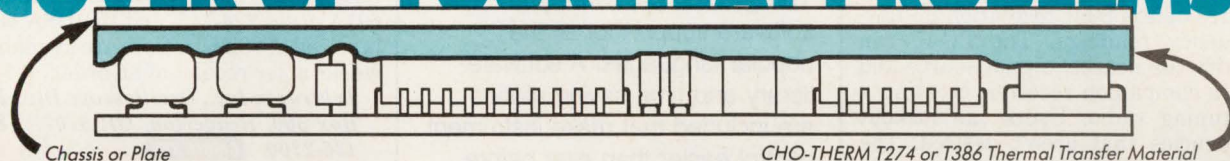
**Accel Technologies Inc., 6825 Flanders Dr., San Diego, CA 92121; (619) 554-1000. CIRCLE 322**

### HIGH-POWER BOARD LAYOUT RUNS ON A PC

The Schema PCB-2000 pc-board layout and routing package brings the power of a workstation tool to 80386-based PCs. PCB-2000 can handle designs with over 2000 ICs and up to 54 in.<sup>2</sup> board sizes. Users can define grids and tracks as small as 1  $\mu$ m; pad sizes and shapes are also user-defined. Schema PCB-2000 libraries have over 5000 parts. Components can be rotated in 1-degree increments. Schema PCB-2000, which runs on 80386-based PCs, is shipping now for \$6995.

**Omaton Inc., 801 Presidential Dr., Richardson, TX 75081; (800) 553-9119 CIRCLE 323**

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CHO-THERM T274 and T386 materials are pliable elastomers which blanket over uneven component surfaces to draw heat away from PC boards into metal covers, frames or spreader plates.

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Property	T274			T386		
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Voltage Breakdown Rating (VAC/mil)	200	150	100	450	240	150
Compression Deflection @30 psi, % Strain	4.5	8.4	18.1	3.5	6.8	9.0

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CIRCLE 112

ELECTRONIC DESIGN 117

APRIL 25, 1991

## NEW PRODUCTS

INSTRUMENTS

### IEEE-488



Control any IEEE-488 (HP-IB, GP-IB) device with our cards, cables, and software for the PC/AT/386, EISA, MicroChannel, and NuBus.

### PC-BASED COUNTER-TIMER FEATURES 2.4-GHZ RANGE

The PC-10 universal frequency counter-timer is an IBM PC plug-in board with a 10-Hz-to-2.4-GHz range. The unit's interface is a Windows 3.0-based control panel and display window. Sensitivity is 10 mV or better through the unit's frequency range. For optimum balance between sample time and resolution, the PC-10's input gate is continuously variable from 1 ms to 28 seconds. A reciprocal-counting feature offers 8-bit resolution on low-frequency readings. The PC-10 can identify the nearest signal source and tune a companion receiver, creating a self-tuning radio. Users can lockout frequencies that aren't desired. The counter includes an easy-to-use software self-calibration feature. The PC-10 costs \$335 in unit quantities and is available from stock. Model AP10H, an option that adds custom input amplifiers, signal conditioning, and frequency prescalers, costs \$295.

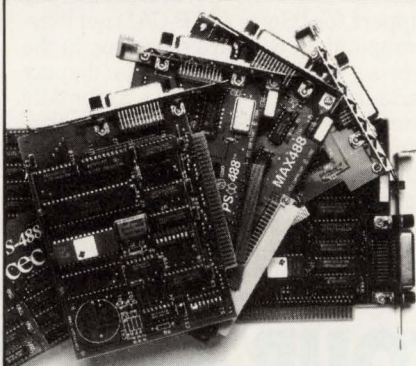
*Optoelectronics Inc., 5821 N.E. 14th Ave., Fort Lauderdale, FL 33334; (800) 327-5912 or (305) 771-2050. CIRCLE 324*

### DEVELOPMENT BOARD KEEPS COSTS DOWN

The DB-51 development board, geared for the budget-minded, allows designers to prototype and develop applications for the 80C51 family of microcontrollers. The board, which ties into a PC's serial port, offers extensive debug and development capabilities through a ROM-resident monitor and a host software package that runs on the PC. Sockets on the board allow the DB-51 to accept any member of the Philips Components-Signetics 80C51 family. Hardware included on the board con-

sists of an 80C552 that runs a monitor program held in a 32-kbyte EPROM, a preprogrammed 87C751 to handle the I/O, 32 kbytes of RAM, and a 1.25-by-7.25-in. prototyping area. Host software includes a symbolic debugger, an on-line assembler and disassembler, an upload and download facility, and other tools. Including the host software, the DB-51 sells for \$320. The user must provide a 5-V supply.

*Philips Components-Signetics Co., 811 E. Arques Ave., P.O. Box 3409, Sunnyvale, CA 94088-3409; (408) 991-2000. CIRCLE 325*



You get fast hardware and software support for all the popular languages. A software library and time saving utilities are included that make instrument control easier than ever before. Ask about our no risk guarantee.

### INTERFACE SYSTEM MAKES TIGHT VXI CONNECTIONS

An interface system for VXIbus mainframes offers one highly reliable connection between the mainframe and the unit under test. Two major components make up the system: an Interconnect Adapter and an Interlocking Receiver. The adapter connects the VXI card to two connector modules so that the entire module can be easily inserted and removed from the mainframe. Connections are completed with signal paths as short as 4 in. The receiver hinges downward for easy access to the VXI modules in the mainframe. When closed, the receiver automatically positions the connector modules. System prices start at \$3820.

*Virginia Panel Corp., 1400 New Hope Rd., Waynesboro, VA 22980; (703) 949-8376. CIRCLE 327*

### ANALYZERS ENHANCE PROCESSING ABILITIES

A number of new signal-processing functions and a built-in 1.44-Mbyte floppy-disk drive add to the capabilities of two digital-signal analyzers. The DSA 601A and DSA 602A perform inverse fast-Fourier-transform, convolution, and correlation operations, and can generate vertical or horizontal histograms. Other new features include the ability to select part of a waveform for further processing and a variable-rise-time low-pass digital filter for data smoothing. Users can select (six x)/x or linear interpolation to fill in between data points. The new 3-1/2-in. disk drive accepts MS-DOS format disks for storing waveform data and instrument settings for easy transfer to and from PCs. Several data formats are available to ensure compatibility with analysis and spreadsheet software. The 602A captures signals at rates to 2 Gsamples/s using four 8-bit ADCs with a 1-GHz bandwidth. The 601A, which acquires signals at 1 Gsample/s, has a 500-MHz bandwidth. Record lengths to 32 ksamples are available. A set of sophisticated trigger functions discriminate between glitches, too-slow logic transitions; runt, missing, or extra pulses; and timing violations. The DSA 601A costs \$24,745, and the DSA 602A is priced at \$32,635. Both are available 8 weeks after receipt of an order.

*Tektronix Inc., Oscilloscope Div., P.O. Box 500, Beaverton, OR 97077; (800) 426-2200. CIRCLE 326*



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CIRCLE 123

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## BOARD TEST SYSTEM FOSTERS CONCURRENT ENGINEERING

The HP 3078 board test system offers design-based tools to create a concurrent test environment that shortens time to market. The shared toolset helps designers communicate complex designs to test engi-



neers, so that test development can be complete when the design is.

The system works by integrating Mentor Graphics simulation tools and HP test software. The toolset includes schematics, simulation models, stimulus-response data, and test-simulation tools. With the aid of Mentor's QuickGrade and QuickFault, and HP's preview testability software, the test engineer develops digital functional tests concurrently with the design data.

QuickGrade is a graphical, statistical fault grader that delivers results faster than standard fault simulators. QuickFault creates thorough deterministic fault-coverage reports. HP preview software incorporates real-world test considerations into the circuit to improve it without affecting the design process. Instead of post-processing the design simulation results, the software simulates the tester and fixture effects on the design during the simulation.

The HP 3078 includes an HP 307X test head and controller, an HP Apollo Series 400 workstation, Mentor Graphics CAE software, and HP simulator-based digital functional test capability with concurrent-test-environment software. Prices start at \$460,000. The simulator and concurrent-environment capability can be added to an HP 3070AT/SMT and Mentor Idea Station for prices starting at \$61,000. The HP preview software can be added for \$31,000.

**Hewlett-Packard Co.** 19319 Pruneridge Ave., Cupertino, CA 95014; (800) 752-0900. **CIRCLE 328**

■ JOHN NOVELLINO

## INSTRUMENT LINE MAKES VERY PRECISE AC MEASUREMENTS

Expanding its traditional focus on low-level dc measurements, Keithley Instruments has introduced a line of precision ac instruments, including two 4-1/2-digit LCZ meters and three multifunction synthesizers. All are IEEE-488 compatible.

The Model 3321 and 3322 LCZ meters feature basic accuracy within 0.1%. D and Q resolution is 0.0001, and phase resolution is 0.01°. The 3321 has four test frequencies from 120 Hz to 100 kHz and manual or automatic trigger-reading rates to 150 ms. The 3322 offers 11 test frequencies to 100 kHz and also has deviation and binning capability. Reading rates to 64 ms are available.

The synthesizers employ a technology called direct digital synthesis, which makes it possible for the instrument to change frequencies immediately on command, without requiring several cycles to stabilize on the new frequen-

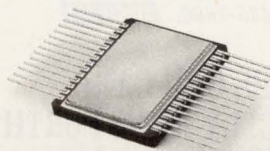
cy. This technique ensures phase-continuous waveforms. Accuracy is within 0.0005%, and resolution is 11 digits (12 digits on the 3940).

All three units have five built-in waveforms: trigger, burst, and gate functions; and on-off oscillation control. Ranges are 0 to 1 MHz on the 3910 (30-ppm accuracy), 0-1.2 MHz on the 3930A (5-ppm accuracy), and 0 to 20 MHz on the 3940 (5-ppm accuracy). The Models 3930A and 3940 can be used as sweep generators, with user selectable linear, logarithmic, or stepped sweeps.

The Model 3321 and 3322 LCZ meters cost \$3490 and \$3990, respectively. The 3910, 3930A, and 3940 are priced at \$1695, \$3590, and \$5390, respectively. Delivery is in 4 weeks.

**Keithley Instruments Inc.** 28775 Aurora Rd., Cleveland, OH 44139; (800) 552-1115 or (216) 248-0400. **CIRCLE 329**

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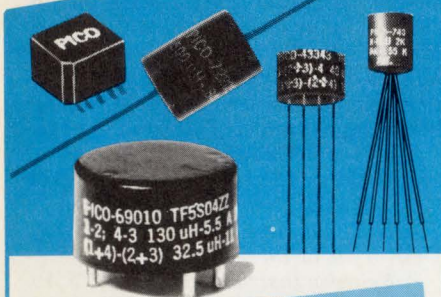
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CIRCLE 186

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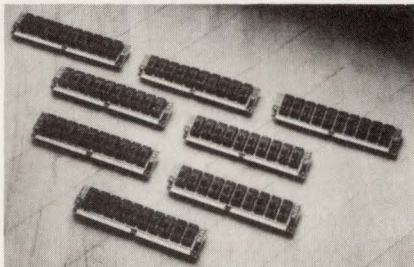
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CIRCLE 145

## NEW PRODUCTS

COMPUTER BOARDS

### MEMORY MODULES PLUG ONTO SYSTEM BOARD



Low-cost, third-party memory-upgrade kits are now available for IBM's System/6000 RISC workstations. The memory upgrades replace existing 8-Mbyte single-in-line memory modules (SIMMs) with higher-capacity modules. This saves cost because IBM's memory upgrade requires an additional board for each upgrade. The kits are available with either 2- or 4-Mbyte modules, for a maximum of 32 Mbytes. A 16-Mbyte upgrade kit costs \$3995, while a 32-Mbyte kit sells for \$8995. Both the 2- and 4-Mbyte versions are available from stock. Discounts exist for large-quantity purchases.

**Kingston Technology Corp., 17600 Newhope St., Fountain Valley, CA 92708; (714) 435-2600. CIRCLE 330**

### 15-MIPS CPU CARD DIRECTLY RUNS FORTH

The SBC32 Eurocard-sized single-board computer directly executes Forth-language programs at up to 15 MIPS. It's based on the SC32, a 32-bit stack-chip microprocessor developed at the Johns Hopkins University. The 100-by-160-mm SC/Fox SBC32 card with a 10-MHz SC32 CPU has a throughput that's comparable to 2 to 5 times that of a 20-MHz Intel 80386 CPU. On the card are a 56-kbit/s RS-232 serial port, 128 kbytes of shadow EPROM, and up to 512 kbytes of zero-wait-state static RAM. The board comes in 8-, 10-, or 12-MHz versions, and with 64 to 512 kbytes of static RAM. Software supplied in the EPROM consists of the SC/Forth-32 language, a Forth-83 standard with 32-bit extensions. The language takes advantage of the SC32's instruction set and architecture, automatically optimizing multiple Forth primitives into single-cycle machine instructions. Price start at \$1495 for the 8-MHz card with 64 kbytes of SRAM. A version that serves as a coprocessor in a PC/AT bus system sells for \$2295.

**Silicon Composers Inc., 208 California Ave., Palo Alto, CA 94306; George Nicol, (415) 322-8763. CIRCLE 331**

### X.25 WAN/LAN CONTROLLER FITS SBus

The SXCM three-channel X.25 controller is an intelligent high-packet-rate wide-area-network (WAN) controller for the SBus. This high-performance, data-communications front-end processor supplies control and interface for three full-duplex serial channels on a single-width card. The board supports T1 and CEPT (2.048 Mbits/s) data rates. Each serial channel may be programmed independently to support various data-communications protocols. These include bit- and byte-oriented synchronous, asynchronous, and packet-switched protocols. The SXCM is configured around a 20-MHz MC68302 16-bit integrated multiprotocol processor with 128 or 256 kbytes of external EPROM. It also includes 512 kbytes or 2 Mbytes of external DRAM for program and data storage. The controller board, available now, is priced at \$1800.

**Themis Computer, 6681 Owens Dr., Pleasanton, CA 94588; (415) 734-0870. CIRCLE 332**

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CIRCLE 130



# CLASSIFIEDS

## EMPLOYMENT OPPORTUNITIES

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Situated between the shores of Daytona Beach and metropolitan Orlando, talented professionals set the pace at **Sparton Defense Electronics**, a Fortune 900 company involved in the design and high volume manufacture of expendable submarine tracking devices.

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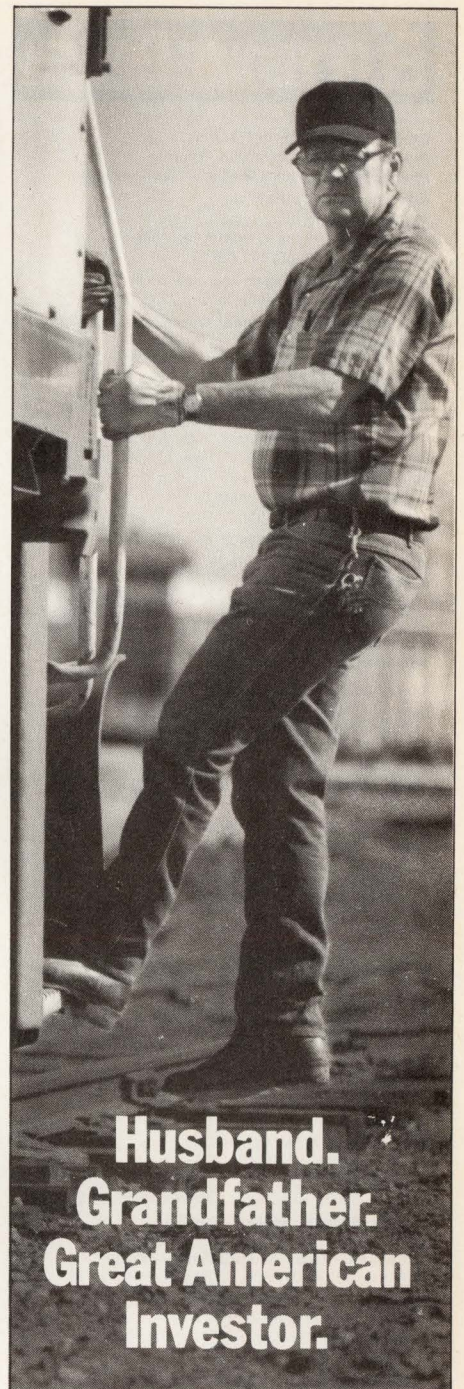
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## NEW PRODUCTS

COMPUTERS & PERIPHERALS

### 5-1/4-IN. DRIVES COMBINE 2-GBYTE CAPACITY AND 11-MS SEEK TIME

The release of Fujitsu America Inc.'s M2652 family has raised the capacity level of 5-1/4-in. Winchester disk drives. The M2652 family has an unformatted capacity of 2.0 Gbytes, an average seek time of 11 ms, and an average latency of 5.6 ms. This family is designed to meet the needs of high-performance computing systems, such as supercomputers, mainframes, and engineering workstations. To increase the speed of data access, the drives' spindle-motor speed was increased to 5400 rpm.

The family consists of four members: the M2652P, the M2652H, the M2652HD, and the M2652HS. Model P incorporates the ANSI standard IPI-2 (Intelligent Peripheral Interface), which offers 16-bit-wide data transfers. Model H uses the SCSI-2 interface to supply a burst data-transfer rate of 10 Mbytes/s. It also supports the long-cable lengths required in super mini-computers and mainframes.

The HD SCSI-2 drive allows parallel access to a storage device. The fourth member is the HS, a single-ended SCSI-2 model that's suited for deskside or desktop workstations. All four of the M2652 drives are constructed with 12 platters.

The family carries an MTBF of 200,000. This high reliability comes from an enclosure casting that contains a large surface area to dissipate any heat generated by the spindle and actuator motors. Because the actuator is integrated into the casting wall, heat is dissipated outside the drive. The drives' component count was also reduced, which cut power consumption in addition to raising reliability. Evaluation units of all four drives are available now. They are priced at \$5995. Production volumes will ship during the second quarter.

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### WORKSTATION FAMILY IS EXPANDED, UPGRADED

The RISC System/6000 family from IBM Corp. has been expanded to include new models, hardware upgrades, enhanced graphics, and expansion units. The Model 320H, evolved from the 320, was given a 25-MHz processor, upgraded from the previous 20-MHz unit. It also comes standard with 16 Mbytes of RAM, expandable to 128 Mbytes. The internal storage capabilities include a 160-Mbyte disk drive. A second similar drive is optional, as are two 320-to-400-Mbyte SCSI disk drives. The 320H is available now, starting at under \$20,500.

Another family addition is the Powerserver 950, a rack-mounted server. This system uses a 41.6-MHz processor and boasts 25.2 MFLOPS and a SPEC rating of 56.3. The system can be used either as a compute server or a high-performance multiuser system. It comes with 32 Mbytes of RAM, expandable to 512 Mbytes. Standard internal fixed-disk capacity is 857 Mbytes, with a maximum of 11.9 Gbytes. More fixed-disk space can be added with the 010 Drawer Expansion Unit, pushing the

total to 22.2 Gbytes. This system starts at \$164,335 and will be available in June. Users of the Model 930 can upgrade to the level of the 950 with a conversion option. This option is planned for September. The 010 expansion unit starts at \$9900.

Adding to the RISC System/6000 graphics capabilities is the Powergraphics GTO. This product also works with the Xstation 130, a low-cost X terminal. Xstation 130 comes standard with 2.5 Mbytes of memory and 1 Mbyte of video memory. Powergraphics GTO is an external graphics subsystem that offers high-performance graphics and supports PHIGS. It connects through a Micro Channel adapter. Powerstations that previously achieved 90,000 3D vectors/s now perform 990,000 vectors/s. The 8-bit version of Powergraphics GTO supplies 256 simultaneous colors and dual frame buffers. It sells for \$19,500. The 24-bit model, which goes for \$29,500, adds a shading processor and support for 16.7 million direct colors.

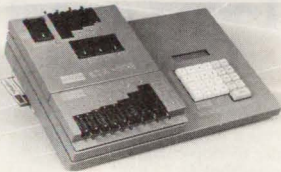
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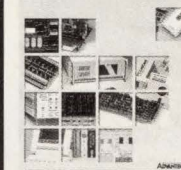
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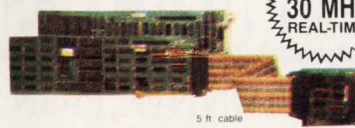
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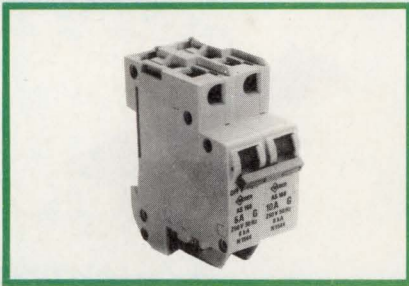


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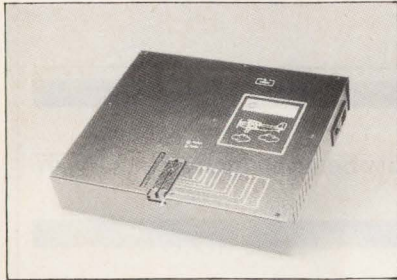
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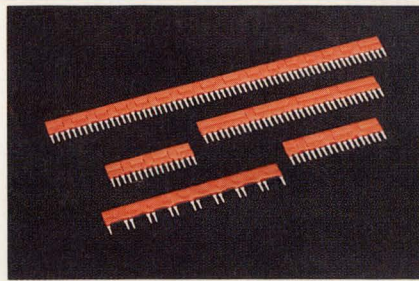
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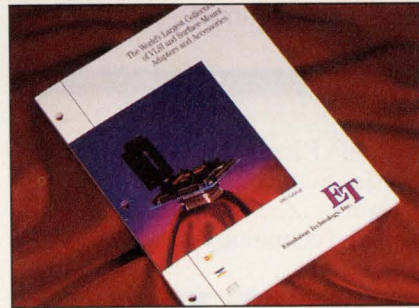
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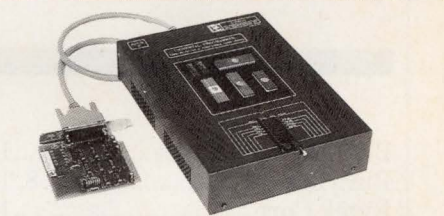
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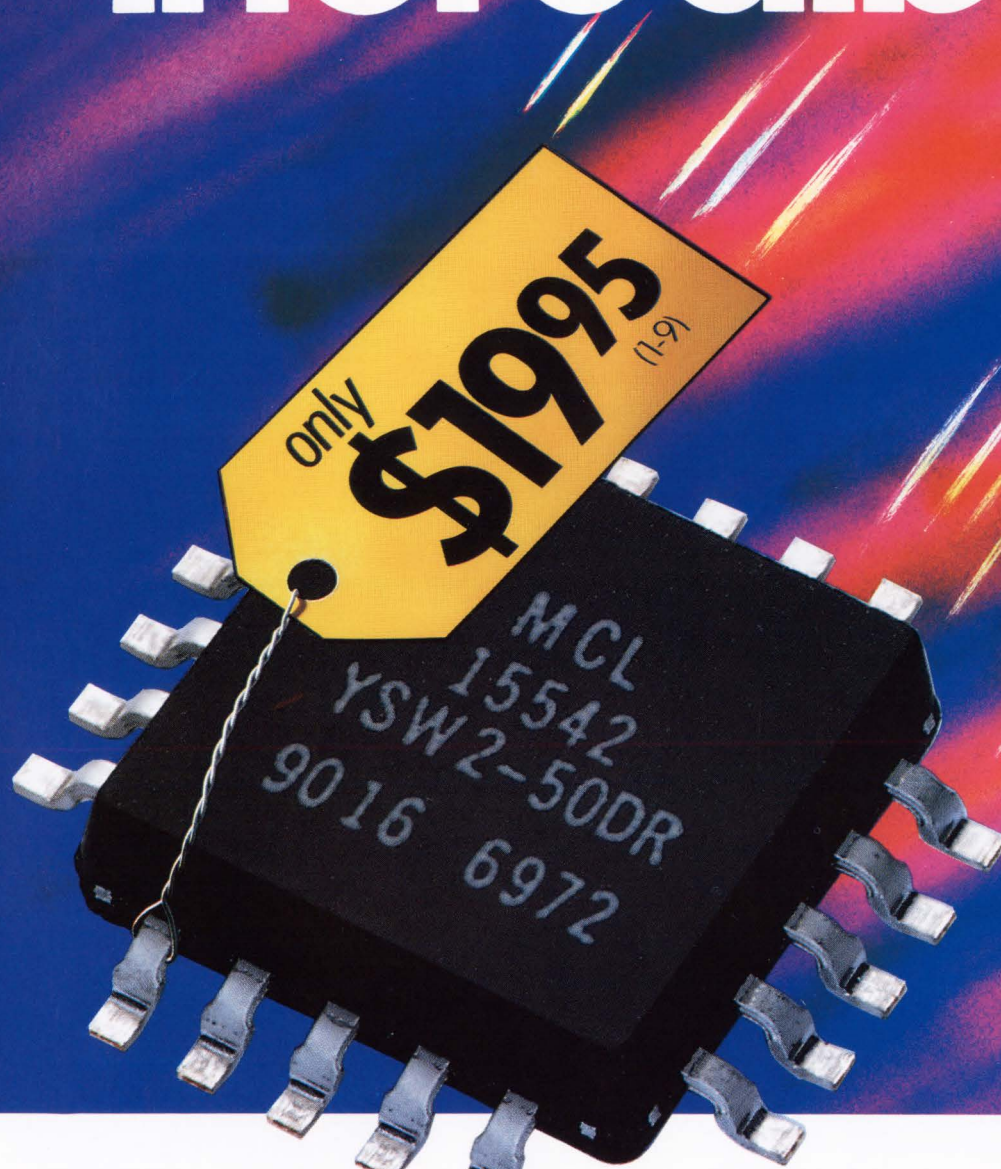
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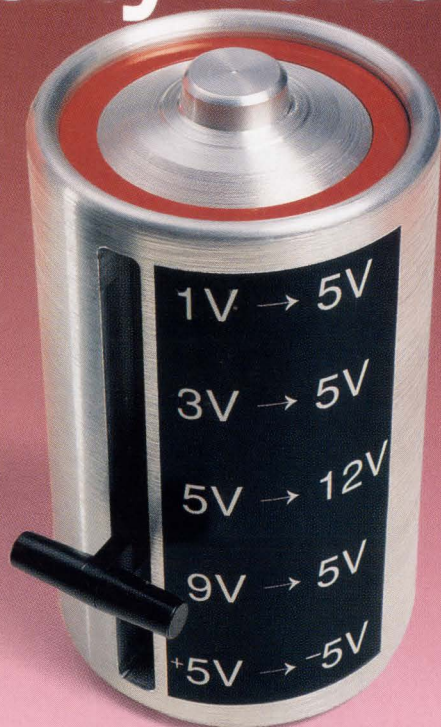


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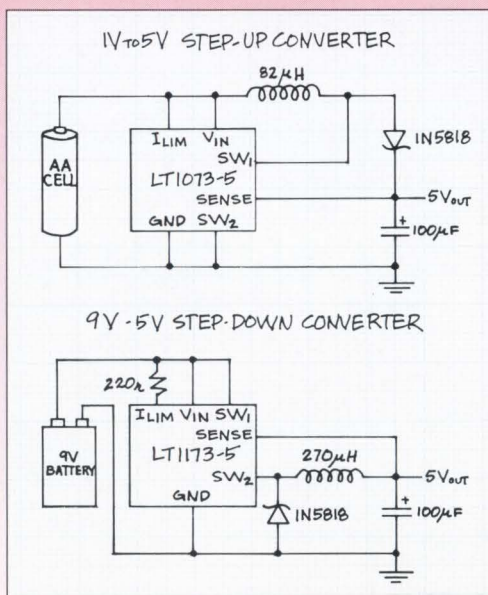
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- Only three external parts needed
- Operates at supply voltages from 1.0V to 12V
- Startup guaranteed at 1.0V
- Consumes only 95 $\mu$ A supply current
- Space-saving 8-pin Mini-DIP or SO8 package
- Works in step-up, step-down, or inverting mode
- Low-battery detector comparator on-chip
- User-adjustable current limit
- Internal 1 amp power switch
- Fixed or adjustable output voltage versions
- Programmable current limit with single resistor
- No frequency compensation required



Operation of the LT1073 is guaranteed down to 1.0V, so you can squeeze more useful energy out of a battery. Its duty cycle is set at 72%, optimizing operation where  $V_{OUT} = 3V_{IN}$ . And the LT1073 delivers 5V at 40mA from a single cell, and 5V at 100mA from a 3V input.

**The LT1173 is optimized for higher input voltages (two or more cells) up to 30V.**

It's ideal for low-to-medium power step-down applications. The 1173 features a 50% duty cycle and operates with as little as 2 volts input. Both the LT1073 and LT1173 are available now. Pricing in quantities of 100 are \$3.15 for the LT1073CN8 and \$2.40 for the LT1173CN8. For true micropower switching solutions and more details on these new parts contact: Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035. Or call toll free 800-637-5545.



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FOR TOUGH APPLICATIONS.