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FEBRUARY 20, 1992

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- CACHED DRAM TRIMS ACCESS TO 10 ns
- PC DESIGN SECTION

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1992 ISSCC REVIEW

QUICKLOOK

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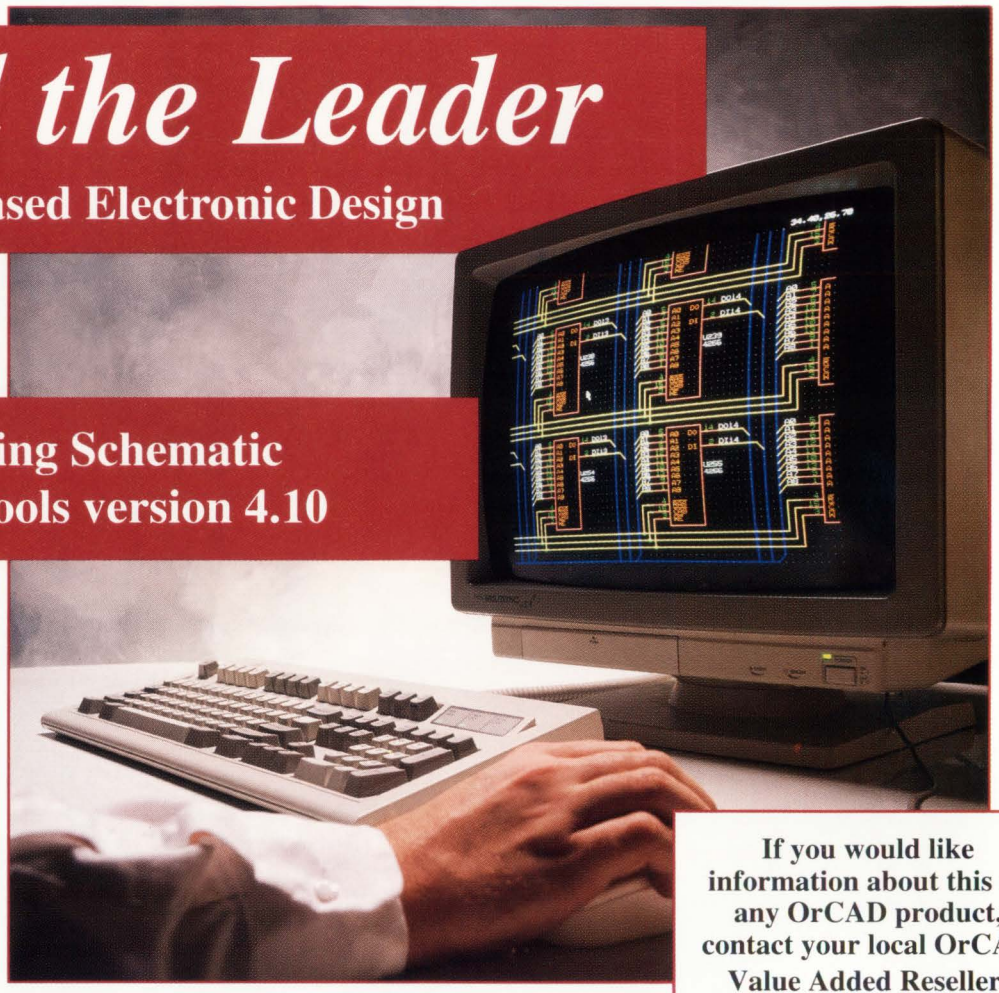
in DOS based Electronic Design



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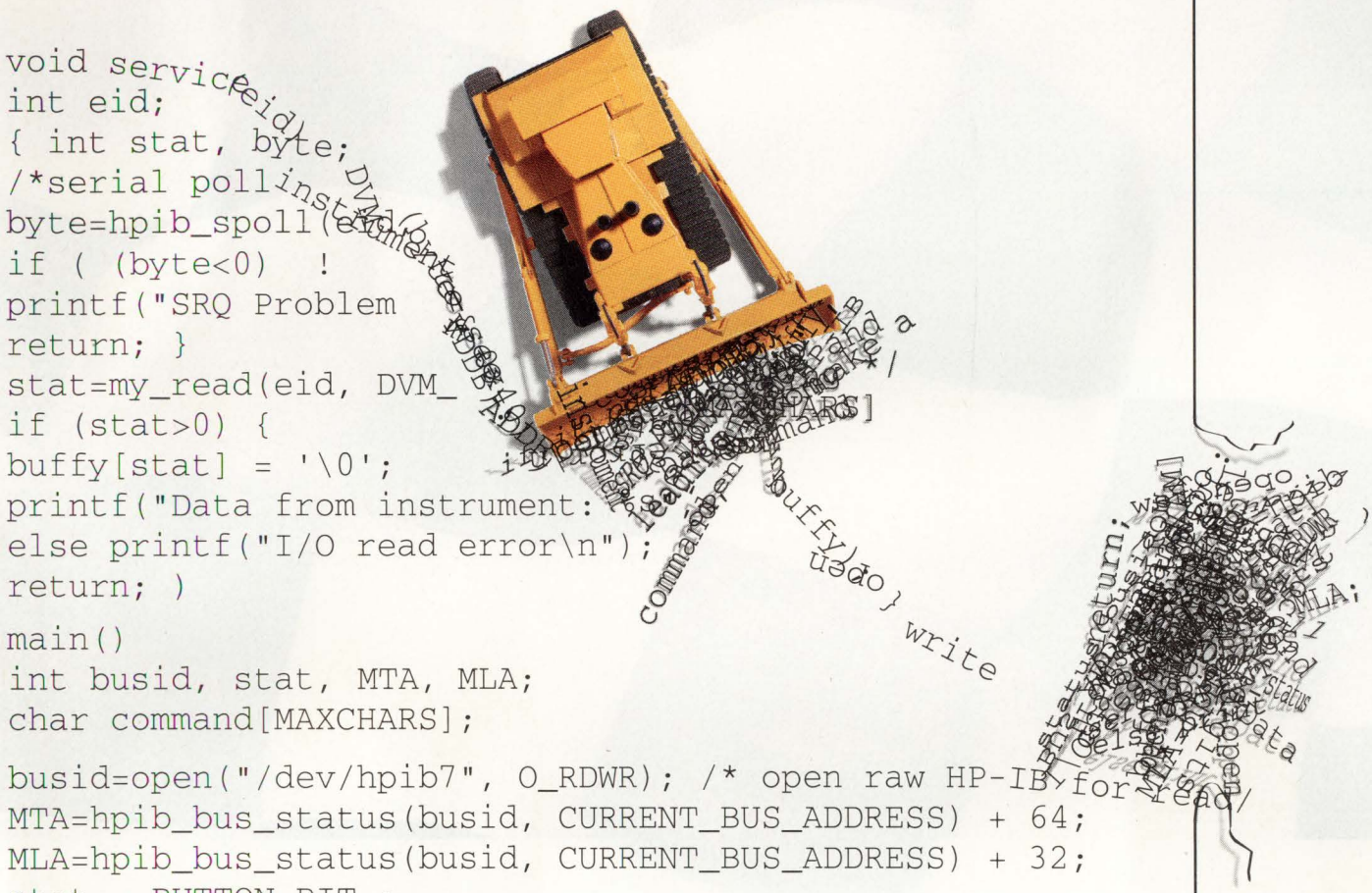
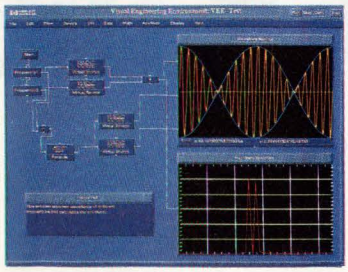


```
void service(eid)
int eid;
{ int stat, byte;
/*serial poll instrument*/
byte=hpib_spoll(eid);
if ( (byte<0)  !
printf("SRQ Problem
return; }
stat=my_read(eid, DVM_
if (stat>0) {
buffy[stat] = '\0';
printf("Data from instrument:
else printf("I/O read error\n");
return; )

main()
int busid, stat, MTA, MLA;
char command[MAXCHARS];

busid=open("/dev/hpib7", O_RDWR); /* open raw HP-IB for
MTA=hpib_bus_status(busid, CURRENT_BUS_ADDRESS) + 64;
MLA=hpib_bus_status(busid, CURRENT_BUS_ADDRESS) + 32;
stat = BUTTON_BIT ;
sprintf(command, "KM%02o", stat); /* 2 octal digits; no
```



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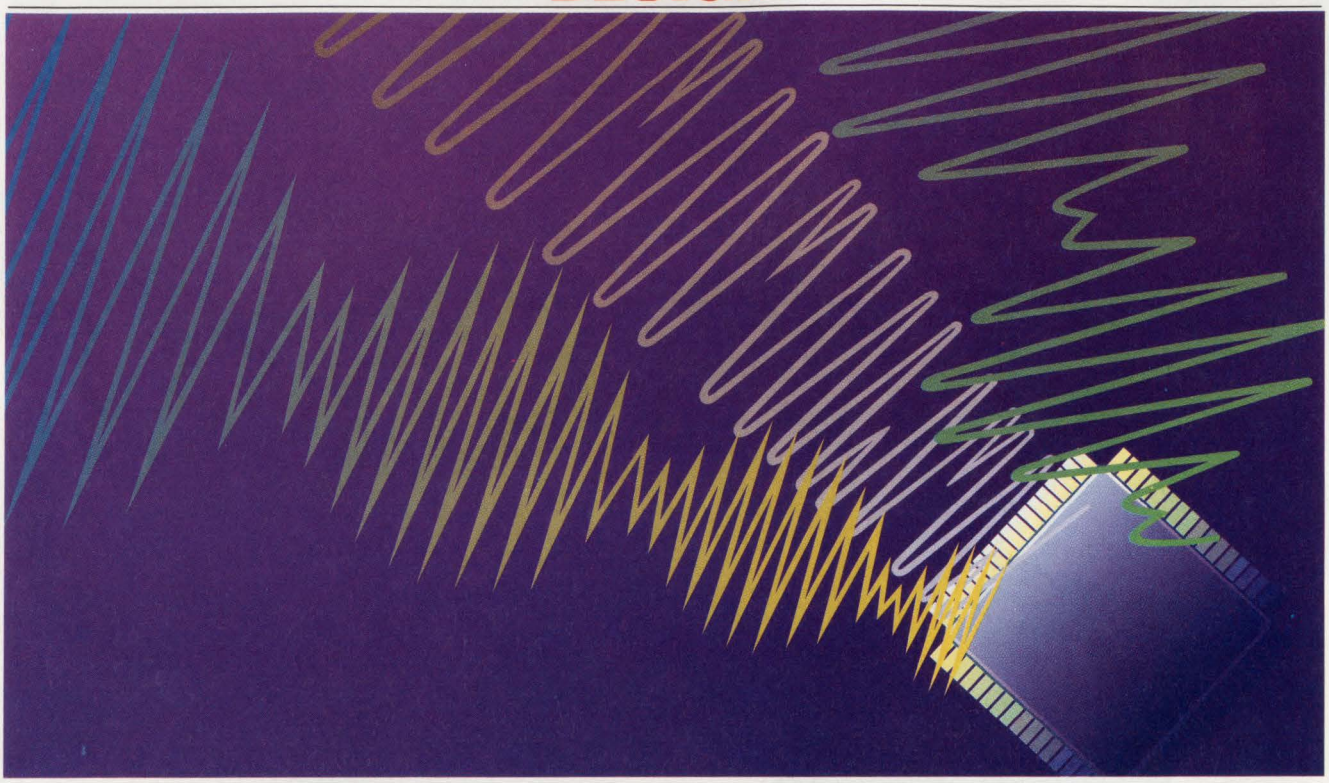

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Cover Illustration: Tony Vitolo

ELECTRONIC DESIGN (USPS 172-080; ISSN 0013-4872) is published semi monthly by Penton Publishing Inc., 1100 Superior Ave., Cleveland, OH 44114-2543. Paid rates for a one year subscription are as follows: $95 U.S., $175 Canada, $255 International. Second-class postage paid at Cleveland, OH, and additional mailing offices. Editorial and advertising addresses: ELECTRONIC DESIGN, 611 Route #46 West, Hasbrouck Heights, NJ 07604. Telephone (201) 393-6060. Facsimile (201) 393-0204.

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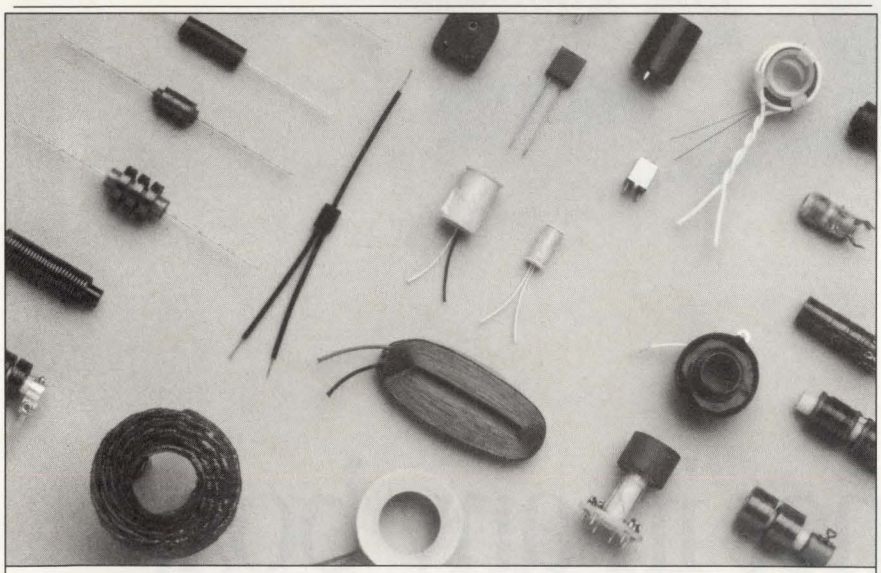

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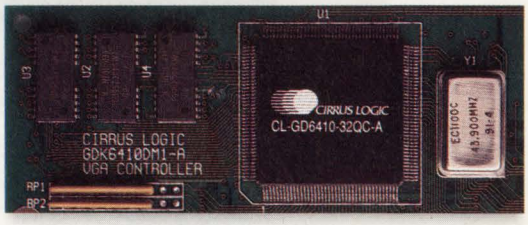

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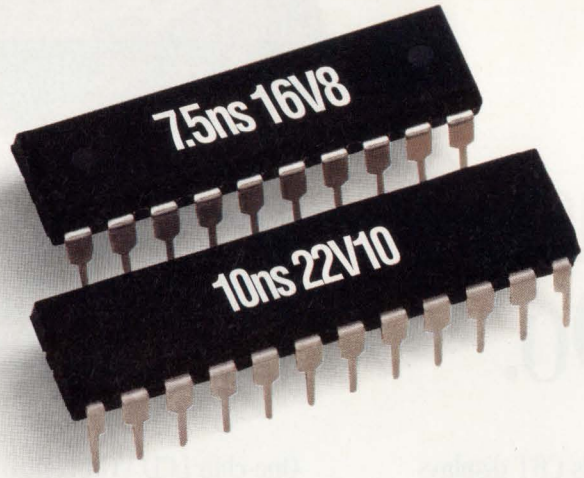

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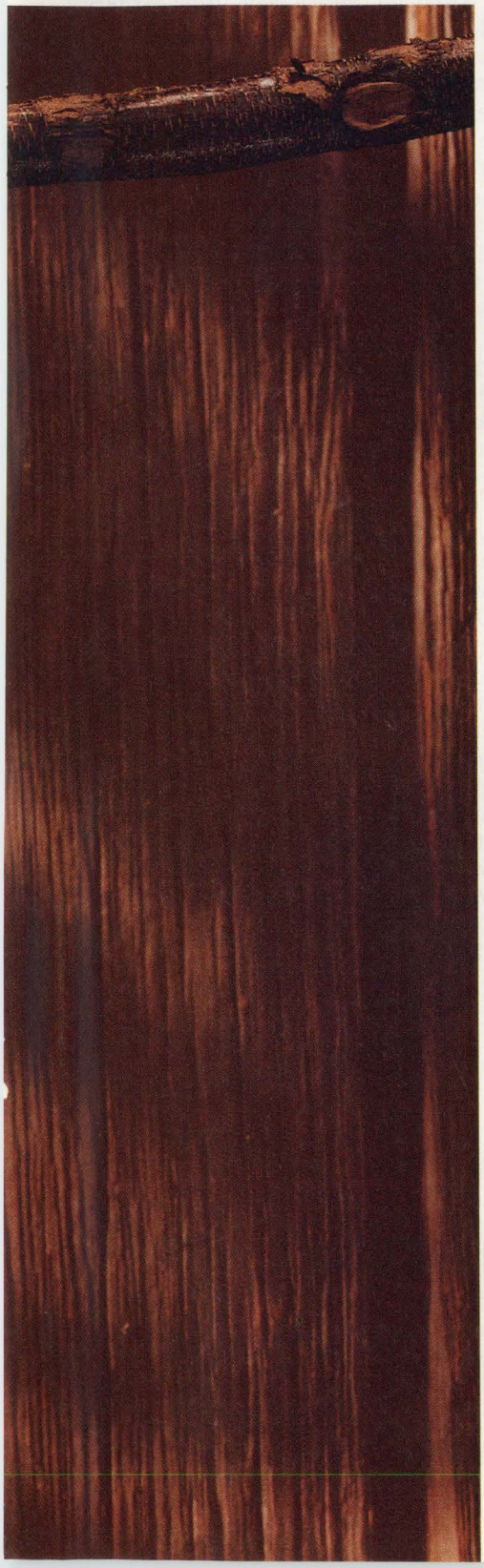

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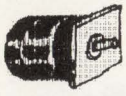

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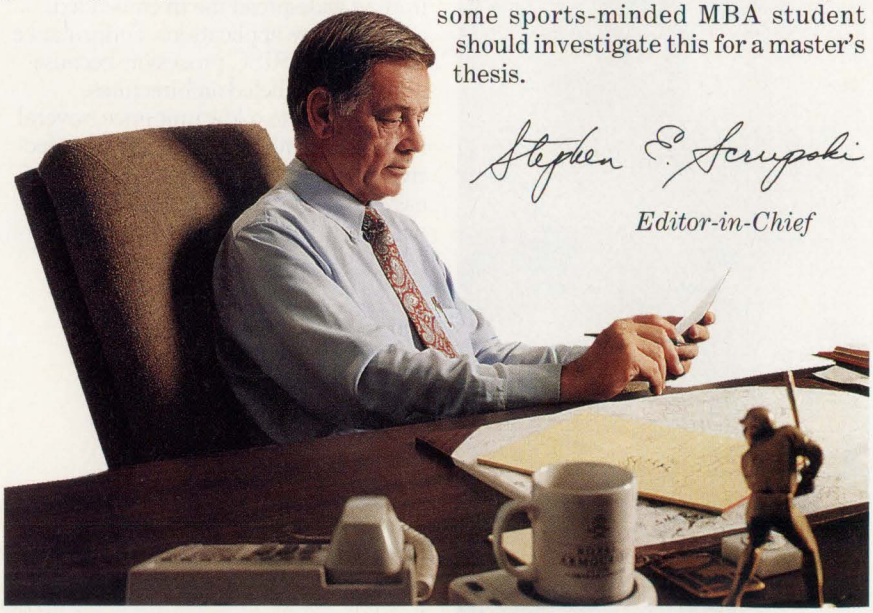
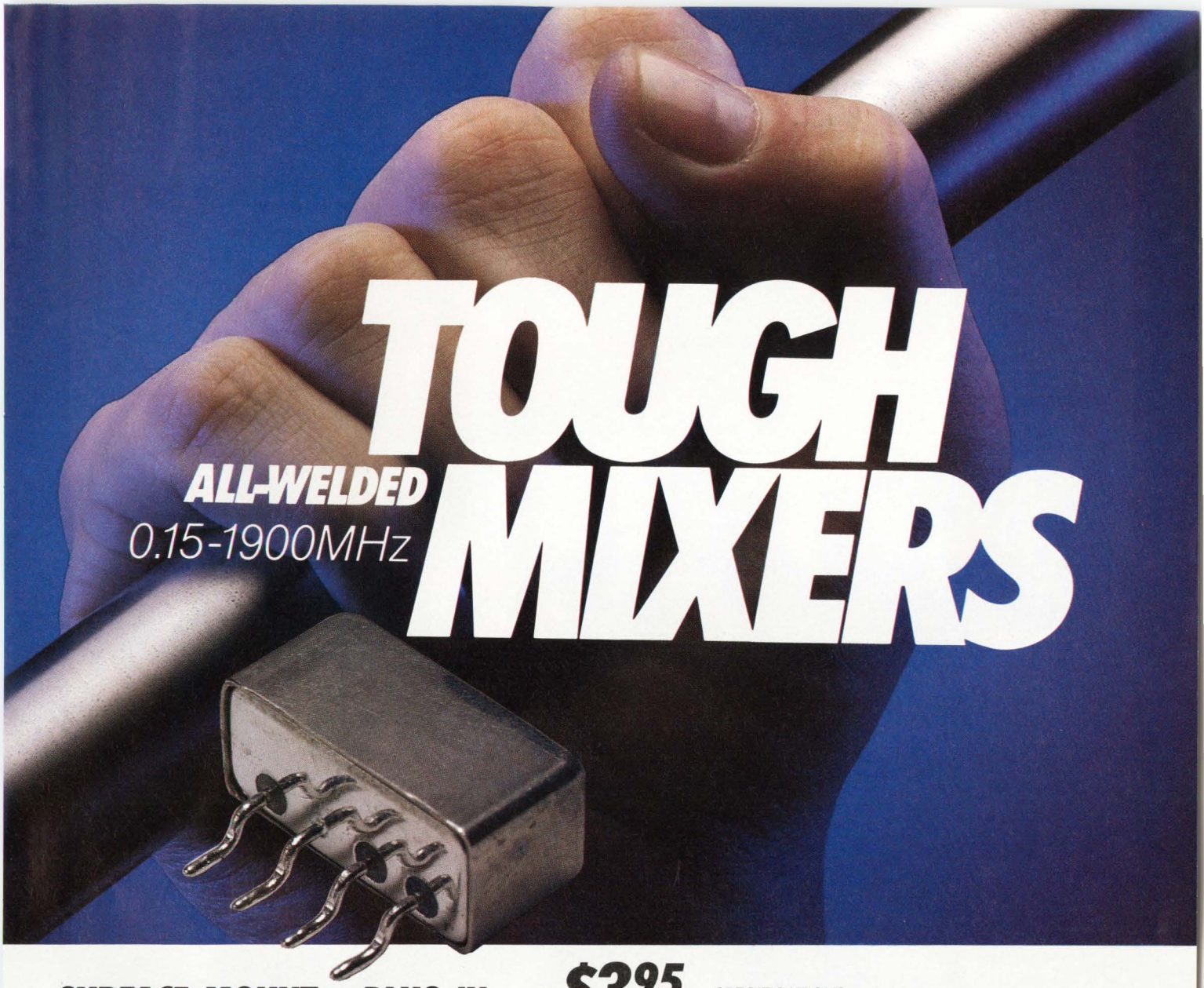
THE MIND TENDS TO DRIFT

Random thoughts while stuck in morning traffic on I-80 in Saddle Brook, N.J., and the only sports news is about player contracts and a few basketball scores....*I hope the Pentagon* realizes that its plan to put prototypes on the shelf until they're needed, and then put them into production, is chancy at best. Although there's been great strides made in smoothing the transition from design to manufacturing with concurrent-engineering schemes, experience shows that you're still never really sure about a product until you can do final testing on production models....*Despite the deep cuts* planned in defense procurement for airplanes, submarines, and other weapons platforms, shouldn't there still be a strong market for upgraded military electronics subsystems? Even if we don't build more airframes, tank bodies, and rocket enclosures, we still must continue to improve communications, guidance, countermeasures, and other subsystems. Electronics technology is advancing at a dizzying pace, and, if the systems were designed properly in the first place, it shouldn't be difficult to retrofit them with the latest technology....*Speaking of today's technology*, isn't it amazing to look back and realize that, in 1969, we landed men on the moon and brought them back using 1960's-vintage guidance and communications systems?....*Japanese politicians* aren't doing any good for Japanese business by characterizing America as Japan's subcontractor, or calling American workers lazy. The next thing you know, they'll claim that U.S. semiconductors and computers, like American cars, are designed only for driving on the right side of the road – that would make as much sense as their earlier statements....*On the other hand*, we must acknowledge the need to revitalize the American educational system. Conversations with U.S. manufacturers reveal that many companies must put employees through the three-R courses to bring them to a productive working level....*Has anyone else* ever noted the fundamental difference in baseball and football philosophies and wondered if there are any links between those philosophies and business management philosophy? In baseball, you play just about every day in a season comprising 162 games. You know games will be lost, so you take a long-range approach and make a series of individual, day-by-day decisions to produce an overall optimum result. In football, you play once a week in a 16-game season, so you take a short-range, must-win attitude for every game. Given the growth of interest in pro football in American business over the past two decades, is this football philosophy reflected in the short-range, quarter-by-quarter planning that prevailed in business throughout the 1970s and 1980s? Maybe some sports-minded MBA student should investigate this for a master's thesis.



Stephen E. Scrupski

Editor-in-Chief



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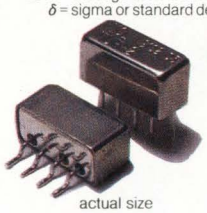
TUF-5 TUF-5SM	20-1500	6.58	0.40	42	8.95
TUF-860 TUF-860SM	860-1050	6.2	0.37	35	8.95
TUF-11A TUF-11ASM	1400-1900	6.83	0.30	33	14.95

■ $\bar{X}$ = average conversion loss at upper end of midband ($f_U/2$)
δ = sigma or standard deviation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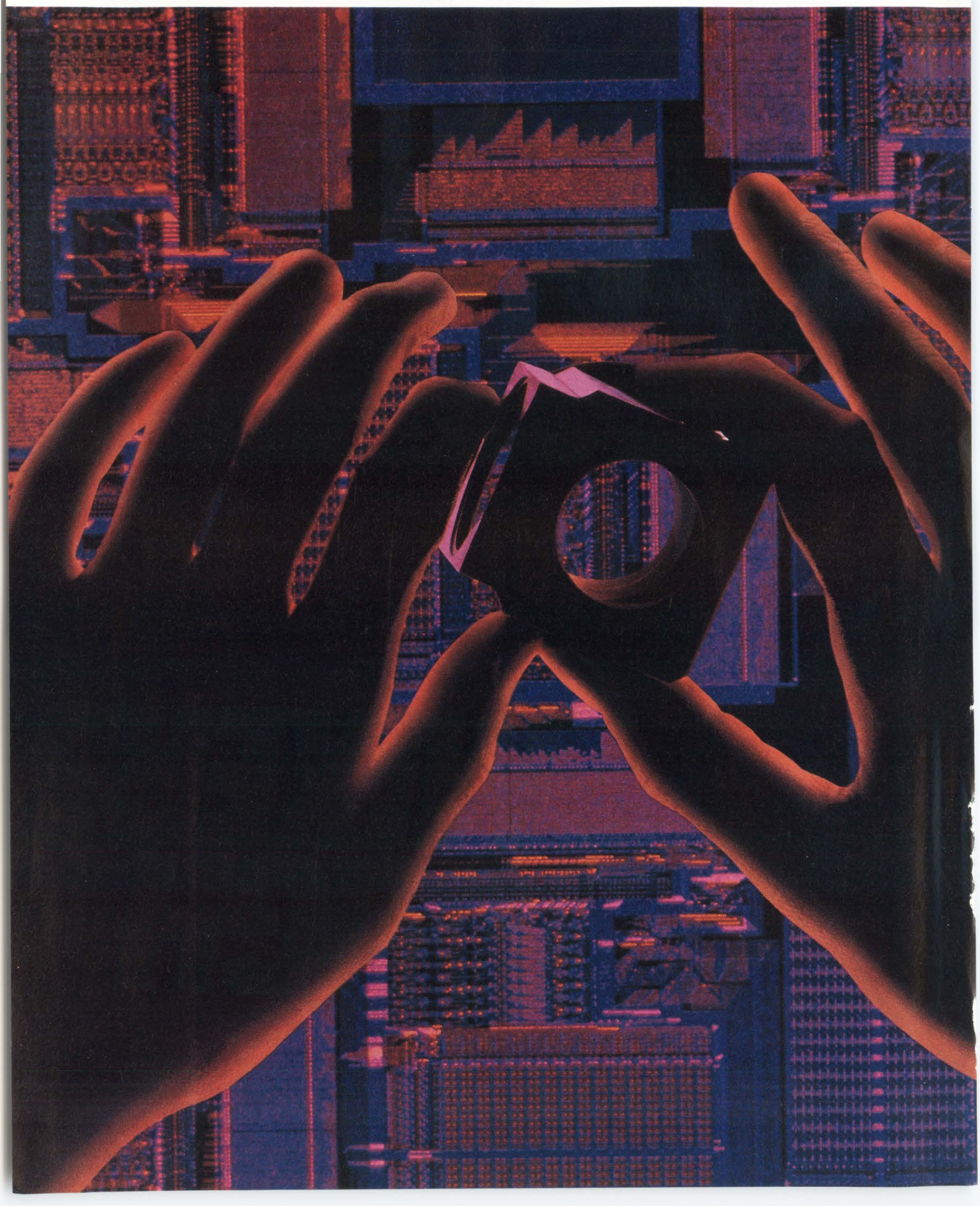
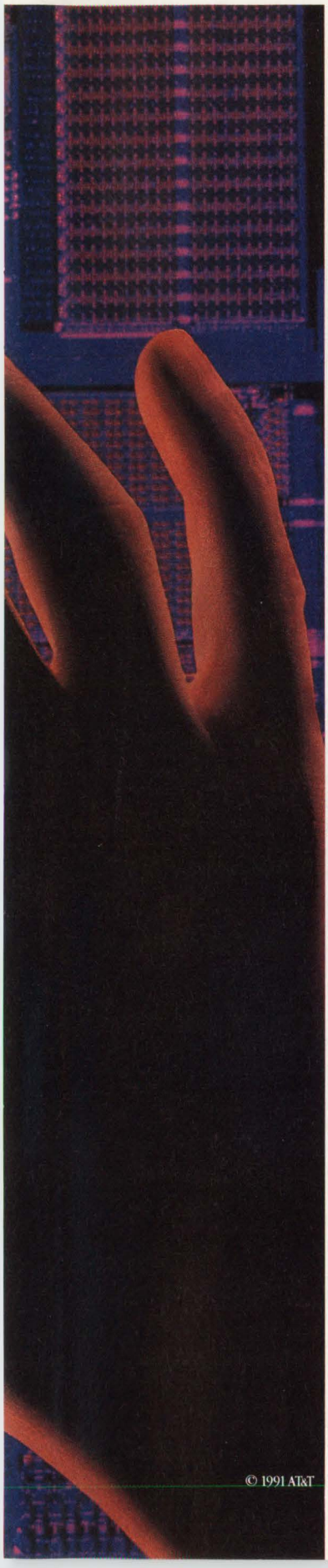


the portable market.



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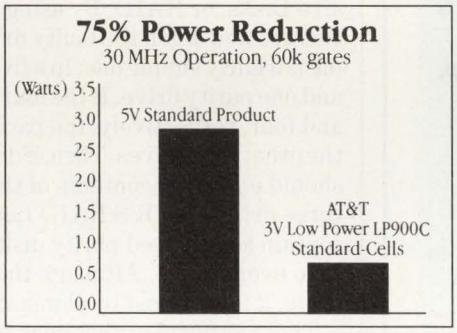

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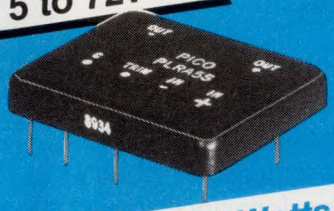

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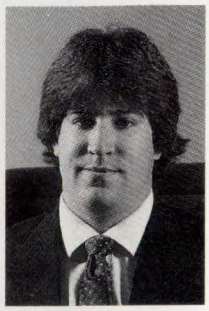


RICHARD NASS
COMPUTER SYSTEMS

With computers weaving their way into all areas of business, the amount of data that requires storage has grown exponentially. In nearly every business, it's essential that archival data be preserved so that it's always accessible and can't be lost. More and more, system designers faced with this problem turn to a disk array – a group of disk drives, which supply hundreds of gigabytes of capacity, that are tied together specifically to recover all data if the disk fails. Disk arrays offer still another benefit: They help increase the disk transfer rates. That's because if two disks in a disk array can be accessed simultaneously, then the access time is theoretically cut in half.

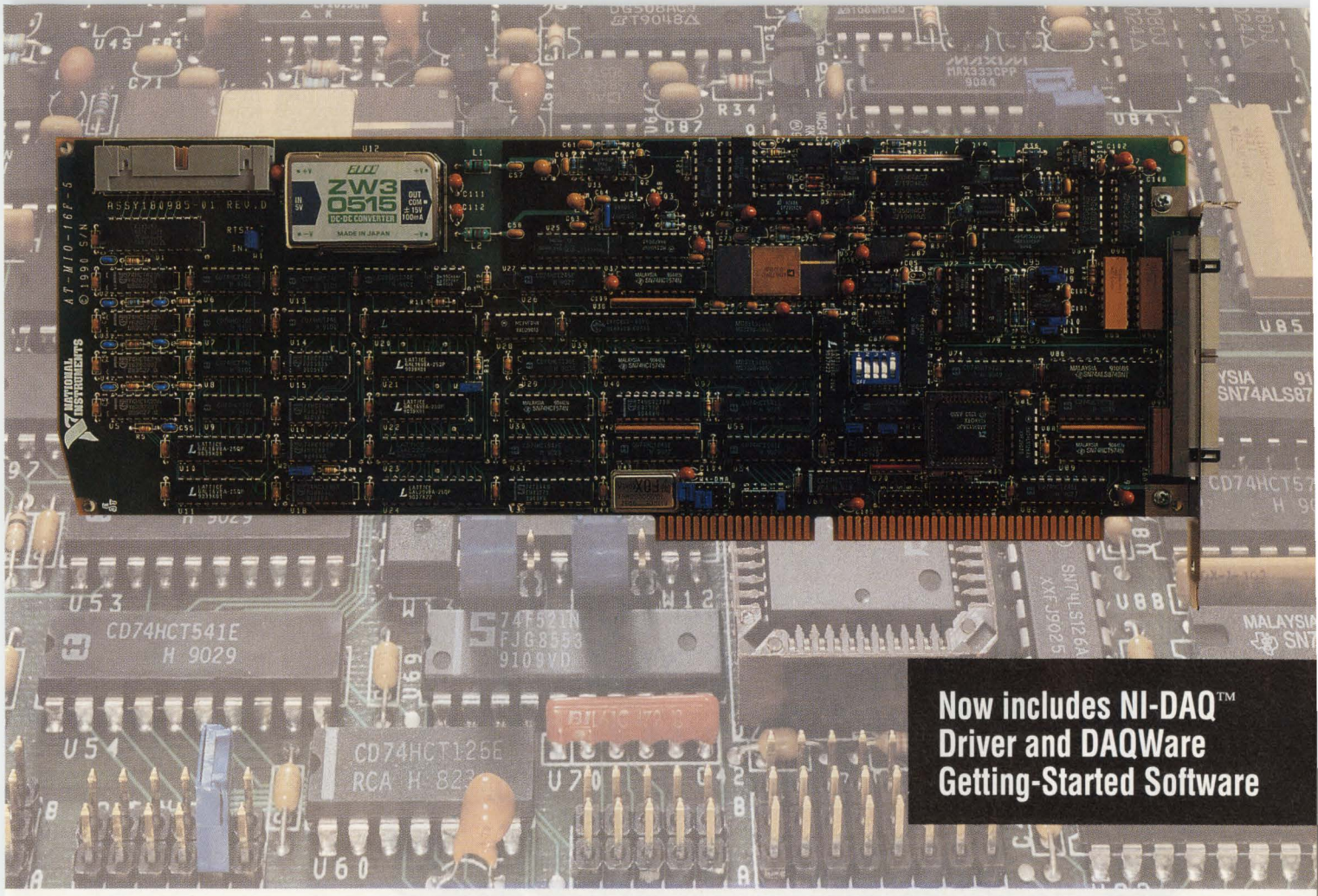
Disk arrays aren't a new technology. Most fault-tolerant systems have employed some type of disk array to prevent any data loss under any circumstance. And, before disk arrays, parallel-transfer drives (PTDs), striping, and mirroring were some of the methods used to reduce the I/O bottleneck between the processor and the disk drive.

PTDs increase the transfer rate by reading and writing from multiple heads simultaneously on one large drive. The transfer rate may increase with this method, but it doesn't address the reliability problem (if the drive fails, it's difficult to recover the data). Striping divides the data into many pieces, than transfers the pieces to multiple drives in parallel. This action may occur in the host software or in the drive controller. Mirroring simply duplicates the data on a second drive. If one drive fails, the same data is on the second drive in its original form. This is expensive because it doubles the hardware requirements.

One recent disk-array architecture was developed by NCR Corp., Fort Collins, Colo., which developed a concept called Redundant Array of Inexpensive Disks, or RAID. By using RAID, data lost due to drive failure can be reconstructed when the faulty drive is replaced. The data-reconstruction principle is a fairly simple one: In a five-drive system, there would be four data drives and one parity drive. If the four data drives contained numbers one, two, three, and four, respectively, the parity drive would contain number ten, the sum of the other four drives. Then, if drive two fails and is replaced, the recovered data should equal the contents of the parity drive minus the contents of the other three drives. NCR'S RAID Level Five, currently being implemented, doesn't contain a dedicated parity disk. Instead, the parity information is spread out onto every drive. Although this method is slightly slower than the dedicated drive, it lowers cost by eliminating one drive.

That methodology has been taken to the next level by the Iceberg disk-array storage subsystem for mainframe, midrange, and network-attached systems. Iceberg, from StorageTek Corp., Louisville, Colo., is based on the company's Extended Storage Architecture (XSA). Ryal Poppa, StorageTek's president and CEO claims, "This technology puts us at least two years ahead of the competition, probably three years." The heart of XSA is a mapping capability that presents an IBM 3990 interface to the host, user, and system programmer. Tables of pointers in the Iceberg controller supply dynamic mapping between the functional configuration that the host system sees and the physical devices that make up the Iceberg subsystem.

Built-in hardware buffers minimize the losses caused by the creation of redundancy data. Because XSA rewrites all updates to a new disk location, redundancy information isn't rewritten, as is the case with conventional disk-array designs. Consequently, XSA eliminates the write-performance penalty associated with updates to conventional disk arrays. Moreover, the parallelism built into XSA helps ensure a real-time response for functional track recovery by allowing virtually all drives in the array to seek, read, or transfer data simultaneously.



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							Channels	Resolution (bits)	Digital I/O Channels	Counter/Timers	LabWindows	NI-DAQ™ DOS	NI-DAQ Windows	Measure	VisionScope	Third Party
EISA-A2000	EISA	4 SE SS	1,000,000	12	±5	1	–	–	–	–	✓	✓	✓		✓	
AT-MIO-16F-5	AT	16 SE 8 DI	200,000	12	±5, 0 to 10	0.5, 1, 2, 5, 10, 20, 50, 100	2	12	8	3	✓	✓	✓			✓
AT-MIO-16H-9 AT-MIO-16H-25	AT	16 SE 8 DI	100,000	12	±10, ±5, 0 to 10	1, 2, 4, 8	2	12	8	3	✓ ✓	✓ ✓	✓ ✓	✓ ✓		✓ ✓
AT-MIO-16L-9 AT-MIO-16L-25	AT	16 SE 8 DI	100,000	12	±10, ±5, 0 to 10	1, 10, 100, 500	2	12	8	3	✓ ✓	✓ ✓	✓ ✓	✓ ✓		✓ ✓
Lab-PC	XT	8 SE	62,500	12	±5, 0 to 10	1, 2, 5, 10, 20, 50, 100	2	12	24	3	✓	✓	✓	✓		✓
PC-LPM-16	XT	16 SE	50,000	12	±5, 0 to 10 ±2.5, 0 to 5	1	–	–	16†	3	✓	✓	✓			
AT-DIO-32F	AT	–	–	–	–	–	–	–	32	–	✓	✓	✓			✓
PC-DIO-96	XT	–	–	–	–	–	–	–	96	–	✓	✓	✓			
PC-DIO-24	XT	–	–	–	–	–	–	–	24	–	✓	✓	✓			✓
PC-TIO-10	XT	–	–	–	–	–	–	–	16	10	✓	✓	✓			

* SE – Single-Ended, DI – Differential, SS – Simultaneous Sampling

† 8 Channels In, 8 Channels Out

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RF TRANS

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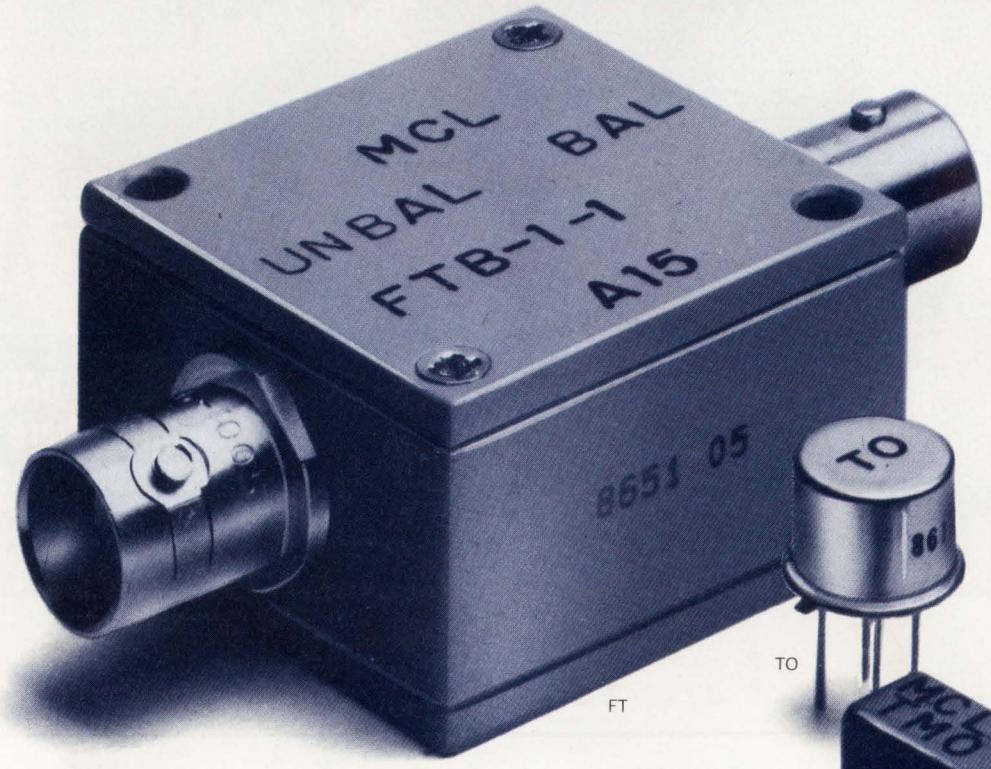
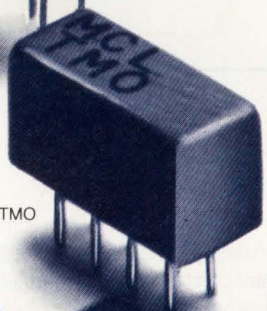
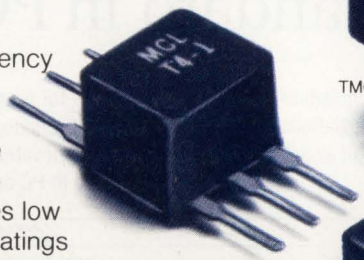


FT

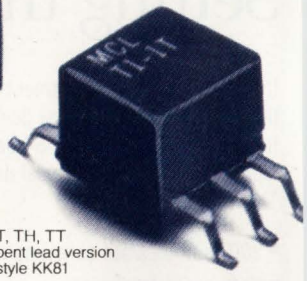
TO



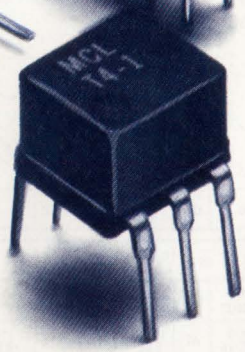
TMO



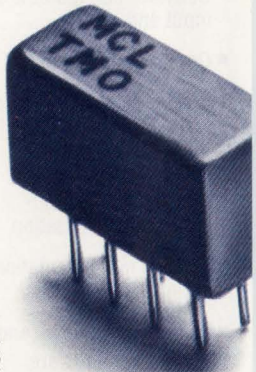
T, TH, TT



T, TH, TT
bent lead version
style KK81



T, TH, TT
bent lead version
style X 65



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TMO, case A 11, † case B 13 FT, FTB, case H 16
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MCL NO.	NSN	MCL NO.	NSN
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FTB1-6	5950-01-225-8773	TMO2.5-6	5950-01-215-4038
T1-1	5950-10-128-3745	TMO2.5-6T	5950-01-215-8697
T1-1T	5950-01-153-0668	TMO3-1T	5950-01-168-7512
T2-1	5950-01-106-1218	TMO4-1	5950-01-067-1012
T3-1T	5950-01-153-0298	TMO4-2	5950-01-091-3553
T4-1	5950-01-024-7626	TMO4-6	5950-01-132-8102
T9-1	5950-01-105-8153	TMO5-1T	5950-01-183-0779
T16-1	5950-01-094-7439	TMO9-1	5950-01-141-0174
TMO1-1	5950-01-178-2612	TMO16-1	5950-01-138-4593

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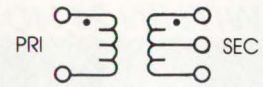
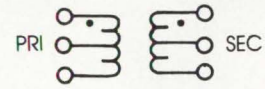
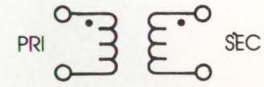
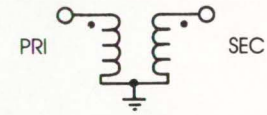
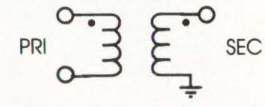
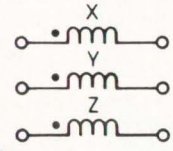
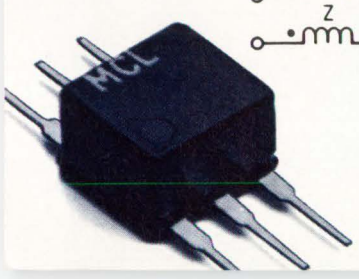
case style number see opposite page		MODEL NO.	Ω RATIO	FREQUENCY MHz	INSERTION LOSS 3dB MHz	INSERTION LOSS 2dB MHz	INSERTION LOSS 1dB MHz	PRICE $ Qty. (1-9)
A* 	T	T1-1T	1	.05-200	.05-200	.08-150	.2-80	4.45
		T1-6T	1	.003-300	.003-300	.01-150	.02-50	6.95
		T2-1T	2	.07-200	.07-200	.1-100	.5-50	4.95
		T2.5-6T	2.5	.01-100	.01-100	.02-50	.50-20	4.95
		T3-1T	3	.05-250	.05-200	.1-200	.5-70	4.95
		T4-1	4	.2-350	.2-350	.35-300	2-100	3.25
		T4-6T	4	.02-250	.02-250	.05-150	0.1-100	4.45
		T5-1T	5	.3-300	.3-300	.6-200	.5-100	4.95
		T8-1T	8	.03-140	.03-140	.10-90	1-60	7.95
		T13-1T	13	.3-120	.3-120	.7-80	5-20	4.95
		T16-6T	16	.03-75	.03-75	.06-30	.1-20	5.65
	TH	T4-1H	4	10-350	10-350	15-300	25-200	5.95
	TMO	TMO1-1T	1	05-200	.05-200	.08-150	.2-80	7.95
		TMO2-1T	2	.07-200	.07-200	.1-100	.5-50	8.45
		†TMO2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	8.45
		†TMO3-1T	3	.05-250	.05-250	.1-200	.5-70	7.95
		TMO4-1	4	.2-350	.2-350	.35-300	2-100	6.25
		TMO5-1T	5	.3-300	.3-300	.6-200	5-100	8.45
		TMO13-1T	13	.3-120	.3-120	.7-80	5-20	8.45
B* 	TT	TT1-6	1	.004-500	.004-500	.02-200	.1-50	6.95
		TT1.5-1	1.5	.075-500	.075-500	.2-100	1-50	5.95
		TT2.5-6	2.5	.01-50	.01-50	.025-25	.05-10	6.45
		TT4-1	3	.05-200	.2-50	.2-50	1-30	5.95
		TT4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	6.95
		TT25-1	25	.02-30	.02-30	.05-20	.1-10	9.95
	TTMO	TTMO25-1	25	.02-30	.02-30	.05-20	.1-10	11.95
		TTMO1-1	1	.005-100	.005-100	.01-75	.05-40	11.45
		TTMO4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	13.95
C 	T	T1-1	1	.15-400	.15-400	.35-200	2-50	3.25
		T1.18-3	1.18	0.01-250	0.01-250	0.02-200	0.03-50	5.65
		T1-6	1	.01-150	.01-150	.02-100	.05-50	5.65
		T1.5-1	1.5	.1-300	.1-300	.2-150	.5-80	4.45
		T1.5-6	1.5	.02-100	.02-100	.05-50	0.1-25	5.65
		T2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	4.45
		T4-6	4	.02-200	.02-200	.05-150	.1-100	4.45
		T9-1	9	.15-200	.15-200	.3-150	2-40	3.95
		T16-1	16	.3-120	.3-120	.7-80	5-20	4.45
		T36-1	36	.03-20	.03-20	.05-10	.1-5	6.95
	TO	TO-75	1	10-500	—	10-500	40-250	6.95
	TH	T1-1H	1	8-300	8-300	10-200	25-100	5.95
		T9-1H	9	2-90	2-90	3-75	6-50	6.45
		T16-H	16	7-85	7-85	10-65	15-40	6.45
	TMO	TMO1-02	1	1-800	1-800	2-500	—	9.45
		TMO1-1	1	.15-400	.15-400	.35-200	2-50	6.25
		TMO1.5-1	1.5	.1-300	.1-300	.2-150	.5-8	8.45
		†TMO2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	7.95
		†TMO4-6	4	.02-200	.02-200	.05-150	.1-100	7.95
		TMO6-1	6	.3-200	.3-200	.5-150	5-50	7.95
		TMO9-1	9	.15-200	.15-200	.3-150	2-40	7.95
		TMO16-1	16	.3-120	.3-120	.7-80	5-20	7.95
D 	T	T2-1	2	.050-600	.050-600	.1-400	.5-200	3.95
		T3-1	3	.5-800	.5-800	2-400	—	4.45
		T4-2	4	.2-600	.2-600	.5-500	2-250	3.95
		T8-1	8	.15-250	.15-250	.25-200	2-100	3.95
		T14-1	14	.2-150	.2-150	.5-100	2-50	4.95
	TMO	TMO2-1	2	.050-600	.050-600	.1-400	.5-200	7.95
		TMO3-1	3	.5-800	.5-800	2-400	—	8.45
		TMO4-2	4	.2-600	.2-600	.5-500	2-250	7.95
		TMO8-1	8	.15-250	.15-250	.25-200	2-100	7.95
		TMO14-1	14	.2-150	.2-150	.5-100	2-50	8.45
	FT	FT1.22-1	1.22	.005-100	.005-100	.01-50	.05-25	35.95
		FT1.5-1	1.5	.1-400	.1-400	5-200	1-100	35.95
E 	FTB	FTB-1	1	.2-500	.2-500	.5-300	1-100	36.95
		FTB1-6	1	.01-125	.01-125	.05-50	.1-25	36.95
		■FTB-1-75	1	.5-500	.5-500	5-300	10-100	36.95
F 	T	T-622	1	0.1-200	0.1-200	0.5-100	5-80	3.25
		T626	1	0.01-10	0.01-10	0.2-5	.04-2	3.95



■ Denotes 75 ohm models

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FIDUCIAL-MARK STANDARD SMOOTHES SMD PLACEMENT

A major step in the standardization of surface-mounted assembly processing has occurred in the form of a fiducial-mark standard. The Surface Mount Equipment Manufacturers Association (SMEMA), Lafayette Hill, Pa., has issued its document 3.1 on the subject, which provides common measurable points for all steps in the pc-board assembly process. Compliance with the standard's requirements will allow each piece of equipment used for surface-mount-technology assembly to accurately locate component land patterns. Topics covered in the standard include global and local fiducials, fiducial-mark design, clearances, base materials, and more. Contact Judith Ginsberg at (215) 825-1008 for a copy of the document. *DM*

FIRST ALTERNATIVE TO 486 COMING FROM AMD

Although the 80486 microprocessor family has been sole-sourced since its inception by Intel Corp., Santa Clara, Calif., the first alternative to the family, the Am486 series, has now been developed by Advanced Micro Devices Inc., Sunnyvale, Calif. As with its 386-compatible family, AMD's designers created direct replacements for Intel's microprocessors that rely on the same microcode as in the Intel original chips. (The use of Intel's microcode continues to be the subject of a major lawsuit between the two companies. Intel claims that AMD has no rights to use the code, while AMD claims it does based on an earlier licensing accord that allowed them to copy most Intel microcode in x86 family members.)

Like the 386-compatible chips, the forthcoming Am486 chips with 25-, 33-, and 50-MHz versions use fully-static CMOS logic. Thus, the clock can be stopped or slowed to any speed to minimize power consumption during low-activity periods. The triple-level-metal 0.7-μm process used to build the Am486 series keeps the chips performance-competitive and their sizes cost-effective. Low-voltage versions, which can run from 3.3-V supplies, will also be available as an option. The 486DX chips come in pin-grid-array packages. A 25-MHz 486SX version will be offered in either PGA or plastic surface-mountable packages. CPU samples are expected in the mid-to-late third quarter, with production slated for the late fourth quarter. Low-voltage Am486DXLV processor samples will be released in the fourth quarter of this year. Coupled with the release of the Am486 family is a 33-MHz version of the 386 SX/SXL and a 40-MHz version of the Am386DX/DXL that's housed in a space-saving 132-lead plastic surface-mountable package. In 1000-unit lots, the 386SX-33 sells for $76 each, and the 386DX-40 sells for $114 each. Prices for the Am486 family will be released this summer. For more information, contact AMD at (408) 732-2400. *DB*

MODULATION ANALYSIS IS POSSIBLE AT OVER 5 GHZ

A new instrument can now provide precise modulation analysis up to 5.2 GHz, the first time that analysis at this high range is possible. With more new radio services using the range above 1.36 GHz, analysis in this frequency range is becoming increasingly more important due to congested classic frequency bands. The FMB modulation analyzer, created by Rohde & Schwarz, Munich, Germany, combines all features and universal measurement capabilities of its FAM (50 kHz to 1.36 GHz) and FMAB (for FM sound broadcasting) forerunners, such as accuracy, dynamic range, broadband characteristics, and versatile measurement function—all up to 5.2 GHz. The FMB's applications above 1.36 GHz include special outside-broadcast links, 2.7-GHz radio links, and testing and calibration of microwave generators. Due to its versatility, the FMB can also be used as an RF counter, power meter, voltmeter, and distortion meter. Its negligible residual FM of less than 2 Hz (up to 2.72 GHz) and 4 Hz (up to 5.2 GHz), as well as its residual AM of less than 0.02%, ensure precise measurements even at higher carrier frequencies. *JG*

IC FM RECEIVERS TARGET LOW-POWER SYSTEMS

Equipment designers can drastically cut size and power consumption of portable communication systems, such as wireless LANs and cellular and cordless telephones, with two single-chip FM receiver ICs developed by Philips Semiconductors, Eindhoven, the Netherlands. The company claims that its NE606 and NE607 are the industry's most advanced single-chip solutions for FM mixer-IF systems. The ICs, which typically hold off-chip components, reduce pc-board area by as much as 15%, cut current drain from 5.8 to 3.4 mA, and lower supply voltages from 5 to 3 V. In addition, their shrink-small-outline package, or SSOP (the SSOP is the world's smallest commercial 20-pin package), is only one-third the size of a conventional receiver IC in a small-outline-large package (SOLP). Each IC has a mixer/oscillator, dual op amps, IF amplifiers, a limiter amplifier, a voltage regulator, and a quadrature detector. An on-chip logarithmic receiver-signal-strength indicator can be configured as a feedback network to check incoming signal strength and adjust

You Design Actel FP
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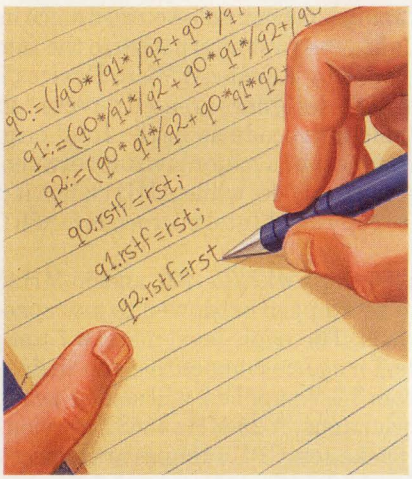
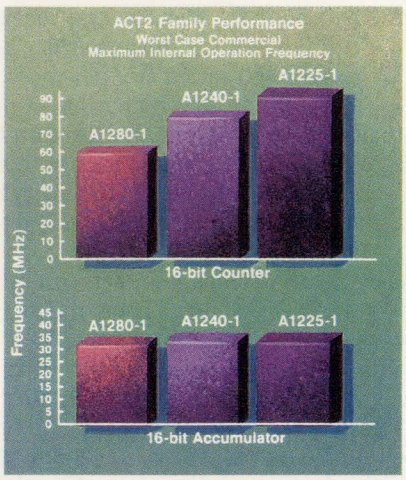


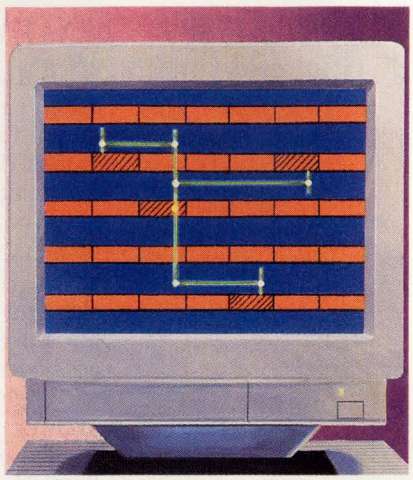
Use PLD Tools.

You design Actel FPGAs using the same tools as you would a PLD: ABEL,™ CUPL,™ LOG/iC™ and PGADesigner.™ But that's where the similarity ends.



Fast. Fast. Fast.

Our FPGAs are real speed demons. Whatever application you may be working on, our parts will give you the kind of performance you're looking for.



100% Automatic Place And Route.

Coupled with your PLD tools, Actel's Action Logic™ System (ALS) software lets you create your own FPGAs—using a 386 PC or workstation—right at your own desk. With Auto Place and Route that's proven in thousands of applications.

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If you're a PLD designer with an interest in fast, flexible FPGAs, but you think you don't have time to learn new design techniques, we'd like to change your mind.

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Actel devices offer everything you want in an FPGA. Like high I/O and flip-flop counts. And 100% automatic place and route gets you to market fast.

Once your FPGA is designed, our Action Logic™ System (ALS) converts the captured design into a completed device in minutes. To give you true, high-density, field-programmable, channeled gate arrays.

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It's never been easier to make your innovative designs a reality. We offer you a complete family of powerful FPGAs, like the A1010 and A1020, available in 44, 68 and 84 pin PLCC versions and implementing up to 273 flip-flops or up to 546 latches. And the first member of our ACT 2 family, the power-

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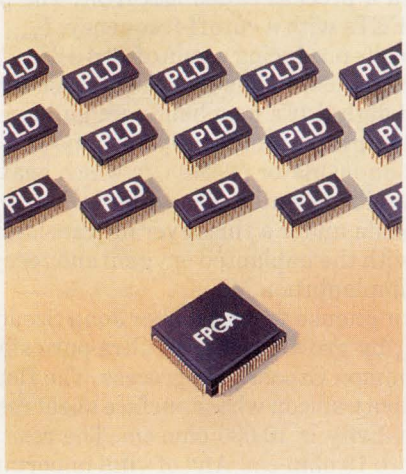
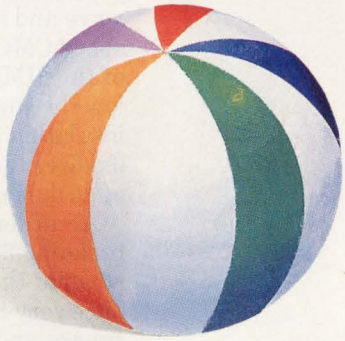


Small Footprint.

Actel FPGAs give you far more gates per square inch. As much as ten times as many as the densest PLDs. That can save a lot of real estate.



More Fun.

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ful A1280. With 8,000 gates, up to 998 flip-flops, and 140 I/O pins, it's the highest capacity FPGA today. And our A1240-1 is the fastest. In the A1240-1, 16-bit counters run at 75 MHz, 16-bit accumulators at 33 MHz. Enough capacity and speed to handle almost any application.

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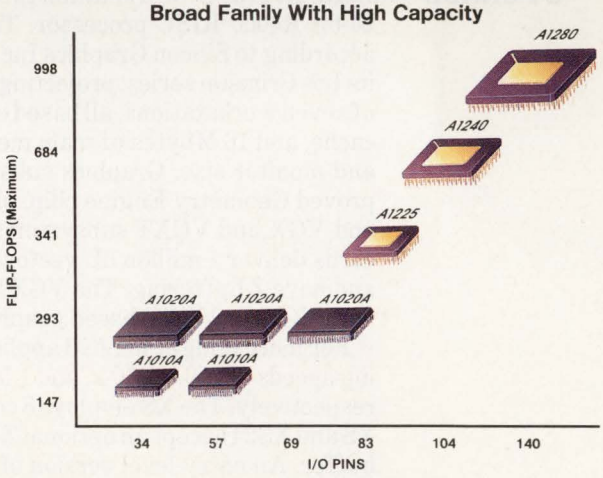

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transmit power accordingly to ensure reliable communications. The 607 also includes an automatic-frequency-control pin to stabilize the IF in narrow-band applications. Production quantities of the NE606 and NE607 are available in SSOPs, DIPs, and SOLPs. Prices depend on the importing country. *JG*

SILICON PROCESS YIELDS 30-GHz MOSFETs

ICs built with gallium-arsenide MESFETs offering frequencies of 30 GHz are almost routine these days. And development groups are releasing reports of silicon bipolar transistors with similar performance. Now, a team of researchers at the Westinghouse Science and Technology Center, Pittsburgh, Pa., has gone one step further with a process called MICROX. The process makes it possible to build n-channel silicon MOSFETs with a cutoff frequency, f_{max}, of 30 GHz. The f_{max} of the p-channel FETs runs 15 GHz. While producing a gain of 13.4 dB at 2 GHz, the transistors achieved a noise figure of 3 dB. Westinghouse claims that the process significantly reduces the cost of microwave and high-speed digital ICs now built with gallium arsenide, and makes practical ECL-speed CMOS logic, though at significantly lower power. MICROX is a Westinghouse version of the SIMOX silicon-on-insulator process, in which heavy doses of oxygen are implanted below the surface of the silicon wafer. The wafer is then annealed at 1300°C, forming a layer of insulating silicon dioxide under a thin layer of transistor-quality silicon. The annealing both oxidizes the silicon (with the implanted oxygen) and recrystallizes any crystal structure damaged during oxygen implantation.

According to Westinghouse team member John Szedon, the company achieved its record-breaking 30-GHz f_{max} by growing its own ultra-pure silicon, using float-zone technology instead of the more common Czochralski process. The float-zone process was modified to produce very-high resistivity silicon whose surface sheet resistance runs greater than 10^5 ohms/square and bulk resistivity is 10,000 ohm-cm. The resistivity of typical silicon wafers runs 1000-fold lower, a mere 10 ohm-cm. And of vital importance, the MICROX silicon maintained this abnormally high resistivity after six hours of annealing at 1300°C (earlier attempts also started with high resistivity, 5000-ohm-cm silicon). The high substrate resistivity is key to minimizing the effects of frequency-response-limiting parasitic resistance and capacitance, and also makes possible the low-loss (0.07-dB/cm) microstrip interconnects. The oxide layer and high-resistance silicon are comparable to the semi-insulating properties of the GaAs substrates used for monolithic microwave ICs. MICROX transistor geometries are based on those of similar GaAs MESFETs, and feature 100-μm widths and short (0.2- to 0.5-μm) electron-beam-defined gates. All other patterns were defined with optical lithography. *FG*

NEW CPU, GRAPHICS ICs UPGRADE WORKSTATIONS

A family of desktop systems that can deliver SPECmark throughputs of over 70 MIPS when running at 50 MHz is claimed to be the first 3D-graphics workstation group to employ the expandable, secondary-cache version of the 64-bit R4000 RISC processor. That throughput is even higher than originally anticipated, according to Silicon Graphics Inc., Mountain View, Calif. Initially, the company had simulated its Iris Crimson series, projecting the throughput at about 60 SPECmarks. The family consists of seven workstations, all based on CPU cards that employ the R4000SC, 1 Mbyte of secondary cache, and 16 Mbytes of main memory. The systems vary in graphics performance, features, and monitor size. Graphics subsystems include four budget-priced options based on an improved Geometry Engine chip, plus other new custom circuits. The company's existing high-end VGX and VGXT subsystems can also be used with the new CPU. The VGX and VGXT cards deliver 1 million 3D vectors/s and 180,000 3D quadrilaterals/s; employ 64 color planes; and have Z buffering. The VGXT version also supports textured surfaces. Crimson systems with VGX- or VGXT-based graphics systems sell for $69,900 and $99,900, respectively.

For more budget-minded applications, the XS, XS24, and Elan graphics options offer drawing speeds of 250-k, 250-k, and 1-M 3D vectors/s, and 25-k, 25-k, and 225-k 3D-quadrilaterals/s, respectively. The XS employs 8 color planes, while the XS24 and Elan have 24 planes. Both the XS and XS24 accept an optional Z-buffer expansion module, while the Elan card has a built-in Z buffer. An entry-level version of the Crimson system includes an 8-plane display subsystem that draws 231-k 3D vectors/s, but just 6.6-k 3D quadrilaterals/s. Prices range from $29,900 for the entry-level version with a 16-in. 1024-by-768-pixel color monitor, to $42,900 for the Elan, which includes a 1280-by-1024-pixel, 19-in. monitor. A server version without the graphics sells for $27,900. The XS, XS24, and Elan options can also be added to the company's Iris Indigo family to enhance the graphics of the price-conscious 3D workstations. Contact Silicon Graphics at (415) 960-1980. *DB*

THINK OF ADDING EIGHT NEW NSP PLAYERS TO YOUR TEAM!

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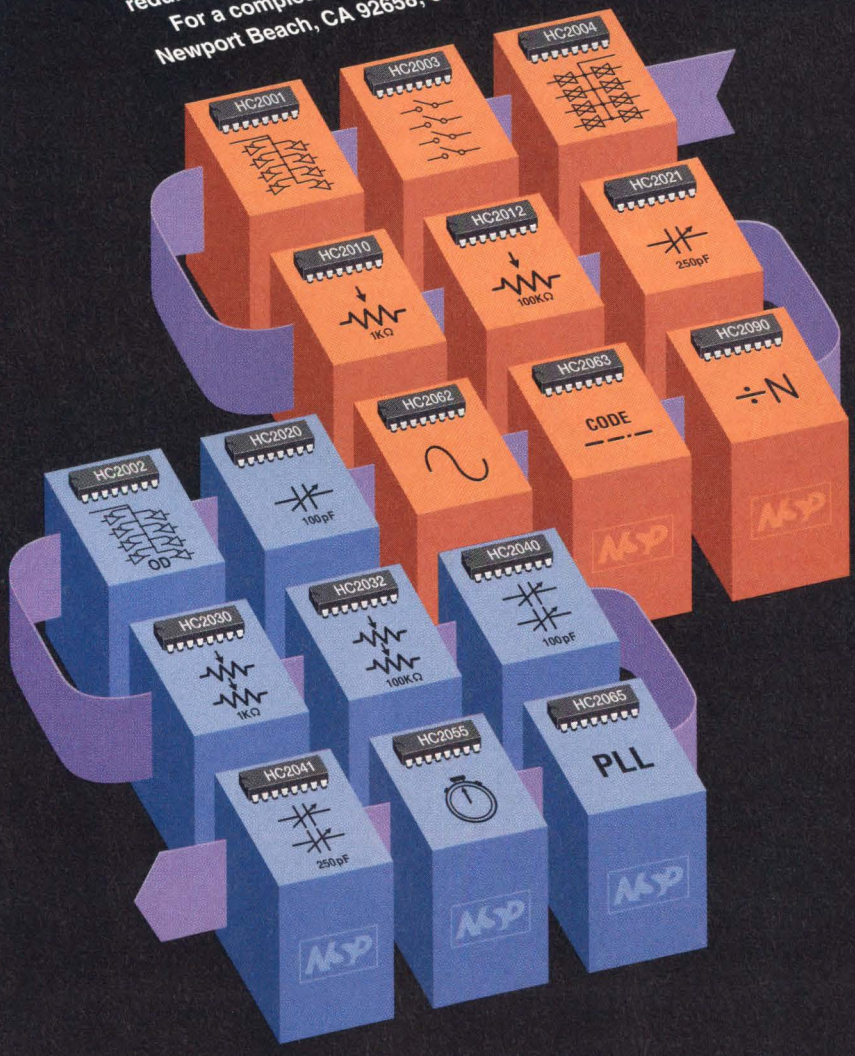
Last year the Semiconductor Products Center of Hughes Aircraft Company announced "a whole new ballgame" with an initial lineup of nine multitalented NSP players. (Remember, these are the Nonvolatile Serially Programmable ICs that can work together in any order, won't forget their plays and can take new instructions anytime from homeplate.)

Hughes NSP devices presented so much potential that over 7,000 circuit designers asked for more specific data. No wonder our IC engineers are so enthusiastic about fielding another eight new NSP players...with even more to come.

These new NSP devices provide a greater variety of functions and extend the capabilities of existing NSP models. They feature micro power, wide operating voltage range, common serial interface, wide temperature range and single power supply. Also, each device has a nonvolatile memory with redundant memory elements to insure reliable storage of settings while power is removed.

For a complete information packet, contact Hughes Semiconductor Products Center, P.O. Box H, Newport Beach, CA 92658; or call the NSP Hotline Number (714) 759-6589 or FAX to (714) 759-2913.



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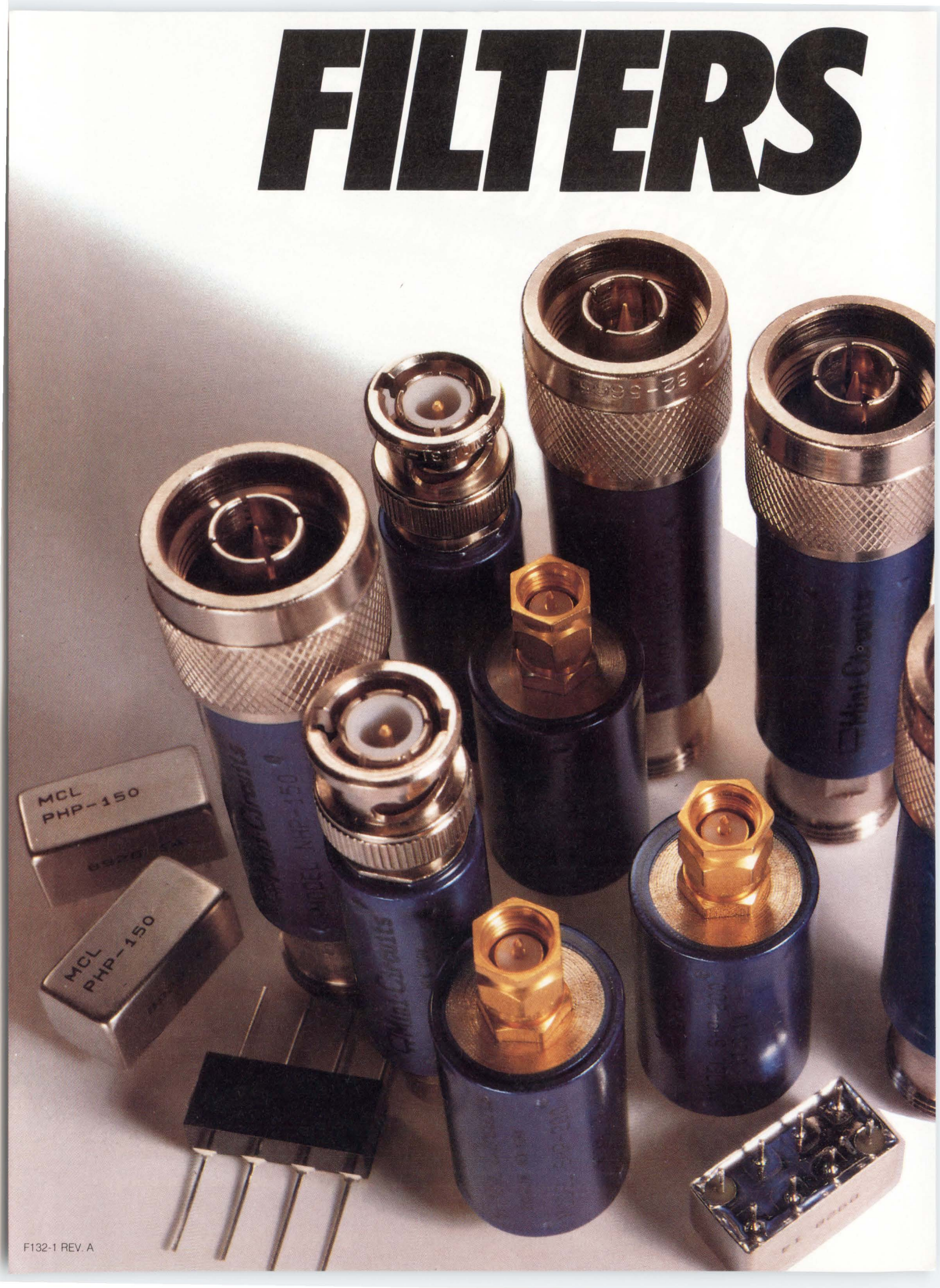
CIRCLE 113 FOR RESPONSE OUTSIDE THE U.S.

FILTERS



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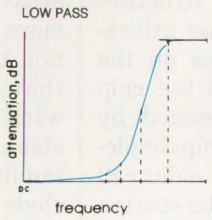


Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	loss > 40dB	Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	loss > 40dB
PLP-5	DC-5	8-10	10-200	PLP-250	DC-225	320-400	400-1200
PLP-10.7	DC-11	19-24	24-200	PLP-300	DC-270	410-550	550-1200
PLP-21.4	DC-22	32-41	41-200	PLP-450	DC-400	580-750	750-1800
PLP-30	DC-32	47-61	61-200	PLP-550	DC-520	750-920	920-2000
PLP-50	DC-48	70-90	90-200	PLP-600	DC-680	840-1120	1120-2000
PLP-70	DC-60	90-117	117-300	PLP-750	DC-700	1000-1300	1300-2000
PLP-90	DC-81	121-137	167-400	PLP-800	DC-720	1080-1400	1400-2000
PLP-100	DC-98	146-189	189-400	PLP-850	DC-760	1100-1400	1400-2000
PLP-150	DC-140	210-300	300-600	PLP-1000	DC-900	1340-1750	1750-2000
PLP-200	DC-190	290-390	390-800	PLP-1200	DC-1000	1620-2100	2100-2500

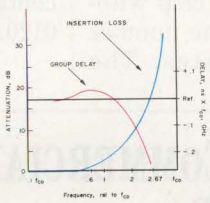
Price, (1-9 qty), all models: plug-in $14.95, BNC $32.95, SMA $34.95, Type N $35.95

Surface-mount, dc to 570MHz

SCLF-21.4	DC-22	32-41	41-200	SCLF-190	DC-190	290-390	390-800
SCLF-30	DC-30	47-61	61-200	SCLF-380	DC-380	580-750	750-1800
SCLF-45	DC-45	70-90	90-200	SCLF-420	DC-420	750-920	920-2000
SCLF-135	DC-135	210-300	300-600				

Price, (1-9 qty), all models: $11.45

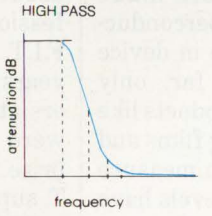
Flat Time Delay, dc to 1870MHz



Model No.	Passband MHz loss < 1.2dB	Stopband MHz loss > 10dB	loss > 20dB	VSWR Freq. Range, DC thru 0.2fco X	0.6fco X	Group Delay Variations, ns Freq. Range, DC thru fco X	2fco X	2.67fco X
PBLP-39	DC-23	78-117	117	1.3:1	2.3:1	0.7	4.0	5.0
PBLP-117	DC-65	234-312	312	1.3:1	2.4:1	0.35	1.4	1.9
PBLP-156	DC-94	312-416	416	0.3:1	1.1:1	0.3	1.1	1.5
PBLP-200	DC-120	400-534	534	1.6:1	1.9:1	0.4	1.3	1.6
PBLP-300	DC-180	600-801	801	1.25:1	2.2:1	0.2	0.6	0.8
PBLP-467	DC-280	934-1246	1246	1.25:1	2.2:1	0.15	0.4	0.55
▲BLP-933	DC-560	1866-2490	2490	1.3:1	2.2:1	0.09	0.2	0.28
▲BLP-1870	DC-850	3740-6000	5000	1.45:1	2.9:1	0.05	0.1	0.15

Price, (1-9 qty), all models: plug-in $19.95, BNC $36.95, SMA $38.95, Type N $39.95
NOTE: ▲: -933 and -1870 only with connectors, at additional $2 above other connector models.

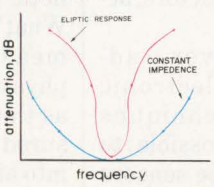
high pass, Plug-in, 27.5 to 2200MHz



Model No.	Stopband MHz loss < 40dB	loss < 20dB	Passband MHz loss < 1dB	VSWR Pass-band Typ.	Model No.	Stopband MHz loss < 40dB	loss < 20dB	Passband MHz loss < 1dB	VSWR Pass-band Typ.
PHP-25	DC-13	13-19	27.5-200	1.8:1	PHP-400	DC-210	210-290	395-1600	1.7:1
PHP-50	DC-20	20-26	41-200	1.5:1	PHP-500	DC-280	280-365	500-1600	1.8:1
PHP-100	DC-40	40-55	90-400	1.8:1	PHP-600	DC-350	350-440	600-1600	2.0:1
PHP-150	DC-70	70-95	133-600	1.8:1	PHP-700	DC-400	400-520	700-1800	1.6:1
PHP-175	DC-70	70-105	160-800	1.5:1	PHP-800	DC-445	445-570	780-2000	2.1:1
PHP-200	DC-90	90-116	185-800	1.6:1	PHP-900	DC-520	520-660	910-2100	1.8:1
PHP-250	DC-100	100-150	225-1200	1.3:1	PHP-1000	DC-550	550-720	1000-2200	1.9:1
PHP-300	DC-145	145-170	290-1200	1.7:1					

Price, (1-9 qty), all models: plug-in $14.95, BNC $36.95, SMA $38.95, Type N $39.95

bandpass, Elliptic Response, 10.7 to 70MHz



Model No.	Center Freq. (MHz)	Passband I.L. 1.5 dB Max. (MHz)	3 dB Bandwidth Typ. (MHz)	Stopbands I.L. > 20dB at MHz	I.L. > 35dB at MHz
PBP-10.7	10.7	9.6-11.5	8.9-12.7	7.5 & 15	0.6 & 50-1000
PBP-21.4	21.4	19.2-23.6	17.9-25.3	15.5 & 29	3.0 & 80-1000
PBP-30	30.0	27.0-33.0	25-35	22 & 40	3.2 & 99-1000
PBP-60	60.0	55.0-67.0	49.5-70.5	44 & 79	4.6 & 190-1000
PBP-70	70.0	63.0-77.0	68.0-82.0	51 & 94	6.0 & 193-1000

Price, (1-9 qty), all models: plug-in $18.95,
BNC $40.95, SMA $42.95, Type N $43.95

Constant Impedance, 21.4 to 70MHz

Model No.	Center Freq. MHz	Passband MHz loss < 1dB	Stopband loss > 20dB at MHz	VSWR 1.3:1 Total Band MHz
PIF-21.4	21.4	18-25	1.3 & 150	DC-220
PIF-30	30	25-35	1.9 & 210	DC-330
PIF-40	42	35-49	2.6 & 300	DC-400
PIF-50	50	41-58	3.1 & 350	DC-440
PIF-60	60	50-70	3.8 & 400	DC-500
PIF-70	70	58-82	4.4 & 490	DC-550

Price, (1-9 qty), all models: plug-in $14.95,
BNC $36.95, SMA $38.95, Type N $39.95

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CIRCLE 136 FOR U.S. RESPONSE **CIRCLE 137 FOR RESPONSE OUTSIDE THE U.S.**

INTERLEAVED GATES ON BASIC CELLS IN GATE ARRAYS BOOST ROUTABILITY

Although many basic arrangements have been developed for multitransistor cells that form the core array in mask-programmable gate arrays, routing efficiencies for high-density gate arrays are usually still limited to 40 to 50%. That number is typical of today's double-level-metal chips which employ a sea-of-gates architecture. A third metal level would raise the routing efficiency, but it can add considerably to the array's cost due to extra processing steps. As a result, it's no surprise that there's an incentive to remain with two levels of metal interconnections.

Designers at S-MOS Systems, San Jose, Calif., however, think they have found a solution: a new cell layout that employs an interleaved gate structure. Unlike earlier cells that use straight metal lines to form the gates, the new layout uses opposing E-shaped gate contacts that are interleaved with each other. The E-shaped gates provide more contact points for first- and second-level metal layers, simplifying the wire routing computations and enabling more of the array's gates to be utilized (the easier the gates can be contacted, the easier it is to route the metal, because more options are open to the routing software). The company expects that routing efficiencies of 80 to 95% can routinely be achieved for circuits with complexities exceeding 100,000 gates.

The advantage of the new approach is demonstrated in the layout of a common gate-array function—a transmission gate. Using the older cell-layout method might mean that first-level metallization would have to occupy or block many of the metal-1 wiring tracks typically routed over a cell. In contrast, the interleaved structure requires just three short, straight metal (or silicided polysilicon) jumpers that occupy only three wiring channels. The straight metal jumpers also can be extended to connect to the cells above or below the cell being used, simplifying the cell interconnections to an even greater extent. That frees up more channels for cell-to-cell routing, which further improves the efficiency of the layout.

Two test cases were used to evaluate the cell structure: a circuit containing 7000 gates and one containing about 16,000 gates. In the first case, an array employing the interleaved gate cells achieved a utilization of greater than 95%. In the second case, chip utilization exceeded 80%.

The new cell structure thus allows higher utilization of the gates on the base array, and the chip size can be trimmed by about 15% over chips implemented with the older cell layout. The smaller size is a result of the improved efficiency, because the number of "raw" gates can be reduced on the chip without affecting the number of utilized gates. The smaller physical chip size might typically translate into lower chip cost for the circuit designer.

The interleaved-gate cell design will be incorporated into a family of gate arrays—the SLAS1 series—by S-MOS Systems. The company plans to release the family next quarter. By employing a CMOS process with 0.8-μm minimum features, the array family will pack a large number of gates into reasonable chip areas. This results in a more cost-effective solution than previous arrays that were implemented with the same feature sizes. Initial gate-array family members will include arrays with usable gate counts of 7, 18, 33, 80 and 120 kgates.

For more information, contact S-MOS at (408) 954-0120.

DAVE BURSKY

PLANAR PROCESS YIELDS COMMERCIAL HIGH-TEMPERATURE SQUIDS

By using planar semiconductor technology, a small German company has readied magnetic sensors made from ceramic superconductors with high critical temperature and is now offering them as commercial products on the market. The firm, Forschungsgesellschaft für Informationstechnik (Research Institute for Information Technology or F.I.T.), has just sold the first of its so-called superconducting quantum interference devices, or SQUIDs, to a German customer.

F.I.T., located in Bad Salzdetfurth, considers fabricating marketable magnetic sensors made from high-T_c superconductors a milestone in device technology. So far, only semi-finished products like superconducting films and simple meters to measure liquid nitrogen levels have been available on the market as products using ceramic superconductors, according to F.I.T.

Now, however, advanced microelectronic fabrication techniques have made it possible to build SQUID-type sensors for magnetic field measurements. That opens the door for devices based on high-T_c superconducting materials to be integrated into a wide range of tools used in measuring and professional electronics. The F.I.T. feat comes only six years after two researchers at IBM in Switzerland were awarded the Nobel prize for discovering high-T_c superconductors.

SQUID magnetometers are the most sensitive magnetic flux sensors around. What's more, a SQUID can measure every known physical quantity, as long as the quantity to be measured can be transformed into an equivalent magnetic flux via a transducer. Applications for these sensors range from precision measurements to detecting minute brain currents, explains Jens Würten-

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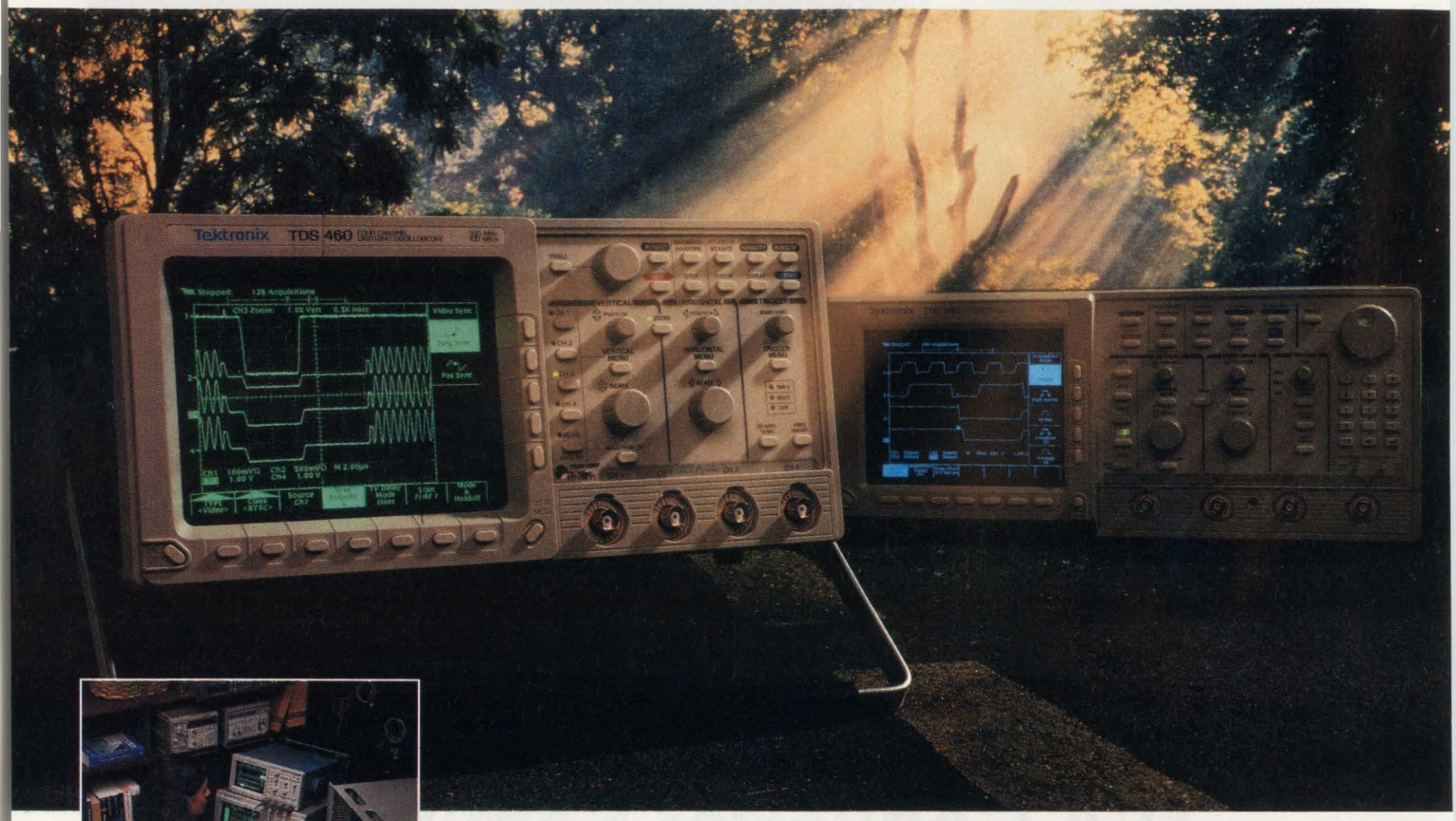

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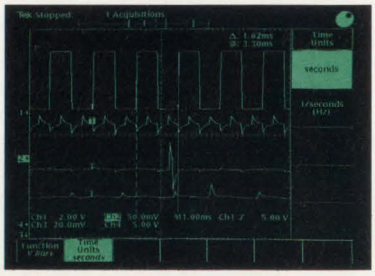

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CIRCLE 165 FOR RESPONSE OUTSIDE THE U.S.

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3GA-188087-0

berg, responsible for marketing at F.I.T.

A special fabrication process, developed to the point where it can be used in production, has enabled the F.I.T. experts to produce high-T_c SQUIDs with consistent properties—a prerequisite for a commercial product. In the configuration implemented by the F.I.T. experts, the high-T_c SQUIDs aren't as sensitive as low-T_c types. But their sensitivity is already one to two orders of magnitude higher than that of conventional nonsuperconducting magnetometers.

Specifically, the sensitivity of the F.I.T. devices checks in at one pico-tesla, or 1×10^{-12} tesla, Würtenberg says. The earth's magnetic field, in comparison, measures around 1×10^{-4} tesla.

Compared to commercial low-T_c magnetometers made of, say, niobium SQUIDs, the prime advantage of the new devices is the considerably reduced cost for cooling. They operate at temperatures of −190°C, a level attainable with either liquid nitrogen or a specially designed cooling apparatus. As a result, the unique properties of superconducting devices can be exploited with much simpler handling and at considerably lower cost than with helium-cooling equipment.

High-precision measuring of magnetic and electric quantities is an obvious application for high-T_c SQUIDs. Others are precise measurements of such mechanical quantities as translation, rotation, or acceleration via special transducers. In the future, Würtenberg notes, high-T_c SQUIDs may be widely used in material evaluation by non-destructive testing methods. Shrink holes, fissures, corrosion, mechanical stress, and plastic and elastic deformations can thus be detected and localized in the material. In medical electronics, high-T_c SQUIDs could bring about magnetocardiograms. Their use in geophysics, such as exploring for mineral resources, is also being discussed.

To fabricate their high-T_c SQUIDs, the F.I.T. researchers are using a laser-deposition technique, whereby a 100-nm- to 300-nm-thick superconducting film is put on a ceramic substrate consisting preferably of strontium titanate. A small disk made from superconducting ceramic is evaporated by the light from a high-power pulsed laser and deposited on the substrate in an oxygen atmosphere. Producing the superconducting film, which is made of yttrium barium copper oxide, is a routine operation at the institute. The high and consistent quality of this film is a prerequisite for the SQUIDs' excellent performance properties.

The SQUID's coarse structure—its dimensions are about 300 by 300 μm—is made by photolithography and wet-chemical etching. The most difficult part of the fabrication process involves producing a well-defined weak link, or Josephson junction bridge, in the superconducting film. This bridge determines the magnetic flux in terms of fundamental constants (that is, microscopic quantum quantities).

The F.I.T. SQUIDs have a weak bridge about 0.3 μm long and 3 μm wide. To achieve reproducible structures at these dimensions, electron-beam lithographic techniques are needed. The "weakening" of the bridge is attained by ion implantation, whereby the tiny bridge region is bombarded with oxygen ions. With this process, the superconducting properties in the bridge region are modified in a controlled manner.

JOHN GOSCH

TRANSCONDUCTANCE IC AMP HAS BANDWIDTH OF OVER 300 MHz

When built on a high-speed complementary process, a new basic analog IC circuit building block from Burr-Brown can form the heart of various wideband amplifiers, including both current and voltage-feedback op amps with bandwidths of several hundred megahertz.

This building block, from the company's design center near Frankfurt, Germany, is dubbed a "diamond transistor." It basically functions as a voltage-controlled current source, otherwise known as an operational-transconductance amplifier (OTA).

Although built from ten transistors, the OTA's three terminals are labeled base, emitter, and collector, just like the terminals of a conventional bipolar transistor are labeled *(Fig. 1a)*. The building-block's developer Burr-Brown has even created a symbol for these terminals *(Fig. 1b)*.

The analog building-block circuit can used in a conventional common-emitter configuration *(Fig. 2a)*. It can also be used in a common-collector (emitter-follower), configuration *(Fig. 2b)*.

In the common-collector configuration, connecting the collector terminal to the emitter terminal doubles the device's current output *(Fig. 2c)*.

Unlike conventional bipolar transistors, use of the common-emitter circuit configuration doesn't

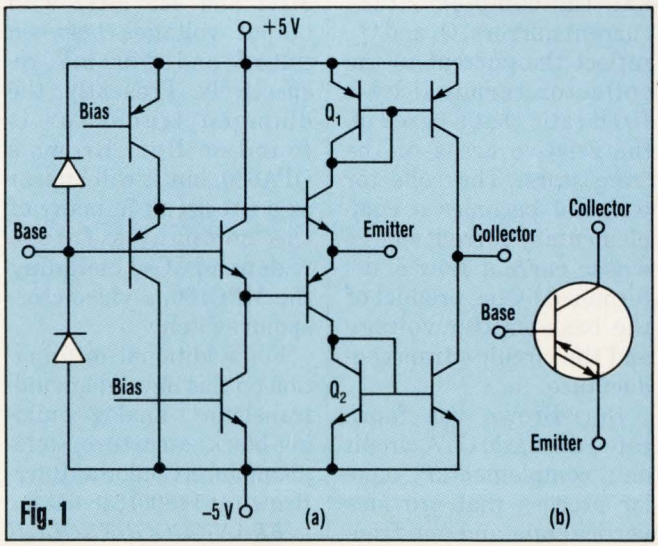

Fig. 1

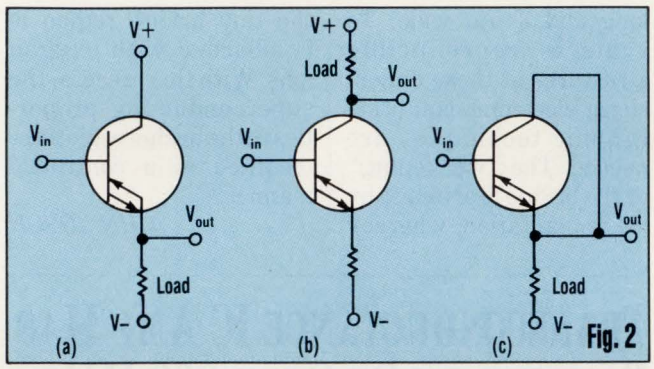

Fig. 2

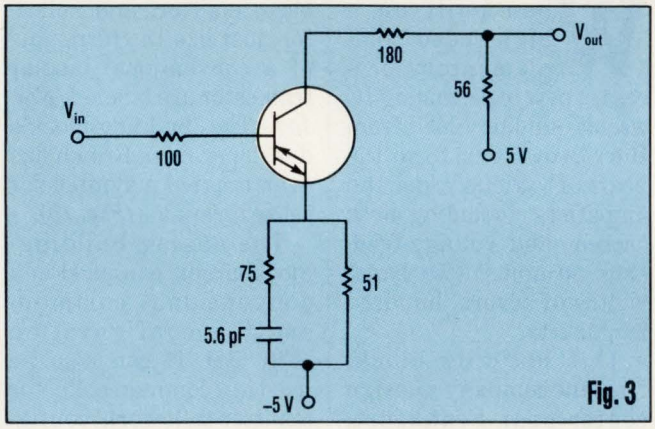

Fig. 3

result in the inversion of the input-to-output phase.

In the diamond transistor, ideally, the voltage at the high-impedance base terminal is transferred to the emitter input/output terminal at a low impedance. If a current flows out of or into the emitter terminal, the complementary current mirrors, Q_1 and Q_2, reflect the current to the collector terminal by a fixed ratio that's based on the relative areas of the transistors. The collector terminal becomes a complementary current source whose current flow is determined by the product of the base-emitter voltage and the circuit's transconductance.

Burr-Brown has fabricated the basic OTA circuit on a complementary bipolar process that provides vertical npn and pnp transistors with transit frequencies (f_ts) of 3.5 and 2.7 GHz, respectively. Connected in an open-loop circuit the IC's designers call the"straight-forward amplifier," it can achieve a voltage gain of 3.85 *(Fig. 3)*. The circuit offers 3-dB bandwidths between 350 MHz and 443 MHz with output voltages between ±2.5 V and ±100 mV, respectively. Presently, the diamond transistor is found on Burr-Brown's OPA660, but it will appear as a subcircuit in many of the company's future wideband ICs, including the MPC100, a video crosspoint switch.

For additional information on this new "diamond-transistor" analog building-block structure, telephone John Conlon at Burr-Brown at 1-(800) 548-6132.

FRANK GOODENOUGH

GEOPHYSICISTS GET 24-BIT, 0.1-W ADC TO SENSE SEISMIC SIGNALS

Oil-hunters and other geophysicists need every digitized decibel of dynamic range they can squeeze from their seismic data-acquisition systems. And because the systems are battery powered for field use, low power drain is vital. Designers at Crystal Semiconductor in Austin, Texas, have come to the aid of their brother engineers with a 24-bit two-chip delta-sigma analog-to-digital converter (ADC) that provides up to 133 dB of dynamic range, yet works on just 100 mW of power. When asleep, it draws less than 1 mW.

In the search for likely drilling sites, oil-exploration engineers spend their time stringing large arrays of geophones (transducers resembling loudspeakers) across miles of rugged terrain. Then they generate "signals" by setting off underground explosions, or with machines called "thumpers" that pound the earth. The resulting waves of acoustic energy penetrate deep into the earth.

As each wavefront reaches each new layer of rock, a portion of the signal is reflected back toward the surface. The reflections are caused by the difference in density between each rock type. The geophones pick up the energy from each of the multiple returning wavefronts, including that directly from the signal source, and convert it to a voltage. Depending on the distance between the signal source and the transducer, the depth of the reflecting rock layers, and the attenuation of the returning energy by the rock it passes through, the voltage from the transducer easily spans a dynamic range of over 120 dB. Information is contained in the relative amplitude and phase of all the wavefronts.

About 20 years ago, the data-gathering systems were purely analog from geophone to graphic recorder. More recently, the wide dynamic range has been achieved with multi-transducer, floating-point systems.

Here, the outputs of many geophones are cabled to a box containing a multiplexer circuit followed by a programmable-gain amplifier (PGA) and finally a 12- or 16-bit ADC. Such systems are heavy power users and can pick up electrical noise in the cabling. But, regardless of the multiplexer's speed and the PGA's speed and accuracy (when switching from one gain to another), phase and amplitude errors will creep in. With the 100-mW Crystal converters, a battery-powered ADC can be used for each geophone providing 24 bits of instantaneous (no delay in the system between data points) dynamic range.

Crystal's analog and digital designers have optimized their circuit-design technology to build a self-calibrating, variable-bandwidth delta-sigma ADC that provides a resolution of 24 bits.

The converter circuit is comprised of two chips: a delta-sigma modulator IC

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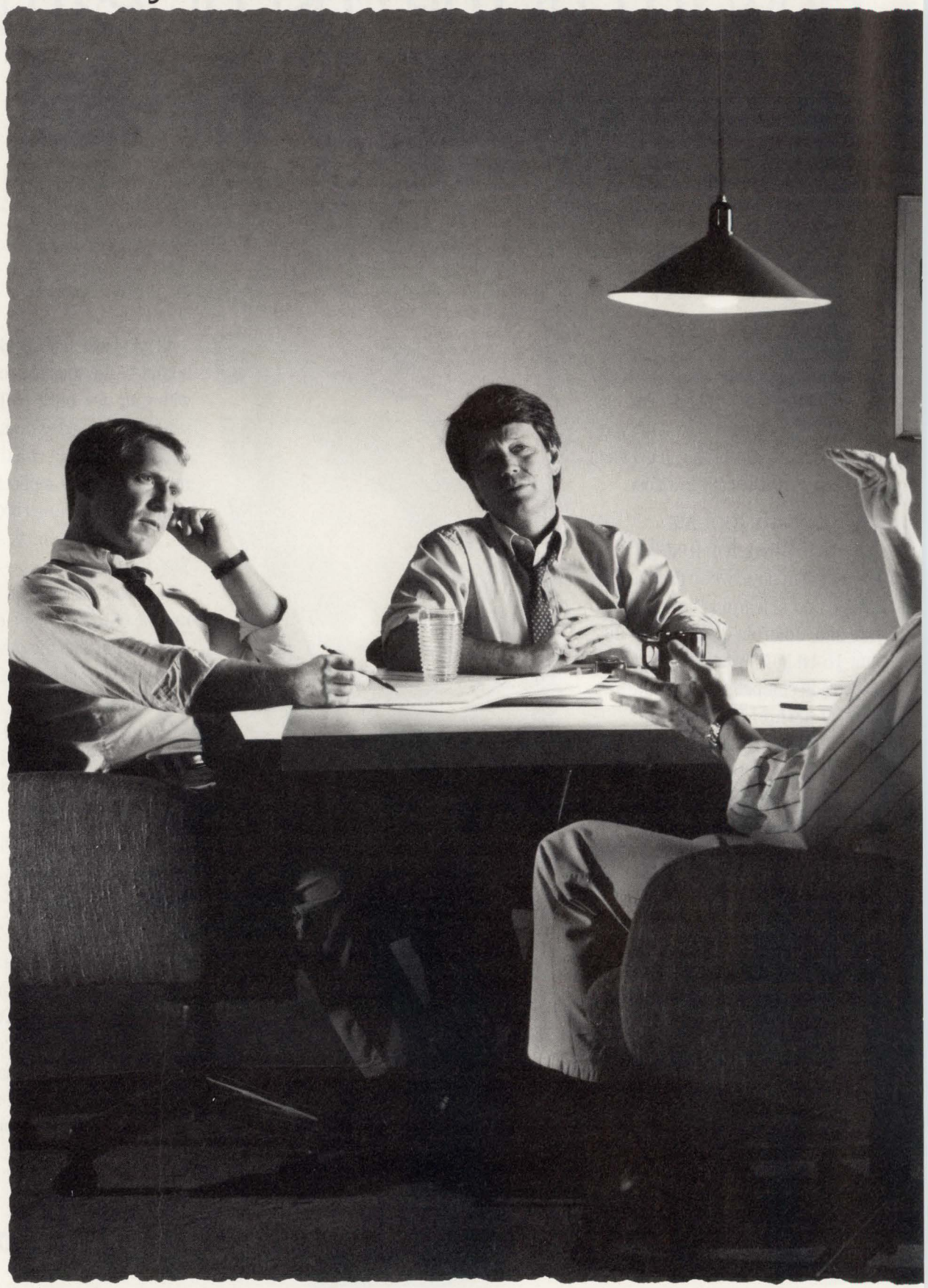

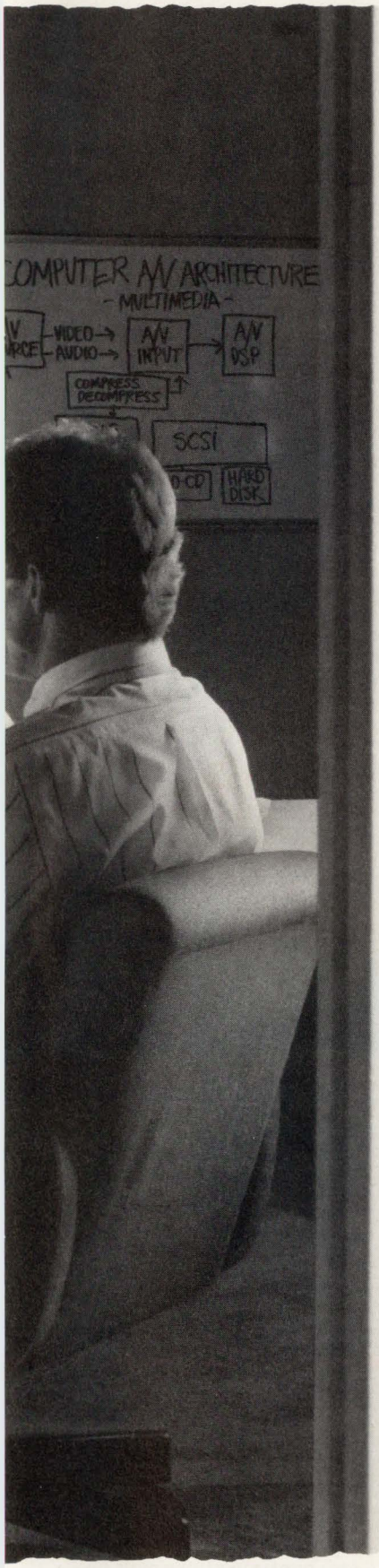

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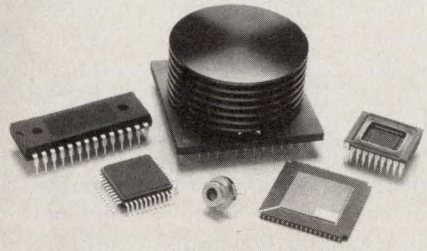

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and an FIR filter IC, both CMOS devices. The former is built on a process with 3-μm feature sizes, while the latter's process features 1.2-μm feature sizes.

The ADC is designed to handle input signals from dc to 1500 Hz. The front-end chip, the CS5323 modulator, consists of a fourth-order delta-sigma modulator circuit that can be programmed to oversample the input from 64 to 4096 times, virtually eliminating the need for antialiasing filters. Its 256-kHz output (serial) bit stream feeds the CS5322 filter, which contains a low-pass FIR filter and decimator. The decimator's programmable serial (digital) output provides an instantaneous dynamic range of 103 dB for a 1500-Hz input signal, 110 dB for 411 Hz, and 133 dB for a 31.25 Hz input. Signal-to-distortion at 411 Hz runs 110 dB.

Seven input-frequency ranges (3-dB corner frequencies of the filter) can be programmed: 25, 51, 102, 205, 411, 824, and 1650 Hz. Passband frequencies that are flat to within 0.2 dB run approximately 90% of the corner frequency (70% of Nyquist). Stopband (Nyquist) frequencies in which the input is down at least 130 dB run approximately 1.3 times the programmed passband frequency. Other applications include the acquisition of seismic signals from earthquakes, underground nuclear explosions (treaty verification), and the low-frequency passive sonar that tracks vessels 1000 or more miles away.

For additional information, call Mike Paquette at Crystal Semiconductor at (512) 445-7222.

FRANK GOODENOUGH

PLASTIC PACKAGES DISSIPATE HIGH HEAT OF ICS

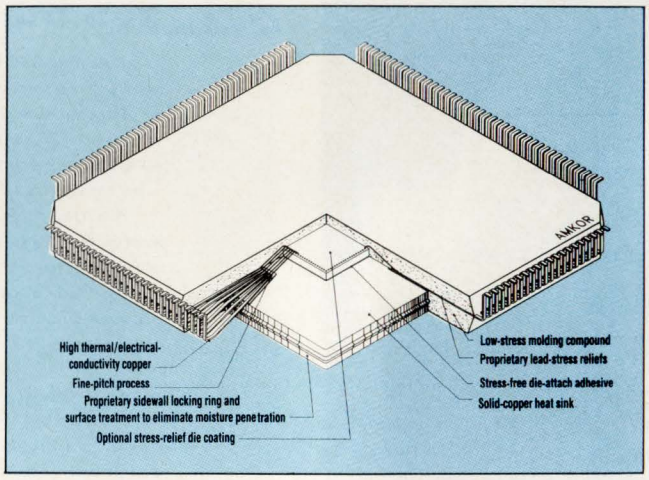
Using advanced thermal-management concepts, including direct attachment of the semiconductor die to a large-area solid-copper heat sink, a new plastic IC package handles die sizes up to 0.350 by 0.350 in. The 28-by-28-mm package, developed by Amkor Electronics Inc., Tempe, Ariz., also features an internal ground plane and has a very low thermal resistance of less than 0.4°C/W from junction to case *(see the figure)*.

The packages are designed to work with EG&G Wakefield's external Deltem pin-fin heat sinks. When used with these heat sinks and flowing air, a junction-to-ambient thermal resistance of 8°C/W can be expected.

In applications that don't permit the use of air flow or an external heat sink, the package's thermal coupling to the pc board is still better than that of other high-performance packages like multilayer ceramics, according to the company. Power dissipation is up to 4 W without the use of an external heat sink and more than 10 W with the use of an external heat sink and airflow.

To reduce the thermal coupling to the board, large regions of each package lead were closely coupled to the package's massive internal heat sink. The heat sink consists of oxygen-free, high-conductivity copper.

Oxygen-free copper is one of the purest forms of copper, thus its thermal conductivity is very high. This permits the package to be used in medium-power applications without concern for heat-sink attachment. The heat sink is made even more effective by virtue of its direct coupling with the die. Other packages are fabricated with intervening layers between die and heat sink, which can impede the process of thermal coupling.



A stress-free die-attach process was also developed for the package, so that large silicon chips can be attached directly to the solid-copper heat sink with only a few percent of the usual stresses. Typically, high-power, large-area ICs exhibit high die stress when mounted to copper. Amkor's engineers came up with a die-attach adhesive formulation that relieves those high stresses on the die.

In addition, the leadframe itself provides spring tension to the heat sink during the molding operation to prevent flash. The stress relief assures that the built-up spring forces are properly released. A molding compound with specially shaped fillers further reduces stress on the package. A high-conductivity copper-alloy leadframe is used in the package, and a fine-pitch internal lead structure allows shorter bond wires. At present, Amkor is using 4.7-mil pad-to-pad pitch on the die in production, and is evaluating 4.5- and 4.0-mil pitches for future use.

A frequent cause of IC-package failure is moisture permeability. To address the problem of moisture ingress along the heat-sink-to-plastic interface, the company's designers incorporated a locking ring and sidewall treatment, which provides a barrier to moisture penetration.

Initially, the package, called the PowerQuad2, will be offered in 160 and 208 leads in the 28-by-28-mm plastic EIAJ quad-flatpack outline. Other package configurations will be added later this year.

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500-MHz 12-Bit DAC Creates 100-MHz Signals

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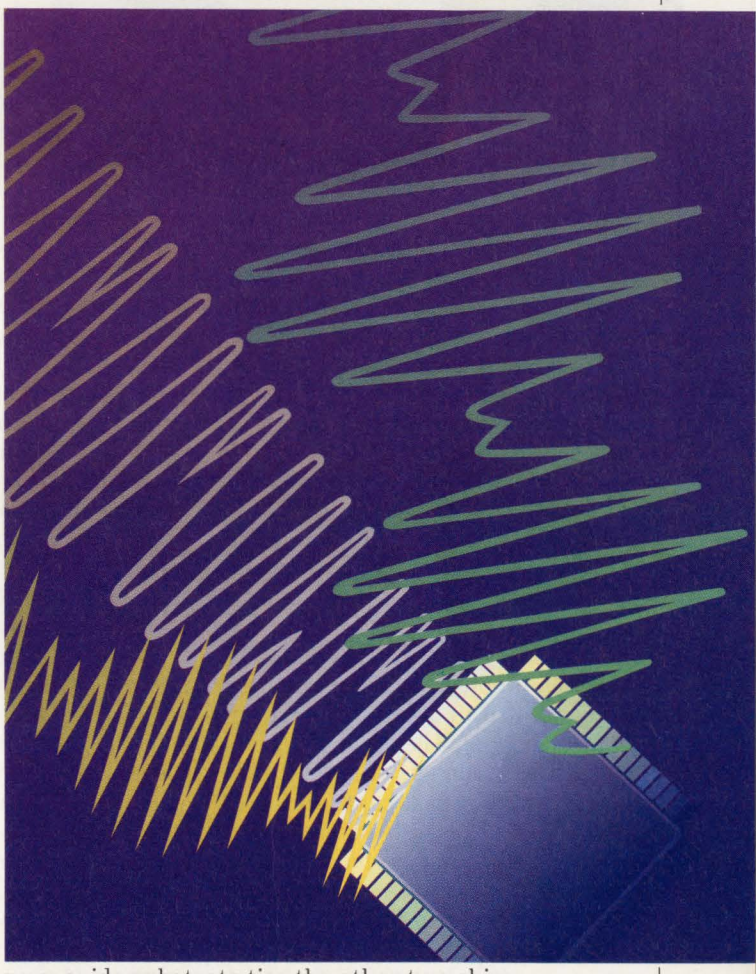


From early on, computers have driven digital-to-analog converters, generating random analog waveforms from look-up-table memories. While system designers could procure general-purpose DACs with 8 to 16 bits of resolution, most update (clock) rates were limited to about 1 MHz (except for limited-accuracy 8-bit video/graphic chips). These limitations kept DACs from generating output frequencies above a few hundred kilohertz.

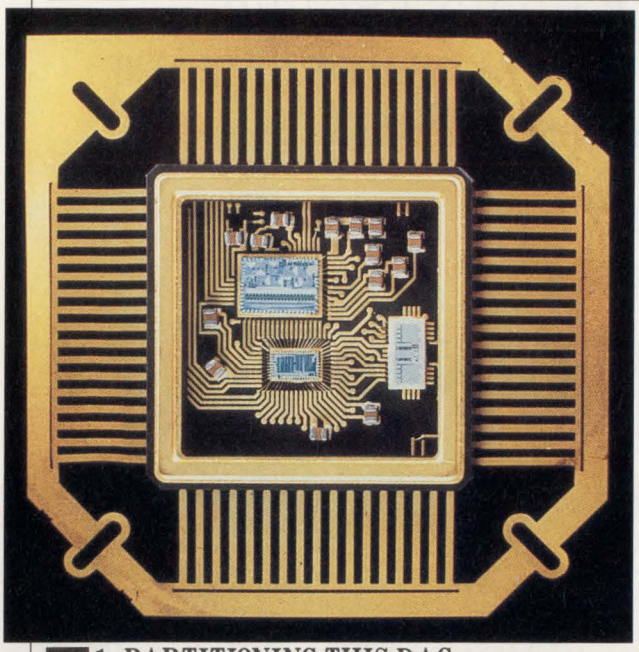
But this situation is evolving with the arrival several 12-bit IC DACs with clock rates from 20 to 100 MHz. These DACs are aimed specifically at direct digital synthesis (DDS) of analog waveforms. The latest manifestation of this trend is Burr-Brown's DAC650, which has a clock rate that's a factor-of-five faster than the former speediest—a whopping 500 MHz *(for a look at other 12-bit DACs and how they're used, see* ELECTRONIC DESIGN, *Sept. 12, 1991, p. 63.)*

The DAC650 is a good example of innovative designers asking themselves, "What's the best way to build a better mouse trap?" Rather than insist (as many did) that a DAC be a single IC built on the fastest available silicon process, Burr-Brown designers took a multi-chip approach. The result was not only a faster DAC, but also a more accurate one.

The DAC650 employs three devices, each taking advantage of the features offered by a different technology *(Fig. 1)*. One IC, supplied by Vitesse Semiconductor, includes gallium arsenide MESFETs for high-speed current switches, as well as logic and clock circuits. A second silicon IC provides precision dc current sources and a dc reference. A thin-film nichrome-resistor network on an aluminum oxide substrate ties the other two chips together, further insuring accuracy *(Fig. 2a)*. The last two chips are fabricated by the company, Burr-Brown.

The DAC's partitioning into three circuits allowed each circuit to be optimized for the job it does best. The GaAs chip provides the necessary speed, while the silicon and nichrome devices supply the needed precision. The DAC's basic architecture is not very dif-

500-MHz 12-BIT DDS DAC



1. PARTITIONING THIS DAC into three chips allows it clock out 12-bit words at 500 MHz, making it useful for direct digital synthesis of arbitrary waveforms. The three chips forming Burr-Brown's DAC650 are a GaAs IC that provides the speed (lower left), and a silicon IC and a thin-film nichrome-resistor device that supplies the precision and accuracy (upper left, and right, respectively). The entire circuit is housed in a 68-pin surface-mount package with gull-wing leads.

ferent from most high-speed current DACs.

The GaAs MESFETs are optimized for the high-speed jobs, while bipolar silicon transistors and laser-trimmed, nichrome resistors provide the necessary precision. Demanding just 2 W of power, the three devices are contained in a ceramic surface-mount package. The only additional off-chip components required are power-supply bypass capacitors.

DDS DACs "earn their spurs" by not producing spurious harmonics of the fundamental generated frequency, as can be seen by their spurious-free dynamic range (SFDR) specifications, which are critical for most DDS-DAC applications. The SFDR specification typically runs 70 dB for the DAC650 while putting out a 1-MHz sine wave and driven by an 85-MHz clock. SFDR, usually expressed in dB, can be defined as the ratio of the amplitude of the DAC's output sine wave's largest harmonic to the amplitude of that output sine wave itself. By raising the clock to 500 MHz, the DAC650 can create a 100-MHz sine wave with an SFDR of 50 dB. The use of a 12-bit DAC increases the signal-to-noise ratio commonly available on 8- and 10-bit high-speed DACs.

According to Tom Anderson, the DAC650's designer, tests on prototypes indicate that the DAC should be useful with clock rates to over 800 MHz, and a test system is being built to measure SFDR up to those clock rates. Such a system *is not* a trivial task. It must accurately measure the magnitude of the harmonics of a complex waveform as much as 70 dB below a several-hundred-megahertz fundamental "sine wave."

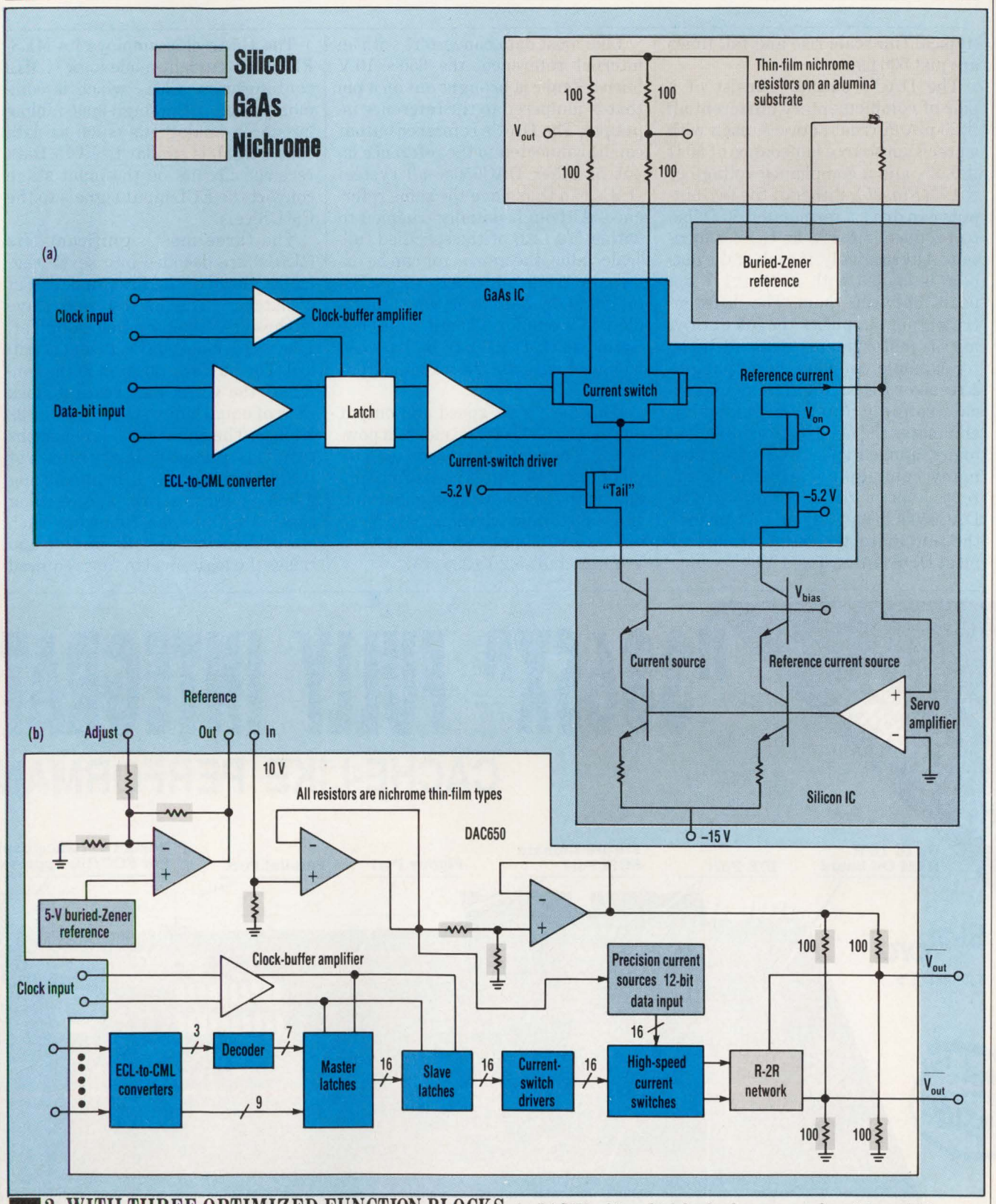
The DAC650 will readily find a home in the communications arena, its original destination. Here, it will replace multiple crystal oscillators and phase-locked loops in systems requiring sophisticated modulation techniques using variable-phase and/or frequency signals. Examples include tunable receivers, modems, and the now burgeoning spread-spectrum systems still in their infancy outside the military. Compared with conventional techniques, DDS combines unparalleled frequency agility (the ability to change frequency rapidly) with both phase and frequency resolution, accuracy, and stability. Many systems require two local oscillators (in-phase and quadrature) with a constant phase relationship. Using two DACs guarantees such performance, because both signals are derived from one clock.

The DAC650 will also find a home generating high-speed arbitrary waveforms (including sine waves) in various test applications ranging from general-purpose bench instruments to ATE systems for boards and ICs, particularly fast/high-frequency analog and mixed-signal chips. It's possible to project the DAC650's use in high-end raster-scan and the few remaining vector-scan graphics applications. In the former (now using 400-to-600-MHz 8-bit DACs or 100- to 150-MHz 10-bit DACs), it offers gray-scale resolution and/or color accuracy or refresh rates undreamed of. To vector-scan applications, the DAC offers unprecedented complete-screen, or local-area, update rates.

Filling sockets that now use lower-clock-rate 10- or 12-bit competitive devices represents a third venue for this DAC. Depending on the application, typical systems operate (sample) at clock rates from 2.5 to over 10 times the output frequency. Replacing a currently available device sampling at 20 MHz to create a 1-MHz sine wave with an SFDR of 65 dB, with a DAC650 sampling at 85 MHz, can up the SFDR to 70 dB and significantly simplify the filter required at the output of the DAC. Upping the clock rate even more, while potentially reducing SFDR, can further simplify the filter. A beta site was clocking a 10-bit 160-MHz DAC at over 150 MHz and achieving an SFDR of 35 dB. Switching to the DAC650 upped the SFDR by 20 dB.

Unlike many other so-called "12-bit" DDS DACs, the DAC650 is truly 12-bit accurate. Credit this to its laser-trimmed thin-film resistors and silicon buried-Zener reference. Moreover, it's 12-bits accurate at both dc and dynamically. Both differential linearity (DNL, which guarantees monotonicity) and integral linearity (INL) are trimmed at the wafer level to 12 bits to within $\pm 1/2$ a least-significant bit (LSB), and remain within ± 1 LSB after packaging. In comparison, many other DDS DACs specify a DNL and INL of ± 2 (or more) LSBs. Moreover, the DAC650's output settles to within $\pm 0.01\%$ of final value, for a full-scale step change, in under 5 ns. Such precision pulse handling lets it generate 12-bit-accurate arbitrary waveforms with fast rising and falling edges

500-MHz 12-BIT DDS DAC



2. WITH THREE OPTIMIZED-FUNCTION BLOCKS, the DAC650 achieves high levels of accuracy and precision at high speeds (a). The DAC employs a relatively conventional architecture with high-speed current switches steering the current from precision current sources whose accuracy is set with thin-film nichrome resistors (b). The current switches and other high-speed circuits reside on the GaAs chip, while the precision current sources and a buried-Zener reference reside on the silicon chip. All the precision resistors are thin-film nichrome types on an alumina substrate. A single-bit switch and bit-current source are shown for simplicity.

500-MHz 12-BIT DDS DAC

(typical full-scale rise and fall times are just 500 ps).

The DAC's outputs consist of a pair of complementary (differential) ±20-mA current sources, each with a precision source impedance of 50 Ω ±0.5%, and a compliance voltage of ±1 V *(Fig. 2b)*. Either of the two outputs can drive a terminated 50-Ω line to produce ±0.5 V at the termination. Alternatively, if each of the outputs is loaded with 50 Ω, ±1 V appears between them. The differential output simplifies the job of driving a transformer in RF applications, for example, coupling the output into a receiver for tuning. The symmetrical-around-ground output swing eliminates the need for ac coupling in many applications, and eliminates many common-mode parasitic effects, as well. Grounding the DAC650's offset-adjust pin converts the output to the output range of most DDS DACs, 0 to -1 V.

Like most data converters with an internal reference, the 650's 10-V buried Zener is brought out on a pin that is jumpered to the reference input pin. The DAC's reference output can be connected to the reference input of other DAC650s—all system DACs can thus have the same reference. Although initially trimmed to within 1/2 LSB of the specified full-scale value, the gain error can be externally trimmed to zero with a potentiometer. Moreover, when multiple DACs employ a single reference circuit, each DAC may be trimmed independently to the exact output voltage.

Considering its speed and output power, the 650 is by no means a power hog. The converter dissipates a total of just 2 W. But it needs five supplies with the following nominal voltages/maximum currents: +15 V/15 mA, –15 V/55 mA, +5 V/65 mA, –5 V/2 mA, and –5.2 V/225 mA.

The GaAs chip employs its MESFETs in a current-mode logic (CML) configuration. CML, which is commonly used within high-speed, bipolar-silicon analog ICs (such as data converters), is similar to ECL. Data receiver circuits on the input stage convert the ECL input signals to the CML levels.

The three most-significant bits (MSBs) are decoded into seven segments ahead of the first (master) set of latches. The master and slave latches are driven by a clock buffer. Like all high-speed ICs, layout is critical. The buffer is located in the center of the GaAs die creating clock lines of equal length to each of the 32 latches. The equal clock-line lengths result in equal clock delays to each of the 32 latches, in turn minimizing glitch energy, spurs, and settling time. An amplifier following each slave latch buffers the output and raises the logic level to that required

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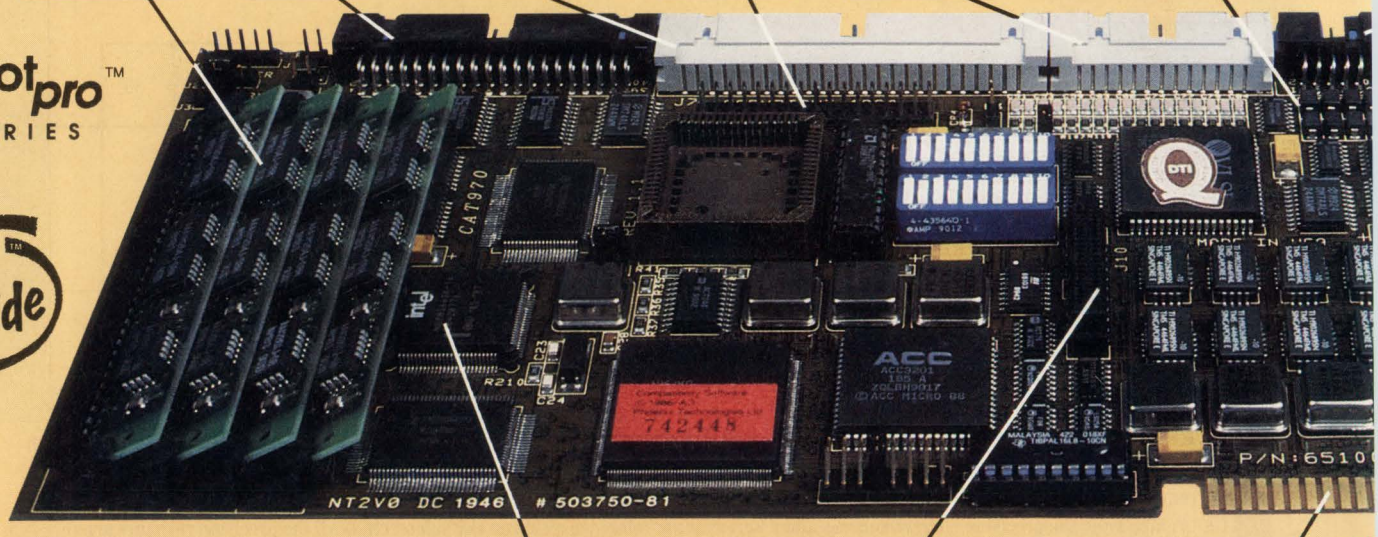

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500-MHz 12-BIT DDS DAC

to drive (turn on) the current switches. The analog performance of the MESFET logic circuits was optimized to enhance the matching of the waveforms driving the gates of the MESFET current switches.

A pair of depletion-mode MESFETs, with their areas bit-weight-scaled for current density, forms each of the differential current switches *(Fig. 2b, again)*. The differential-switch's "tail current" comes from a third MESFET whose gate is tied to the –5.2-V rail. Connecting the gate to the –5.2-V rail helps keep the switching glitch, which occurs at the common-source node of the current switches, out of the bipolar current sources.

The current-source chip is similar to a bipolar DAC lacking its current switches. Seven equal-current sources feed the seven, segment switches creating bits 1 (the MSB), 2, and 3. Like the current switches they feed, the areas of the output transistors of the current sources for bits 4 through 8 are scaled down in binary fashion. Currents for bits 9 through 12 are identical to bit-8's current. MESFET current switches connect bits 9 through 12 to a nichrome R-2R ladder for scaling down.

The currents are laser-trimmed on the wafer for both absolute accuracy and matching. Thus, no package trimming is required, increasing yield, and lowering manufacturing cost. The bipolar IC also contains the buried-Zener reference which is trimmed (also while still on the wafer) so its temperature coefficient (TC) is zero. A servo-amplifier circuit impresses the reference voltage across a gain-setting, nichrome resistor, creating a reference current through an "always-on" MESFET switch. Because the DAC's output currents are also flowing through the thin-film resistors, the absolute TC of the nichrome resistor is canceled. The reference current links the DAC's three elements, maintaining accuracy over variations in supply voltage and temperature.

The 68-pin surface-mount package employs gull-wing leads on a standard 50-mil pitch and is 1 in. to a side. Each of the two outputs connect to three adjacent pins to minimize output inductance. □

PRICE AND AVAILABILITY

The DAC650 is rated for commercial-temperature-range operation. In quantities of 100, it is priced at $250 each. In lots of 1000, the price drops to less than $200 each. Small quantities are available from stock.

Burr-Brown Corp., P.O. Box 11400, Tucson, AZ 85734; Pat Kirk, (602) 746-1111.

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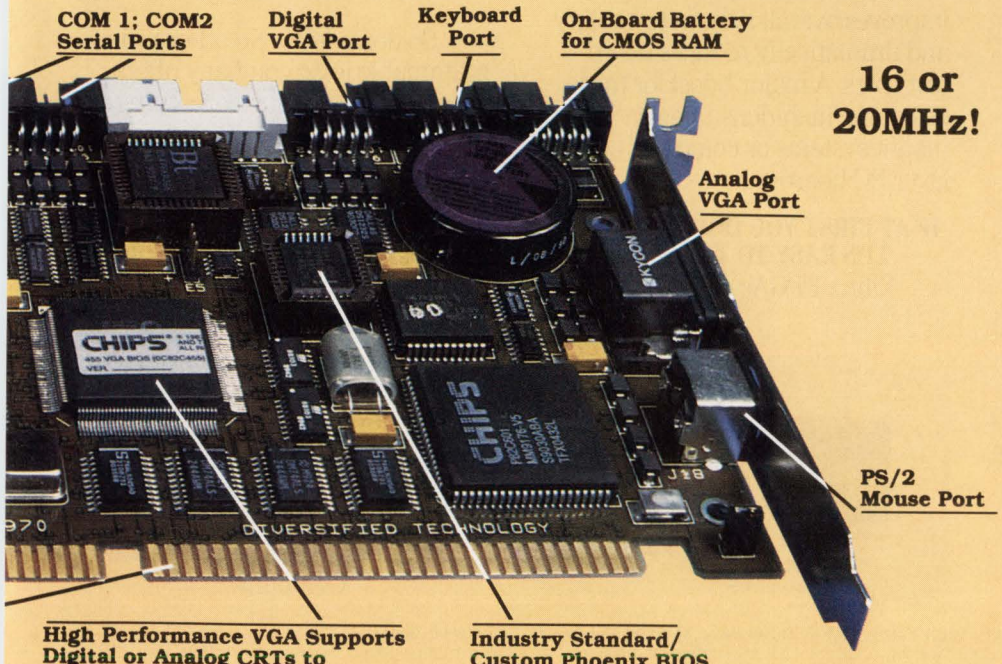

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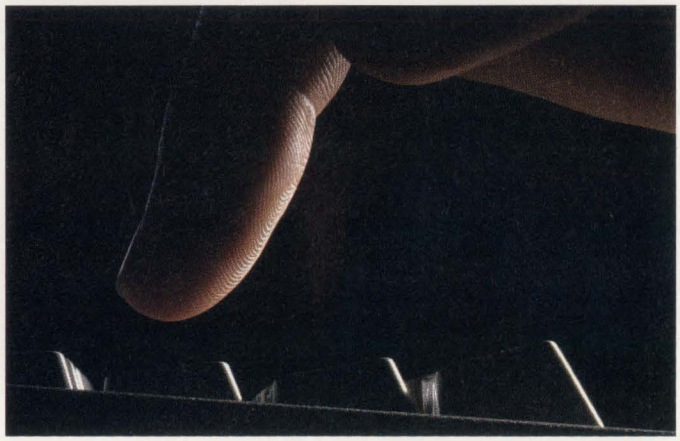

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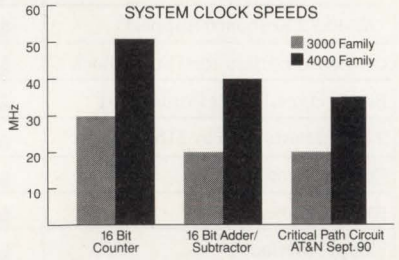

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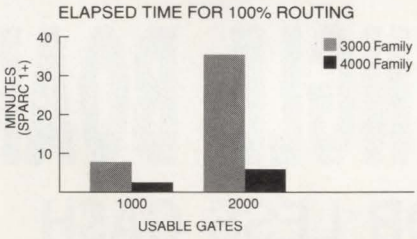

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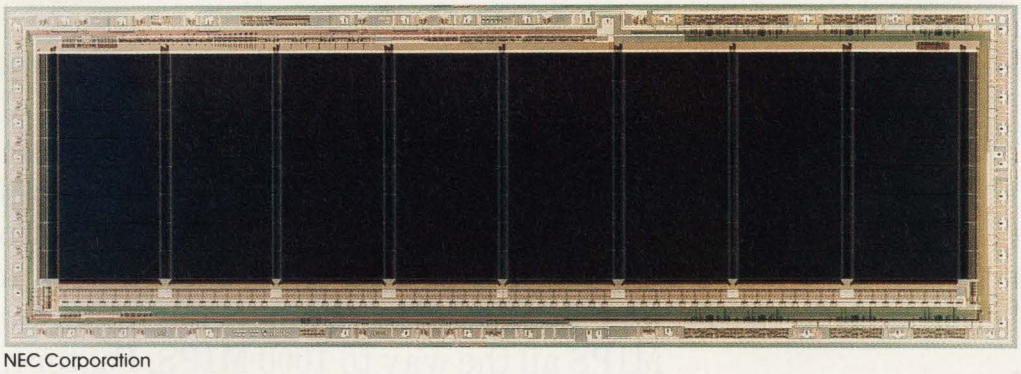

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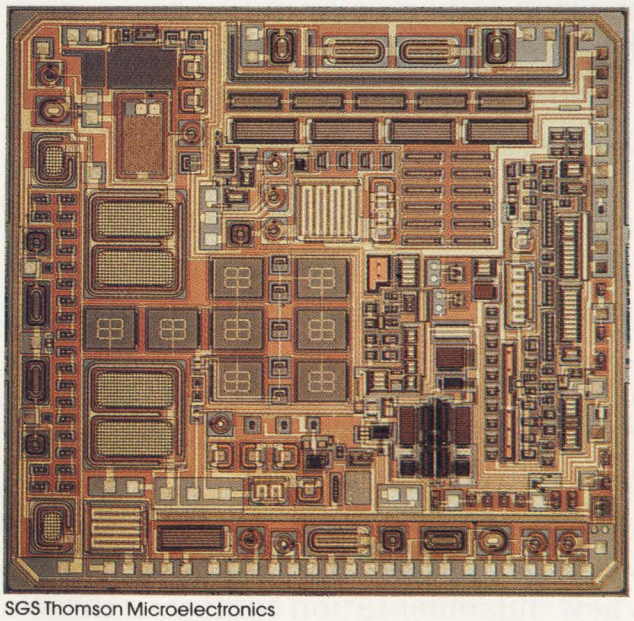
In the first report, Semiconductors Editor Dave Bursky examines the top digital technology developments. These include the latest advances in CISC and RISC microprocessors, high-speed static, dynamic, and flash memories, and neural-network chips. Processors with throughputs up to 1000 MIPS are described. A noteworthy memory development is a "system ULSI" superchip that holds 44 Mbits of 65-ns DRAM, 384 kbits of 14-ns SRAM, and 18,000 gates of custom logic.

In the second report, Analog & Power Editor Frank Goodenough provides an overview of analog technology developments. These include a multitude of analog-to-digital converter designs with many different architectures. Analog technology is also busy in the bioelectronic arena, where researchers have developed an implantable probe containing 16 independent stimulus sites. For use in studying human deafness, the probe's 11-mm^2 micromachined circuit displaces no more space in the human head than previous probe circuits with a single stimulus site. The latest in tunable filters, disk-drive controllers, and thin-film-transistor drive circuits for liquid-crystal displays are also on tap.



SGS Thomson Microelectronics

Communications & Industrial Editor Milt Leonard wraps up coverage of the ISSCC with a report that details device developments for high-speed telecommunications and data-communications systems. These include crosspoint switches, RF arrays, prescalers, transceivers, oscillators, and circuit designs for fiber-optic networks.

BY
DAVE
BURSKY

ISSCC

DIGITAL TECHNOLOGY

Parallelism (par-ə-lel-iz-əm) *n* 1: the quality or state of being parallel. 2: the key aspect of achieving higher performance in this year's crop of microprocessors and memories at the International Solid State Circuits Conference. In the CPU arena, designers are turning to superscalar, superpipelined architectures, or even multiple processors on a chip running in parallel to attain throughputs ranging from about 50 MIPS all the way to 1000 MIPS. Faster memory chips also do more in parallel to improve overall system performance. A novel cache-DRAM allows wide-word parallel on-chip transfers between the DRAM and SRAM sections for fast updates, while a system-level superchip combines multiple DRAMs, SRAMs, and a gate array to create a monolithic memory subsystem that performs multiple memory accesses in parallel.

Advances in both CISC and RISC architecture—macropipelining, dual-instruction-issue, superscalar multiprocessor implementations—are detailed in one session. The lone CISC presentation by Digital Equipment Corp., Hudson, Mass., demonstrates how macropipelining and multiple functional units (as well as better compilers) can work together to reduce the clocks per instruction by a factor of 2.4 over a chip set described at the 1989 ISSCC. In addition to the improved instruction efficiency, the new CPU operates at about three times the clock rate of the previous processor.

A 400-MHz external ECL clock drives the on-chip clock generator. The generator creates on-chip 100-MHz four-phase internal clocks. It also creates four-phase off-chip clocks that run at about 33 MHz. These latter clocks control the bus interface, the I/O pads, and the peripheral chips that tie into the CPU. The CPU in this new implementation combines three of

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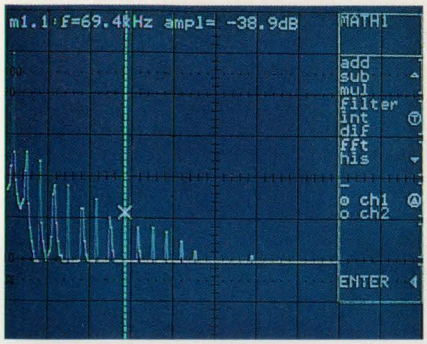

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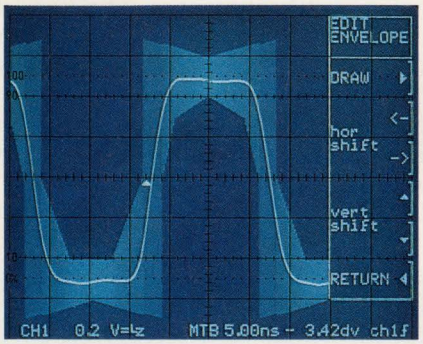

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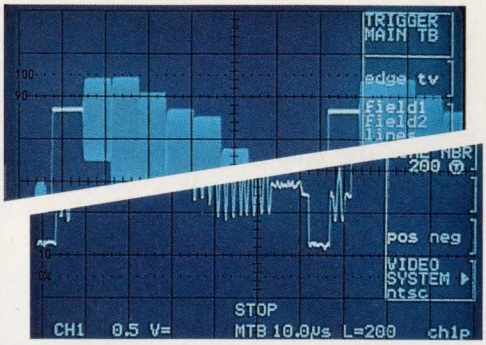

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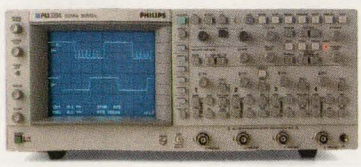

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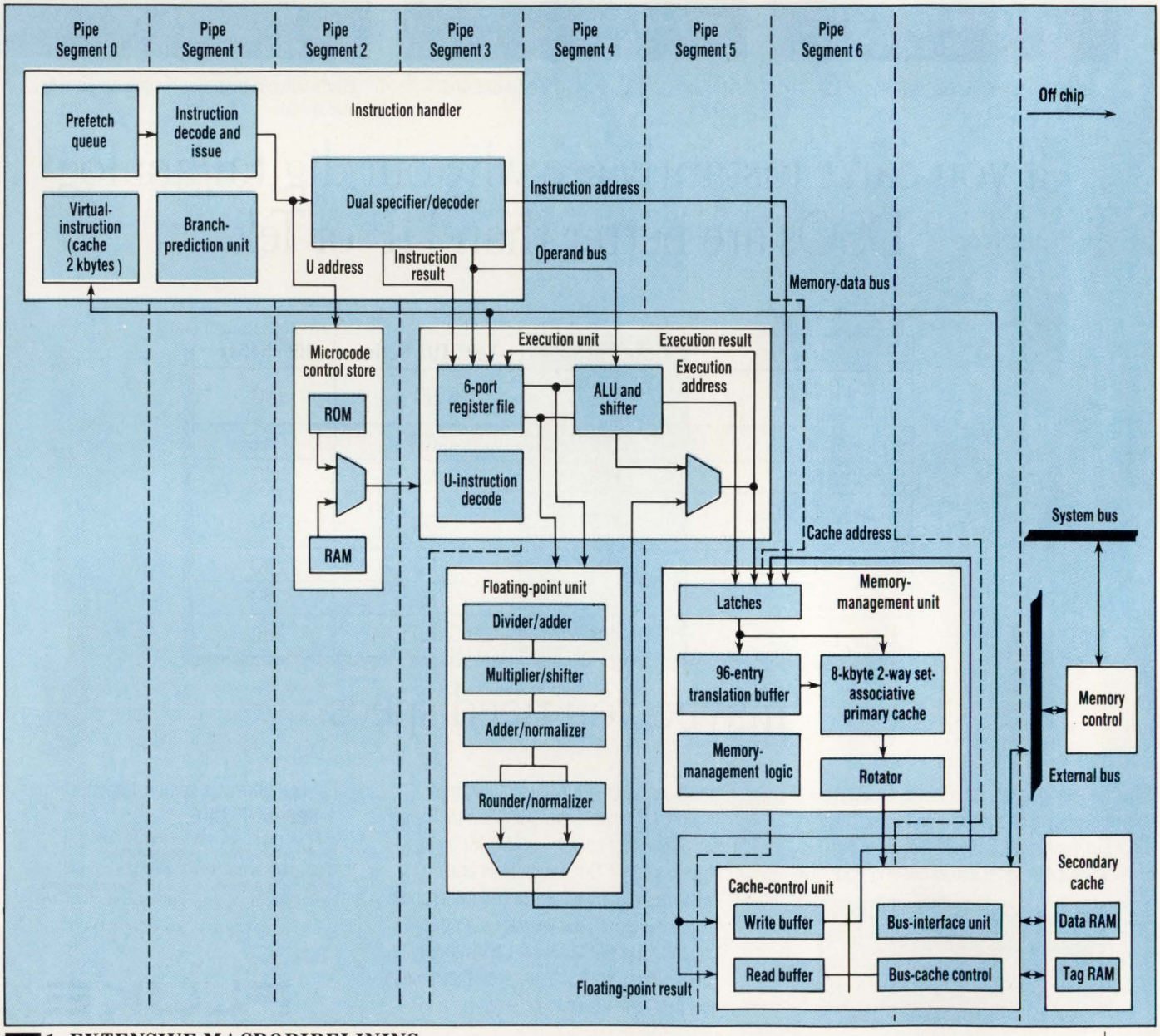
the four circuits described at the 1989 ISSCC by employing a 3.3-V, 0.75-μm CMOS process that packs 1.3 million transistors on a 1.62-by-1.46-cm piece of silicon. Three levels of metal provide dense interconnections and minimize clock and signal delays. The clocks' high speed combined with the on-chip parallelism pushes the chip's power consumption up, to a peak of 18 W, even with the reduced supply voltage.

By running the internal clocks at 100 MHz, the CMOS chip had to undergo extremely careful design, with much attention paid to node loading. A 3D capacitance extractor determined loading on every node, and a trapezoid-based extractor ascertained node resistances. The extracted R and C values were fed to a static timing verifier that traversed 350,000 signal paths and checked 42,000 timing constraints on a 500,000-transistor net list in one run. Extensive logical and electrical verifications were also done prior to silicon fabrication. From this analysis, first silicon was able to boot the operating system and run at 100 MHz. At that speed, the chip delivered a throughput rating of 50 Specmarks—the highest rating for a CISC processor to date.

To achieve the improved instruction efficiency, the processor archi-



1. EXTENSIVE MACROPIPELINING as well as micropipelining was employed by designers at Digital Equipment to maximize the throughput of all sections of a 100-MHz CISC processor. By performing multiple, overlapped operations on the chip, as well as applying some improved compilers, performance levels achieved for the CPU were 2.4 times better than an earlier CISC implementation of the chip set.

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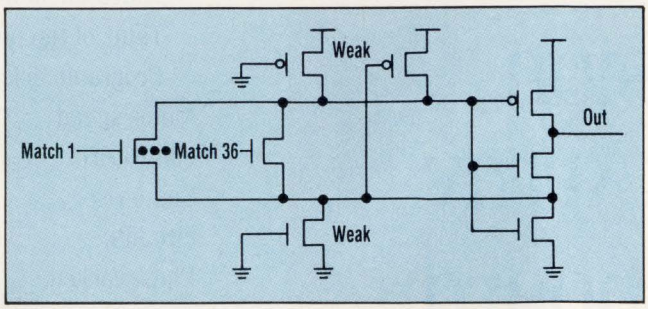
tecture is divided into six major functional units—instruction handler, control store, execution unit, floating-point execution unit, memory manager, and external cache and bus interface controller. The units are set up in a seven-segment macropipeline that allows each block to start its operations at the earliest possible time *(Fig. 1)*.

Within each block, the functions are pipelined to minimize data flow. For example, in the instruction-handler block, words are read from the prefetch queue by the instruction decoder and issue unit, which works with the branch-prediction unit and a closely coupled 2-kbyte virtual-instruction cache. The resulting command is fed to both the control store block and to an operand decoder and instruction parser (the dual specifier decoder box).

A four-stage micropipeline is also implemented by the control-store and execution units. The control store contains 1600, 61-bit-wide words (over 1700, 50-bit words were used in the 3-year-old CPU) and can be patched by employing a small on-chip content-addressable memory. Floating-point operations are done in a four-stage pipeline. Most operations have a latency of four cycles and a repetition rate of one cycle. Memory-management operations employ a two-way set-associative 8-kbyte primary cache that gets the physical address from the nearby 96-entry fully-associative translation buffer. About two cycles are needed to handle the memory-address translation and lookup.

In an effort to push the on-chip clock up to 200 MHz, another design team at DEC turned its attention to RISC architectures and a 64-bit dual-instruction-issue approach to execute 400 MIPS. The processor implements a large linear address space and includes dual 8-kbyte caches (data and instruction) and matching translation buffers. The pipelined integer execution unit contains a 32-entry register file and ties into a four-entry 32-byte/entry write buffer. The bus interface can be configured for either 64- or 128-bit widths, logic-family type (CMOS/TTL or ECL), external cache size and speed, and bus clock rate.



2. A SIMPLE DISTRIBUTED NOR circuit developed by Sun Microsystems and Texas Instruments takes all 36 address inputs. The circuit is used in the translation look-aside buffer of the SuperSparc processor to perform high-speed matching of the memory address bits.

Coupled closely to the integer unit is a pipelined 64-bit floating-point unit that contains an additional 32 registers and supports both VAX-standard and IEEE-standard data types and rounding. The bus interface control block on the chip also supports off-chip secondary caches. The processor architecture handles both 32- and 64-bit operations on an instruction-specific basis. It provides continuity to an earlier CISC architecture without sacrificing the advantages of RISC implementation.

Instruction issues support pairwise execution among combinations of the four basic functional blocks on the chip: load/store, integer operate, floating-point operate, and branch. The pipeline depth is seven cycles for everything except floating-point operations, which require ten cycles. The integer unit has a typical latency of one cycle and a load latency of three cycles; the floating-point unit has a six-cycle latency. However, the floating-point block can generate a 64-bit result every cycle for all operations except divide. Instructions are issued in order and under control of register scoreboarding logic.

Almost the same size as the CISC processor, the 1.68-by-1.39-cm device packs about 400,000 more transistors (due mostly to the larger caches), but consumes almost twice the power—30 W. The doubling of power is mainly due to the higher operating frequency. The chip is also implemented with the same 0.75-μm CMOS, triple-level metal 3.3-V process. To achieve 200-MHz operation, many novel circuit structures and detailed analysis techniques had to be applied to deal with the concurrence and wide data paths. For instance, a level-sensitive, single-phase clocking scheme was developed to eliminate any of the "dead time" that often exists with multiphase clocking.

The single-phase clocking, though, requires high clock integrity to avoid race-through in latches and clock skew contributions to delay paths. The clock, which must drive a total capacitance of 3250 pF, requires extremely large devices: the p-channel transistor has a width of 250,000 μm and the n-channel device required 100,000 μm. To better distribute the signals, the p- and n-channel driver transistors were positioned in the center of the chip.

To build a high-speed 64-bit adder, designers combined both logic and circuit techniques. The logic approach combines two schemes: A Manchester adder carries for the initial 8-bit groups, followed by a logarithmic carry-select tree. In the Manchester portion, the NMOS circuit sections are precharged low and then conditionally pulled high. That avoids threshold delays in the pass transistors and improves the carry-chain performance by about 10% over the pull-down approach.

A joint team from Sun Microsystems Inc., Mountain View, Calif., and Texas Instruments Inc., Dallas, applied biCMOS processes to high-speed RISC processors to create a CPU that runs at a 40-MHz clock frequency. Another team at Hitachi Ltd., Tokyo, Japan, created a faster CPU that runs at a 250-MHz clock frequency. Some of the joint Sun-TI efforts for the three-instruction-per-

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issue processor have already been made public at conferences in 1991, such as the IEEE Hot Chips Symposium and the Microprocessor Forum. However, the internal chip details, as yet unreleased, include a unique in-circuit emulation mechanism for remote symbolic source-code debugging, hardware that directly supports multiprocessor systems, built-in self-test logic, and internal and JTAG capabilities.

The chip, referred to as the SuperSparc processor, squeezes over 3 million transistors onto a piece of silicon just under 1.6 cm on a side. The chip dissipates about 8 W when running at 40 MHz. Incorporated on the processor are a 32-bit integer pipeline with three fully-static 32-bit ALUs, one 32-bit adder, and one shifter; a memory-management unit; a 20-kbyte instruction cache; a 16-kbyte data cache; an IEEE-compatible 64-bit floating-point unit; and the bus interface. Instructions are processed in an eight-stage pipeline that executes commands in four clock cycles. Two instruction-fetch stages, three decode stages, two instruction-execute stages, and one result write-back stage are included.

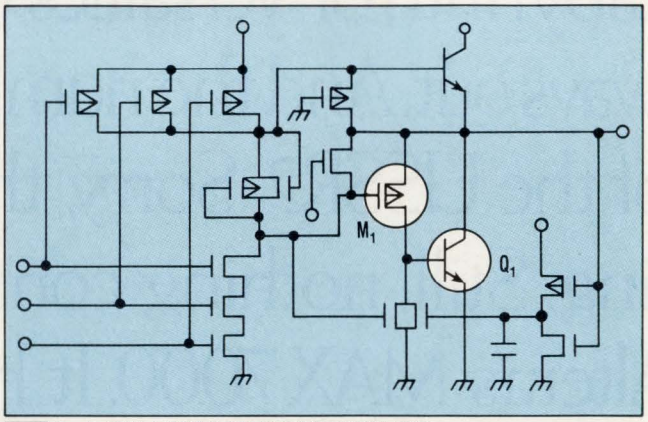
The large, 20-kbyte I cache is five-way set-associative and has a 64-byte line size. To ensure sufficient yield during manufacturing, redundant rows and columns were included in the cache. And to sustain the execution of up to three instructions/cycle, the data path from the I cache to the integer pipeline unit is 128 bits wide. The four-way set-associative D cache is also quite large. It contains redundant rows and columns, and can be configured as either a write-back or a write-through cache.

Because both the I and D caches are physically addressed, that requires the memory management unit to translate the virtual-to-physical address before the cache-set selection and alignment is done. Consequently, the 64-entry fully associative translation look-aside buffer in the MMU must be very fast. To get the high speed, static bipolar sense amplifiers are used for the memory to trim the access time to 2 ns. Furthermore, a new high-speed matching circuit that executes a distributed NOR of a match in each bit is employed. That circuit trims the time for a 36-bit match to 1.1 ns *(Fig. 2)*.

To keep data and instructions in the instruction unit ready, both a sequential prefetch queue (8 instructions) and a target prefetch queue (4 instructions) are included. Either of the queues receives up to 4 instructions from the I cache. Instructions are issued out of the queue in single, double, or triple instruction groups and operate on a 136-word, 32-bit, 4-port register file, which performs two reads and two writes or four reads in a single clock phase. The register file is time-shared, and also serves as a six-read, two-write port memory each clock cycle.

A biCMOS companion chip for the CPU, a cache controller, supports up to 2 Mbytes of direct-mapped secondary cache, as well as an interface with two multiprocessor busses. An on-chip synchronous tag RAM, organized as 8 kwords by 33 bits, includes redundant rows and columns and consumes all but 500,000 of the 2.2 million transistors. One of the two buses is the 64-bit MBus extension, a circuit-switched multiprocessor bus operating at TTL levels. The other is the XBus, a local packet-switched bus operating at either TTL or GTL (Gunning-transceiver logic) levels with 1.2-V logic swings.

In the XBus mode, the controller chip connects to multiprocessor buses through special bus-watcher chips. Up to four bus-watcher chips can be connected to tie the controller into four multiprocessor buses. At any instant, the controller can handle multiple operations—for example, one read miss, one write miss, and up to 30 pending writes at the same time. Special hardware support is included for block-copy and block-zero operations.



3. A QUASICOMPLEMENTARY biCMOS structure, demonstrated by this three-input NAND gate designed by Hitachi, can operate at twice the speed of similar CMOS circuits when either is powered by 3.3 V. The PMOS device (M_1) drives the base of the pull-down npn bipolar transistor (Q_1), improving the gate speed.

By pushing biCMOS to clock rates of 250 MHz—the fastest yet for a silicon microprocessor—designers at Hitachi created a dual-CPU superscalar processor that runs at 1000 MIPS. The chip, implemented with 0.3-μm features, measures just 8 by 8 mm, and represents the most-complex logic chip yet (excluding memories) implemented with such small feature sizes. Each 32-bit processor executes two instructions per clock cycle, and includes an 8-port 32-word register file, two 32-bit ALUs, a 30-bit program-count adder, and about 3500 gates of control logic.

The chip also holds four primary caches, each containing 1 kbyte of two-way set associative memory and four translation look-aside buffers (64 entry, two-way set-associative), to supply data and instructions to the CPUs. In addition, each CPU shares a global secondary cache—8 kbytes set up as four banks of two-way set-associative memory. In each processor is a five-stage pipeline, with most stages implemented in a quasi-complementary biCMOS structure that was described at the 1991 IEEE Symposium on VLSI Circuits *(Fig. 3)*. Thus, the chip can operate from a 3.3-V supply.

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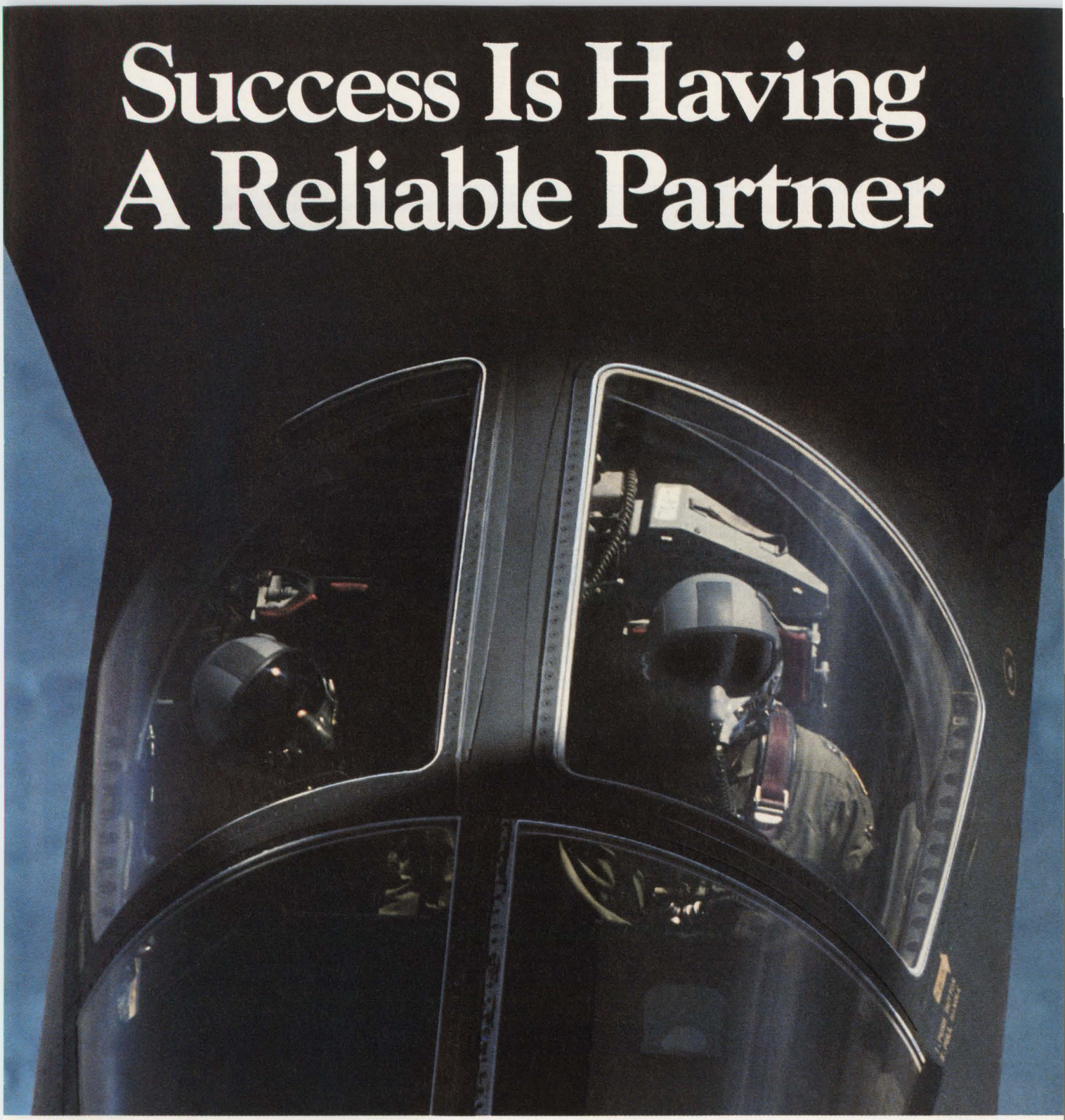

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chip supercomputer designed by Fujitsu Ltd., Kawasaki, Japan, employs 0.5-μm CMOS technology and runs at a clock rate of 70 MHz. To get the high throughput, chip designers employed a single-instruction, multiple-data processor (SIMD) approach by implementing multiple vector pipelines, all of which can operate concurrently.

The vector unit contains the multiple vector pipelines as well as 8 kbytes of vector registers, a 64-byte mask register, and a 128-byte scalar register. The vector processor employs a four-way bank structure for the vector registers. The structure permits the parallel operation of four pipelines—add, multiply, divide, and a load/store unit. Furthermore, each vector register (VR) has a basic structure of 8 bytes by 16 vector elements by 64 registers. Each VR can be divided into 8, 16, 32, or 64 partitions, depending on the vector length set in a vector-length register. At 70 MHz, the SIMD processor can perform 149 MFLOPS of double-precision computations or 289 MFLOPS of single-precision calculations.

A complex microprocessor is typically supported by an equally complex memory subsystem consisting of secondary cache and high-capacity DRAM. To simplify that subsystem, Hitachi researchers integrated the DRAM and SRAM together on a "superchip," creating a "System ULSI." On one piece of silicon, they integrated a full memory subsystem containing 44 Mbits of DRAM (eleven 1-M-by-4 DRAMs), 384 kbits of SRAM (six 16-k-by-4 SRAMs), and 18 kgates of custom logic. The DRAMs can be accessed in just 65 ns, while the SRAMs can access their contents in just 14 ns.

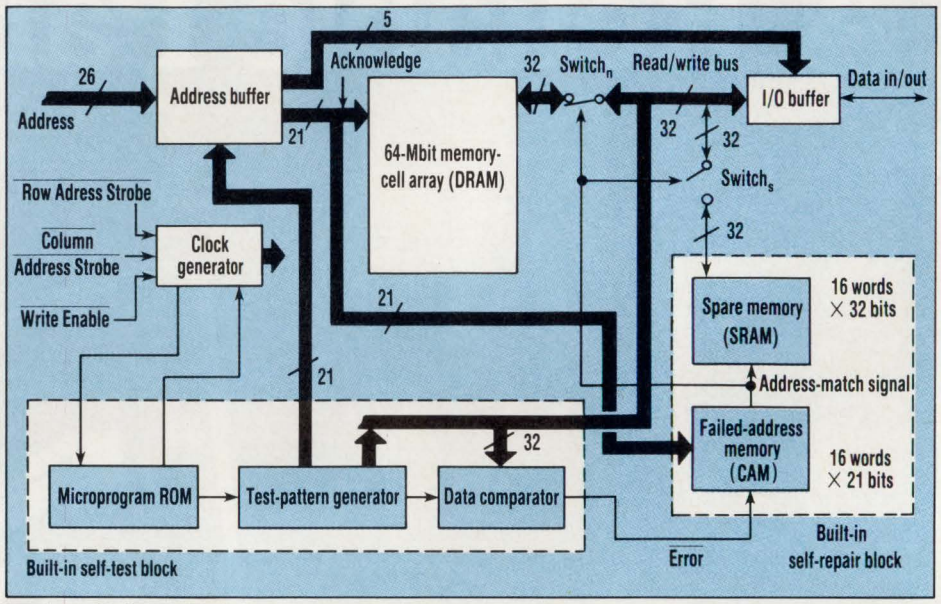
Both intra and interchip repair schemes are included to improve yield on the huge 3.816-by-5.04-cm chip. The intra-device repair switches off failed blocks. For the memory chips, just 23 DRAM I/O lines are needed out of a possible maximum of 44 existing lines. Thus, the on-chip logic will be set up to switch off defective elements and route the best 23 I/O lines from the DRAMs to the outputs. Similarly, it selects the best 16 I/O lines of the 24 possible for the static RAMs. Inter-chip repair tries to mix and match good blocks of memory amid all of the DRAMs or SRAMs to achieve the desired memory capacity.

On a smaller scale, designers at Mitsubishi Electric Corp. have done the same type of integration by combining a 4-Mbit DRAM and static RAM cache on one chip. The DRAM section, organized as 1 M by 4, ties directly into a 4-k-by-4 SRAM block. The close coupling of the DRAM and SRAM allows 16 words to be written simultaneously from the DRAM to the SRAM, or vice versa. As a result, the cache-miss penalty for the DRAM update time is reduced drastically. When a cache hit occurs, data can be transferred out of the SRAM block at 100 MHz (10 ns per nibble), allowing fast data bursts to update primary caches that typically reside on the processors *(see "Intgegrated Cached DRAM Lets Data Flow at 100 MHz," p. 142).*

Large DRAMs are usually a hot subject at ISSCC, but this year seems to be the year between generations. The one lone high-density DRAM discussion comes from the Microelectronics Research Laboratories of NEC Corp., Kanagawa, Japan. The company described a 64-Mbit memory implemented with a 0.4-μm CMOS process that packs several circuit improvements. It can access in just 30 ns, operate from 3 V, and even test and repair itself.

Mask-configurable as either a 64-M-by-1 or 16-M-by-4 memory, the chip employs a latched-sense/shared-sense circuit with open-bit-line readout and folded bit-line rewrite operations that reduce inter-bit-line coupling noise. Alternatively activated and separately end-located word drivers and X decoders help reduce word-line selection delay time. Built-in self-test (BIST) and repair using spare memory cells extend chip usability and reduce test costs. At last year's ISSCC, the company described a BIST approach that uses an on-chip microprogram ROM.

By extending that approach to in-



4. IN ADDITION to incorporating on-chip self-test circuits, a 64-Mbit DRAM developed by NEC includes spare memory cells that can be switched in if the self-test block detects any failed bits. When a failed DRAM bit is detected, the error signal generated by the data comparator activates the match line in the failed address memory. That line then activates the spare memory cells whenever the address for the defective cells is sent to the main DRAM array.

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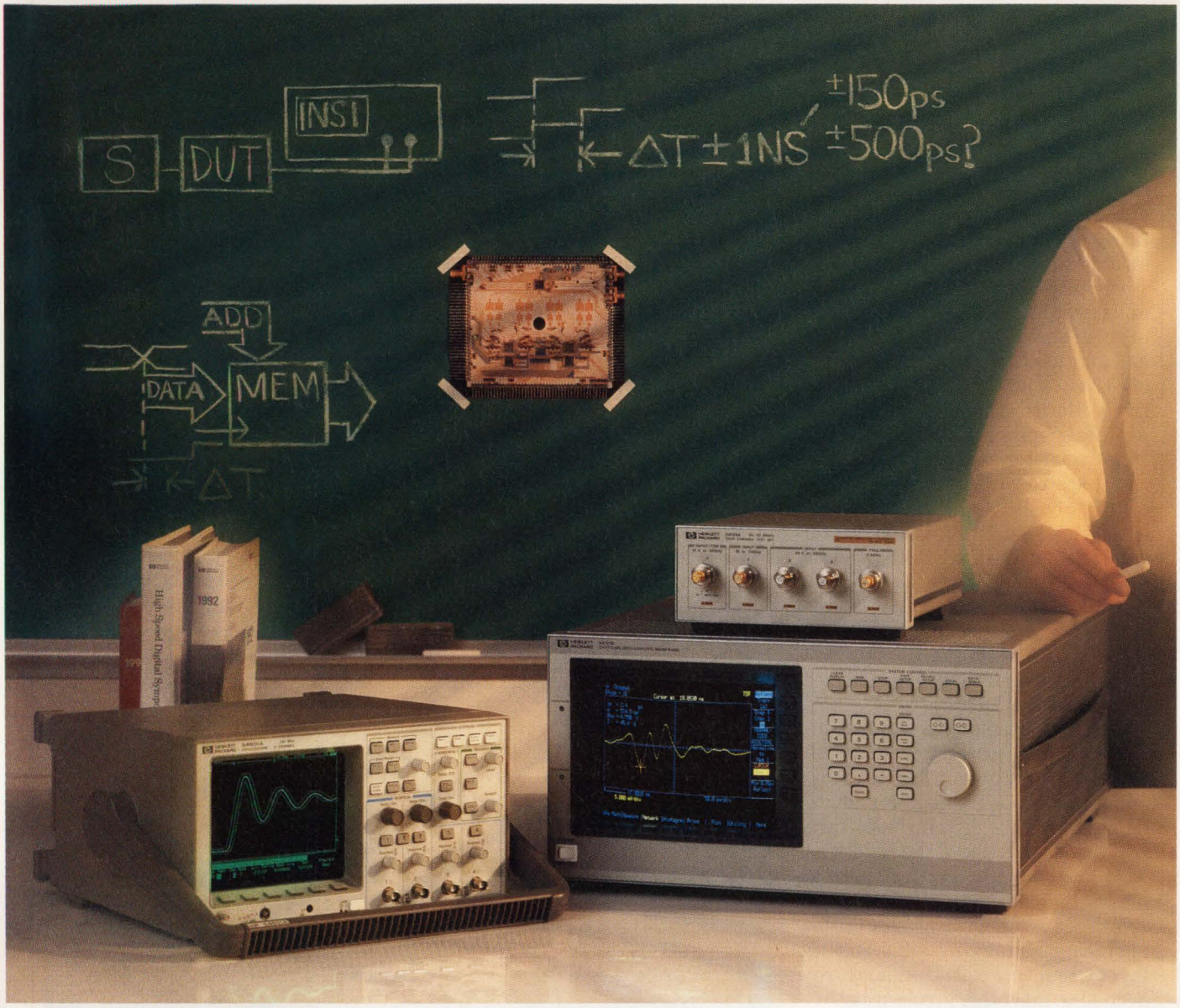

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clude some repair circuitry, DRAM chips could remain operational significantly longer *(Fig. 4)*. When the BIST section detects a failed bit, it stores the address in a special block called the failed-address memory. When an access to the same address is attempted during normal operation, the failed-address memory generates an address-match signal that turns off the usual I/O signal and switches in the spare memory cell.

Packing about the same number of devices as a 64-Mbit DRAM, a pair of 16-Mbit SRAMs, one from NEC and another from Fujitsu, allow data accesses of just 12 and 15 ns, respectively. Both are implemented in a 0.4-μm CMOS process and employ thin-film-transistor active loads rather than passive-resistor loads. Four levels of polysilicon and two metal layers form the active loads and interconnects on NEC's SRAM. Fujitsu adds a fifth layer of polysilicon to employ a special split-gate p-channel load element. A rather large 1.83-by-1.25-cm chip holds the 16-Mbit NEC memory, while Fujitsu's SRAM measures 1.04 by 2.15 cm.

The NEC memory is organized as 2 M by 8 and operates from a 3.3-V supply, drawing about 90 mA when running at 30 MHz and just 800 nA on standby. The chip includes three test modes that check the redundant rows and columns, and perform a 16-bit parallel memory test. The memory's design was optimized for the low operating voltage by adjusting the layout, memory-cell positioning, row decoding, and other structures.

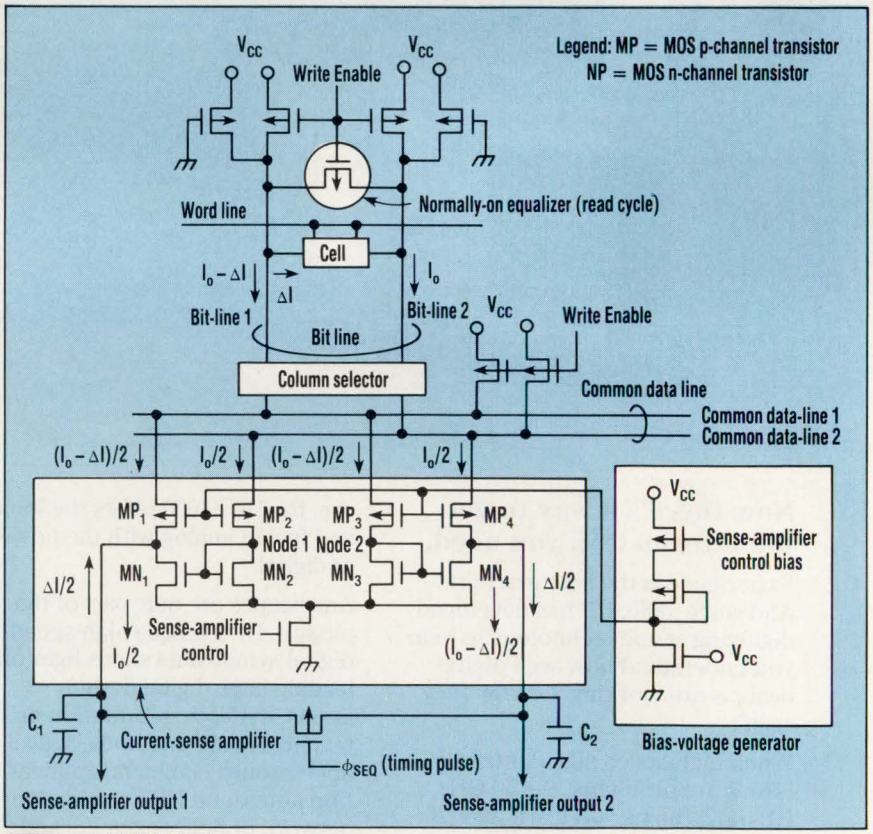
Opting for a 4-M-by-4 organization, Fujitsu designers kept the access time low by using a hierarchical sense amplifier and a reduced-voltage-amplitude data bus. The thin-film p-channel transistors used for active loads have dual gates and help keep the memory's standby current to about 1100 nA. The gate electrodes are formed on the second and fourth polysilicon layers and their channels on the third polysilicon layer. An interdigitated approach for bit-line pairs, alternately connected to either upper or lower groups of data-bus lines, minimizes data-bus line length and improves access time.

Although 4-Mbit SRAMs are already being sold, they're still being refined to become faster and smaller. Both NEC and Toshiba have applied biCMOS technology to the dense SRAMs to push access times down to just 6 and 9 ns, respectively.

NEC designed the I/O lines to provide 100K-family ECL compatibility for minimal off-chip to on-chip (and vice versa) signal delays. With a mask option, the company can switch the part to TTL-compatible I/O, which adds just 2 ns to the access time. A 0.55-μm triple-well biCMOS process was used to fabricate the chip. An on-chip voltage converter provides a –3.3-V secondary-supply voltage that's isolated from the primary –4.5-V supply. Furthermore, special attention was paid in the design to the ECL-to-CMOS level converters to minimize signal delays.

Optimized for wide-word TTL systems that operate at 3.3 V, the Toshiba SRAM is organized as 256 k by 16. Even with the wide words, it keeps its power consumption low—just 430 mW when operating at 50 MHz and 3.3 V. To maintain the low power, the chip was designed with biNMOS gates for the decoders and control circuits, which provide good performance with low supply voltages. A triple-polysilicon, double-metal half-micron process is used. The first polysilicon layer is used for the gate electrodes of the MOS devices The second polysilicon layer is actually a polycide and is employed for the emitter electrodes and for ground lines of the cell array. The third polysilicon layer holds the resistor loads for the memory cells.

Although speed usually comes at the expense of power, designers at Hitachi managed to trim the power of a 7-ns 1-Mbit SRAM to just 140 mW when operating at 100 MHz from a 3-V supply. In comparison, previously reported sub-10-ns RAMs have typically had power require-



5. A SPECIAL current-sense amplifier was incorporated by Hitachi designers into their ultra-low power (140-mW) high-speed 1-Mbit static RAM. The sense amplifier turns the small current difference between paired bit-lines (the common data lines) into a large voltage swing.

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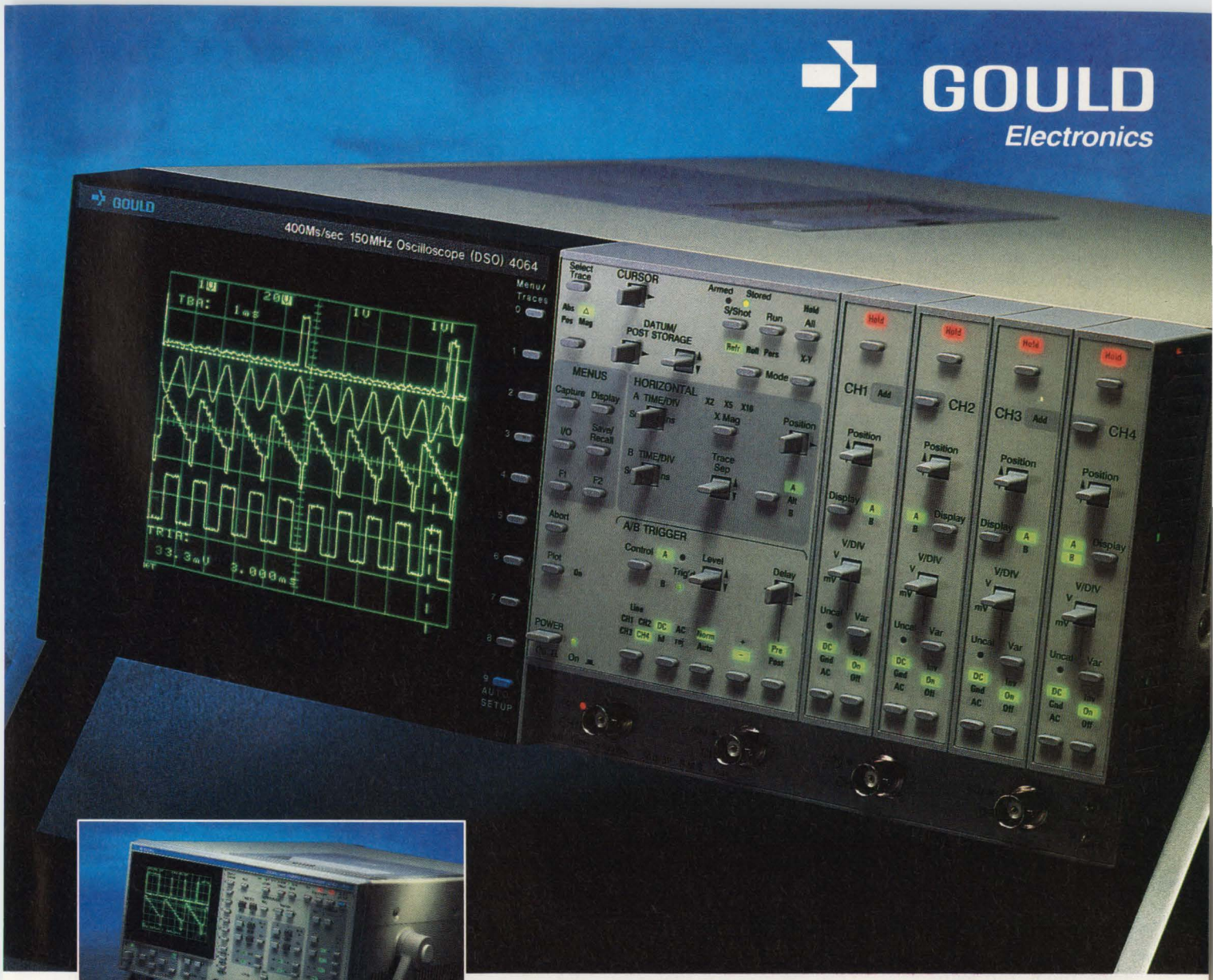

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CIRCLE 104 FOR U.S. RESPONSE

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ments of well over 500 mW. Fabricated with 0.3-μm features, the four-polysilicon, double-metal part is organized as 256-k-by-4 and delivers a 2-V swing. To get the low power, designers created a current-sense amplifier and a special pre-output buffer. The amplifier provides good amplification for a small voltage swing close to the supply voltage, because it converts the small current difference between paired bit lines (common data lines) into a large voltage swing *(Fig. 5)*.

Operation from a 3-V supply is fine for many applications. But as weight requirements migrate to even lighter systems that require single-cell operation, chips running from a 1-V supply will be needed. Looking into that future need, Hitachi researchers developed the first experimental 1-V SRAM that employs thin-film-transistor loads rather than passive loads. Although the chip designed by the researchers was only 4 kbits, the same design rules could let them fabricate a 4-Mbit device with a chip area of 75 mm^2 and a 700-nA standby current.

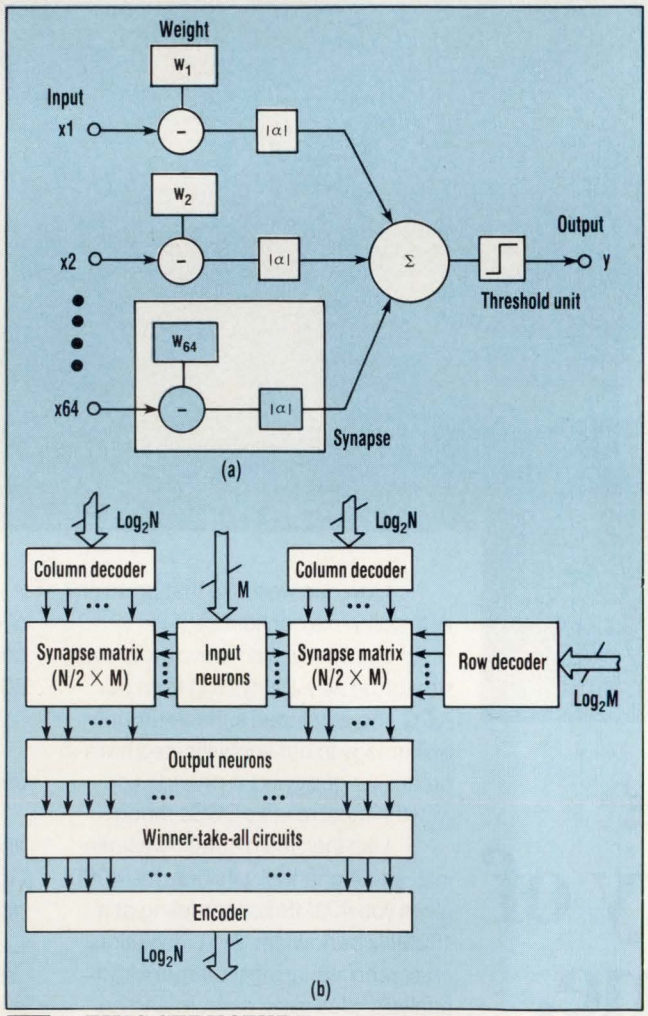
To operate from a 1-V supply, the memory uses a two-step word-voltage scheme, a level-shift sense amplifier, and a low-current (230-nA) boosted-level generator. The two-step scheme first raises the word voltage to almost the supply voltage level, as set by the decoders. The voltage can then be increased to a level higher than the supply voltage. That's accomplished by switching the voltage created by the boosted-level generator onto the word line through a p-channel device controlled by an internal memory-access timing signal. Consequently, enough potential is given to activate the cell.

Efforts to reduce the operating power-supply levels adversely affects current-generation flash memories, because they typically require a 12-V programming level. Reducing the external programming voltage to match that of today's 5-V power-supply level will start the ball rolling toward a 3-V-only part, which will most likely emerge sometime in the next few years. At this year's conference, both Toshiba and NEC detailed 5-V-only flash memories implemented in 0.6-μm CMOS—a 4-Mbit device for Toshiba and a 16-Mbit unit with sector-erase capability from NEC.

The NEC chip employs a 512-word (1024-byte) sector and the memory array architecture is switchable between 1-M-by-16 and 2-M-by-8 organizations. To reduce programming-voltage requirements, designers optimized the memory cell and developed a channel-erase mechanism. The channel-erase approach applies positive pulses to the channel area and negative high-voltage pulses to a control gate through a new row-decoding scheme. Programming time is 5 μs/word with a 5-V drain level and a 12-V gate voltage. On-chip circuits generate the 12-V level from the 5-V supply. The chip's total erase-verify time is about 2.7 seconds. When the auto-erase mode is used, a maximum time of 4 seconds is needed.

Another approach that focuses on shrinking row decoders involves a triple-well process, a process that has led to the creation of a 4-Mbit test device from Toshiba. The triple-well row-decoder design keeps the voltage stress on the transistors to less than 10.5 V for erase and program operations (a conventional row decoder could see stresses of up to 15 V). That allows the use of small, thin-oxide devices and eliminates the need for the p-channel transfer gates that provide negative-voltage isolation. Thus, circuits with the tightest pitch possible can be fabricated, in addition to saving 30% of the area. Redundant memory columns, controlled by EEPROM storage cells, are also included on the chip.

Neural-network technology, which falls some-



6. THIS STRUCTURE, which has one of thirteen neurons on its digital neural network chip, implements what Nippon Telegraph and Telephone calls a polyhedric-discrimination-neuron model (a). It contains 64 synapse cells, each containing an 8-bit weight memory, an 8-bit subtracter, absolute-value gates, control logic, and an 8-bit adder. Employing a winner-take-all analog computing approach, a chip developed at the University of Southern California uses many Gilbert multipliers to perform parallel computation of many dot products in the synapse cells (b).

where between memory and microprocessors, has become a regular part of the conference program. Only one of the four papers this year, from Nippon Telegraph and Telephone Public Corp., Atsugi, Japan, focused on digital implementations of neural-network technology. The others, from the University of Southern California, Los Angeles, Toshiba, and Mitsubishi Electric, highlighted analog implementations.

The digital circuit developed by NTT can perform 8 Gconnections/s while consuming just 54 mW. To achieve the high connection rate at such a low-power level, designers created a neuron cell based on a polyhedric-discrimination-neuron (PDN) model and a low-power chain-reaction (LCR) architecture. The PDN model employs a local-representation structure that contains modified elements of radial-basis-function and restricted-coulomb-energy models. The modifications were done to minimize the number of transistors needed for the synapse units. In addition, the chip's equivalent-gate count is kept to just 155,000 gates.

In the neuron model, 64 inputs are fed through 64 weights (one in each of 64 synapse units), then the resultant values are summed and fed into a threshold unit that performs the evaluation *(Fig. 6a)*. Each synapse unit consists of an 8-bit memory, an 8-bit subtracter, absolute-value gates, control gates, and an 8-bit adder that uses about 700 transistors.

By employing 0.8-μm features, designers integrated 832 digital synapse units with 8-bit weights onto the CMOS chip. That level of integration translates into 13 neurons on a 10.3-by-14.1-mm chip with a forward propagation time of 104 ns—the fastest reported for a digital neural-network implementation operating at 3 V. At 5 V, the chip performs 13 Gconnections/s and has forward propagation time of just 64 ns. The combination of the PDN model for the cells and the LCR architecture results in a circuit that offers improvements in power dissipation and computational speed, almost two orders of magnitude better than conventional approaches like multilayer perceptrons and learning-vector quantization.

The LCR architecture uses three circuit techniques. The first is an automatic stop scheme for the calculating circuits. Second is a fully implemented digital synapse; each synapse block has a calculating circuit and embedded-weight memories. Third is self-control operation without internal clocks. Automatic stop operations are controlled by carry signals of the summing adders, using control gates on signal paths.

Mixed digital and analog techniques are applied by Toshiba on a neuron chip set with on-chip back propagation and/or Hebbian learning. By dividing the synapse and neuron control functions into separate chips, Toshiba designers created an expandable scheme based on the two circuit types. This approach is an extension of the two-chip architecture described at last year's ISSCC. In the new neuron circuit, 24 neurons are integrated together, while the synapse chip contains nine synapse groups and differential-to-single-ended converters to minimize I/O pin count. Synapse circuits, which measure 6.8 mm on a side and have 148 I/O pins, contain about 150,000 transistors. The neuron circuits employ just 11,000 transistors on 6-by-6-mm chip with 136 I/O pins.

Optimized for pattern-mapping applications, an experimental analog neural-network processor with a self-organizing algorithm was developed at the University of Southern California and partially funded by the Defense Advanced Research Projects Agency (DARPA), NKK Corp., Samsung Electronics, and TRW Inc. The network produces spatially organized representations of aspects of the input signals—ideal for such applications as image and vision processing by pattern recognition and vector quantization. In this type of network, competition is performed within a "winner-take-all" function that's fed by an array of neuron outputs. Those neuron outputs are generated by the input signals going through a synapse matrix and an input neuron block *(Fig. 6b)*.

The analog neural network performs the parallel evaluation of a large number of dot products that are generated by the input vectors and stored weight vectors. Lateral competition is performed among the analog output voltages, and the neural unit with the largest voltage level becomes the single winner. Each input synapse cell is built from a wide-range Gilbert multiplier, with the weight value that's stored on the gate capacitance of a MOS transistor refreshed periodically. The summed current is linearly converted to a voltage in a summing amplifier that has the linear feedback resistance implemented by six MOS transistors. Fabricated with 2-μm design rules, the analog circuit packs 25 neurons in the input layer and 64 neurons in the competitive layer. When clocked at 4 MHz, the circuit produces 3.33 Gconnections/s.

Packing 400 neurons and 40,000 synapses on one chip, researchers at Mitsubishi were able to achieve 2 teraconnections/s (1 bit by 5 bit) and a learning speed of 80 Gconnection updates/s. The 1.45-cm-on-a-side circuit was implemented with 0.8-μm design rules in a double-metal, double-polysilicon process. It has a throughput time (pattern input to recalled pattern output) of just 3.5 μs. To get that throughput, researchers first set up the chip architecture in four main sections—a Boltzmann-machine main network, a three-layer feedforward sub-network, control logic, and the I/O drivers.

Synaptic weights are represented by charges stored on capacitors. The charges must be refreshed, giving rise to the description of the synapse as a dynamic synapse. Each dynamic-synapse unit contains a learning control circuit and weight modifier that follows the Boltzmann-machine learning algorithm. The learning algorithms have a 2-μs period for each teach pattern, and a refresh time of less than 300 μs. This chip, though, is also the most power-hungry of the four chips, consuming about 4.5 W.□

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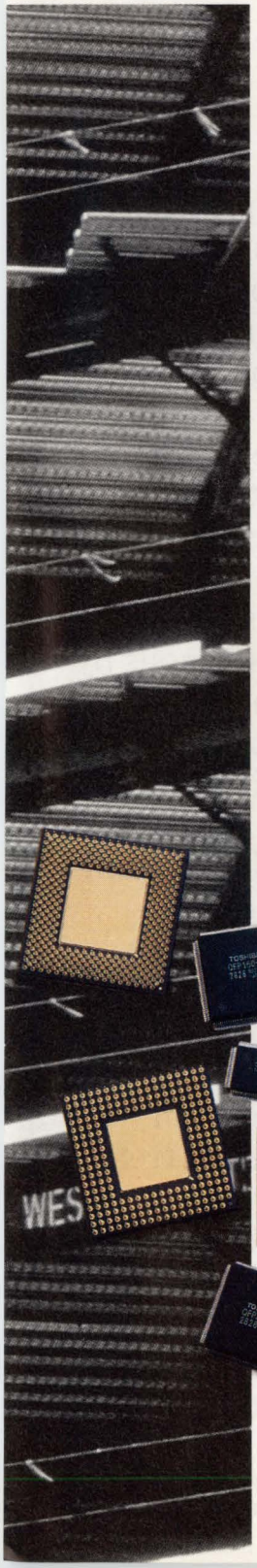

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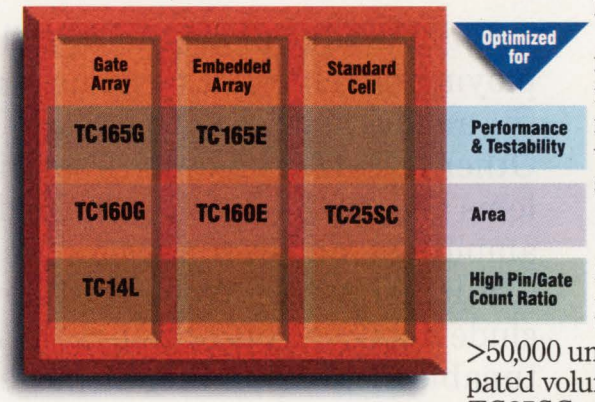

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CIRCLE 172 FOR U.S. RESPONSE

CIRCLE 173 FOR RESPONSE OUTSIDE THE U.S.

BY
FRANK
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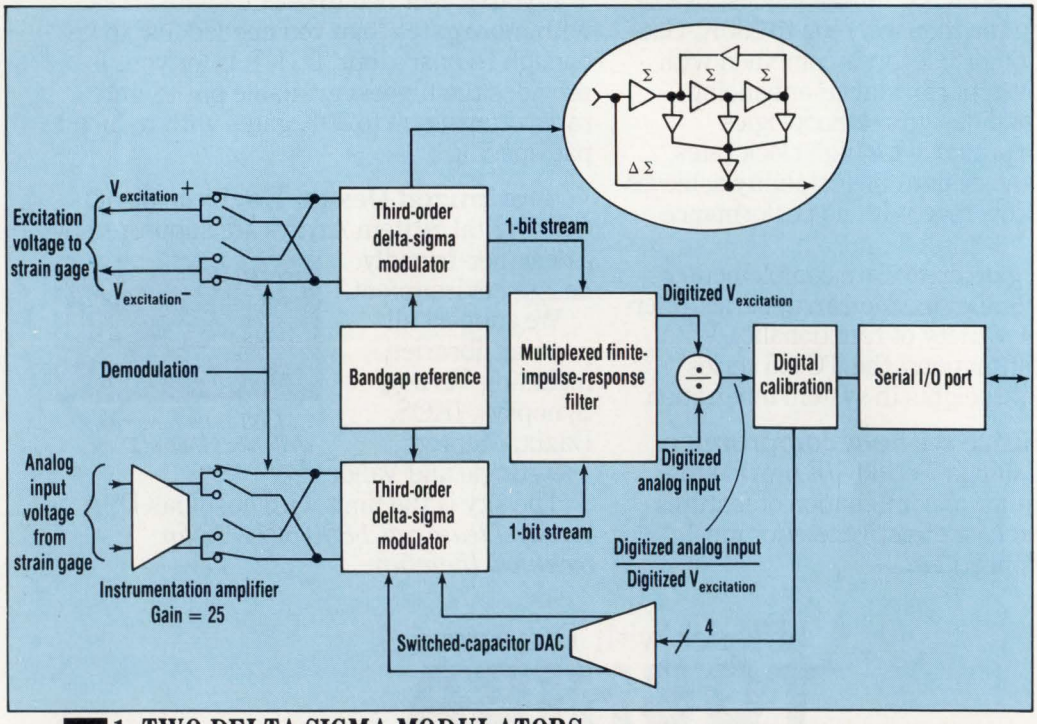
ISSCC

ANALOG TECHNOLOGY

Eight unique analog-to-digital converter designs, all employing novel circuit techniques and architectures, dominate the analog portion of this year's ISSCC technical program. Other ICs offer innovative solutions to longstanding problems and can be found embedded in filters, op amps, sampling amplifiers, and even sensors.

Further analog-technology developments at the ISSCC include improved disk-drive read circuits, an implantable and tunable 27-to-51-MHz transmitter, and a micromachined nerve stimulator. On the other hand, though, developments in digital-to-analog converters and analog multipliers seem almost conspicuous by the absence of any presentations within the ISSCC technical program. And outside of telecommunications, developments in complex mixed-signal ICs are likewise few and far between in the ISSCC program.

The upstart trend of a few years ago, which involved replacing single-ended circuits in the signal path with differential circuits, now



1. TWO DELTA-SIGMA MODULATORS developed by Crystal Semiconductor sample the excitation voltages for, and the analog input voltage from, a strain-gage transducer to create a 22-bit (serial) digital word. The word represents the ratio of strain-gage excitation to its output.

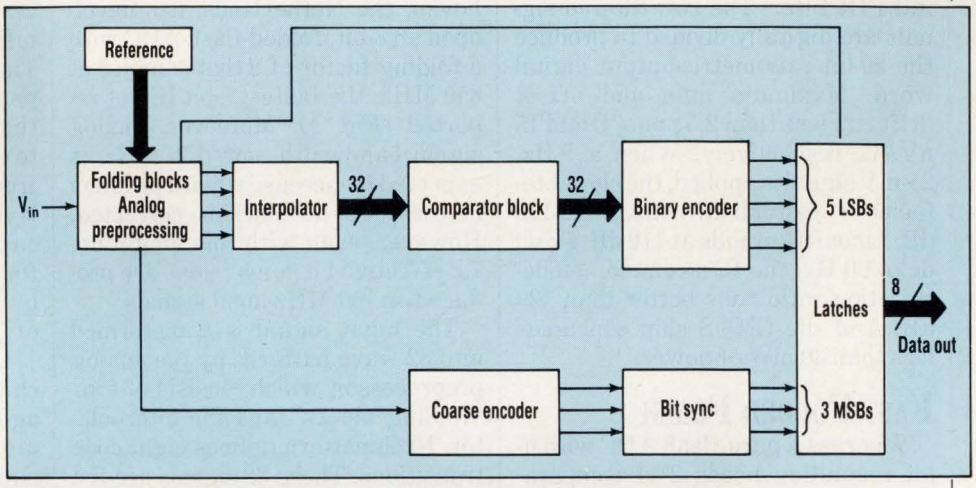
CIRCLE 124 FOR U.S. RESPONSE →
CIRCLE 125 FOR RESPONSE OUTSIDE THE U.S. →

dominates analog-IC developments at the ISSCC. Using twice as many active devices in the signal path may raise die size, but is more than offset by reduced common-mode errors and an increase in dynamic range for a given supply voltage. Its wide use has certainly been aided with the move to finer device geometries and thus smaller transistors. Powerful new circuit design, simulation, and layout tools have also impacted on the creation of more complex differential circuits.

In the world of analog-IC design, the ADC may well offer designers the biggest challenge in terms of architectural and circuit innovation. The eight ADCs at this year's conference certainly bear that out. They run the gamut from a 650-MHz 8-bit flash ADC that needs a mere 850 mW of power, to a 20-bit delta-sigma machine which oversamples at a low 19.2 kHz. In between lie a trio of 12-bit converters serving up sampling rates between 5 and 20 MHz, a 10-bit 50-MHz converter, a 500-μs converter offering 17-bit resolution, and an 8-channel, 16-bit, charge-to-digital (C-to-D) converter developed to acquire CCD signals. This last converter offers 600-electron resolution and incorporates an on-chip signal processor. As can be expected, bipolar processes are employed for designs with sampling rates above 5 MHz, while CMOS and biCMOS processes are called upon at 5 MHz and below.

Architectures for the eight ADCs are as diverse as their performance levels. Three of the ADC designs include two-step architectures. Other architectures include delta-sigma, pure flash (albeit folded), algorithmic, and ripple-through designs. There's also the aforementioned C-to-D converter that employs a floating-point architecture.

It's worth noting that while merchant-market successive-approximation-register (SAR) ADCs continue to proliferate, they haven't been reported on at the ISSCC for several years. Integrating converters are also long absent (unless delta-sigma converters can be considered integrators). And unlike the past few ISSCCs, developments in video-speed 8- and 10-bit CMOS devices are not to be found.



2. THIS 8-BIT, 650-MHz FLASH ADC employs a folded architecture in which analog pre-processors produce the three most-significant bits. The technique, devised by Philips Research, cuts the comparator count from 255 to 32, reducing power to 850 mW and overall die size.

STRAIN-GAGE ADC

A unique ADC development comes from Crystal Semiconductor, Austin, Texas. The company's 20-bit oversampling delta-sigma converter digitizes the 30-mV full-scale output voltages from strain gages employed in ratiometric applications, such as super-market check-out-counter scales. Besides offering rejection of 50/60-Hz noise (provided by the oversampling converter's digital finite-impulse-response filter), the design addresses the problems of low-noise amplification, amplifier and circuit drift and aging, as well as interference modulation (intermodulation distortion) *(Fig. 1)*.

To eliminate the drift errors (offsets) caused by thermocouple junctions between the strain gage and the converter (which is potentially many times a system's least-significant-bit value), the strain gage is excited with an ac (chopped) voltage, $V_{excitation}+$ and $V_{excitation}-$. The drift is removed by modulating these out-of-band offsets when the transducer's excitation voltages are demodulated by the ADC IC. A fixed-gain instrumentation amplifier increases the millivolt-level signal from the strain gage 25-fold. The signal is further amplified in the delta-sigma converter by user-selectable factors of 1, 2, 4, or 8. For weighing-scale applications, the 4-bit switched-capacitor DAC within the ADC removes typical offsets (up to 200% of the strain-gage's full-scale output) created by the weight of the pan.

In the past, the strain-gage-excitation voltage was used as the converters' reference voltage to produce a ratiometric output signal. Noise (interference) picked up on the excitation and strain-gage outputs intermodulate both the signal and the reference, causing dc errors when they're demodulated and ratioed. As a result, the reference is typically filtered prior to analog-to-digital conversion. However, filtering a demodulated excitation voltage in the analog domain can introduce a drift component due to temperature-dependent transition times of the external ac excitation.

To avoid such interference and drift, the ratioing and filtering in this converter are performed digitally. Two third-order, delta-sigma modulators running at 19.2 kHz independently sample and quantize the amplified strain-gage output as well as the excitation, with respect to an internal bandgap reference. Interference and out-of-band signals are removed from the modulators' 1-bit bit-stream by a time-multiplexed dig-

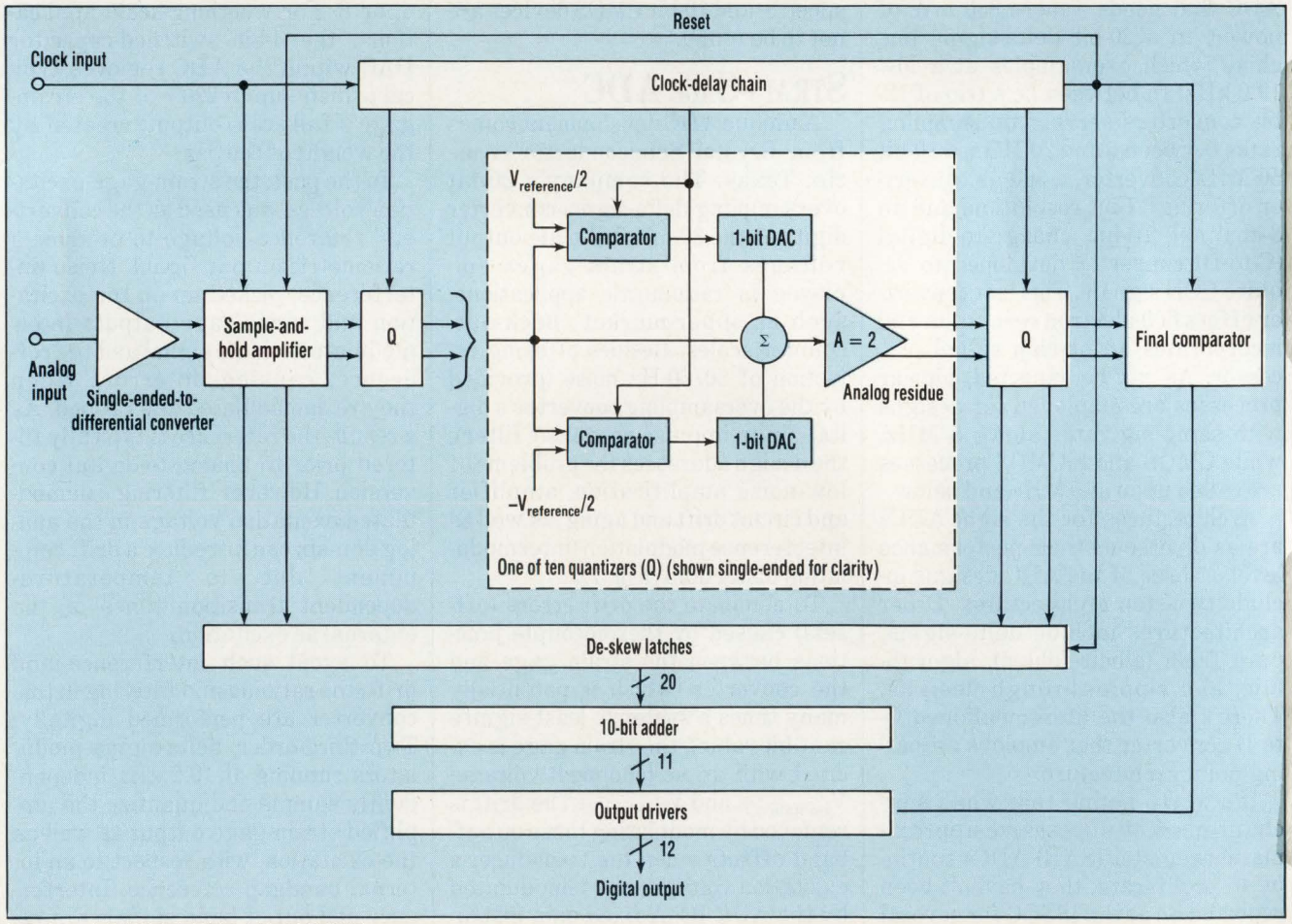
ital FIR filter. The two filtered signals are digitally divided to produce the 20-bit ratiometric-output digital word. Maximum gain and offset drift run less than 2.5 ppm/°C and 15 nV/°C, respectively. When a 5-Hz, 25-mV signal is applied, the signal-to-(noise + distortion) ratio runs 100 dB. Linearity stands at 110 dB. From dc to 60 Hz, the IC's common-mode-rejection ratio runs better than 130 dB. And the CMOS chip consumes less than 30 mW of power.

Fast Folded Flash

Whereas a pure-flash ADC with n-bit resolution needs 2^n-1 comparators, a folding converter requires significantly fewer comparators as defined by the relationship $2^n/M$, where M represents the folding factor. Such an architecture can cut chip size and power as it increases speed. Philips Research Laboratories, Eindhoven, the Netherlands, has developed an 8-bit, folded-flash ADC with a folding factor of 8 that samples at 650 MHz, the fastest 8-bit IC yet reported *(Fig. 2)*. Moreover, analog signal bandwidth, now 150 MHz, is expected to increase when a problem in the bit-sync block is corrected. However, even with this limitation, 7.8 effective-bit conversions are produced on 150-MHz input signals.

The input signal is transformed into 32 wave patterns by the analog preprocessor, which consists of four "folding blocks" and the interpolator. Each pattern defines eight code transitions. These 32 signals are fed to the comparator block that consists of 32 master/slave flip-flops, generating a 32-bit cyclic (gray) code. The flip-flops are then converted to the five LSBs by the binary encoder. At the same time, additional information coming from the analog preprocessor is converted to the 3 most-significant bits by the coarse encoder. The signal delays through the independent analog circuits generating the 3 MSBs and 5 LSBs differ enough to cause errors while digitizing high-frequency input signals. These delays are de-skewed in the "bit-sync" circuit. Additional circuitry corrects for "wrong" comparator decisions by averaging the outputs of each set of three adjacent comparators.

Like old soldiers, old converter architectures never die. About 15 years ago, Computer Laboratories (now a division of Analog Devices) announced some of the first 8-bit video-bandwidth ADCs. These large modules employed a "ripple through" architecture that needed just one comparison per bit. Now a modified version of the same architecture has been implemented by Hewlett Packard Co., Palo Alto, Calif., to put a 20-



3. A MODIFIED VERSION of the classic "ripple-through" architecture, developed by Hewlett-Packard, has produced this 12-bit ADC, which samples at 20 MHz. Needing just 21 comparators, its signal-to-(noise + distortion) ratio runs 64 dB.

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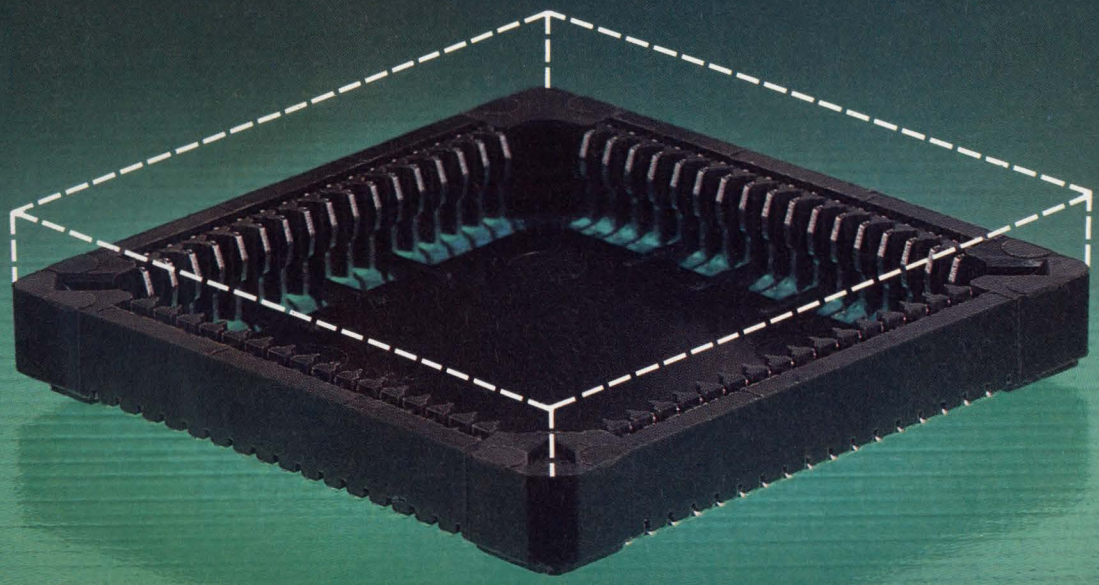

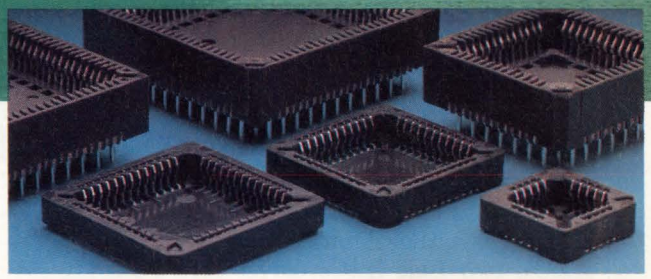

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CIRCLE 82 FOR U.S. RESPONSE

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MHz, 12-bit ADC on a 28,000-mil^2 chip. The chip is a power hog, though, dissipating 3.5 W. H-P's design employs 21 comparators and one sample-and-hold amplifier (SHA). Clocking at 20 MHz, the ADC achieves a signal-to-(noise + distortion) ratio of 65 dB on a 2-MHz sine wave. At a Nyquist frequency of 10 MHz, the ratio is 63 dB. Spurious-free dynamic range (SFDR) runs –80 dB and –72 dB, respectively, at the same input frequencies.

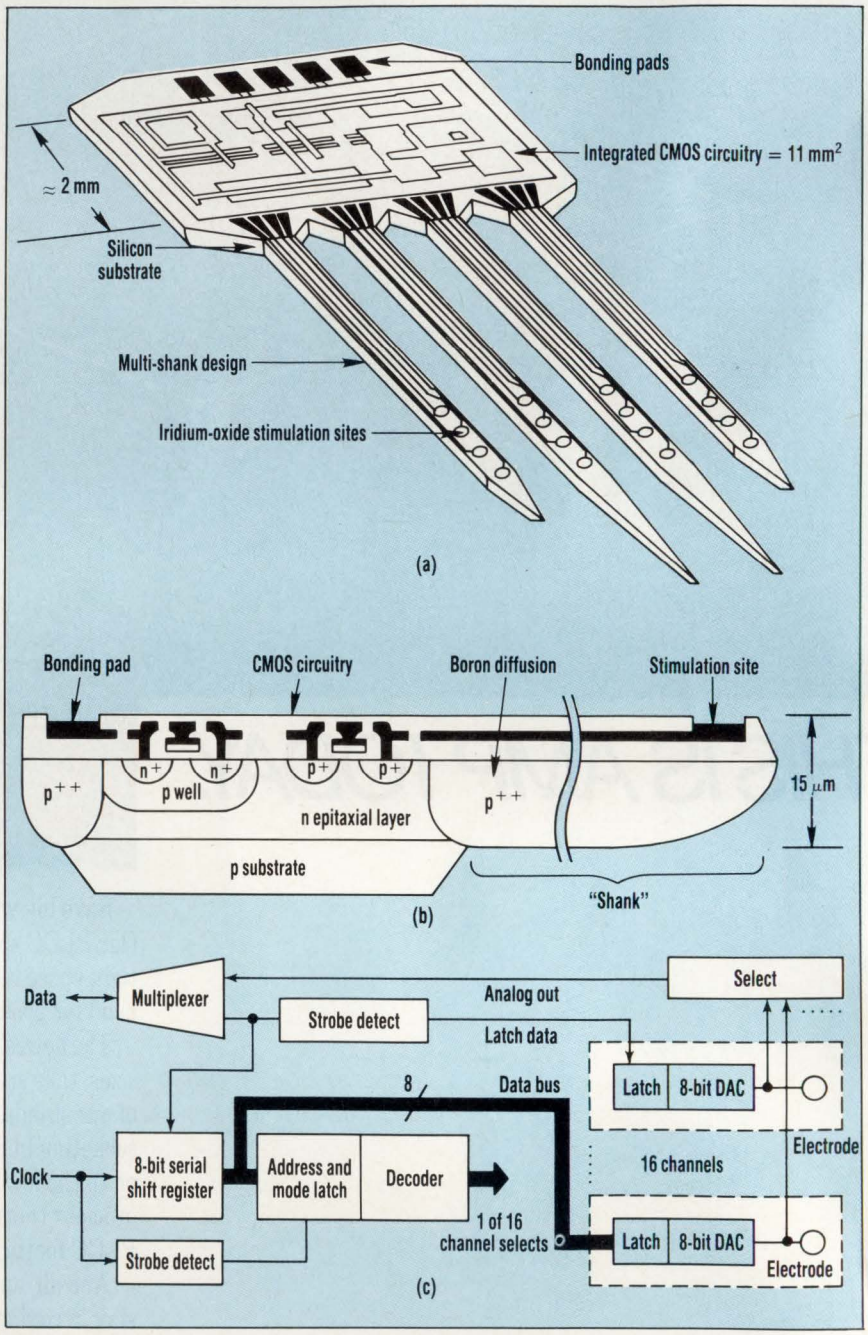
All signal processing following the single-ended-to-differential preamplifier is fully differential *(Fig. 3)*. The clock puts the SHA into the hold mode and sequentially strobes the ten identical quantizer stages via the clock-delay chain. The 11th stage, a simple comparator, acts on the final analog residue. The quantizer (shown single-ended for simplicity) compares the input signal with positive and negative thresholds ($V_{reference}/2$ and $-V_{reference}/2$). If the signal lies between the two values, the signal is amplified by a factor of two. If it exceeds either limit, one of the ADC's two 1-bit DACs moves (offsets) the voltage at the SHA's output closer to zero via the summing circuit Σ. Then the amplified residue moves to the next stage.

Three possible states result, representing 1.5 bits of data. However, redundancy will occur because the gain of each stage is two. Later stages employ the redundancy to correct comparator-offset errors as great as 250 mV. Conversion takes 35 ns, after which the quantizer-comparator states are transferred into the de-skew latches. The adder now performs error correction by removing the redundancy in the data, passing its sum (a digital word) to the output drivers. The SHA then has 15 ns to get a new sample.

Philips has also employed a pipelined, two-step architecture in the design of a 10-bit, ADC that can sample at better than 50 MHz. While sampling at 40 MHz, effective bits for a 10-MHz signal runs over 9.5 and remains above 8.5 at the Nyquist frequency. Under similar conditions, SFDR runs 66 dB at 50 MHz and 62 dB at 40 MHz. Although built on an all-npn, bipolar process—not CMOS—this 17,000-mil^2 chip needs just 750 mW of power.

It employs a pair of cascaded differential SHAs that feed the 5-bit coarse flash ADC. Like the Philips 8-bit pure-flash ADC, both the coarse and the 6-bit fine-flash ADCs employ a folded structure. The architecture reduces the number of comparators and latches, and thus the die size and the power.

Until recently, 12-bit IC-ADC throughput rates have been limited to 1 MHz, and the new faster devices have had access to bipolar transis-



4. THIS MIND PROBE independently stimulates up to 16 tissue sites in a space where only one could fit before (a). The probe, developed at the University of Michigan, is built on a CMOS process (b). Micromachining was added to the process to build the 15-μm thick "shanks"(c). The active circuit contains 16, 8-bit DACs.

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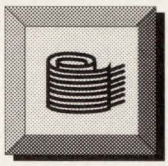

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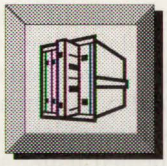

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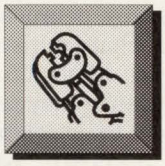

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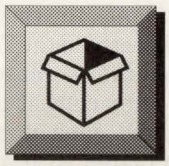

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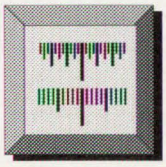

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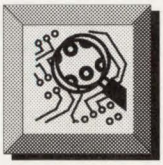

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CIRCLE 84 FOR U.S. RESPONSE

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tors (ELECTRONIC DESIGN, *Oct. 24, 1991, p. 47*). Now the Center for Integrated Systems at Stanford University, Stanford, Calif., has put a 12-bit, 5-MHz ADC on a CMOS chip using 1-μm design rules. The chip employs a classic two-step architecture, with some refinements, and needs just 200 mW from a 5-V rail. A 7-bit coarse flash ADC on the input is followed by a 12-bit-accurate, 7-bit DAC. It in turn is followed by a summing network and a 6-bit fine-flash ADC that achieves 1-bit redundancy for error correction. As in all CMOS ADCs, the comparators employ switched-capacitor techniques to eliminate offset and low-frequency (flicker) noise errors.

In contrast to two-step designs, in which the thermometer-code output of the first flash is converted to binary form and applied to a binary-weighted DAC, the flash outputs are applied directly to the 7-bit DAC. The DACs hold the secret to this simpler method. They consist of an array of equal-valued capacitors that share their top plates with MOS switches connected to the bottom plate of each capacitor. Controlled by the first-stage comparators, the MOSFETs switch the bottom plates between ground and the reference voltage. The DAC can be viewed as a capacitive voltage divider that causes the top-plate voltage to change by an amount proportional to the number of ONEs in the thermometer code. Sampling a 5-kHz signal at 5 MHz results in a no-missing-code conversion and a signal-to-(noise + distortion) ratio of 65 dB. It should be noted that the IC doesn't contain a SHA.

More CMOS

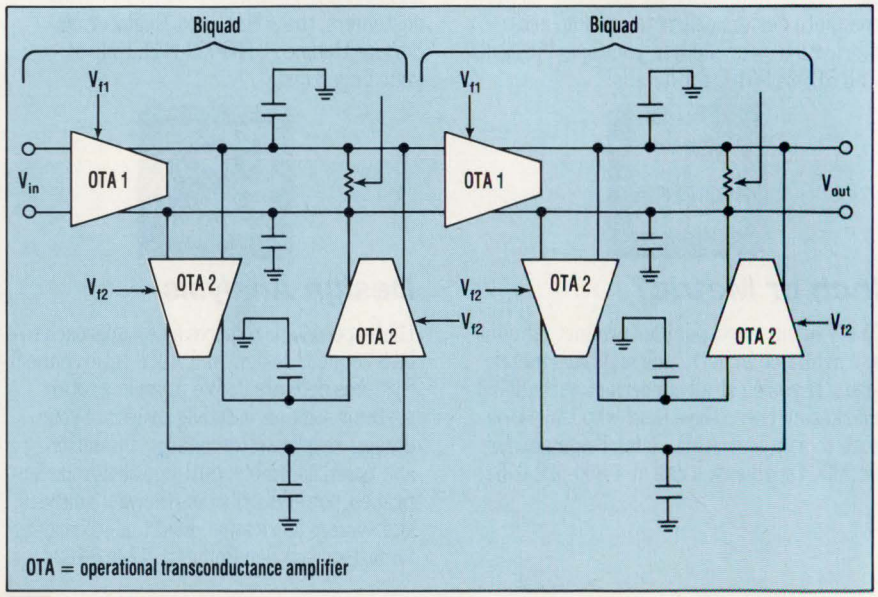
A second 12-bit CMOS two-step converter that can sample at similar rates but with a very different architecture has been designed jointly by Analog Devices, Wilmington, Mass., and the University of Illinois at Urbana. Though analog self-calibration techniques have developed into a fine art, they don't adapt readily to two-step or multistep architectures. Instead, this converter implements a unique code-error calibration technique in the digital domain. It calibrates digital outputs obtained (after conversion) from uncalibrated ADCs. The technique cuts feedthrough, offset, and interstage-gain errors simultaneously. Though designed to sample at a few megahertz, the prototype IC wasn't testable above 100 kHz due to a malfunction of the calibration logic. However, while sampling a 4.86-kHz sine wave at 92.16 kHz, after calibration, harmonics above –80 dB disappeared.

Mind Probe

Electrical stimulation in a human body's central nervous system represents a valuable technique for the study of information-processing techniques in neural circuits, and is a key element in the development of neural prostheses for the deaf. In the past, wire electrodes have been used to inject small currents into tissue to activate nearby neurons. However, the physical characteristics of these electrodes are difficult to control. In addition, because they tend to splay out in tissue, their relative position becomes unknown, particularly when used in multi-electrode arrays. Now, by using micromachining, the University of Michigan at Ann Arbor has developed a probe that carries 16 independent stimulus sites, yet displaces no more tissue than a single-wire electrode *(Fig. 4)*. Highly selective stimulus patterns are generated electronically by superimposing currents at several spatially distributed sites on the probe.

The probe's four shanks are 15-μm thick and are defined during an etching process by a diffused, boron etch stop *(Figs. 4a and 4b)*. Because they're in direct contact with the tissue, the shanks must be grounded, necessitating the use of a 3-μm, n-type/p-type p-well CMOS process with an epitaxial layer. Fabrication follows a standard process flow with several exceptions. Since the drive-in for the p-well and the deep p^{++} diffusion for the etch stop are performed simultaneously, the p-well implant dose must be adjusted for the additional thickness of the masking oxide. Bonding-pad oxide and nitride are used for the dielectrics under the shank conductors. The probe's upper dielectrics consist of planarized chemical-vapor-deposition (CVD) oxide/nitride films developed to ensure long-term viability in human tissue. The 16 exposed stimulation sites of iridium are formed using sputtered titanium/iridium films in a self-aligned lift-off process.

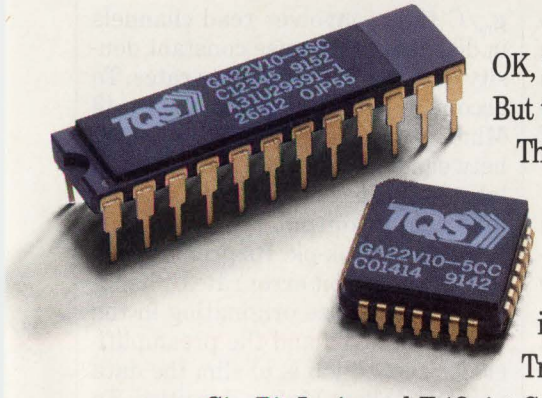
For their final processing step, the wafers are placed in an etchant of ethylenediamine-pyrocatechol water. It dissolves the silicon substrate but leaves the boron-doped silicon



5. UNLIKE MOST G_m/C filters, this voltage-tunable 250-kHz-wide 10-MHz bandpass circuit, designed at the Catholic University of Leuven, offers a dynamic range of 68 dB.

For years, people have been trying to run 100 meters in under 9 seconds, clear 8 feet in the high jump, and hit 5.5 ns in a 22V10 PLD.

We're still having some trouble with the first two.



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and other exposed materials untouched. After separation from the wafer into individual probes, iridium oxide is grown on the iridium electrode sites using voltage cycling in a buffered saline solution. The conductive oxide delivers charge in excess of 3 mC/cm^2, representing an order-of-magnitude higher charge delivery than other materials can provide.

In the circuit for the probe, a 4-MHz clock shifts 16-bit control words onto the chip *(Fig. 4c)*. Four bits handle the site address, two bits set the circuit into one of four modes, eight bits determine the stimulation-current amplitude, and two bits handle strobing and status. In the normal operating mode, specified current values are set up on addressed channels and remain there until readdressed. A second mode grounds the selected channel, permitting external DAC calibration without stimulating the tissue. When in the third mode, the analog voltage developed in response to stimulus current can be observed. The fourth mode biases the electrode above ground to increase the charge delivery. The heart of the probe consists of an array of 16 DACs, each delivering an analog current of $\pm 254\ \mu$A with 8-bit precision. The probe operates at clock rates to 10 MHz and dissipates just 80 μW of power in the quiescent mode. The circuitry occupies an area of just 11 mm^2.

Fancy Filters

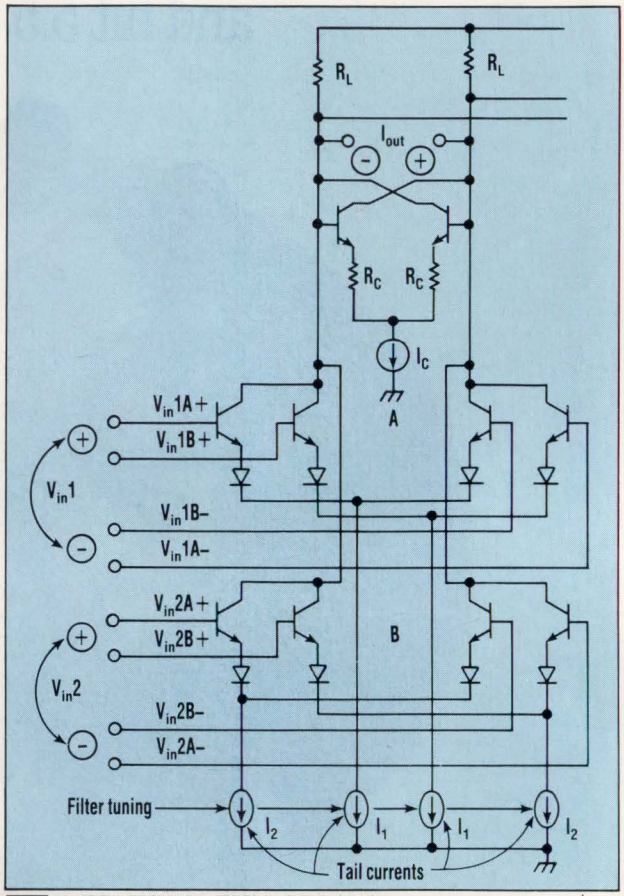
Tunable filters and other tuned circuits are basic to many analog systems. At frequencies to about 150 kHz, switched-capacitor circuits dominate. The last few years has seen a number of conference/journal technical papers describe ICs representing so-called g_m/C filters for frequencies between 10 and 100 MHz. At their heart lies a transconductance (g_m) amplifier stage, often an operational transconductance amplifier (OTA). Adding a capacitive load C creates a single filter pole, the response of which is a function of g_m/C. Varying the stage's transconductance with a dc voltage directly varies the response. Complex circuits, such as biquads, can be built up from these g_m/C blocks to form virtually any conventional analog filter. They have, however, two major drawbacks: limited dynamic range and the need for a relatively large supply voltage. The latter can be difficult to integrate because the IC processes capable of building reasonable-gain 50-to-100-MHz amplifiers tend to limit supply voltages to about 10 V.

However, the Catholic University of Leuven, Haverlee, Belgium, has come up with a maximally flat, 10.7-MHz, narrow-bandpass filter offering 68 dB of dynamic range. Moreover, it runs off a ± 2.5-V supply, yet intermodulation distortion is below –40 dB for an input signal of 3.4 V pk-pk. The 3-dB bandwidth and ripple are just 250 kHz and 0.5 dB, respectively. Both the center frequency and the quality factor Q are independently tuned by on-chip controllers. The filter's architecture is based on a pair of biquad sections connected in cascade *(Fig. 5)*, forming a circuit with a gain of unity—and thus maximum dynamic range—around the center of the passband.

The on-chip Q and frequency-control circuits generate the dc voltages V_{f1} and V_{f2}, respectively, from off-chip clocks. The clock optimizing the filter's Q passes through a closed-feedback-loop circuit that includes a model of the filter. The dc control voltage from the circuit alters the g_m of an OTA up or down to peak the Q of the model. The control voltage resulting in the peak Q is applied to the OTAs in the filter. A similar closed-loop circuit and model set the filter's center frequency as a function of the clock frequency.

Today, the major application for g_m/C filters involves read channels in disk drives that use constant density with their variable data rates. To accommodate data rates up to 48 Mbits/s requires a cutoff frequency between 9 and 27 MHz. The filter is located inside an AGC loop and its differential output typically runs less than 1 V pk-pk. Its primary role is to lower the bit-error rate by band-limiting the noise originating in the magnetic media and the preamplifier. Its second job is to slim the data pulses to allow higher densities. To minimize peak pulse shifts in time, a linear-phase (constant-group delay) response over the signal bandwidth is essential.

The latest such filter, from Silicon Systems Inc., Tustin, Calif., employs a 7th-order, 0.05° equiripple linear-phase design. The negligibly small



6. BY USING TWO STAGES (A and B) instead of one, and by adding the currents of the two stages, the dynamic range of Silicon Systems' transconductance amplifier for G_m/C filters was raised by a factor of three. Signal-to-noise ratio was increased by a factor of 2.4.

ripple extends the constant-delay region from that of the commonly used Bessel filter, or 1.5 times the cutoff frequency f_c, to 2 times f_c. The transconductance element itself represents the critical element in these filters, particularly to avoid Q tuning, which was required in the previously described circuit. To minimize undesirable excess phase delay, the circuit must be as simple as possible without internal high-impedance nodes. High input and output resistances, as well as easy tunability, are mandatory. Transconductance amplifiers meeting these demands can be built with bipolar transistors. But, as noted earlier, they may suffer from a limited input-signal linear dynamic range.

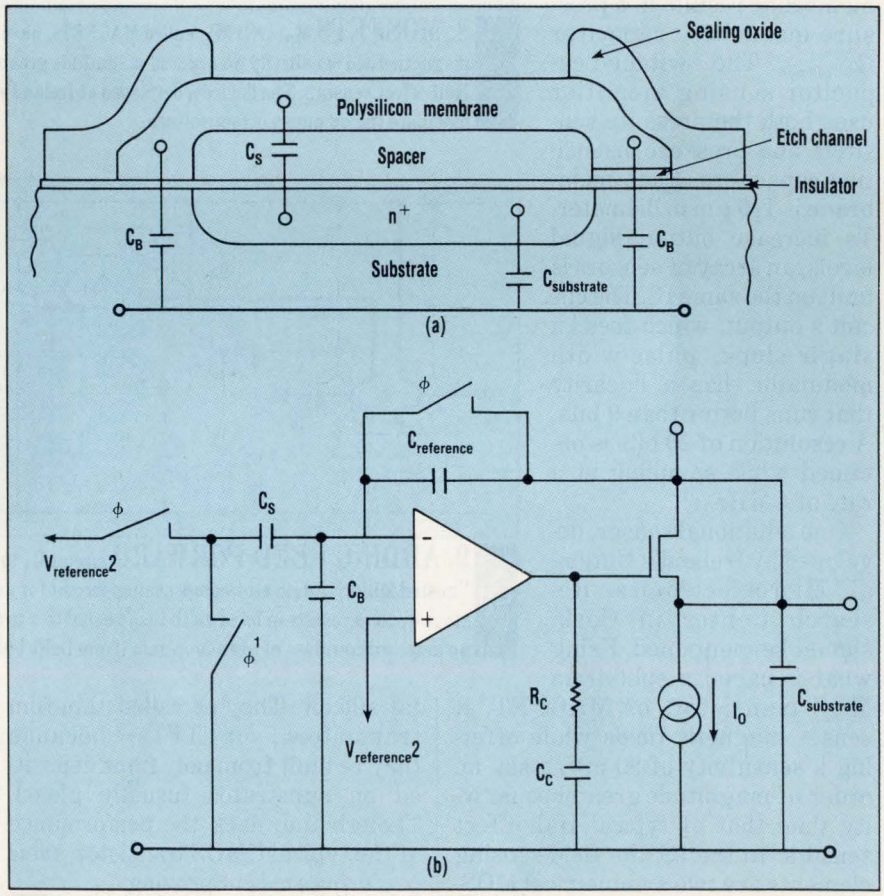
Designers from Silicon Systems upped the linear dynamic range of their circuit by a factor of 3 while improving its signal-to-noise ratio (SNR) by a factor of 2.4. This was accomplished by building a transconductance stage using two matched emitter-coupled transistor pairs (A and B) with emitter-area ratios of 1:4 and 4:1 (rather than a single pair), respectively, and by adding their output currents *(Fig. 6)*. The upper pair lies in the forward signal path of the biquads forming the filter, and the lower pair lies in a negative-feedback path around each biquad. Adding diodes in series with the emitters increases the dynamic range and SNR by an additional factor of 2 and $\sqrt{2}$, respectively. Varying the "tail currents" changes the g_m of the stage tuning the filter.

All On One Chip

The push for smaller disk drives has spurred IC suppliers to put more and more of the disk drive's circuitry on fewer chips, with a one-chip drive becoming the ultimate goal. With that in mind, Analog Devices, Wilmington, Mass., put the complete read channel (except for the preamplifier) for a 32-Mbit/s disk drive on one IC, and that includes a programmable 7th-order Bessel filter. The IC, which was fabricated with a 1.5-μm biCMOS process, has a total power dissipation of just 800 mW.

Today, virtually any "implantable" system aims to be a complete system on a chip. A joint research project between North Carolina State University in Raleigh; Digital Equipment Corp., Hudson, Mass.; and the Microelectronics Center of North Carolina in Research Triangle Park, has borne an implantable, digital, telemetry system operating between 27 and 51 MHz on a CMOS die designed with 1.2-μm design rules. The digital data phase-shift modulates the carrier. To maximize the transmitted power, a voltage-controlled oscillator (VCO) and amplitude detector on the chip search for the resonant frequency of the antenna prior to each transmission, and then set the carrier to that frequency instead of tuning the antenna. A strobe signal from an implanted microprocessor starts the search by forcing the VCO to operate at a frequency well above the expected resonant frequency. The VCO output is then reduced 400 kHz every 800 ns, until a 6-V pk-pk swing is detected at the chip's antenna node. At this point, the VCO's frequency is locked and the carrier is then phase-shift modulated (keyed).

Another implantable chip, to be employed in 1-mm-diameter medical catheters (like the mind probe that uses micromachining), was developed at the Fraunhofer Institute of Microelectronic Circuits and Systems in Duisburg, Germany. For use during surgery, the chip provides the anesthesiologist with continuous information about the patient's arterial blood pressure and body temperature *(Fig. 7)*. This CMOS IC not only senses pressure and temperature, it also conditions and amplifies the signals from the sensors and converts them to a train of easily digitized pulse-width-modulated (PWM) pulses for transmission through a noisy environment. Temperature ac-



7. DESIGNED TO FIT IN A CATHETER 1 mm in diameter, the Fraunhofer Institute's micromachined pressure sensor measures blood pressure during surgery (a). Its capacitance, C_S, is embedded in the circuitry of a CMOS, switched-capacitor op amp (b).

curacy is within 0.1° between 35° and 42°C (94° and 107°F), and pressure accuracy is within 1 mbar between 900 and 1400 mbars.

The pressure sensor consists of capacitor C_s formed from a polysilicon membrane (diaphragm) and an n^+ silicon diffusion in a silicon substrate. The membrane is obtained by lateral (anisotropic) etching of a sacrificial oxide spacer. Etch channels in the polysilicon lead the etchant to the oxide. During the etching process, the already created CMOS circuits are protected from the etchant by a layer of the same polysilicon that forms the membrane. The etch channels are sealed by adding a layer of oxide that initially covers the whole membrane. The oxide is removed to build a pressure-sensitive capacitor. Leaving the oxide on the membrane results in a pressure-insensitive capacitor $C_{reference}$. The switched-capacitor sensing amplifier uses both the pressure-sensitive and pressure-insensitive capacitors. Each membrane is 110 μm in diameter. To increase output signal levels, an array of sensors is built on the same IC. The circuit's output, which feeds a single-slope, pulse-width modulator, has a linearity that runs better than 9 bits. A resolution of 10 bits is obtained while sampling at a rate of 4 MHz.

One additional sensor, developed by Ireland's National Microelectronics Research Center in Cork, should be mentioned. Using what is called a split-drain MOS transistor, or MAGFET, it senses magnetic fields while offering a sensitivity of 80 mV/tesla, an order-of-magnitude greater sensitivity than that of typical Hall-effect sensors. In the IC, the field-sensing elements are two symmetrical MOSFETs, M3 and M4, which form the loads for the differential current mirror *(Fig. 8)*. In this op-amp configuration, the MAGFET modulates the offset voltage of the op amp. Closed-loop gain is set by the two resistors.

POLY TRANSISTORS

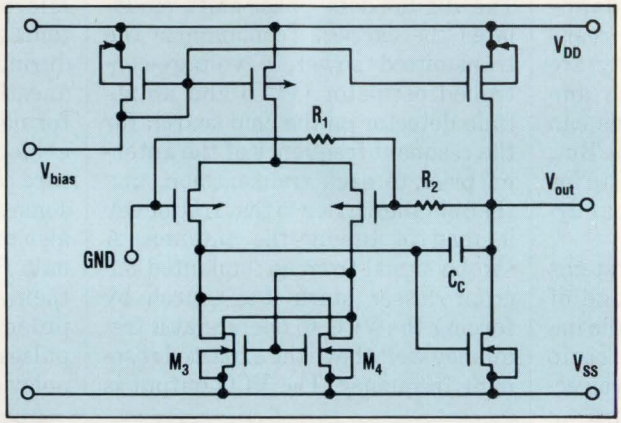
Active-matrix liquid crystals used for flat-panel displays in portable PCs and "pocket" TV sets have become the driving force for CMOS-type circuits built from poly-crystalline silicon, rather than single-crystal silicon. They're called thin-film transistors, or TFTs, because they're built from poly films deposited on substrates (usually glass). Though they lack the performance of the typical CMOS transistor, their performance is improving.

Xerox Corp.'s Palo Alto Research Center in California has built three different switched-capacitor op amps using TFTs. Two of them offer flat, uncompensated, open-loop gains of better than 40 dB, and unity-gain bandwidths of 300 kHz. A third, multistage design needing compensation provides a dc open-loop gain of 50 dB, an open-loop gain of 80 dB at 3 kHz, and a unity-gain bandwidth of about 200 kHz. A 4-bit, switched-capacitor DAC offering 8-bit accuracy was also built, with operational amplifiers used as output amplifiers to provide an output voltage of 10 V.

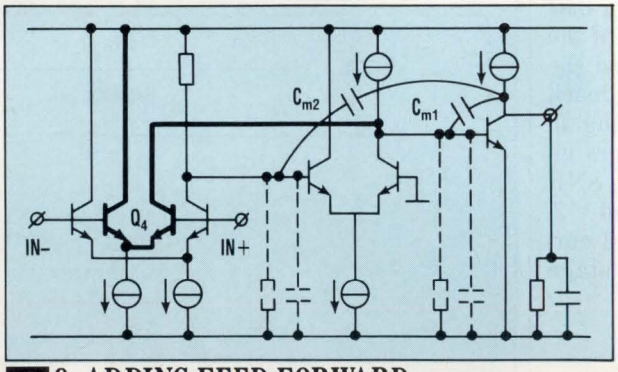
Until now, TFTs have basically stayed in the low-frequency-device realm. However, a joint effort from CNET, Grenoble, France, and Lannion and SAGEM in Paris, has put 162, 25-MHz video amplifier/column driver/SHAs on a 50-mm^2 chip. The column drivers sample the video of each successive line at high frequency (25 MHz for PCs), hold it, and then transfer it to the active matrix during the next line period. LCDs operate with a 3-to-4-V signal and respond to ac voltages (they can be damaged by dc biasing), so the applied voltage must be symmetrical around zero. Therefore, the output signal of the column drivers is inverted between each successive frame. The chip contains a digital section with a control block and registers, an analog video section that provides clamping, the inverting and noninverting channels that create the ac signals, and the 162 drivers.

During output sampling, the clamping amplifiers are switched to a capacitor for charging. Its charge is then transferred to the hold capacitor, which is in the feedback loop of a TFT operational amplifier. While holding, the capacitor's output is connected to the column it's driving. The op amp has an open-loop gain of 40 dB and a 1% settling time of 2 μs while driving 150 pF.

One of the most interesting ISSCC



8. MOSFETS M_3 AND M_4, called MAGFETs, have magnetic-field sensitivity an order-of-magnitude greater than Hall-effect sensors. The devices, developed at Ireland's NMRC, modulate the op amp's offset voltage.



9. ADDING FEED-FORWARD circuit Q_4 to a "nested Miller" integrator compensation circuit for a three-stage op amp results in bandwidth that's equal to a two-stage op amp, without loss of open-loop gain (from Delft University).

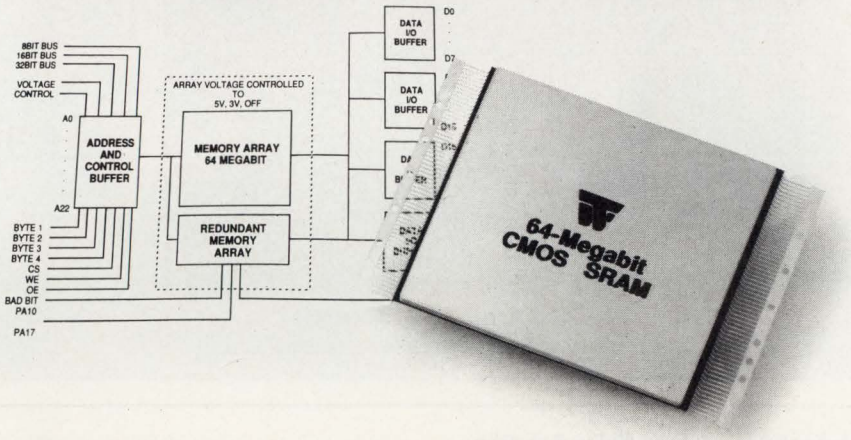
presentations involves a widely useful design technique from Delft University of Technology in the Netherlands. They show how an op amp containing as many as three gain stages can be compensated without sacrificing bandwidth. Three-stage op-amp circuits were used to maximize open-loop dc gain of an op amp, such as the OP-27. But if the three-stage op amp is to operate at low, closed-loop gains without oscillating, it usually can't be frequency compensated with simple pole splitting typically used for two-stage op amps like the 741. That's because the third stage adds an extra dominant pole.

A "nested Miller" structure (patented in 1984 by Johan Huijsing, who is involved with Delft University's ISSCC presentation) represents a more effective way to compensate an op amp containing three (or more) gain stages *(Fig. 9)*. If the bold-lined circuitry, including transistor Q_4, is deleted from the figure, the circuit is a "nested Miller" structure. The two capacitors form "nested Miller" integrators. The circuit rolls off at 20 dB/decade to an open-loop gain of 0 dB. Unfortunately, bandwidth is half that obtained with simple pole splitting.

The Multipath Nested Structure from Delft University overcomes the reduced bandwidth by adding a feedforward path (formed by transistor Q_4) for high frequencies. At low frequencies, the op amp behaves as a three-stage "nested Miller" compensated op amp, while at high frequencies it has the nature and bandwidth of a two-stage circuit using pole splitting. Two op amps, identical except for compensation techniques, were built and tested. Op amp 1 used Huijsing's earlier nesting compensation and op amp 2 used the new technique. Op amp 2's unity-gain bandwidth improves from 60 to 100 MHz and its slew rate from 19 to 31 V/μs. Open-loop dc gain drops from 102 to only 98.□

How Valuable?	Circle
Highly	541
Moderately	542
Slightly	543

64-MEGABIT CMOS SRAMs



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V_{OLV}*	0.8	1.0
V_{IHD}*	1.5	1.7
V_{ILD}*	0.8	0.8

*V_{OLP} = Peak Ground Bounce V_{OLV} = Undershoot
V_{IHD} = Dynamic Input High V_{ILD} = Dynamic Input Low

Performance's FCT-T vs. Leading Competitor's FCT-T

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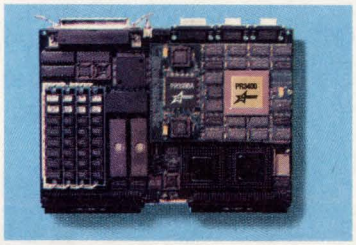

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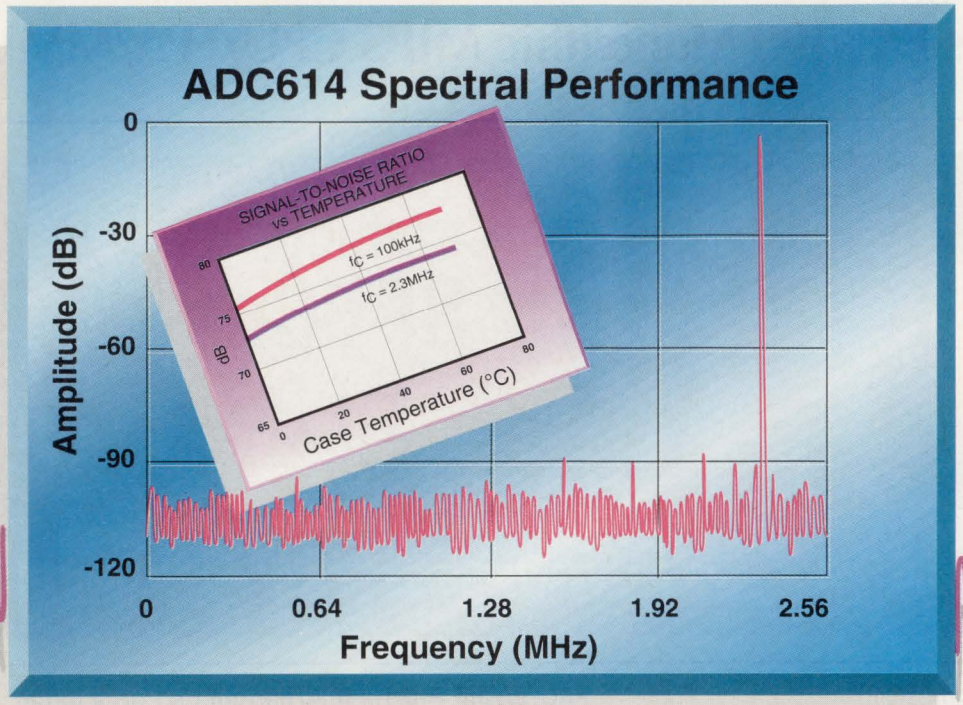

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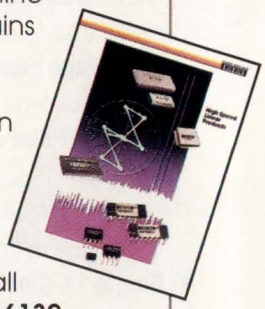

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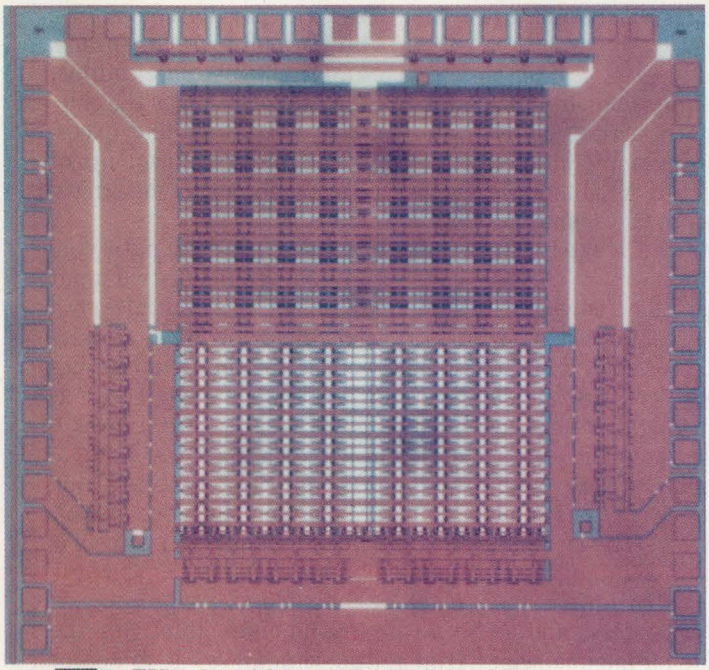
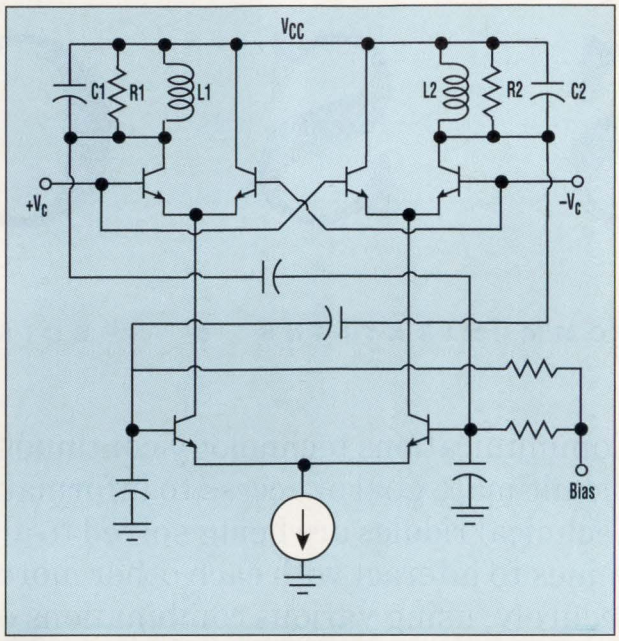


1. THE CROSSPOINT SWITCH CHIP from IBM contains about 4200 transistors and measures 3 mm on a side. The chip has 64 pads, 20 of which are used for the +1.4-V and -2.2-V power supplies and ground. The 16-by-16 switch multiplexers and outputs are located on the lower part of the die. The setup circuits with latches sit on the upper part.

This year's ISSCC continues to reveal impressive device innovations that support high-speed communications systems. One example is a crosspoint switch design under development at IBM Thomas J. Watson Research Center, Yorktown Heights, N.Y., that promises to shatter present bandwidth limitations in broadcast Integrated Services Digital Network (ISDN) applications. Multiple high-speed processors coupled together in a wideband communication network rely on a high-bandwidth, non-blocking circuit switch for maximum data throughput. Prior crosspoint switches for broadband ISDN applications

have used silicon-bipolar or gallium-arsenide MESFET devices whose bandwidths are limited to 2 Gbits/s.

IBM's experimental 16-by-16 non-blocking, asynchronous crosspoint switch features a data rate of 5 Gbits/s per channel. Implemented in a 0.8-μm double-polysilicon, double-metal, self-aligned silicon-bipolar ECL process, the chip has a 420-ps data-path delay, a 1-ns setup time, and dissipates about 4.6 W *(Fig. 1)*. Included on the chip are 16 input buffers, 16 output buffers with tri-state capability, 16 16:1 multiplexers represented as 16-by-16 crosspoint switches and sense amplifiers, and 16 5-bit master-slave latches for storing switch-setup information. Selectively writing the latches according to the Y or output addresses is supported by on-chip 1-of-16 decoder logic.



2. A MONOLITHIC DESIGN of a voltage-controlled oscillator (VCO) devised by University of California at Berkeley researchers consists of a single-ended-to-differential input stage, a main VCO stage, and an output buffer amplifier that drives a 50-Ω load. The two inductors in the RCL tank circuits are implemented as metal spirals on the chip. Control voltages plus V_c and $-V_c$ are used to vary the oscillator continuously between the resonant frequencies of the two tank circuits.

Significant developments are reported for wireless-communications applications for the growing 800-to-2500-MHz range. This range includes cellular and spread-spectrum systems operating at 800 to 950 MHz, L-band satellite transceivers working at 1500 to 1700 MHz, and various personal communication networks, cordless telephones, and wireless local-area networks (LANs) operating in the 1800-to-2500-MHz range. Such high-volume industrial and consumer applications require RF components that must be small in size, dissipate low power, and are low in cost.

These are the design objectives of a mixed-signal, parametrized-cell array for wireless applications revealed by Avantek Inc., Newark, Calif. Developed for receiver-on-a-chip (ROC) applications, the 1.8-by-1.8-mm ROC-1 array is intended for receiver operations up to 4 GHz, but can also perform many transmit functions up to 2 GHz using external power amplifiers. The array's digital cells include standard ECL gates, and CMOS/TTL inputs and outputs. The logic swing for the digital cells is 240 mV, and the single V_{CC} supply can range from 3 to 6 V. Minimum gate delays are about 60 ps, and the toggle frequency for a D-latch can exceed 4 GHz.

The RF cells include a low-noise amplifier, an RF preamplifier, various IF amplifiers, an oscillator, and a variable-gain amplifier. The array also provides a bandgap-reference cell. Avantek fabricates the array with a silicon-bipolar process with peak f_t and f_{max} frequencies of 14 and 20 GHz, respectively. The process has two-level gold, 2-μm emitter-base-pitch interdigitated devices, polysilicon thin-film resistors, and 2-μm-thick field oxide for minimal wiring parasitics.

Similar design goals for wireless communications have been met by engineers at Fujitsu VLSI Ltd., Kasugai, Japan, with a silicon-ECL dual-modulus prescaler (divide ratios of 64/65 and 128/129). Designed for a 3-V, 1-GHz phase-locked-loop (PLL) synthesizer system, the device dissipates just 3 mW. The prescaler chip includes I/O buffers, 8 D-type flip-flops, a 6-input OR gate, a divide-ratio switching gate, and a modulus-control gate.

Test results have confirmed 1-GHz operation with a supply voltage down to 2.58 V. At this voltage, power consumption is 3 mW. The 1.2-by-1.2-mm chip is made on a 0.2-μm self-aligned emitter-base process with polysilicon electrodes and resistors.

High-speed parallel-data transfer is the function of a transceiver chip set under development by the Hewlett-Packard Microwave Semiconductor Div., San Jose, Calif. The silicon bipolar chip pair is designed to transfer parallel data across a 1.5-Gbit/s serial link. For use with parallel computers, high-resolution graphics, and network backbones, this two-chip set overcomes the chip-interconnect difficulties and excessive support-circuit requirements of Hewlett-Packard's earlier design using four chips.

The receiver-chip data path consists of an input selector, two input sampling latches, a demultiplexer, a control-field decoder, and a data-field decoder. An input equalizing amplifier provides a 3-dB boost at 600 MHz to compensate for skin losses in long coaxial lines. In addition, an on-chip PLL extracts a timing reference from the serial input. The startup handshaking protocol is handled by the receiver chip's state-machine controller.

A programmable option on the transmitter chip allows it to accept either 16 or 20 bits of data to produce a 20- or 24-bit line-code frame. When needed, parallel data words are transmitted in either true or complement form to maintain dc balance on the line. The two chips are made with a 3-level-metal full-custom differen-

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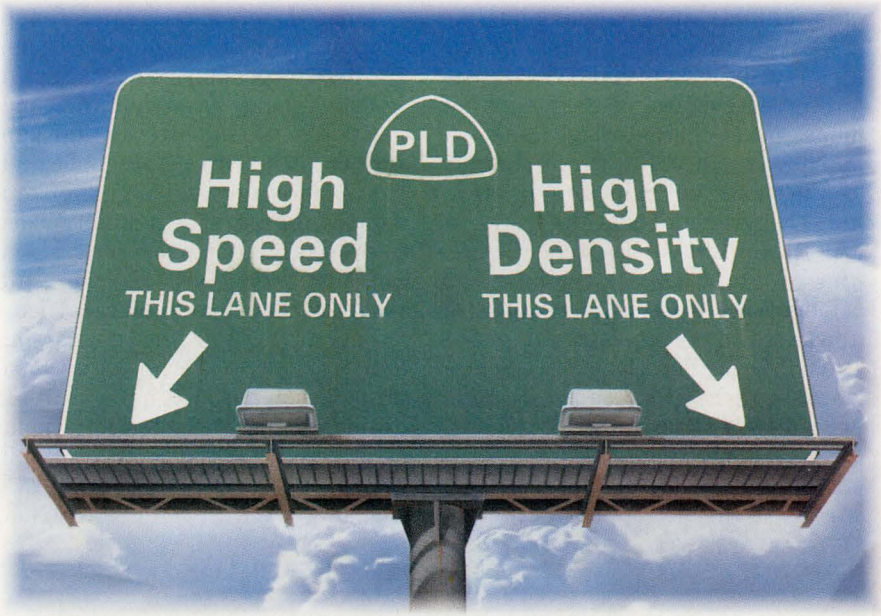

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tial 4.5-V ECL process whose device f_ts reach 25 GHz. A custom 68-pin surface-mounted package houses the chips along with their bypass and integrating capacitors. The 1.8-W transmitter and 2.0-W receiver chips are 3.5-by-3.5-mm each in size and contain 6100 and 6600 active devices, respectively.

Voltage-controlled oscillators (VCOs) are important building blocks for communications systems, particularly in applications like PLLs. For high-frequency operation, LC-type sinusoidal VCOs are preferred because of their superior phase-noise characteristics and frequency stability. But they generally require external inductors or varactors. Now scientists at the University of California at Berkeley believe this limitation can be overcome with a monolithic VCO they developed for the microwave-frequency range.

The device is a Colpitts oscillator containing two LC-tuned circuits with different resonant frequencies *(Fig. 2)*. The inductors are formed as metal spirals on the silicon substrate, so the circuit doesn't require any external components. The device has a tuning range from 1.68 to 1.86 GHz, and active die area is 0.315 by 0.670 mm. The chip consumes 70 mW from a 5-V power supply.

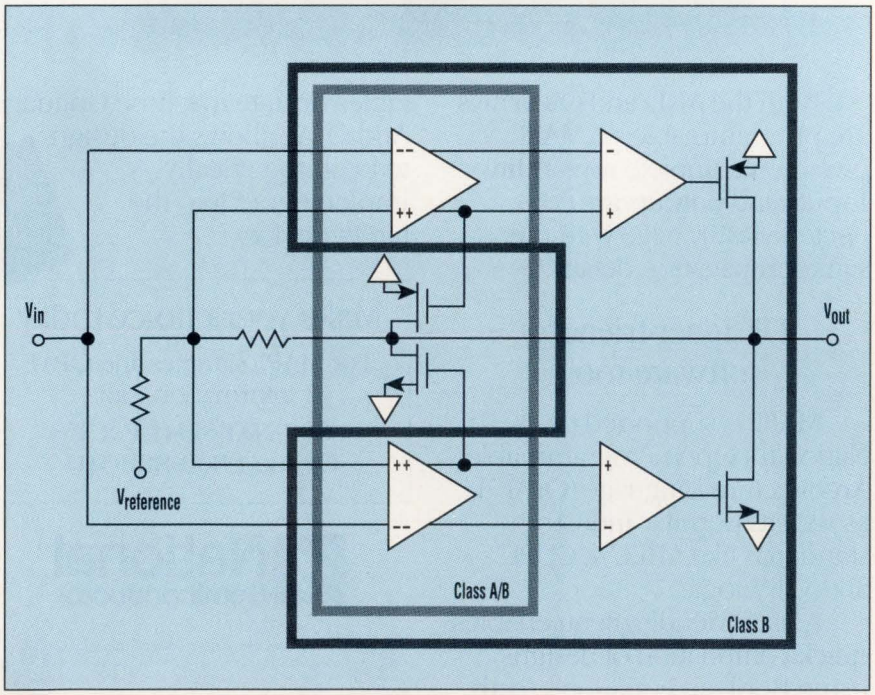
Chip vendors are also responding to increasingly tough demands imposed by new applications involving data transmission over telephone lines. One emerging application is the high-rate digital subscriber line (HDSL), which uses echo-cancellation-based modem techniques for operation at the T1 rate of 1.554 Mbits/s over a repeaterless loop up to 12,000-ft. long. Even more demanding is the asymmetric digital subscriber line (ADSL). This application has a more aggressive goal of providing 1.5-Mbit/s VCR-quality video over existing copper loops to residential customers, with a lower rate from the home to the central office.

Current digital-signal processing (DSP) and ASIC technologies have proven economically impractical for providing intensive computational operations required by ADSL applications. However scientists at AT&T Bell Laboratories, Middletown, N.J., offer a promising alternative—the general adaptive finite-impulse-response (FIR) filter, also called GAFF. The GAFF supports a simple frequency-multiplexed core for ADSL operations, or a full-feature unit that includes echo cancellation, a decision-feedback equalizer, and Tomlinson precoding. The design also incorporates binary functions for all real-time modem operations.

The 37.3-mm^2 chip is a RAM-based, dual-processor engine consisting of an FIR processor, three FIR engines, a binary processor, and an interface to external processors. These function blocks reside on a time-division-multiplexed (TDM) bus that allows software to configure the system functions and interconnections. The FIR processor is a single-instruction, multiple-data processor, and the binary processor is a simpler controller with binary operations. The binary processor contains a program RAM whose content defines the signal-processing operations. It also generates coefficients and data-address pointers, and transfers results from the FIR engines to the output registers in the binary-processor space.

The FIR engines perform all operations in parallel, executing vector multiplications and coefficient updates concurrently. Each engine contains a multiplier, an accumulator, data multiplexers, and its own coefficient and data RAMs. The program RAM of the programmable binary processor uses the partial-product outputs of the FIR engines to configure the FIR structure. It also performs basic binary operations, such as slicing, and defines the system's interconnectivity on the TDM bus.

Packaged in an 84-pin PLCC, the GAFF was designed for a 0.9-μm double-metal CMOS process. It contains 240,000 transistors and dissipates 750 mW at 33 MHz. At this clock rate, the FIR processor executes 100 million multiply/accumulate operations/s, while the binary processor executes an additional 33 MOPS plus other program-control operations executed in parallel. At a 1-Mbaud symbol rate, the GAFF can support a 99-tap transmitter. At 257



3. THE OUTPUT AMPLIFIER STAGE of AT&T's prototype chip for an ISDN U-interface line driver uses paralleled class-B and class-A/B amplifiers to minimize bandwidth loss, quiescent power dissipation, and silicon area. The device has an active area of 0.63 mm^2.

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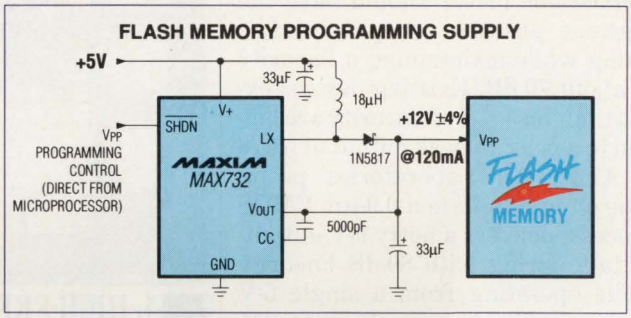
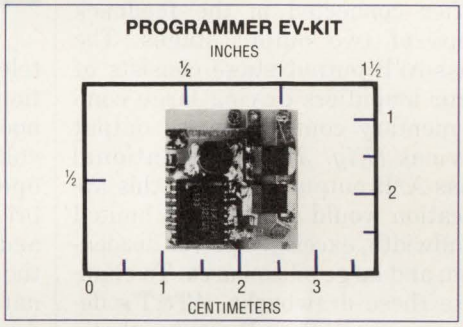
- **Small 18µH Inductor**
- **Direct Microprocessor Control**
- **Space-Saving Footprints: 16-Pin SOIC and 8-Pin DIP Packages**
- **Pre-Trimmed +12V Output with ±4% Accuracy**
- **Wide Input Range: +4.0V to +9.3V**
- **Guaranteed Output Currents up to 200mA**
- **Low-Noise Operation and Excellent Transient Responses**
- **Short-Circuit and Soft-Start Protection**



This MAX732 flash memory programmer supplies +12V ±4% at 120mA with 88% efficiency from a +5V source. The shutdown current for this entire circuit is 75µA.



The complete surface mount MAX732 flash memory programmer fits into less than 1/2 in^2 (3.2 cm^2). Additional capacitors can be added for higher current operation — up to 200mA.

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* Order "MAX732EVKIT"

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CIRCLE 222 FOR U.S. RESPONSE

CIRCLE 223 FOR RESPONSE OUTSIDE THE U.S.

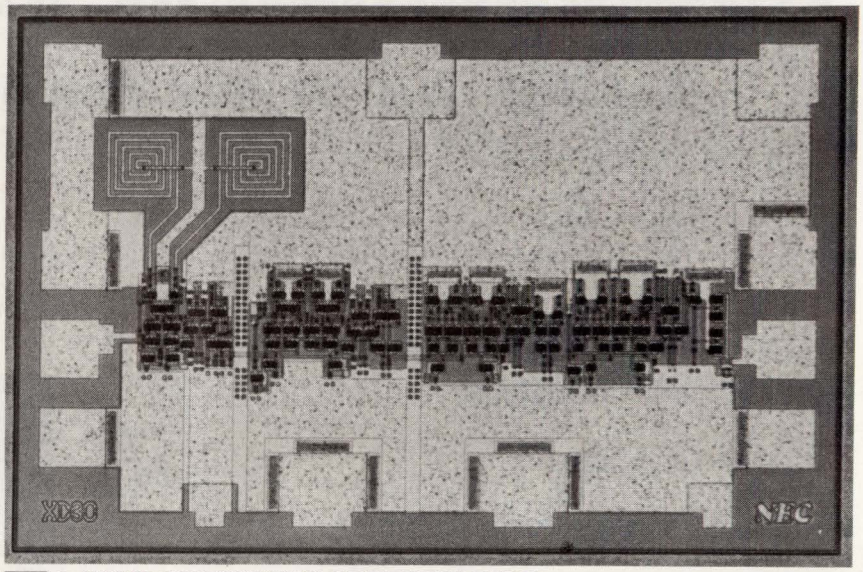
kbaud, it can support a 190-tap echo canceller with a 100% update rate, or an echo canceller with about 300 taps using a partial update rate of 10%.

Another AT&T Bell Laboratories development, which comes from its Holmdel, N.J. facility, involves a new CMOS line driver for the ISDN U interface. Ideally, an ISDN U-interface line driver should have the highest possible output-voltage swing while maintaining a linearity of about 70 dB. Existing devices exhibiting this level of linearity are limited to a peak-to-peak output of 5 to 6 V. AT&T Bell Laboratories' prototype circuit, built in a 0.9-μm CMOS process, delivers a hefty 9-V output-voltage swing with 80-dB linearity while operating from a single 5-V power supply. As a result, up to 40% of power is saved.

The line driver consists of a preamplifier connected in the feedback loops of two output stages. The class-A/B output stage consists of error amplifiers driving large complementary common-source output devices *(Fig. 3)*. A conventional class-A/B output stage for this application would suffer from limited bandwidth, excessive power dissipation, and large silicon area. To eliminate these drawbacks, AT&T's design uses a class-B stage that's placed in parallel with the conventional class-A/B stage.

At the ISSCC, SGS-Thomson Microelectronics, Milan, Italy, described its efforts to integrate on silicon all of the functions necessary to support different telephone operations, such as ringing, conversation, and dialing. For a monolithic silicon solution, these operations impose severe and conflicting electrical requirements, namely, high voltage, high power, low leakage, and very low voltage. For example, in some cases a telephone's ringing circuit must deal with peak potentials as high as 230 V. On the other hand, circuits that handle voice signals must operate at 4 to 5 V to satisfy regulatory standards.

SGS-Thomson's solution was to develop a 250-V process technology that combines vertical DMOS transistors with CMOS transistors on a telephone-line interface chip. In addition to the line interface and main hook switches, the device contains a voltage multiplier for low-voltage operation and a ringer rectifier bridge. Along with circuit operation and protection techniques, the author discusses how the design eliminates the need for external support devices, and how high-density logic can be added to the same chip.



4. HIGH-FREQUENCY PERFORMANCE of NEC's silicon-bipolar frequency divider is enhanced by the spiral inductors in series with the load resistors of the Gilbert multiplier, which comprises the dynamic first stage. The inductors, shown above the first stage at left, increase the maximum frequency by 7% over that of a conventional circuit.

A separate ISSCC session deals with specialized high-speed functions developed to support gigahertz communications systems. Such functions include a prescaler NEC Corp., Kawasaki, Japan, developed for phase-locked oscillators for use in microwave and satellite communications systems.

The 1/16 dynamic frequency divider operates at a frequency of up to 28 GHz *(Fig. 4)*. Fabricated with NEC's advanced borosilicate-glass, self-aligned process, the 1.5-by-1.0-mm chip uses bipolar transistors with a cutoff frequency of up to 40 GHz.

The first stage is a dynamic circuit based on regenerative frequency division. This stage is followed by three stages of static circuits based on master/slave D-type flip-flops. Except for the input and output signals, the internal signals are all transferred in differential form.

Frequency division is accomplished by feeding the output of a Gilbert multiplier back to the input, where it mixes with the input frequency. Contributing to the device's high-frequency performance are aluminum-interconnect line lengths of under one-tenth wavelength, polysilicon resistors for loads and dc biases, a single-ended input, low-impedance supply voltages, and spiral inductors for the inductive loads. The chip dissipates 590 mW from a +5-V power supply.

A more exotic solution to dynamic prescaler design for microwave and millimeter-wave applications was described by Varian Research Center, Palo Alto, Calif. The company's divide-by-N prescaler has a maximum toggle frequency that's limited only by the charge-transit time between charge-coupled-device (CCD) electrodes. Based on two-dimensional, electron-gas CCD (2DEG-CCD) technology, the prescaler uses a two-phase CCD shift register with charge-domain feedback to obtain divide-by-N frequency division, where N represents twice the number of CCD stages.

Descriptive details include the prescaler's circuit design, Spice cir-

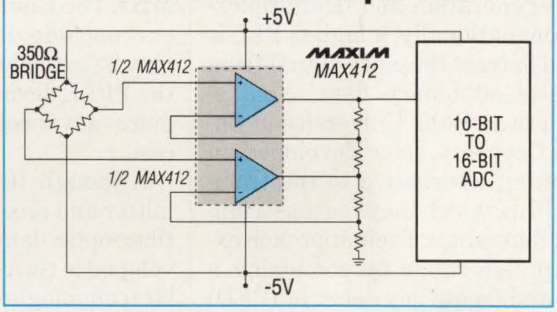
LOWEST NOISE DUAL OP AMP FOR ±5V SYSTEMS

<2.4nV/√Hz NOISE GUARANTEED!

Maxim's new MAX412 delivers superior noise performance when you need it most—when supply voltages are low. The MAX412 is 100% tested to guarantee noise of <2.4nV/√Hz at 1kHz, and the 7.3V_{P-P} output voltage swing is guaranteed while operating from ±5V supplies. Unlike other low noise dual op amps, the 8-pin DIP or SO package reduces the footprint size to save board space over the 14- and 16-pin industry standard devices. Ideal for low level signal conditioning, applications for the MAX412 include high resolution, high speed data acquisition, sensor interface, audio circuits, or active filters.

- **Two Op Amps in one 8-Pin DIP/SO**
- **±2.4V to ±5V Supply Voltage Range**
- **28MHz Bandwidth**
- **Unity Gain Stable**
- **115dB Min Open Loop Gain**
- **2.5mA Supply Current per Amplifier**

Eliminate ±15V Amplifiers



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8-Pin Dual Op Amp Outperforms the Competition

	MAX412	OP227	OP270
Amps/Package	2	2	2
Spec'd at ±5V	YES	NO	NO
Supply Current (mA max)	2.6	5.6	3.25
Input Voltage Range (V min)	|Vs-1.5|	|Vs-4|	|Vs-3|
Noise Voltage Density at 1kHz (nV/√Hz max)	2.4	4.6	5
GBW (MHz)	28	8	5

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* Not included with the Evaluation Board

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cuit simulation based on two-dimensional device modeling, and characterization of a divide-by-2 prototype circuit operating at input frequencies between 8.7 and 18.2 GHz. At that frequency, power dissipation is 325 mW. Varian designers feel that input frequencies could approach 100 GHz for a CCD with a 1-μm gate length and an indium-gallium-arsenide channel layer.

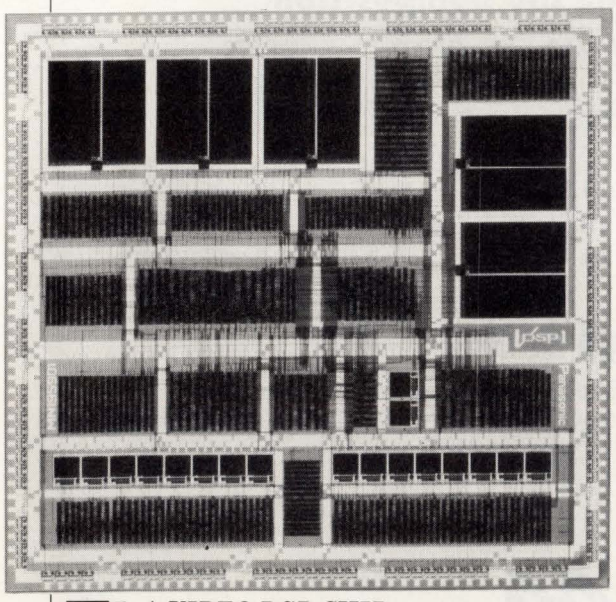
The receiving end of a fiber-optic data link requires clock recovery for data regeneration and demultiplexing. Conventionally, a high-Q PLL is used to extract the clock signal from the received binary data. But researchers at Ruhr University in Bochum, Germany, have developed an interesting alternative to the traditional PLL, which they feel has a limited pull-in range. Their approach extends pull-in range by combining a phase and frequency detector (PFD) with a PLL to create a phase- and frequency-locked loop (PFLL).

An experimental silicon-bipolar PFD operates at frequencies up to 8 Gbits/s, and can be used effectively within a PFLL. The device consists of two sample-and-hold circuits that serve as a phase detector and a quadrature phase detector, and a logic block that detects the sign of any frequency offset between a VCO and the incoming nonreturn-to-zero (NRZ) data. The logic block issues a correction signal, which drives the loop circuit toward a lock.

Test results show a pull-in time of 1 ms for a frequency offset of 400 MHz. The Ruhr University researchers conclude that the PFD operation may be extended to higher bit rates if the PFLL device is fabricated with a more advanced silicon-bipolar process.

Although ICs for 1-Gbit/s transmitter and receiver functions used in fiber-optic data links have been developed in GaAs and high-speed bipolar technologies, wider acceptance of such data links requires lowering the cost of the interface electronics. This was the objective of researchers at the University of California at Los Angeles, who used silicon MOS technology for two critical analog elements required in a fiber-optic receiver. The first device is a decision circuit that can resolve 35-mV NRZ signals at 1.1 Gbits/s with a 10^{-11} bit-error rate (BER). With an active area of 0.56 by 3 mm, the circuit dissipates 200 mW. The clock-phase margin of 650 ps at 1 Gbits/s for an 80-mV input corresponds to 234 degrees of the clock-cycle phase, which compares favorably to bipolar-circuit performance at similar data rates.

The second device is a clock-recovery circuit that extracts the clock signal from a 2^{23}-long pseudorandom sequence at 1.8 Gbits/s, with 13-ps rms jitter. This chip includes a PLL; a high-frequency, low-jitter VCO; and a phase detector to eliminate the manual phase alignment and high-frequency I/O required in conventional schemes using surface-acoustic-wave (SAW) resonators. The chip has a 0.625-by-0.4-mm active area and dissipates 350 mW. Both the decision and clock-recovery circuits are implemented in a 1-μm NMOS process and operate from 5-V power supplies.



5. A VIDEO DSP CHIP from Matsushita crams 930,000 CMOS transistors on a 12.38-by-12.90-mm die and uses a 16-bit fixed-point data format. The processor has a 16.5-ns instruction cycle at 60 MHz and dissipates 2.4 W at 5 V. Each of three 16-bit-by-1-kword data RAMs (dark areas across the top) has an address generator. The dark areas on the right are 32-bit-by-1-word instruction memories. Discrete-cosine-transform circuitry appears across the bottom of the chip.

SONET Developments

Two device-development efforts for next-generation SONET communications networks are on tap at the ISSCC. SONET communications networks are design to operate at data rates up 10 Gbits/s.

One development effort involves a three-way joint design between Bellcore, Red Bank, N.J.; Rockwell International, Thousand Oaks and Newbury Park, Calif.; and the University of California at San Diego, La Jolla, Calif., to make critical building blocks for SONET systems. These blocks are a high-speed demultiplexer and a phase aligner.

The 1:4 demultiplexer circuit combines features previously unavailable in a single 10-Gbit/s-plus device. These features include output data that's unstaggered in time, an input clock frequency equal to the input data rate, bit-pattern alignment capability, and external alignment only for input-data and input-clock phases. Equipped with bit-rotation control, the demultiplexer circuit consists of two shift registers that operate on different phases of the half-clock rate, enabling alternating bits of the input data stream to be shifted. The chip measures 1.9 by 1.6 mm. Device dissipation is 1.4 W using a –5-V power supply.

The 6.1-GHz phase-aligner chip has an auto-latching feature, and consists of a transition detector, an edge detector, a phase comparator, a phase selector, and read and write registers. Measuring 1.1 by 0.85 mm, the phase-aligner chip dissipates just 0.8 W of power when running from a –5-V power supply.

Both the demultiplexer and the phase aligner chips are fabricated with an AlGaAs/GaAs heterojunction-bipolar-trnasistor (HBT) process. This technology features emit-

VIDEO BUFFER GUARANTEES 0.99V/V GAIN OVER TEMP FOR $4.25*

Sharpest Video Images: 0.01°/0.03% Diff Phase/Gain

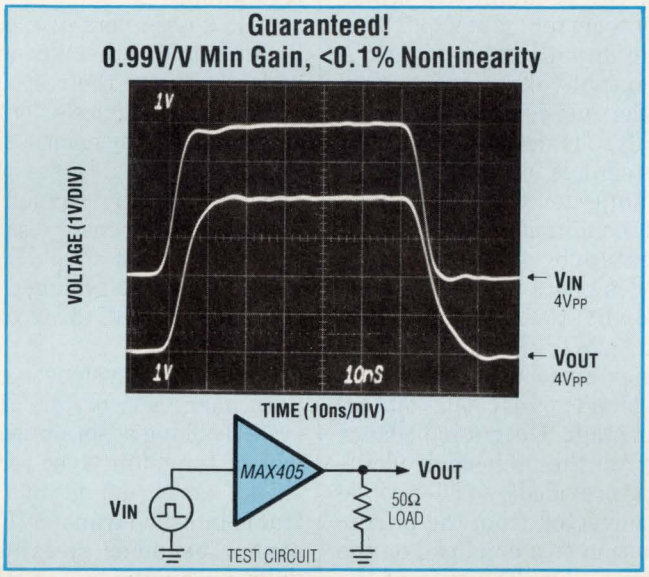
Maxim's new 180MHz MAX405 high-speed, precision buffer amplifier combines superior differential gain and phase with 650V/µs slew rate while operating from ±5V supplies. Gain is guaranteed to be greater than 0.99V/V over -40°C to +85°C, with loads as low as 50Ω. The MAX405 comes in compact 8-pin DIP or SOIC packages and, unlike existing buffers, access to the inverting input allows accurate gain adjustment from 0.99 to 1.1V/V.

Precision

- ♦ 0.01° Differential Phase
- ♦ 0.03% Differential Gain
- ♦ 0.1% Nonlinearity Over Temp
- ♦ 0.99V/V Min Gain Over Temp
- ♦ 0.01Ω ROUT
- ♦ Adjustable Gain

Speed

- ♦ 180MHz Bandwidth
- ♦ 650V/µs Slew Rate
- ♦ 35ns Settling to 0.1%



Drives Four 150Ω Loads

The MAX405, with a guaranteed 60mA continuous output current, directly drives a 50Ω load to ±3V, or as many as four 150Ω loads (four 75Ω back-terminated loads) to ±2.25V. The MAX405 is ideal as a 50Ω and 75Ω coaxial cable driver for NTSC, PAL or SECAM color video signals.

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ter-up/single-heterojunction bipolar transistors, integrated Schottky diodes, NiCr thin-film resistors, and MIM capacitors. The process also features up to three levels of metal interconnect.

The second SONET development effort comes from NEC, which designed a silicon-bipolar chip set for a 10-Gbit/s optical receiver. The chip set consists of a preamplifier, a gain-controllable preamplifier, and a decision circuit. In an optical-receiver application, the preamplifier transforms photocurrent detected by a photodiode into a voltage signal. A constant output-voltage swing is ensured by the gain-controllable amplifier. Finally, the decision circuit regenerates signals from the gain-controllable amplifier when they meet threshold conditions. Each circuit must operate at over 10 GHz.

NEC's designers were able to obtain a 53.4-dBΩ flat transimpedance gain and a 11.2-GHz bandwidth in the preamplifier by focusing on a dual feedback loop (current and voltage) in the gain stage. Output impedance matching to the gain-controllable amplifier is provided by a 50-Ω coplanar line connected from the preamplifier's output to a bond pad on the 0.8-by-0.8-mm chip. The gain of the gain-controllable amplifier has been varied from –5 dB to 15 dB with a 11.4-GHz bandwidth. Maximum peak-to-peak output swing of 0.8 V was measured at 10-dB gain.

The decision circuit is based in a master-slave D-type flip-flop. Both the data and clock inputs are terminated with an on-chip 50-Ω resistor to prevent electrical reflections between the IC and external circuits. According to NEC, the decision circuit's 160-mV sensitivity can recognize an 800-mV signal from the gain-controllable amplifier in a 10-Gbit/s optical receiver. The three circuits are made with the same process used for NEC's dynamic frequency divider discussed earlier.

Image Sensing

Accelerated efforts to perfect image-scanning and high-definition-TV (HDTV) technologies are producing improved designs for image sensing and processing devices, particularly from Japanese manufacturers. NEC Corp., Sangamihara, Japan, for example, has developed a 5000-element CCD linear image sensor with a 100-Mpixel/s data rate and sensitivity of 20.3-μV/electron. Intended for imaging-scanning applications, the device makes it possible to read 11-by-17-in. paper at a rate of 176 sheets/min. This performance translates to a 50-μs line-scan time for reading an 11-in. sheet of paper with 40-dot/in. resolution.

NEC's designers overcame speed limitations of other image sensors, which is due to the reset period required for the device's floating diffusion amplifier, by using a circuit that automatically adjusts the reset-pulse level to the floating diffusion amplifier. The sensor dissipates 160 mW and has a 67.8-dB dynamic range. Using self-aligned implantation allowed NEC to increase device sensitivity.

NEC also developed a 2-Mpixel CCD image sensor for HDTV cameras. By using a 1-in. optical-lens format, a tungsten layer for a photoshield, and a shunt bus line, the frame-interline-transfer (FIT) image sensor becomes suitable for the unique requirements of HDTV with performance featuring a –110-dB smear level. The sensor device has a 1.2-by-10^5 electron-charge-handling capability and a 75-dB dynamic range. Shunt wiring suppresses fixed-pattern noise and minimizes power consumption.

Also designed for HDTV camera applications is a 2/3-in. FIT-CCD image sensor from Sony Corp., Atsugi, Japan. The sensor uses a lenticular microlens array and a scaled output structure to get a 30-nA/lux sensitivity and 70-dB dynamic range. A thin aluminum layer acts as a light shield and performs shunt wiring to improve sensor transfer efficiency. The device acheives a –90-dB smear-reduction ratio. The sensor's image area is 9.6-mm horizontally and 5.4-mm vertically.

Two CCD image sensors from Toshiba Corp., Kawasaki, Japan, are other devices receiving attention at the ISSCC. The first sensor is a 1-in.-optical-format device overlaid with an amorphous-silicon photoconversion layer. It achieves a 110-dB dynamic range and a noise specification of 52 electrons, without capacitive image lag. This performance is credited to a pixel structure that has a storage-diode resetting gate and a bias-charge-injecting diode. The sensor's image area is 14.0-mm horizontally and 7.8-mm vertically, and its aspect ratio is 16:1.

The second Toshiba CCD sensor is a 160-kpixel device with an 85-dB dynamic range. The sensor employs signal-charge summation of four pixels to get a wide dynamic range from the same pixel size used in the company's 2-kpixel sensor. A unit pixel is composed of one photodiode and one CCD transfer electrode with four transfer gates connected to four photodiodes. Charge summation is accomplished by moving the charge packets of four pixels through transfer gates to the vertical CCD registers located at the center of the four pixels.

A final development worth noting comes from Matsushita Electric Industrial Co. Ltd., Osaka, Japan. The firm developed a 2-GOPS, 60-MIPS digital-signal processor with a vector-pipeline architecture for video codec systems. Fabricated in a 0.8-μm CMOS process, the 60-MHz processor has all of the trappings of a conventional digital-signal processor: RAM with address generators, external memory ports, ALUs, registers, a multiplier, and an accumulator *(Fig. 5)*.

The chip also contains a discrete-cosine-transform (DCT) core as a special processing unit. With this array of functions, the processor chip can perform motion-vector detection, motion compensation, DCT/IDCT (inverse DCT), loop filtering and inverse quantizations, and variable-length coding and decoding as specified in CCITT specification H.261.□

How Valuable?	Circle
Highly	532
Moderately	533
Slightly	534

INDUSTRIAL 12-BIT A/D NEEDS NO ADJUSTMENTS OVER -55°C TO +125°C

4- or 1-Channel A/Ds with Track/Hold Maintain ±1 LSB Accuracy

Maxim's new MAX178 and MAX182 are automatically corrected at every conversion, eliminating adjustments and holding total error below 1 LSB. By including a track/hold on chip, accuracy of the complete 12-bit CMOS system is guaranteed over time and temperature, eliminating trimpots, a common source of error and drift. The MAX182 combines a 4-channel multiplexer with all the features of the single-input MAX178.

- **1LSB Total Unadjusted Error Over: -55°C to +125°C & -40°C to +85°C**
- **On-Chip Track/Hold**
- **Easy-to-Drive (R_{IN} < 500MΩ) Inputs**
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- **100% Tested DC and Dynamic Specs**
- **8- or 16-bit µP Interface**
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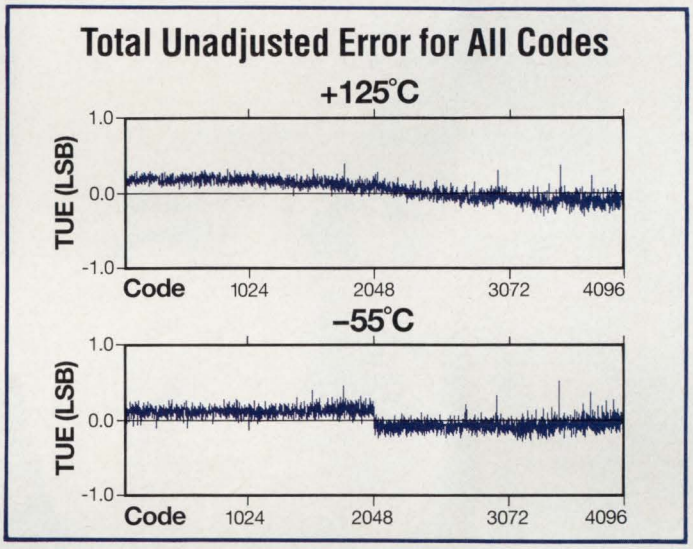

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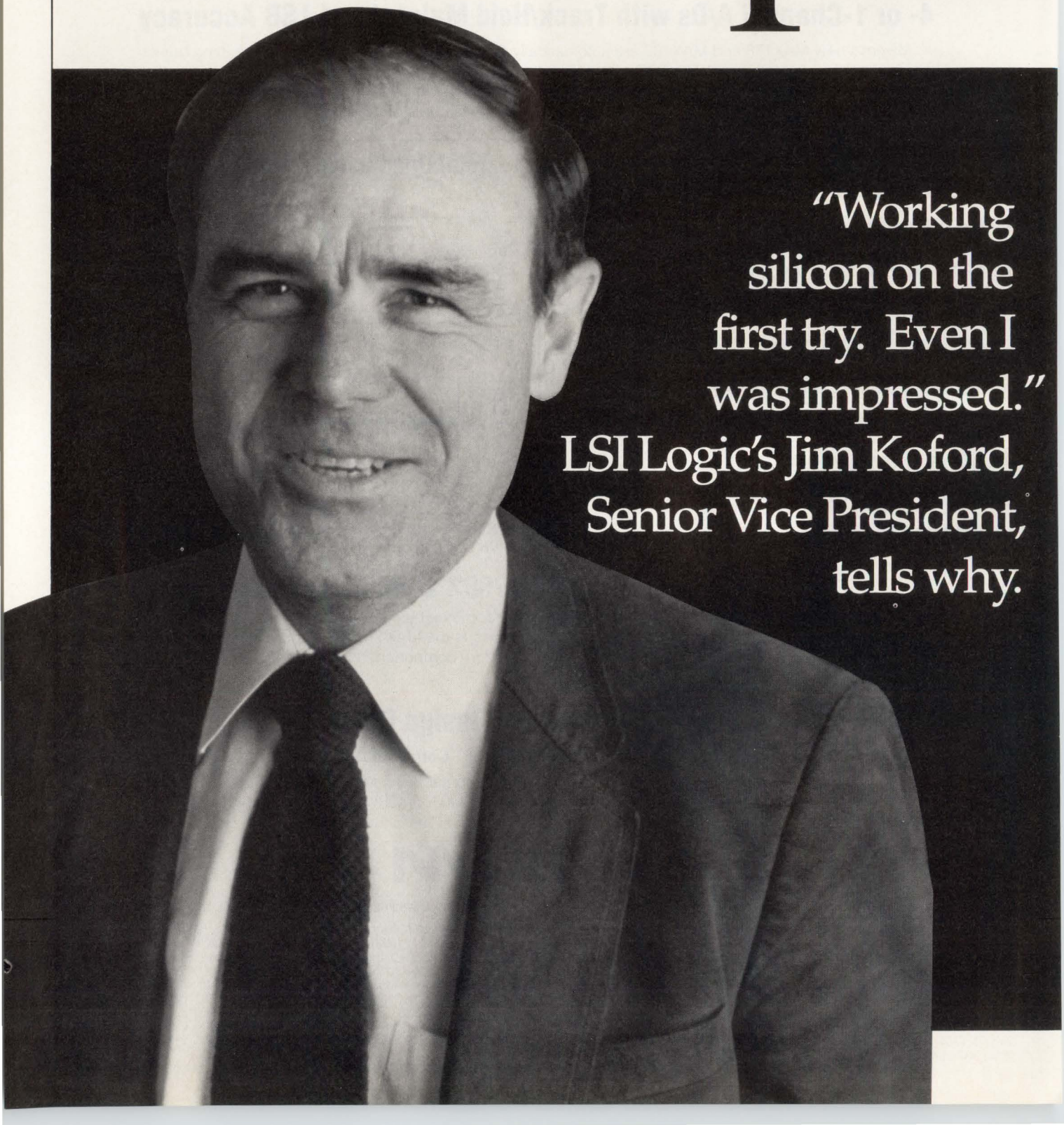

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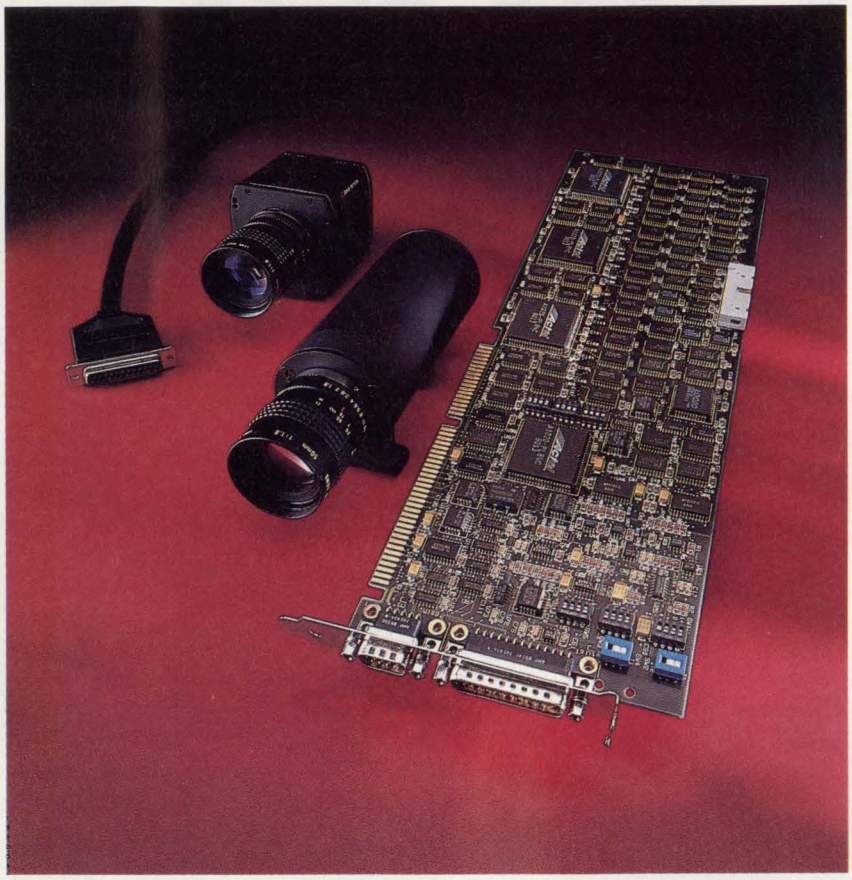

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CIRCLE 94 FOR U.S. RESPONSE CIRCLE 95 FOR RESPONSE OUTSIDE THE U.S.

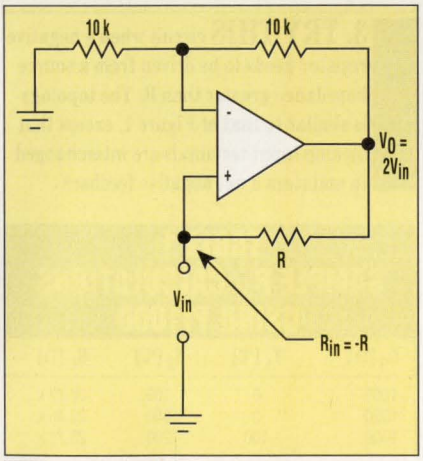
USE THESE HANDY CIRCUIT ELEMENTS TO LINEARIZE RTD TEMPERATURE SENSORS AND ELIMINATE PARASITIC RESISTANCE.

NEGATIVE RESISTORS ARE VERSATILE DESIGN AIDS

By exploiting the advantages accorded by the often-overlooked negative resistor, analog-circuit designers can simplify their designs, improve accuracy, and reduce costs. For example, negative resistor circuit elements can be employed by designers to linearize resistance temperature detector (RTD) temperature sensors and to eliminate unwanted parasitic resistance in interconnecting wiring.

Moreover, designing accurate negative resistors need not be a complicated task. A negative resistor can be accurately synthesized by placing a standard (positive) resistor in the feedback loop of an op amp. Of course, op-amp specifications must always be kept in mind *(see "Limitations of negative resistors," p. 96)*.

To create a precision negative resistor with a value of $-R\Omega$, a positive resistor of $R\Omega$ supplies feedback to an op amp's noninverting input *(Fig. 1)*. The 10-k/10-k resistor network, connected to the op-amp inverting input, places the op amp in a noninverting gain of 2 V/V. A 1-V increase of voltage across a positive resistor of $R\Omega$ would result in a current increase (in amperes) of $1(V)/R(\Omega)$.



1. TO SYNTHESIZE a negative resistor with a value of $-R\Omega$, a positive resistor of $R\Omega$ is placed in the feedback path to an op amp's noninverting input. This circuit is good for source impedances < R.

For the negative resistor circuit, a 1-V increase at the input results in an increase of 2 V at the op amp's output (and the other side of R), resulting in a current increase (in amperes) of $-1(V)/R(\Omega)$. The circuit behaves like a resistor with a value of $-R\Omega$.

For stability, net negative feedback must be maintained around the op amp. The 10-k/10-k network maintains a negative feedback of 1/2. For stability, the source impedance looking into the negative resistor must

R. MARK STITT AND DAVID KUNST
Burr Brown Corp., P. O. Box 11400, Tucson, AZ 85734; (602) 746-7445.

NEGATIVE RESISTORS

be less than R to keep positive feedback less than 1/2.

If the source impedance equals R exactly, an interesting condition exists—the impedance looking into the op-amp noninverting input is ∞.

$-R$ in parallel with $+R = \infty$

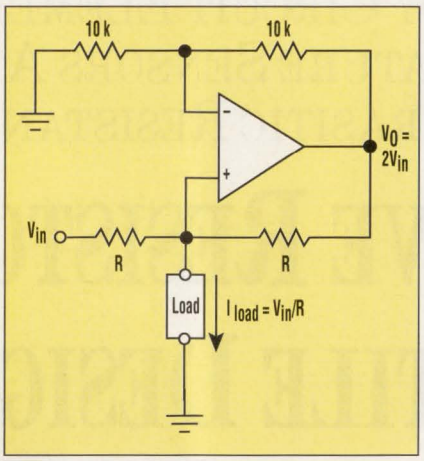
$$\frac{-R \times R}{-R + R} = \frac{-R^2}{0} = \infty \qquad (1)$$

This circuit, sometimes called a Howland current pump, can serve well as a voltage-to-current converter *(Fig. 2)*. Any load resistance connected to the op-amp noninverting input results in net negative feedback satisfying the stability requirement. Output current into the load is V_{in}/R.

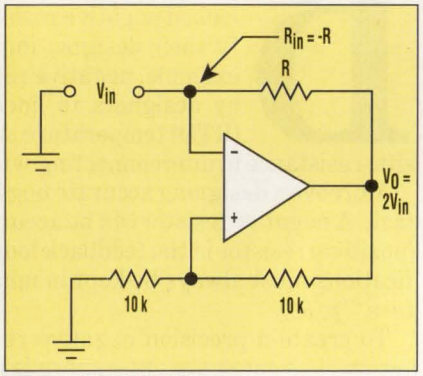
To make a current source, however, you should consider a circuit sometimes called the improved Howland current pump. Similar to the Howland current pump shown in Fig. 2, the circuit uses a difference amplifier with four equal-value resistors, say 10 kΩ or 25 kΩ. The current-sensing resistor R is then connected between the op amp's output and the difference-amplifier resistor, which is typically goes from the op amp's positive input to ground. This point is called the reference connection of a difference amplifier. For a current source, the load is connected to the junction of the reference connection and the current-sensing resistor.

A difference amplifier keeps the voltage between its output and reference connection equal to the differential voltage between its inputs. Therefore, differential signals are amplified while common-mode signals are rejected. In the improved Howland current pump, the voltage across the load becomes the common-mode signal rejected by the difference amplifier. Thus, the output current is constant, regardless of the voltage across the load.

Both of these circuits are described on page 21 of Burr-Brown's application guide AN-165 entitled *Implementation and Applications of Current Sources and Current Receivers*. The guide is available free of charge from the company.



2. ANOTHER circuit example based on negative-resistor concepts is the familiar Howland current pump. The circuit functions as a V-I converter.



3. TRY THIS circuit when a negative resistor needs to be driven from a source impedance greater than R. The topology is similar to that of Figure 1, except that op-amp input terminals are interchanged to maintain a net negative feedback.

TABLE 1: SAMPLE R_L CALCULATIONS USING Pt1000

R_0 [Ω]	T_1 [°C]	T_2 [°C]	R_L [Ω]
1000	0	100	26.73 k
1000	0	850	22.46 k
1000	100	200	25.71 k

For source impedances greater than R, the circuit is the same as Fig. 1 except for the op-amp input terminals, which are interchanged so that net negative feedback is maintained *(Fig. 3)*. It's interesting, and perhaps somewhat surprising at first, to note that op-amp feedback analysis is unchanged when the input connections are interchanged.

LINEARIZING RTDs

Turning to some real-world applications, a negative resistor of the correct value in parallel with a platinum RTD linearizes its response. Temperature is the most often measured physical parameter, and platinum RTDs offer the best overall performance of any commonly used temperature measurement transducer. Pt100, Pt500, and Pt1000 type RTDs are the most frequently used types. The Pt1000 is in general use throughout Europe, the U. S., and in many other parts of the world.

In the range from 0°C to 850°C, the temperature-resistance relationship of a Pt type RTD is:

$$RTD = R_0 \times [1 + (A \times T) + (B \times T^2)]$$

Where:

RTD = dc resistance value of RTD at temperature T (Ω at °C)
R_0 = value of RTD at 0°C (Ω)
R_0 = 100 Ω for Pt100
R_0 = 500 Ω for Pt500
R_0 = 1000 Ω for Pt1000
A = detector constant
$= 3.908 \times 10^{-3}$ ($°C^{-1}$)
B = detector constant
$= -5.802 \times 10^{-7}$ ($°C^{-2}$)

The second-order term, $B \times T^2$, in the temperature-resistance relationship causes a nonlinearity in the response of about 2.7% for a 0°C to 850°C temperature change. A plot of the voltage across an RTD with constant current excitation would show the output increasing linearly with temperature but with a gentle sag.

Increasing the current

TABLE 2: SAMPLE R_Z & R_G VALUES FOR THREE-WIRE TEMPERATURE MEASUREMENT SYSTEM USING Pt1000s WITHOUT LINEARIZATION CIRCUITRY

R_0 [Ω]	T_1 [°C]	T_2 [°C]	R_L [Ω]	R_Z [Ω]	R_G [Ω]
1000	0	100	∞	1004	259.8 k
1000	0	850	∞	1030	34.45 k
1000	100	200	∞	1389	370.5 k

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NEGATIVE RESISTORS

through the RTD by the appropriate amount as temperature increases straightens out the curve to eliminate the sag and mitigate the nonlinearity. Placing a negative resistor in parallel with a constant-current-excited RTD causes the current through the RTD to increase as temperature rises. That's caused by less current going through the negative resistor as the voltage across it increases. With a negative resistor of the proper value, the linearity can be significantly improved.

TABLE 3: SAMPLE R_Z & R_G VALUES FOR THREE-WIRE TEMPERATURE MEASUREMENT SYSTEM USING Pt1000s WITH LINEARIZATION CIRCUITRY

R_0 [Ω]	T_1 [°C]	T_2 [°C]	R_L [Ω]	R_Z [Ω]	R_G [Ω]
1000	0	100	26.73 k	1043	246.1 k
1000	0	850	22.46 k	1085	28.43 k
1000	100	200	25.71 k	1468	345.2 k

A circuit for RTD linearization with a negative resistor can be easily realized *(Fig. 4)*. Comparing the residual nonlinearity (over a 0° to 850°C span) of both a linearized and an uncorrected RTD clearly illustrates the benefits obtained *(Fig. 5)*. The nonlinearity is improved from about 2.7% to about 0.08%, a better than 30-fold improvement. Correction of nonlinearity for smaller spans is even better. The nonlinearity of a 0° to 100°C span can theoretically be improved from about 0.1% to about 0.0004%, a 250-fold improvement.

The value of the negative resistor needed for the best correction of nonlinearity depends on the temperature range of interest. The exact relationship for determining the linearization resistor, R_L, is difficult to evaluate, but the following expression gives excellent results *(Table 1)*:

$$R_L = R_0 \times (27.3 - 0.00455 \times T_1 - 0.0057 \times T_2)$$

$$850°C \geq T_2 \geq T_1 \geq 0°C$$

Where:

R_L = value of negative resistor needed for linearization (Ω)
R_0 = value of RTD at 0°C (Ω)
T_1 = lower temperature in the range of interest (°C)
T_2 = upper temperature in the range of interest (°C)

THREE-WIRE RTD SYSTEMS

Designers can also improve accuracy in a three-wire, RTD-based temperature measuring system by using a negative resistor to cancel wiring resistance. If the RTD is located remotely, as it often is, voltage drops in the interconnecting wiring can cause excessive errors. The typical solution to this problem is to use four wires and make Kelvin connections to the RTD. Two wires carry the current excitation signal to the RTD, and the other two wires sense the voltage across the RTD.

With constant current excitation, voltage drops due to wiring resistance in the excitation wiring don't affect the excitation signal applied to the RTD. In addition, because no current flows in the sense connections, no error-producing voltage drops occur. Therefore, the errors due to wiring resistance are eliminated.

The problem with a four-wire approach is that required additional wiring can be very expensive. The three-wire circuit eliminates one wire *(Fig. 6)*. One of the cable wire resistances is placed in the feedback loop of A_1 to form an effective resistance of $-R_{wire}$ connected to the bottom side of the RTD. The top side of the RTD is connected to a 100-μA excitation current through the second cable resistance of R_{wire}. If the two

LIMITATIONS OF NEGATIVE RESISTORS

Precision negative resistors are inexpensive and easy to fabricate, but they do have limitations. By keeping these limitations in mind, trouble in applying them can be avoided.

Limitations of the negative resistor are due to op amp's limitations and the resistors used to synthesize it. For the negative resistor to function properly, the op amp must operate within its linear input and output range. When used on ±15-V power supplies, most op amps operate properly over an input and output range of at least ±10 V. Monolithic op amps, such as the Burr-Brown OPA445, operate at ±40 V on ±45-V power supplies. The negative resistor is referenced to the op amp input and the output voltage is gained-up by the feedback resistors. If the op amp has a ±10-V output swing and equal-value resistors are used in the feedback, the negative resistor has a ±5-V linear operating range.

The op amp has to supply the current that the negative resistor must deliver. Most general-purpose op amps supply at least ±10 mA. The monolithic OPA541 can supply up to ±10 A.

The dynamic performance of the selected op amp sets the ac performance limitations of the negative resistor. With equal-value feedback resistors, the op amp's noise gain can be up to 2 V/V. Then, the f_{-3dB} frequency of the negative resistor will be one-half the op-amp unity-gain bandwidth. For high-bandwidth applications, consider the OPA671—a FET-input, monolithic op amp with a 35-MHz bandwidth.

The usual dc op-amp specifications set the precision of the negative resistor. The most important specs to consider are bias current, offset voltage, and offset voltage drift. In addition, the ratio matching of the 10-kΩ feedback resistors used in the negative resistor circuit set the actual accuracy of the negative resistor in relation to the positive resistor R_L. Of course, even if the other components are perfect, the negative resistor is only as good at the positive resistor used for R_L.

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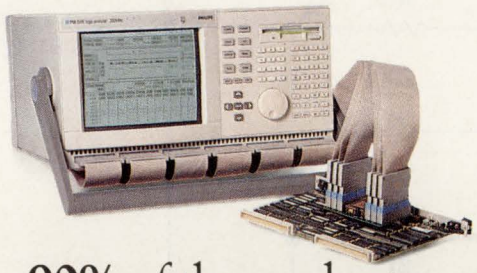

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NEGATIVE RESISTORS

cable wiring resistances match, the effect of the cable wiring resistance is canceled. Any error due to cable wiring resistance mismatch can be trimmed out by shorting the RTD and trimming the ratio of the 10-k feedback resistors of A_1 for 0 V at the noninverting input of A_2.

A second 100-μA current source from a REF200 dual current source drives resistor R_Z to provide output offsetting (zero adjustment). Op-amp A_2 amplifies the voltage output from the temperature sensor to provide full-scale output setting (span adjustment). The gain of A_2 is:

$$1 + (R_G/R_Z)$$

For instance, R_Z can be selected to provide 0 V out at the lower temperature (T_1) in the range of interest, and R_G to provide 10 V out at the higher temperature (T_2) as shown in the following example:

To calculate R_Z and R_G for the three-wire RTD-based temperature measurement system *(Fig. 6, again)*, assume 0 V out at temperature equals T_1 and 10 V out at temperature equals T_2.

$$R_G = R_Z \times \left(\frac{10\ V}{100\ \mu A \times (R_2 - R_1)} - 1 \right) \quad (2)$$

To attain 0 V out at T_1, the value of R_Z in parallel with R_G must be equal to the resistance of the thermal sensor at T_1.

Therefore:

$$R_1 = R_Z \times R_G/(R_Z+R_G)$$
$$R_Z = R_1 + (R_1 \times R_Z)/R_G$$

By substituting R_G from equation 2, the R_Z on the right-hand side falls out and:

$$R_Z = R_1 + R_1 / \left(\frac{10\ V}{100\ \mu A \times (R_2 - R_1)} - 1 \right) \quad (3)$$

To solve for R_Z, use equation 3, substituting R_Z into equation 2 to solve for R_G.

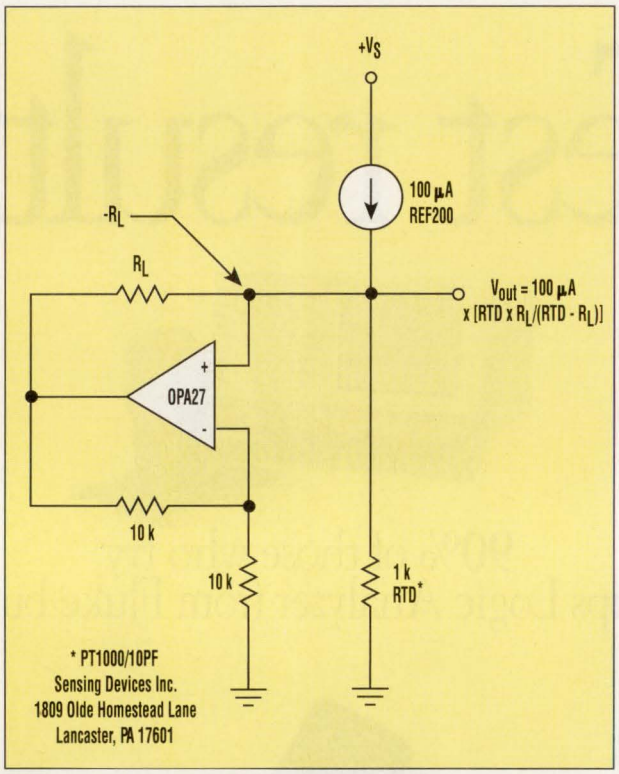
R_1 = resistance of thermal sensor at T_1 (Ω)
R_2 = resistance of thermal sensor at T_2 (Ω)

For a nonlinearized RTD:

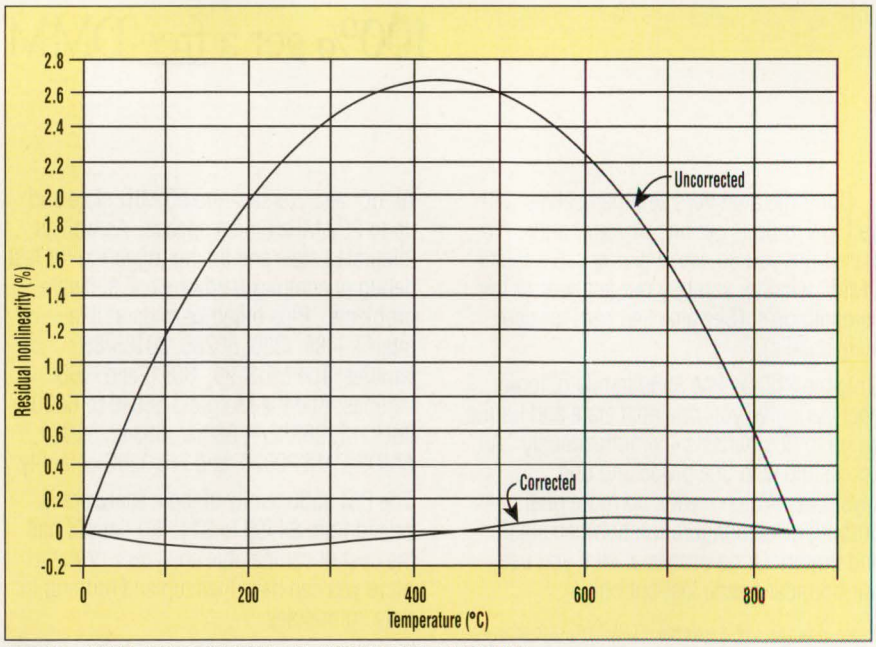
R_1 = RTD at T_1
R_2 = RTD at T_2

The preceding equations can be used to construct a chart of R_Z and R_G for various temperature spans *(Table 2)*.

Because the effects of cable wiring resistance are canceled, the RTD temperature response in the three-wire temperature-measurement system can be linearized with a negative resistor as demonstrated before. Op-amp A_3 is connected the same way as in Figure 4 to provide the linearity correction negative resistance. The same procedures outlined previously can be applied to calculate the value for the linearizing resistor, R_L. Values needed for R_Z



4. A GOOD WAY TO LINEARIZE a platinum RTD is paralleling it with a negative resistor. The value of negative resistance required is determined by the temperature range of interest.



5. WHEN RESIDUAL NONLINEARITY for an uncorrected and corrected RTD is plotted over a 0° to 850°C temperature span, nonlinearity improves from about 2.7% to 0.08%, a better than 30-fold improvement. If a smaller temperature span is chosen, residual nonlinearity can be reduced to even lower levels.

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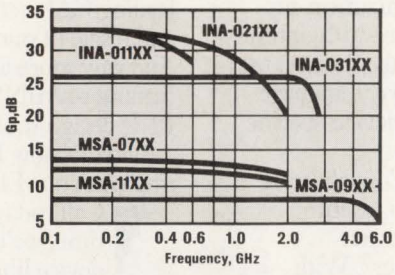
Power Gain vs. Frequency



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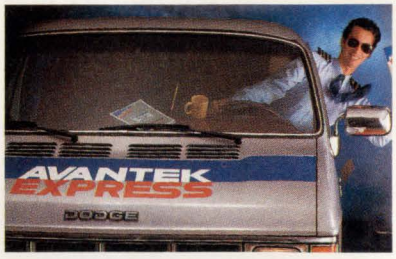

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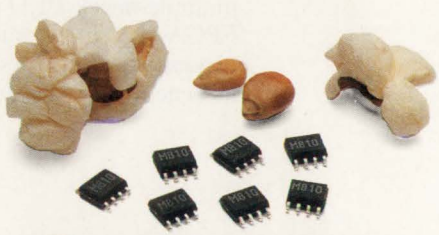

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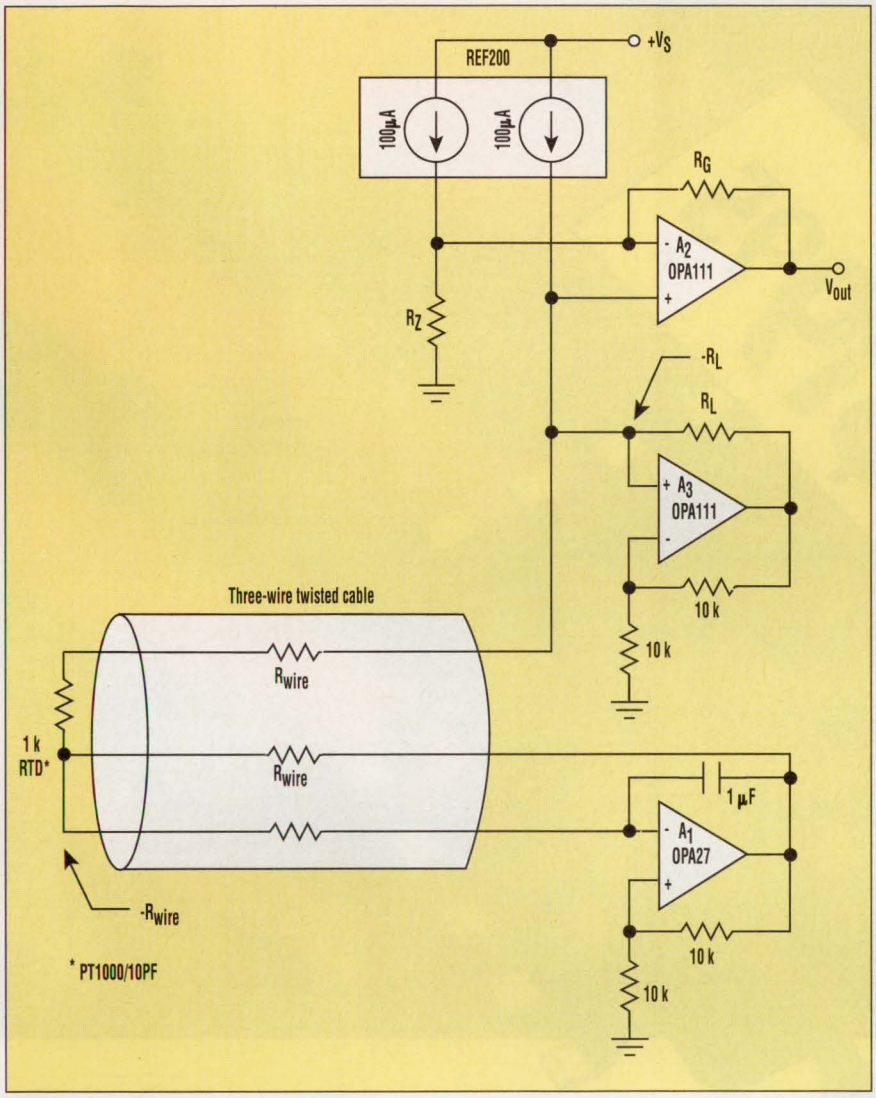
CIRCLE 128

NEGATIVE RESISTORS



6. A NEGATIVE RESISTOR, realized with op-amp A_1, cancels the effects of cable wiring resistances. Op-amp A_2 forms a negative resistor that linearizes the RTD.

and R_G are different because the negative resistance in parallel with the RTD temperature sensor changes the voltage drop across it *(Table 3)*. To calculate values for R_L and R_Z, use the procedure outlined in the previous example, except insert the following relationships for R_1 and R_2. For the linearized RTD:

$$R_1 = \frac{RTD_{(T_1)} \times (-R_L)}{RTD_{(T_1)} - R_L} \quad (4)$$

$$R_2 = \frac{RTD_{(T_2)} \times (-R_L)}{RTD_{(T_2)} - R_L} \quad (5)$$

Where:

$RTD_{(T_1)}$ = RTD at temperature T_1 (Ω)
$RTD_{(T_2)}$ = RTD at temperature T_2 (Ω)

Mark Stitt, a senior engineer at Burr-Brown, manages the design of linear ICs. He received his BSME from the University of Arizona, Tucson.

David Kunst, a senior engineer at Burr-Brown, designs linear ICs. He holds a his BSEE from the University of Arizona.

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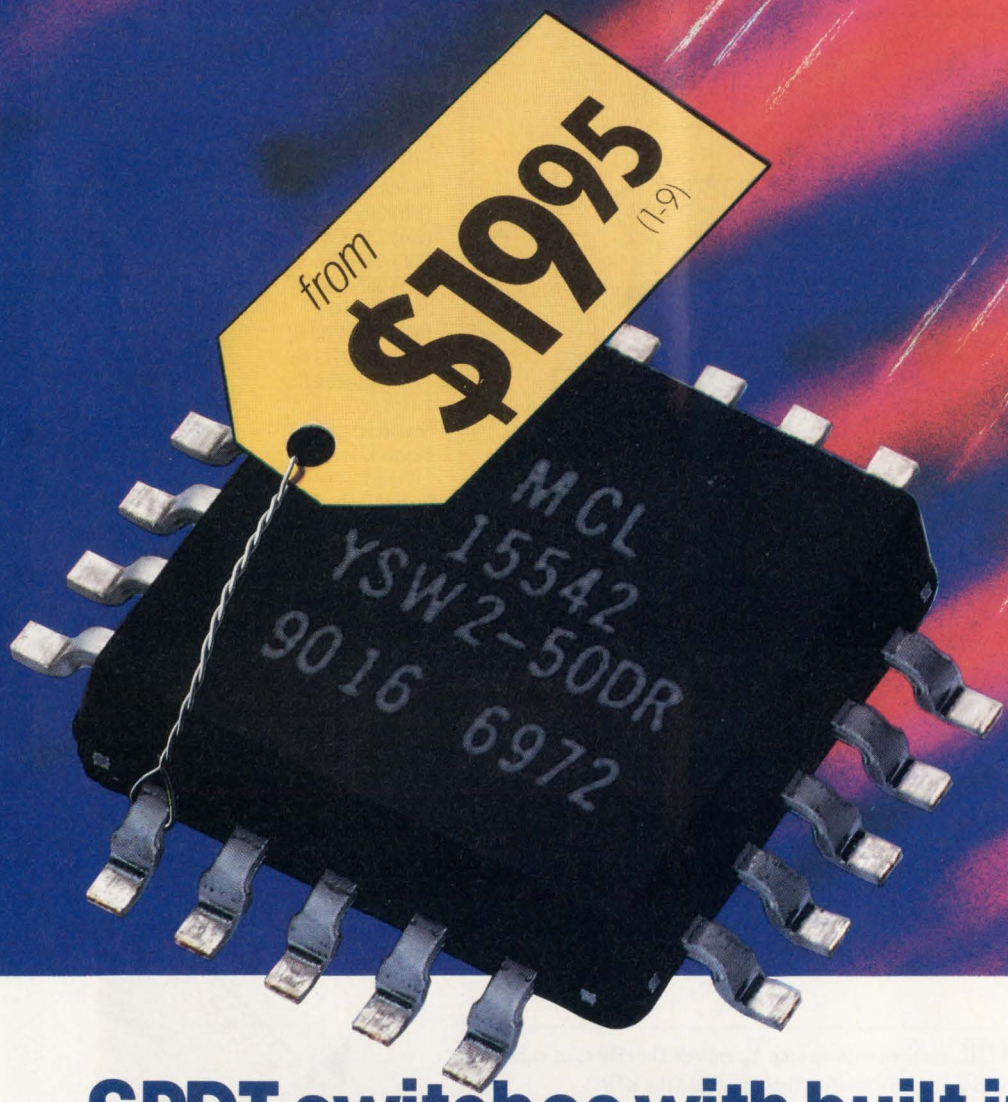

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SPECIFICATIONS (typ)

	Absorptive SPDT YSWA-2-50DR ZYSWA-2-50DR			Reflective SPDT YSW-2-50DR ZYSW-2-50DR		
Frequency (MHz)	dc-500	500-2000	2000-5000	dc-500	500-2000	2000-5000
Ins. Loss (dB)	1.1	1.4	1.9	0.9	1.3	1.4
Isolation (dB)	42	31	20	50	40	28
1dB Comp. (dBm)	18	20	22.5	20	20	24
RF Input (max dBm)	—	20	—	22	22	26
VSWR "on"	1.25	1.35	1.5	1.4	1.4	1.4
Video Bkthru (mV,p/p)	30	30	30	30	30	30
Sw. Spd. (nsec)	3	3	3	3	3	3
Price, $ (1-9 qty)	YSWA-2-50DR (pin) 23.95 ZYSWA-2-50DR (SMA) 69.95			YSW-2-50DR (pin) 19.95 ZYSW-2-50DR (SMA) 59.95		

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CIRCLE 521

DETECT QUADRATURE WAVEFORMS

KENNETH GENE KEESE
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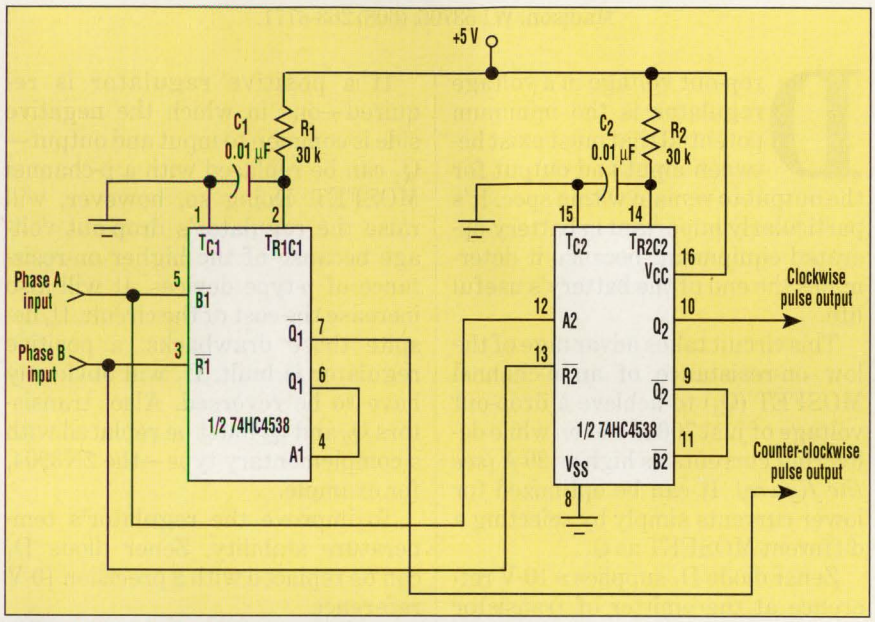


BUILT AROUND a dual monostable multivibrator, this circuit functions as a simple quadrature waveform decoder. R_1–C_1 and R_2–C_2 set the period of the outputs, which should be less than the shortest quadrature pulse seen by the system.

The characteristics of the 74HC4538 dual monostable multivibrator make it ideal for use as a a decoder for digital quadrature devices—that is, devices with two pulsed outputs such that the output information is contained in the phase relationship between the outputs. With this circuit, information from devices of that type—linear or optical rotary encoders, for example—can be obtained easily.

One phase of the quadrature waveform is tied to the rising- and falling-edge trigger inputs from different sections of the 74HC4538 *(see the figure)*. The other phase is tied to both Reset inputs for coordination. The circuit's output depends on whether phase A leads or lags phase B, and only occurs while Reset is high.

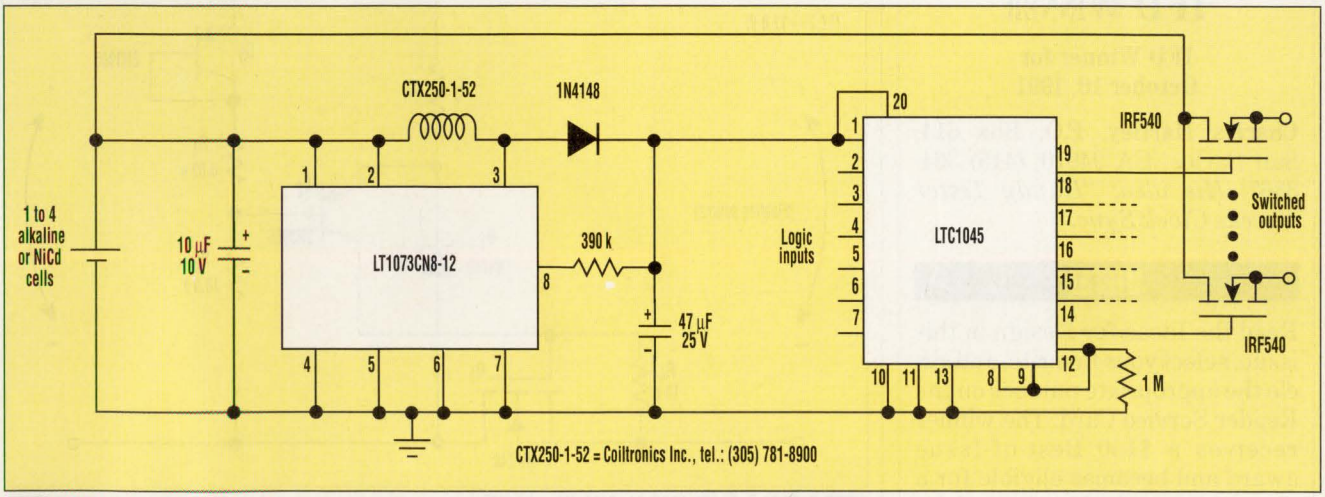
A pair of external resistors and capacitors determine the period of the outputs according to the formula: $t = 0.7 \times RC$. The length of t should be less than the shortest quadrature pulse that the system may encounter. For the values shown in the figure, $t = 210\ \mu s$.□

CIRCLE 522

LEVEL TRANSLATOR SWITCHES MOSFETS

MITCHELL LEE
Linear Technology Corp., 1630 McCarthy Blvd.,
Milpitas, CA 95053-7487; (408) 432-1900.

Power inside battery-operated portable instruments and computers is often "soft-switched" by MOSFETs or transistors so that the product can be completely microprocessor con-



THIS BATTERY-OPERATED CIRCUIT, based on an LTC1045 universal level translator powered by an LT1073 micropower switcher, allows microprocessor control of up to 6 n-channel MOSFETs used as high-side switches.

trolled. This approach also eliminates bulky toggle switches and allows the microprocessor to follow a safe power-down sequence when told to turn off. In addition, selective portions of the instrument or computer can be powered up only as necessary, extending battery life.

With this circuit, up to six independent n-channel MOSFET switches can be controlled by 3.3- or 5-V logic signals *(see the figure)*. Control is accomplished with an LTC1045 universal level translator. While the inputs are logic compatible and switch at approximately 1.6 V, the device's outputs swing from ground to a 16-V rail generated by an LT1073 micropower switcher. This is more than sufficient to fully enhance low-cost, n-channel MOSFETs.

As shown in the figure, the drains are connected to the raw battery supply. However, one or more MOSFETs could switch regulated voltages by simply interconnecting the appropriate drain and source. The MOSFETs should be sized according to the switch dissipation limits and the tolerable switch voltage drop. The IRF540 devices used here switch 1 A with less than a 77-mV drop and 77 mW of power dissipation.

Operation is possible from 1 to 6 V (one to four cells)—ideal for portable equipment. Quiescent current consumption is just 4 mA for one cell, dropping to 1 mA for four cells.□

IFD WINNER

IFD Winner for October 10, 1991

Charles Hartley, P.O. Box 614, San Carlos, CA 94070; (415) 364-3367. *His idea: "Handy Tester Checks Clock Sync."*

VOTE!

Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $150 Best-of-Issue award and becomes eligible for a $1,500 Idea-of-the-Year award.

CIRCLE 523

20-A REGULATOR HAS LOW DROP-OUT

SCOTT ELLINGTON
Space Science and Engineering Center, Univ. of Wisconsin, Madison, WI 53706; (608) 263-6771.

Drop-out voltage in a voltage regulator is the minimum potential that must exist between input and output for the output to remain within spec. It's particularly important in battery-operated equipment, because it determines the end of the battery's useful life.

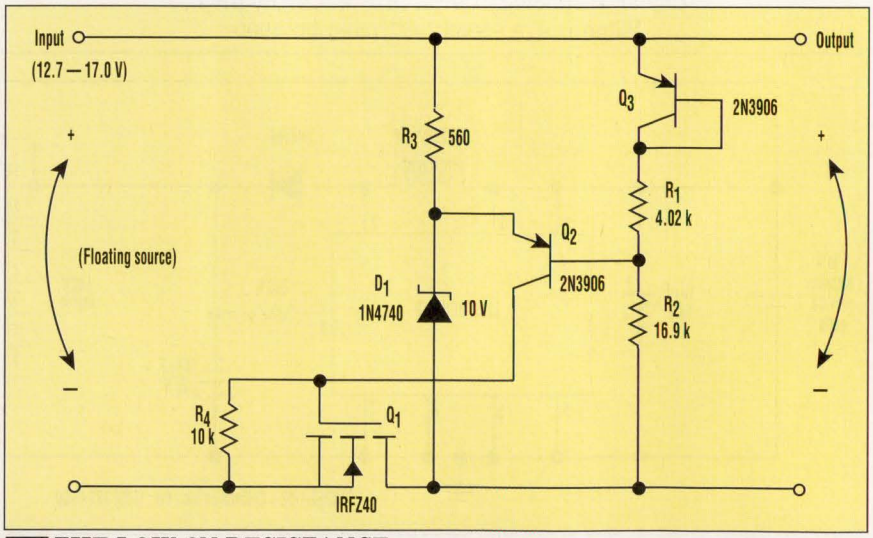
This circuit takes advantage of the low on-resistance of an n-channel MOSFET (Q_1) to achieve a drop-out voltage of just 700 mV even while delivering currents as high as 20 A *(see the figure)*. It can be optimized for lower currents simply by selecting a different MOSFET as Q_1.

Zener diode D_1 supplies a 10-V reference at the emitter of transistor Q_2. To regulate the regulator's output voltage, a fraction of that voltage, as determined by resistors R_1 and R_2, is applied to the base of Q_2. Q_2 then drives the gate of Q_1 to maintain the desired output voltage. Transistor Q_3 is included in the feedback loop to provide temperature compensation for the emitter-base junction of control transistor Q_2.

If a positive regulator is required—one in which the negative side is common to input and output—Q_1 can be replaced with a p-channel MOSFET. Doing so, however, will raise the regulator's drop-out voltage because of the higher on-resistance of p-type devices. It will also increase the cost of the circuit. If, despite those drawbacks, a positive regulator is built, D_1 will obviously have to be reversed. Also, transistors Q_2 and Q_3 must be replaced with a complementary type—the 2N3904, for example.

To improve the regulator's temperature stability, Zener diode D_1 can be replaced with a precision 10-V reference.

With the components shown, the regulator delivers an output of 12.0 V from inputs as low as 12.7 V. To obtain a different output voltage, simply change R_1 and R_2. For operation below 10 V, Q_1 should be replaced with a low-threshold device like an MTP50N05EL, and D_1 should be replaced with a lower-voltage Zener diode or a 5-V reference.□



THE LOW ON-RESISTANCE of the IRFZ-40 MOSFET gives this voltage regulator a drop-out voltage of just 700 mV. The MOSFET must be fitted with an adequate heat sink.

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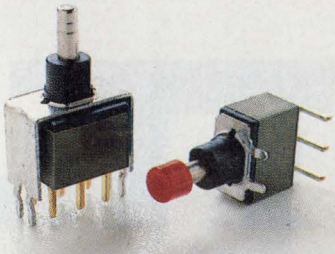

Washable M2B subminiature pushbuttons feature very-light-touch, snap-acting contacts. Straight, right angle, vertical PC terminals.

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New ND switch is half the size of ordinary binary coded DIP rotaries. Washable and universal footprint pattern.

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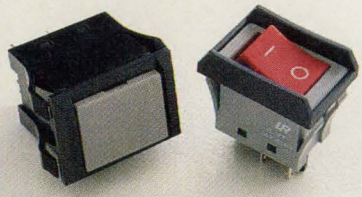
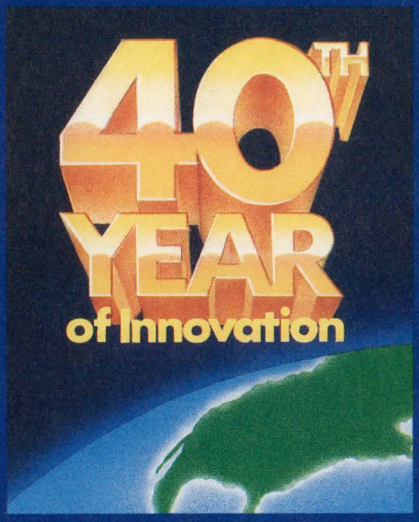
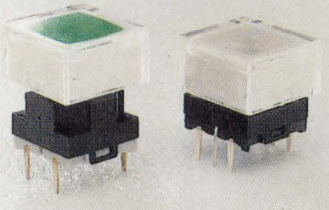


JW rockers & JP pushbuttons. High inrush current resistance protects against contact welding. TV-8 (16 Amp) + TV-5 (10 Amp) Rated.



WORTH A MILLION



Million operations from unique LED illuminated JB keypad switch. Red, green or yellow LED options.

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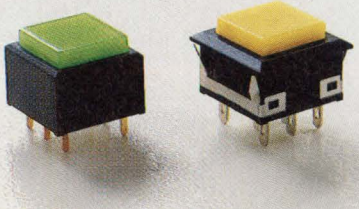
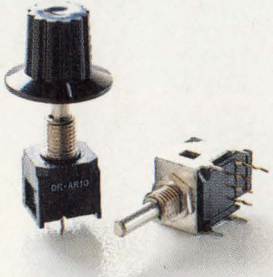


Logic-level for PCB or power rating for snap-in panel mounting, from very low-profile UB pushbuttons with full-face LED illumination.

TURNING POINT



Washable Binary Coded DIP rotary DR-A switch can be PC or panel mounted. Crisp operation. Right angle or straight terminals.

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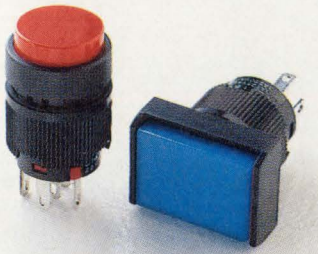
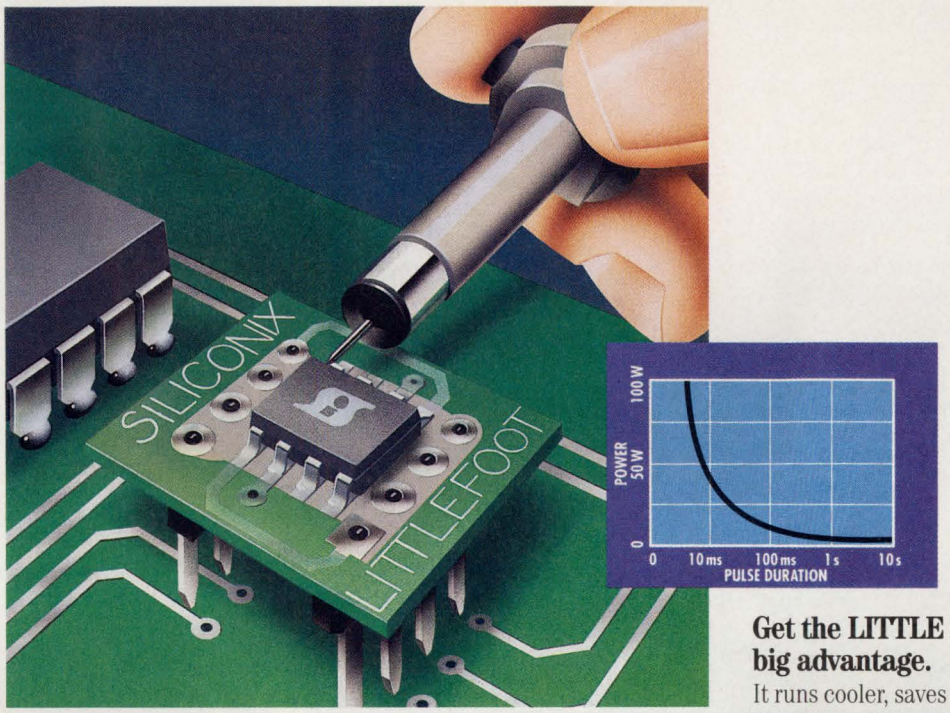


YB pushbutton yields literally 100,000+ part numbers with variations in mounting, illumination, circuitry and color.

LITTLE FOOT.

"SIZE IS POWER" DEBUNKING THE MYTH



The myth of mass.
Many say, "Size is power." We say different, but understand a few of you may have doubts. Sometimes it's just hard to believe a device so small can dissipate so much power. A full 2 watts.

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It also delivers the highest current rating available, up to 3.5 amps, in a tiny SOIC-8 package. This results from a combination of our unique copper lead-frame design that conducts heat directly from the backside of the die to optimize thermal performance, and our SiMOS 2.5 (2.5 million cells/sq.in.) technology that creates the industry's highest power density and lowest on-resistance. Just what you need for motor control, load switching, and DC/DC conversion in applications where space and heat are critical constraints.

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LITTLE FOOT is designed for manufacturability.
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It runs cooler, saves space, improves reliability, increases efficiency, simplifies design, extends battery life, reduces costs, and cuts time to market. With this kind of designed-in performance it's not surprising that LITTLE FOOT sales have surpassed 20 million devices.

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- P-ch MOSFETs (duals & singles)
- N- & P-ch MOSFETs

Voltage:	20-50 V (200 V coming)
On-resistance:	50-300 mΩ
Current Rating:	4.5 A
Power Dissipation:	2 W

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Hillsboro, Oregon 97124

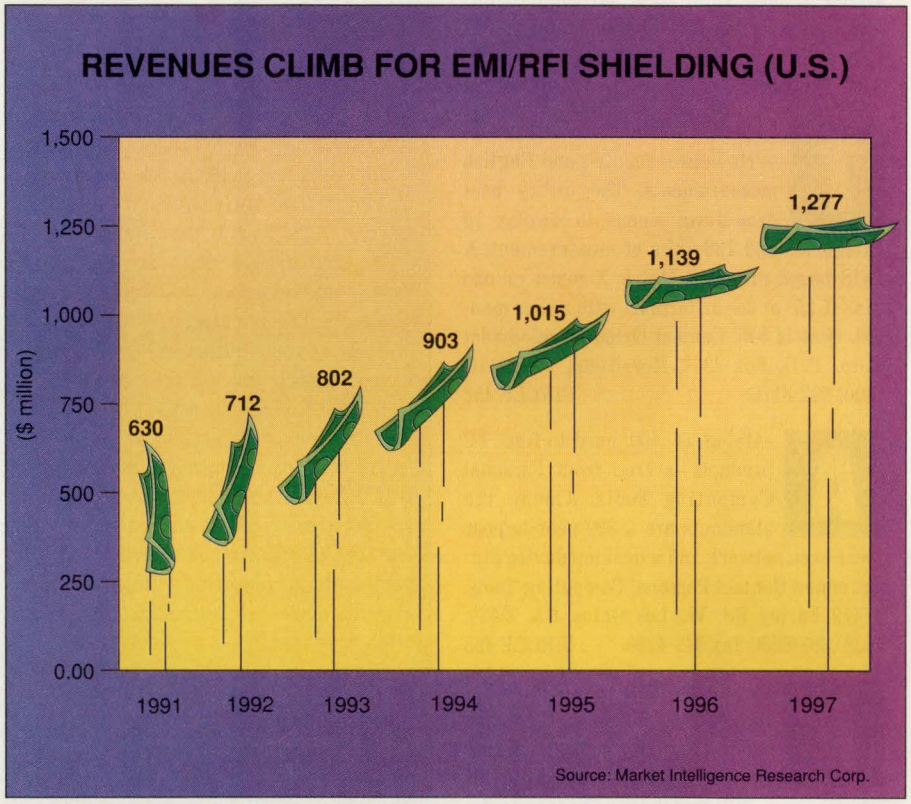
ELECTRONIC DESIGN

QUICK LOOK

EDITED BY SHERRIE VAN TYLE

MARKET FACTS

Revenues in the market for shielding electromagnetic and radio frequency interference (EMI/RFI) should double between 1990 and 1997 to more than $1 billion, according to a report from Market Intelligence Research Corp. Revenues will grow an average of 12.8% a year in that period. Better shielding is needed for new compact, voltage-sensitive semiconductors, says the Mountain View, Calif., market researcher. Also, cellular phones, pagers, and high-definition TVs are straining the overcrowded RF spectrum, requiring shielding. Use of low power circuitry for fast, high-density ICs boosts demand for EMI/RFI shielding. Despite cutbacks in defense spending, the retrofit market for military equipment will fuel demand for shielding products. Demand for shielding products should stay strong in U. S. aerospace, automotive, medical instrumentation, telecommunications, and test and measurement equipment. Eastern European and Russian markets also have potential for growth.



QUICK NEWS

The federal government has $72 billion to spend for R&D in fiscal 1992. About $475 million of the money will be set aside for small companies under the 11-agency Small Business Innovation Research (SBIR) program. About 3000 small high-tech companies have been supported in SBIR's nine years.

To spread the word, the National SBIR Conference will be held in Atlanta, Ga. April 27–29. At the conference small companies learn how to win and make use of government prime and subcontracts, with 100 program managers and specialists participating. Among the agencies to be represented are the Commerce Department (NIST), DoD, Darpa, NASA, National Science Foundation, Nuclear Regulatory Commission, and Small Business Administration. Companies include Honeywell, Allied Signal, Boeing, Cray Research, General Dynamics, General Motors, IBM, Lockheed, Martin Marietta, and 3M.

To register or for further information, contact Foresight Science & Technology, P. O. Box 6157, Delray Beach, FL 33484-6157 or call (407) 274-4005. Registration is $115, which covers sessions, materials, and six meals. Foresight is contractor for conference sponsors, the National Science Foundation, and the Department of Defense.

QUICK NEWS: CONFERENCES

A conference on real-time development will be held in San Jose, Calif., March 16–17, 1992. The Windays USA Real-time Developers Forum will take up issues such as embedded applications development, operating systems performance and functionality, and cross-development environments. Registration fee for the forum is $695. Fee for a VxWorks tutorial is $250. Registration for a national VxWorks Users Group Meeting is $50. For information, contact the conference sponsor, Wind River Systems, P. O. Box 2035, Andover, MA 01810; (800) 767-2336.

A two-day conference on improving the software testing process will be held in various U. S. cities between March 9 and April 14. Sponsored by Data-Tech Institute, the seminar covers partitioning tests for thorough execution and review, debugging, structured testing procedures, and CASE tools. Testing procedures apply to all hardware, language, and development methods, the institute says. Course fee is $795. Contact Data-Tech Institute, P. O. Box 2429, Clifton, NJ 07015; (201) 478-5400.

OFFERS YOU CAN'T REFUSE

A six-page application note is free from Datel. Note AN-3 is a reprint of *Electronic Design*'s design application "Data Converters: Getting to Know Dynamic Specifications" by Robert Leonard. After a review of A/D architectures, the note covers dynamic, frequency domain specifications, including signal-to-noise ratio, total harmonic distortion, and effective bits. Contact Datel Inc., 11 Cabot Blvd., Mansfield, MA 02048; (508) 339-3000; fax 339-6356. CIRCLE 451

The Metric X conversion utility converts between metric and English measurements. The utility uses drop-down menus to display 10 categories and 138 units of measurement. A DOS-based program, Metric X comes on one disk (5.25- or 3.5-in. format) with a user manual. Cost is $15. Contact Orion Development Corp., P. O. Box 2323, Merrifield, VA 22116; (800) 992-8170. CIRCLE 452

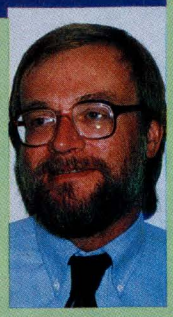
A catalog of 400 hard-to-find PC products is free from Personal Computing Tools. Among the standouts are a $99 peer-to-peer local-area network and a desktop device programmer. Contact Personal Computing Tools, 17419 Farley Rd. W., Los Gatos, CA 95030; (408) 395-6600; fax 345-4260. CIRCLE 453

A free demo disk is available for Hypersignal-Macro, a standalone superset of Hypersignal-Workstation DSP software. New to this version are DSP/acquisition board device drivers, overlaid-trace display, system decibel calibration based on real-time analog input, real-time system response compensation in the frequency domain, and new documentation. Contact Signalogic, 9704 Skillman, Suite 111, Dallas, TX 75243; (214) 343-0069. CIRCLE 454

Measuring microwave devices and components often requires constant input power. A free application note details a highly accurate, automated procedure for flattening power at all measured frequencies using Wiltron's 360B vector network analyzer and an external power meter. Request the 12-page Flat Test Port Power Correction Application Note. Also free is a 12-page data sheet on the 360B vector analyzer, which enables a user to display two traces on one graph. Contact the Wiltron Co., 490 Jarvis Dr., Morgan Hill, CA 95037-2809; (408) 778-2000, fax (408) 778-0239. CIRCLE 455

KMET'S KORNER

...Perspectives on Time-to-Market



BY RON KMETOVICZ
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458; fax (408) 253-6085

Now that a working knowledge of the TTM (time to market), BEAR (break-even after release), and BET (break-even time) measures have been developed, let's talk about using that information. As you may recall from previous columns, BET = TTM + BEAR.

An overall sense of urgency is captured by striving to keep BET as low as possible. The major functions of research and development, marketing, and manufacturing have a vested interest in minimizing the metric of break-even time.

Research and development—along with manufacturing—tend to take ownership of the time-to-market portion with support from marketing. Meanwhile, BEAR is championed by marketing and manufacturing with support from research and development. As a function of time, the contribution, or lack thereof, of each function, influences the break-even-time metric through time to market and break even after release.

Besides giving urgency visibility, BET measures if the product sells enough to recover investment expense. The link between product development and the customer's willingness to part with his/her money is established. All functions are held accountable for TTM and BEAR. Research and development can't take TTM to low extremes while producing a product that doesn't sell. Research and development must design and develop products that the market wants; that manufacturing can build; and that can be effectively marketed, distributed, sold, and supported. In the same manner, other functions' impact on financial performance is made visible through their contribution to time-to-market, break-even time after release, or both.

Time-to-market and break-even after release are highly influenced by product-development classification. First-of-a-kind efforts can have an extended TTM and an extended BEAR. Time-to-market is lengthy because promoting a new concept takes extended time and product development takes place in a sea of technical and market uncertainty. Likewise, expect BEAR to extend for a period as manufacturing, distribution, marketing, and sales methods are produced to serve the newly created market. Time-to-market can range from 24 to 60 months while BEAR spans 12 to 36 months. This leads to a break-even time ranging from 36 to 96 months.

In contrast, me-too products have to be done quickly. Time-to-market can be held to 12 to 24 months. Because the infrastructure is in place, the BEAR for a "good" product can be achieved in 6 to 18 months. As such, break-even time for the "me-too" classification is realized in 18 to 42 months.

Break-even time for next-generation products is usually quite long. Time-to-market expands because it takes time to figure out how to replace an existing product line. At the same time, BEAR extends because of cannibalization of existing product sales and a decline in profit margin. Expect time-to-market to at least equal the TTM of the pioneering first-of-a-kind effort. With good fortune, BEAR can be achieved in 12 to 24 months.

Derivatives have the potential for very short TTM and short BEAR. Six- to twelve-month time-to-market figures are not unusual. Along the same lines, BEAR can be achieved in 6 to 12 months. As such, BET for derivative classifications is often achieved in 12 to 24 months.

To internalize this discussion, assemble data within your organization on TTM, BEAR, and BET sorted by product classification. It should be both an interesting and an informative exercise.

Ron Kmetovicz will lead a Time-to-Market seminar entitled "Speeding New Ideas to the Marketplace" at Santa Clara University's Executive Development Center, to be held March 19, 1992. For more information call Elmer Luthman, center director, at (408) 554-4521; fax (408) 554-4571.

Oh no. Please, not now. Not with manufacturing release next week.

THE PROTOTYPE DOESN'T WORK.

Six ASICs, fifteen PLDs and the whole thing's gone south. Maybe I should go south too. Yeah, hop a bus. Head for Mexico.

THE PROTOTYPE DOESN'T WORK.

Software? Could be. Hardware? Might be. So where do I start? At the beginning, of course. And just where is that, smart guy?

THE PROTOTYPE DOESN'T WORK.

And my performance review comes up next month. Maybe they'll just forget about all this, right? Yeah. Sure.

THE PROTOTYPE DOESN'T WORK.

Wait. What about that glitch in the handshake on the first pass? Couldn't reproduce it. Maybe it just reproduced itself.

THE PROTOTYPE DOESN'T WORK.

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CIRCLE 168 FOR U.S. RESPONSE

CIRCLE 169 FOR RESPONSE OUTSIDE THE U.S.

QUICKLOOK

HOT PC PRODUCTS

Picking CASE (computer-aided software engineering) tools should get easier with the help of a PC-based database. Toolfinder cross-references tools using 400 attributes in eight categories—application types, development tasks, methods and notations, platforms, operating systems, databases, networks, and languages. The program accompanies a 350-page Case Outlook Guide to Products and Services, which describes 850 tools from 300 suppliers.

The guide has nine reference sections, a glossary, and a report on technical trends in automating software design, along with market information. A workstation section includes a review of the leading computing platforms for CASE, platform features and prices, and a cost-per-seat analysis for modern CASE environments.

The database and guide come with two reports: A Case Outlook Software Tool Census has 27 graphs showing how the 850 tools are distributed by application type, development tasks, methods and notations, platforms, operating systems, and so forth. Also included is an analysis of tool trends, areas of opportunity, and emerging tool niches. A Case Outlook Software Tool Topology has 300 graphs representing the industry's CASE suppliers and how their products address the software development life cycle.

The package, which has a list price of $195, is available from CASE Consulting Group, 11830 Kerr Parkway, Suite 315, Lake Oswego, OR 97035; (503) 245-6880; fax (503) 245-6935.

BEST SELLERS

Which technical books are the most popular in Silicon Valley?

ELECTRONICS:

1. *C Language Algorithms for Digital Signal Processing* by Paul Embree and Bruce Kimble. Prentice-Hall, 1990. ***$55.***
2. *Switching Power Supply Design* by Abraham Pressman. McGraw-Hill, 1991. ***$49.95.***
3. *Noise Reduction Techniques in Electronics* by Henry Ott. Wiley, 1988. ***$51.95.***
4. *Art of Electronics, 2nd ed.*, by Paul Horowitz and Winfield Hill. Cambridge University Press, 1989. ***$54.50.***
5. *Spice for Circuits and Electronics Using PSpice* by Mohammed Rashid. Prentice-Hall, 1990. ***$25.80.***

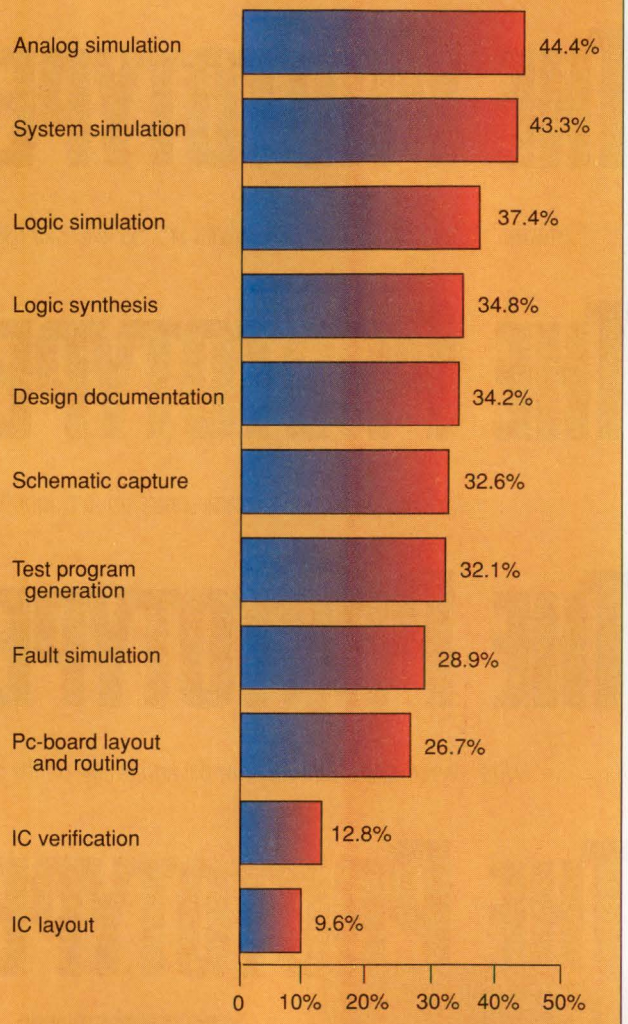
COMPUTER SCIENCE:

1. *Learning GNU EMACS* by Debra Cameron and Bill Rosenblatt. O'Reilly, 1991. ***$27.95.***
2. *C++ Programming Language*, second edition, by Bjarne Stroustrup. Addison-Wesley, 1991. ***$34.50.***
3. *Object-oriented Technnology: A Manager's Guide*, by David Taylor. Addison-Wesley, 1991. ***$19.50.***
4. *C Programming Language*, second edition, by Brian Kernigan and Dennie Ritchie. Prentice-Hall, 1991. ***$34.***
5. *Essential System Administration* by Aeleen Frisch. O'Reilly, 1991. ***$29.95.***

This list is compiled for *Electronic Design* by Stacey's Bookstore, 219 University Ave., Palo Alto, CA 94301; (415) 326-0681; fax (415) 326-0693.

CAD/CAE SURVEY

WITH IMPROVED TOOLS, WHICH FUNCTIONS WOULD YOU USE MORE OFTEN?



Source: a survey of Electronic Design readers by The Adams Co., Palo Alto, Calif.

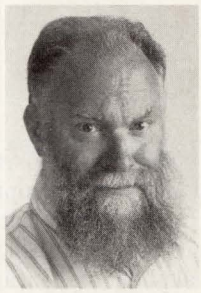
Readers gave more than one answer to question.

DID YOU KNOW?

... that engineering design quality greatly affects profitability, according to 77% of electronics companies polled in a recent survey. To improve product quality and ease of manufacturing, engineering and manufacturing are working more closely together, say 54% of those polled. Increasing emphasis on product quality and reliability stems in part from foreign competition, especially Pacific Rim countries. Two-thirds of companies polled say they are experiencing foreign competition, and half say it's on the rise.

A survey of 311 electronics companies by the American Electronics Association

PEASE PORRIDGE



BOB'S MAILBOX

Sir:

I love you! (Do not get your hopes up, I am 50, overweight...and male). I was beginning to think I was the only engineer left in the world who still thought there was merit in breadboards, or common sense designs for that matter.

I am fighting a losing battle against the invasion of simulated labs (plastic labs as a friend put it). Recently, the administration at the engineering school where I teach was talked into replacing our logic design laboratory (undergraduate) with a network of workstations.

I have been trying to convince everybody that such an action was a huge mistake, and that the only people who should have (limited) access to such tools were *experienced* designers who could instinctively know when they were being fed rubbish. But I have been sadly outgunned by those (almost all) around me. The main argument against me and my position has always been: "that is how INDUSTRY does it."

My contention that such machines are a hindrance to learning and should be banned from a learning environment was always received with total disbelief, because "those are the tools REAL ENGINEERS use to improve their productivity."

I also got *absolutely nowhere* when pointing out that those engineers who do derive advantages from such tools are people who learned their trade *without* these machines. They use them to *supplement* their knowledge and abilities rather than *replace* them.

It gives me immense pleasure to see that someone else (with maybe a limited knowledge of the real world, not an academic type like myself) seems to be fighting the same battle. I might not win the war, but I shall not be alone in my abject defeat.

What can we do? These people will not read (at least not seriously) such "sour grapes" prose as yours. After all, they *know* that is how INDUSTRY does it. I sometimes get the feeling technology is shooting itself in the foot. By using technology to replace thinking, we are freezing it at the state the software engineers used to design their wares. And I sense that, a generation or so from now, when everyone else has forgotten how a transistor works, and the computers start to die off, nobody will be left to fix them or design new ones.

Are we seeing the last technical generation? Will the computer simulations do to creativity what the calculator has already done to mental arithmetic? I fear it might, and I am at a loss on how to stop it. Taking a hammer to the darned things will only divert more funds to fixing and protecting them. Maybe a more direct plea from people such as yourself to university planners would help, since it is not "politically correct" to criticize computers within our walls. People were less defensive of their religion during the Spanish inquisition than they are of their computers these days. Anything you can do would be greatly appreciated.

GEORGES-EMILÉ APRIL
Professor of Electrical Engineering
École Polytechnique de Montréal,
Montréal P.Q, Canada

I hear you! I agree.—RAP

Dear Bob:

I enjoyed your article "What's All This Spicey Stuff, Anyhow? (Part III)" in the October 10, 1991 issue. Unfortunately, the main idea of the article expressed with a Russian proverb "Trust, but verify" was somewhat turned upside down for me, because *Proverai no doverai* means exactly the opposite: "Verify, but trust." The reason for this confusion is that you misplaced two words. This proverb should read *Doverai no proverai*. Being a recent newcomer from Russia to the U.S., I couldn't help but notice this little mistake.

MIKE KORKIN
Development engineer
Fischer Imaging Corp.
Denver, Colo.

I sorry. Thanks for the correction.—RAP

Dear Bob:

Gee, I wish we had more sensible people like you. One of my young engineers came to me with the plaintive cry that his SCR R/C snubber circuit was oscillating!

He had set up the circuit in Tutsim, or something of the sort, and kept juggling component values in an effort to "stabilize" it. He had not even examined what he was doing far enough to realize he had a passive circuit oscillating. The problem, of course, was the default step size on the canned program.

KEITH H. SUEKER, PE
Engineering manager
Robicon Corp.
Pittsburgh, Pa.

Exactly my point!—RAP

Dear Mr. Pease:

I have read your article in the October 10, 1991 issue, "What's All This Spicey Stuff, Anyhow? (Part III)", and I find that I agree with most of what you say.

The current debate on the extent to which universities should rely on simulation in the teaching of electronics has an interesting historical parallel. Twenty years ago, many universities replaced their electrical machine labs with analog (and later digital) simulations. The "old school" regarded this as a backward step in the education of practical electrical engineers.

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PEASE PORRIDGE

There is one part of your article on which I would appreciate some further elaboration: the paragraph on metastability. Since this is a statistical phenomenon, a deterministic circuit simulation is not going to give much directly usable information, even if there were no artifacts due to numerical problems.

However, the probabilistic model for the metastable behavior of a latch is simple, and has been thoroughly tested over a number of years. The circuit design problem is finding the parameters to use in the statistical model, and then to optimize the circuit with respect to its metastable operation. Here, the use of Spice can help. (Many papers have been published on this topic, not all from universities.) Obviously, the only model in which you can have full confidence is the breadboard. But CAD can help, in my opinion. Any comments?

MARTIN J.P. BOLTON
Inmos Ltd.
Bristol, England

Spice can develop the facts you need to study metastability, but can't do it directly.—RAP

Dear Bob:

Thank you for writing all those great articles. I save all of them and share your views of this linear world.

Would you believe that strain-gauge power supplies are now extinct? I sure wish I could still buy one, but have been unable to find a single vendor that still sells them. I think we need to raise a hue and cry about this. I have always considered them one of the true basic building blocks and are about as close to batteries as you can get. Too many power supplies today have high capacitance between windings and they transfer line noise right into the circuit we are trying to clean up. Once in a while, we can find a simple foil shield between windings. But almost no one will tell us about it, much less give any specs on the strays.

When you specifically buy an isolation transformer, the single shield seems to be added by the vendor as an afterthought, and there are no specs. And to add insult to injury, it is arbitrarily grounded at the case and/or returned to the third wire on the line cord.

I am convinced that nobody makes decent power transformers anymore. Any bench supply should have carefully isolated windings with adequate shielding from the power line. A little care in that area would save us hours later on when the noise hunt begins.

In the meantime, I'm going to be watching for old strain-gauge supplies in the junk stores. There should be a lot of them out there, unwanted and unused. Maybe it's about time to rediscover what they can do.

NEIL IVERSON
Boeing Co.
Seattle, Wash.

Can anybody recommend where to buy good, well-isolated supplies; or a good transformer so you can make them?—RAP

Dear Sir:

Please keep up the good work. I have read trade publications for ten years now and have never regularly read a columnist. But now I read your column.

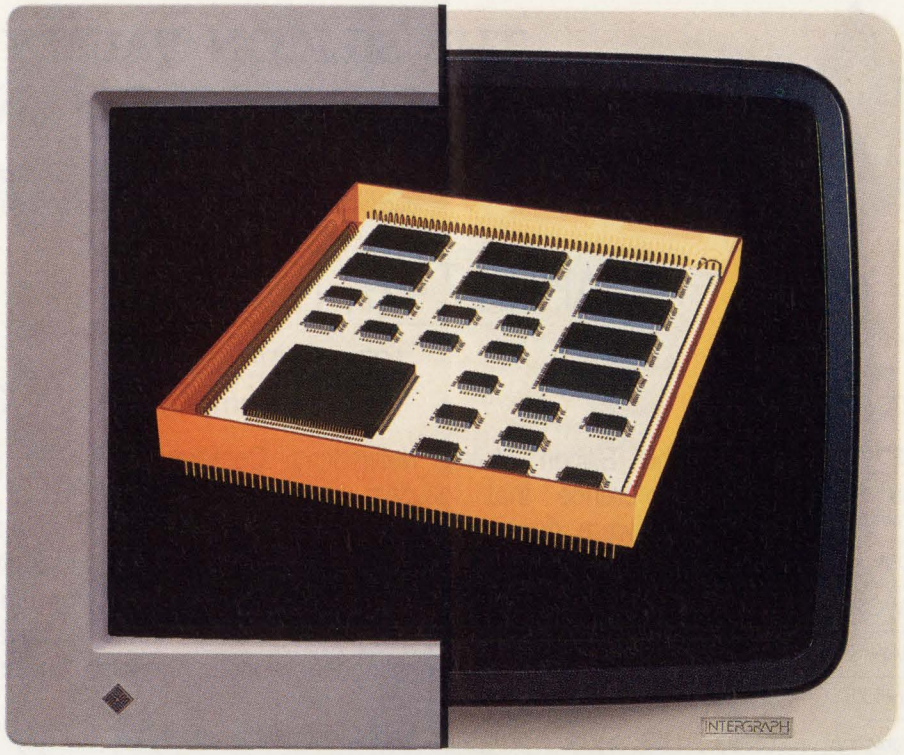
The pictures and handwritten captions are great. I have also never written a letter to a columnist, which means I'm enthused about yours.

I want more of the black magic of analog engineering. Things like why amplifiers oscillate, and why oscillators amplify. I'd also like to see more of your circuit breadboards. I teach "communications" here; we build (my students and myself) RF amps, VCOs, mixers, etc., on breadboards. I want to see how you do it.

Send a copy of this letter to your publisher and ask for a raise.

DAVID D. DRAPER
Electronic Technology Dept.,
Utah Valley Community College
Orem, Utah

I'll hire your kids a lot quicker than guys who can only drive a simulator.—RAP



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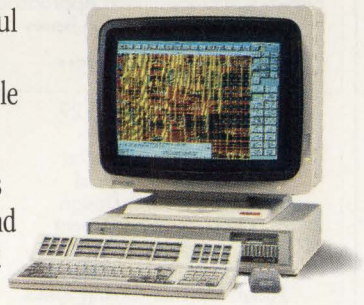

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CIRCLE 118 FOR U.S. RESPONSE **CIRCLE 119 FOR RESPONSE OUTSIDE THE U.S.**

THE SILICON VALLEY NETWORKING CONFERENCE

Location : The Santa Clara Convention Center, Santa Clara, California and the adjacent Westin Hotel

APRIL 27 - 29, 1992

KEYNOTE SPEAKER:
Eric Benhamou, C.E.O. 3Com Corp.

The Silicon Valley Networking Conference is the only networking conference that focuses on the DESIGN side of network-related hardware down to the chip level as well as the development and use of network management and testing software. In addition to technical papers that focus on design issues there will be panel sessions and papers for system planners and strategic MIS executives that focus on future technology trends and network implementation issues.

The SVNC program venue consists of three full-day tutorials on the opening day (Monday, April 27) and more than 70 technical and management-oriented paper and panel presentations arranged in three parallel sessions on the second and third days (Tuesday and Wednesday, April 28 and 29). Table-top product exhibits and demonstrations will supplement the technical paper program on Tuesday and Wednesday. Limited exhibit space is still available; contact Ken Majithia at SysTech Research - (408) 924-3930 - for exhibition details.

The Silicon Valley Networking Conference is a creation of SysTech Research. SVNC is co-sponsored by 3Com Corp., and Electronic Design and Electronics Magazines.

SVNC'92 TECHNICAL PROGRAM OVERVIEW*

Monday, April 27

Tutorial Subjects
(full day seminars)

(T1) FDDI

(T2) INTERNETWORKING

(T3) NETWORK MANAGEMENT

Tuesday, April 28

Keynote Presentation
(morning subjects)
FDDI
Distributed Systems
LAN Foundations
Future Technology Issues
Panel: Technology's Impact on Networking

PRODUCT EXHIBITS** & Lunch

(afternoon subjects)
Internetworking
ISDN and SONET Design
Distributed Systems
LAN Applications and Protocols
LAN Technology Issues
Network Implementation Approaches
Panel: Implementation Issues

PRODUCT EXHIBITS**

Wednesday, April 29

Keynote Presentation
(morning subjects)
Physical Layer Design
Network Management
Internetworking
Wide-Area Networking
Panel: Internetworking Issues

PRODUCT EXHIBITS** & Lunch

(afternoon subjects)
Physical Layer Design
New Architectures and Functions
High-Speed Networking
Network Implementation Approaches
Panel: Wrap-up of All Issues

* tentative; subject to change

*** Product exhibits are open from Noon to 2 pm and from 5:30 to 7:30 pm on Tuesday, April 28, and from Noon to 2 pm on Wednesday, April 29.*

Note: Registration fees for the conference include coffee-break refreshments, lunch, one set of tutorial notes and/or conference proceedings, and one exhibits admission. A $100 handling fee will be charged for registrations cancelled before March 6, 1992; no refunds after March 6.

Make your room reservations directly with the Westin Hotel, 5101 Great America Parkway, Santa Clara, Calif. (408) 986-0700; Ask for the special SVNC room rate.

SVNC'92 REGISTRATION FORM

Please mail in this form with your payment. Make checks payable to SysTech Research and mail to: SysTech Research, 1248 Olive Branch Lane, San Jose, CA 95120. FAX inquiries to (408) 997-8265.

	Payment postmarked by 3/6/92	Payment postmarked after 3/6/92	Payment at the door
(A) Tutorials only (one tutorial on 4/27) Select one: T1 --- T2 --- T3	$250	$295	$350
(B) Papers only (Technical paper sessions on 4/28, 29).	$350	$395	$450
(C) Full conference (includes 1 tutorial, all papers and exhibits); mark tutorial in (A). . .	$450	$495	$595
(D) Exhibits-only admission (Table top exhibits only on 4/28 or 4/29). .	$ 25	$ 25	$ 25
(E) Extra proceedings (For pick-up at the conference); If not attending, add $20/domestic, $40/intnl, for shipping. . . .	$ 85	$ 85	$100

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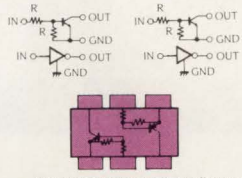
SMallTalk.

Let's talk savings.

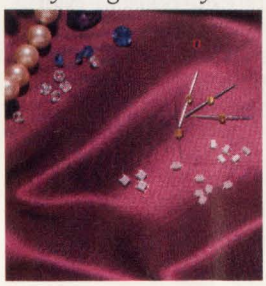
Surface mount transistors—or even T092s used with resistors in network pairing—can be replaced with a single digital transistor from ROHM. One small SOT-25 or -36 package can contain up to two transistors and four resistors. One component provides several functions, and that means lower placement cost, higher reliability, lower component count, less real estate, and reduced inventory. Standard V_{CE} ratings of 11V to 120V, and current ranges from 30mA to 100mA, are available.



Dual digital transistor circuit diagram. Dozens of layouts available.

Let's talk added value.

If you want maximum benefit from SMT, don't change to through-hole when it comes to LEDs. You can keep everything SMT by incorporating ROHM's surface mount LEDs as indicators on your board.



Our lineup includes single-chip LEDs in red, orange, yellow and green; and dual-chip types that give you combinations of colors. You can even get a three-color effect with red and green chips combined to make amber.

We offer standard brightness and high luminance, lensed LEDs packaged in SOT-23s, and lensed mini-molded styles. Brightness ranges from 555 to 660 nanometers.

They can turn product designs into gems.

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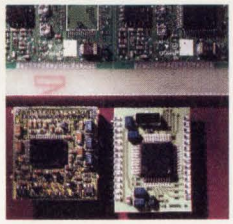

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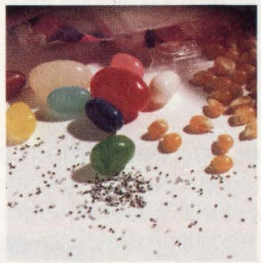

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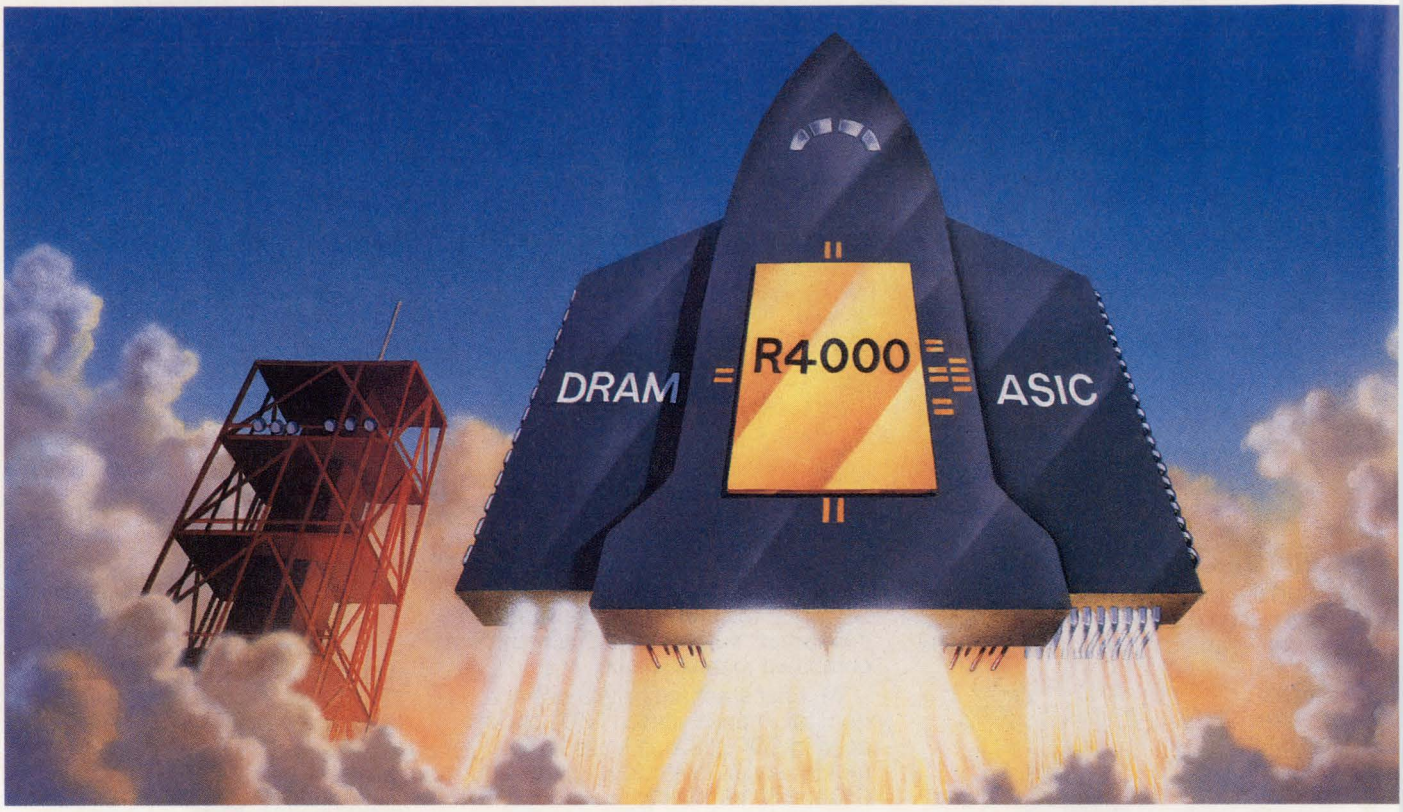

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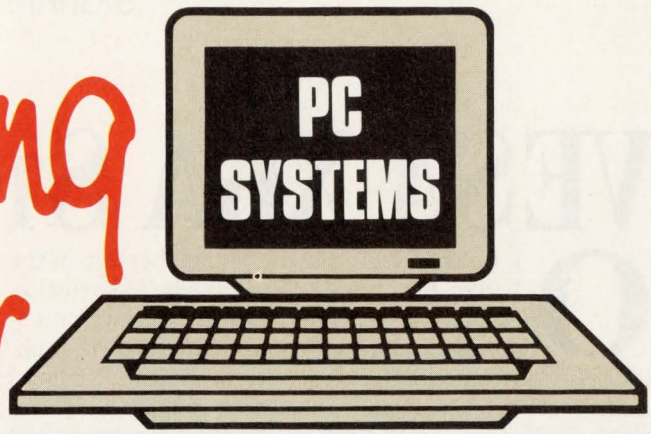
Designing For PC SYSTEMS



Chip Set For 486 Scraps Secondary Cache

A TWO-CHIP MOTHERboard chip set for 80486 systems enhances the performance of the 80486SX and DX processor's internal cache, potentially eliminating the need for a secondary cache altogether. The HTK340 chip set from Headland Technology Inc., Fremont, Calif., consists of the HT321 bus and HT342 memory controllers. The HT321 includes a four-word-deep write buffer that allows out-of-order execution of processor reads and writes, and performs byte gathering of processor byte-writes to system memory. Once data is written to the write buffer by the CPU, the CPU performs another read or write, regardless of whether the controller rewrites the data to the DRAM. That reduces the number of system wait states and eliminates the write bottleneck in most 486 DOS-based systems. The company estimates that the efficiency of DRAM write operations improves 200 to 400% by eliminating the bottleneck, increasing the system-level performance to nearly that of a system with a secondary cache. The HT321 also has extra signals (such as a Local Bus Acknowledge line) that let it offer a local bus for video or other high-speed I/O controllers. The HT342 memory controller handles all of the DRAM control. Both the bus and memory controller chips are available in 184-lead PQFPs and are priced at $45/set in quantities of 1000. For more information, contact Eric Christenson at (510) 623-7857.

CIRCLE 571

Floptical Association Adds Member

THE STANDARDS ASsociation for Floptical-drive technology has added a seventh member, Peripheral Land Inc., Fremont, Calif., a manufacturer of Apple Macintosh storage subsystems. The Floptical Technology Association, Cupertino, Calif., is attempting to standardize on a 3.5-in., 21-Mbyte (formatted) removable-media flexible disk developed by Insite Peripherals. The 1-in.-high drive used for the disks operates from a 5-V power supply and can also read and write 720-kbyte and 1.44-Mbyte 3.5-in. floppy disks, permitting system users to interchangeably employ multiple media types. Current members in the Floptical Technology Association include such companies as Adaptec Inc., Future Domain Corp., Insite Peripherals, Iomega Corp., Maxell Corp. of America, MKE, 3M Data Storage Products, Procomm Technology, and Rancho Technology Inc. For more information, contact the Floptical Technology Association at (408) 446-0470.

CIRCLE 573

Wide-Word SRAMs Ease Cache Design

A FAMILY OF WIDEword static RAMs—up to 36 bits wide—is currently being developed by newcomer Silicon Design Technology, Inc., Newark, Calif. Later this quarter, the first products in a family known as Busswide fast static RAMs are expected to be released by the company. The memories are general-purpose devices with word widths of 9, 16, 32, and 36 bits in densities up to 1 Mbit, ideal for high-performance single-chip cache applications. Other products from Silicon Design Technology on the drawing board include a family of low-voltage (3.3-V) SRAMs, also in 16- and 32-bit word widths, a series of standard 1-, 4-, and 8-bit RAMs with access times as fast as 10 ns, and some CPU-specific chips optimized for microprocessors like 80486s, 68040s, and other chips. For more information, contact John Hall at (510) 651-9343.

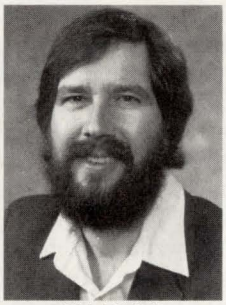
3.5-In. Minicartridges Moving To 410 Mbytes

THE POPULARITY OF 3.5-in.-format drives has led to the adoption of a higher-density minicartridge drive standard by the Quarter-Inch Cartridge (QIC) Drive Standards committee. The standard encompasses both a 385-Mbyte and a 410-Mbyte recording format as well as a new standard for magnetic heads for each product class. Smaller-format drives that use the cartridges will accommodate system makers who are already pressured to downsize their systems without giving up features. Furthermore, the new drives will allow current users of the QIC-40 and -80 products to get a major upgrade in capacity. Capacities of the minicartridge tapes are expected to increase by almost an order of magnitude over the next two years—to storage space of about 3 Gbytes (uncompressed)—thus offering a storage solution to most system implementers. For more information, contact Tony Miller for details on the QIC standards organization at (714) 497-8138.

VESA XGA STANDARD

On February 21, the voting membership of the Video Electronics Standards Association (VESA) is expected to ratify a proposal endorsing a standardized XGA (eXtended Graphics Array) interface. XGA, originally developed by IBM as a successor to VGA, includes hardware graphics acceleration and supports up to 1024-by-768-pixel resolution and 256 colors in an interlaced manner. The VESA XGA proposal standardizes the XGA interface across all standard PC buses, and supplies support for future extensions sporting higher resolutions and pixel depths.

The XGA video-standard proposal identifies a set of register extensions to IBM's original XGA standard and a set of call extensions to the Interrupt 10h BIOS video services. By following the VESA XGA standard, engineers can design XGA-compatible video subsystems with a standard system-level interface independent of the system bus.



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The proposed standard doesn't define the basic XGA product. It defines and reserves several registers in Power-on Self test (POS) and XGA register address space. The registers are:

- PCS8 - ISA instance POS enable (only defined for ISA systems)
- PCS 7 and POS 6 - 16-bit index value
- PCS 4 and POS 3 - data ports for POS 7, POS 6 indices
- POS Data 3, Index 0 - external memory enable
- POS Data 4, Index 1 - VESA-assigned manufacturer ID byte
- POS Data 4, Index 2 - optional manufacturer ID byte
- POS Data 4, Index 3 - BIOS configuration

All other indices are documented in the IBM or INMOS technical reference manuals, or are reserved for future expansion. The XGA index register extensions are:

- 21xAh, Index 4 - auto-configuration for bus type and width
- 21xAh, Index 74 - DMA channel read-back (only defined for ISA systems)
- 21xAh, Index 75 - subsystem vendor ID (chip-manufacturer assigned)
- 21xAh, Index 77 and 76 - manufacturer-specific extension
- 21xAh, Indices 70 through 73 - reserved for future expansion

There are also four 8-bit read-write registers required for VGA BIOS chaining. The addresses for these registers aren't specified and will be chip-specific.

To guarantee compatibility across multiple vendor's XGA products, some register bits must be defined as "preserved" or "reserved." Preserved bits must always be written with the value previously read from them, while reserved bits must always be written with the value documented for them in the VESA standard. Adhering to this convention will maintain compatibility with future VESA-compliant XGA products.

Seven new video service subfunctions have been defined at extended function 4Eh in the XGA BIOS:

- Function 00h - return XGA environment information
- Function 01h - return XGA adaptor information
- Function 02h - return XGA mode information
- Function 03h - set XGA video mode
- Function 04h - return current video mode
- Function 05h - set feature connector state
- Function 06h - set feature connector state

The proposed BIOS, which doesn't support any drawing-engine functions, addresses two key items. The first involves returning information about the video subsystem environment to the application. The second assists the application in initializing the hardware and setting up the video modes.

As video-mode resolutions and pixel depths increase, it's increasingly difficult to assign a standard set of mode numbers. As an alternative, the BIOS employs mode tags. To set a video mode, the BIOS is queried to determine which mode tags are defined. Then the BIOS is queried with each tag to determine the mode's characteristics. When the desired tag is identified, the set-mode function is called.

This method permits uniform handling of configuration-specific modes. High-resolution direct color modes require more video memory and displays with specific characteristics. The required information to support the mode can be supplied in utilities or configuration files supplied by the XGA controller or the display manufacturer.

The XGA proposal addresses the issue of supporting dual-VGA-display switching functions in systems whose VGA isn't identical to the XGA product's VGA function. Thus, XGA products can exist in environments where there's already an super-VGA board with drivers. The VESA-compatible XGA will contain four bytes of scratch RAM for BIOS chaining. Before hooking the interrupt in those four bytes, the XGA BIOS stores the address of the INT 10h service handler that was present. The XGA BIOS will pass any INT 10h service requests that don't apply to XGA to the routine at the stored address.

Because of the different bus types, some redundancy exists in the proposal. To maintain compliance with the XGA standard, it's only necessary to implement features required for the bus on which the product runs. For example, an ISA-based product doesn't need to decode EISA or Micro Channel slot addresses.

For information on VESA or to obtain a copy of the VESA XGA standard, call VESA at (408) 435-0333.

A VESA-related column, such as this one, will appear in each of the five coming PC Design Special Sections throughout the year.

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CIRCLE 150 FOR U.S. RESPONSE

CIRCLE 151 FOR RESPONSE OUTSIDE THE U.S.

Designing For PC SYSTEMS

Dual Processors Boost Computer Power

Combining an i860 RISC processor with an i486 can boost the latter's throughput tremendously at little extra cost.

BY MARK ATKINS

Intel Corp., MS SC4-62, 2625 Walsh Ave., Santa Clara, CA 95052; (408) 765-5237.

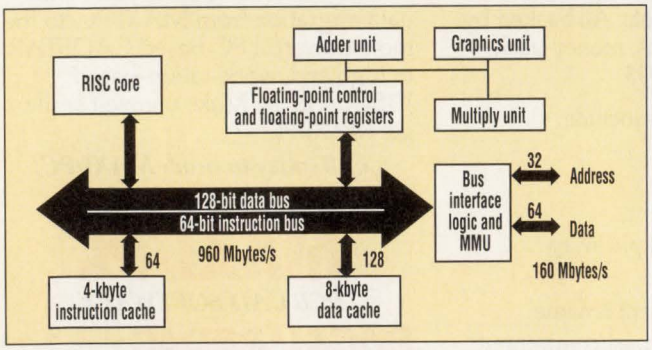
Building microprocessor-based systems is a thankless task. Every increase in performance opens up new application areas, which require yet higher performance. As a result, even though personal computers based on the latest microprocessors run significantly faster than their predecessors, users still demand more speed for their graphics and other computationally intensive applications programs. Needless to say, those same users would like that speed to cost as little as possible.

Fortunately, there's a way to boost microprocessor power at moderate cost: combine a floating-point coprocessor (FPC) with the CPU in an arrangement known as a dual-processor architecture. That approach differs from conventional coprocessor arrangements because the FPC in a dual-processor system operates independently of the CPU.

The first coprocessor, the 8087, which complemented the 8088 CPU in the original IBM PC, had to rely on the CPU to fetch its data and instructions from memory. The CPU had to do at least two writes (one instruction, one or two data) and a read (result) each time it wanted coprocessor help. More recent generations of PC (80286, 80386) and Macintosh (68020, 68030) CPUs also have corresponding FPCs, and suffer from the same type of speed limitation.

A major step forward occurred with the latest CPU generation—exemplified by the i486 DX and the 68040—which brought the FPC on-chip. Placing the FPC there improves overall performance significantly by eliminating the delays associated with external bus transfers. It's only a partial solution, though, because the FPC still depends upon the CPU for its data and instructions. Moreover, the on-board FPC shares the CPU's bus and on-chip cache, and hence suffers from bandwidth bottlenecks.

A better solution would be an intelligent dedicated floating-point processor with its own instruction stream, external bus, and dedicated cache working in concert with a high-end CPU, such as the i486. This combination constitutes a dual-processor system.



1. The i860 RISC coprocessor has its own dedicated data and instruction buses, as well as data and instruction caches.

An appropriate coprocessor to work with the i486 is the i860 XR RISC processor, which combines the functions of a graphics processor, digital signal processor (DSP), and FPC *(Fig. 1)*. It can deliver 80 MFLOPS peak at 40 MHz, and can sustain over 10 MFLOPS on double-precision Linpak benchmarks thanks to its high bus bandwidth, extensive on-chip cache, and high-speed registers.

The i860 isn't new. It's well established in many workstations, including models made by Hewlett-Packard, DEC, Next, and Sun. Those workstations exploit its ability to perform extremely fast floating-point matrix multiplications to execute fast 3D transforms.

What is new is the idea of incorporating the i860's power into a PC. Makers of boards for PCs, such as Hauppauge, Hercules, IBM, Spea, Myriad, Truevision, and Microway, are building i860s into their products to give them workstation-quality graphics. At the same time, some Unix-based workstation manufacturers are offering add-in cards to run DOS and other PC applications. The Mars Mariner 4i, for example, contains both a Sparc and an 80386. Puzzle Systems plugs an i386 card into the Sbus in Sparcstations. And VME and Multibus industrial computers have "PC-on-a-card" boards that allow DOS to run beside RISCs, 68Ks, and real-time software. Clearly the trend is toward dual-capability systems, which on the one hand have sophisticated graphics and floating-point computational power, and on the other hand can run DOS and Windows programs.

But designing a dual-processing system is no small chore. If it's not done right—for example, if the two processors continually have conflicts over access to system memory and I/O—the two processors together may wind up being less powerful than either one by itself. Done properly, however, the results can be spectacular. Although an i860 processor can be used to advantage with any member of the 80X86 family, it works particularly well with the 486 because of the latter's on-chip cache, burst external bus, and high clock rate capability.

The i486 and i860 microprocessors also have similar hardware and data types, so they fit tightly together in a system without overhead. Both use a 168-pin pin grid array (PGA) package, with similar bus protocols and signals *(Fig. 2)*. Most of the signals connect directly, with the same wire feeding both processors on a dual-processor motherboard.

The locked access indicator output ($\overline{\text{LOCK}}$) provided by each processor helps control multiprocessor data sharing.

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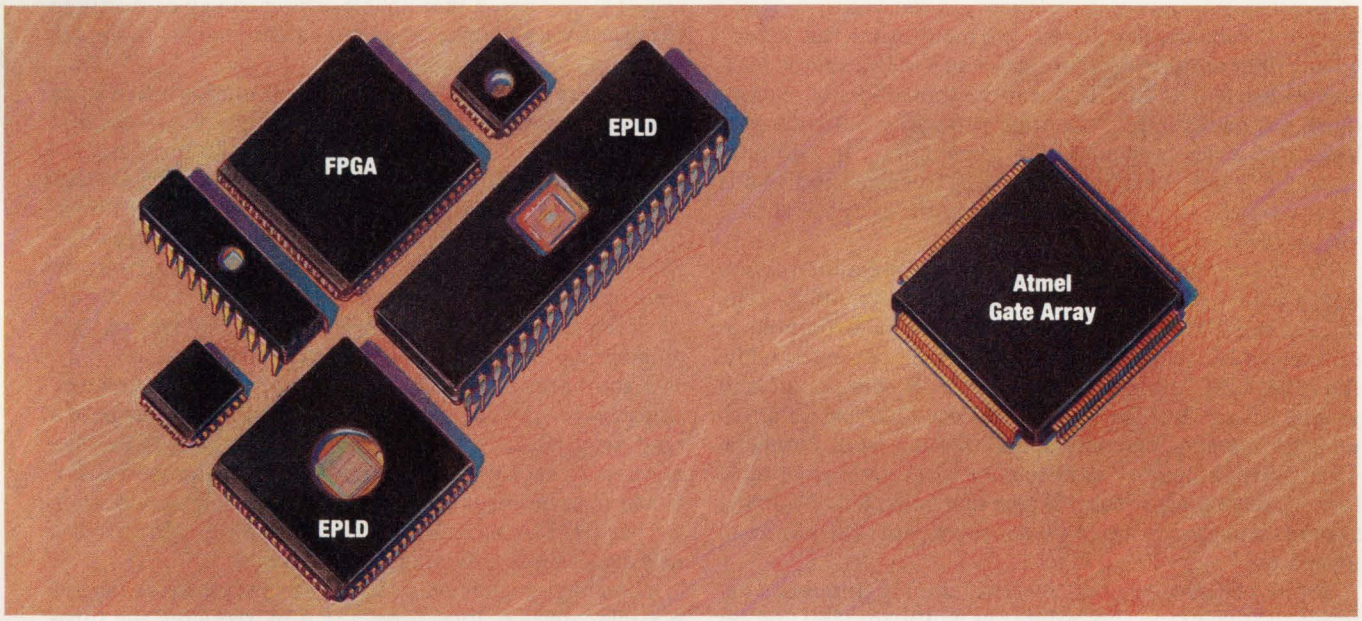

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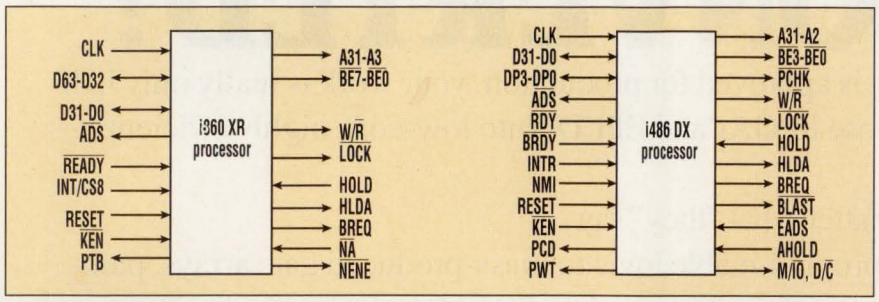

2. Combining an i486 with an i860 is simplified by the many functions and control lines they have in common. Most of them can be connected directly with the same wire feeding both processors.

A memory controller knows, by monitoring this signal, when either chip requires exclusive access to a shared variable. When active, LOCK warns the controller not to relinquish bus ownership to the other processor. Software uses locked accesses to manipulate semaphores. In addition, each chip's hardware asserts LOCK to ensure indivisible access to page tables when modifying the status of shared virtual memory.

Of course, the two processors have different instruction sets. The i486 maintains compatibility with the 8088, 8086, 80286, and 80386 processors, which are incorporated in millions of PCs and thousands of software packages, while the i860 RISC architecture runs new floating-point and graphics code. But the two devices use identical data formats for integers, characters, and floating-point numbers. Their virtual-memory architecture (page size, page table format, paging algorithm) is also identical. Therefore, the system software can maintain one set of page tables for both processors.

From a hardware point of view, the big difference between the two processors is data bus width: the i860's 64-bit bus doubles the i486 CPU's 32 bits. Consequently, any board containing both must use transceivers to convert widths whenever the processors exchange data. Fortunately, many i486 machines already use a 64-bit memory width to squeeze better performance out of relatively slow DRAMs. Typical DRAM chips have a cycle time of approximately 80 ns compared to 30 to 40 ns for the 486.

With a 64-bit memory accessed every two clock ticks, the i486 CPU bus can get 32 bits on every tick by alternating between two interleaved banks of DRAM. The i860 XR sits conveniently on that 64-bit path to absorb data every two clocks. In fact, it requires two ticks per data transfer, whereas the i486 transfers data with every tick in its burst mode. Thus, if they're driven by the same clock, their peak bus bandwidths will be identical.

The bus of the i860 XP processor, the successor to the i860 XR, combines i486 bursts with i860 XR pipelining capability. It also contains parity, M/IO, BOFF (Backoff), EADS (External Address Status), D/C (Data/Code), non-maskable interrupts, and other i486-like pins. With full MESI (Modified, Exclusive, Shared, Invalid protocol) cache consistency implemented on-chip, it allows either software or external hardware to select write-back or write-through caching. Its large on-chip caches (16 kbytes for data and 16 kbytes for instructions) reduce bus usage over the i860 XR and i486 DX.

Bus arbitration is a key issue in multiprocessor systems. In the case of the 486 and the 860, it's simplified by the fact that both chips have HOLD and HLDA (hold acknowledge) pins, These pins can be used to give either chip uncontested ownership of the bus when it's deemed desirable. Consequently, a software-programmable arbiter can give priority to the processor whose response-time matters most in a given situation.

For example, the aptly named 4860 motherboard from Hauppauge Computer Works, Hauppauge, N.Y.—the first PC motherboard to combine i860 and i486 processors—includes an arbiter programmable logic device (PLD) that implements several bus priority modes *(Fig. 3)*. Its "Priority i486" mode keeps Wordperfect or Lotus 1-2-3 response time fast by giving the i486 ownership whenever it asks, in spite of simultaneous requests from the i860. Similarly, its "Priority i860" mode would benefit an interactive graphics animation program by allowing faster image updates.

A third priority mode, named "Fair," alternates ownership between the two processors. Fairness could result in a ping-pong effect, where bus ownership changes too frequently. At each ownership change, the arbiter wastes two clocks to ensure that the former owner is no longer driving the bus (HLDA active), and then gives the go ahead to the new owner by deactivating its Hold input.

Therefore, giving ownership to one processor as long as possible improves total throughput by reducing the turnaround frequency. The Fair protocol of the 4860 tries to let the current owner complete a cache line-fill (four transfers) before yielding to the other processor's bus request (BREQ). With a completed line-fill, the processor can commence processing internally.

The flexible programmable arbiter allows the 4860 to function with either the i860 alone or i486 alone, as well as with both chips in their sockets.

Cacheability of memory blocks is controlled at 32-kbyte resolution by a software-writable mapping-RAM (MRAM), with an output feeding the KEN (Cache Enable) pin of the i486 and another feeding the i860 KEN. With those programmable cacheability controls, software can determine how to handle the consistency of shared data. The i486 CPU snoops (monitors) accesses by the i860 on the shared external bus, and invalidates any on-chip cache entries written by the i860. Furthermore, the i486 uses write-through caching, making all writes update memory when updating the internal cache. However, the i860 XR doesn't monitor the i486 accesses and employs write-back caching, meaning i860 XR writes can update the internal cache without informing the i486 and memory. To

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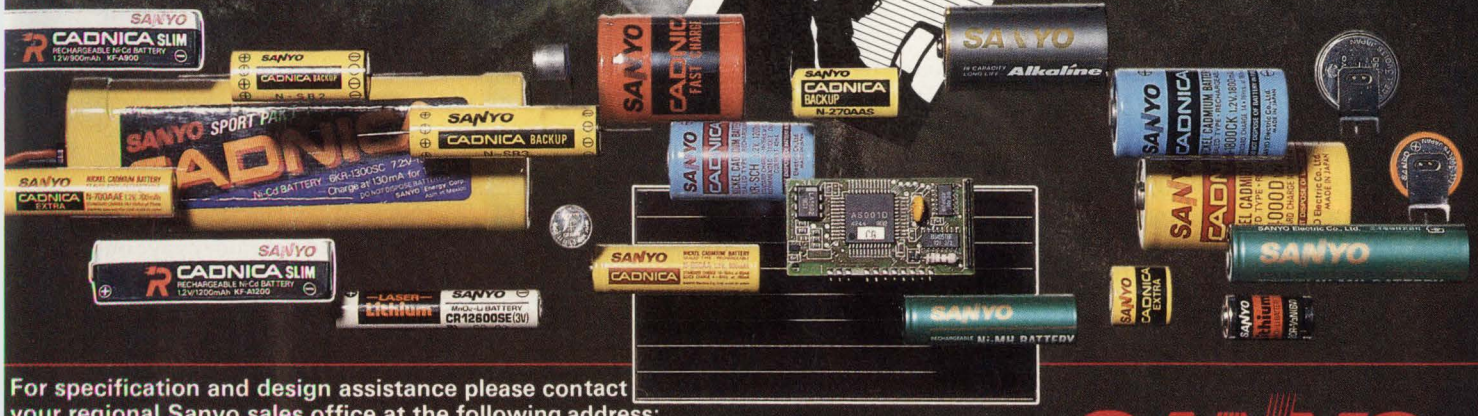

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assure consistency, software can configure the MRAM to prevent caching data readable by one CPU but writable by the other.

For higher performance, software can make shared locations cacheable. It can also explicitly flush from the i860 XR cache any data it writes for the other processor's viewing. Of course, the MRAM marks all memory-mapped I/O locations as uncacheable. Software initializes MRAM contents by setting the "MRAM-Write" bit in a motherboard configuration register, then writing a byte to each 32-kbyte block—each write controls parameters for that block. Thus, MRAM doesn't consume any address space in the normal mode of operations.

Because the i860 XR CPU contains 12 kbytes of on-chip cache, and the i486 has 8 kbytes, traffic on the shared bus remains far below that of an i386 with a 387 or Weitek 3167 coprocessor, neither of which has an on-chip cache. Keeping bus traffic low ensures that neither processor has to wait long for external accesses.

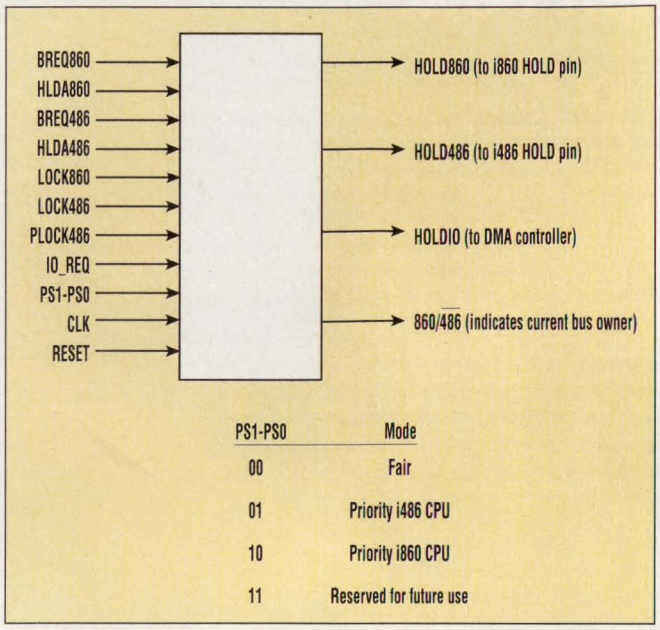
Conversely, a "saturated" (overutilized) bus makes one of them stall during the wait for instruction fetches until the other processor is forced off the bus.

The second-generation i860 XP processor, with 32 kbytes of on-chip cache, uses the shared bus even less. Furthermore, it snoops on i486 accesses, enabling software to cache shared data in both chips. The second-generation i860 also allows software and external address-decode hardware to determine whether cached data is write-through or write-back.

Most PC I/O chip sets (including the 82350 EISA chips in the 4860) can't tolerate the "back off" intervention that occurs when I/O tries to access a modified line in the CPU cache. When I/O reads or writes a location already in the CPU cache, the I/O access must be postponed (backed off) until the CPU dumps the modified line to memory. Then the I/O controller can retry the access and receive correct data. Without backing off, it would receive obsolete data from memory, rather than the CPU's modified copy.

Thus, memory blocks obtained by direct memory access or I/O must be write-through or non-cacheable for the CPU. Alternatively, software can allow the CPU to cache such blocks by making sure they're always flushed from the CPU before dispatching the DMA controller.

While the dual processors in the moderately priced 4860 share all memory, a high-cost motherboard might include dedicated private buses and DRAM for each CPU in addition to the shared memory. That would reduce contention for the shared bus, because most accesses hit the local area. An external cache for the i486 processor can serve as a private memory to improve performance. Not only would such a cache reduce the i486's usage of the bus, it would reduce the wait states for external accesses as well. The cache architecture can also provide the 32-to-64-bit conversion logic, as some cache RAMs have 32 bits on the CPU side and 64 bits on the memory side. Benchmark tests yield i486 DX performance improvements in the range of 5 to 60% with external caches, depending on the software, memory bus speed, cache protocol, and cache size.



PS1-PS0	Mode
00	Fair
01	Priority i486 CPU
10	Priority i860 CPU
11	Reserved for future use

3. The bus arbiter PLD on the 4860 board from Hauppauge Computer Works uses the HOLD and HLDA pins to implement three bus access modes: Priority i486, Priority i860, and Fair.

While a system could also include a cache for the i860 processor, it would benefit less. The large amount of data typical in i860 graphics and vector floating-point algorithms could not fit in an external cache, so it would get a high miss rate. The i860 memory interface, being optimized to work with DRAMs, tolerates their relatively low speed without a significant throughput penalty compared with external cache.

In a dual-processor system, each CPU must be able to interrupt the other to allow synchronization and cooperation. For example, the i486 CPU may do all of the disk control, requiring the i860 to interrupt the i486 to request file transfers. While the i860 program could simply wait for the transfer to finish, more efficient code would dispatch another i860 task and depend on an interrupt from the i486 to signal that a disk read is completed. Then, the task waiting for the disk could continue.

Other reasons for cross-processor interrupts include: the need to handle various types of errors; status inquiries, in which either processor checks on whether the other is functional and/or busy; performing diagnostic tests; and flushing the translation lookaside buffer (TLB), which may happen when both processors need to invalidate their address translation caches because one swapped a memory page out to disk.

In the Hauppauge 4860, a PLD implements interrupt control. Either CPU can write to I/O port 0xFC to interrupt the i860, and to port 0xFB to interrupt the i486. I/O addresses in the range 0xF0:0xFF serve as interrupts and configuration registers, as the original PC/AT designers reserved those addresses for the 80287 numerics coprocessor. Neither the i486 nor i386 system would use an 80287,

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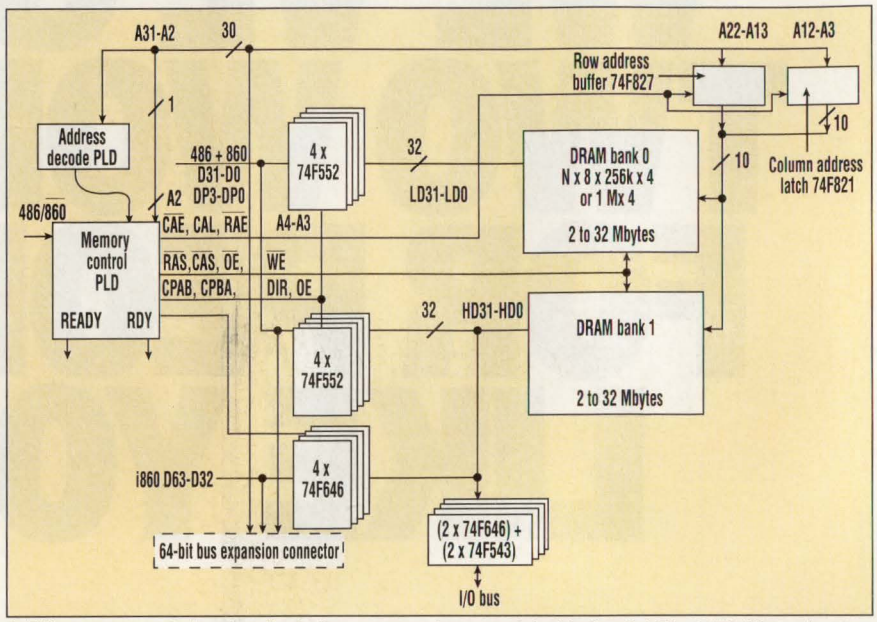
so the 0xF0:0xFF locations remain safe for usage as i860 controls. The 4860 address map remains PC/AT compatible.

The system allows software to determine, via a "motherboard configuration register," whether the i486 sees a nonmaskable interrupt (NMI) or a maskable interrupt of lower priority (INTR) when the i860 interrupts it. This same configuration register also contains the arbiter priority select bits PS1:0, along with the I/O command delay insertion (2 bits), and the i860 reset line (1 bit).



4. This memory control system for both processors has a sustainable bandwidth of 133 Mbytes/s at 33 MHz. It pipelines i860 XR accesses by activating NA when it latches address and control lines.

To help keep costs down, both the i486 and i860 microprocessors were designed to deliver top performance with ordinary DRAMs. The i860 CPU provides two pins to speed up DRAM accesses: NA (next address) and NENE (next near). NA indicates willingness by memory to accept another request even though the previous cycle hasn't yet completed. With it, the processor can issue up to three requests for reads and writes before the first READY signal indicates valid data on the data pins.

By latching an address in external buffers and/or inside the DRAMs, using the RAS (row address strobe) and CAS (column address strobe) signals, DRAM controllers can pipeline more requests onto the external bus. That allows the long DRAM row access and precharge time to be overlapped with the CPU's next request on the address pins. With NA and pipelining, the average number of clocks per access drops from five to two. Benchmarks on the i860 XR show pipelined systems to be twice as fast as non-pipelined memories using the same 80-ns DRAMs.

NENE, which comes from an internal comparator, provides support for fast page mode and static column DRAMs. Such DRAMs can access data on the same page (1 kbit in a 1-Mbit chip) in half the time required to access data on a different page. For example, an 80-ns static column DRAM requires only 40 ns for a "near" read. The NENE pin indicates that the current memory access falls on the same DRAM page as the previous. Consecutive accesses to the same page occur frequently. For example, i486 cache line-fills fetch 16 consecutive bytes; on the i860 CPU they fetch 32 bytes. These transfers consist of three near accesses after the first access of the line.

The i486 CPU usually accesses memory in bursts, in which each CPU request retrieves 16 bytes to fill an internal cache line. Four 32-bit transfers and BRDYs (Burst Readys) occur for each ADS (Address Status). Memories optimized for bursts exploit the "nearness" of the three most recent accesses, with fast page-hit transfers requiring no RAS. However, the CPU has neither a NENE output pin nor a NA for pipelining.

As explained earlier, fast systems interleave banks of relatively slow DRAM chips to increase data-transfer rates in order to better match CPU bus bandwidths. If a 40-MHz CPU can transfer 32 bits every 25 ns, 40-ns DRAMs will be a major drag on the system. However, if two banks of DRAM are interleaved, the effective cycle time becomes about 20 ns, because access to the next word in bank 1 has already begun while bank 0 transfers data to the CPU. The DRAM system is actually 64 bits wide, and multiplexers compress that to 32 bits, doubling the transfer rate. To provide two-way interleaving for the 64-bit i860 processor, a DRAM system 128 bits wide could be treated as four-way interleaved for the i486.

By implementing these ideas in hardware, one can build a memory system for both processors that's either 64 or 128 bits wide, uses either two-way or four-way interleaving, and has a sustainable bandwidth of 133 Mbytes/s at 33 MHz *(Fig. 4)*. The system pipelines i860 XR accesses by activating NA when it latches address and control lines. It contains static-column-mode or fast-page-mode DRAMs for faster accesses on successive page hits, including bursts. It intelligently accesses DRAM banks in bursts of four 32-bit transfers for i486 cache line-fills.

Several software architectures exist for 4860 systems, each suited for certain uses. Many 4860 users have Unix for the i486 and a separate Unix V/4.0 kernel for the i860. When they turn on the power, they can choose to boot i486 Unix or i860 Unix. Each can access both file systems on disk, but they don't share a single file system because of object-code differences: the "vi" editor compiled for the i860 won't run on the i486. All data and shell scripts, however, can be transparently shared.

In another alternative, the i486 runs Unix, but the i860 does not. However, the i486 can dispatch jobs to the i860

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processor. A utility called APX (attached processor executive) allows the user to split jobs between the two processors. In the APX scheme *(Fig. 5)*, the i486 controls the Unix file system, while the i860 directly manipulates the 64-bit frame buffer for 3D graphics work.

The i860 runs a small (170 kbyte) APX kernel with multitasking and paged virtual memory, supporting most Unix system calls. It requests services of the i486 processor, such as keyboard input and disk I/O. Under the APX kernel, programs written in C, Fortran, assembly language, or combinations thereof run on the i860 processor. In such a case, the i860 itself doesn't run Unix, but benefits from the i486 processor's handling of the file system under Unix and X-Windows.

Versions of APX exist for Unix, OS/2, and DOS. With X-Windows or OS/2 Presentation Manager executing an i486 CPU, i860 APX can occupy one or more windows. Because APX multitasks, several users and several jobs can use the i860 simultaneously.

One user might compile Fortran or C programs on the i860 processor while another runs an image-enhancement routine. On a 4860 or the "Fire" card from Spea (located in Starnberg, Germany) with a high-resolution monitor and frame buffer, the i860 processor running APX can interactively render realistic color 3D images. The i486 concurrently maintains menus, text, mouse, and keyboard for multimedia creations.

Application binaries targeted for the i860 alone also under APX run unmodified under Unix/i860, because the OS interface contains the same functions. However, applications can be partitioned between the two processors with a remote procedure call (RPC) paradigm. Intel is researching the possibility of automatically generating the RPCs, using the DOS-Windows and OS/2 dynamic-link-library (DLL) facilities. The compiler and operating system then will automatically partition the application between processors, passing to the i860 tasks befitting it.

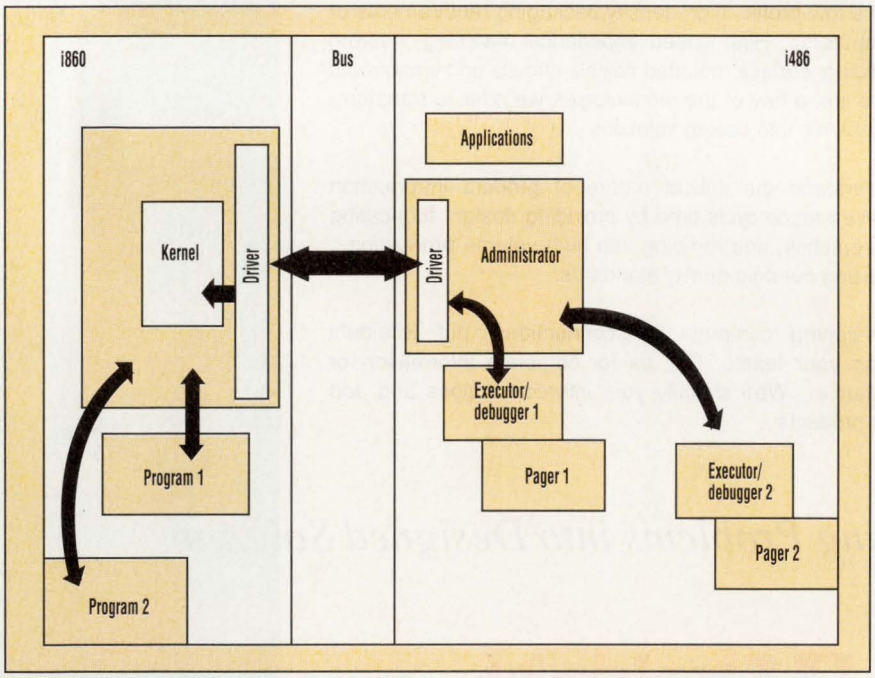
To benefit from the i860, the system must pass through large enough tasks to mitigate the communication overhead of task dispatching. This overhead can range from a hundred to a few thousand clocks.

Whereas a fast Fourier transform (FFT), which takes about a millisecond, is appropriate, a floating-point division of a single pair of numbers, which takes about a microsecond, is unacceptable. Such tasks as vector math, megabytes of data movement, and rendering 3D images have about the right degree of granularity.

Of course, the i860 CPU could emulate a Weitek x167 interface by polling the memory-mapped locations used by Weitek software, and doing a single divide (or sine, square root, etc.) when the i486 writes the divide op code and data to those memory locations.

However, the i860 would perform no faster than the x167 because both do scalar floating-point operations in a few clocks. Bus contention due to the continuous polling would slow performance even further.

To summarize these ideas, the autonomy and bandwidth of the i860 fit full algorithms and mass data movements rather than single instructions. The processor is best utilized when it operates simultaneously with the i486, rather than requiring constant i486 processor attention and serializing execution (the i486 usually waits while the Weitek coprocessor executes its code). The i860 processor is not an instruction-level accelerator.



5. With the APX operating environment, the i486 runs its conventional operating system while the i860 operates under the APX kernel. The host executive communicates with the APX kernel to create new processes for the i860 when needed.

Besides separate Unix systems and APX, multiprocessing Unix offers a third system alternative. this alternative allows both processors to run Unix kernels simultaneously, sharing I/O, semaphores, signals, and memory. A homogeneous MP Unix for multiple i486 processors could be ported to the 4860 combination. So far, this possibility remains speculative because of the complex implementation of heterogeneous MP Unix with two different kernel images.

For users who already own a PC, PS/2, Mac-II, or workstation, over a dozen vendors have developed i860-based add-in accelerator cards. Such cards generally attach to an I/O bus, such as VME, EISA, ISA, MCA, or Multibus-II, for communication with the host CPU and I/O devices. Because the I/O bus at 2 to 30 Mbytes/s has fairly low bandwidth, these accelerator cards contain dedi-

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cated DRAM for the i860 processor. They therefore provide looser coupling between the host CPU and the i860, which allows the processors to operate at their own clock rates and without contention for memory.

The cards typically contain an entire computer with interrupt controllers, timers, DRAM controller, DRAM, I/O interface, and sometimes video RAM and video controllers. A user purchases the card bundled with software, including libraries and an executive or operating system to link to the host OS (DOS, Unix, or OS/2). To coexist with the existing disk file system and OS protocols, the i860 software typically requests the host CPU to carry out any file reads, updates, keyboard input, and screen output.

The higher the I/O bus bandwidth, the better the add-in card performance as it accesses remote disk, network, or video displays. The card should be a bus master, preferably for the EISA, MCA, MB-II, or VME buses. Video bandwidth problems can be solved by placing a frame buffer directly on the i860 card or on a 64-bit-data expansion connector, isolated from the I/O bus.

With accelerator cards, interprocessor communication occurs only through the I/O bus. Cache consistency therefore can't be handled by hardware. Moreover, the card will probably not benefit from an external cache beyond the i860 CPU's internal cache because the i860 bus tolerates slow DRAM interfacing exceptionally well. Nonetheless, to manage the on-chip cache, software for add-in cards must explicitly flush any shared data from on-chip caches, and must pass messages to the other processor explicitly by interrupts and/or memory-mailbox locations. For example, to request that a memory page be swapped out to hard disk, the i860 software flushes all modified data from its cache. Then it puts a message requesting the disk write and a pointer to the memory block into shared memory. Finally, the i860 software interrupts the i486 processor, which reads the message and executes the transfer. After completion, the i486 interrupts the i860 to signal completion.

Compared with graphics coprocessors (34010, 34020, XGA), floating-point coprocessors (80387, 3167, 4167), and digital-signal processors (320C30, 96002, 56001), the superiority of the i860 processor lies in its versatility. One i860 can replace all of those chips, and with similar or better performance. An i860 card or motherboard socket can perform 2D graphics, 3D graphics, floating-point acceleration, image compression, digital-signal processing such as speech recognition, and even DMA data movements. Software for each function can be loaded from disk as the function is needed.

Mark Atkins, an applications engineer at Intel Corp., received BSEE and MSEE degrees from Purdue University, West Lafayette, Ind.

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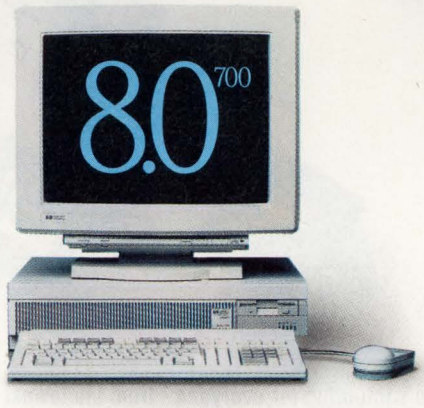

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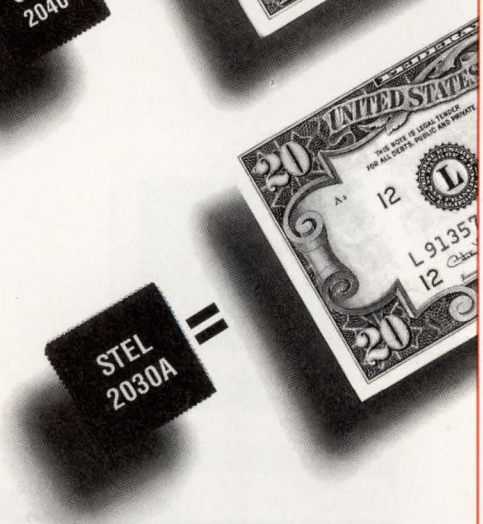

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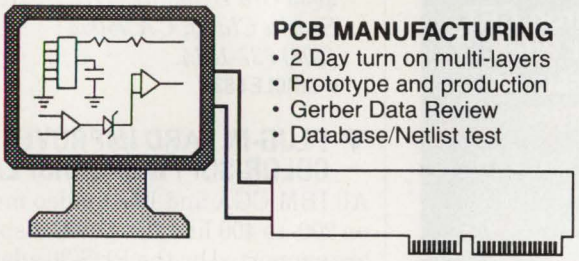

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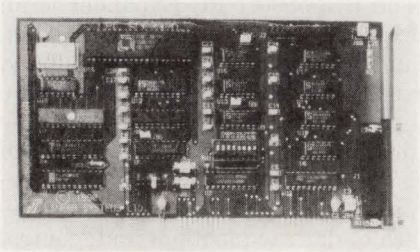

Presently, most PC/AT computers can't operate with modems whose baud rates exceed 9600. Using the Modem Pump as a serial port, baud rates up to 96,000 can be accommodated. The board supplies two high-speed synchronous multiprotocol serial I/O channels with full modem support for applications such as X.25 and fractional T1 gateways. The board features DMA support, extensiveinterrupt channel-selection options, and support for local, remote, and test-mode interchange circuits. Both external receive and transmit clock inputs can be accepted. In single quantities, the Modem Pump sells for $325. Large-volume discounts are available.

Computer Modules Inc.
2350A Walsh Ave.
Santa Clara, CA 95051
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▼ LOCAL BUS ACCELERATES GRAPHICS UP TO 20 TIMES

Opening, scrolling, and pulling down Microsoft Windows 3.0 files can be done virtually instantaneously using a high-speed video-graphics local bus module from Synergistic Computers Inc. The VGA module can accelerate graphics performance up to 20 times because the local bus runs at a clock speed equal to the processor's speed instead of the standard AT bus speed. The adapter also contains a Window's engine to supply high-speed-image and bit-block transfer.

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551 Lundy Pl.
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(408) 946-0500.
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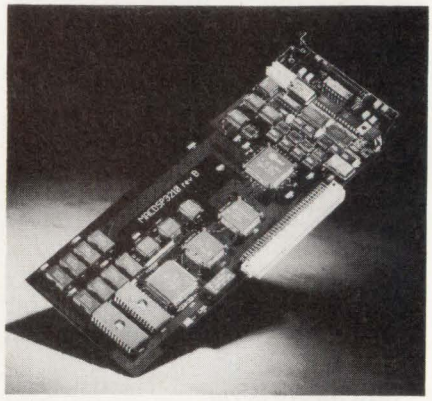
▼ DSP BOARD AIDS SOFTWARE DEVELOPMENT ON A MAC

Aimed at multimedia and engineering software development, the MacDSP3210 DSP card is designed to work with an Apple Macintosh. The 25-MFLOPS card is built with AT&T's DSP3210 32-bit floating-point digital-signal processor and VCOS real-time multimedia operating system for complex imaging and signal processing algorithms.



The board features two-channel analog-to-digital and digital-to-analog converters that directly interface the DSP chip and 4 Mbytes of DRAM. This configuration avoids unnecessary Nubus data transfers. Available immediately, the MacDSP3210 development board is priced at $3995.

Spectral Innovations Inc.
4633 Old Ironsides Dr., Suite 401
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▼ PLUG-IN CARD IMPROVES COLOR-SOFTWARE DISPLAY

All IBM CGA and EGA video modes on 200- to 400-line flat-panel displays are supported by the PDS-30 adapter card. The card improves the display quality of existing software. The compact PC XT/AT-compatible half-size card converts RGB color information to gray-scale and hatching patterns, including normal and bold fonts that are active in either 40- or 80-column text modes. In quantities of 100, the PDS-30 sells for $360 and is available now.

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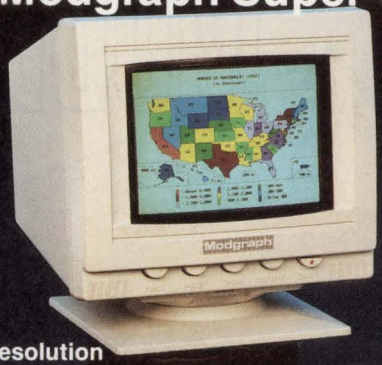

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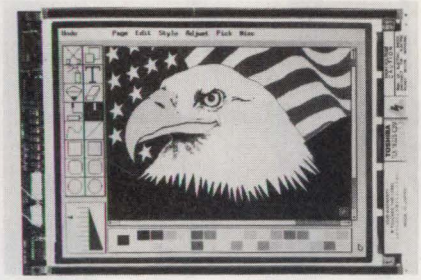
▼ HIGH-PERFORMANCE LCDS GET THINNER, LIGHTER

Suited for laptop and notebook computers, the TLX-1832S-C3M liquid-crystal display boasts a depth of 6.5 mm, a weight of 320 g, and a twelve-to-one contrast ratio. The improved depth and weight specs come from using thin stainless-steel crimps at



the top and bottom of the display instead of the large metal bezel used in competitive displays. In addition, the tape-automated-bonded (TAB) chips used to drive the columns and rows can be folded behind the thin cold-cathode fluorescent side lighting (CCFL) system to reduce thickness. Samples of the LCD cost $425.

Toshiba America Inc.
9775 Toledo Way
Irvine, CA 92718
(714) 455-2000.
▶ CIRCLE 585

▼ VGA CONTROLLER DIRECTS FLAT-PANEL DISPLAYS

By operating at 3.3 and 5 V, the 65520 VGA controller meets the low-voltage requirements of the growing portable-computer market. The chip, aimed at flat-panel displays, offers high speed, high resolution, and a low power consumption. With its companion chip, the 82C404 clock synthesizer, the 65520 lets designers build small, low-cost, high-quality displays. For example, a complete VGA controller can be built in less than 4 in. of board space. The chip can be interfaced through an ISA bus, a Micro Channel bus, or the Peripheral Interface bus of the 386SL microprocessor. The controller and clock synthesizer are both sampling now. Production will start in April. Both in quantities of 1000, the 65520 costs $40 and the 82C404 costs $5.

Chips and Technologies Inc.
3050 Zanker Rd.
San Jose, CA 95134
(408) 434-0600.
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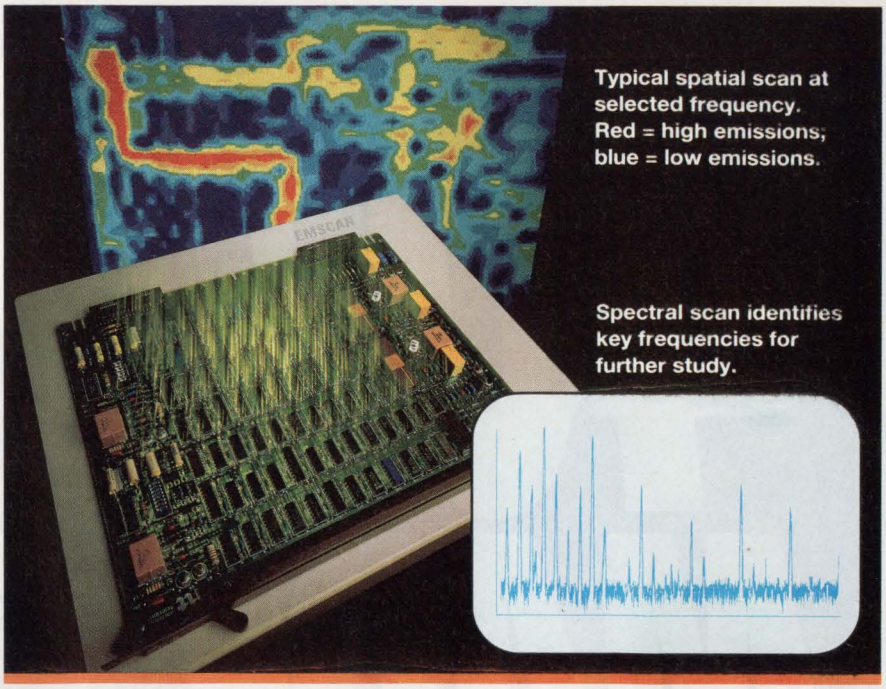

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The software operates under "Windows" to make early diagnosis easy, even for those who are new to compliance testing. It can run on several PCs and workstations, and is readily ported to other environments for analysis.

You should learn all about this qualitative and quantitative measure of emissions for use during product development—where design corrections are least costly. To start, call toll-free (1-800-933-8181) to speak with an applications engineer and arrange to see a demonstration in your office or plant.

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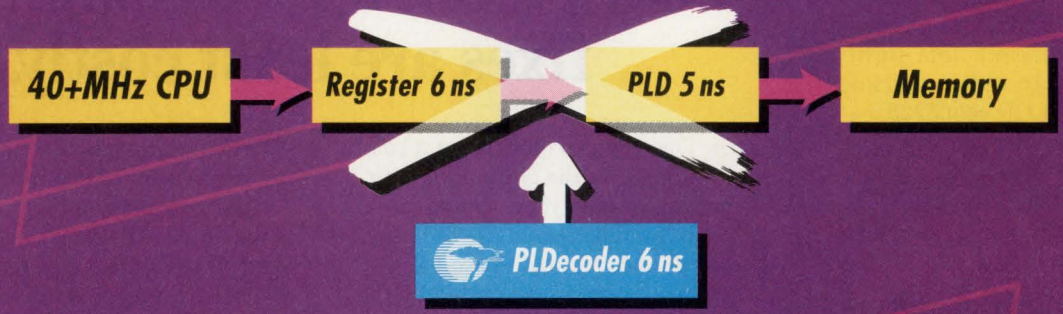

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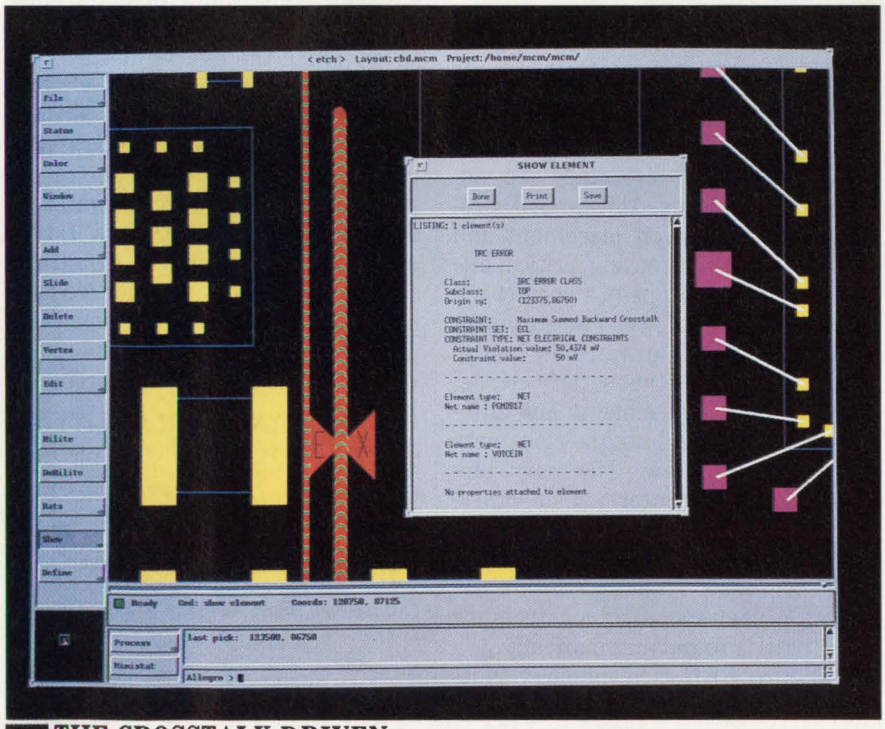
A CORRECT-BY-DESIGN EDA SYSTEM HELPS ENGINEERS BUILD HIGH-SPEED BOARDS, MCMS, AND HYBRIDS, WITHOUT ERRORS.

CONSTRAINT-DRIVEN TOOLS LAY OUT HIGH-END DESIGNS

LISA MALINIAK

Design tools must constantly undergo change to meet the demands of the burgeoning electronics field. Shrinking product-development cycles and the complexity of high-end systems like multichip modules (MCMs) mean that the correct-by-verification methodologies used by today's engineers won't meet the needs of future engineers. The engineers of tomorrow will require design tools that not only find errors, but also prevent them from happening in the first place.

Cadence Design Systems Inc. is homing in on that approach with a new system-level design tool called Allegro CBD (correct-by-design). Allegro CBD, the newest version of the Allegro product first introduced by Cadence (formerly Valid) in 1987, is a constraint-driven design-layout system for high-speed pc boards, MCMs, hybrids, and multiwire boards. The CBD product incorporates more than 60 new features, all of which contribute to its correct-by-design methodology. Many of the new features came about from the MCM contract work with Microelectronics and Computer Technology Center Corp. (MCC), Austin, Texas.



THE CROSSTALK-DRIVEN router in Allegro CBD addresses signal-integrity concerns imposed by performance and quality constraints. While routing, the tool computes the forward and backward crosstalk generated by the addition of a new line segment, and indicates with a red marker that a user-specified electrical constraint has been violated.

Allegro CBD is built on three critical components of the correct-by-design methodology: constraint definition, constraint adherence, and technology independence. With its Constraints Editor, users can assign constraints up front in the design cycle, so that all of the Allegro automatic and interactive tools can adhere to them throughout the entire design cycle, and can evaluate tradeoffs at various design phases. In addition, each Allegro CBD tool can be

applied across multiple packaging technologies.

Users employ the Constraints Editor, the central command center, to define constraints (data used to limit or check a particular design specification or implementation). Electrical, physical, and thermal constraints ensure signal integrity, reliability, testability, and manufacturability. The constraints are observed by design-rule checks (DRCs) within Allegro's tools.

Constraints are grouped into sets according to their behavior and the types of elements to which they're applied. Specific constraint sets could include: component spacing (restrictions for pairs of components, orientation); net data or layer (restrictions for individual nets, via types used); and net electrical (timing, differential-pair-length tolerances, noise). Within the technology used, these constraint sets may be applied to particular conductor, dielectric, or positive- and negative-plane layers.

Constraints can be read, written, and compared. For example, predefined constraints can be read into an active Allegro layout. Constraint sets from an active layout can also be written to a new or existing file. And comparisons can be made between the constraint sets of an active layout and an existing file. This allows any deviations from a preferred set of constraints to be verified prior to manufacturing.

The Constraints Editor gives users the optimum balance of control and flexibility to ensure that engineering creativity isn't inadvertently handcuffed during the constraint-driven design process. Enforcement may be defined in three ways: always enforced, deferred, or not enforced. When a constraint is always enforced, it's checked by both the interactive and batch DRC operations. When deferred, it's checked only when a separate batch check is invoked. When the constraint is not enforced, it's not considered by any DRC operations. Furthermore, a constraint can be locked, prohibiting users from changing or overriding the values.

Instead of following the traditional design-and-analyze methodology, Allegro CBD's constraint-adherence mechanism follows all constraints to drive the layout process *(see the figure)*. Signal-integrity checks are built into the system, as are traditional checks for physical spacing. All Allegro interactive and automatic tools support these checks.

Many of the performance and quality constraints imposed on designs directly relate to signal-integrity concerns, such as settling delays, clock skews, signal distortion, reflections, and crosstalk. To address these issues, Allegro CBD provides timing-driven placement and crosstalk-driven routing, critical elements of the company's correct-by-design methodology. For example, Allegro CBD features new placement algorithms that satisfy critical path-timing requirements and automatically redistribute the clock nets to minimize skew. The new constraint-driven router avoids crosstalk—while routing, it computes crosstalk caused by putting in a new line segment. If the crosstalk exceeds a user-specified constraint, a new path is found automatically.

THE CONSTRAINTS EDITOR HAS THE OPTIMUM BALANCE OF CONTROL AND FLEXIBILITY TO ENSURE THAT CREATIVITY ISN'T HANDCUFFED.

Allegro CBD is technology independent, so it accommodates multiple packaging technologies. Users have one system that satisfies design and fabrication requirements for multiple packaging technologies, including MCMs, hybrids, multiwire boards, and pc boards. Having one system handle that wide range improves designer productivity by eliminating the steep learning curve associated with adopting multiple design tools for physical layout of different technologies. Productivity is further enhanced because the librarian can easily develop, implement, and maintain multiple packaging-technology definitions. These definitions supply a central control mechanism for managing the many complexities and interdependencies between the design, test, and manufacture of advanced electronic systems. Because design and fabrication specifications are built-in to the design and layout process, it also ensures higher fabrication yields and built-in quality.

With the CBD system, the constraint-definition process is separate from design layout. The Constraints Editor creates external files using an EDIF-like syntax to maintain a standardized structure that contains all constraints, such as physical spacing and placement clearances, as well as electrical constraints for signal noise and timing delays, impedances, and so on. Once the overall design constraints are established, they're applied to specific interconnect technologies (such as MCM, hybrid, and pc board) to drive all design and analysis functions. Through a forms-driven matrix, the Constraints Editor presents users with the constraint options that must be considered for a particular design type, depending upon the interconnect technology involved.□

PRICE AND AVAILABILITY

Allegro CBD is available on Sun, DEC, IBM, and HP RISC-based workstations. Pricing ranges from $12,500 to $60,000, depending on software configuration. Allegro CBD is provided at no charge to Allegro customers on software maintenance.

Cadence Design Systems Inc., 555 River Oaks Pkwy., San Jose, CA 95134; (408) 943-1234. **CIRCLE 512**

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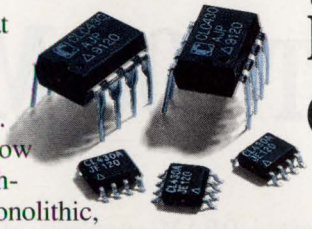

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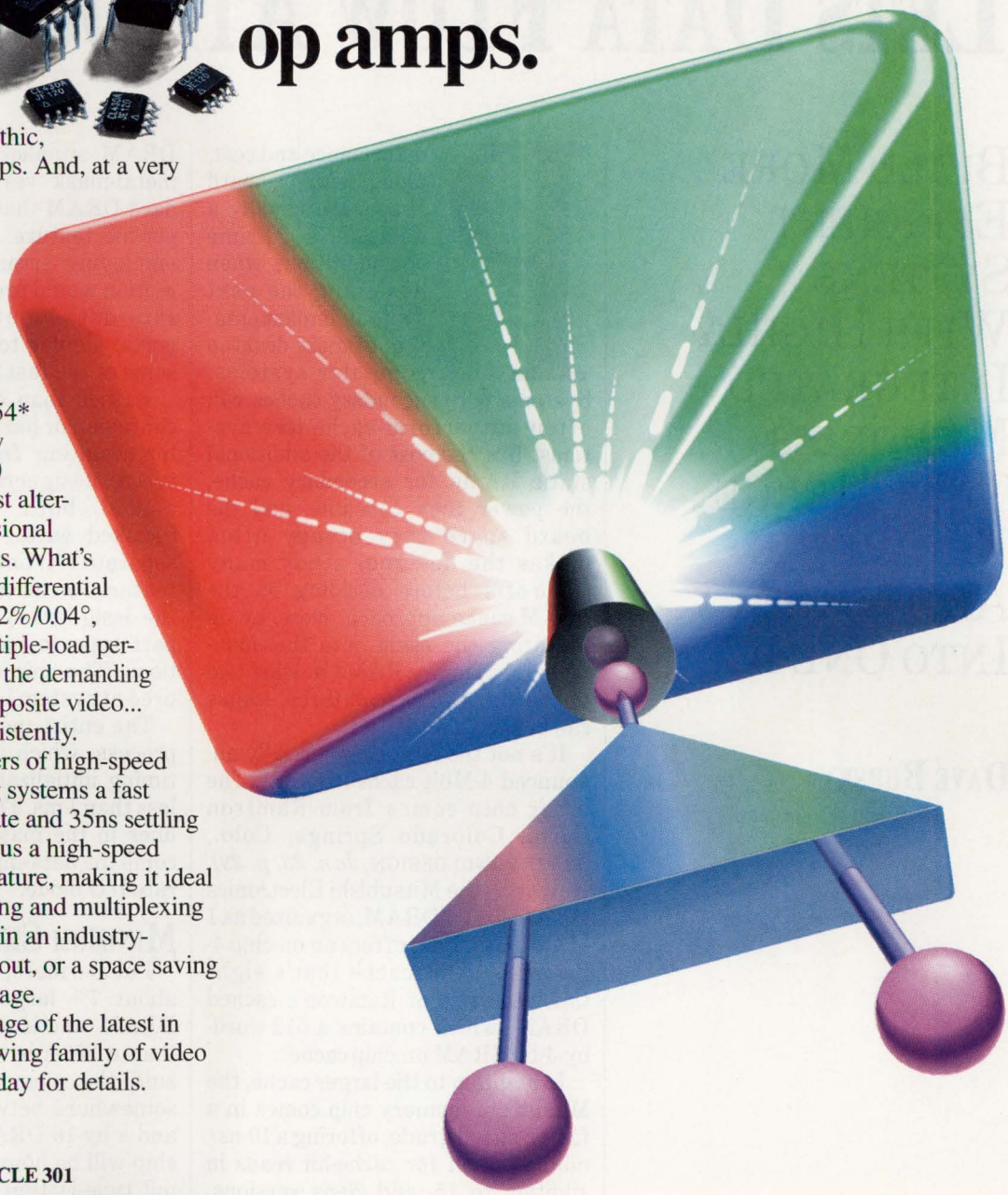

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DAVE BURSKY

Performance and cost, along with pc-board space, are usually a designer's prime considerations when designing the next system implementation of most desktop computer systems. Systems with secondary caches will often outperform cache-less systems. But the cost of the additional static RAMs for secondary cache, the power they consume, and the board space they occupy often makes the designer study many trade-offs before deciding on the SRAM-cache approach. Now, by integrating the cache into the main-memory dynamic RAMs, at least two of the three, if not all three, issues can be put to rest.

It's not the first commercially announced 4-Mbit cached DRAM. The other chip comes from Ramtron Corp., Colorado Springs, Colo., (ELECTRONIC DESIGN, *Jan. 23, p. 39).* However, the Mitsubishi Electronics M5M44409TP DRAM, organized as 1 Mword by 4 bits, offers an on-chip 4-kword-by-4-bit cache that's eight times the size of Ramtron's cached DRAM, which contains a 512-word-by-4-bit SRAM on-chip cache.

In addition to the larger cache, the Mitsubishi memory chip comes in a faster-speed grade, offering a 10-ns/nibble option for cache-hit reads in addition to 15- and 20-ns versions. Standard DRAM accesses take place in 70, 75, or 80 ns, respectively, for the memory's three available speed grades.

For memory systems that require parity, a write-per-bit feature becomes a necessity so that one 1-M-by-4 chip can handle four byte-wide groupings (one bit for every pair of standard 4-bit-wide DRAMs). Most DRAM suppliers offer a separate metal-mask version of their standard DRAM that includes the write-per-bit feature. However, systems employing error checking and correction would prefer chips with separate data-input and data-output ports, similar to the capabilities of some of the fast SRAMs.

Rather than create the ordering confusion or parts proliferation clutter resulting from multiple device types, designers at Mitsubishi included both the write-per-bit (masked write) capability and the separate I/O lines as programmable features on its cached DRAM. Thus, the designer need only order a single part type to handle many applications. The chip can then be configured at system boot time.

The entire memory configuration process, which includes all internal timing initializations, takes place in less than 1 ms. The four Mask Enable lines in the masked-write mode become the data-input lines in the separate I/O mode.

MINIMUM CHIP AREA

Furthermore, the chip area is only about 7% larger than a standard DRAM, and is actually 11% smaller than a 256-k-by-16 DRAM. As a result, the memory's price will fall somewhere between that of a by-4 and a by-16 DRAM. In addition, the chip will be housed in a 44-lead, 300-mil type-II thin small-outline package with a 0.8-mm lead pitch (just 18.4 mm from end to end—about 3/4 of an inch).

There are 16 additional pins on Mitsubishi's cached DRAM than on Ramtron's 28-lead device. More than half of those pins were added to give the chip separate DRAM and cache-address inputs. Consequently, both sections of the chip can be accessed

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simultaneously. Two other pins provide a third set of power and ground lines, and four serve either as the write-per-bit mask lines or as the data inputs in the separate I/O interface-mode option.

To ensure optimum system timing, the memory accepts a master clock signal that can be set from 10 ns to 16 μs. The clock sets all timing for synchronous operation, making the memory the industry's first synchronous DRAM. The high speed of the internal cache enables the same cache DRAMs to operate as the second-level cache, main memory, and even as a video-frame buffer—all in the same system—according to Chris Tennant, an applications engineer at Mitsubishi. However, the chip also has an asynchronous Output Enable pin for bus control, and its DRAM auto refresh is comparable to the CAS-before-RAS (Column Address Strobe-before-Row Address Strobe) refresh available on standard DRAMs.

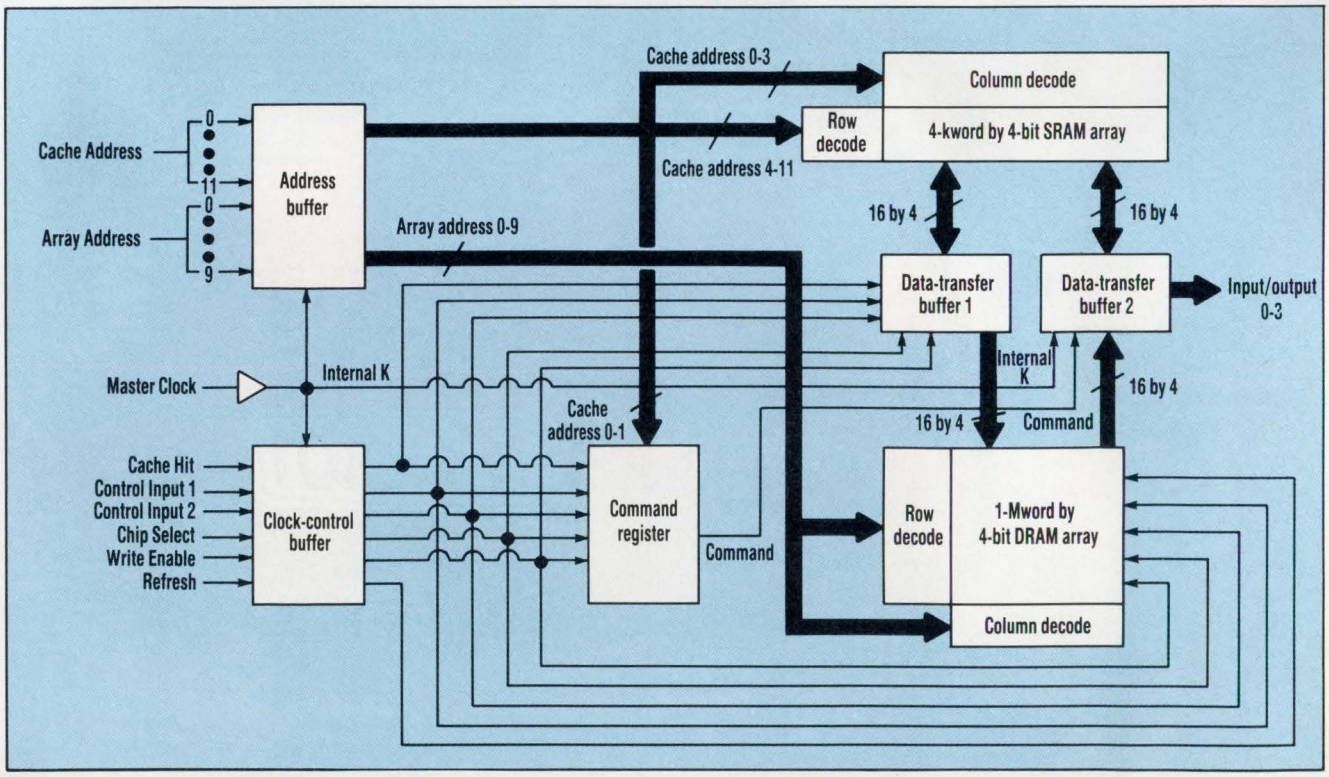
In a 32-bit memory system, eight of the chips would be linked together to form a 1-M-by-32 array (nine to form a 1-M-by-36 array with parity). The cache portion of the array is 16 kbytes (4 k by 32) and its efficiency is significantly better than a much larger discrete cache. That's because the transfers between the DRAM and cache portions of the chip take place 16 lines at a time (16 words by 4 bits). In fact, according to some Mitsubishi studies, the 16-kbyte embedded cache with its 64-byte block size has a hit rate equivalent to a 128-kbyte cache that employs a 4-byte block size.

Bottleneck Breaker

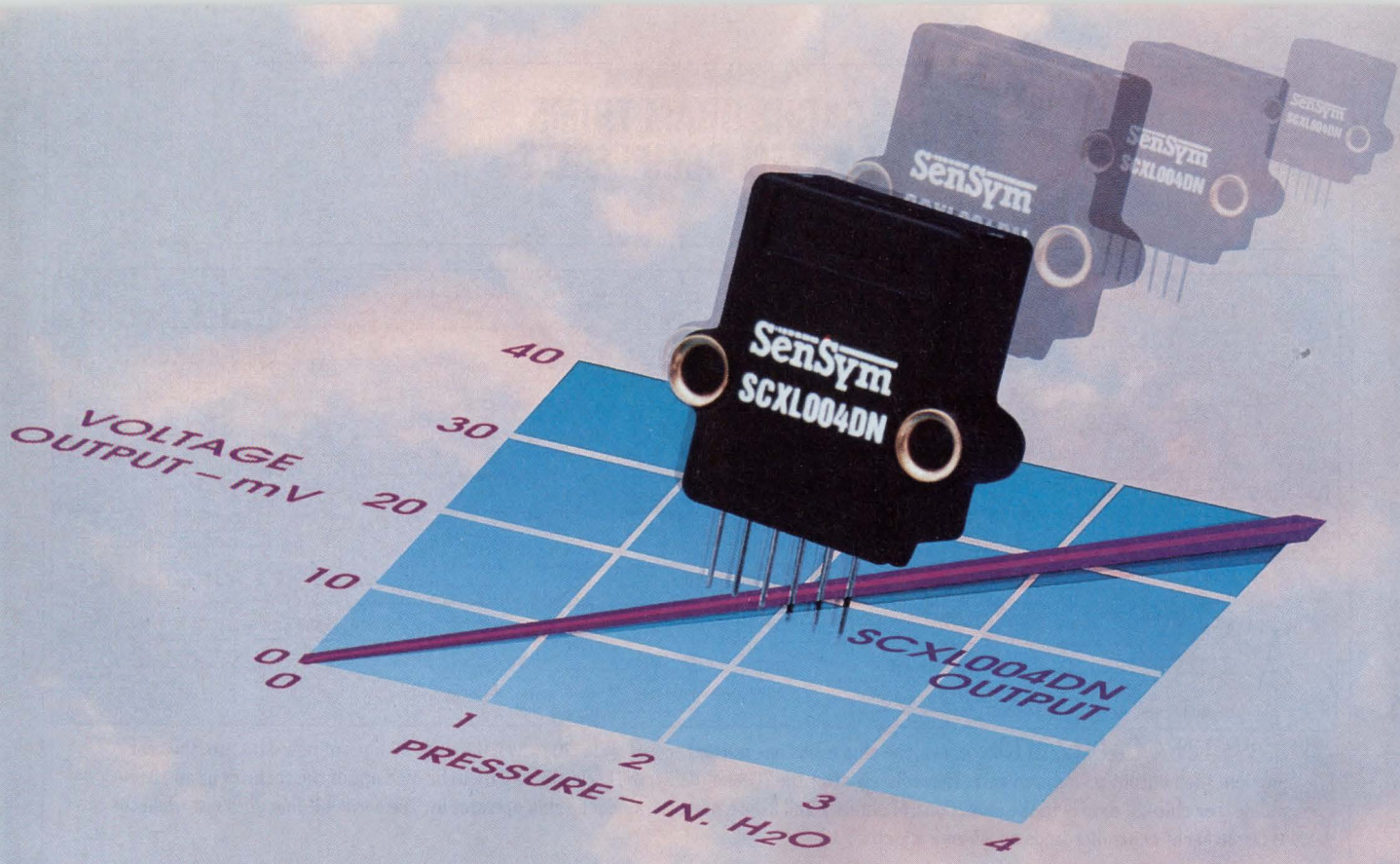
The embedded cache breaks the word-serial "bottleneck" between the DRAM and cache in discrete systems. The single-cycle replacement (one DRAM access cycle of 70 to 80 ns) of 16 cache lines greatly improves the system efficiency. Like the other cached DRAM, integrating the cache on the same chip with the DRAM provides the very wide data-transfer path that enables all 16 lines to transfer in one cycle.

The fast copy-back capability that updates the cache in about one-third the miss cycle time of a conventional copy-back scheme takes advantage of two internal data-transfer buffers *(Fig. 1)*. The miss data is latched into one of the data-transfer buffers while the expected data is transferred simultaneously from the DRAM to the SRAM through the second data-transfer buffer's amplifiers. As a result, the expected data becomes available in just one DRAM access cycle.

One typical event is a cache miss in which the chip must read the new lines as well as copy back the updated data to replace the stale data in the DRAM array *(Fig. 2)*. When the clock line goes high, the DRAM data is read and transferred to the cache block and outputted in one 70-80-ns access cycle. Then, during the following clock cycle, the cache hit line goes low if the next desired data is residing in the cache. That data can



1. TWO DATA-TRANSFER BUFFERS in the cache DRAM from Mitsubishi allow the memory to implement a fast copy-back scheme. Miss data is latched into one buffer while the expected data is transferred simultaneously from the DRAM to the SRAM through the second data-transfer buffer.



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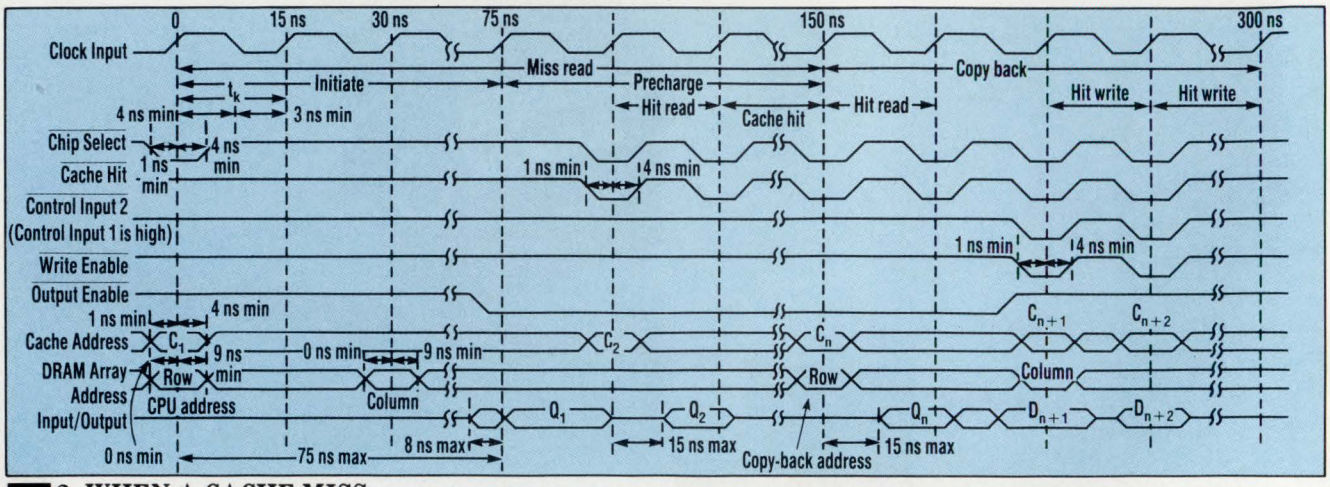
CACHE DRAM TRIMS SYSTEM COMPLEXITY



2. WHEN A CACHE MISS occurs, the chip needs one normal access cycle (70 to 80 ns) to load 16 lines of new data into the cache portion, then output the desired data. Immediately after the 70-80-ns delay, the cycle allows data to be read out of the cache at up to 10 ns/nibble (per chip), if data is in the chip. Control inputs 1 and 2 determine the mode the chip operates in. The cache-hit line goes low when the external cache controller finds an address match.

then be read from the cache over the I/O lines.

Because cache I/O transfers can occur in parallel with DRAM array operations, the copy-back transfers into the DRAM array are performed in the background. This operation requires 280 to 320 ns to complete. If the data in the cache isn't "dirty," the copy-back cycle needn't be performed, because the contents are the same.

To give designers lots of flexibility in their system implementations, many aspects of the chip's operation are user-configurable through patterns loaded into internal command registers. For instance, power consumption can be set for either a low-power mode that saves power at the input buffers, or the standard high-speed mode that allows 100-MHz data transfers.

There are several other programmable features. These include the ability to select transparent, latched (available after the falling edge of the clock input), or registered (available after the next rising edge of the clock input) output interfaces. Moreover, the chip can be user-programmed for either separate-I/O 4-bit-wide operation, or for write-per-bit (masked-write) operation.

The device's ability to map the cache blocks anywhere within the DRAM address space is also user-programmable. The chip outputs must operate in the transparent mode when the circuit is used in the low-power mode.

To handle a memory array composed of multiple cached DRAMs, system designers must create a controller. In a controller for a direct-mapped cache, there would have to be some tag memory (8 words by 256 bits), a valid-bit memory (1 word by 256 bits), some decoding logic, comparison circuits, and some selection logic.

For a four-way set-associative cache, the tag memory would be designed as four banks of 8 words by 64 bits. The valid-bit memory would alter to four banks to an organization of 1 word by 64 bits.

POWER PICTURE

When active, the chip's cache portion consumes 737, 556, and 369 mW, respectively, at access times of 10, 15, and 20 ns. At those same speeds, the DRAM segment of the chip consumes 360, 336, and 314 mW, respectively. In an actual 40-MHz system application, those power numbers translate into a 140-mW dissipation during a cache-hit cycle, and about 450 mW during a cache hit and array copy-back cycle.

In another example, four cache DRAMs could be used in a 386SX system to form a 2-Mbyte memory with 8-kbyte cache. Such a system would draw just 69 mA when active and just 0.8 mA on standby, while improving system throughput by a factor of about 25%.

In contrast, a system built with four 256-k-by-16 DRAMs would consume 80% more active current and about 25% more standby current. The low-power mode of the cached DRAM can reduce the average total power consumption to as little as 10 mW if the clock input line is toggled intermittently (a clock period of 30 ns or larger).

In the works is an even lower-power version—a device that will trim the power drain down to a level of 1 mW. This will be achieved by using an extended-refresh mode.□

PRICE AND AVAILABILITY

The M5M44409TP comes in a 300-mil 44-lead thin small-outline surface-mounted package with a 0.8-mm lead pitch. Initial samples will be available next quarter. In 100-unit quantities, the 20-, 15-, and 10-ns cache DRAMs (cache-access versions) will sell for $15.00, $15.50, and $16.20 each, respectively. Production will start in the third quarter.

Mitsubishi Electronics America Inc., 1050 E. Arques Ave., Sunnyvale, CA 94086; Mai Ha, (408) 730-5900. **CIRCLE 513**

HOW VALUABLE?	CIRCLE
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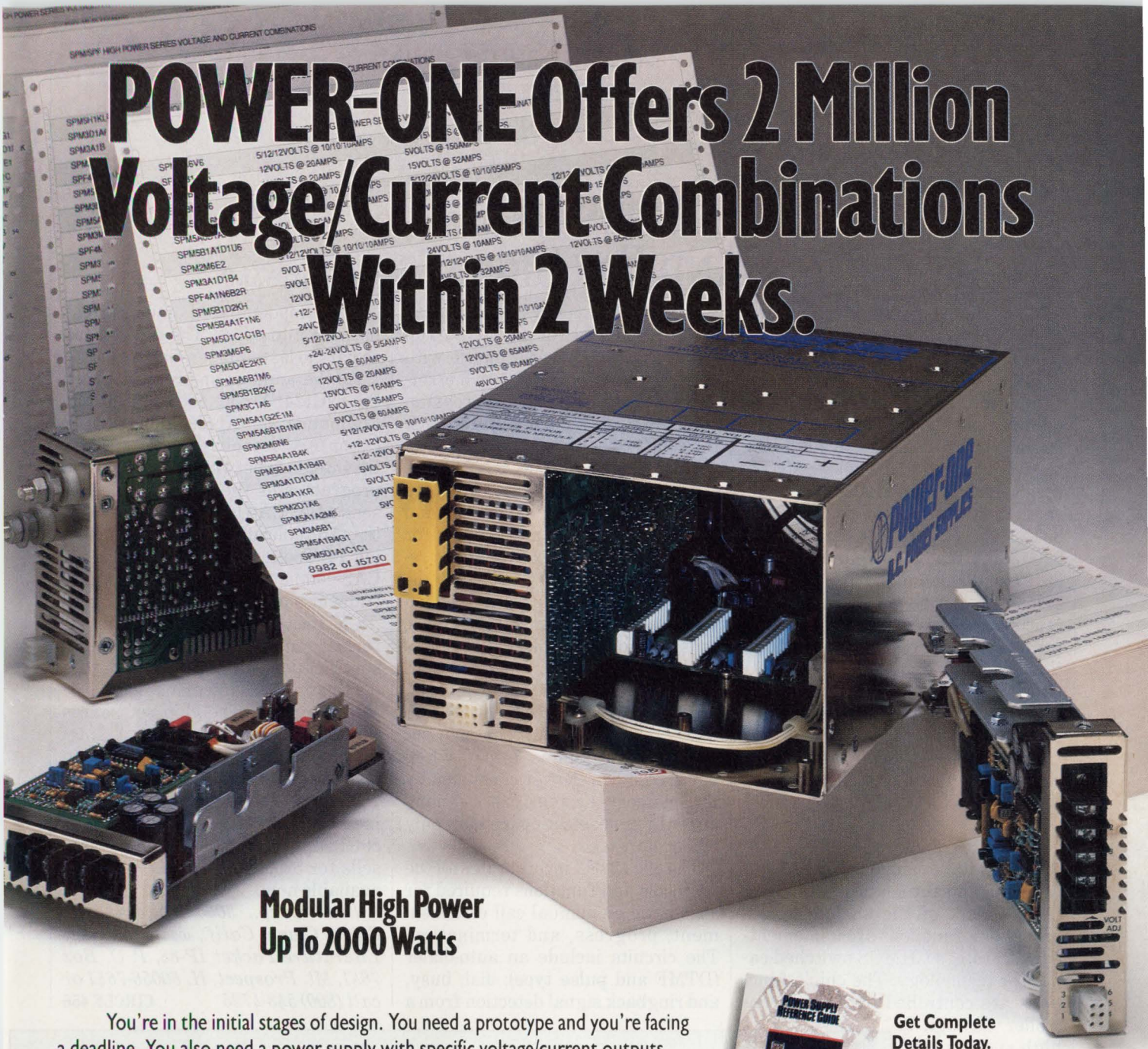

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CIRCLE 204 FOR U.S. RESPONSE

CIRCLE 205 FOR RESPONSE OUTSIDE THE U.S.

Two-Chip Modem Sends And Receives Data And Fax Signals

Milt Leonard

Requiring only external memory chips and a telephone-line interface, the 89C124FX two-chip set from Intel Corp. implements a full-featured data-fax modem while typically consuming just 530 mW from a 5-V battery. Featuring 9600-bit/s send-and-receive fax, and V.42/V.42bis error correction and data compression, the 89C124FX chipset consists of the 89C126FX microcontroller and the 89127 analog front end (AFE).

Housed in a 68-pin PLCC, the microcontroller executes digital signal processing algorithms for modulation, demodulation, and data formatting, and provides user-interface functions. It requires a single 128-kword-by 8-bit ROM and a 32-kword-by-8-bit RAM to execute standard or custom code to perform V.42/V.42bis, MNP4/5, and fax-protocol functions.

The 89127 analog front end provides digital-to-analog conversion, filtering, and automatic gain control (AGC). Most of the analog signal-processing functions are implemented with Intel's CHMOS switched-capacitor technology. The chip's functions are controlled by a microcontroller through a high-speed serial data link.

Occupying only 3 square inches of pc board space, the 89C124FX modem ICs and associated components are suited for use in notebook and laptop computers.

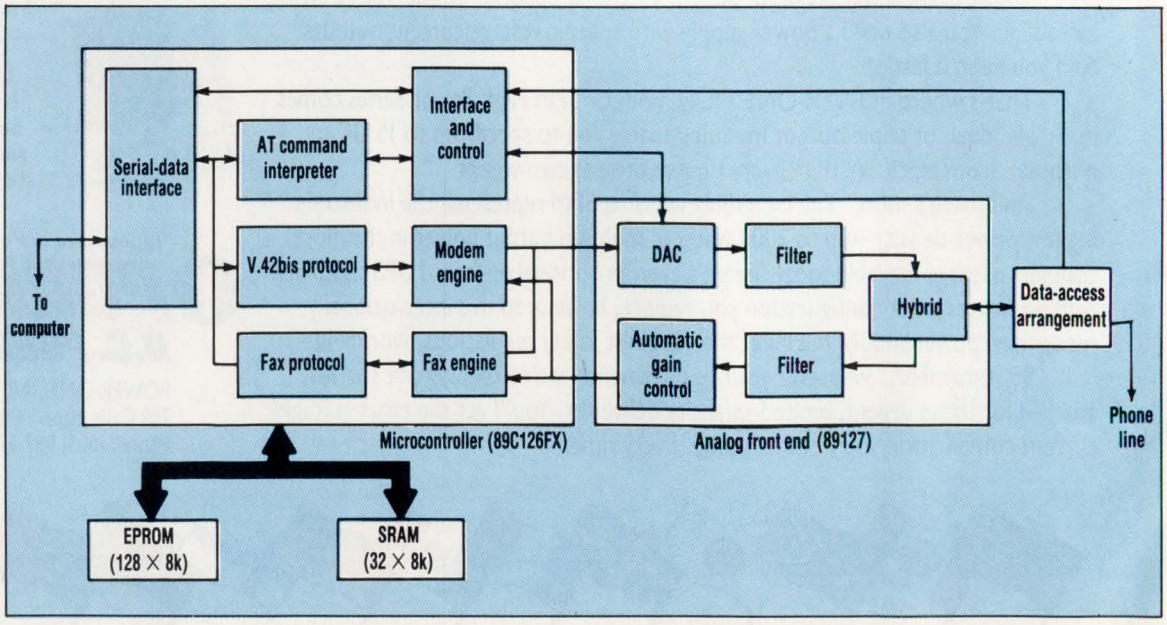
The chip set is compatible with CCITT (Consultative Committee for Telephony and Telegraphy) V.29 and V.27ter specifications for sending and receiving faxes at 9600 and 4800 bits/s. Data can be transferred at virtual rates up to 9600 bits/s, in conformance with V.42, V.42bis, and MNP 1 to 5 error-correction and data-compression standards. The modem can drop back to 2400-, 1200-, or 300-bits/s rates as needed for compatibilty with CCITT V.22bis, V.22, V.21, and Bell 103 and 212A. It also executes the AT and EIA-578 (Class 1) command sets for data-modem and fax operation, respectively.

Power-down modes are selected through the AT command set. Power consumption is typically 530 mW during a connection. When the AFE is not connected to a remote modem, an idle mode reduces power consumption to 365 mW. The chip set typically consumes 7 mW when powered down. Power consumed by the memory system can be minimized by chip-selecting memory only when addressed.

The 89C124FX incorporates all the protocols and functions required for automatic or manual call establishment, progress, and termination. The circuits include an auto-dialer (DTMF and pulse type); dial, busy, and ringback signal detection from a remote modem; and call-progress messages to users. The modem can redial the last number dialed.

At the application-program level, the 89C124FX chip set supports the Communiation Application Specification (CAS) standard, which defines the interface between an application program and the tasks needed to send a fax. CAS is supported by more than 75 application programs, including PC Tools, Q&A, and cc:MAIL. A CAS-compatible driver can schedule transmissions, convert ASCII and .PCX files to compressed graphics format required by the Group 3 fax specification, dial and connect to a destination fax, and manage fax session protocols. The chip set shares the architecture of existing Intel data-modem designs. Intel offers an in-circuit emulator and software-development tools for OEM-customized modems. In thousands, the 89C124FX data/fax modem chip set sells for $29.85 per set. Samples are available now.

Intel Corp., 3065 Bowers Ave., Santa Clara, Calif., write for Intel Literature Packet IP-88, P. O. Box 7641, Mt. Prospect, IL 60056-7641 or call (800) 548-4725 **CIRCLE 456**



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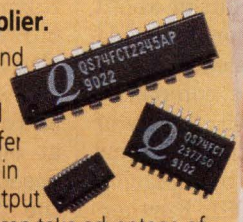

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2191	2374	2648	2845
2193	2377	2651	2854
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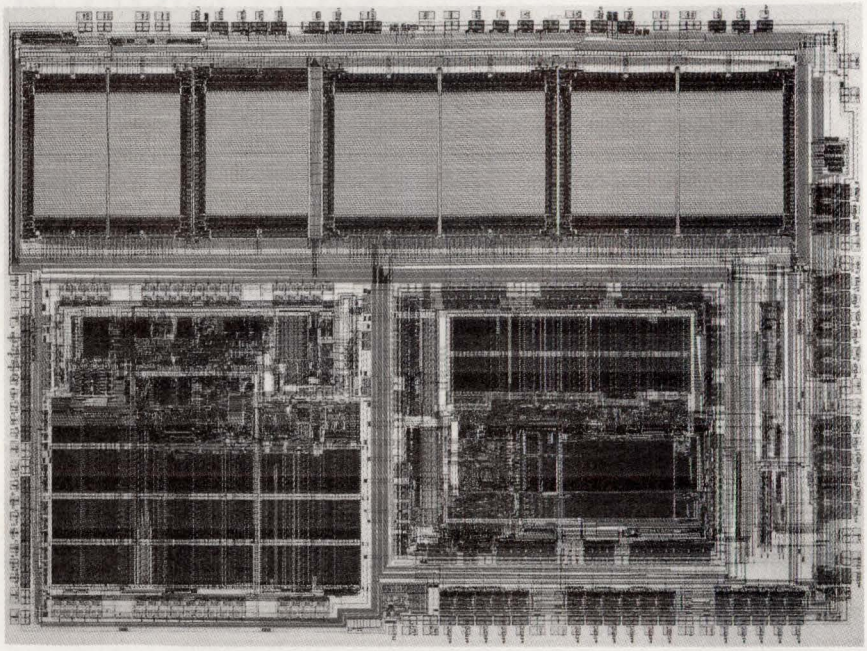
CIRCLE 234 FOR U.S. RESPONSE CIRCLE 235 FOR RESPONSE OUTSIDE THE U.S.

HIGH-INTEGRATION RISC PROCESSOR TARGETS ACE PLATFORM DESIGNS

DAVE BURSKY



Based on the R3000A processor core, the IDT79R3081 integrates the floating-point coprocessor as well as many of the support circuits and memory needed to form a complete CPU subsystem. Such a subsystem can form the heart of a low-cost platform that meets the requirements of the Advanced Computing Environment (ACE) platform specification based on the MIPS-family of RISC processors. Developed by Integrated Device Technology, the R3081 32-bit processor packs a full R3010A-compatible floating-point coprocessor, large on-chip configurable caches (20 kbytes total) as well as four-level-deep read and write buffers and an arbiter for direct-memory-access control.

The processor will be available in clock speeds ranging from 20 to 40 MHz. At the 40-MHz top speed the chip delivers a throughput of about 35 MIPS, 64,000 Dhrystones, and 11 MFLOPS. Since the 84-lead CPU is pin-compatible with the company's previously released R3051 family of RISC processors, existing systems can be upgraded simply by replacing the R3051 with the R3081. Furthermore, like the R3051, the new CPU also comes in two versions, one with the on-chip memory-management unit for virtual-memory subsystems, and a version without the on-chip MMU for real-time applications (the R3081 and R3081E).

Depending on the application the processor will handle, the cache organization can be switched from its default configuration of 16 kbytes of instruction cache and 4 kbytes of data cache to equal 8-kbyte I and D caches. The organization can be dynamically reconfigured, thus eliminating the need to reset the processor. However, all data in the cache must be invalidated each time the configuration is altered.

On-chip cache-coherency support circuits ensure data integrity during DMA writes. The chip can invalidate a specified line of data cache or perform burst invalidations during burst-DMA writes. The processor also has a flexible system interface that employs a multiplexed address and data bus and can operate the bus at either the full processor clock speed or at half the clock rate to ease the timing restriction for support logic. An on-chip clock generator allows the user to employ an inexpensive single-phase external clock source and will internally double the clock frequency when the highest-performance option is selected.

To minimize system pipeline stalls due to data-write operations, the 4-level write-buffer intercepts writes to memory and allows the processor to continue with its next operation, while writing the buffered data to main memory at a slower rate.

The small size of the R3081 chip in comparison to the recently released R4000 CPU makes the R3081 a more cost-effective solution for low-end ACE systems since the performance of it is close to that of the internal-cache-only version of the R4000. On-chip drivers allow the R3081 to source or sink many CMOS loads up to a bus capacitance of about 50 pF. That drive capability eliminates the need for buffers in small systems. When running at top speed, the processor will dissipate between 4 and 5 W, while at 20 MHz, maximum power drain is about 3.5 W.

Existing MIPS software can run on the R3081 since its instruction set it binary-compatible with the MIPS instruction-set architecture. The software compatibility also allows the chip to immediately take advantage of the existing software development tools and application libraries. Additional tools such as a full behaviorial simulation model will be available later this year.

The R3081 can be used in 3-D color X-terminals, PostScript-compatible laser printers, and graphic accelerators. Samples of the R3081 will be available later this quarter. Prices for the processor start at $130 in thousands for the 20-MHz version; the price for higher volumes drops to under $100.

Integrated Device Technology Inc., 3236 Scott Blvd., P. O. Box 58015, Santa Clara, CA 95052; Bob Rowe, (408) 492-8631. **CIRCLE 457**

HARDWARE AND SOFTWARE ADD TO RS/6000 FAMILY

The performance and flexibility of IBM's RISC System/6000 family is growing with the addition of five new models and some software offerings. The five platforms include three desktop systems—the 220, 340 and 350—and two deskside systems—the 520H and 560. All are based on the company's Performance Optimization with Enhanced RISC (Power) architecture and Micro Channel bus.

The 33-MHz model 220 is currently the lowest priced RS/6000 system—$9715. The platform is based on a single-chip implementation of the Power architecture. It can operate as a network-attached diskless system, a standalone workstation, or as a server. Ethernet and SCSI interfaces are built in. The 340 is a 33-MHz system that delivers 56.6 SPECmarks and 14.8 MFLOPS. The 350, at 42 MHz, offers 71.4 SPECmarks and 18.6 MFLOPS. The 520H supplies a 25% floating-point performance improvement over existing 520 systems. It comes with a 25-MHz processor. The 560 is the most powerful RS/6000 system to date. With its 50-MHz RISC processor, it achieves 89.3 SPECmarks and 30.5 MFLOPS, the performance needed for compute-intensive multiuser applications. Prices start at $64,110 for a workstation and $62,240 for a server.

A new version of AIX, Version 3.2, heads the software offerings. The latest release of IBM's version of Unix features usability and performance improvements, as well as enhanced system management facilities. It adds some features to take advantage of the new hardware platforms as well as the Power Gt3 graphics adapter and 9330 high-performance disk-drive subsystem. Prices range from $650 to $40,900, depending on the number of users.

***IBM Corp.**, 1133 Westchester Ave., White Plains, NY 10604.* **CIRCLE 458**

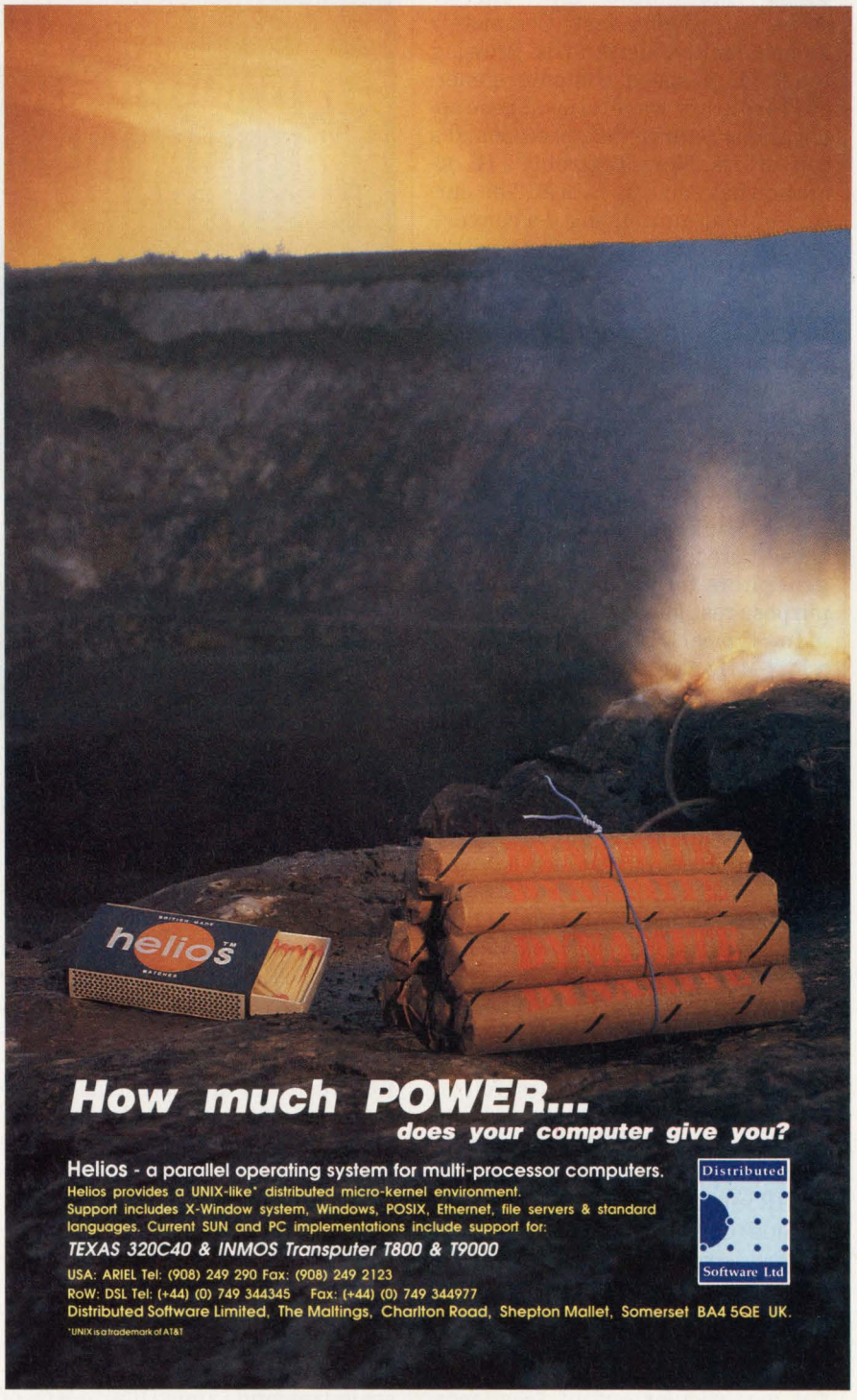
■ *RICHARD NASS*

CARTRIDGE HOLDS USER-PROGRAMMABLE FONTS

Typically, laser-printer cartridges come with built-in fonts. The FontMaster cartridge from Kelly Computer Systems comes with more than 100 fonts, but it can also be programmed by the user with bit-mapped or scalable fonts, forms, or macros.

This helps speed development and printing times by eliminating the downloading of soft fonts each time that they are used. The fonts permanently reside in the cartridge. Users can program a cartridge in a few minutes using FontMaster software utilities. Any soft fonts compatible with HP LaserJet printers are supported. The card comes in 1- and 2-Mbyte versions and sells for $449 and $599, respectively.

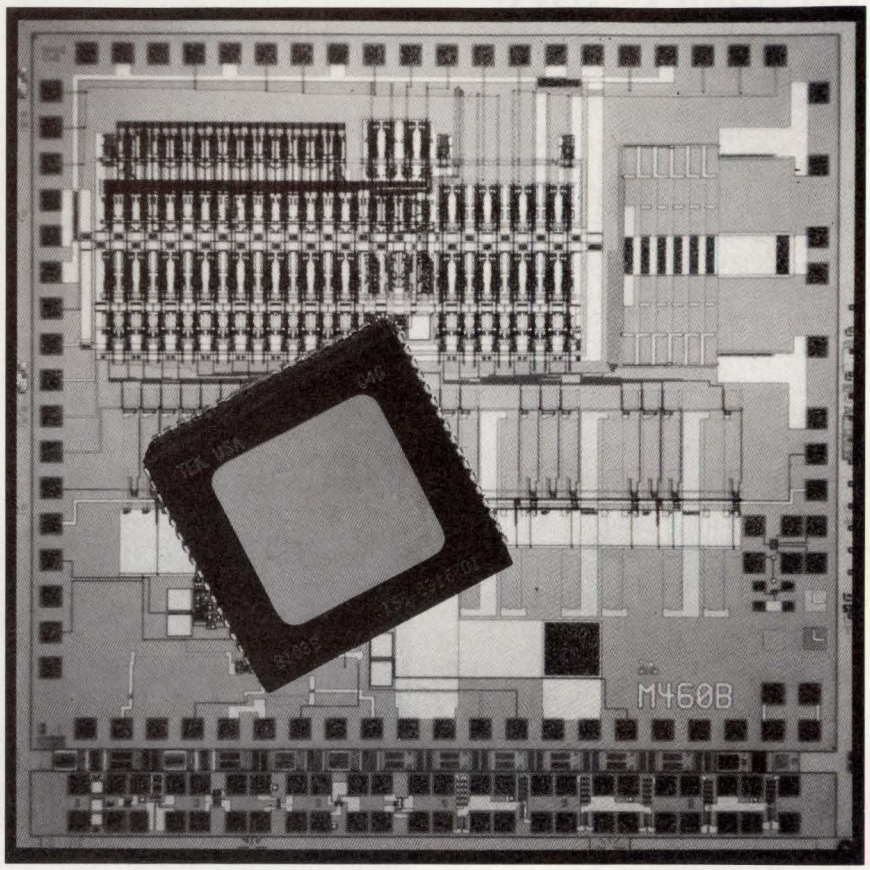
Kelly Computer Systems, 274 Ferguson Dr., Mountain View, CA 94043; (415) 960-1010. **CIRCLE 459**



CIRCLE 98 FOR U.S. RESPONSE
CIRCLE 99 FOR RESPONSE OUTSIDE THE U.S.

100-MHz DAC Creates 10-MHz Sine Waves With An SFDR Of 55 dB

Frank Goodenough



Demand for direct digital synthesis (DDS) of radio-frequency waveforms, both modulated and carrier alone, is growing fast. Completely independently, demand is growing too for high-speed, computer-generated arbitrary waveforms. These applications require fast, precision, d-a converters. Now, Tektronix's IC operation has come up with a 12-bit current-output multiplying d-a converter (M-DAC) that can operate with a 100-MHz clock (100-MHz update rate). Called the TKDA30, this DDS IC DAC is built on the company's oxide-isolated Super Hi Pi (SHPI) process, which provides npn transistors with an f_t of 8.5 GHz.

The converter was developed for RF applications, such as replacing local oscillators in transmitters and receivers. But it can find use in high-speed, precision, pulse and signal generators for general- and special-purpose test jobs *(see p. 41)*.

In a typical DDS application, using a 14.3-MHz clock to produce a 2-MHz sine wave, the DAC achieves a typical spurious-free dynamic range (SFDR) of 65 dBc. At a clock rate of 50 MHz SFDR runs 68 dB for a 1.5-MHz sine wave. Upping the clock rate to 80 MHz, and the output frequency to 10 MHz, results in a typical SFDR of 55 dBc.

In traditional DAC applications differential nonlinearity and integral nonlinearity (DNL and INL), along with settling time, represent the prime specifications. However, in the burgeoning radio-frequency arena these characteristics fall by the wayside and spurious-free dynamic range, or SFDR, becomes the critical specification. Essentially, SFDR represents the ratio of the amplitude of the output sine wave's largest harmonic to the amplitude of that output sine wave (the carrier). The units of SFDR are dB, or dBc (dB below the carrier). They must be specified at a particular clock rate, for a particular output frequency. Most suppliers of DDS DACs specify SFDR at several clock rates and with several output frequencies. However typical, rather than guaranteed, specifications are usually given because of the difficulty (cost) of production testing the parameter.

Unlike many IC DDS DACs, which specify DNLs and INLs of 2 or more LSB (that is potentially they are not monotonic), the TKDA30 is a true 12-bit device at dc. Its precision thin-film resistors are laser-trimmed to guarantee both DNL and INL errors of less than 0.012% of full scale, or better than 1/2 LSB at 12 bits. While such performance is not required for communications applications, it truly enhances using the DACs in synthesizing high-speed, precision, arbitrary waveforms. The ICs, guaranteed-maximum absolute gain (full-scale) error and typical sub-1-ns full-scale transition time (10%-to-90% of full-scale output swing) also add to its performance in this application.

As noted, the TKDA30 is a current output DAC offering a full-scale current of 20 mA with 1-V of compliance. Its source impedance is also laser-trimmed, resulting in a value guaranteed to be between 49.5 Ω and 50.5 Ω. For maximum speed, the output should drive a terminated 50-Ω load, like a transmission line, at the output of which it produces 0.5-V full scale. But it can also drive a virtual ground and achieve 12-bit accuracy.

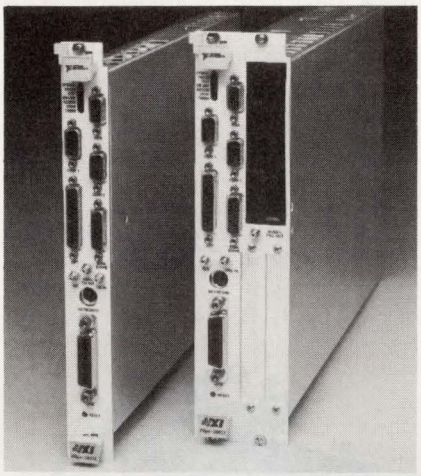
The TDKA30 comes in a 1-in. square, 68-pin, quad plastic flat pack and in die form. In hundreds the packaged device goes for $118 each. Hundreds in die form run $90 each. DACs are available from stock.

Tektronix Inc., Howard Vollum Park, P. O. Box 500, M/S 59-420, Beaverton, OR 97077-0001; Dave Bernel (503) 627-7625. **CIRCLE 460**

EMBEDDED VXI CONTROLLERS SUPPLY 386SX PERFORMANCE

Two embedded VXIbus controllers offer full 80386SX PC/AT capability in C-size modules. The VXIpc-386SX controllers feature 20-MHz speed and up to 16 Mbytes of RAM.

The VXIpc-386SX/1, which fills one slot, includes a 40- or 80-Mbyte hard-disk drive. The VXIpc-386SX/2, which takes up two slots, adds a 3.5-in. floppy drive and has up to 525 Mbytes of hard-disk storage. An optional expansion kit for the VXIpc-386SX/2 holds two PC plug-in boards. Both controllers have an IEEE-488.2 port, advanced VXI trigger capability, and an optional math coprocessor.



The new modules are controlled by the company's NI-VXI DOS and NI-VXI Windows software. These packages include a resource manager, an interactive VXI resource eidtor program called VXIedit, a comprehensive library of VXI driver software routines for VXI programming, and a VXI interactive control program for monitoring and interacting with VXI devices. IEEE-488 instruments can be controlled using the NI-488.2 software.

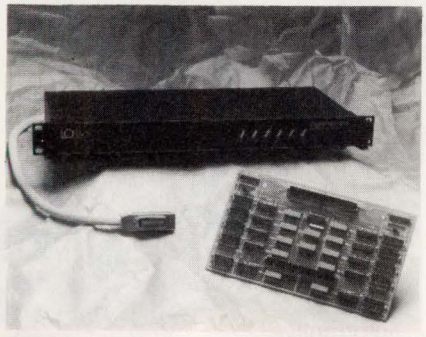
Prices for both models start at $3995. NI-VXI for DOS or Windows costs $795, and NI-488.2 for DOS or Windows costs $295. Delivery is in 6 to 8 weeks.

National Instruments Corp. 6504 Bridge Point Pkwy., Austin, TX 78730-5039; (800) 433-3488 or (512) 794-0100. **CIRCLE 461**

■ *JOHN NOVELLINO*

GPIB INTERFACE OFFERS HIGH-LEVEL LOGIC OPTION

The Digital488/80A digital I/O interface offers 80-line capability to or from the IEEE-488 bus via two 40-line ports. The lines are software selectable as inputs or outputs in 8-bit multiples. Each 40-line channel has six handshake lines: trigger, data strobe, inhibit, clear output, service request, and external data ready. An optional HVCX1 daughter board allows each port to control 200-mA open-collector drivers. The option also makes the interface compatible with 12-, 24-, and 48-V logic when the unit is used with non-TTL devices. The Digital488/80A costs $995 and the HVCX1 option is $295. Both are available from stock.



IOtech Inc., 25971 Cannon Rd., Cleveland, OH 44146; (216) 439-4091. **CIRCLE 462**

VME INPUT BOARDS OFFER DYNAMIC RANGE TO -80 DB

Applications involving high-performance data acquisition over the VMEbus can use either of two analog input boards that offer a choice of specifications. The ZPB 1603 incorporates the 12-bit, 10-MHz ADC603, which features a spurious-free dynamic range of –72 dB, a signal-to-noise ratio (SNR) of 67 dB, and a total harmonic distortion (THD) of 68 dB. For applications needing a higher dynamic range, the ZPB 1604 uses the 12-bit, 5-MHz ADC604, which has a spurious-free dynamic range of –80 dB, an SNR of 67 dB, and THD of –80 dB. The ZPB 1603 costs $3495, and the ZPB 1604 is priced at $4495. Quantity and OEM discounts are available. Small quantity deliveries are from stock to 4 weeks.

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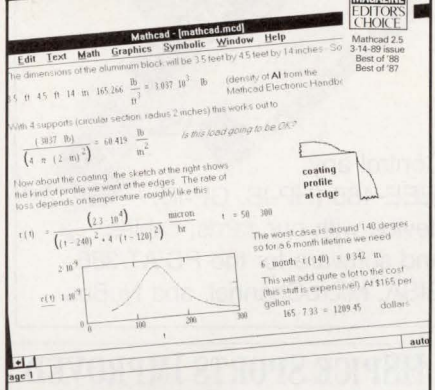

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HSPICE SPORTS IMPROVED GRAPHICAL INTERFACE

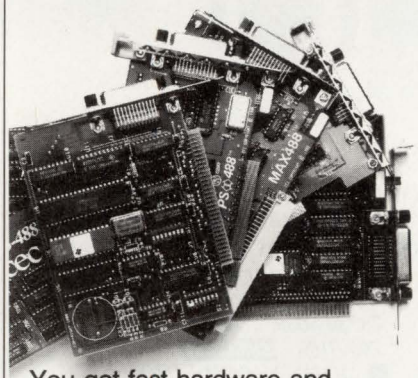
The HSpice circuit simulator now offers an enhanced version of its Graphical Simulation Interface (GSI). GSI is a mouse-driven user interface with interactive capabilities for quick analysis of simulations in an X-Windows environment. A machine-independent file format connects the HSpice output to the GSI, so users can run HSpice on a mainframe and graphically view results on a workstation. In addition, the interface supports concurrent simulation and waveform review, point-and-click node and property selection, interactive curve measurement, and flexible viewing with zoom, pan, and multiple-panel operations. Users can run all HSpice analyses from GSI, including parameter sweep. HSpice handles dc, transient, RF, and microwave circuit simulation. The GSI runs on Unix workstations with X Windows. It's shipping now for $2000 per node-locked license. A floating license will be available by the end of ths quarter. Pricing for the HSpice simulator ranges from $3500 to $90,000, depending on the platform.

Meta-Software Inc., 1300 White Oaks Rd., Campbell, CA 95008; (800) 346-5953. CIRCLE 464

PLD SOFTWARE RUNS IN CAE ENVIRONMENT

ViewPLD, a PLD design and verification system from Viewlogic, works with the company's Workview CAE product, allowing users to design, simulate, synthesize, and re-target in an integrated environment. With ViewPLD, users can import data from all existing PLD design methodologies, including Abel, Jedec, and gate-level descriptions, to generate full-timing VHDL models for simulation and documentation. The software features automatic PLD partitioning, device fitting for 250 architectures and over 4000 standard devices, a VHDL model generator, a logic simulator, and a waveform analyzer. Device fitters automatically assign pins and/or nodes, optimize macrocells, factor logic for channel-based FPGAs, and synthesize to a variety of register types. ViewPLD, which runs on DOS- or Unix-based platforms, is shipping now. Prices range from $5000 to $9000.

Viewlogic Systems Inc., 293 Boston Post Rd. W, Marlboro, MA 01752-4615; (508) 480-0881. CIRCLE 465



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NETWORK SIMULATOR SPEEDS DESIGN CREATION

The popular personal-computer-based Susie simulator can now be used as a network-based, multiuser, real-time logic simulator using a product called Susie/NT. Susie/NT allows many engineers to work on their portions of a design all at once, speeding overall design development. With Susie/NT, users can dynamically exchange design information and share the workload. For example, some engineers may work on a programmable-logic device, while others create a gate array, and some others integrate the partially developed sections. All sections of the design, even if partially completed, can be integrated and analyzed at the board level. This is possible because outputs from improperly operating devices or blocks can be substituted by test vectors representing the properly-working circuit. The Susie/NT software acts as a supervisory program for the single-user Susie programs, and comes with one keylock installed on the network server. Susie/NT is shipping now for $3995.

Aldec, 3525 Old Conejo Rd., Suite 111, Newbury Park, CA 91320; (805) 499-6867. CIRCLE 466

AUTOROUTER DESIGNS FOR MANUFACTURABILITY

Version 3.01 of Cooper and Chyan's Specctra autorouting software lets users incorporate manufacturing requirements for surface-mount technology into the design process. There are two Specctra autorouting products: SP20 for high-density surface-mount pc boards and SP50, which includes all the features of SP20 but adds a set of design rules to handle fast-circuit pc boards. Both products include the surface-mount manufacturability rules, which include such requirements as the elimination of wire bends too close to surface-mounted pads. Also, both the SP20 and SP50 products have new CAD interfaces to the Valid and P-CAD pc-board design systems. Specctra autorouters run on most Unix workstations. SP20, which is available now, costs $29.900. SP50 will ship by the end of this quarter for $44,900.

Cooper and Chyan Technology Inc., 1601 Saratoga-Sunnyvale Rd., Suite 255, Cupertino, CA 95014; (408) 366-6966. CIRCLE 467

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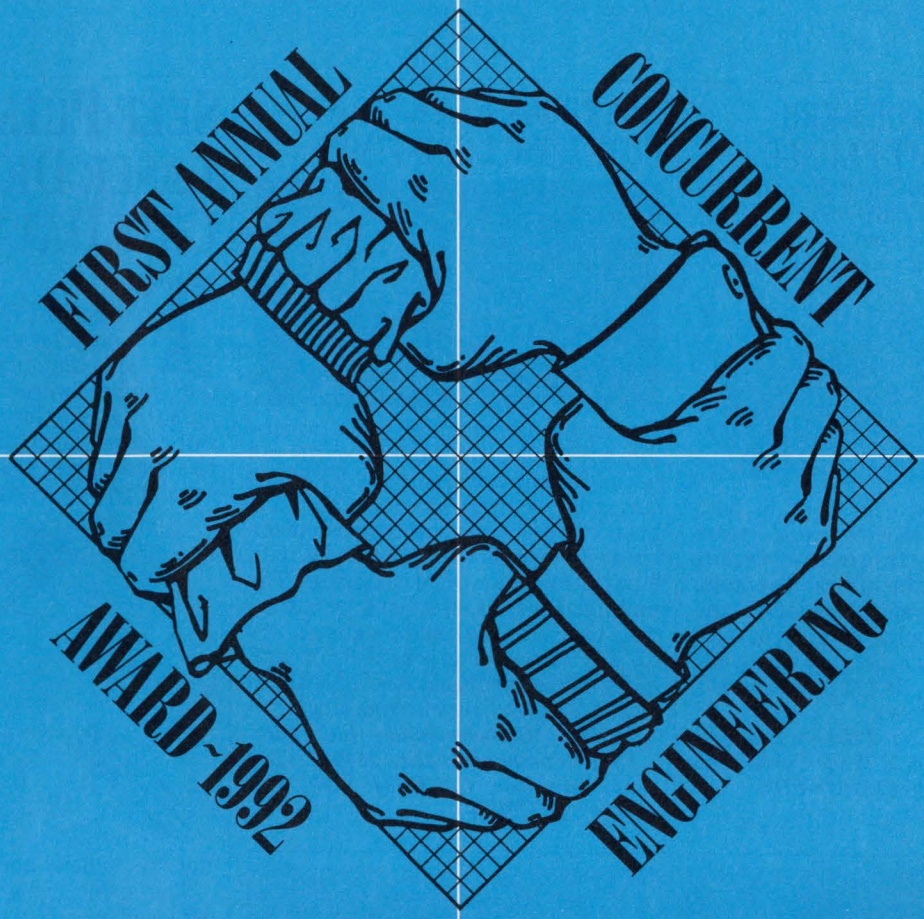

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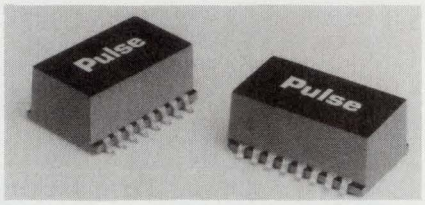
ISDN TRANSFORMERS TAKE THE SMT PLUNGE

One of the last remaining through-hole components now finally offers the cost savings of surface-mount assembly. Pulse Engineering's series of ISDN S-



interface transformers contain both the transmit and receive transformers and operate with transceiver circuits from many manufacturers. The units provide 2000 V rms of isolation and pass the surge-voltage tests of IEC 950, the FCC, and emerging European standards. Pricing is $11 in lots of 500. Delivery is from stock.

Pulse Engineering, Telecom Products Group, 12220 World Trade Center, San Diego, CA 92128; (619) 674-8100.

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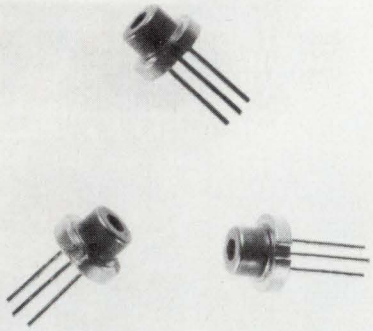
NOTEBOOK KEYBOARD CUTS LONG LEAD TIMES

The long waits and high costs for custom notebook-computer keyboards can be sidestepped by using the FKB7200 series keyboards. The standard keyboards with a low profile and membrane keyboard were developed with input from major OEM customers. The unit measures 11.56 in. long by 5.02 in. wide by 0.59 in. high and weighs about 9 oz. Keystroke travel is a full 3 mm with quiet tactile feedback. Pricing is $21 in lots of 5000. Delivery is from stock.

Fujitsu Microelectronics Inc., Electronic Components Div., 3545 N. First St., San Jose, CA 95134; (800) 642-7616. **CIRCLE 469**

SELF-PULSATING LASER DIODE CUTS DATA COSTS

The cost of fiber-optic transmission in local-area networks and long-distance data communication can be lowered by virtue of a self-pulsating, single-longitudinal-mode, self-aligned laser diode. The RLD Series diode is an AlGaAs, double-heterostructure device that offers modula-



tion frequencies above 1 GHz.

The diode's high frequencies are achieved by means of an extremely low junction capacitance in the die's active area. Thanks to the company's molecular-beam epitaxy process, atomic-layer control of the structure's growth produces an active area that's typically just angstroms thick with a typical surface area of 4 by 250 μm. The resulting device produces very high data-transmission rates with very low noise.

Because epigrowth of the die structure can be programmed literally in layers of atoms, near-infrared wavelengths between 720 and 900 nm can be fine-tuned within ±10 nm. Theoretical modulation frequencies of more than 1.5 GHz can be achieved, which result in an NRZ data-transfer rate of more than 3 Gbytes/s.

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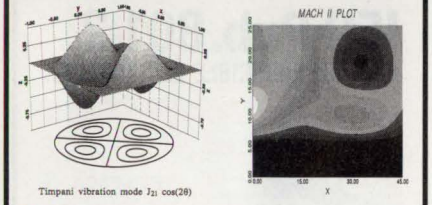

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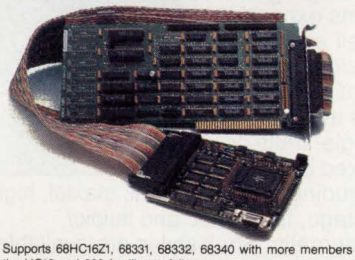

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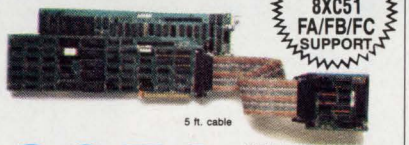

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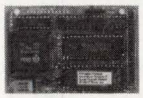

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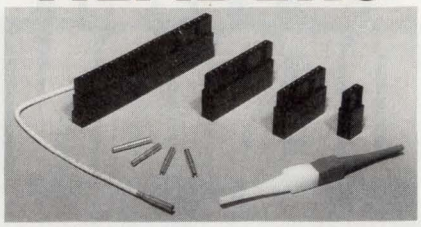

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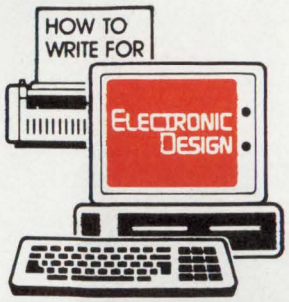

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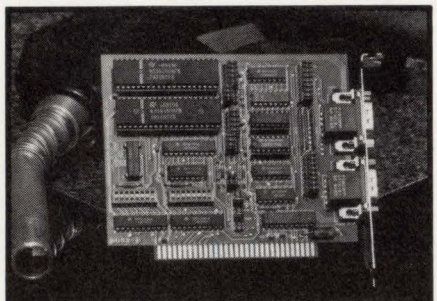

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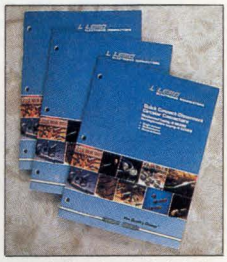

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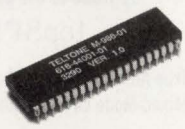

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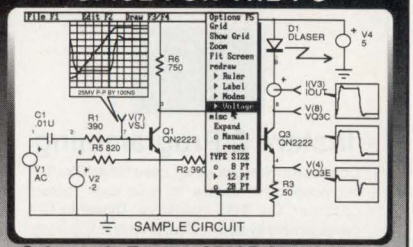

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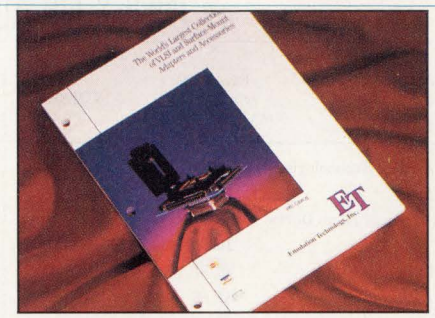

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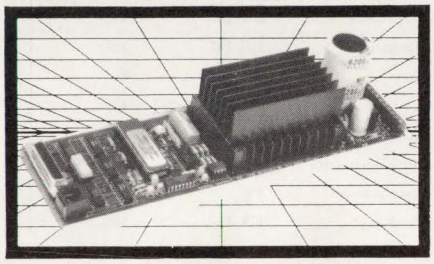

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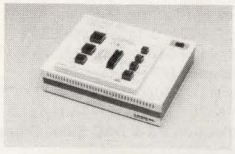

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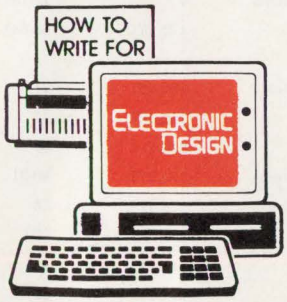

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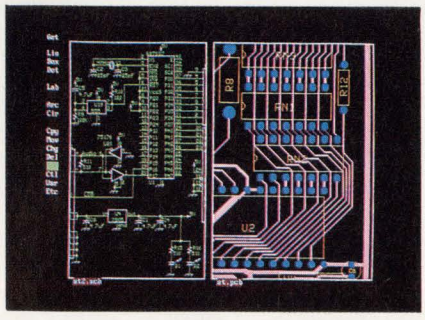

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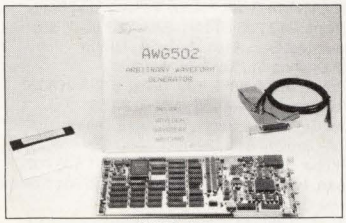

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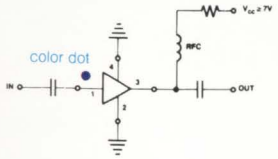

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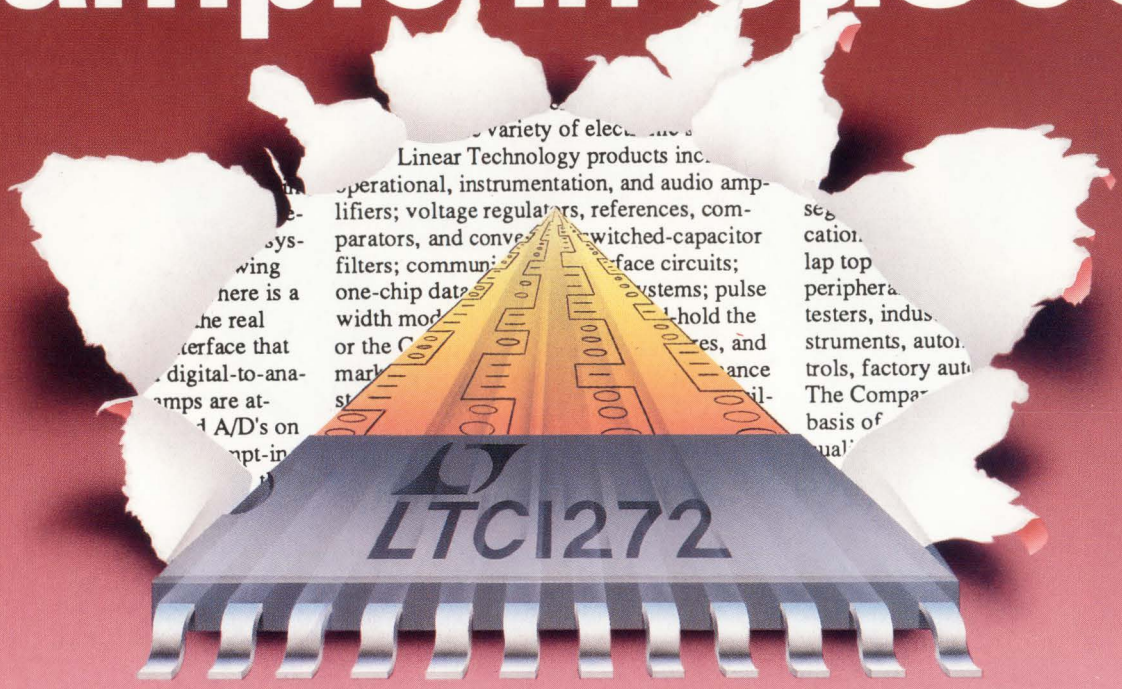

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