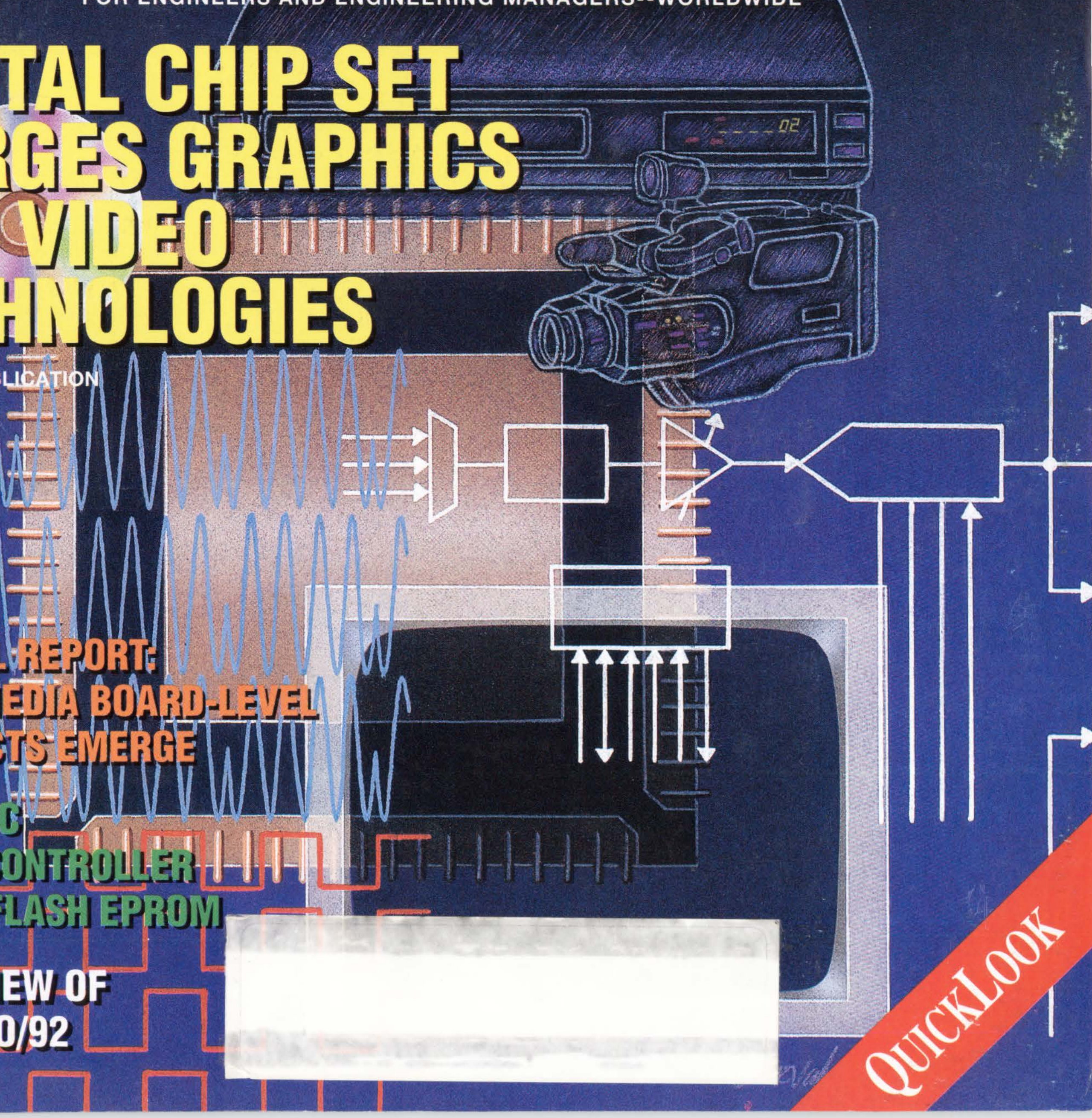
ELECTRONIC DESIGN

May 14, 1992

FOR ENGINEERS AND ENGINEERING MANAGERS--WORLDWIDE

DIGITAL CHIP SET MERGES GRAPHICS AND VIDEO TECHNOLOGIES



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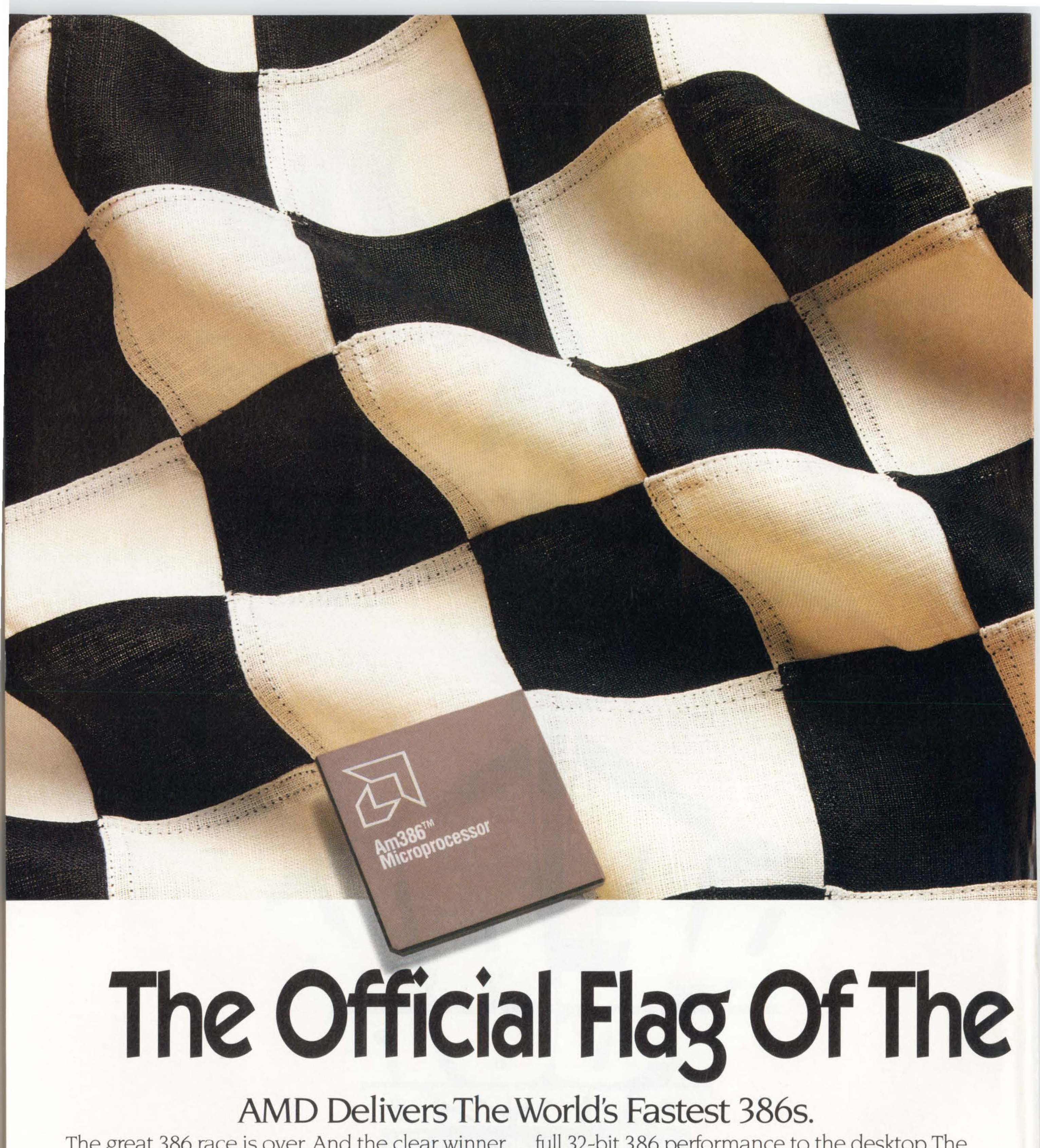
- 16-BIT IC MICROCONTROLLER HOLDS FLASH EPROM
- A PREVIEW OF ELECTRO/92

QUICKLOOK



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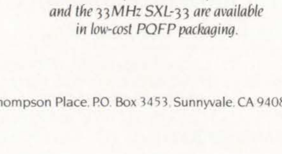

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MAY 14, 1992 VOL. 40, NO. 10

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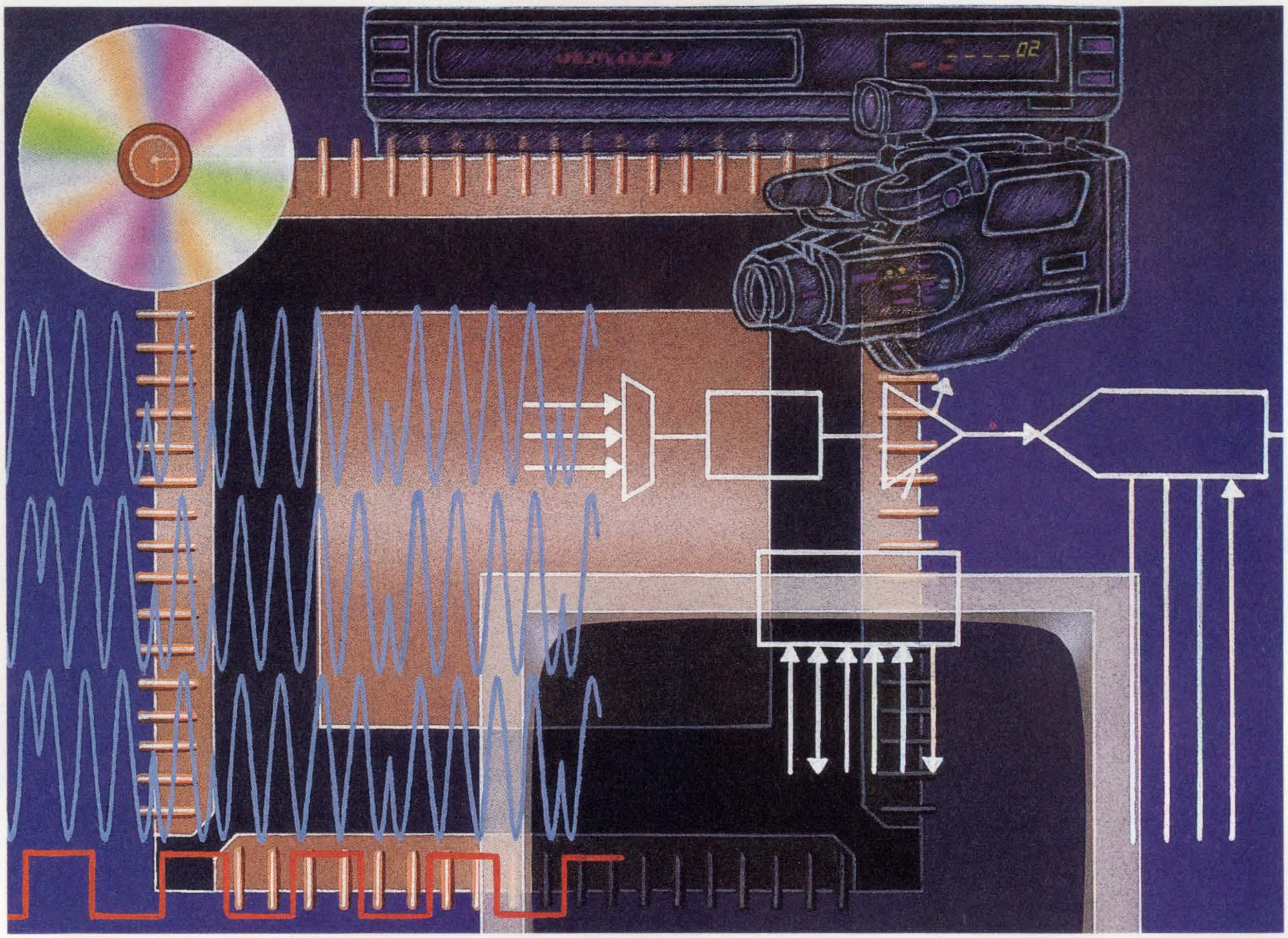

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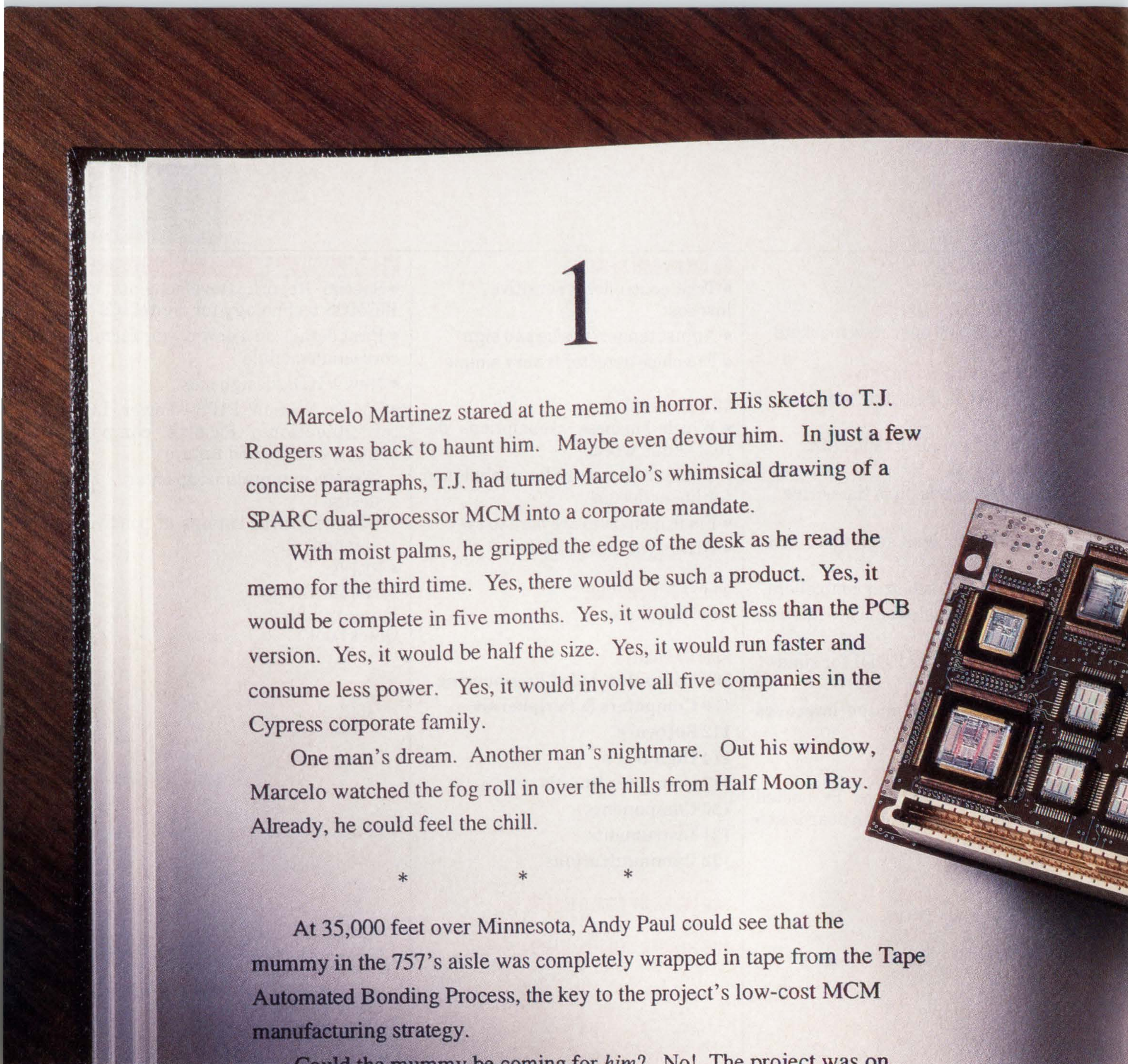

If Only This MCM Could Talk,

At Cypress Semiconductor, the memo from T.J. Rodgers was quite specific:

Create a high-density, dual-processor SPARC® CPU in an MCM the size of a credit card. Eliminate interconnects as a speed limit to the chip set. Put it all on a low-cost PCB substrate. Solve any heat dissipation problem. And finally, make it manufacturable and cost-effective in volume.

Why all the fuss? Simple. Cypress realized that the next generation of SPARC chips will run at speeds that far outstrip PCB interconnects, and that MCM substrates will become the rule rather than the exception.

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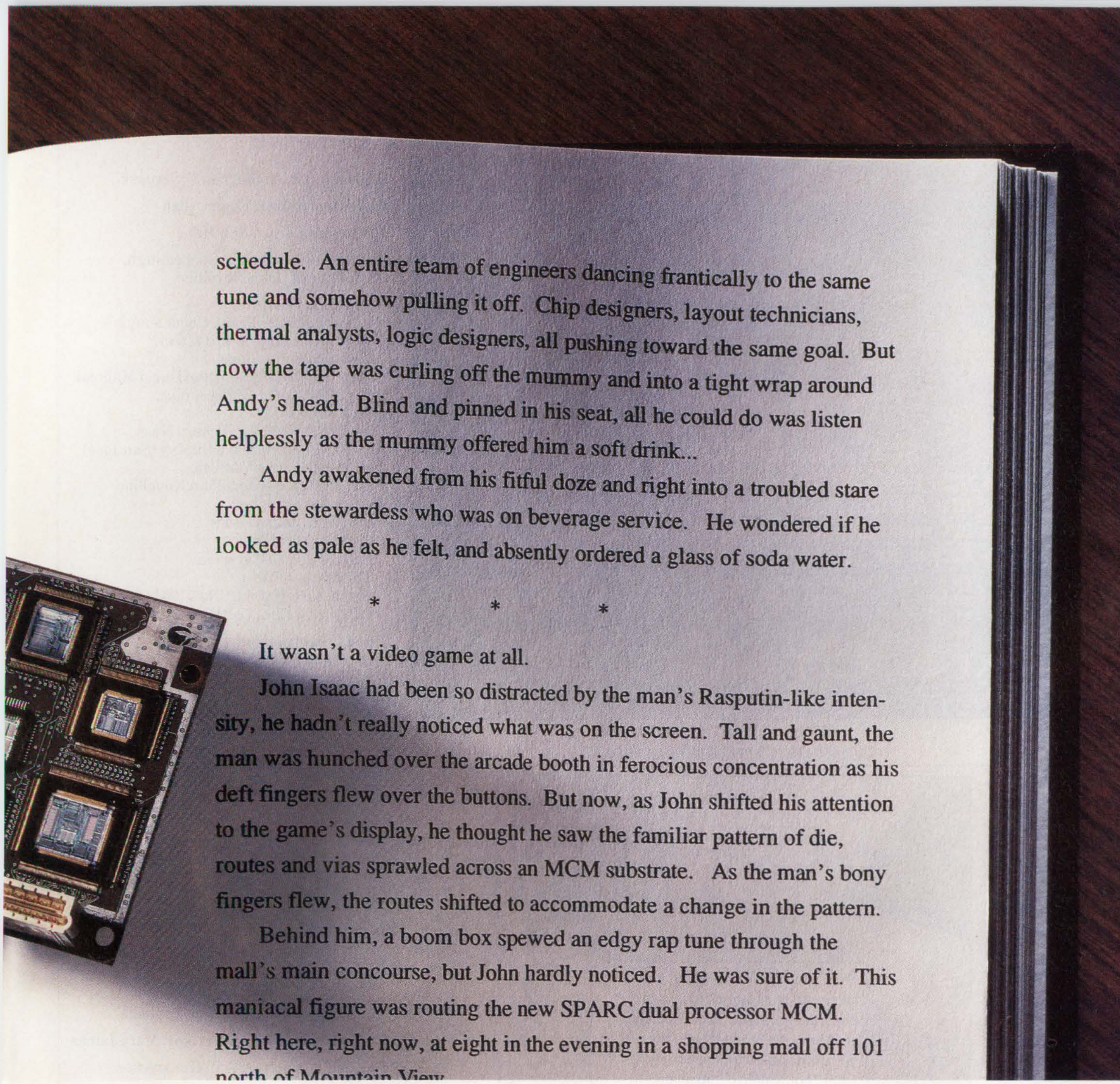

The Stories It Would Tell.

over seventeen hundred PCB-size signal traces in a space just 2.5 by 3.5 inches. And accurately predict junction temperatures to within 1° C.

Our MCM Station® not only met these challenges, it also integrated directly to the project's other tools and data, like signal analysis from Quad Design, a member of our OpenDoor℠ program.

Just five months later, the very first MCM off the line was fully functional. Which proved to both Cypress and their customers that low-cost MCM CPU technology is now a workable reality.

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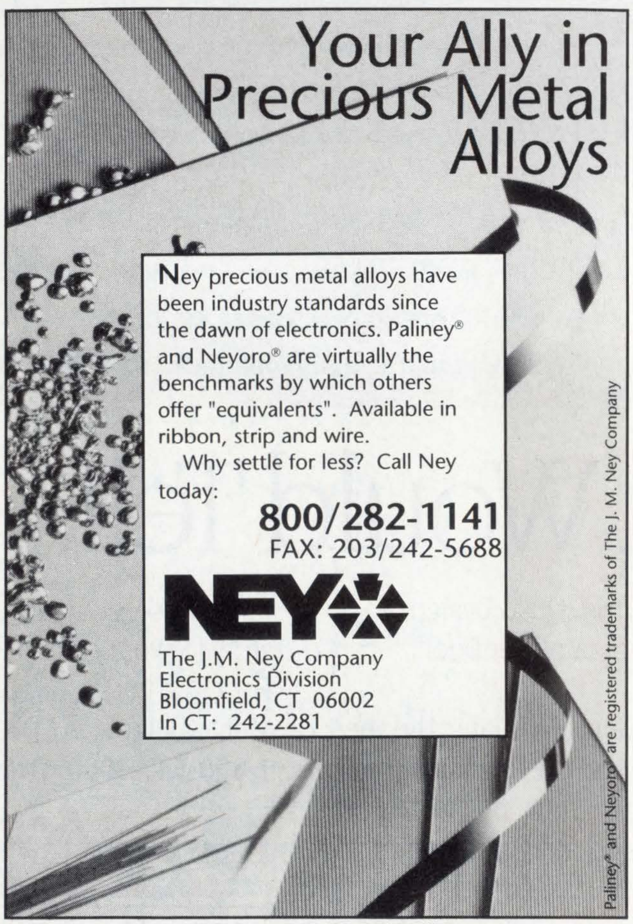

ELECTRONIC DESIGN

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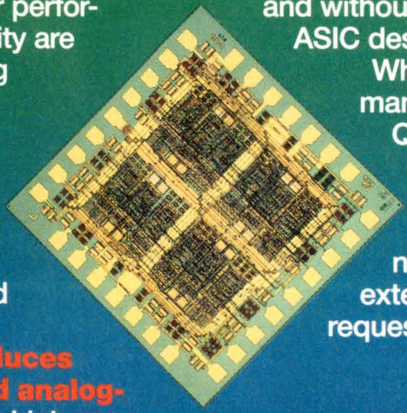
QuickCustom™ ASIC design methods from Tektronix provide convenient access to high performance bipolar technology. There are three effective design methods offered on the SHPi process with 8.5 GHz NPNs, Schottky diodes, JFETs, thin-film resistors, and PNPs. ◆ **QuickChip™ 6** semicustom analog arrays offer the fastest, lowest risk route between concept and finished product. ◆ Higher performance and greater flexibility are possible using the building block approach of **QuickTiles.™** Integration of mixed signal ASICs is fast using the digital cell library. ◆ **Full custom** design provides optimum performance and minimum die size.



Tektronix now introduces the QuickChip™ 7 mixed analog-digital array using a new, higher performance technology, GST-1. This high-density, 12 GHz process is Tektronix' most advanced bipolar technology. Fiber optic telecommunications transceivers and high-speed mixed-signal applications are quickly implemented on the QuickChip 7 semicustom array.

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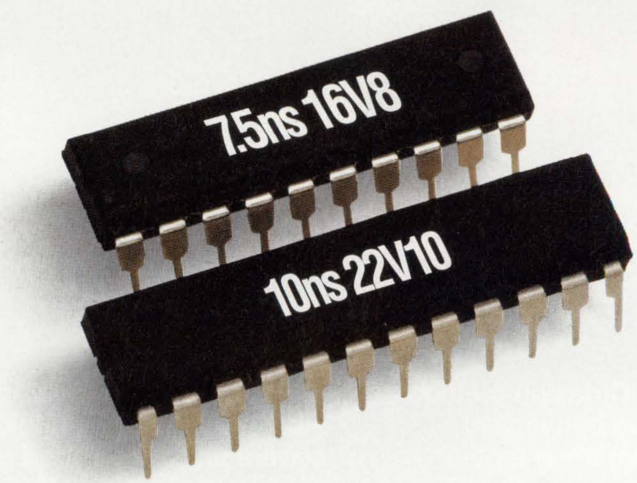

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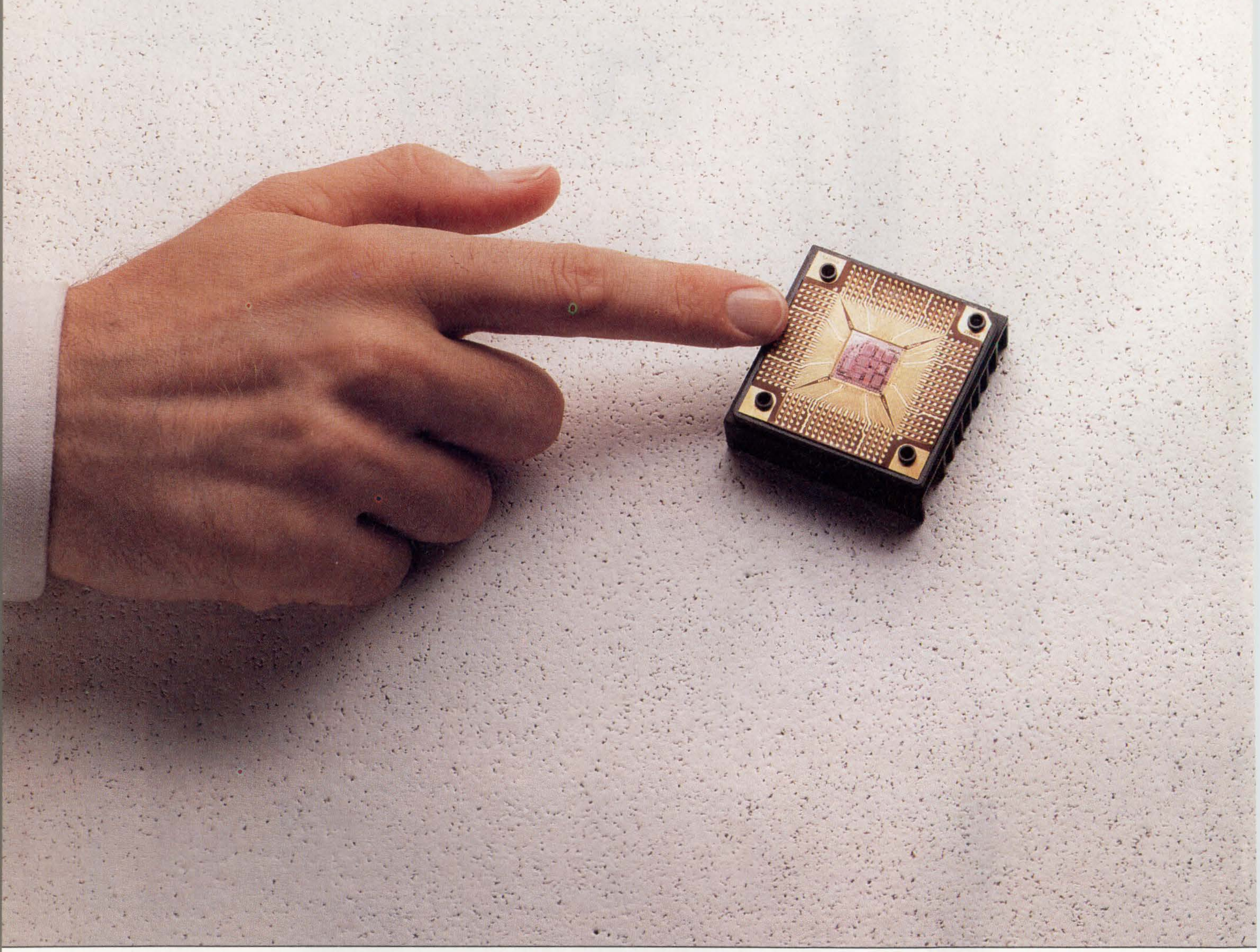
While you've been pushing the limits of digital devices,



HP's specially designed per-pin architecture makes high-performance testing an economic reality.

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Yet, the HP 83000's highly integrated, modular electronics bring you all this performance at a cost that's less than tradi-

BUCKLEY'S TEN QUESTIONS

It's clear that professional organizations like the IEEE should remain politically neutral during this presidential election year. But it does not mean they should stand on the sidelines when important national issues directly related to their professional expertise are being discussed. Instead, they should be leading the charge to open up such issues to serious debate, particularly when questions involve keeping the U.S. competitive in the global marketplace. Thus, it's gratifying to see IEEE president Merrill W. Buckley, Jr., at a news conference in Washington D.C., challenging presidential candidates to reveal their plans to spur growth in the electronics industry and its related technologies.

Buckley poses ten questions for the candidates:

"What will you do to...

...ensure that industrial technology policy is made an integral part of our national economic policy?"

...help industry produce high-quality, marketable products?"

...improve education in order to ensure a technology-literate work force?"

...rejuvenate our declining electronics industry and restore jobs?"

...encourage long-term investments to revitalize the manufacturing base in the United States?"

...enhance Federal support to develop commercially relevant civilian technologies?"

...maximize the commercial return on our investment in defense R&D?"

...ensure that foreign acquisitions of U.S. high technology won't threaten long-term U.S. competitiveness and national security?"

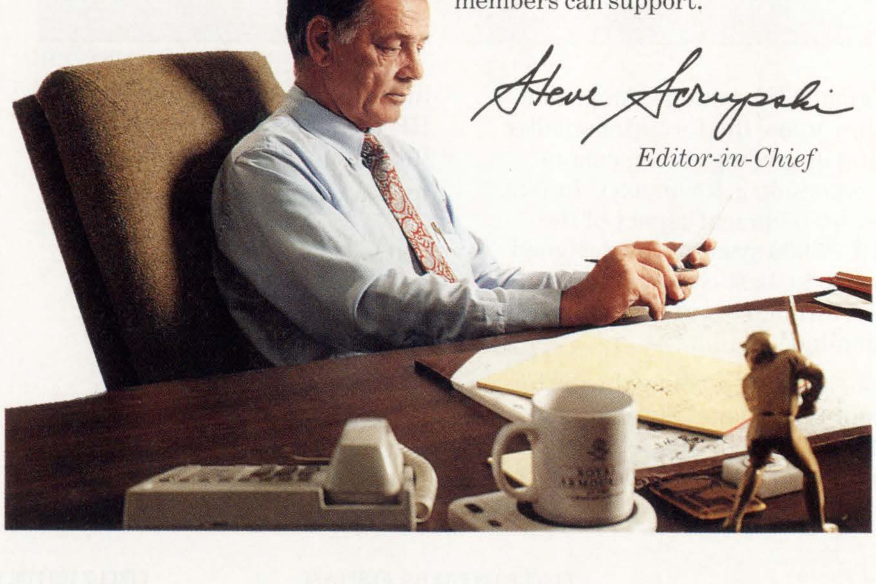
...overhaul U.S. antitrust laws to promote strategic partnerships in U.S. industry?"

...improve the global competitiveness of U.S. products through appropriate trade policies?"

Each question strikes to the core of critical issues facing all of us. Electronic Design congratulates Buckley on assuming this leadership position for the electronics industry, the nation's largest employer. It's about time that our industry become recognized as such by our national policy makers. Since meeting Buckley at a local IEEE meeting here in New Jersey last year, we've been impressed with his grasp of the issues affecting engineers. With these types of actions, he may also begin to heal some of the internal conflicts that have plagued the IEEE between working engineers, company management, and academics.

Buckley's stance on these important issues is a platform all U.S. IEEE members can support.

Steve Scrupski
Editor-in-Chief



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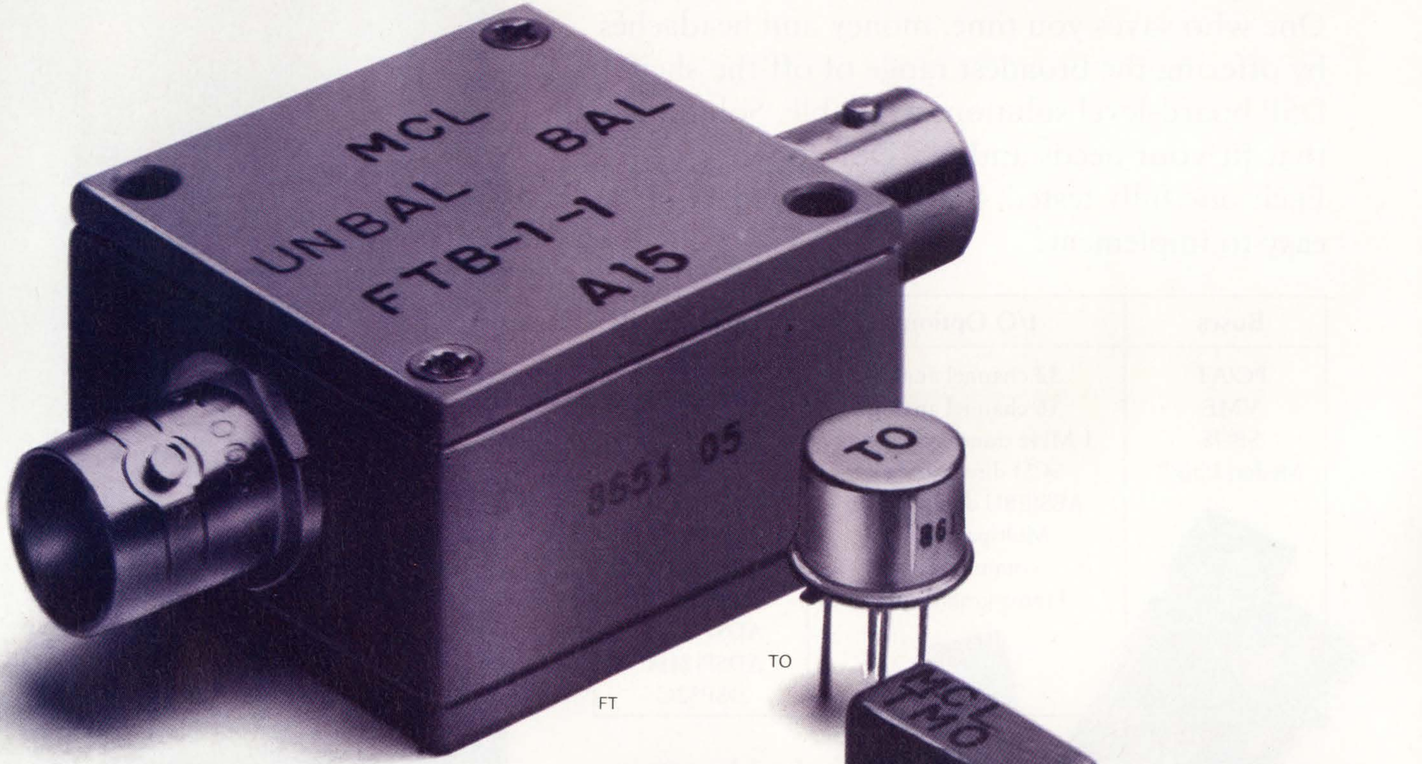

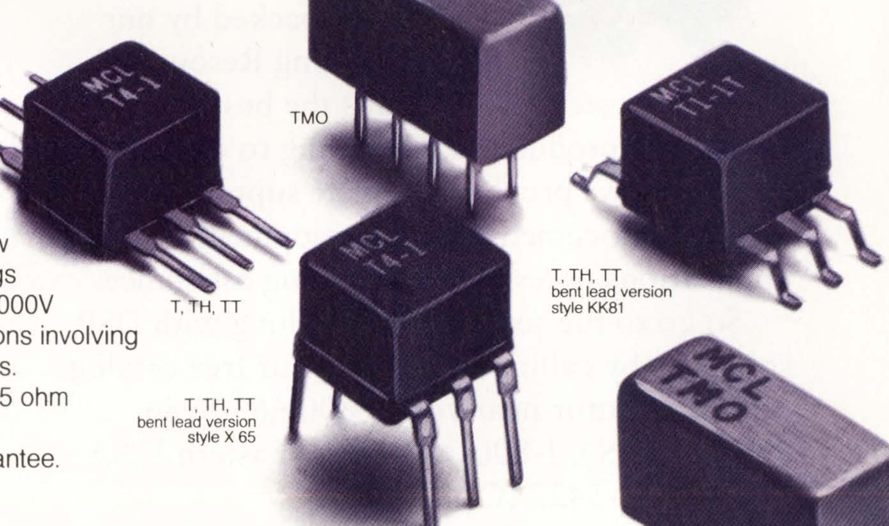

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T1-1	5950-10-128-3745	TMO2.5-6T	5950-01-215-8697
T1-1T	5950-01-153-0668	TMO3-1T	5950-01-168-7512
T2-1	5950-01-106-1218	TMO4-1	5950-01-067-1012
T3-1T	5950-01-153-0298	TMO4-2	5950-01-091-3553
T4-1	5950-01-024-7626	TMO4-6	5950-01-132-8102
T9-1	5950-01-105-8153	TMO5-1T	5950-01-183-0779
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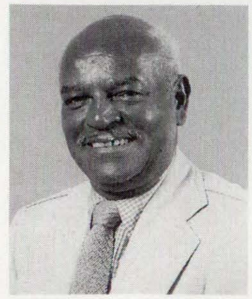
CUTS IN MILITARY OPEN NEW MARKETS



MILT LEONARD
SENIOR EDITOR

Defense-spending cutbacks represent only one side of the coin for suppliers of military-grade integrated circuits. The flip side offers a door to opportunity. This can be deduced from a recent address before the Joint Economic Committee of the U.S. Congress by Don Fuqua, president of the Aerospace Industries Association, the trade association representing the nation's manufacturers of aircraft, missiles, spacecraft, and related components and equipment. Fuqua outlined proposals for maintaining a world-class military while ensuring competitiveness in a global market despite a declining defense budget and a recessed economy.

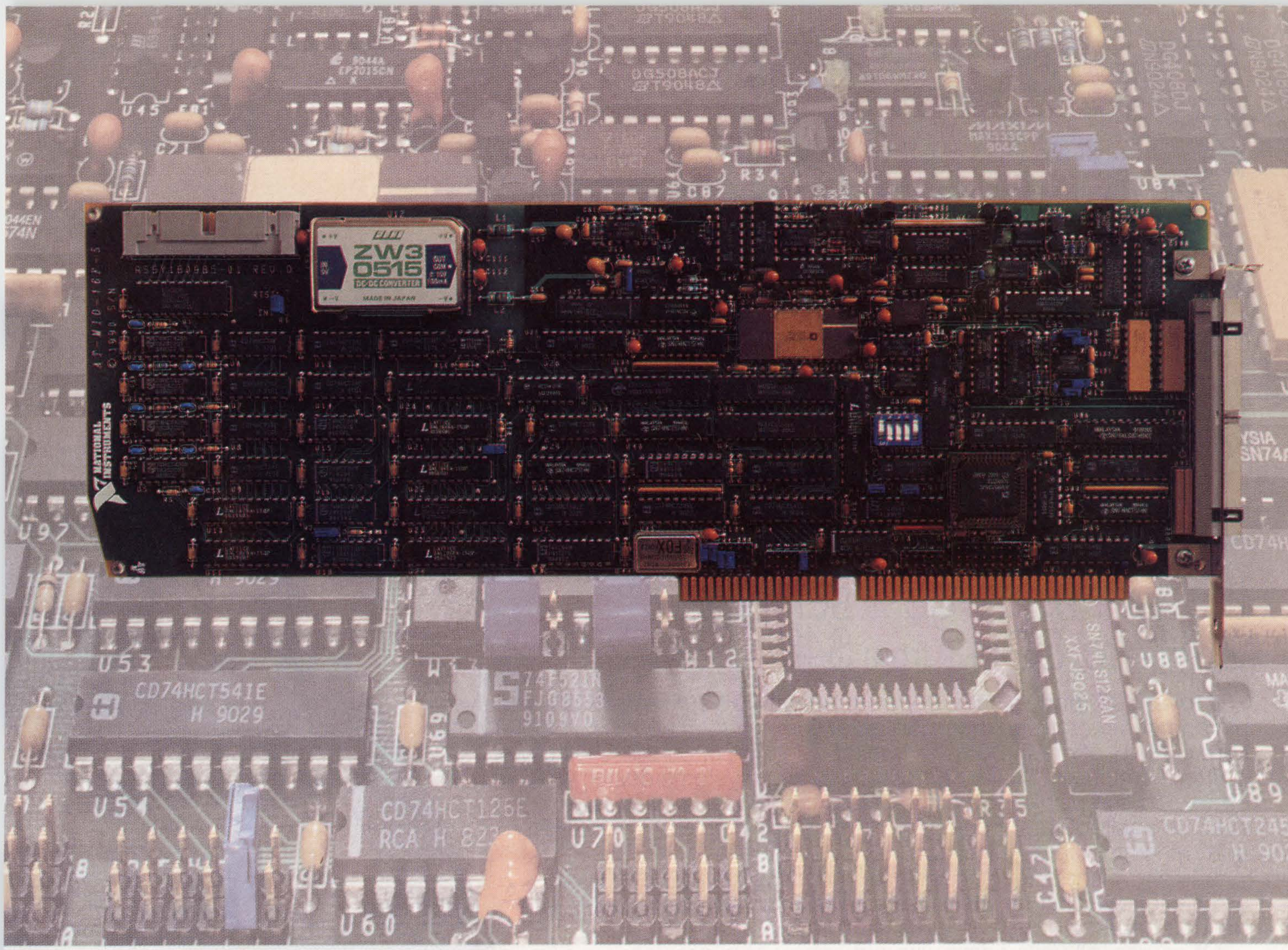
Fuqua also gave a strong boost to continued development of advanced electronic devices. If there's a lesson to be learned from recent military conflicts, he warns, it's that future unanticipated threats to our national security will call for quick response by superior armed forces. He goes on to say that to ensure protection of vital national security interests, government and industry must work to retain a skilled defense-specific labor force, facilities, and critical suppliers, promote technological development, and sustain the ability to surge production when needed. "Of these goals, I believe continued advancement of technology is the most important," says Fuqua.

With government-industry cooperation, much of the support for such technology advances could also come from civilian markets. Take the case of Harris Semiconductor, Melbourne, Fla., the nation's leading supplier of radiation-hardened ICs for military and aerospace applications. Regardless of the shrinking military budget, Harris continues to hone its rad-hard expertise in support of new programs mandated by the Strategic Defense Initiative programs and upgraded existing systems. Moreover, two years ago, foreseeing a weakening military market, Harris established its Space Products Operations to augment its military business by applying its rad-hard technology base to products for nonmilitary markets.

Nonmilitary opportunities for rad-hard ICs include U.S., European, and Japanese communications satellites and space stations. A report available from BIS Strategic Decisions, Woburn, Mass., forecasts an average annual growth rate of 50% for Global Positioning System (GPS) satellites alone, with the U.S. market reaching $1-2 billion by 1995. Other opportunities for high-rel ICs include video and image processing, high-speed communications, test and measurement equipment, and scientific and medical equipment.

Ongoing R&D at Harris is projected to produce the industry's first 64-kbit rad-hard Class S PROM by early 1993. The memory is fabricated with a nichrome-fused CMOS process built on a sapphire-insulated substrate to get a 1-Mrad radiation hardness and a single-event-upset (SEU) immunity below 10^{-10} errors/bit/day in a worst-case environment. High SEU immunity from solar flares is more critical than radiation hardness for space applications.

Furthermore, Harris and Xilinx Inc., San Jose, Calif., have agreed to produce the industry's first rad-hard Class-S field-programmable gate array fabricated with a CMOS/SOS (silicon-on-sapphire) process developed for radiation environments. This chip is particularly attractive for on-the-fly reprogrammability of satellites in orbit. Because memory chips constitute the largest IC content of a space system, designers continually search for ways to increase speed, as well as reduce parts count and weight. Harris' 0.8-μm CMOS/SOI (silicon-on-insulator) SIMOX (silicon implant with oxygen) technology, which has produced a 25-ns 256-kbit rad-hard SRAM, will be applied to future ASICs and other standard digital ICs like microprocessors and logic. "These and other rad-hard, high-rel products are expected to comprise 70% of our sales to nonmilitary markets," says Scott Moody, director of Harris' Space Products Operations.



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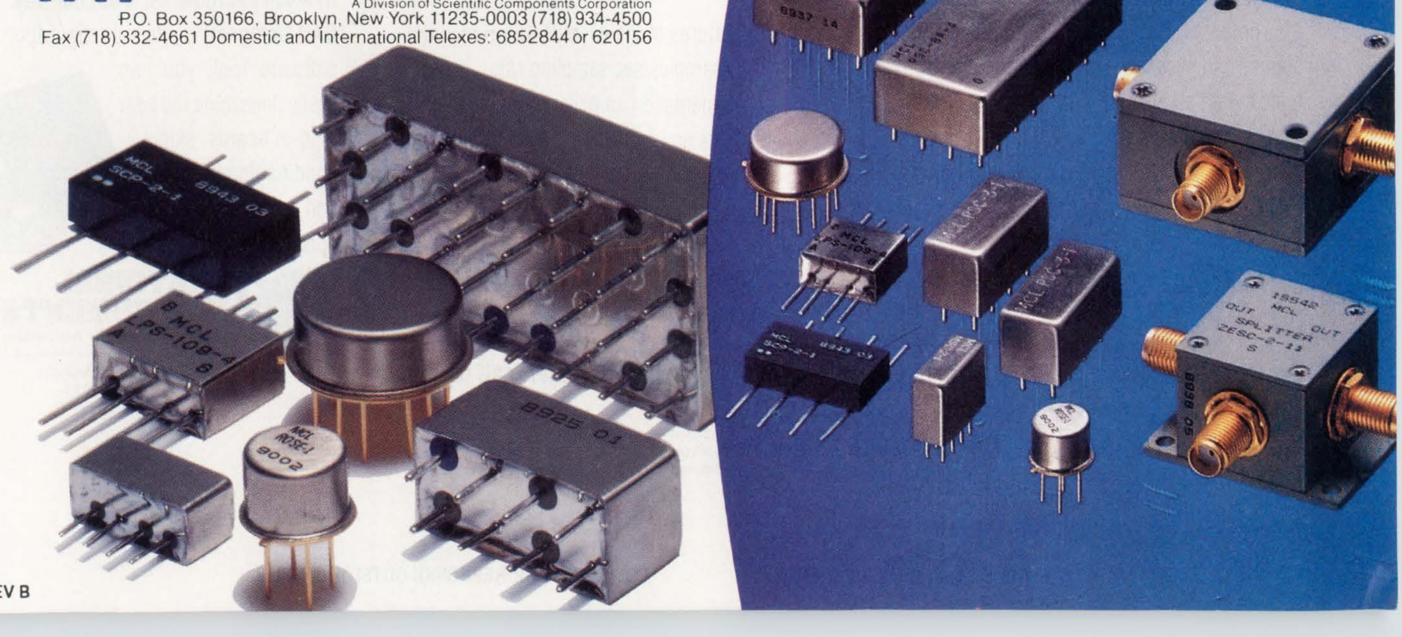

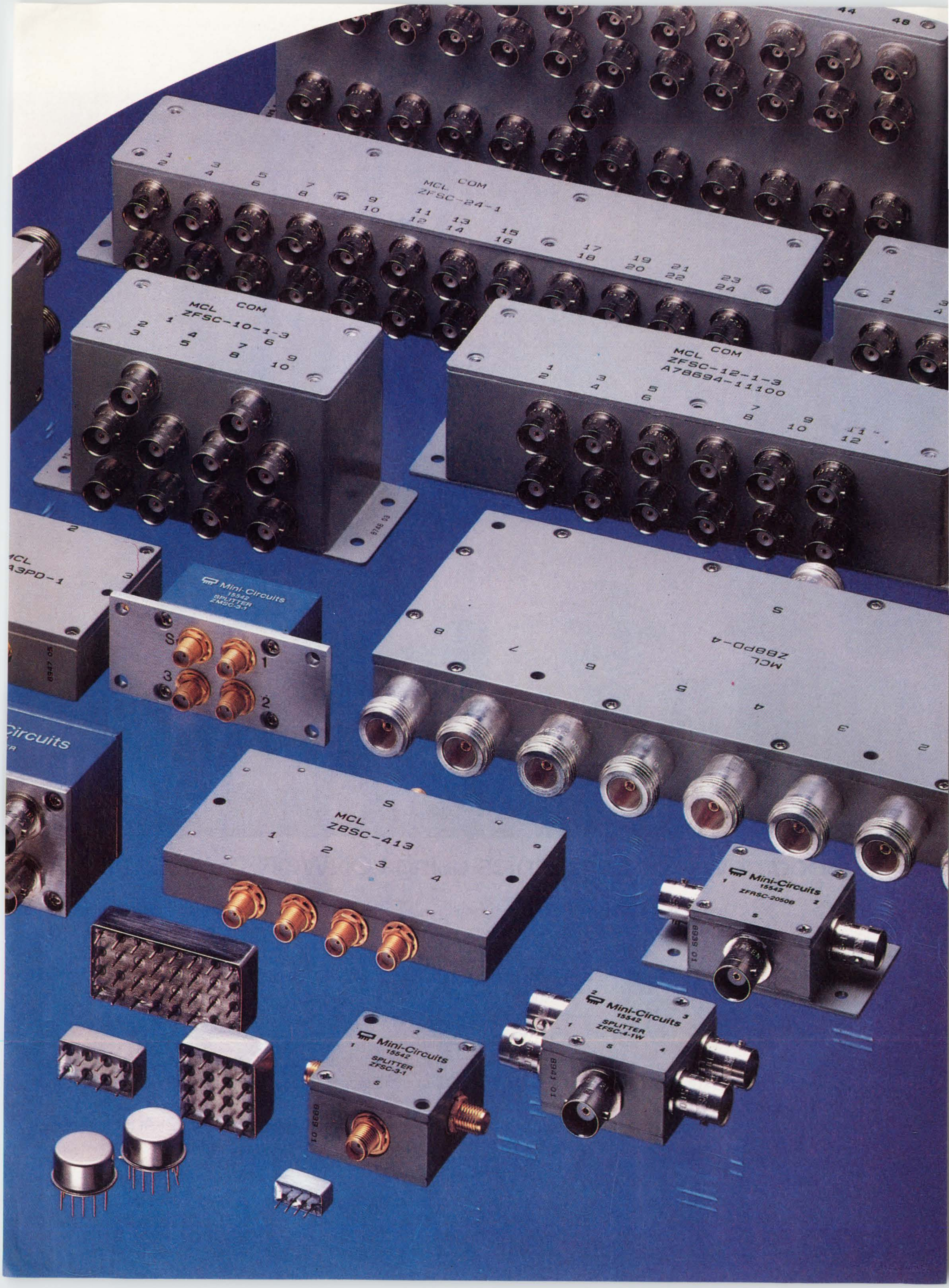

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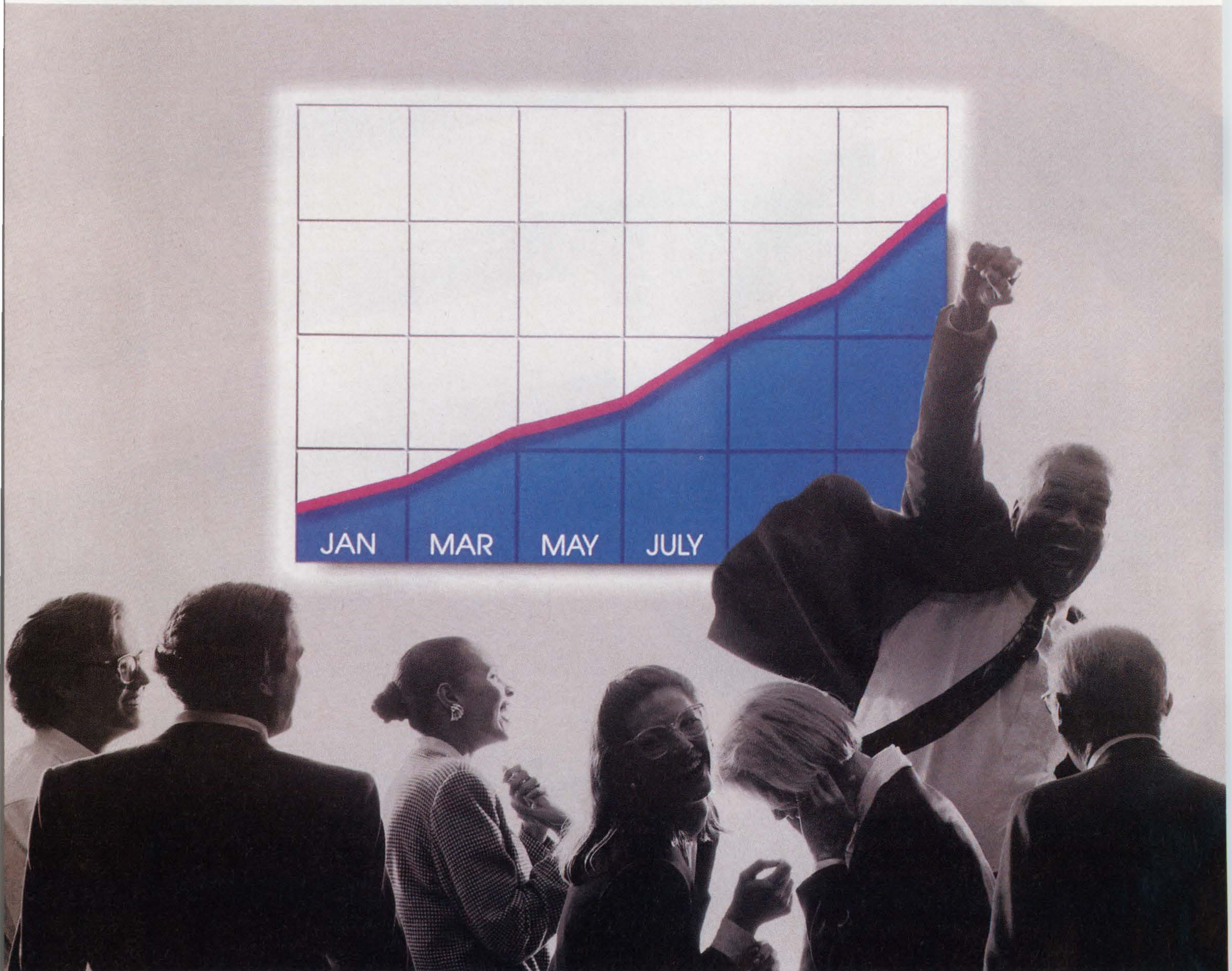
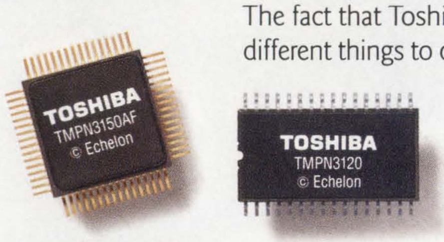


Good news for companies using LONWORKS technology.



The fact that Toshiba is the first company to ship the NEURON 3150™ CHIP in production quantities means different things to different companies.

For companies already using LONWORKS™ technology and tools from Echelon,® it means they can get their new generation of intelligent products to market very quickly.

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LONWORKS technology lets you build control networks into products and environments for intelligent distributed control applications. Quickly and inexpensively. To produce products that are able to interoperate and perform more functions, more efficiently.

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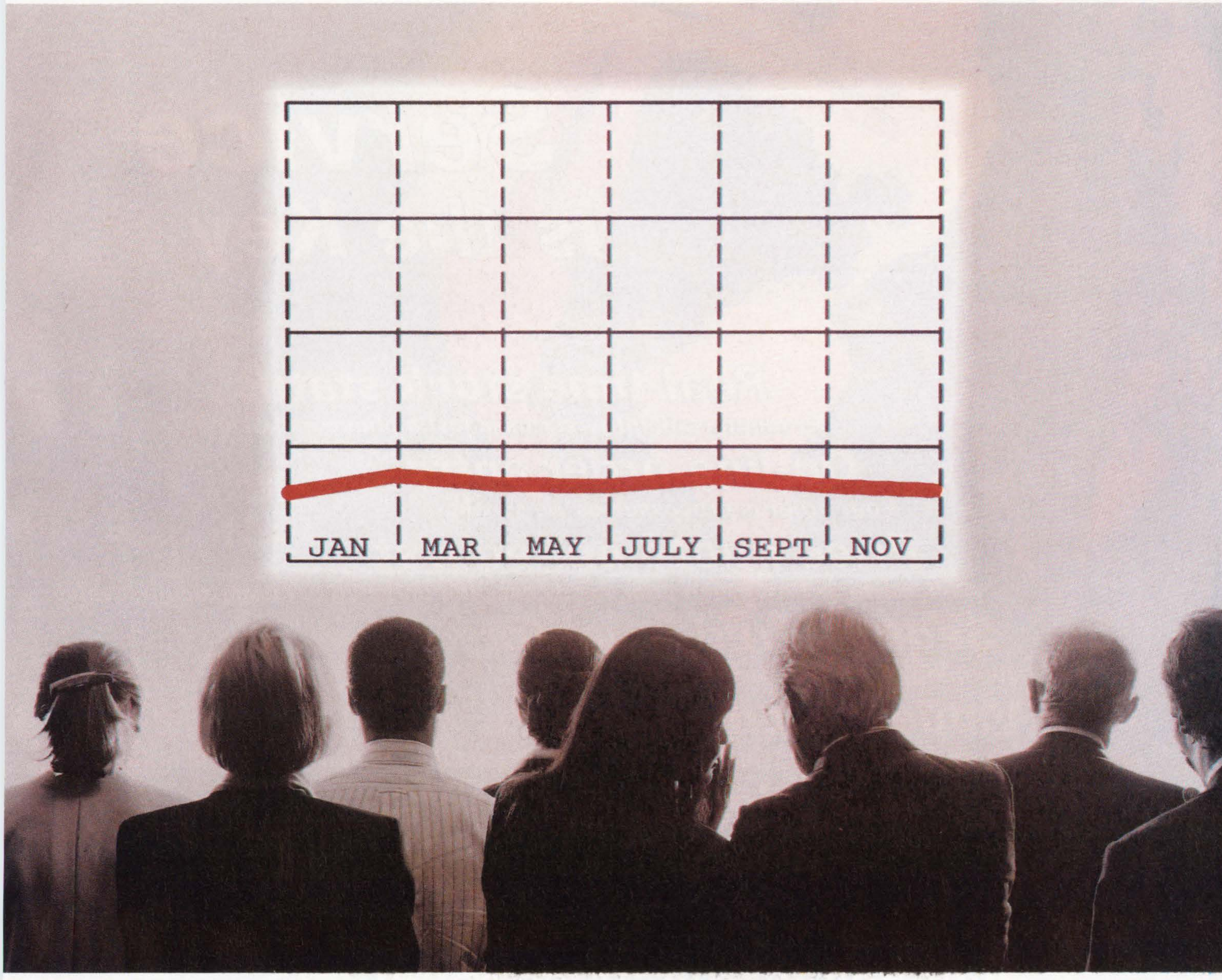

Bad news for companies that aren't.

and the NEURON 3150 CHIP with external memory support for more complex functions. Each node also contains an interface to communicate with other nodes over a wide range of standard media using the common LONTALK™ protocol. And to design those LONWORKS nodes into your products quickly and inexpensively, there's the PC-based LONBUILDER™ 2 Developer's Workbench.

More than 200 companies, many of them on the Fortune 100 list, are using LONBUILDER 2 Developer's Workbenches right now to design and develop more intelligent, more competitive products.

If you're one of them, congratulations. With Toshiba shipping NEURON CHIPS in quantity, you're that much closer to bringing your new products to market.

And if you're not already using LONWORKS technology and tools, don't give up. Toshiba and Echelon are ready to help you get started. Call the LONWORKS Hotline at **1-800-879-7566**. Fax **1-415-856-6154**. (From outside the U.S., please fax.) Or write Echelon Corporation, 4015 Miranda Ave., Palo Alto, CA 94304.

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IBM's MCM Dielectric Won't React With Copper

An advanced polyimide multichip-module dielectric developed by IBM Corp. offers compatibility with copper metallurgy. The material is based on an ester technology, which eliminates the acid content that causes most other polyimide precursors to interact with copper. As a result, users won't need a passivation coating on the copper module substrate. Moreover, the material's isomer ratio permits the manufacturing of high-solids formulations, yielding coatings up to 20 μm thick. Ordinary polyimide dielectrics must often be spun on twice to achieve thick coatings. The dielectric, developed for use in ES9000 Series mainframe computers, is to be marketed by OCG Microelectronic Materials Inc., West Paterson, N.J., under the name Probimer 600. OCG had produced the material for IBM since 1989. Call OCG at (201) 977-6011 for more information. *DM*

Video-Telecom Link To Benefit Community

Subject to approval by the California Public Utilities Commission and the Federal Communications Commission, Pacific Bell will link a fiber-optic telecommunications network and cable TV system to provide a new California community with services such as telecommuting, two-way educational programs, and video teleconferencing. The model development is located about 15 miles north of Sacramento in South Sutter County. In the first phase of the community's development, Pacific Bell will install a fiber-to-the-curb network for delivering digital light-based telephone transmissions to pedestals outside homes and offices. After conversion from light to electricity, the signals will travel the remaining distance over copper lines. South Sutter Cable Inc. will then build a parallel cable-TV system composed of fiber-optic lines feeding video into high-capacity metal cables. When the two networks are linked, customers can interact with a televised program through the telecommunications network. Network construction could begin as early as 1993. *ML*

Thin-Film Heads Push Tape-Drive Capacities

Thin-film heads, embedded servos, and higher-Oersted gamma ferric-oxide media should allow 1/4-in. tape-drive manufacturers to build 3-Gbyte 3-1/2-in. and 10-Gbyte 5-1/4-in. drives. With data compression, these capacities will double to 6 and 20 Gbytes, respectively. The heads, designed by Applied Magnetics Corp., Goleta, Calif., are four-channel devices that use inductive write and magneto-resistive read elements. Three channels are used in a read-write-read pattern and one channel is dedicated to reading servo-positioning information on the tape for accurate head positioning with the 144-track format. The heads support dual-channel read and write operations with a sustained transfer rate of 1.5 Mbytes/s. *RN*

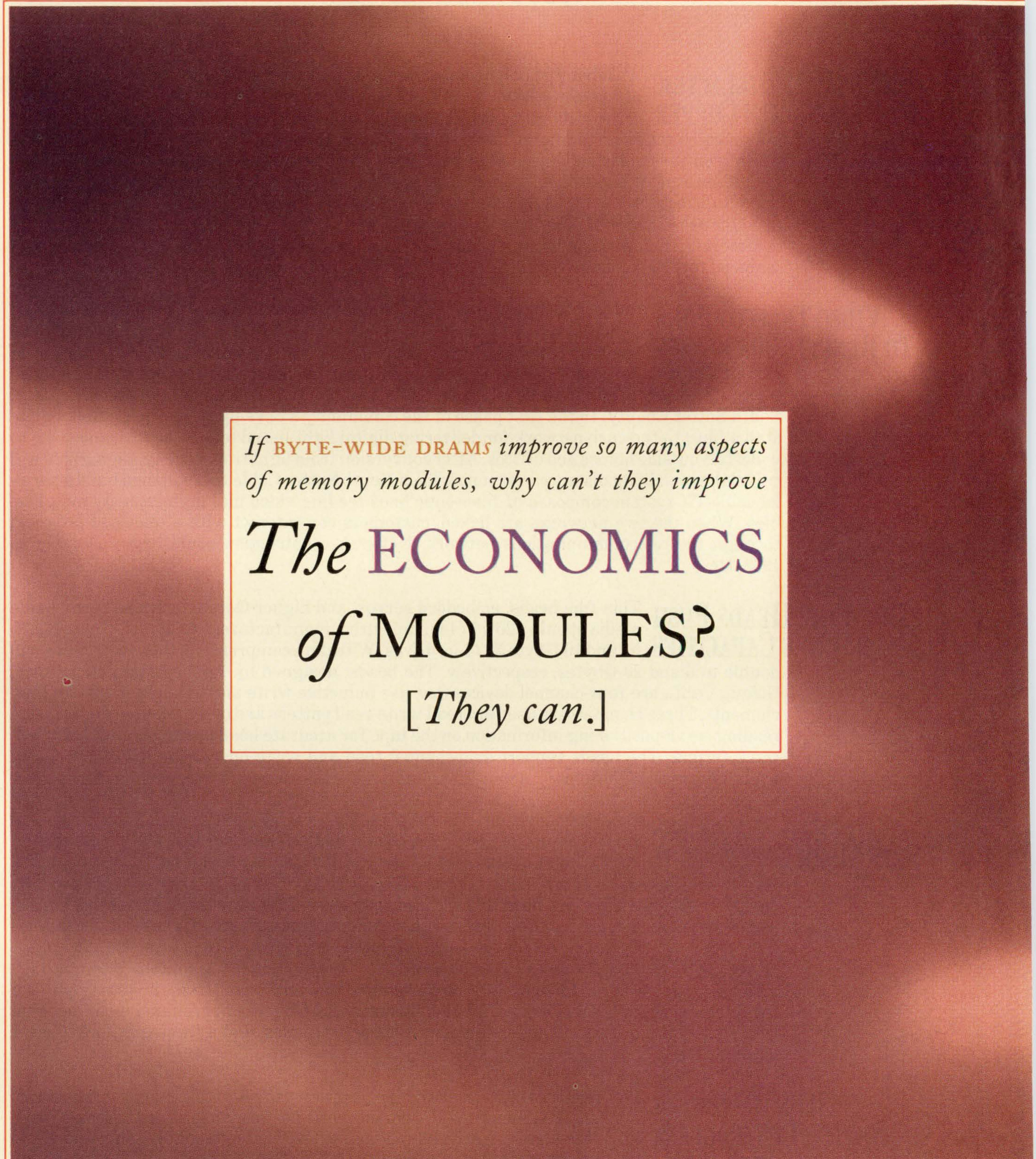
Optical-Fiber Lens Sees More Laser Light

Conventional hemispherical microlenses fabricated on the ends of an optical fiber capture just 50% of a laser's emitted energy. However, scientists at AT&T Bell Laboratories, Murray Hill, N.J., have designed experimental fiber microlenses that capture up to 90% of a laser's light. The lenses are micromachined by moving a spinning fiber in a narrowly focused laser beam that shapes the lenses by simultaneously cutting and heating the end of the fiber under computer control. The result is an aberration-free, aspherical hyperbolic lens with an increased effective aperture size. Prototype lenses have exhibited 2.9-terabit-kilometer capacity for a system using solitons (a terabit-kilometer is a measure used to compare lightwave-system performance). Experiments employing the fiber lenses involved all-optical demultiplexing at 2.5 Gbits/s, an erbium-doped fiber ring laser, gap solitons in aluminum-gallium-arsenide wave guides, and a frequency-locked laser package. *ML*

BiCMOS Builds Better Controllers

By moving from a standard-bipolar process to biCMOS, Unitrode Integrated Circuits, Merrimack, N.H., increased the performance of its UC3842-45 family of standard pulse-width-modulated switching-regulator controllers. The availability of MOS transistors for the new pin-for-pin UCC3802-5 family simultaneously reduced operating-current drain and increased packing density. A lower current drain dramatically raises the efficiency of small (under 50-W) supplies, while a higher packing density raises chip complexity, resulting in the addition of several new features. The startup current was reduced an order of magnitude to just 100 μA. Now, a 1/8-W series resistor from the rectified ac line can replace a several-watt device to drive the IC at power-up. Furthermore, the operating quiescent current was reduced to just 500 μA from over 10 mA.

In many applications, the lower operating current eliminates the need for a bootstrap winding on the transformer due to its attendant rectifier and filter capacitor. In addition, with the low startup current, the typical off-chip 10-μF soft-start capacitor can be replaced with an on-



Byte-wide DRAMS in memory modules. When you compare a 4-meg byte-wide with the normal combination of 1-megs and 256K's, you find that one chip can replace six.

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Because the single byte-wide costs less than the six chips it replaces.

chip MOS device, bringing the complete soft-start circuit on-chip. The full-cycle soft-start circuit also provides a restart delay or "hiccup" type operation, preventing "fast soft-start" oscillations when a fault occurs. Moreover, the PWM circuits are blanked for the first 100 ns of each pulse to prevent the always-present leading-edge spike from shutting the power switch off. Finally, the totem-pole outputs supply an active-low condition. That is, the output drive circuit is at a very low impedance to ground when it's holding the FET switch off. In quantities of 1000, the commercial grades of the 1-MHz controller (the UCC3802-3805) go for $2.08 each. For additional information, call Al Fuller at (603) 429-8595. *FG*

CAD VENDOR HELPS EDUCATE EASTERN EUROPE

As part of its participation in a program aimed at sharing technology research with Eastern European engineers, Technology Modeling Associates (TMA) Inc., Palo Alto, Calif., will contribute its technology computer-aided-design (TCAD) software to a Romanian university. TMA will also send company specialists to lead a class on Western TCAD developments, and partake in a researcher-exchange program with Eastern European companies. The program is part of the Trans-European Mobility Scheme for University Studies (Tempus) project, which is designed to bring advanced semiconductor-related education and training from Western Europe to partners in Eastern European nations. Tempus partners include leading European academic and government research groups who plan to develop an up-to-date curriculum, focusing on electron devices, at Romania's Polytechnical Institute of Bucharest, as well as build a supporting a state-of-the-art laboratory. Two TMA researchers will teach a course called "Curriculum development in the field of analysis and modeling of VLSI structures." The ongoing course is scheduled from Sept. 1992 through Aug. 1994. For more information on the Tempus project, call Dr. Marcel D. Profirescu at the Polytechnical Institute of Bucharest, 40-0-317800, ext. 334 or 122. *LM*

U.S. NAVY DRAFTS FDDI FOR SIMULATED SCENARIOS

An FDDI controller board developed by Vista Controls Corp., Valencia, Calif., has been installed at the U.S. Navy's Coastal Systems Station at Panama City, Fla., to link computers that assess the performance of underwater vessels in various marine environments. The Coastal Systems Station required a high-speed data link between two Encore Concept /32 computers located in separate laboratories. One computer simulates ocean acoustical characteristics. The other computer, located in a different laboratory, runs various scenarios by inserting simulated underwater vehicles into the ocean environment created by the first computer. Real-time data is then transmitted between the laboratories over the 100-Mbit/s FDDI network. Built around the Supernet 2 chip set designed by Advanced Micro Devices, Sunnyvale, Calif., and fitting into a standard 6U VME slot, Vista Controls' VC-FDDI-SEL controller board provides over 70 Mbits/s of throughput and under a 25-ms start for I/O latency. *ML*

ELECTROLYSIS TECHNIQUE IMPROVES MICROMACHINING

Researchers at Sandia National Laboratories, Albuquerque, N. M., developed an improved process for uniformly etching micromachined silicon structures. The process involves the electrolysis of silicon in hydrofluoric acid to make a porous, very thin layer of silicon on top of a silicon wafer. This intermediate porous phase enables silicon to be etched away with no more than a 0.03% variance in results, according to Sandia's Terry Guilinger, a member of the research team that developed the process. Because the etching rate of silicon is directly proportional to the current passed in the electrochemical cell, the depth of the porous silicon can be regulated by controlling the charge through the electrochemical cell. After being immersed in the acid, the silicon wafer is removed and the porous cell is etched by bathing it in a hydroxide solution at room temperature. A mirror, rather than matte, finish is achieved due to the uniformity of pore depths. Sandia claims that the new method is completely compatible with standard wafer-fabrication procedures. A patent on this process has been issued to the U.S. Department of Energy, which operates Sandia Laboratories. The DOE has also filed a patent application for a humidity sensor that's also fabricated by the new process. The sensor is to be used inside IC packages. For more information, contact Sandia's Terry Guilinger at (505) 845-9043. *RA*

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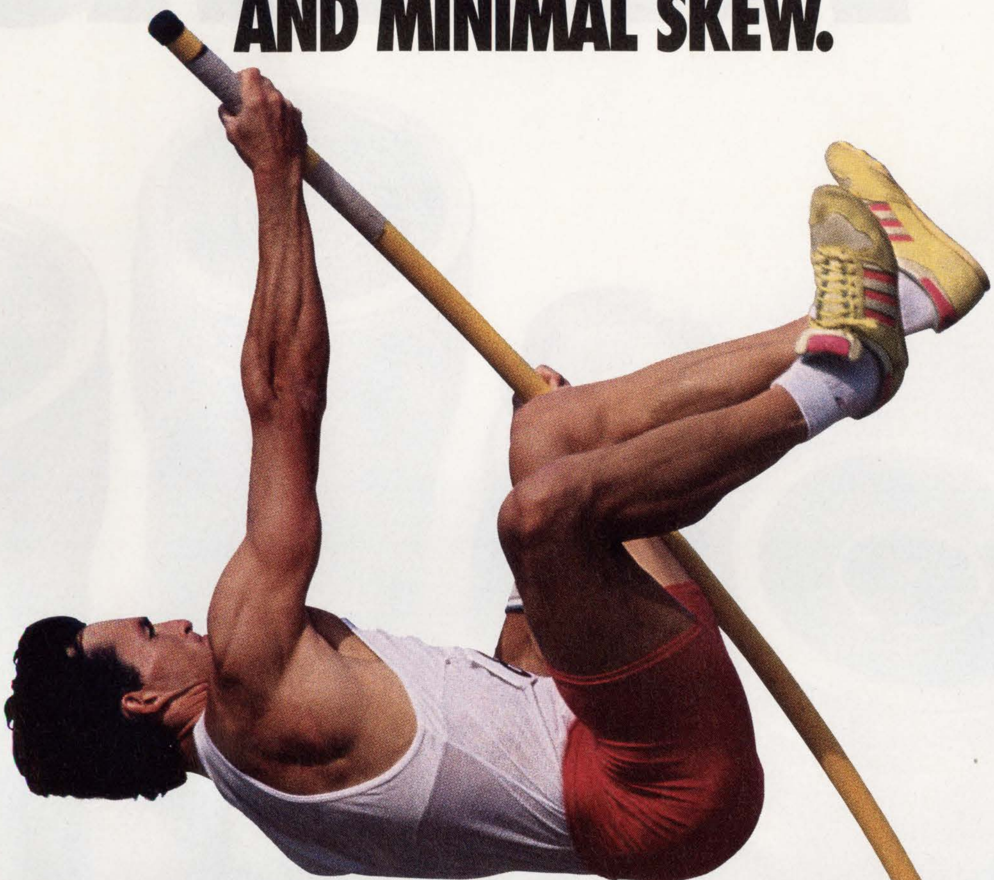

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GA 1000	20–80 MHz	6 individually configurable	20 – 160 MHz	Individually configurable

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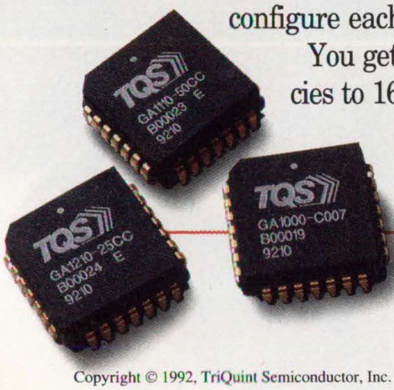

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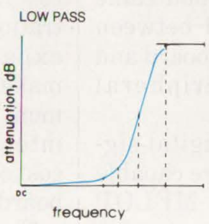


low pass, Plug-in, dc to 1200MHz

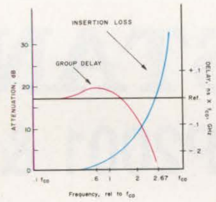
Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB	Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB
PLP-5	DC-5	8-10	10-200	PLP-250	DC-225	320-400	400-1200
PLP-10.7	DC-11	19-24	24-200	PLP-300	DC-270	410-550	550-1200
PLP-21.4	DC-22	32-41	41-200	PLP-450	DC-400	580-750	750-1800
PLP-30	DC-32	47-61	61-200	PLP-550	DC-520	750-920	920-2000
PLP-50	DC-48	70-90	90-200	PLP-600	DC-680	840-1120	1120-2000
PLP-70	DC-60	90-117	117-300	PLP-750	DC-700	1000-1300	1300-2000
PLP-90	DC-81	121-137	167-400	PLP-800	DC-720	1080-1400	1400-2000
PLP-100	DC-98	146-189	189-400	PLP-850	DC-760	1100-1400	1400-2000
PLP-150	DC-140	210-300	300-600	PLP-1000	DC-900	1340-1750	1750-2000
PLP-200	DC-190	290-390	390-800	PLP-1200	DC-1000	1620-2100	2100-2500

Price, (1-9 qty), all models: plug-in $14.95, BNC $32.95, SMA $34.95, Type N $35.95

Surface-mount, dc to 570MHz

Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB	Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB
SCLF-21.4	DC-22	32-41	41-200	SCLF-190	DC-190	290-390	390-800
SCLF-30	DC-30	47-61	61-200	SCLF-380	DC-380	580-750	750-1800
SCLF-45	DC-45	70-90	90-200	SCLF-420	DC-420	750-920	920-2000
SCLF-135	DC-135	210-300	300-600				

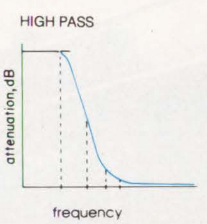
Price, (1-9 qty), all models: $11.45



Flat Time Delay, dc to 1870MHz

Model No.	Passband MHz loss < 1.2dB	Stopband MHz loss > 10dB	Stopband MHz loss > 20dB	VSWR Freq. Range, DC thru 0.2fco $\bar{X}$	VSWR Freq. Range, DC thru 0.6fco $\bar{X}$	Group Delay Variations, ns Freq. Range, DC thru fco $\bar{X}$	Group Delay Variations, ns 2fco $\bar{X}$	Group Delay Variations, ns 2.67fco $\bar{X}$
PBLP-39	DC-23	78-117	117	1.3:1	2.3:1	0.7	4.0	5.0
PBLP-117	DC-65	234-312	312	1.3:1	2.4:1	0.35	1.4	1.9
PBLP-156	DC-94	312-416	416	0.3:1	1.1:1	0.3	1.1	1.5
PBLP-200	DC-120	400-534	534	1.6:1	1.9:1	0.4	1.3	1.6
PBLP-300	DC-180	600-801	801	1.25:1	2.2:1	0.2	0.6	0.8
PBLP-467	DC-280	934-1246	1246	1.25:1	2.2:1	0.15	0.4	0.55
▲BLP-933	DC-560	1866-2490	2490	1.3:1	2.2:1	0.09	0.2	0.28
▲BLP-1870	DC-850	3740-6000	5000	1.45:1	2.9:1	0.05	0.1	0.15

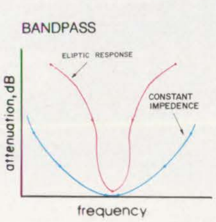
Price, (1-9 qty), all models: plug-in $19.95, BNC $36.95, SMA $38.95, Type N $39.95
NOTE: ▲: -933 and -1870 only with connectors, at additional $2 above other connector models.



high pass, Plug-in, 27.5 to 2200MHz

Model No.	Stopband MHz loss < 40dB	Stopband MHz loss < 20dB	Passband MHz loss < 1dB	VSWR Pass-band Typ.	Model No.	Stopband MHz loss < 40dB	Stopband MHz loss < 20dB	Passband MHz loss < 1dB	VSWR Pass-band Typ.
PHP-25	DC-13	13-19	27.5-200	1.8:1	PHP-400	DC-210	210-290	395-1600	1.7:1
PHP-50	DC-20	20-26	41-200	1.5:1	PHP-500	DC-280	280-365	500-1600	1.8:1
PHP-100	DC-40	40-55	90-400	1.8:1	PHP-600	DC-350	350-440	600-1600	2.0:1
PHP-150	DC-70	70-95	133-600	1.8:1	PHP-700	DC-400	400-520	700-1800	1.6:1
PHP-175	DC-70	70-105	160-800	1.5:1	PHP-800	DC-445	445-570	780-2000	2.1:1
PHP-200	DC-90	90-116	185-800	1.6:1	PHP-900	DC-520	520-660	910-2100	1.8:1
PHP-250	DC-100	100-150	225-1200	1.3:1	PHP-1000	DC-550	550-720	1000-2200	1.9:1
PHP-300	DC-145	145-170	290-1200	1.7:1					

Price, (1-9 qty), all models: plug-in $14.95, BNC $36.95, SMA $38.95, Type N $39.95



bandpass, Elliptic Response, 10.7 to 70MHz

Model No.	Center Freq. (MHz)	Passband I.L. 1.5 dB Max. (MHz)	3 dB Bandwidth Typ. (MHz)	Stopbands I.L. > 20dB at MHz	Stopbands I.L. > 35dB at MHz
PBP-10.7	10.7	9.6-11.5	8.9-12.7	7.5 & 15	0.6 & 50-1000
PBP-21.4	21.4	19.2-23.6	17.9-25.3	15.5 & 29	3.0 & 80-1000
PBP-30	30.0	27.0-33.0	25-35	22 & 40	3.2 & 99-1000
PBP-60	60.0	55.0-67.0	49.5-70.5	44 & 79	4.6 & 190-1000
PBP-70	70.0	63.0-77.0	68.0-82.0	51 & 94	6.0 & 193-1000

Price, (1-9 qty), all models: plug-in $18.95,
BNC $40.95, SMA $42.95, Type N $43.95

Constant Impedance, 21.4 to 70MHz

Model No.	Center Freq. MHz	Passband MHz loss < 1dB	Stopband loss > 20dB at MHz	VSWR 1.3:1 Total Band MHz
PIF-21.4	21.4	18-25	1.3 & 150	DC-220
PIF-30	30	25-35	1.9 & 210	DC-330
PIF-40	42	35-49	2.6 & 300	DC-400
PIF-50	50	41-58	3.1 & 350	DC-440
PIF-60	60	50-70	3.8 & 400	DC-500
PIF-70	70	58-82	4.4 & 490	DC-550

Price, (1-9 qty), all models: plug-in $14.95,
BNC $36.95, SMA $38.95, Type N $39.95

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F132-2 REV. A

Parallel Bus Connects PC-Hosted DSP And Data-Acquisition Boards At 6 MSamples/s

Because of their standardized bus architecture, IBM-compatible personal computers make ideal hosts for digital-signal-processing (DSP) systems that perform image processing; noise and vibration analysis; and digital-audio, speech and signal processing. In such systems, a DSP board might sit next to a standard data-acquisition board and rely on the PC to transfer blocks of data between the two boards.

However, according to Andy Christofi, marketing director of Loughborough Sound Images Ltd., Loughborough, U.K., the PC industry-standard-architecture (ISA) bus creates a major roadblock to attaining efficient real-time PC-based DSP systems. "Relying on the PC's bus to transfer data is almost guaranteed to underutilize both the DSP and the data-acquisition boards," he asserts.

To accelerate data transfers, Loughborough Sound Images has come up with a high-speed parallel bus architecture that can be used to connect PC-hosted DSP and data-acquisition boards to each other. Christofi describes it as a "lean, mean interface that gets the job of transferring data done with a minimum of fuss." He dubs it DSPLINK, and expects the interface to become a de-facto standard.

This "lean and mean" interface is no slouch, either. Christofi claims it can transfer data at up to 6 Msamples/s and can support a single master with multiple slaves. It's a strobed parallel-I/O port with address decoding for 16 registers. Physically, the bus is implemented as a 50-conductor ribbon cable that's connected between the DSP master board and the slave peripheral boards.

"Typically, digital-signal processors are capable of working at MFLOP speeds, while data-acquisition boards might be sampling several channels simultaneously at rates of several-hundred kHz," he says. The limited speed at which PCs can transfer data across the ISA bus, and the need to wait for the bus to be free, combine to form a severe bottleneck. Time that could be spent processing or analyzing real-time signals is wasted waiting for the bus to transfer data.

The idea is to stick strictly to the signals needed to transfer parallel digital data, and ignore "luxuries" like multimaster arbitration and fast memory-expansion issues. This makes it easier to implement and debug a custom interface and keeps the cost of standard peripheral boards as low as possible.

The signal set is defined in two subsets called "minimum signal subset" and "additional signals." As a result, designers can use DSPLINK as a basic interface for standard off-the-shelf peripheral boards, or as a more sophisticated custom interface.

All DSPLINK off-the-shelf slave peripheral boards use only the minimum signal subset, making them compatible with any DSP master board. Additional signals include more interrupts, more address lines, and other DSP-specific signals, and can be used to build DSP-specific peripheral boards.

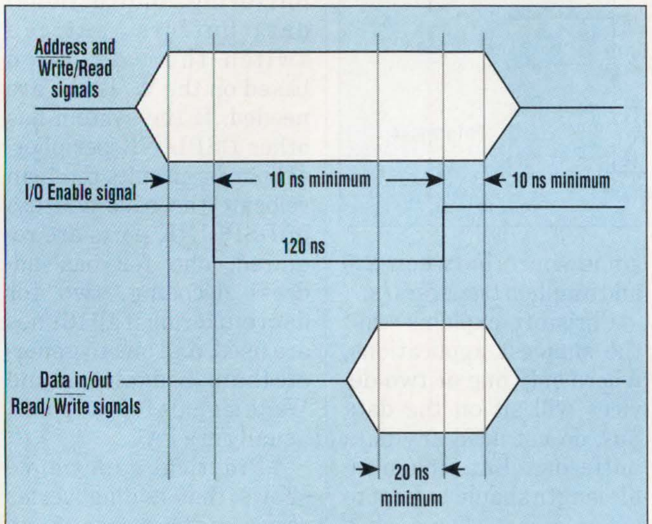


Fig. 1. DSPLINK timing diagram

Just three signals manage data transfers between master and slave boards. A Read/Write line indicates transfer direction, an I/O Enable (IOE) line provides the transfer strobe, and an Interrupt line lets the slave interrupt the master.

The timing of the minimum-signal bus is kept simple. Typically, the master will output the Address and Read/Write signals at the beginning of a cycle. It then expects the slave to have valid output data or get ready to input data at the rising edge of the $\overline{\text{IOE}}$ signal.

There's no fixed cycle-time definition *(Fig. 1)*. Instead, the bus defines minimum setup and hold times. A typical minimum cycle time of about 150 ns implies a top hardware-limited transfer rate of about 6.7 MHz.

The actual cycle time will vary depending on the digital-signal processor that implements the bus. This time will always be determined by the processor's cycle time, taking into account the number of wait states needed to satisfy the 120-ns-minimum $\overline{\text{IOE}}$ pulse width. Using the additional signal lines, it's possible to build peripheral boards that operate at higher rates, notes Christofi.

Overall transfer rate is usually determined by the I/O capabilities of the digital-signal processor being used. Typically, when outputting data, the processor reads values from memory, puts them into an internal register, and outputs them over DSPLINK. Conversely, when inputting data, the processor reads them in from DSPLINK and ends up writing them to memory.

This process varies depending on the processor used. For example, if the DSPLINK addresses are memory-mapped, the presence of a memory-to-memory DMA controller can speed up the transfer rate. Also, the rate will depend on whether the programmer exploits features like zero-overhead looping to move data through the processor, and on whether the source or destination memory is on or off the DSP chip.

Finally, throughput rate will depend on how many ALU operations the programmer performs on the data as it passes through the processor, and on the way the DSP chip implements those operations (for example, whether it's pipelined or not). In practice, a typical unidirectional sustained transfer rate, accounting for software overhead and a minimum of ALU operations, falls somewhere between 2.5 and 5 million transfers/s.

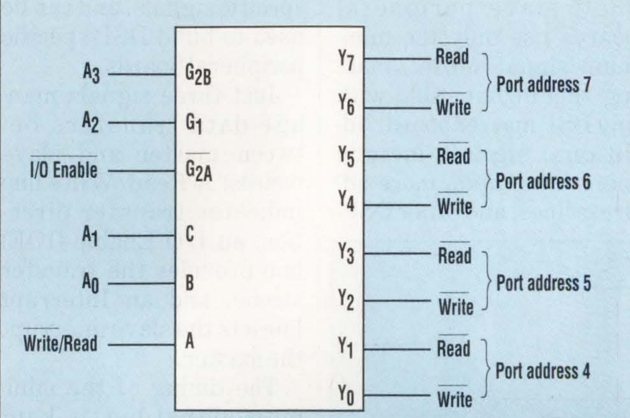


Fig. 2 74AS138 decoder

Christofi explains that the simplest applications, where only one or two devices will sit on the data bus, do not need any data buffering. But ribbon-cable length should be kept to a few inches. For such a simple case, a designer could use a single chip, such as a 74AS138 decoder, to produce Read and Write signals for up to four DSPLINK address ports *(Fig. 2)*.

For larger peripheral circuits that require data buffering, bidirectional data buffers that can switch their direction based on the $\overline{W}/R$ line are needed. If the system has other DSPLINK peripheral boards, circuits that can relocate the base address of DSPLINK ports are required: one for base-address decoding, two for data buffering if all 16 lines are used, and one to generate the individual Read and Write signals for the ports, usually in a PAL.

"Practical experience shows that adding series resistors of between 25 and 30 Ω in the control and data lines will allow the DSPLINK ribbon cable to be extended from several inches to several feet in length," Christofi says. The series resistors reduce ringing due to transmission-line effects, and won't affect the maximum data-transfer rate. He notes that "with cables of this length, you could put master and slave boards in separate PC chassis."

The aim of DSPLINK is to keep data transfer simple. As a result, Loughborough chose to support multiprocessor capabilities of DSP devices by adding a separate connector to boards based on such chips as the Motorola DSP96002 and Texas Instruments TMS320C30. Christofi comments that custom high-speed memory expansion falls into the same category, and is best left to buses separate from DSPLINK.

"But multiple masters can be supported on DSPLINK by designing a slave card that acts as a mailbox," he adds, and Loughborough has designed a "dual-processor communication module" that plugs between two master boards for just such a purpose. "It would also be quite reasonable to design such a board with on-board FIFO memories that would automatically buffer blocks of data between masters."

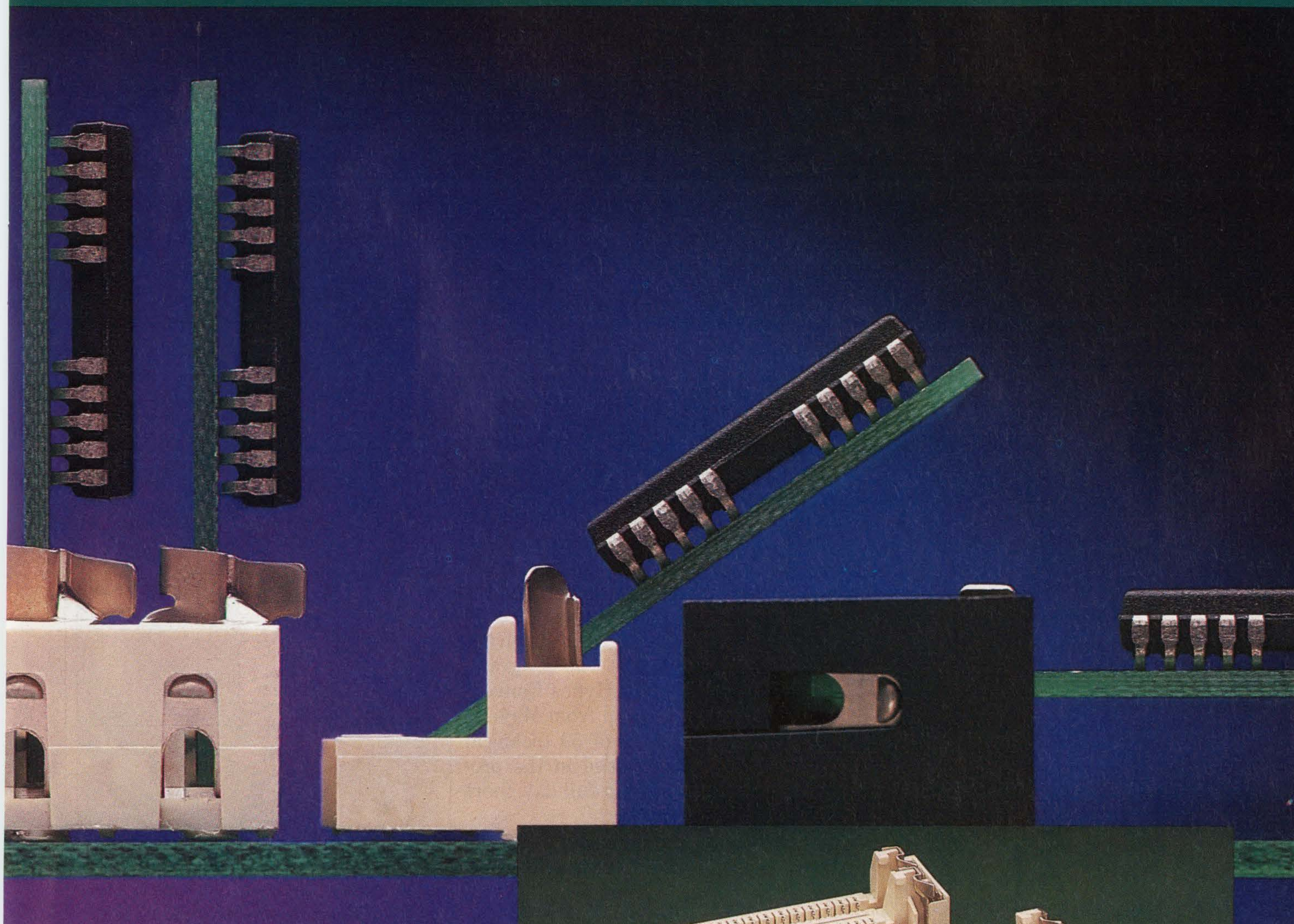
Christofi claims that designers are adopting DSPLINK for use in custom boards. Applications range from real-time 3D sound generation for virtual reality, to multichannel sleep/wake monitors in biomedical instrumentation. The bus has proven itself especially useful for factory test systems, and for test-and-measurement setups. "Because DSPLINK is so simple, you can often take an existing circuit attached to a PC or microcontroller chip and use DSPLINK to attach it to a DSP chip instead," he says.

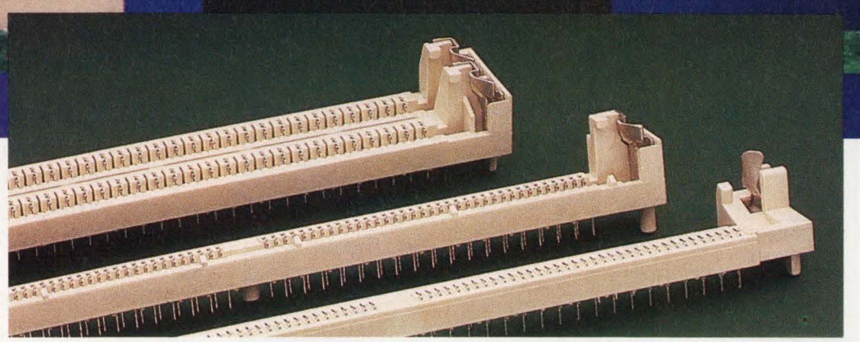
Several companies have built expanded versions of DSPLINK on processor boards of their own design, or produced peripheral boards for the bus. One company is Quantawave, a U.S.-based (Marlborough, Mass.) spin-off of Loughborough-Spectrum. It has announced a line of DSPLINK peripherals, and markets a peripheral board that links DSPLINK to DT-Connect for analog and image I/O boards developed by Data Translation, also located in Marlborough.

Loughborough is in the process of defining a DSPLINK II standard that will expand the address space to 8 bits and the data width to 32 bits. It will also allow for increased transfer speeds.

For more information, contact Loughborough Sound Images Ltd., the Technology Centre, Epinal Way, Loughborough, Leicestershire LE11 0QE, England; phone: +44 (0)509 231843. In North America, contact Spectrum Signal Processing Inc., Suite 301, Discovery Park, 3700 Gilmore Way, Burnaby B.C., Canada V5G 4M1; phone: +1 (604) 438 7266.

PETER FLETCHER





AMP MICRO-EDGE SIMM sockets give you all the advantages you need for maximum packaging flexibility. Straight, slant, and right-angle versions provide just the board-space/stack-height combo you want.

Straight and slant versions come in single or dual styles on .100" and .050" centers. Our latest right-angle versions offer .100" or .050" centers; 50-mil styles give you a choice of .125", .160", or .250" card slot heights to simplify tight packaging with either single- or double-sided modules.

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For product literature and more information, call our Product Information Center at 1-800-522-6752 (fax 717-986-7575). In Canada call 416-475-6222. AMP Incorporated, Harrisburg, PA 17105-3608.

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ELECTRO/92 SPOTLIGHTS ENGINEERING SOFTWARE

TECHNICAL SESSIONS FEATURE DISCUSSIONS ON OBJECT-ORIENTED DESIGN, SOFTWARE REUSE, AND CAE/CAD.

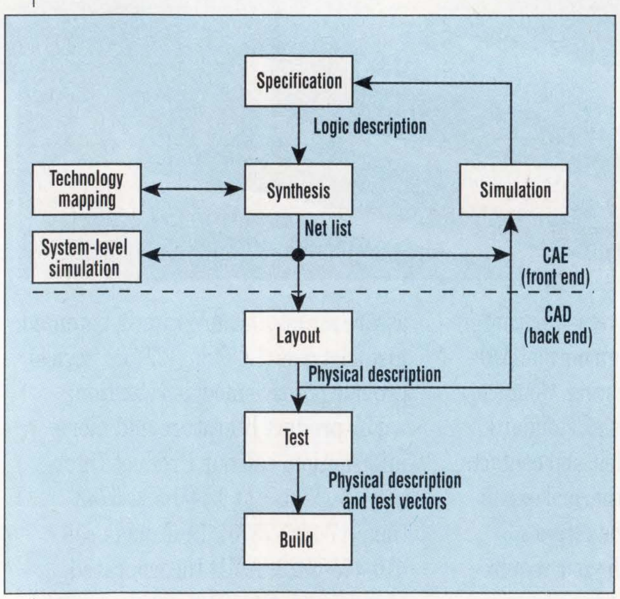
JOHN NOVELLINO

Concurrent engineering, semiconductor-device technology, manufacturing, software engineering, education, and international issues are among the common subject threads that, when woven together, form the Electro/92 program. The program, held at the John B. Hynes Convention Center in Boston from May 12-14, contains a total of 59 technical sessions. Also included in the program are 11 half- and full-day short courses and seminars.

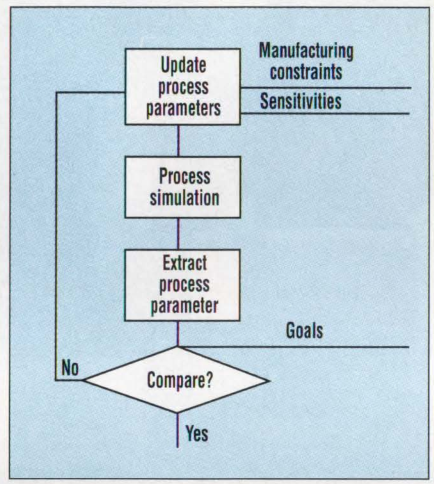
An expanded focus on software for the engineering environment highlights Electro/92's technical program. Six sessions over two days cover a variety of software issues. In addition, the exhibit floor features a dedicated software section. This section is designed to go along with areas for design, test, production, electronic design-automation tools, and semiconductors.

Software sessions on day one include a tutorial on a re-engineering process for large software systems, as well as paper sessions on software-engineering process trends and overviews and software-reliability engineering. Day two features a tutorial on object-oriented design, papers on software development and applications using object-oriented design and other technologies, and a panel session on software reuse issues. A number of special Electro/92 events are also devoted to software-related issues and developments.

Electro/92's keynote speaker is Jim Manzi, president and chief executive officer of Lotus Development Corp. In his address, "Networks and mobile users: Personal computing in the 90s," Manzi talks about trends and issues surrounding what he calls the "second revolution" in personal



1. A SIMPLIFIED FPGA design flow diagram indicates where CAE and CAD tools can help the designer improve productivity.



2. THIS FLOW chart describes an algorithm that lets users change process parameters based on a comparison of a simulation and the parameters' goals.

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Tektronix
Test and Measurement

High-Power Supply Is Current-Mode Controlled

Using the latest in single-converter geometry, the M series 3500-W high-density power supply fits into a 5-by-8-by-11.5-in. package. The supply's 100-kHz "H" bridge MOSFET design, which delivers a 7.6-W/in.^{3} power density, is current-mode controlled, allowing true N+1 configurations of up to eight units. The series permits input ranges of 208-230 V ac and 220-350 V dc. Standard features include overvoltage, overcurrent, and overtemperature protection, power-fail and power-good flags, redundant bidirectional error signals, remote margining, and bidirectional synchronization signals. The M series power supplies cost $2495.

***OPT Industries Inc.**, Phillipsburg, NJ; (908) 454-2600.* **CIRCLE 500**
■ *Booth 5123*

computing.

Manzi examines the rapid growth of networks and the boom in laptops and palmtops. His talk also focuses on how mobile users connect to networks, the importance of communications software, making collaborative computing a reality, "smart" applications, and why PCs haven't improved productivity.

In one of the software-oriented sessions, Jiri Soukup, president of Code Farms Inc., Richmond, Ontario, Canada, discusses the need to carefully balance the two basic parts of a program—data and algorithms. Soukup's paper, "The secret of efficient software design: Internal data organization," states that programmers often start coding without thinking about data. The result is an intricate network of pointers that's difficult to debug. According to Soukup, even though an object-oriented language forces programmers to consider data from the start, the relations between objects are still often not treated properly.

Soukup's answer is a new way to manage internal program data by separating data objects from relations. The technique improves code clarity and software productivity, as well as run-time performance. On large industrial projects, the new method reduces coding and debugging time by a factor of 2 to 3, and enhances both code maintenance and reusability.

The paper goes through an actual example: The program stores a set of towns connected by highways, and calculates the shortest distance between any two requested towns. The programmer must weigh the advantages and disadvantages of whether to store the data in an array, a linked list, or a hash table. The example uses the C++ version of the Code Farms library, which is also available in C.

One session within the thread of semiconductor device technology—"FPGA design technology enhances design productivity"—opens with a paper describing FPGA design aims. It also addresses CAE and CAD tools, including various types of sili-

Controller Links GPIB To Sparcstation Ethernet

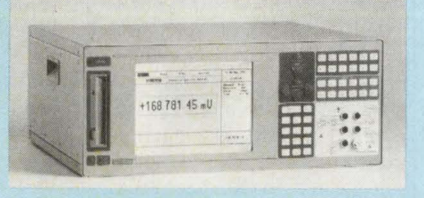
The GPIB-ENET/Sun kit lets users control IEEE-488 instruments from any Sparcstation Ethernet host connected to a TCP/IP network. The controller eliminates the 20-m cable limitation of GPIB. Multiple controllers, each handling 14 instruments, can be connected to one network. The kit comes with high-level NI-488M software for SunOS, which is compatible with ex-

isting NI-488 application programs and automatically handles Ethernet and GPIB protocols. Two versions are available: A Thick Ethernet-(10Base5)/Twisted pair(10BaseT) kit that costs $1595, and a Thick Ethernet(10Base5)/Thin Ethernet-(10Base2) kit that goes for $1695. Both prices are for single-workstation use. Site licenses for multiple workstations are optional.

***National Instruments Corp.**, Austin, TX; (800) 433-3488.* **CIRCLE 502**
■ *Booth 2201*

7-1/2-Digit DMM Includes 386-Based Computer

The Model 8047/386 is a precision 7-1/2-digit multimeter combined with a 386-based computer. The 19-in. chassis also houses a 20-channel, 4-wire scanner. Thus, users need only one instrument to log data and process, analyze, and display measurements with real-time graphics on up to 20 channels. The DMM's 24-hr. stability is 1 ppm on



voltage, current, resistance, and temperature. Using its extensive math capability, it can directly display calculated values, including alarm thresholds. The computer has a 40-Mbyte hard-disk drive, a 3-1/2-in. floppy-disk drive, a front-panel foil keyboard, and a VGA LCD screen. The 8047 costs $11,900 and is available from stock to 4 weeks.

***Prema Precision Electronics Inc.**, Montclair, CA; (800) 441-0305.* **CIRCLE 501**
■ *Booth 2408*

con solutions, tool requirements, and the design environment. The paper's author, Vincent J. Coli, field programmability product line manager at VLSI Technology Inc., San Jose, Calif., offers an overview of these three areas.

Coli first describes the three basic types of digital logic: standard logic, programmable ASICs, and masked ASICs. The two distinguishing attributes between the parts is how they're purchased (standard versus custom) and how they're used (standard versus custom), Coli notes. FPGAs fall into the category of programmable ASICs, taking the best from both worlds: They can be bought as standard parts but used as custom products.

Both programmable and masked ASICs, however, require designers to make use of CAE/CAD tools. The paper presents a simplified FPGA design flow diagram to show how CAE/CAD tools fit into the process *(Fig. 1)*.

At the front end, or CAE portion, the tools help the designer specify a logic description, synthesize a net list, and simulate the logic to verify its correctness, Coli says. The backend, or CAD, tools aid in creating a physical layout, generating test vectors, and programming the ASIC.

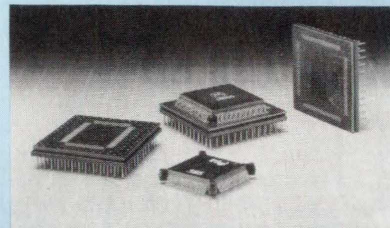
Coli also supplies a hierarchical description of FPGA design technology and of FPGA design platforms. He notes the shift away from vendor-specific frameworks (or DOS in the case of PCs) to open frameworks, such as Windows, X-Windows, and OSIF/Motif. Because FPGA design is only one of a number of jobs that go into system design, this shift will help engineers who have to use a variety of tools.

The concurrent-engineering thread presents two authors from the academic world who give an overview of semiconductor process representation. The authors describe how process representation standards fit into a CAD framework that's used for solid-state device development.

Michael B. McIlrath of the Massachusetts Institute of Technology, Cambridge, and Goodwin Chin of Stanford University, Calif., note that the design of a device and the design of a manufacturing process sequence to fabricate the device generally occur simultaneously. However,

CONVERTERS AID ON-BOARD TESTING OF SMT DEVICES

The SMT-PGA series converters come in 23 generic and device-specific configurations for EIAJ and JEDEC surface-mount technology (SMT) devices. The converters' top boards match the pin patterns of the most popular 25-mil SMT devices. Generic converters are pin-to-pin compatible with the majority of standard SMT device footprints. In the device-specific converters, pin configurations are the same as for the actual PGA package. These converters accept such new devices as the 680320, 68030, 386SX, and 386DX. The compact converter board has a footprint no larger than the PGA device itself. The SMT-PGA converters are priced from $9.98 each in 10-piece quantities and are available from stock.



***ITT Pomona Electronics**, Pomona, CA; (714) 469-2900.* CIRCLE 504
■ *Booth 2321*

LIGHTED PUSHBUTTON SWITCHES GET NEW CAPABILITIES

Three options enhance the functionality of the Series 584 switch line. The extended capsule offers one of the lowest touch temperatures in the industry and a 75° cone of vision. The rod-mount feature saves panel space because switches are gang mounted into the smallest panel opening. And to minimize installation and maintenance costs, the IWTS termination system was added for easy assembly and disassembly of wires. The lightweight, 5/8-in. square units have an 8-A rating. The switches can be individually or matrix mounted, with the matrix accepting MIL-C-39029/57-354 poke-home terminals. Options include RFI/EMI protection, splash-proof shields, and switch guards. Series 584 prices range from $95 to $285 each, in 100-piece lots.

***Eaton Corp.**, Aerospace & Commercial Controls Div. Milwaukee, WI; (414) 449-7326.* CIRCLE 503
■ *Booth 2233*

ENCAPSULATED DC-DC CONVERTERS HANDLE 200 W

The 200-W AMPSS AM80 family of dc-dc converters deliver a 5-V output at 40 A and accept nominal dc inputs of either 48 or 300 V dc. The devices target distributed power applications, such as N+1 redundant systems and modular power. The series features a 1-MHz switching frequency, 84% operating efficiency, and a 36 W/in.^{3} power density. They offer an assortment of safety-isolated, secondary-side programmable status and control functions, including remote sense, output voltage adjust, overvoltage protection adjust, current share, clock sync, remote sense, and enable. Most of these functions can be linearly programmed externally. The AMPSS AM80 costs $245 and is available from stock.

***ASTEC Standard Power**, Oceanside, CA; (618) 757-1880.* CIRCLE 505
■ *Booth 4527*

TRIMMING POTS FIT SMALLER APPLICATIONS

The G3 Series of microminiature trimming potentiometers are single-turn units with a range of 100 Ω to 1 MΩ and a tolerance of +20%. The units measure 3.4 by 3.2 by 2 mm. Two mounting styles are available: the A version with J-hook terminals, and the B version in a gullwing style. The pots are rated for 0.125 W at 70°C and have an operating-temperature range of –55 to +125°C. In addition, the components are sealed to withstand soldering and immersion-cleaning processes in accordance with MIL-R-22097. In quantities of 1000, the G3 Series costs $1.50 each. Delivery is in 6 to 8 weeks.

***TOCOS America**, Arlington Heights, IL; (708) 364-7277.*

CIRCLE 506

■ *Booth 2120*

they say the job of IC manufacturing has suffered from a critical separation between process design and actual fabrication.

Ongoing university research in computer-integrated manufacturing (CIM) aims to solve the problem of managing complex microsystem design and manufacture, and integrating the design and manufacturing process, say the authors. Researchers are looking at modern software technology, such as object-oriented databases and expert knowledge-representation techniques. This work has identified the need for a common mechanism to represent, manage, and access information about the manufacturing process throughout its life cycle.

The research includes work toward establishing standards for semiconductor wafer representation and semiconductor process representation (SPR). The SPR provides a hierarchically organized body of knowledge about the process as it's being developed. As such, the SPR offers both a technology CAD and a manufacturing representation of process steps, according to the paper's authors.

McIlrath and Chin present a flow chart for an algorithm that uses the SPR for process optimization *(Fig. 2)*. With the use of the algorithm, designers can change parameters based on a comparison of the extracted output of process simulation with device and process goals.

The differences between simulation tools are discussed in a paper by

David Bornstein, manager of CAD at Toshiba America Electronic Components, Burlington, Mass. The paper, "ASIC design verification in a multivendor simulation environment," cites the increasing number of design tools available. Given the diversity in the way simulators work, the probability of having two simulators supply the same results is very small, says Bornstein. This can produce friction between the ASIC

MEMORY CARDS RANGE TO 1.5 MBYTES

The TB series of memory cards, which conform to the Personal Computer Memory Card Industry Association (PCMCIA) standard, come in four sizes: 256 kbytes, 512 kbytes, 1 Mbyte, and 1.5 Mbytes. The cards use static RAM and lithium batteries for memory protection. The units have a write-protect switch and an easily transferable battery holder. Included in the cards is a 1-kbyte attribute memory that can store attribute information like type of memory and access time. The cards are suitable for such applications as computer-file memory, sequence memory for robots, data-terminal memory, voice memory for computer generation, data memory for measurement equipment, and dial memory for telephones.

Maxell Corporation of America, *Fair Lawn, NJ; (201) 794-5900.* **CIRCLE 507**

■ *Booth 2014*

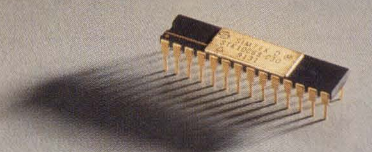
500-W SWITCHING SUPPLY IS SMALL

One of the smallest 500-W power supplies available is the KX500 switching supply, with dimensions of 10 by 5 by 2 in. The unit features 0.99 power-factor correction, which exceeds the IEC 555-2 specification. An FCC/VDE class-B filter is standard. The main +5-V output delivers 80 A, with a remote-sensing capability that can compensate for a 0.3-V cable loss. Available models have from two to four auxiliary outputs, all of which are regulated and fully isolated. With the multiple outputs, users can handle all system-voltage needs with one unit. Input operating voltage is 90 to 264 V ac at 47 to 400 Hz.

Basler Electric, *Highland, IL; (800) 645-2074.* **CIRCLE 508**

■ *Booth 1503*

Batteries not included.



Nonvolatile random access memory doesn't need batteries anymore. It doesn't need an extra chip either. All it needs is this. The nvSRAM from Simtek.

At 64K, the nvSRAM offers the density to handle virtually anything you can come up with. It's extremely fast, with access speeds ranging from 30ns-55ns. It doesn't depend on a battery for nonvolatility, so reliability is unsurpassed. And because it's a one-chip solution, precious little board space is required.

We think you'll find our nvSRAM is well suited to applications ranging from cellular phones to the most advanced military hardware. To prove it, we'll send you a free design kit. And we guarantee you'll get it within 48 hours of your request. So call Simtek at 1-800-637-1667 right now for your free design kit or call us for details on where to buy production quantities. And find out exactly why, when it comes to nonvolatile RAM, batteries are dead.

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MODULES COOL DEVICES MORE EFFICIENTLY

Thermalloy Cooling Modules (TCMs) consist of a pin-fin heat sink combined with a dc brushless fan. Users can select a 5- or a 12-V fan. The five standard TCMs accommodate the Intel i486, i860, and i960; the AMD Am29000; the Motorola 68040; and other pin grid arrays of 15 by 15, 17 by 17, 18 by 18, and 21 by 21 pins. The TCM's cooling efficiency approaches that of recirculated liquid, while taking much less space. With a 5-V fan, the TCM's performance is 6 to 9 times better than a heat sink alone in natural convection, and 1 to 2.7 times better than forced convection at 400 ft./min. linear airflow. A 17-by-17-pin PGA version, the 2321B, costs $13.24 in quantities of 500, with delivery is 4 to 6 weeks.

***Thermalloy Inc.**, Dallas, TX; (214) 243-4321.* **CIRCLE 509**
■ *Booth 5136*

vendor and the customer if the vendor and customer are using different simulation programs.

The author describes a number of factors that can create different simulation results, depending on which tool is used. Among them are event scheduling, resolution, round-off techniques, glitch handling, primitive capability, simulation modeling, and which version of a program is used.

For instance, users must consider the event that gets processed first when inputs are switched simultaneously. Also, different resolutions can create different results. Setup and hold-time margins may disappear at higher-resolution levels, Bornstein notes.

How the ASIC macro cells are modeled, at the behavioral or gate level, is also important. Discrepancies in both timing and functionality results are more likely if one simulator makes use of a distributed delay model and the other employs a pin-to-pin model.

As troublesome as these differing results can be, they can be understood and minimized to the point where using multiple simulation platforms is advantageous, explains Bornstein. For example, ASIC vendors can expand their customer base by supporting third-party tools. Furthermore, these customers can become more confident by having their designs simulated on multiple platforms.□

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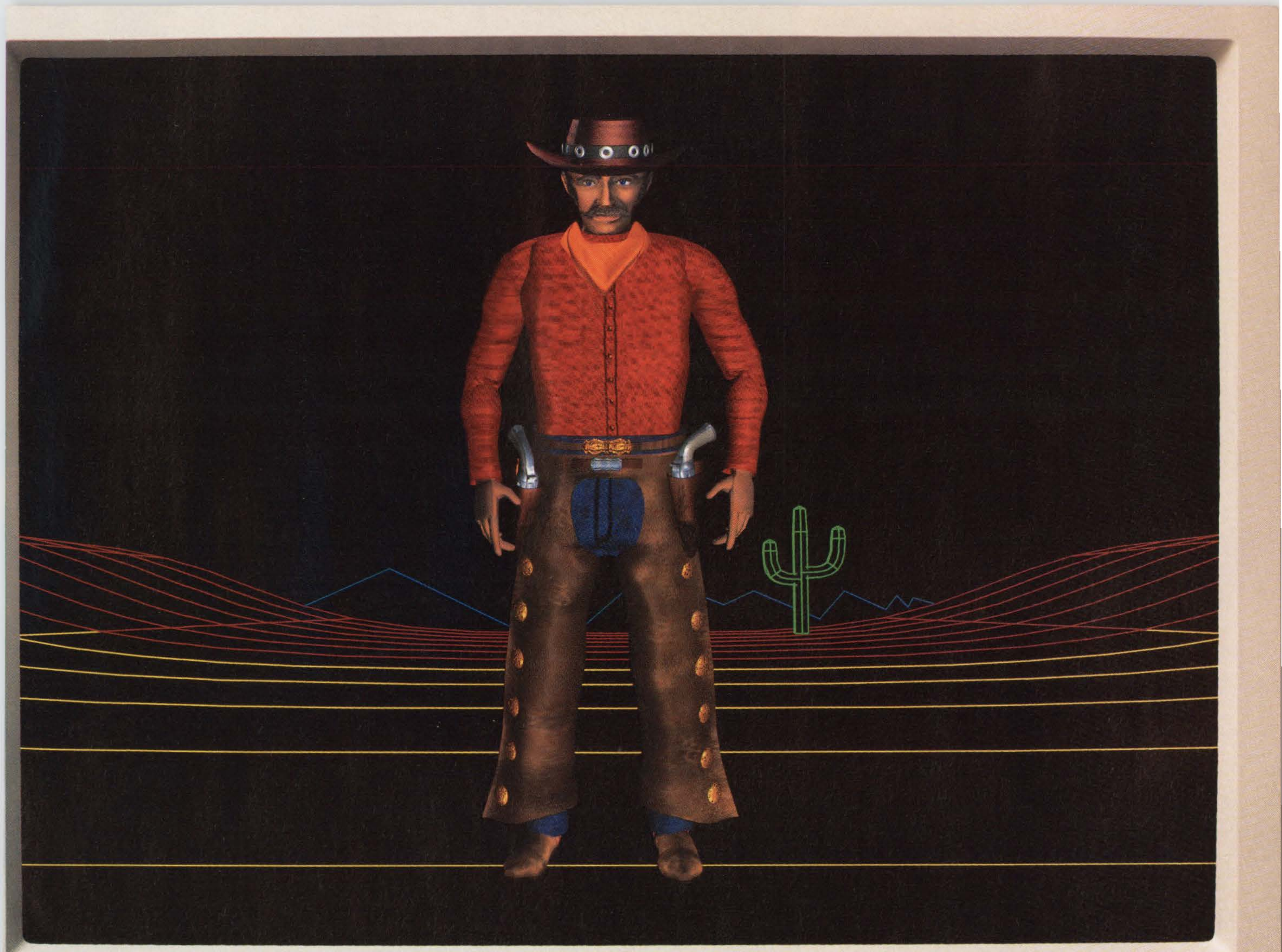

Intel's new RapidCAD™ CoProcessor will help your i386™ PC draw 70% faster.

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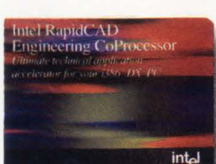
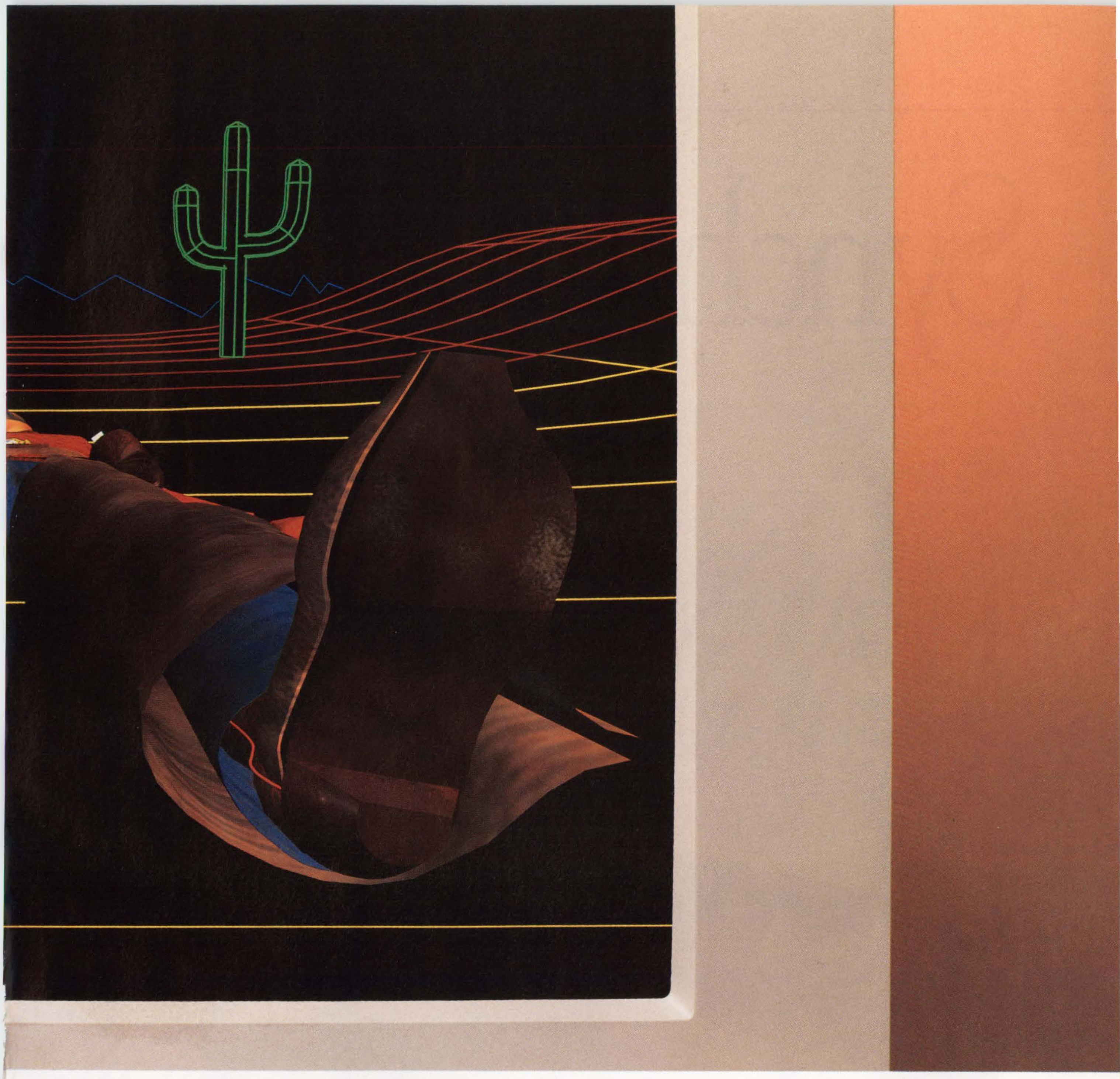


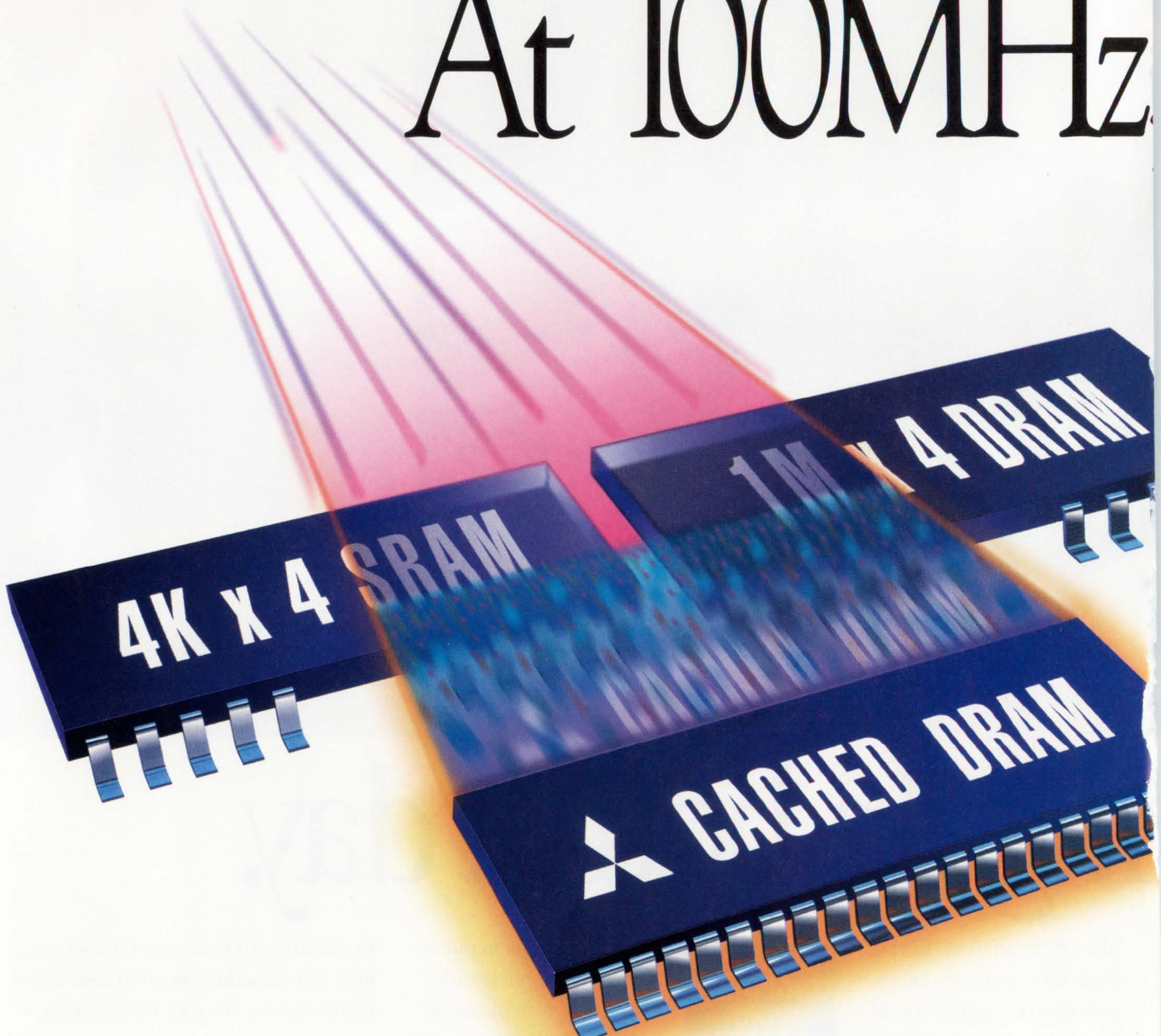
Wait, wait, wait. Do you ever get the feeling that's all you do when your PC is running CAD software? Annoying, isn't it?

Well, pardner, the wait is over. At least a good portion of it. Because now there is new Intel RapidCAD™—the industry's first Engineering CoProcessor. This powerful two-chip set replaces both your i386™DX CPU and your i387™DX Math CoProcessor, to make your PC quick on the draw.

Designed specifically to accelerate PC CAD and other technical applications, the RapidCAD Engineering CoProcessor will help you realize productivity gains of up to



Synchronous 4Mb At 100MHz.



Cached DRAM. It Screams!

Matching low-cost DRAM technology with today's high-speed CPUs can be a design engineer's nightmare. Until now. **Introducing the 100MHz 4Mb Cached DRAM from Mitsubishi.**

FIRST SYNCHRONOUS DRAM

Mitsubishi combined a fast, 4K x 4 SRAM and a 1M x 4 DRAM with a wide, 16 x 4 bit internal bus and a synchronous clock design, all into one tiny TSOP IC. The result is the industry's first synchronous DRAM with on-board cache.

100MHz OPERATION

The Cached DRAM's large, 16 x 4 bit internal data path can transfer a 16-line data block in just one cycle, allowing the small on-chip cache to perform like a much larger external cache. The result is fast, 100MHz performance at a much lower cost than separate cache configurations. Plus, the Cached DRAM's fast copy-back scheme significantly reduces the miss cycle penalty time.

COST-EFFICIENT, SMALL SIZE

The Cached DRAM die and package are only 7% larger than those of a standard 1M x 4 DRAM. And, since they are manufactured with the same process and on the same production line as Mitsubishi's standard 4Mb DRAMs, Cached DRAMs are highly cost-efficient to manufacture.

LOW POWER OPERATION

With a clock that can be stopped to reduce power consumption to as low as 1mW, the Cached DRAM is ideal for portable and highly integrated applications where low power consumption, compact size and fast operation are essential.

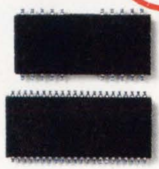
MITSUBISHI'S CACHED DRAM PERFORMANCE

Part Number	Cache Hit Access/Cycle	Cache Miss Access/Cycle	Direct Array Access/Cycle	Package
M5M44409TP-10	10ns/10ns	70ns/280ns*	70ns/140ns	TSOP**
M5M44409TP-15	15ns/15ns	75ns/300ns*	75ns/150ns	TSOP**
M5M44409TP-20	20ns/20ns	80ns/320ns*	80ns/160ns	TSOP**

Samples Available June 1992

*Cache hit cycles can resume after one miss access time, while the copy-back completes in the background.

**TSOP Type II. Also available in reverse pin-out TSOP.



Standard 4Mb DRAM.

Actual size.

4Mb Cached DRAM is only 7% larger than a standard 4Mb DRAM.

Not your ordinary next-generation DRAM, Mitsubishi's 4Mb synchronous Cached DRAM sets a totally new standard for cost-effective, high performance memory. For more information and technical specifications, please call **(408) 730-5900, ext. 2106 or 2226.**

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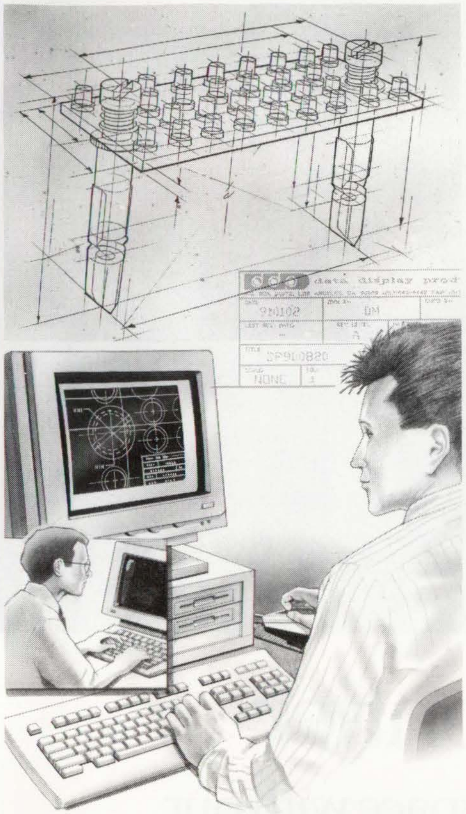
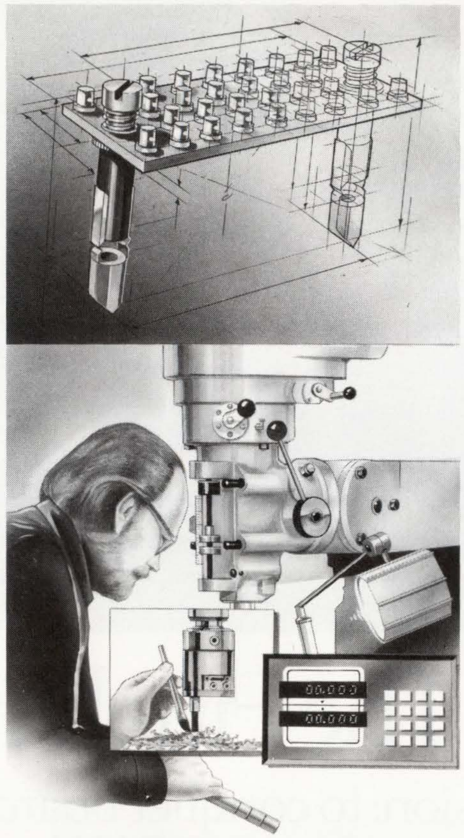
DESIGNING LED SOLUTIONS

DDP® custom lamp-based design
U.S. Patent No. 4,965,457.



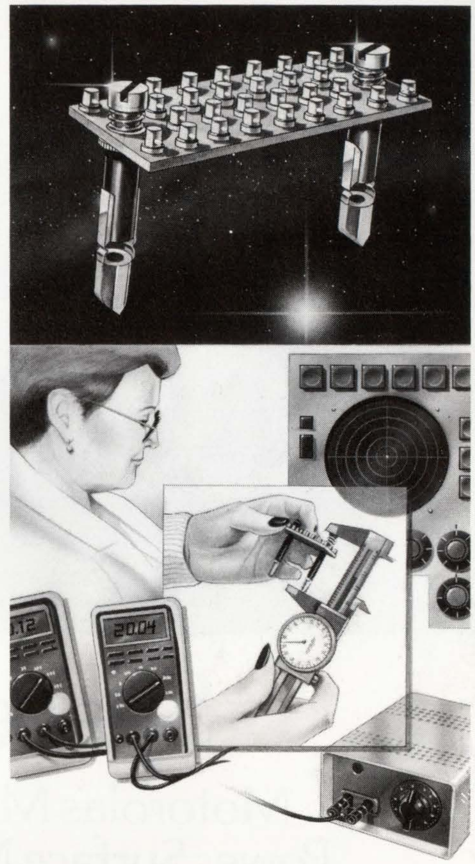
ENGINEERING LED SOLUTIONS

DDP® custom lamp-based design
U.S. Patent No. 4,965,457.



MANUFACTURING LED SOLUTIONS

DDP® custom lamp-based design
U.S. Patent No. 4,965,457.



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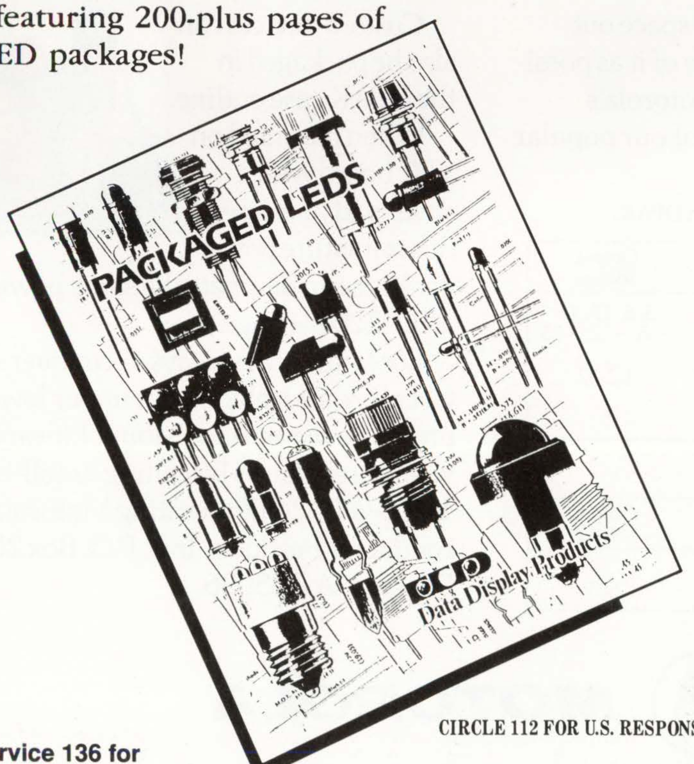

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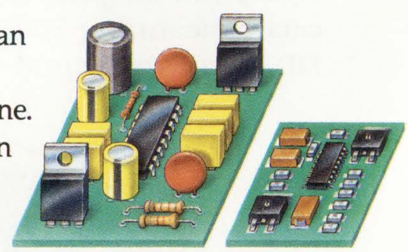

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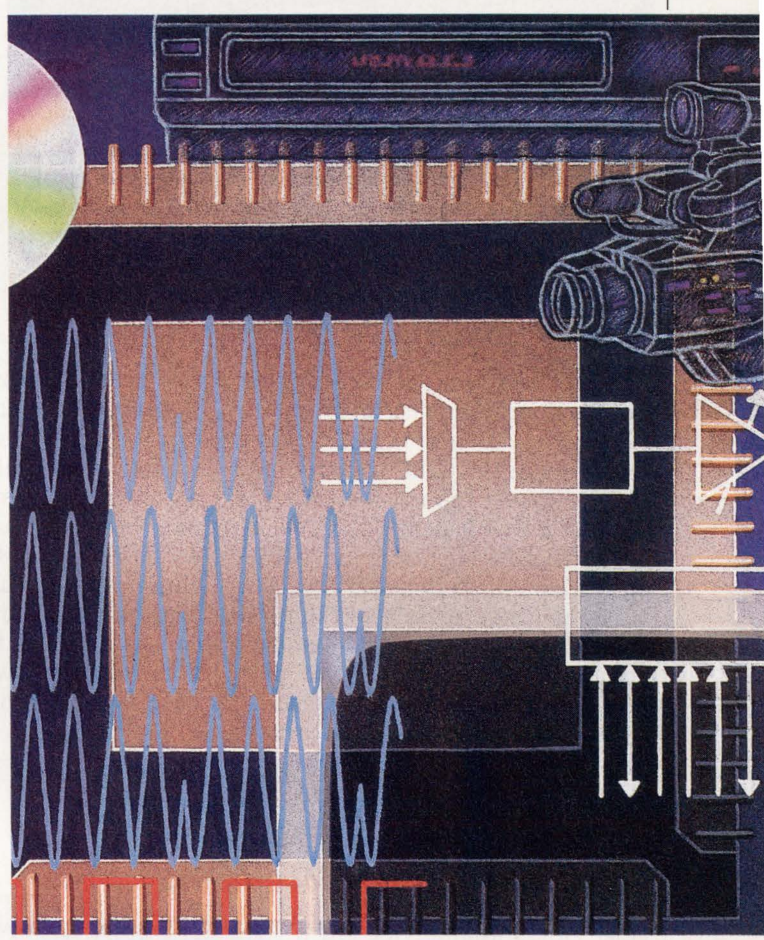
MOTOROLA

Advanced Signal-Processing Techniques Produce Studio-Quality Video From Multiple Sources.

Digital Video Chips Merge Multiple Inputs

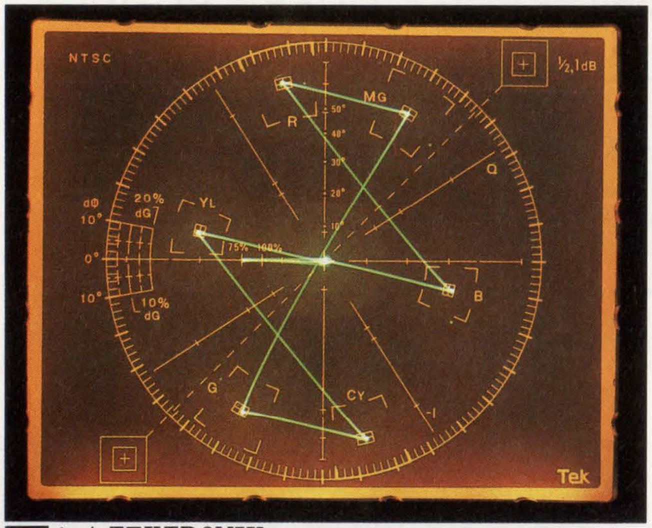
Milt Leonard



Ideally, a multimedia system should accept video signals from various sources and mix them with computer images for display or recording. Unfortunately, computer graphics and video technology have evolved along separate paths, each with its own set of unique and incompatible standards. Nonsimilarities abound among interlacing and noninterlacing schemes, line and frame rates, display aspect ratio, pixel shape, resolution, bandwidth, and transmission format. As a result, early attempts at merging video and computer technologies have required highly complex and costly circuit-board designs, usually found in expensive equipment used in broadcast studios and post-production sites.

Using advanced signal-processing techniques, two mixed-signal CMOS ICs from TRW LSI Products solve this problem. They compose the necessary interface for combining computer graphics with various video sources to produce studio-quality video. The TMC22070 is a genlocking video analog-to-digital converter that converts analog video signals from TV receivers, VCRs, video cameras, and video disks into a digital stream. The TMC22190 encoder converts digitized video from the 22070 or computer-generated sources into S-video (separate luminance and chrominance components) and composite video outputs in either NTSC (National Television Standards Committee) or European PAL (phase-alternating-line) format for use by monitors and VCRs. The 22190 also converts computer graphics into standard video signals. The two chips can be used individually or as a team to produce a functionality and display quality rivaling what is found only in broadcast studios and post-production facilities *(Fig. 1)*.

Containing a three-channel input multiplexer, variable-gain amplifier, and digital back-porch clamp, the 22070 genlocking video digitizer converts standard analog composite-video signals into 8-bit digital composite data under program control *(Fig. 2)*. The device accepts video on one of the three input channels, adjusts the gain, clamps the input level to the back-porch voltage (dc black-reference voltage), and digitizes the video at a multiple of the line rate. Along with the digitized video, the device sends extracted horizontal and vertical sync signals, field identification data, subcarrier frequency and phase information, and a sampling (pixel) clock signal to the companion encoder through an 8-bit



1. A TEKTRONIX model 1780R vectorscope exhibits the color precision produced by TRW's TMC22190 digital video encoder. The instrument demodulates the composite-video signal (color bars) from the encoder and displays each of the six colors (red, magenta, blue, cyan, green, and yellow) as a dot within target rectangles on the screen. Precise dot positioning within each target indicates lack of amplitude noise (radial smearing), phase noise (rotational smearing), and color errors.

digital video port and control pins. The chip operates with an internally generated 2X pixel-clock signal, which controls data transfer and also serves as the master clock for the 22190. Nominal pixel rates can be set at 12.2727 Mpixels/s for NTSC, and 14.75 or 15.0 Mpixels/s for PAL.

The multiplexer selects the three video inputs, which have a standard voltage level (sync tip to peak color) of 1.25 V. Good channel-to-channel isolation allows active video signals to reside on all three inputs simultaneously. The analog clamp ensures that the input video signal falls within the active range of the ADC. Because video signal levels can vary substantially, the 22070 performs automatic level setting to establish correct signal amplitudes for digitizing.

The only amplitude reference that's always present in a video signal is the back-porch voltage. This voltage is subject to various distortions that may affect the active video portion of the waveform. Another classic problem is sync-tip compression or clipping. Rather than track minor variations in sync-tip amplitude, the 22070 fixes proper signal amplitudes during initial genlock acquisition, and then holds the gain constant. This produces a more stable picture under adverse signal conditions.

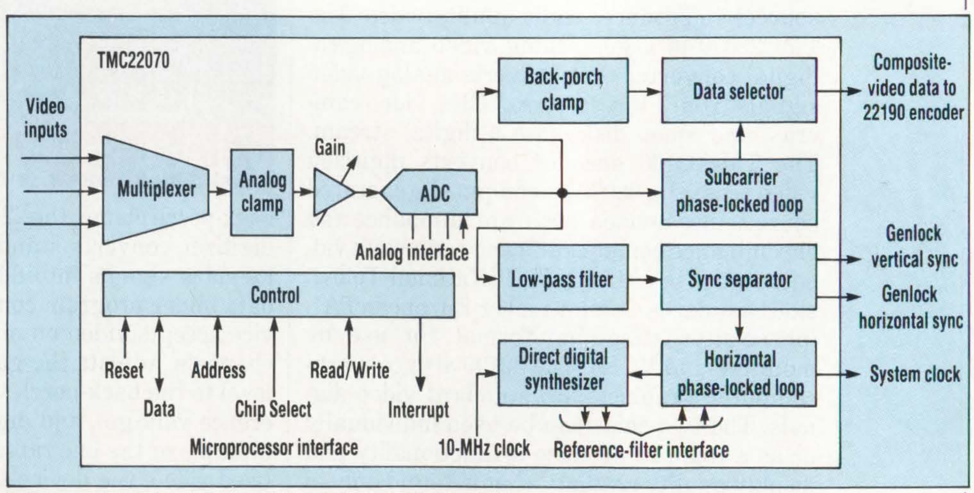
Another common error source in video systems is improper termination of video signals, usually resulting from double termination (connecting two 75-Ω loads at one end of a coaxial cable). To compensate, the 22070 has a selectable gain of 1.0 or 1.5. The higher gain amplifies a doubly terminated signal so that the automatic-gain circuit can establish proper signal levels.

To get true multimedia capability, a system must synchronize video signals from devices ranging from video disks to consumer-grade video cameras. Consumer-grade VCRs present special timing problems because they fail to meet broadcast standards in several ways. Timebase imperfections constitute one way, which probably rates as the most significant. For example, minute variations in mechanical tolerances can vary the absolute length of time per video line. This condition, caused by mechanical tape distortions, requires the device's horizontal phase-locked loop (PLL) to have a wider-than-normal bandwidth. The 22070's genlocking video ADC starts its acquisition process with a wide bandwidth, and then reduces the bandwidth following lock acquisition for higher performance.

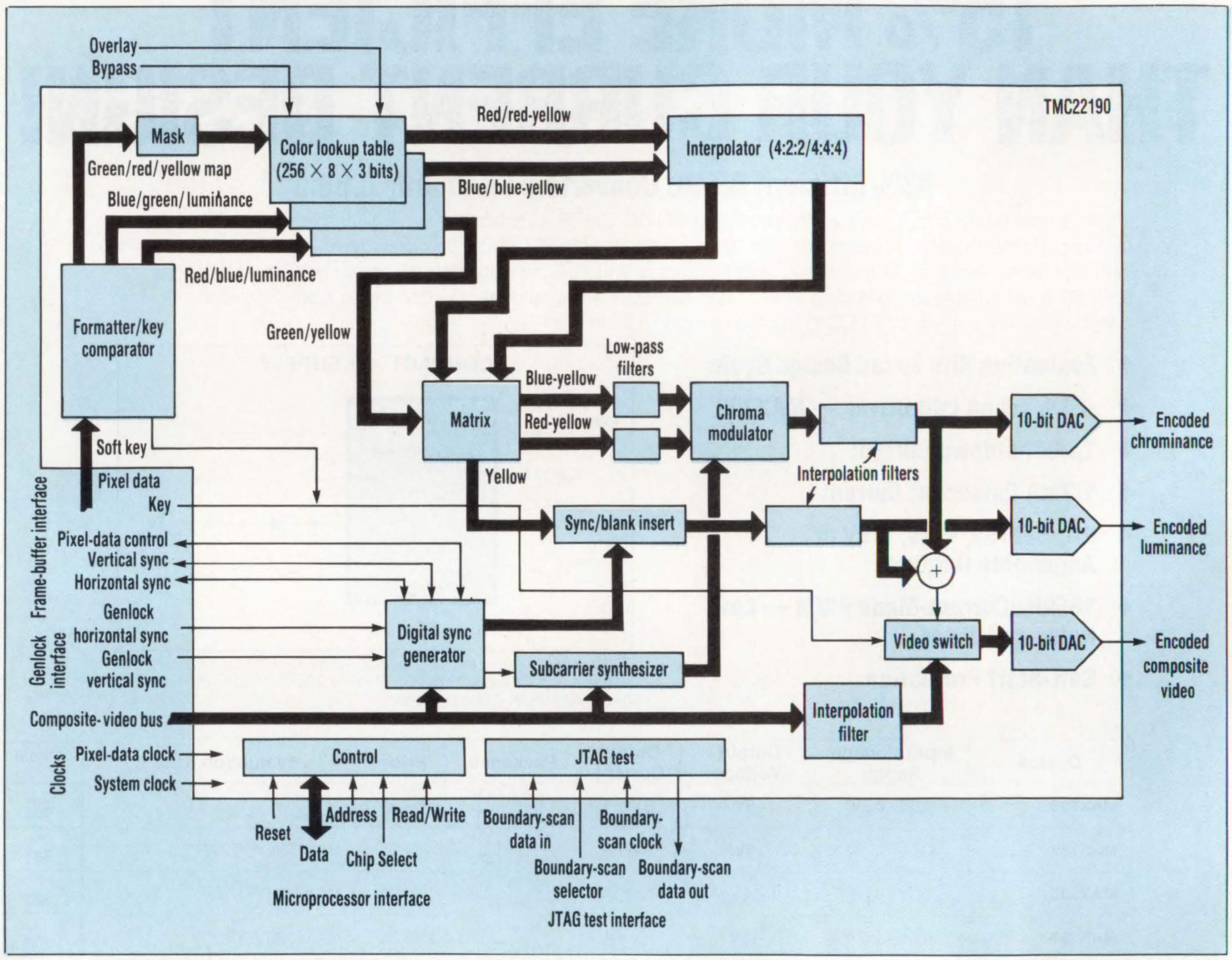
VCRs also suffer from step timebase errors caused by switching between multiple head transducers in a helical-scan system. The 22070 reduces this error by setting the PLL bandwidth to a value that allows recovery from head-switch errors before the start of active video in the succeeding field. Also, circuitry can be enabled to vary the number of pixels only in the line containing the head switch.

Signal degradation also stems from using nonstandard vertical synchronization pulses during fast-forward, rewind, and still-frame operations. The user can improve performance in these modes by selecting a special on-chip vertical-synchronization pulse detector.

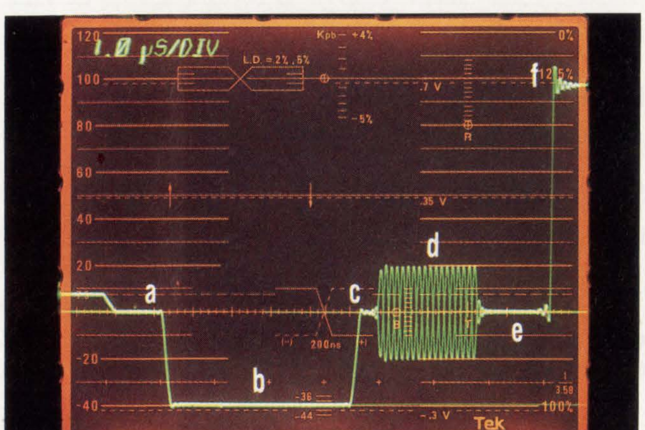
To minimize analog crosstalk from the microprocessor-interface bus, the 22070 reduces the number of pins connected to the bus by serially accessing an internal shift register.



2. AFTER AN ANALOG VIDEO SIGNAL is digitized, the TMC22070's subcarrier phase-locked loop extracts phase and frequency data from the signal. During the horizontal blanking interval, this data exits the composite 8-bit video bus to the 22190 encoder and/or a frame memory. The digital synthesizer generates the reference signal required by the horizontal PLL.



3. THE TMC22190 ENCODER translates between the multiple standard color spaces and data formats used in computer graphics and digital video systems. The device integrates key encoding functions, such as color keying, color lookup table (CLUT), 4:2:2 to 4:4:4 interpolation, color-space conversion, quadrature chroma modulation, and overlay switching. To be compatible with existing hardware and software, color-space mapping by the formatter, CLUT, and matrix functions precisely matches the output of a RAMDAC CLUT.



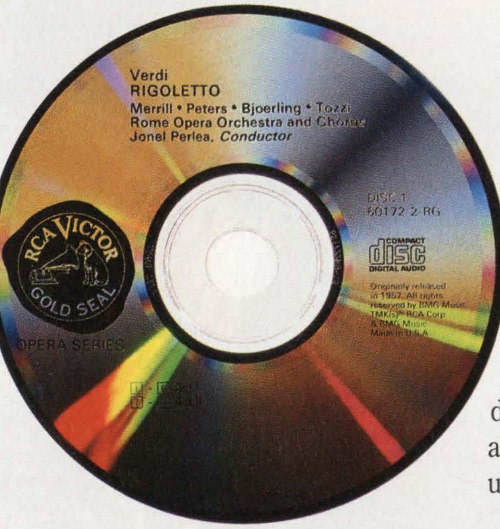
4. ALL SIX PORTIONS of the TMC22190 encoder's horizontal blanking interval are fully programmable. These include the front porch (a), horizontal sync pulse (b), back porch (c), color burst (d), breezeway (e), and active video part (f).

The device comes in a 68-lead plastic chip carrier with J leads and operates from a 5-V supply.

The 22190 digital video encoder performs functions that previously required a board full of analog components *(Fig. 3)*. The chip, which supports pixel rates of 10 to 15 Mpixels/s, accepts various video and computer graphics formats, including 24- and 15-bit GBR (green-blue-red) and RGB (red-green-blue) formats, the YC_bC_r 4:4:4 format, and 8-bit color-indexed data. Input luminance and color data YC_bC_r in a 4:2:2 format is interpolated to a 4:4:4 format for encoding. A mask register receives pixel-mapped data from the input formatter, facilitating pixel animation and other special graphics effects. Its programming and operation are identical to those of the 171/176 family of graphics RAMDACs.

A 256-by-8-by-3 color lookup table (CLUT) that's loaded like a common RAMDAC can serve multiple functions, depending on the data source and input format. Defining three 8-

The difference between AVX tantalum capacitors and the competition is just as noteworthy.



Ask an audiophile to explain why CDs are such an improvement over 78's, and you'll hear phrases like "Superior performance." "Takes up less space." "There's no comparison." Talk to a design engineer about AVX tantalum capacitors and chances are you'll get the same response.

Quite simply, AVX tantalum products are a cut above the competition. That's because recent AVX advances give our tantalum chips greater volumetric efficiency than competing devices. So designers can specify higher capacitance values, even in applications that demand small footprints and lower board heights.

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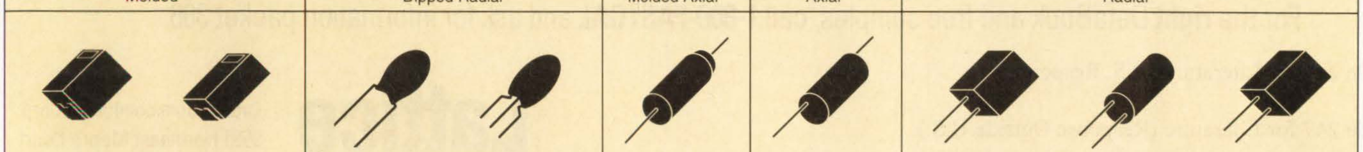
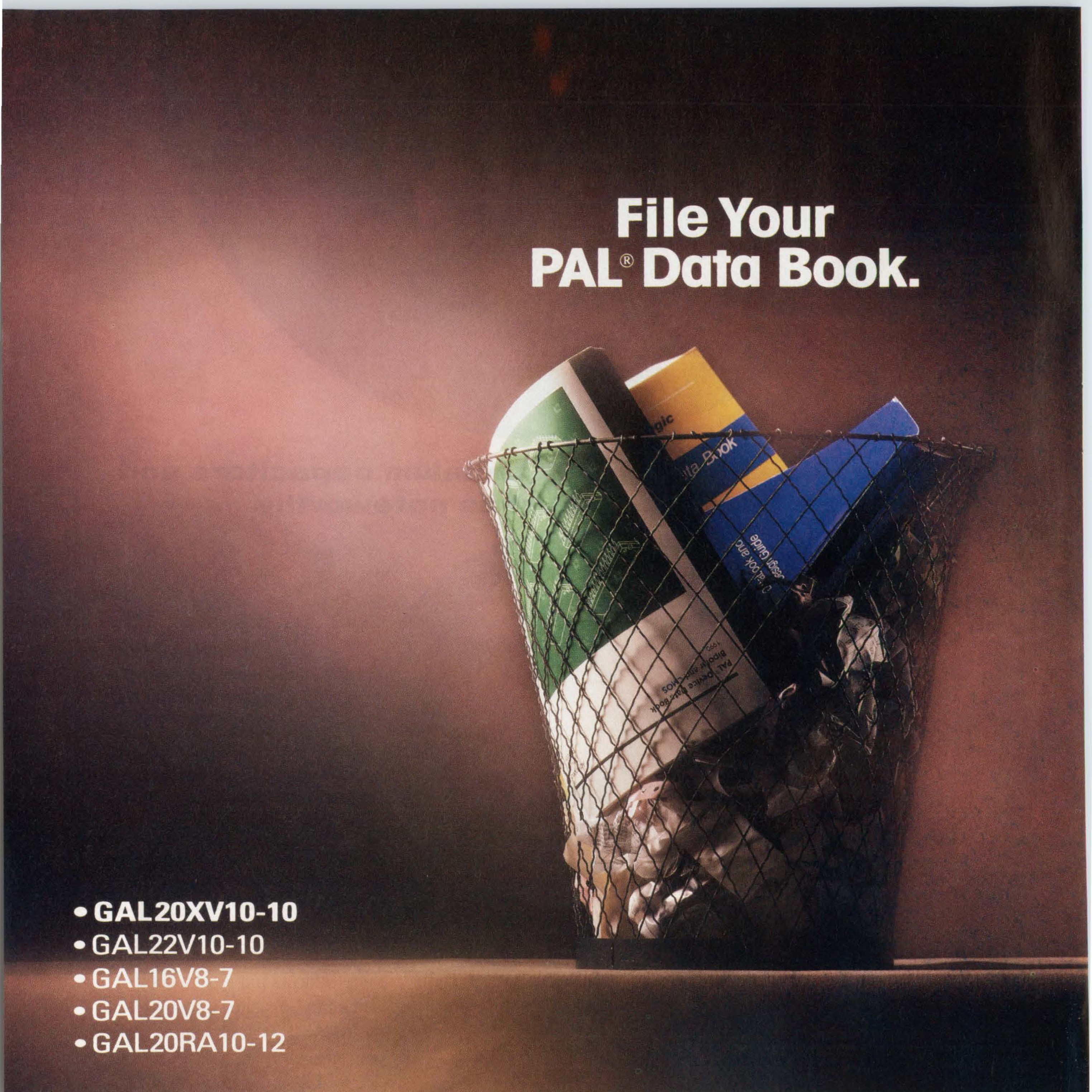
								
TAJ	TAZ	TAP/TAF	TAL	TAR	TMH	TMN	TMZ	TMM
0.1μF–220μF	0.1μF–100μF	0.1μF–330μF	0.1μF–150μF	0.1μF–68μF	0.1μF–22μF	0.1μF–33μF	0.1μF–47μF	.001μF–270μF
4–50V	4–50V	6.3–50V	6.3–50V	4–50V	2–20V	2–50V	2–50V	2–50V

CIRCLE 244 FOR U.S. RESPONSE

CIRCLE 245 FOR RESPONSE OUTSIDE THE U.S.



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bit color values for each of 256 addresses, the CLUT operates with the mask register to define multiple palettes and provide palette animation like a RAMDAC. In the color-index mode, the CLUT stores the color-lookup data and translates 8-bit source data into 24-bit RGB colors. If the encoder is connected in parallel with a RAMDAC in a VGA system, the 22190 CLUT can be loaded simultaneously with the output RAMDAC's CLUT. In GBR and RGB modes, the CLUT can supply gain and offset levels for PAL and NTSC systems. It can also be loaded with transfer functions that translate between CCIR (Consultative Committee for International Radio) and RGB data ranges, as well as between B-Y (blue-yellow), R-Y (red-yellow), and RGB data ranges.

In addition, CLUT-control signals make it possible for input pixel data to bypass the CLUT, which is useful in systems where chrominance and color data is available in a YUV format. CLUT bypassing can be on a pixel-by-pixel basis so that an additional level can be keyed (image combined). The 30 overlay colors in the CLUT aren't used when data is present in a YUV format. Combined with hardware and software keying, these features turn the 22190 into a layering engine that superimposes four digital sources into an encoded four-layer composite image.

The CLUT also plays a role in gamma correction—a correction factor that compensates for signal-path nonlinearities that occur in broadcast TV systems.

When operating with YC_bC_r formats, encoding a CCIR 601 signal requires gamma correction, which is usually 2.2 for NTSC and 2.8 for PAL. Gamma correction can be added to the RGB transfer equations loaded into the CLUT. The CLUT also has the ability to implement various special effects, such as contouring, quantization, and solarization.

Three Modes

The 22190 can operate in a master, genlock, or a slave mode. In the master and genlock modes, the encoder internally generates all timing and sync signals. It also provides horizontal- and vertical-sync signals along with pixel-data control signals to the frame-buffer interface. All horizontal-sync timing parameters are programmable, as are the duration and phase of the color-burst envelope *(Fig. 4)*. The 22070 video digitizer controls encoder timing in the encoder's genlock mode. In the slave mode, pixel-data control, horizontal-sync, and vertical-sync signals from external circuitry control the timing of lines and frames, and the area of the active picture.

The encoded video output comes from three 10-bit digital-to-analog converters operating at twice the pixel clock to simplify output-filter design. Each output (chrominance, luminance, and composite video) can drive an RS-170 signal level into a doubly-terminated 75-Ω video-transmission line. The composite-video output is fed by a video switch, which selects between the encoder's composite-video input from the genlock interface and the composite encoded pixel data on a pixel-by-pixel basis.

The 13-wire microprocessor interface is identical to that of the 22070 video digitizer. The 22190 encoder also includes a four-wire JTAG (IEEE 1149.1-1990) test interface port that provides access to all digital I/O data pins for component- and board-level testing. To verify that the analog video-signal chain is operating properly, the encoder can be instructed to generate standard 100-IRE (U.S. Institute of Radio Engineers) color bars or a 40-IRE modulated video ramp, independent of any pixel or video data input. Color bars also serve well as an output signal to measure system video accuracy. The 22190 is packaged in an 84-lead plastic chip carrier with J leads, and draws 200 mA from a 5-V supply.□

Price And Availability

In 1000-unit lots, the TMC22070 genlocking video digitizer costs $24.75 each, and the TMC22190 digital video encoder goes for $57.30 each. Both will be available in July.

TRW LSI Products Inc., P. O. Box 2472, La Jolla, Calif., 92038; Bill Bucklen, (619) 457-1000. CIRCLE 511

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Moderately	528
Slightly	529

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MULTIMEDIA MOVES FROM THE DRAWING BOARD TO TANGIBLE PRODUCTS

RICHARD NASS

THE TALKING IS OVER. WITH THE HELP OF DSP, MULTIMEDIA IS NOW SET TO TAKE OFF.

Multimedia, one of the hottest buzzwords in the industry for the last few years, has reached the point where it's now becoming a reality. The trend is being assisted by the inclusion of the digital-signal-processing concept to solve many hardware and software problems. These problems arise from the fact that though many standards have emerged and people have been designing multimedia products for a few years, there are just as many software and hardware inconsistencies to solve.

It's not surprising, then, that developers are searching for the right platform to develop for, while end users try to decide which platform to build upon. "It'll be very important for everyone to conform to standards," says Hugh Chang, product manager of Microsoft's Multimedia Systems Group. " Standards provide a consistent interface for the application developers so they don't have to learn many different interfaces."

From a designer's perspective, multimedia can be treated as two separate categories—audio and video. Video, though, isn't as suited for digitization as audio because of the tremendous amount of data it takes to represent an image. Also, putting still video into full motion at 30 frames/s gets extremely complex.

Available video hardware essentially consists of board-level video and window chips that allow users to open a "video window" in a VGA screen. The video board simply blocks out a window and plays an analog signal through the window. However, because the data isn't digitized, not much can be done other than starting and stopping it. Thus, it's difficult to integrate into another application.

The video side of multimedia is much less mature than the audio side because digital audio has been around for about ten years. Hence, a great deal of video-related innovation is arriving on the scene. To take advantage of that innovation, Microsoft Corp., Redmond, Wash., defined a standard command interface so that applications and hardware developers can communicate in a con-

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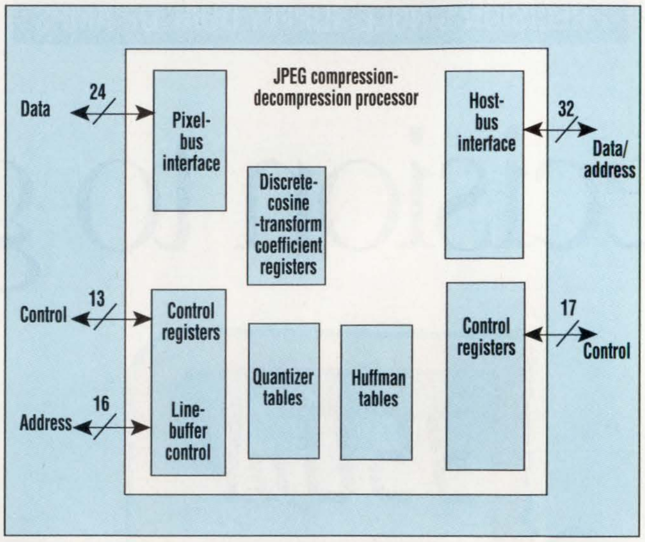
sistent way. The digital-video command set for the media-control interface defines standard functions required for digital-video devices. The command set is also employed by applications using digital video to call those devices. Many different digital video techniques are currently on the market or in development.

One of the standards is the Multimedia PC (MPC). To conform to the MPC standard, the video side only requires a video board with a SCSI interface and a CD-ROM to do animation (8-bit color graphics) with VGA graphics. The CD-ROM is needed to hold the massive amounts of data.



1. THE CL550 COPROCESSOR **developed by C-Cube Microsystems compresses and decompresses images according to the JPEG standard. It eliminates bandwidth bottlenecks associated with imaging by integrating functionality on-chip.**

The biggest constraint with a CD-ROM is its 1.5-Mbit/s transfer rate. The limiting factor is actually the CD-ROM itself, because the SCSI interface can operate at a much higher speed. To utilize full-motion video, the data-transfer rate must improve—there's simply too much data to be moved around. For example, when using 24-bit, true-color video with a resolution of 640 by 480 pixels, each frame in the presentation would occupy 7.4 Mbits of storage. Therefore, each second of video at 30 frames/s requires about 221 Mbits of storage capacity.

Compress The Data

Compression tackles the massive-data problem head-on. There are basically two types of compression: lossless and lossy. Lossless compression is used by the popular Stac chip and by the PKZIP software routine. It gives about a 2:1 compression ratio by replacing the strings of ones and zeros in the data with a 1- or 2-bit identifier. Then, it compresses the redundant data. In other words, it makes a table of the most-used characters and represents each by a 1- or 2-bit identifier. The least-used characters are given longer identifiers. This method allows single bits to represent long strings of data. However, all of the data can be retrieved upon decompression.

The two standard lossy algorithms come from the Joint Photographic Experts Group and the Motion Picture Experts Group (JPEG and MPEG). JPEG, recognized by the IEEE, started as a standard for color facsimile. It takes still images and compresses them for transmission, using primarily the discrete-cosine transform. An image is scanned and then broken up into 8-by-8-pixel blocks. The blocks are then compared and redundant data is removed. Like the lossless method, redundant data is put into a table that assigns certain bits to represent particular character strings. But now, redundant data is thrown away because full-color images involve too much data.

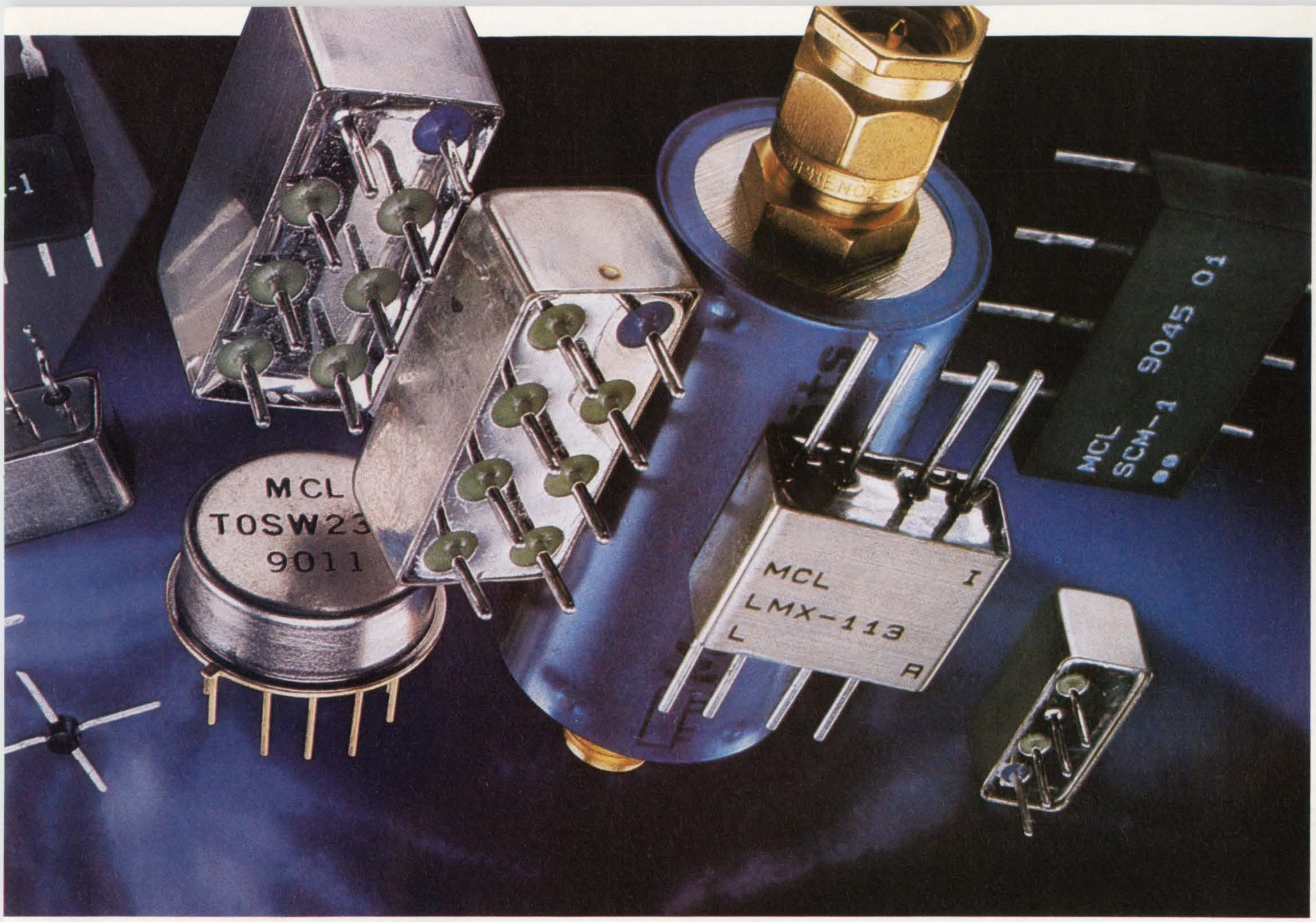
JPEG does intraframe compression, meaning one frame at a time. MPEG also does intraframe compression similar to JPEG, but with 16-by-16-pixel blocks. Its compression algorithm is slightly different, though, because takes those intraframes and makes interframes. By looking at a series of frames, redundant data is spotted and removed. Compression ratios as high as 150:1 can be achieved using MPEG. However, with compression ratios of about 30:1 or 40:1, artifacts (image deterioration) start to appear.

C-Cube Microsystems Inc., Milpitas, Calif., sells a single-chip JPEG coder/decoder (codec) that can perform motion-video JPEG compression at 30 frames/s. The CL550 lets users stream full-motion video from a hard disk *(Fig. 1)*. It doesn't offer interframe compression like MPEG, so the compression ratio runs about 30:1 for a decent-quality image. C-Cube also has a product for an MPEG image, where the data rate tends to be about 1.5 Mbits/s. It enables users to stream from a high-performance hard disk and get full-motion video over the AT bus.

Once the compression problem is solved, the bottlenecks become the bus and the storage medium. The AT bus can be used, but a local-bus implementation is probably more appropriate. The MPEG standard is designed to take motion video from a CD-ROM. JPEG is symmetrical, which means that the processing required for coding and encoding is about equal. Because MPEG is asymmetrical, it requires more power to compress because all of the differences in the frames must be calculated. Once the data is compressed, what remains is a data syntax that any standard decompression algorithm can read.

This year, chips will emerge that can handle full-motion MPEG video from a CD-ROM at 1.15 Mbits/s. As a result, MPEG audio can be added to the video. In effect, a digital audio-video playback system can be supplied with 228-kbit/s channels of audio. Though an image will be high in quality, it won't be a broadcast-quality image. Eventually, MPEG will show up in the broadcast market. But, rather than the 1.5-Mbit/s transfer rate, it'll take about 7 Mbits/s to get the needed resolution.

Rather than mix digital graphics with analog video, designers are moving toward a completely digitized solution. This is the next major step for multimedia, one that will probably be realized this year. The ultimate multimedia chip will handle both JPEG and MPEG, programmable to some degree, as well as the P-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9045 01

64 teleconferencing standard. JPEG will also appear in printers and copiers because of the amount of space it saves by compressing images.

IBM Corp., White Plains, N.Y., claims that the next-generation multimedia platform will have complete video capabilities. A form of the company's Action Media II Digital Video Interactive (DVI) card developed with Intel does full digital video, including capture and playback. IBM's multimedia platform, the Ultimedia 57, is built with a 386SLC processor, which is IBM's 20-MHz 386SX chip that adds an 8-kbyte cache memory to accelerate the system by about 80% over a typical 20-MHz 386SX. The system ships with 4 Mbytes of memory, a SCSI controller, a 160-Mbyte hard-disk drive, a CD-ROM XA drive, and XGA graphics. The CD-quality audio subsystem can handle 8- and 16-bit playback.

Microsoft offers a Multimedia Development kit that supplies three key components for software developers: C libraries, a multimedia Viewer, and data-preparation tools. The Viewer is an authoring tool that lets developers who aren't programmers take advantage of the multimedia functionality under Windows. The data-preparation tools come with sound and images built right in. The Windows 3.1 device development kit contains all of the information hardware developers need to create device drivers that exploit multimedia's functionality.

One challenge brought on by multimedia is that it exercises the hardware in new ways. Because so much data is used in an application, it's not just loaded into memory and executed—it's actually streamed in from the CD-ROM drive. Data is streamed in from the drive while other data is processed in the audio subsystem or by the CPU. Data is also sent to the output device, whether it's a display or speakers. "It's sort of a stress test for your hardware, one that's never been experienced before," says Chang.

Digital-signal processors, which recently migrated into PCs in various forms, may very well take multimedia platforms to a higher plateau, especially if DSP extensions are added to the MPC specification. Already, some palmtop PCs employ digital-signal processors and voice codecs for voice annotation, as well as for high-speed fax-data modems. DSP chips could be used to accelerate JPEG algorithms for image post processing as well as speech and text recognition.

The Signal Computing strategy of Analog Devices Inc., Norwood, Mass., is based on DSP. The concept is defined as an architecture, including a layered software environment. This allows third parties to write algorithm software for such applications as MPEG audio or video compression, as well as speech coding and recognition. Third parties supply the actual compression technology, totally in software.

THE BUILDING BLOCKS

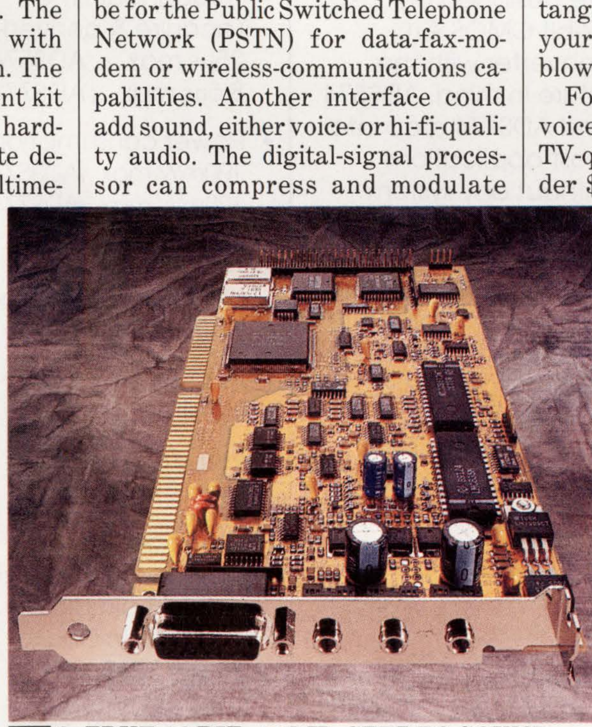
From an architectural standpoint, Signal Computing supplies some basic building blocks—the digital-signal processor and the bus interface for either a peripheral bus or a local bus. One interface to the bus might be for the Public Switched Telephone Network (PSTN) for data-fax-modem or wireless-communications capabilities. Another interface could add sound, either voice- or hi-fi-quality audio. The digital-signal processor can compress and modulate MPEG or JPEG algorithms in real time. And if the system contains a telephone interface, the data can be shipped in a full-duplex mode. This supplies video-conferencing capabilities, albeit without the highest-quality levels. Services like the Integrated Services Digital Network (ISDN) could then be used to supply the high quality if needed.

"Analog Devices is taking the coprocessing concept into the mainstream IBM-compatible market in a manner that's completely different from anyone else," says John Croteau, manager of strategy and planning at Analog Devices. "Designers want highly programmable 32-bit floating-point processors that can implement entire algorithms and also run a high-performance, real-time operating system. Consequently, you end up with system costs that are too high. When you go to 32 bits with a real-time operating system and large amounts of data, it puts a heavy burden on the digital-signal processor."

The Analog Devices alternative employs a 16-bit DSP chip. Other functions are partitioned into tightly coupled chip sets. "If you start with tangible functions like fax-modems, your system software won't be overblown," notes Croteau.

For under \$200, users could get voice-quality and PSTN interfaces. TV-quality audio can be had for under \$300. In the 16-bit multitasking PC business, functionality is defined by the I/O media and the baseline function, such as a telephone-network interface. For another \$200, a voice-quality interface chip could be added; an extra \$50 to \$100 pushes that to CD-quality levels. Now, the integrated system includes a data-fax modem, an answering machine, voice-mail functionality, MPEG audio, music synthesis, and speech and text recognition.

Texas Instruments Inc., Dallas, says that it wants to take the conventional defi&ition of multimedia one step further by letting all of the system's elements, such as audio, video, and te-



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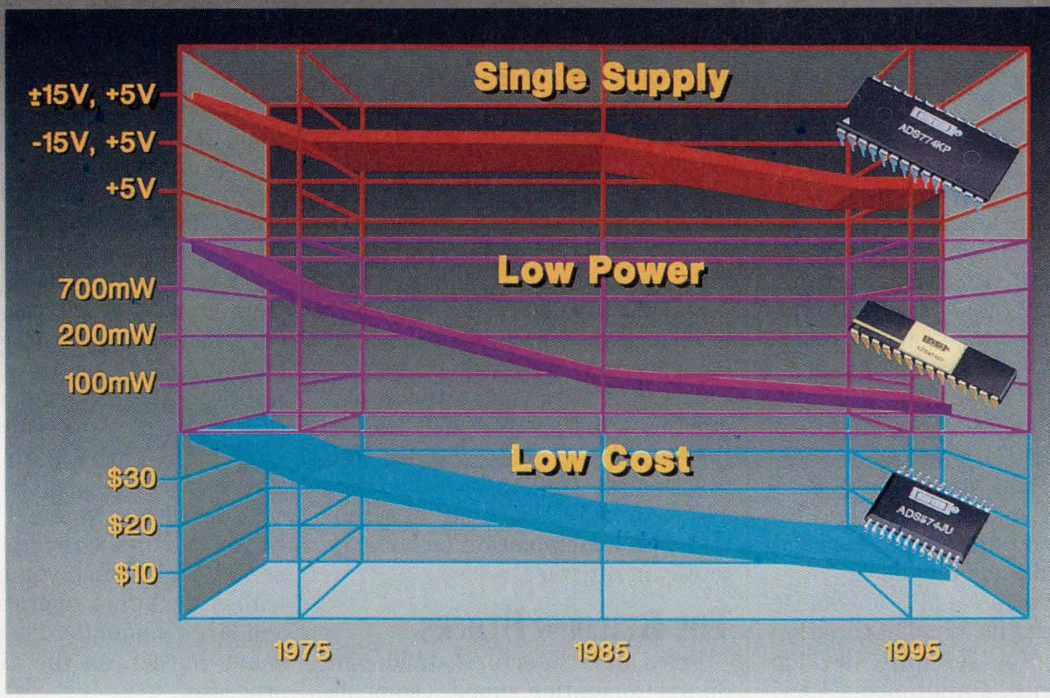

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lephony functions, run concurrently. For example, a system should have the ability to display an image whether its processing or having a fax run in the background.

"Over and above the new technology, the need to combine concurrent functionality will be important," says Rick Rinehart, TI's DSP multimedia marketing manager. "The heart of this system is a high-performance DSP chip. Rather than have individual pieces of hardware out there, such as a fax board, an image-compression board, and a voice-recognition board, it'll all be done in DSP software."

Tie DSP To Software

TI dubs the DSP chip's software functions as "virtual-hardware tasks." To add multitasking, the DSP subsystem will run with a real-time multitasking operating system that can concurrently process the virtual-hardware tasks. But there's got to be a way to integrate this subsystem into the standards that already exist, including Windows 3.1 and OS/2. Underlying software should tie the operating system to the embedded DSP hardware. TI's DSP manager is a piece of software that marries the underlying DSP technology with the host operating system to make it easier for Windows and OS/2 application engineers to write application-specific device drivers for underlying DSP hardware.

"If multimedia is really synonymous with multitasking, then the host-based application itself must be a multitasking operation. Consequently, DOS, a unitasking environment, doesn't lend itself to multimedia," says Rinehart. "Windows, in many respects, is a multitasking environment, although not from a purist's viewpoint. In this case, OS/2 is clearly a differentiator. OS/2 is a clear multitasking preemptive OS." Hence, IBM created the Ultimedia line and its own standard.

"In general, the primary hurdle in multimedia is software," remarks Croteau. "Everybody tends to focus on the hardware, but the problem is often software. PC makers look for a useful solution and still don't incorporate the hardware components because there's no application software." This brings up the chicken-and-the-egg theory. The hardware won't proliferate until the software's available, and vice versa. "The key thing that will ignite multimedia is when hardware costs for a useful multimedia function cross the end-user price threshold of $250. Until that happens, independent software vendors won't develop applications."

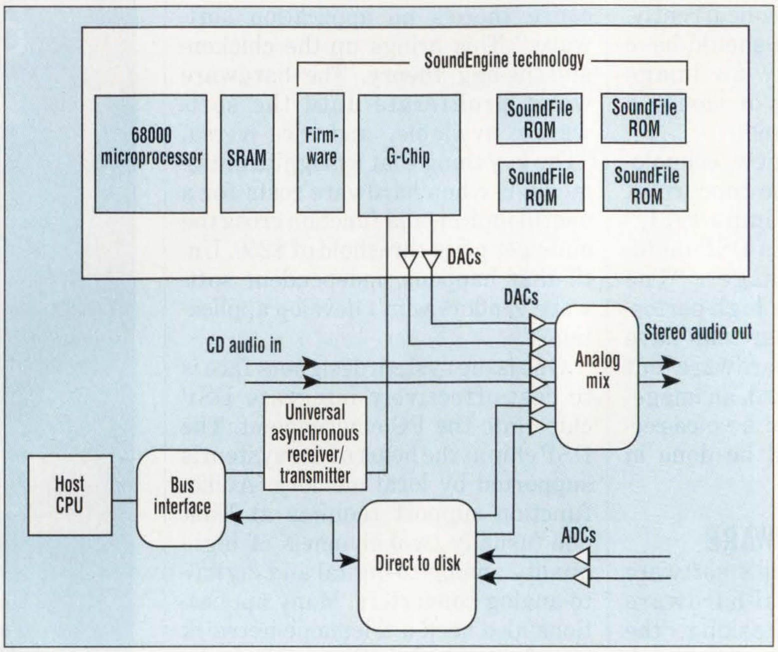
One issue system designers face is to cost-effectively integrate DSP chips into the PC environment. The DSP chip at the heart of the system is supported by local memory. Audio-function support requires at least one (usually two) channels of high-quality analog-to-digital and digital-to-analog converters. Many applications also need a telephone-network interface, which is the analog isolation transformer that links with the telephone network—a common feature among modems and faxes.

TI and IBM allied to develop advanced DSP technology products that address the multimedia market. The first product is the Mwave subsystem, which consists of an optimized DSP chip and a real-time multitasking operating system. Associated with that subsystem is a set of virtual-hardware tasks that let users emulate modems and faxes; perform voice recognition, music compression and playback, and image compression; and convert text to speech. To integrate this into the Windows and OS/2 environments, the DSP Manager ties everything together, keeping the applications compliant with the MPC specification.

When these DSP-related functions migrate to the motherboard, little is eliminated. The need for local memory, or the amount of it, doesn't go away. Furthermore, the digital-signal processor needs its zero-wait-state SRAM to run in real-time. But, even with zero-wait-state SRAM sitting on the host side, the host may not have access to it under all circumstances. This eliminates running the system in real time. Consequently, some local memory is needed.

To keep cost down, designers try to use as little SRAM as possible without affecting the real-time multitasking capability. Some functions, such as speech recognition, require lots of memory. But, if the memory isn't used to its full potential, it's not a cost-effective solution. Thus, there's a trade-off between the caching scheme used to get data onto the subsystem and how many words are recognized in real time. The trade-off, though, is application specific.

Integrating more functionality into the DSP chip will grow in importance as multimedia matures. In the meantime, designers should look for the DSP solution that offers the most system-level integration. For example, multitasking implies that lots of serial data is processed concurrently, requiring more serial interfaces. Whether those are implemented internally or externally to the digital-signal processor could determine the cost of the solution and the size of the subsystem. Mwave isn't a general-purpose digital-signal processor. It's designed for the high serial-I/O demands that a multimedia system places on the DSP chip.



3. THE SOUNDENGINE TECHNOLOGY, built around the G-Chip from E-mu Systems, supplies an integrated musical-instrument digital interface (MIDI) subsystem. The sound module can be combined with a user interface, a host CPU, a MIDI keyboard, a power amplifier, and a speaker system.

Many multimedia applications require real-time signal handling. Quite often, the audio and video signals must be processed on the fly at the rate in which they're received. IBM uses a TI family of DSP chips in its Uitimedia systems. In addition, there's a similar family of TI DSP chips on IBM's audio-playback-capture adapter card.

IBM's original architecture was fairly general purpose in nature, but had some unique features that include its programmability. Most DSP devices perform very specific functions, such as medical imaging, where they just process large amounts of the same type of data. Because IBM's operating system was multitasking oriented, it could perform various functions simultaneously and manage its own resources.

The DSP chip's broad applicability to multimedia-type applications pushed IBM to look for third parties with similar ideas. An alliance was formed with TI and Intermetrix Inc., Cambridge, Mass., resulting in a three-part developer's environment: the silicon (the DSP IC) from TI, the operating system that has built-in task managers and program interfaces (and should eventually plug into Windows and OS/2) from IBM, and the tools from Intermetrix.

The complete toolkit has a number of abilities, such as emulating a modem or a fax machine in software, so communication hardware isn't needed. Because it can emulate an oscilloscope by visually displaying sound inputs, voice recognition can be done. It does fast JPEG decompression so that JPEG-compressed images can be taken from the hard disk, buffered through the DSP chip, and displayed on the screen, all in just over 1 second (as opposed to the typical 5 or 6 seconds). On top of that, these functions can all be implemented simultaneously in a preemptive multitasking mode that manages the resources. IBM says that all of this technology should be available this year.

AT&T Microelectronics, Berkeley Heights, N.J., puts forth three products to serve the multimedia market — the DSP3210 floating-point processor, the host - independent real-time Visual Caching Operating System (VCOS), and the VCOS Multimedia Desktop (VMD) module library. VMD supplies real-time DSP algorithms for audio compression and JPEG image encoding and decoding, as well as application programming interfaces (APIs) to extend algorithm usage to support standards like MPC. Under MPC, for example, music synthesis is defined as a component of a platform. Using the 3210, it's possible to implement music synthesis, a musical-instrument digital interface (MIDI), and other functions. By linking these applications into standards like MPC, application developers are assured that the applications operate across all standard platforms.

DESIGNER'S AID

To help designers build systems based on AT&T's 3210 DSP processor and VCOS, Ariel Corp., Highland Park, N.J., offers the MP3210 development platform that features either one or two 3210 chips. The board fits in one 16-bit PC I/O slot, supporting ISA data transfers to the host at up to 3 Mbytes/s. To support multiprocessor applications, the board also supplies a buffered, nonmultiplexed, memory-mapped local bus that can link up to eight DSP chips on four MP3210 boards.

The algorithms are executed on the DSP chip and their flow is managed through VCOS, which resides under DOS, Apple's MAC-OS, or Commodore's Amiga. By using VCOS as an extension to the platform's operating system, the algo-

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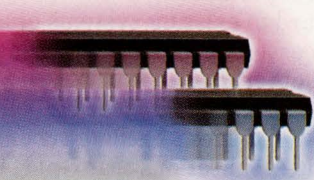

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rithms can multitask on the 3210. VCOS lets the algorithms reside in system memory, so local DSP memory isn't needed. The DSP chip can then be implemented in one of two hardware platforms, either as an add-in card to existing systems or as a coprocessor to the host processor on the motherboard.

The 3210 is a 32-bit floating-point device. VCOS uses a caching scheme to execute applications that reside in the PC's local system memory. So if the 3210 resides on a motherboard with a 32-bit bus, application execution is done very effectively. If it's implemented on an add-in card, it works best in a 32-bit EISA-based system because local system memory can be bus mastered. There's a bandwidth penalty on 16-bit ISA systems: While it doesn't prevent operation, it limits the number of concurrent applications that can run on the DSP chip.

By year's end, we could see this problem solved with a local-bus implementation. Though AT&T will continue to focus on chip development to make faster and lower-power parts to address the notebook markets, it'll also add more algorithms to the VCOS library. The first version of the library will support JPEG image coding and decoding, MPEG audio coding and decoding, sub-band coding, telephone-line interface functions, and sample-rate conversion. Some future functions include speech recognition and synthesis, caller ID, acoustic echo cancellation, and extensions to fit the MPC standard. Handwriting and voice recognition should come later this year.

"What we've found in talking to PC manufacturers is that there's some uncertainty as to what shape multimedia is going to take, where it will succeed and where it will fail, as multimedia defines itself. Right now, different people have different definitions of what multimedia is," says Denis Reginbald, manager of product marketing, multimedia, at AT&T. "We've lowered the risk by letting designers implement functions that they already work with." If the hardware is at first used for a fax or modem, the hardware can be reused for audio, speech, MPC, or other multimedia functions.

HEAR THE AUDIO

A good number of the multimedia hardware developments began on the audio side. "We see multimedia as a big puzzle that's fairly complex and audio is the first piece to that puzzle. So, instead of trying to put together all the pieces at once, we'll do them one at a time," says Satish Gupta, vice-president of strategic product development at Media Vision, Fremont, Calif. "We're doing audio first. Later we'll get into video and the rest of the pieces." The company's latest product, Pro Audio 16, is an audio subsystem board with interfaces to the host processor, the bus, and

Windows *(Fig. 2)*. The board delivers 44-kHz 16-bit stereo samples.

One problem designers confront in designing multimedia products is combining analog and digital circuitry on one board. The Media Vision board has reverse planes—the ground and voltage planes are outside the analog-signal planes, and the digital planes are inside. Consequently, noise from the digital area doesn't emanate out, creating a high degree of isolation between both planes. The company is trying to further reduce the noise problem by capturing as much of the analog circuitry as possible in ICs.

The Pro Audio board is split into five sections: An audio controller that connects to the PC, a 16-bit codec with a DAC and an ADC, a mixer that takes the codec I/O and lets the host control how the channels are mixed, an interface to I/O devices like speakers and microphones, and a coprocessor that attaches to the audio control. The coprocessor, which is buried into the card, isn't a shared resource.

Most audio boards that use 8 bits will soon go to 16 bits because of the better dynamic range. Another forthcoming change is to use compressed audio. To the hardware developer, this means employing DACs to accommodate the 16-bit samples. It may also signal a move to DSP ICs for the compression. Initially, the audio portion of multimedia will probably advance quicker than the video portion because it's cheaper. But the largest base of applications will be for combined audio and video.

By using audio compression algorithms such as MPEG, compression ratios can range from 4:1 (with no loss of quality) to as high as 64:1, while a reasonable amount of quality is still maintained. To get such high compression ratios in full stereo would probably require a DSP chip that operates in the 16-MIPS range. This type of operation could be off-loaded from the host using a DSP. Presently, the trend is to compromise quality somewhat if it will make for a big impact in compression. As full-motion video technology becomes more affordable, dedicated coprocessors will be found working in concert with the multitasking DSP IC to implement full-motion video with audio.

The ability to compress audio data is significant. Even though a CD-ROM holds a large amount of data (650 Mbytes), the combination of sound and image data can take up lots of memory space.

Compressing the audio is a combination hardware-software issue. Parts of the compression, especially the more sophisticated audio-compression techniques, require additional horsepower. And the compression routines are typically more compute-intensive than traditional data-compression techniques.

The typical audio board specified by the MPC has three components. One is a waveform subsystem that's used for digitized audio, which should be able to record 11-kHz, 8-bit samples at a minimum playback of 11- and 22-kHz, 8-bit signals. The SoundBlaster Pro developed by Creative Labs Inc., Santa Clara, Calif., can handle such 8-bit signals.

At 22 kHz, audio should be acceptable for most applications. To put it in perspective, 44-kHz 16-bit samples is what a typical home CD audio player puts out. An FM radio operates at about 20 kHz and a telephone works at about 3 kHz.

Maximizing MIDI

The second audio-board component is the MIDI subsystem that supports synthesized audio. The MIDI specification requires at least six simultaneous melodic voices and two simultaneous percussion voices. The third and final part of the audio subsystem is an analog mixer that takes the waveform from the digitized source, the MIDI source, and the CD-ROM drive, and merges them to produce one output. Windows 3.1 supports that functionality as well as all of the multimedia APIs in Microsoft's Multimedia Extensions 1.0. This signifies that there are device-driver layers, so if a user purchased an audio card with those three subsystems and the card manufacturer had created a Windows driver, there wouldn't be any conflict.

Audio and video should appear on the motherboard within three years. A local bus can be implemented across boards, not just on the motherboard. "Hopefully, there will be a standard local bus," says Jim Anderson, marketing director at C-Cube. "What prevents it from going on the motherboard now is that there are too many standards. There's a still-frame standard, a motion standard, a teleconferencing standard, etc."

But not everyone agrees that a local bus is the answer. Hugh Dyar, manager of industry development at IBM notes, "I don't think implementing a local bus is the issue. You can transmit data around a PC a lot faster than the software can handle it. You really need hardware-assisted jumps to accelerate the software's ability to handle the data. The real problems arise when you start trying to manipulate and edit the data."

Many of today's discussions involve standards for audio and CD-ROM. Audio can be broken into three components: the audio coming directly from the CD-ROM, typically in an analog form; digitized audio; and a form of MIDI-controlled synthesis, which is currently in the standardization process. MIDI is part of the MPC specification, and can help author multimedia applications. Users want MIDI to create music. But, it's also desired in the playback platforms so authors have access to MIDI-synthesis in their systems.

E-mu Systems, Scotts Valley, Calif., designed an application-specific digital-signal processor, the G-Chip, that was developed specifically for reconstructing the recorded sounds of the company's library. Using the G-Chip, the sounds can be played back 32 at a time. The MPC specification only requires 24 voices. This 32-voice playback is important to anyone trying to create music because it offers a full, rich sound. In addition, the G-Chip lets users create unique sounds in real time by changing pitch or amplitude or by altering the mixing of voices as the sound is being played back.

E-mu also offers firmware (software drivers) to interpret MIDI. The company sells the firmware, as well as the G-Chip and the sound libraries, in a kit called the SoundEngine *(Fig. 3)*. The kit contains 4 Mbytes of ROM, the G-Chip processor, and a license to redistribute the firmware. The company also builds music synthesizers built around a technique called sample-playback synthesis. Sample playback is an attempt to get high-quality realistic sound as compared to other synthesis techniques like FM synthesis, which is primarily used for personal-computer games.

In the music world, MIDI controls notes by turning them on and off, changing their volume, etc. It can also control which voice is playing. Bill Snow, manager of business development at E-mu says, "We think that the computer guys can benefit from our technology, not only because it offers 400:1 data compression, but we're also pushing MIDI as a way to get interactivity at the playback platform. You can do things with MIDI that you just can't do

playing a CD back, such as changing the orchestration or the speed."

There are also issues concerning the audio sources. In many cases, the audio signals are coming from an asynchronous source. If the data is streamed from a CD-ROM and mixed with an asynchronous voice input, for example, the two can't be synchronized. It's difficult to sync to any source if it's a data stream, because synchronizing typically involves a phase-locked loop (PLL). When dealing with high-quality audio, the PLLs are typically somewhat jittery since audio has a relatively high bandwidth.

For multimedia to advance, CD-ROM technology will have to keep pace. The MPC specification requires an access time of 1 second from the CD-ROM, and that's okay for some reference type of applications. But most CD-ROMs on the market have access times in the range of 330 to 380 ms, suiting them more toward interactive applications. Access time is how long it takes to complete half of one full rotation on the drive, which is necessary to access the data. Once the data is streaming from the drive, it comes in at about 150 kbits/s.

The CDU-561 drive, developed by Sony Corp., Park Ridge, N.J., doubles the typical CD-ROM transfer rate by doubling the drive's rotational speed. The rotational speed of the media is based on a constant linear velocity (CLV), meaning that the drive always sees the same number of sectors/s, typically 75 blocks of information. With each block containing 2 kbytes, a total of 150 kbytes/s can be transferred. Because of the CLV, the rotational speed varies, depending on which part of the disk is being read. Typically, CD-ROM speed ranges from 200 to 500 rpms, and 400 to 1000 rpms for the CDU-561. In the double-speed mode, the drive's access time is below 300 ms.

Portables, Too

Most multimedia hardware manufacturers agree that power consumption will be a critical issue. Industry trackers say that the largest growth in the PC market will come from portables, whether they're laptops, notebooks, or palmtops. Therefore, for multimedia to be viable on the desktop, users must be able to take the same applications on the road. For this reason, power consumption of multimedia hardware is critical. The goal of system makers is to integrate audio, video, and communications into DSP cores, and migrate that functionality to 3.3 V. To that end, AT&T will offer a 3.3-V version of its 3210 DSP chip. □

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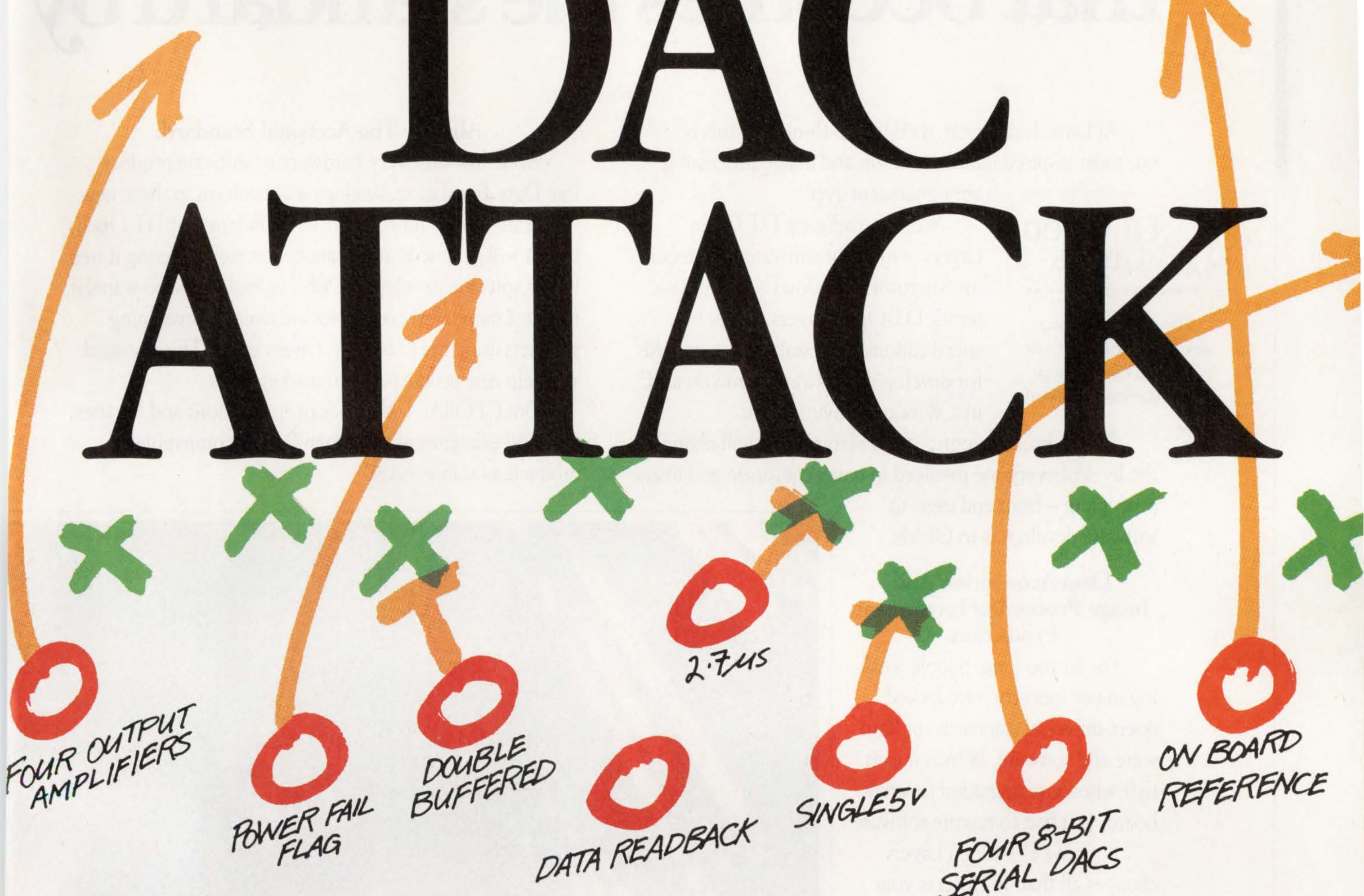

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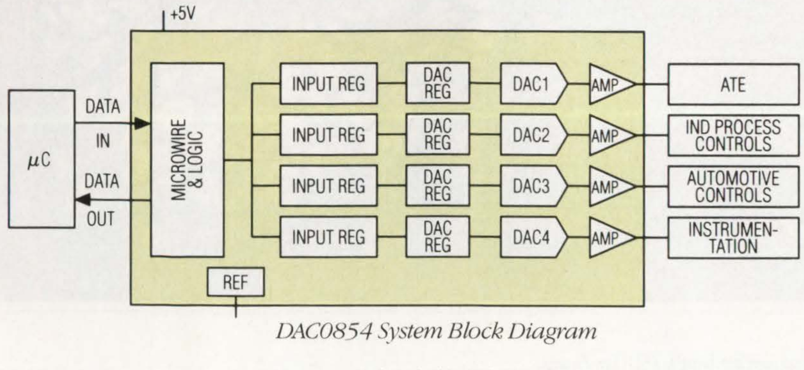

DAC0854 System Block Diagram

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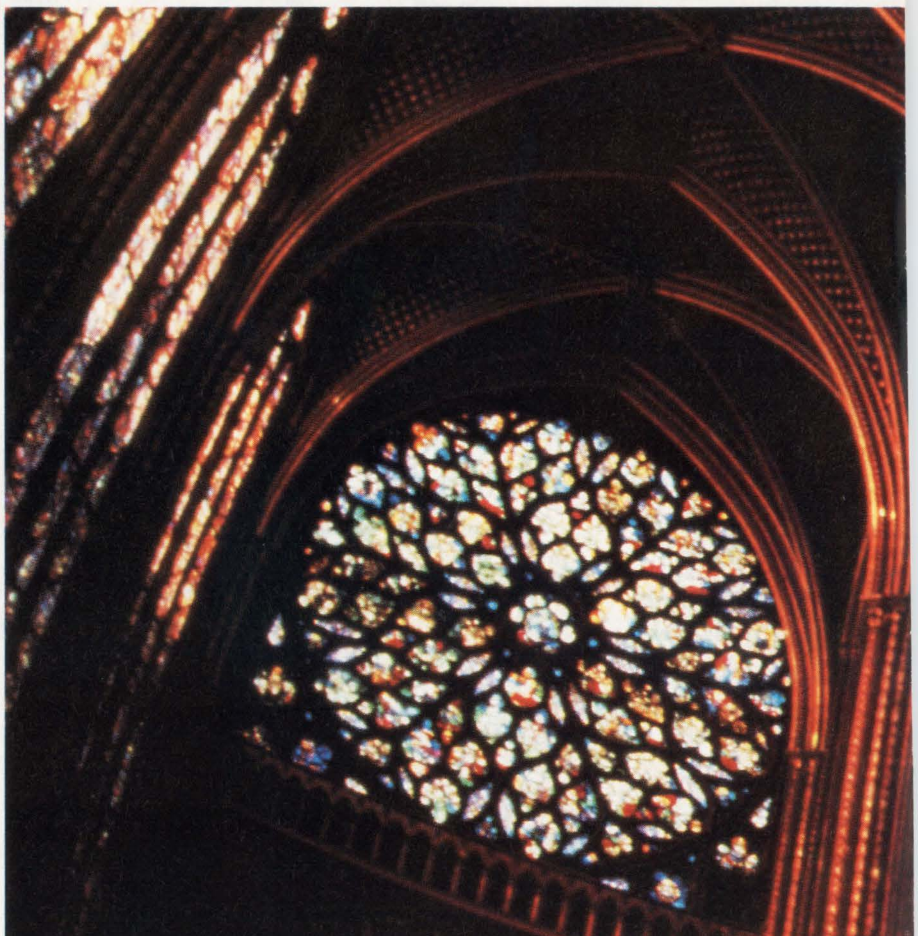

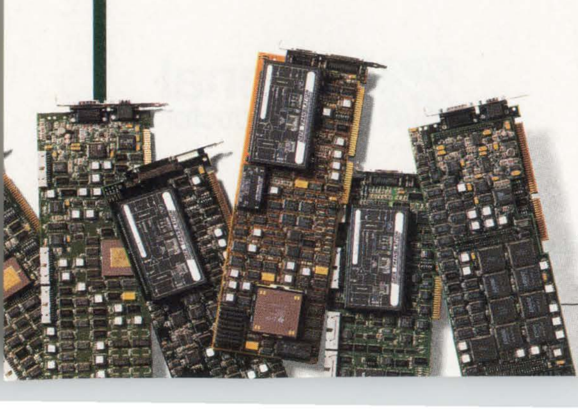

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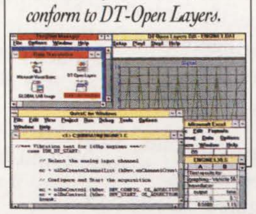

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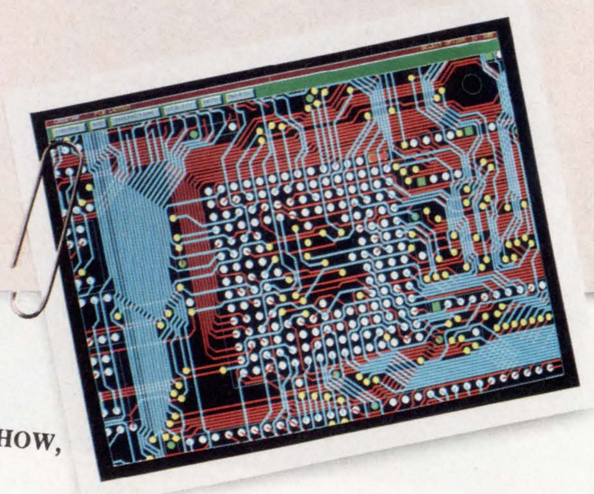

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MAINTAIN SIGNAL INTEGRITY AT HIGH DIGITAL SPEEDS

FAST DIGITAL DESIGNS START TO TAKE ON THE CHARACTERISTICS, AS WELL AS THE PROBLEMS, OF ANALOG CIRCUITS.

YONG-IN S. SHIN
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Increasing operating frequencies have thrust signal integrity in digital systems to the forefront as a critical design criterion. At high frequencies, digital designers must consider the analog nature of signals formerly treated only as ones and zeros. And the combination of different types of logic in bipolar, CMOS, or biCMOS devices is making it more difficult to achieve tight timing control, clean interface signals, and needed tolerances for interface skew in and out of the ICs.

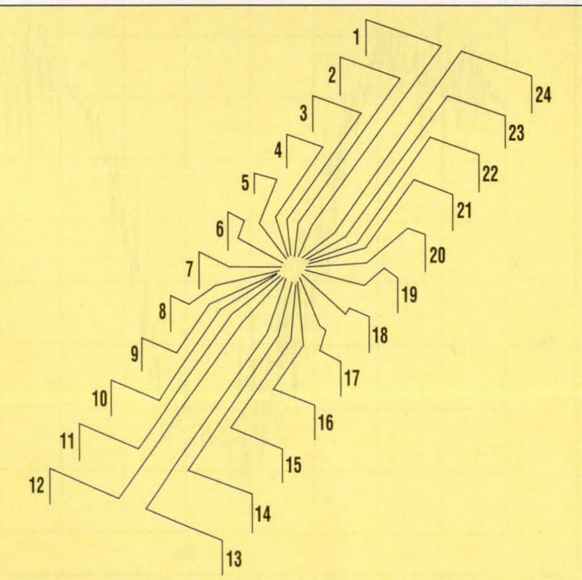
Designers of high-frequency digital systems must look out for ground bounce, setup and hold-time violations, reflections, minimum-pulse-width violations, signal race conditions, and metastability problems. They must also consider problems with interfacing to long and short critical paths and skewing between devices or cells.

This discussion concentrates on system noise and how designers can analyze the effects of noise on signal integrity. Included are experimental data on IC package inductance, transmission-line effects, input noise sensitivity, and detection of output glitches caused by simultaneous switching. Ways to minimize system noise are also covered.

There are several main sources of noise in digital systems, particularly TTL-based systems. For instance, the standard TTL threshold voltage is traditionally the forward voltage of two pin diodes, which is about 1.5 V at room temperature, while the operating power supply is 5 V ±10%. This standard creates a lower noise margin in the low state than in the high state. As a result, ground noise causes more problems than V_{CC} noise and must be more tightly controlled in TTL systems. To avoid these kinds of problems, designers should create good ground planes and provide special features on the ground pins.

Another important factor is the signal path's transmission-line characteristics. At high frequencies, a digital signal path becomes a complex LCR circuit. Charging and

Pin number	Self-inductance	Capacitance
1	15.10 nH	1.86 pF
2	12.20 nH	1.70 pF
3	9.54 nH	1.29 pF
4	7.44 nH	0.95 pF
5	5.31 nH	0.61 pF
6	3.73 nH	0.43 pF
7	3.41 nH	0.43 pF
8	4.66 nH	0.61 pF
9	6.95 nH	0.95 pF
10	8.96 nH	1.29 pF
11	11.70 nH	1.70 pF
12	14.50 nH	1.86 pF
13	14.50 nH	1.86 pF
14	11.70 nH	1.70 pF
15	8.96 nH	1.29 pF
16	6.95 nH	0.95 pF
17	4.66 nH	0.61 pF
18	3.41 nH	0.43 pF
19	3.73 nH	0.43 pF
20	5.31 nH	0.61 pF
21	7.44 nH	0.95 pF
22	9.54 nH	1.29 pF
23	12.20 nH	1.70 pF
24	15.10 nH	1.86 pF



1. THE LEADS TO THE CORNER PINS of a 24-pin, 300-mil DIP are about four to five times longer than those for the center pins. This disparity causes time skews between signals, and the higher inductance of the longer leads can create unacceptable ground bounce.

discharging energy in such circuits creates line noise with a resonant frequency and a certain damping factor. Even the IC package becomes an LCR transmission line. In fact, the ground path's inductance in the package is a main source of ground noise, especially when multiple outputs are switched simultaneously.

A line driver output that switches states can cause problems whether outputs are in-phase or out-of-phase. Similar problems exist when multiple outputs go in or out of the three-state in-phase or out-of-phase. This package-induced ground bounce can cause power-supply line noise, reduced speeds, loss of stored data, output oscillations, metastability, and other problems.

Dynamic currents are also a significant noise source. As speed increases, TTL logic's high voltage swing (3 V for bipolar, rail-to-rail for CMOS) creates a high charging and discharging transmission-line dynamic current, –C × dv/dt. Because transistors operate as on-off switches, all ICs also create a dynamic current, di/dt, which charges and discharges capacitive loads. And as this dynamic current goes through inductances, it generates an inductive voltage, L × di/dt. Because they operate with differential common-mode logic, ECL circuits are less sensitive than TTL circuits to dynamic currents.

Designers must also match impedances between the driver, transmission line, and termination in order to avoid reflections. Otherwise, reflected signals can combine with ground bounce created by the IC package and the pc board's ground inductances to cause problems like electrical overstresses, glitches, oscillations, latch-up, and even electromagnetic interference.

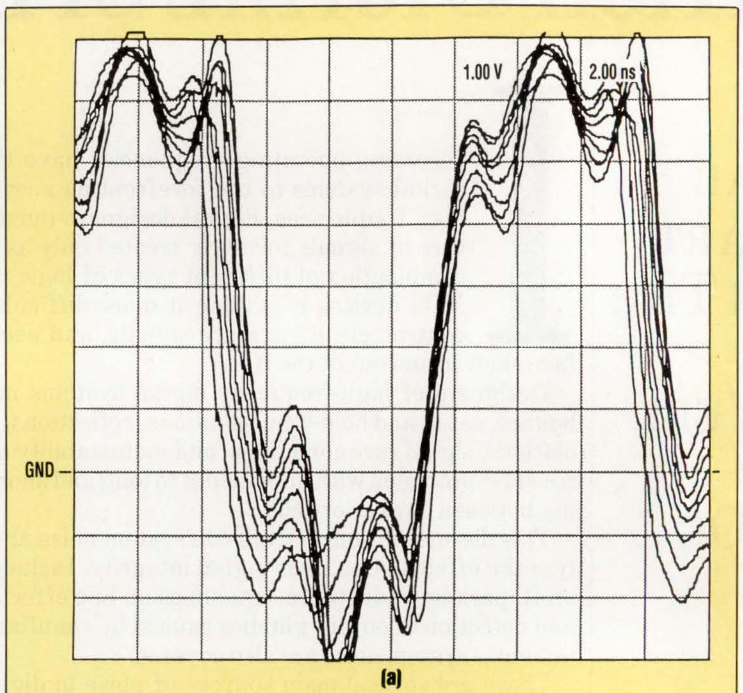
Crosstalk is another source of noise in high-speed digital circuits. Crosstalk is already a problem, as pc-board traces become thinner and denser. High dynamic currents caused by fast operating speeds worsen the problem. Capacitive coupling creates current crosstalk, and inductive coupling causes voltage crosstalk.

Other noise sources include bus contention, improper live insertion, metastability, skew on the clock drivers, overloading, inadequate decoupling, and insufficient power-supply control. Some of these sources can trigger today's faster transistors, causing functional, oscillatory, and other problems.

At high frequencies, designers must also consider ohmic loss, dielectric loss, and skin effects. Long signal paths can cause ohmic and dielectric losses. Skin effect losses are frequency dependent.

Of the three circuit elements in digital systems, inductance plays a major role in generating noise in a high-frequency, high-current system. Basically, two types of inductance are involved: self-inductance and mutual inductance.

In an IC, ground bounce is caused by the induced voltage, L × di/dt, where L is mainly the leadframe self-inductance and di/dt is the dynamic current rate. As noted earlier, the dynamic current, and therefore the induced voltage, rise as



2. IN TESTS WHERE ALL EIGHT outputs were switched, a 74ABT245 created skew and under- and over-shoot problems (a). In the same tests with a 74FCT245, all eight outputs oscillated (b). Probing occurred at the end of an unterminated 50-Ω, 12-in. cable.

the circuit's current drive capability and speed rise.

The self-inductance of a rectangular wire of length l and cross-section B × C is:

$$L = (0.002)(l)\ln[2l/(B+C)] + 1/2\} \quad (1)$$

Thus, the major contributor to self-inductance is the wire length, with the cross-section playing a smaller role. As a result, the inductances of package leads vary significantly depending on the location *(Fig. 1)*.

Differences Create Skew

These differences in inductance between the package pins also cause timing skew. So the type of package used can be important in high-frequency designs. For instance, the maximum difference in inductance between any two pins in a 24-pin DIP is about 11 nH, while the maximum difference in a 52-pin PQFP is about 1 nH.

For this reason, some of the newer line drivers, such as the MB (Multibyte) and FB (Futurebus+) product families, are packaged in PQFPs instead of double in-line (DIL) packages.

Mutual inductance is caused by the inductive coupling of the electric field's flux. As packages shrink and pc-board layouts get denser, mutual inductance becomes more of a problem. This inductance can be calculated by:

$$M = (0.002)(l)[(\ln 2)(l/d) - \ln K - 1 + d/l - (d/2l)^2] \quad (2)$$

where l is the parallel length, d is the distance, and the K factor depends on the medium between the two conductors.

Mutual inductance can be negative or positive, depending on the direction of the current. Designers can thus minimize total inductance by arranging current flow in the pins and traces to create a negative mutual impedance that cancels some of the self-impedance.

Unfortunately, inductance wasn't considered when the TTL device pin configurations were set, so the ground and V_{CC} pins are in the corners, where they have the highest self-inductance and least advantage from mutual inductance.

Other circuit elements must also be considered. The resistance of board traces, soldering joints, sockets, and connectors helps to dampen noise amplitude. But too high a resistance can cause unacceptable RC time-constant delays or static voltage problems created by IR drops. Designers should also account for accumulated load capacitances—such as IC package, via, edge-connector, and socket capacitance—in the transmission-line impedance. It also helps to know the pc board's dielectric constant because designers can then determine the line capacitance between layers and traces.

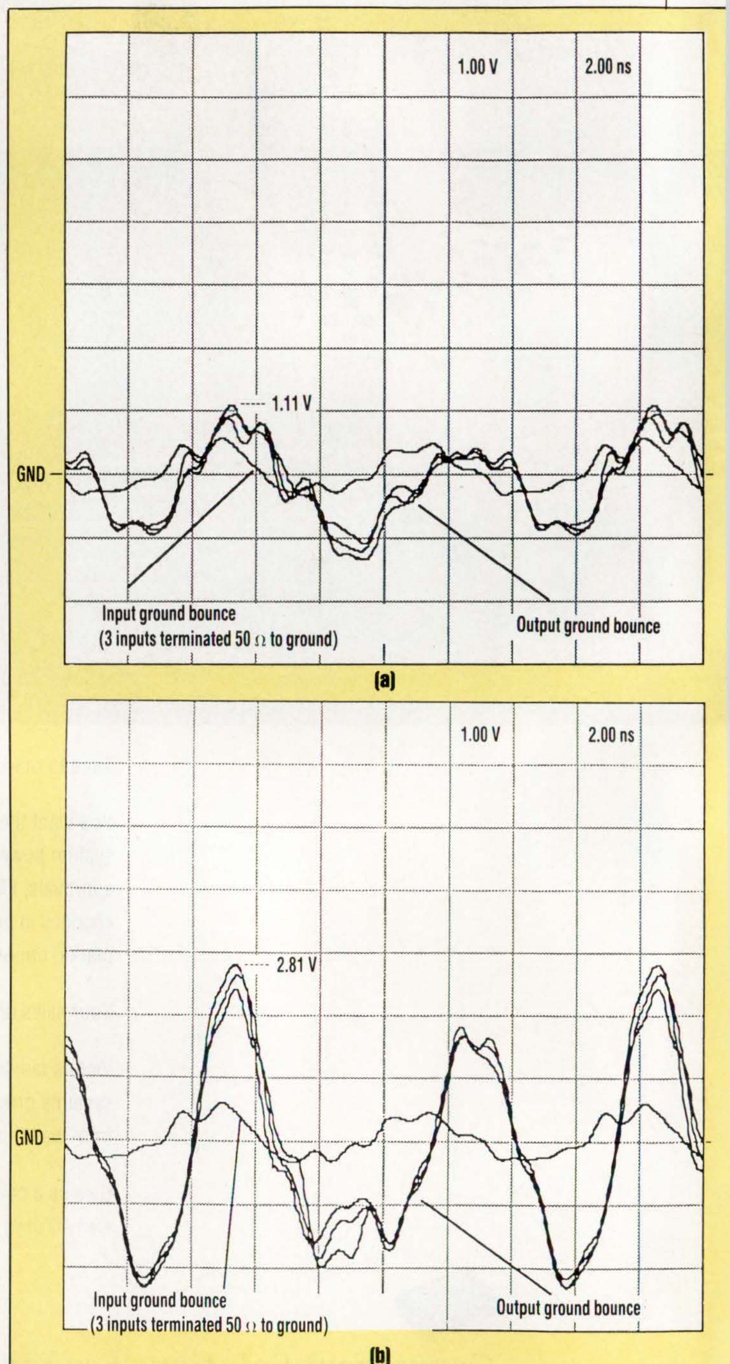
In the ground circuit, inductance causes a problem during an output transition from high to low. At that time, all of the discharging current from output loads, static I_{CC}, and dynamic I_{CC} flow through the ground inductance. Dynamic I_{CC} is:

$$I_{do} = (V_{oh} - V_{ol}) / (Z_l/2) \quad (3)$$

where V_{oh} is the high-state voltage output, V_{ol} is the low-state voltage output, and Z_l is the final line impedance:

$$Z_l = Z_0 / \sqrt{1+C_l/C_0} \quad (4)$$

where Z_0 is the line's characteristic impedance, C_0 is the capacitance per unit length of the line, and C_l is the



3. THESE TEST RESULTS SHOW significant ground bounce on three unswitched outputs when the other five outputs were switched. The output ground bounce and its reflection was lower in the 74ABT245 (a) than in the 74FCT245 (b).

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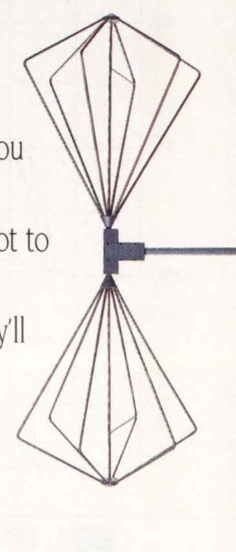

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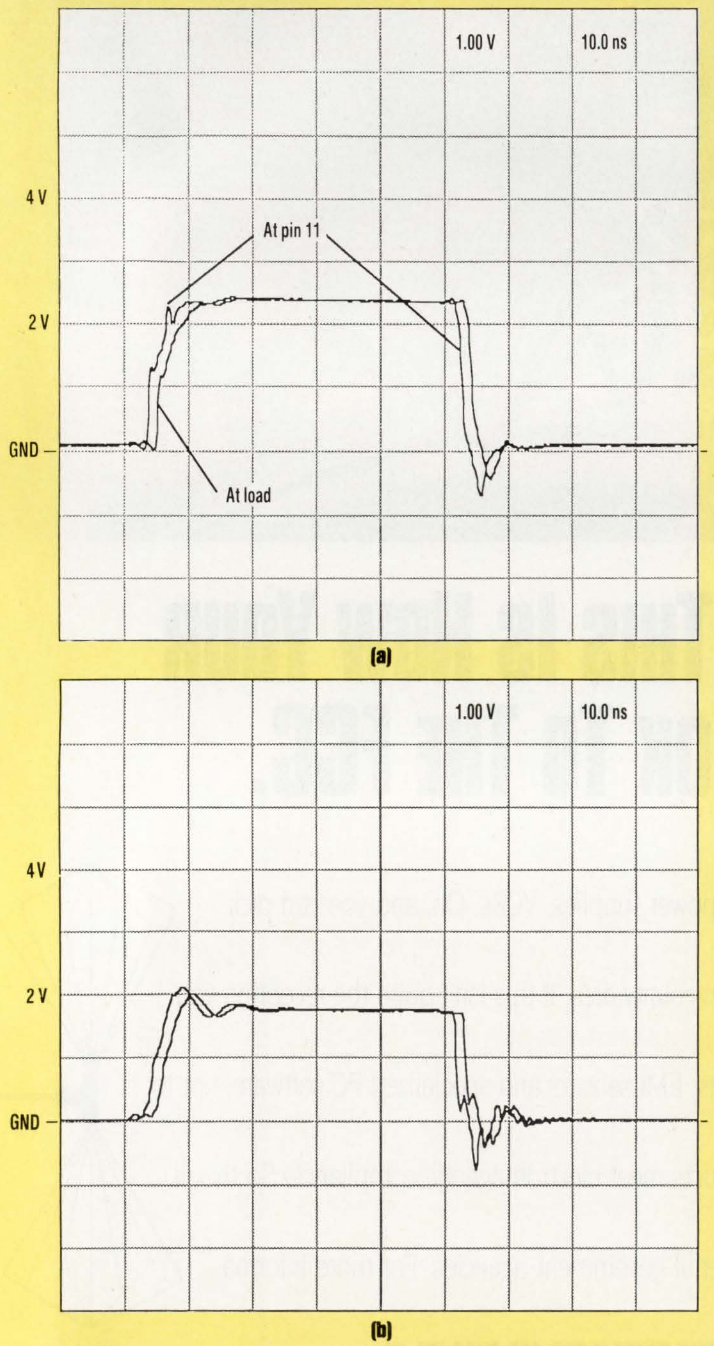
total of the lumped capacitances normalized per unit length. Z_l typically drops to well below the specified Z_0 as loads are added. But for simplicity, assuming that Z_l is 50 Ω and the voltage swing on the bus is 3 V, I_{do} = 120 mA. If all 8 bits switch simultaneously, dynamic current peaks at 120 mA × 8 = 960 mA. Thus, during output transitions from high to low, nearly 1 A must flow through the ground-pin inductance before reaching the board's ground plane. If 16 bits switch simultaneously, nearly 2 A must flow through the ground pin. Any static current from the termination resistors and I_{CC} add themselves to this current.



4. IF RELATIVELY LOW RESISTIVE terminations are used, a driver's ability to sink and source current becomes critical. In this test, two drivers were terminated with 38-Ω resistors. The 74ABT245, with an I_{oh} of –32 mA, supplied a V_{oh} of 2.4 V (a). The 74FCT245, with an I_{oh} of –15 mA, delivered 1.8 V (b).

Many new line drivers, like the MB and BTL (backplane transceiver logic) series, have multiple ground and V_{CC} pins. Multiple ground pins distribute the heavy static and dynamic current. Placing ground pins on both sides of the output pins takes advantage of negative mutual inductance to reduce overall inductance. Some BTL-series drivers, like the FB203X and FB 204X, have an I_{ol} (the current a part can sink in the low state) of 100 mA.

As noted earlier, ground noise is more critical to system failure rates than is noise on the V_{CC} line, because the TTL threshold voltage is about 1.5 V rather than half way between V_{CC} and ground. V_{olp} is a positive ground-bounce voltage, and V_{olv} is negative. V_{ohp} is a positive overshoot on the V_{CC} line, and V_{ohv} is a negative undershoot on V_{CC} (or V_{DD}). It's common to see a V_{olp} peak over 2.5 V and a V_{ohv} under 3.0 V. Those levels result in less than 3 V on the power line to ground, so it's not surprising if latches and flip-flops can't retain stored data momentarily or if outputs oscillate for short periods.

Calculate Ground Bounce

The ground-bounce voltage, as noted earlier, is L × di/dt, where L is the inductance in the current path and di/dt is the dynamic current. Using a 24-pin DIP for an advanced octal line driver, and assuming that all eight units drive a 50-Ω load simultaneously, the ground-bounce voltage is:

$$V_{olp} = 15.1 \times 10^{-9} (960 \times 10^{-3} / 5.0 \times 10^{-9}) = 2.9 \text{ V} \quad (5)$$

In practice, however, many things affect ground bounce. Pulse width is as important as amplitude. And it's often difficult to determine the timing skews between switching outputs, the mutual inductance between current paths, how ground bounce affects edge switching rates, and other factors. CMOS driver transistors tend to have more noise problems than bipolar types because CMOS devices drive from rail to rail, and they don't have a parasitic diode between the drain and source when the transistor saturates.

Designers must understand these transmission-line effects, especially when high-frequency operation is combined with high currents. Transmission-line drivers have many important characteristics, such as rise and fall times for different loads, static and dynamic impedances of the driving transistors, current sinking and sourcing capabilities, and the effects of ground bounce.

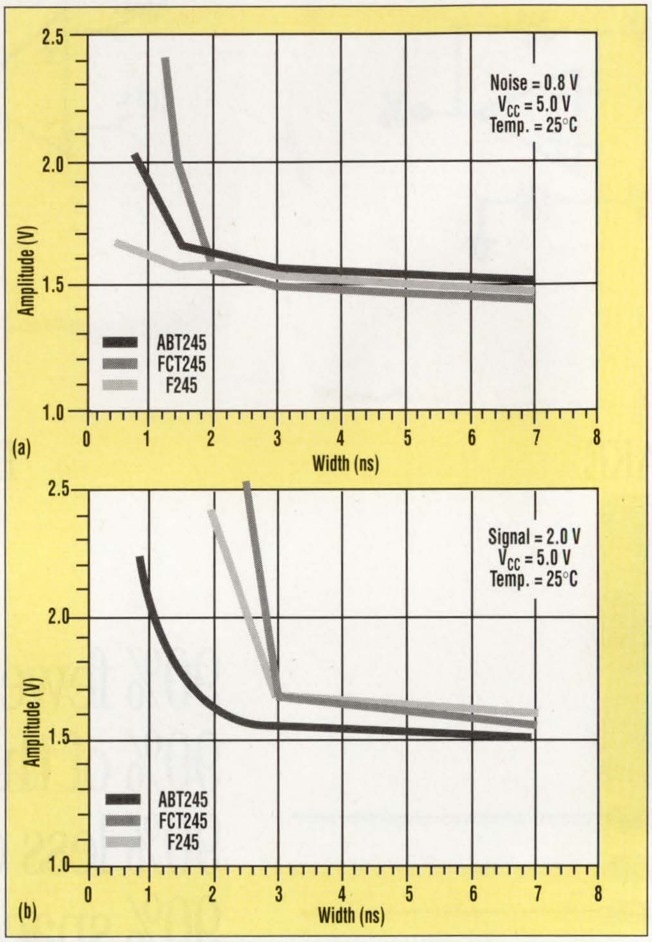
Bipolar transistors are better than CMOS types when high drive current is needed. The current gain of CMOS devices depends on the ratio of transistor width to channel length. For example, the width must be quite large to drive 64 mA. But

output capacitance rises linearly with transistor width. Because the IC's output capacitance is part of the bus load, it may reduce the maximum usable bus frequency.

The main concern in driving transmission lines is avoiding reflections. Reflections caused by improperly terminated lines could create latch-ups, glitches, or ambiguous states. In extreme cases, reflections can exceed a device's absolute maximum voltage, overstressing the device to the point of failure.

How To Terminate

There are three primary methods of terminating line drivers: serial, parallel, and Thévenin (in a few cases, diode terminations are used). Serial terminations are useful when high-impedance loads are distributed along the transmission line. For example, a serial termination is suitable for driving DRAM arrays. In that case, the termination resistors don't have to match the line impedance exactly because the resistors also dampen current flow.



5. THE AFFECTS OF INPUT NOISE and signals were investigated with the input voltage held at 2.0 V and high-to-low pulses of varying width and amplitude applied. The F245 device showed the most sensitivity to input noise (a) and the ABT245 was most sensitive to the input signal (b).

Parallel and Thévenin techniques befit applications with loads at the end of the line. Impedance matching is more important with these methods. One way to avoid static current through the termination resistor is to connect a capacitor in series with the resistor. For proper matching, the capacitor's reactance should be less than 1/10 of the value of the terminating resistance.

Another rule of thumb for terminating transmission lines is that the driver's transition times should be more than twice the line delay. That is,

$$t_r \text{ (or } t_f) \geq 2\sqrt{L_0 C_0} \qquad (6)$$

where L_0 and C_0 are the inductance and capacitance per unit length. Any reflected waves are described by their maximum amplitude and their pulse width:

$$V_{refmax} = -V_i\, C_l\, Z_0 / 2t_r \left[1 - e^{(-2t_r/C_l Z_0)}\right] \qquad (7)$$

where V_i is the initial voltage.

$$P_w(100\%) = t_r + 2\, C_l\, Z_0 \qquad (8)$$

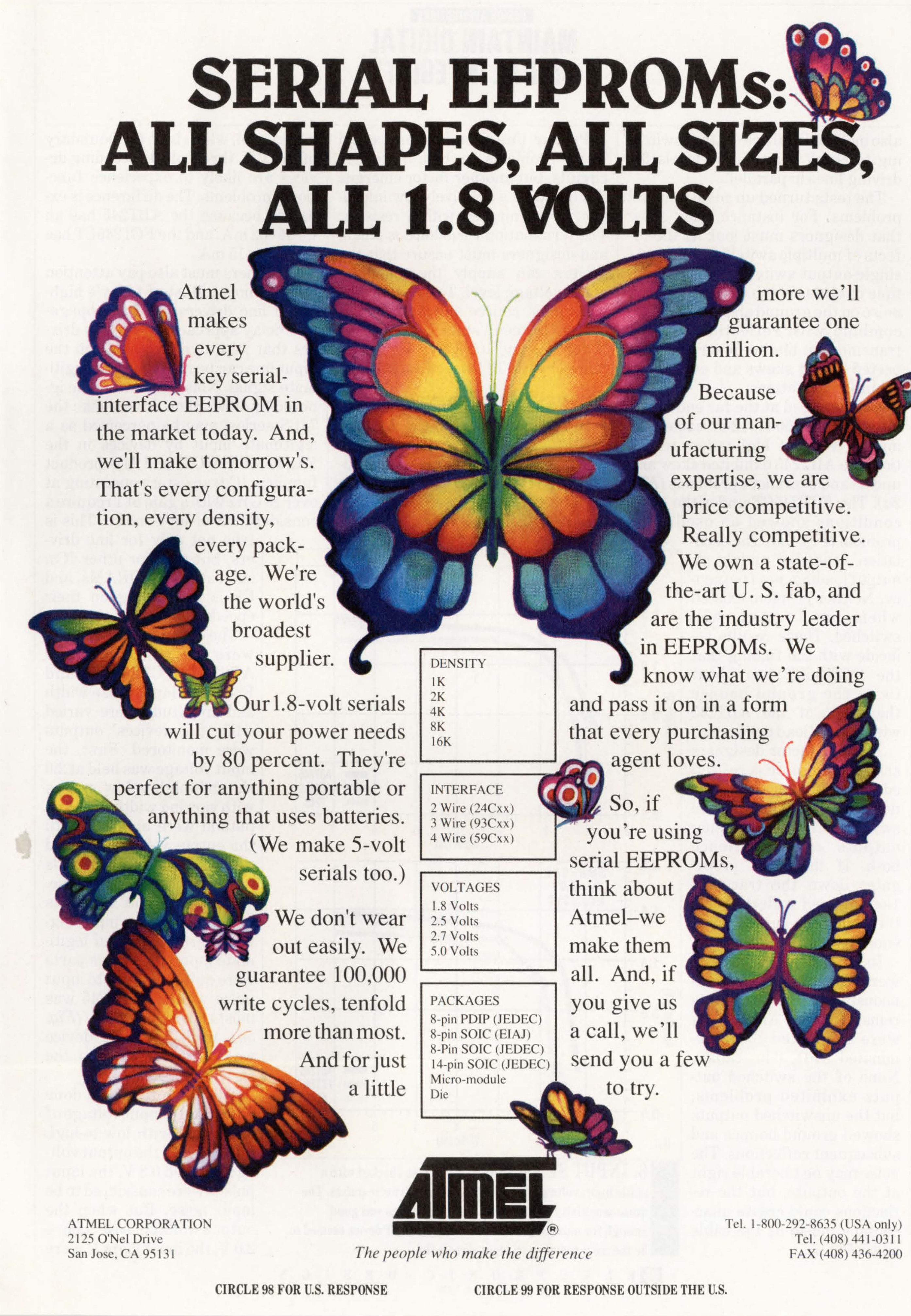
The overshoot voltage can be as high as twice the output voltage. A bipolar TTL device's output voltage swing is only 3 V, rather than the rail-to-rail swing of a CMOS TTL output. As a result, bipolar and biCMOS line drivers have lower overshoot voltages than CMOS products do. For example, in the 74ABT and FCT-T families, a parallel termination to ground is adequate, while in the ACL and FCT families, a Thévenin's termination may be needed. The parallel method eliminates a resistor per line, reducing required pc-board space and power consumption.

Bipolar output transistors, however, must consume static current, while CMOS transistors do not. In bipolar devices, the static current for driving the base output transistors must be high enough to accommodate power-supply line noise, ground bounce, and the output Miller capacitance in high-frequency operations. Otherwise, the drivers will tend to oscillate when multiple outputs are switched. Consequently, bipolar and biCMOS devices typically are designed to consume a static current of 1 to 3 mA per output.

Test Results

To derive some practical design data, the 74ABT245 and 74FCT245CT devices were tested in several line-driving applications. For convenience in simulating pc-board conditions, the tests were conducted at 75 MHz, using 38- and 50-Ω coaxial cables. Except for its better crosstalk characteristics, coax behaves similarly to transmission line. The 75-MHz frequency may be high for bus or backplane driving applications, but the tests considered burst-mode data transfers.

The cables have a line delay of about 800 ps per foot, and the ABT245 output rise and fall times are about 2 ns with 50-pF loads. The tests assumed that the devices should be able to drive up to 1 foot of the coax without a termination. Traditionally, only single-output switching data was used to describe transmission-line driving characteristics. But the tests that were performed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also included multiple-output switching to check degradation levels for driving lines in parallel.

The tests turned up some unusual problems. For instance, they show that designers must look at the effects of multiple switching as well as single-output switching. When multiple outputs switch simultaneously, noise on the ground and V_{CC} lines can combine with reflections on the transmission line to generate unexpected timing skews and even unacceptable oscillations.

When probed at the far end of the unterminated 50-Ω, 12-in. cable during an 8-output high-to-low transition, the ABT245 exhibited skew and under- and overshoot problems *(Fig. 2a)*. The FCT245CT under the same conditions showed an oscillation problem *(Fig. 2b)*. The oscillation depended mainly on output loading, not frequency. Neither problem existed when one output was switched. These results coincide with the finding that the FCT245CT has about twice the ground bounce than that of the ABT245 with a 50-pF load per output.

Another factor designers should not ignore is reflected ground-bounce and V_{CC} noise. If several outputs are switched, the nonswitching outputs can experience both. If the noise propagates down the transmis-lion line and reflects back, the amplitude can be large enough to cause data errors.

In a test, five outputs were switched simultaneously while three outputs remained low. All outputs were connected to unterminated 38-Ω, 6-in. cables. None of the switched outputs exhibited problems, but the unswitched outputs showed ground bounce and subsequent reflections. The noise may be tolerable right at the outputs, but the reflections could create unacceptable noise at the cable ends *(Fig. 3)*.

Proper line terminations avoid many problems in high-frequency circuits, but another factor emerges if a line with a relatively low impedance is terminated with a resistor: The termination resistance is small, and designers must ensure that the drivers can supply the minimum static voltage level. To do so, the devices must source and sink enough current to keep a static IR drop of 2.0 V for V_{oh} and 0.5 V for V_{ol}, as required by the TTL specification.

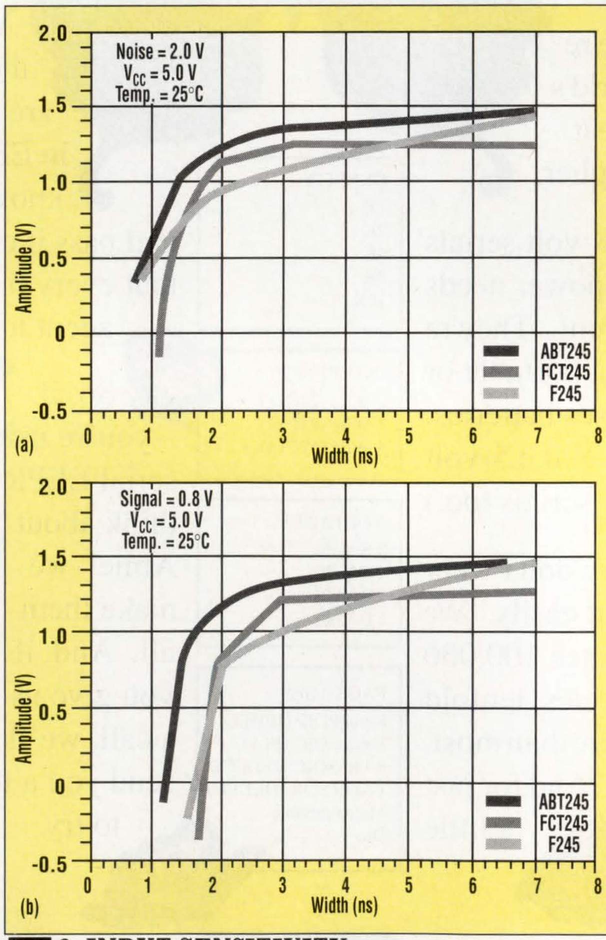
Current Differences

In tests at 10 MHz, the ABT245 and FCT245CT drove a 38-Ω, 12-in. coaxial cable with a parallel termination of 38 Ω. The ABT245 provided a V_{oh} of 2.4 V, while the FCT245CT offered a V_{oh} of 1.8 V *(Fig. 4)*. At that lower level, which is on the boundary of the TTL threshold, succeeding devices are likely to experience functional problems. The difference is expected because the ABT245 has an I_{oh} of –32 mA, and the FCT245CT has an I_{oh} of –15 mA.

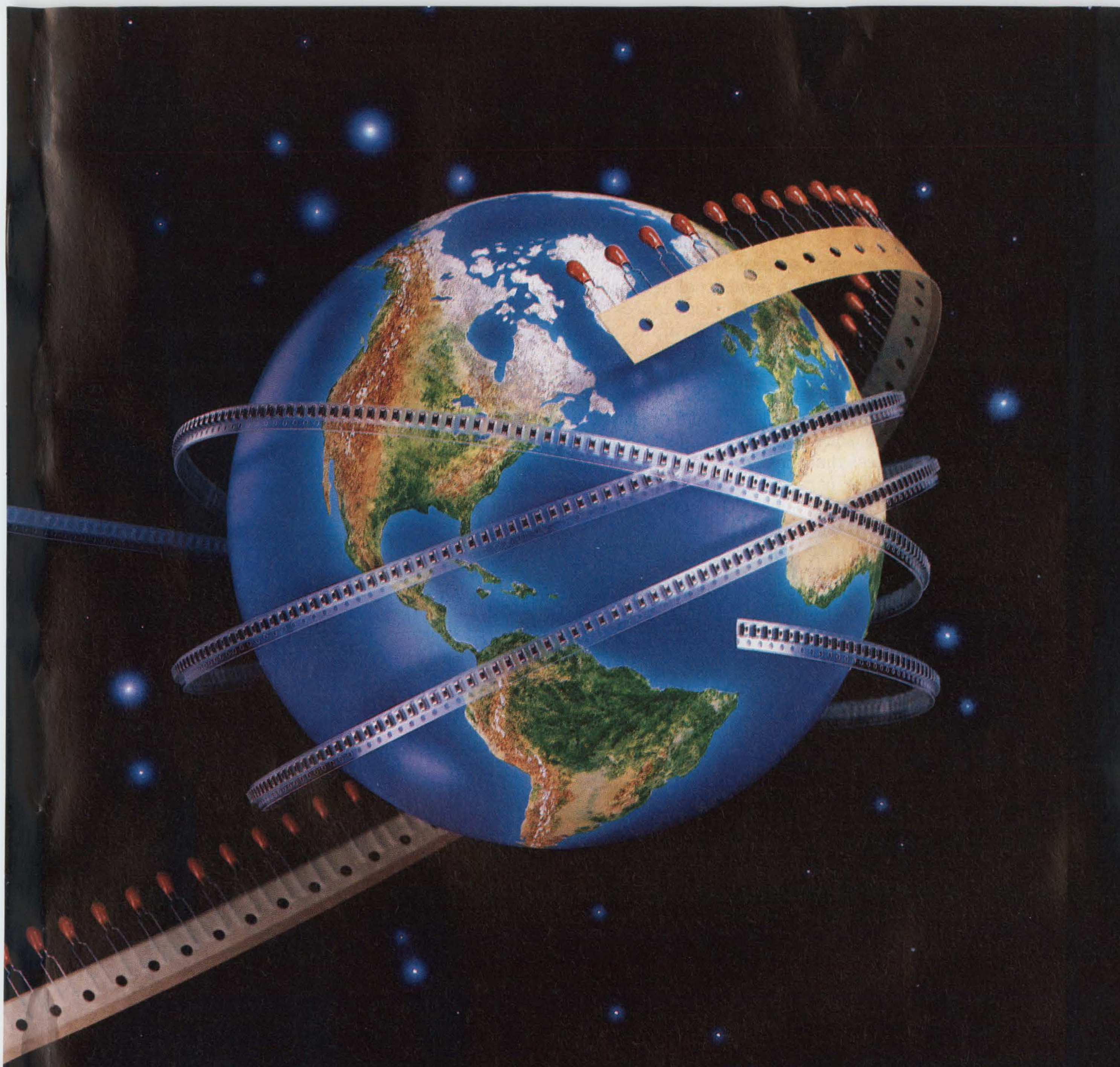
Designers must also pay attention to input noise. Most of today's high-speed line drivers have a propagation delay approaching 1 ns. In drivers that fast, dynamic noise on the input line can be mistaken as a legitimate signal. Noise that would be ignored by slower line drivers, like the 74LS series, may be perceived as a legitimate input by devices in the FAST, ABT, FCT, and MB product families. IC transistors operating at over 10 GHz with a gain of 1 require a consideration of input noise. This is true not only for line drivers, but also for other ICs, such as PLDs, DRAMs, and CPUs (depending on their speeds).

The effects of input noise were examined for the ABT245, FCT245CT, and F245. The input pulse width and amplitude were varied while the devices' outputs were monitored. First, the input voltage was held at 2.0 V, and high-to-low pulses with varying widths and amplitude were applied. Until the output voltage dropped to 2.0 V, the input signals were considered to be noise. When the output level was below 0.8 V, the input signals were considered legitimate inputs. All three parts were quite sensitive to input pulse width. The F245 was most sensitive to noise *(Fig. 5a)*, while the ABT device was most sensitive to the signal *(Fig. 5b)*.

The same test was done with a static input voltage of 0.8 V and with low-to-high pulses. Until the output voltage reached 0.8 V, the input pulses were considered to be input noise. But when the output voltage rose above 2.0 V, the input signals were



6. INPUT SENSITIVITY was also checked with a static input voltage of 0.8 V and low-to-high noise pulses. The noise sensitivity bandwidth of all three devices was good enough for most of the line noise (a). The ABT device seemed to be the most sensitive to input signals (b).



considered legitimate. The results show that the ABT device is the most sensitive. *(Fig. 6)*.

The bandwidth for noise sensitivity of all three devices was good enough for most line noise. The ABT driver appears to be more sensitive to input signals than the FCT245CT and F245 are. To ensure proper operation of these devices, any glitch caused by bus contention, live insertion, or other noise source should have a pulse width less than 1 ns.

At high frequencies, parasitic capacitances on the silicon, such as those created by input electrostatic-discharge protection devices and input clamp diodes, act as feedback channels from the chip ground and V_{CC} line noise to the internal input circuits. And the input leadframe inductance of IC packages dynamically isolates the silicon input from external input pins with high-frequency signals. These factors can cause output glitches or oscillations if the static V_{il} or V_{ih} levels are already close to the input threshold voltage.

As a result, system design engineers must check the drivers' V_{ol} and V_{oh} by calculating fan-out correctly. It's also important for designers to improve input noise margins by choosing correct decoupling capacitances and eliminating crosstalk and reflections.

A noninverting line driver, the ABT245, demonstrated this concern. Identical input signals simultaneously switched seven outputs connected to heavy loads (100 pF per output) from high to low. The eighth input had static voltages of 0.5, 0.7, and 0.8 V, in turn, and its output had no load. Thus, the eighth output should have remained in the low state, and the on-chip ground bounce could be monitored at that pin.

When the static input went from 0 to 0.5 V, the nonswitching output showed only ground bounce *(Fig. 7)*. But when the static input hit 0.7 V, the output included both the ground bounce and an output glitch. The glitch, which became worse at a static input of 0.8 V, resulted from internal feedback through parasitic capacitances on the silicon. As the static input voltage approached the threshold voltage, the danger of both the glitch and oscillation increased. This test showed that designers must heed static input voltages and equally distribute output loads among all outputs.

Fortunately, designers can do a number of things to reduce noise and its impact on their high-frequency digital systems. As mentioned, choosing appropriate decoupling capacitors is important. The capacitors should have short leads to lower their impedance. Other characteristics to look at are temperature, humidity, and capacitance ranges, frequency response, and anticipated life. Designers should also use bulk capacitors to control current and low-impedance decoupling capacitors to bypass high-frequency noise.

Reducing inductance in the ground path is also critical to noise performance. Contributing items in this path include bonding wire and the package leadframe, which are within the IC, and the ground lead or ground plane. From a noise standpoint, the smaller the package the better. But smaller packages raise other issues, such as thermal characteristics and soldering yields.

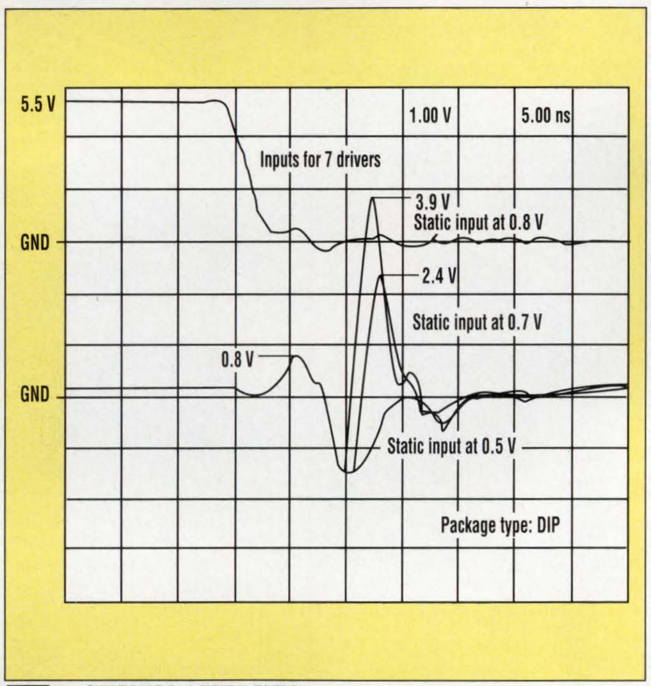
Whenever capacitances and inductances are looped in a circuit, that circuit will have resonant frequencies. It's crucial, therefore, to design a system to operate within the bandwidth of the resonant circuit.

As the tests involving input static voltage showed, input threshold voltages can affect circuit operation. IC design technologies affect threshold voltages. A bipolar device's threshold voltage varies with temperature; in CMOS devices it varies with V_{CC}. Newer BTL-series ICs have very tightly controlled bandgap-referenced threshold voltages.

If bipolar or biCMOS devices drive CMOS units, designers should include a pull-up resistor to V_{CC} on the CMOS inputs. This precaution will avoid input static current problems. The reason is that CMOS inputs require rail-to-rail swings, and bipolar output drivers can't swing rail to rail, particularly in the high state.

As shown earlier, square packages are better than DILs because square types reduce signal skew caused by differences in leadframe lengths. If DILs are used, placing the ground and V_{CC} pins in the center creates less inductance on those key lines than corner locations. Most TTL devices in DILs, however, do include corner ground and V_{CC} lines. In these ICs, a split-ground leadframe offers much less ground-noise sensitivity. This arrangement provides two ground leads to one external pin, which makes it possible to separate a noisy output ground from the rest of the silicon ground.

Multiple grounds and V_{CC} pins are



7. SEVEN OUTPUTS connected to heavy loads were switched simultaneously from high to low. The eighth, which had no load, should have remained low. But with static voltages of more than 0.7 V at its input, unacceptable glitches resulted.

MAINTAIN DIGITAL SIGNAL INTEGRITY

needed if the device must handle high static and dynamic currents. In some ASICs, designers can define these pin configurations. Otherwise, they can use devices with multiple ground and V_{CC} pins, like the FB203x and FB204x BTL transceivers, which have one ground per output on the bus side.

Many line drivers now contain so-called edge-rate control circuits on the output to help reduce noise. These circuits minimize noise caused by the dynamic current, di/dt. Also, smaller voltage swings minimize $-C \times dv/dt$, which cuts the dynamic current. For example, the FCT family swings the output from rail to rail. But the FCT-T devices swing about 1 V less, and are quieter than the FCT units. BTL and GTL logic devices have only a 1-V swing instead of the 3- or 4-V swing of the TTL standard.

Designers may also find it worthwhile to use power-up/down three-state line drivers. These devices minimize functional and dynamic current problems during power-up/down modes, especially during live insertion.

If the combination of ground bounce and its reflection is excessive, the line should be terminated, even if it meets the criteria of Equation 6. For ICs with distributed lumped loads, like memory banks, a 33-Ω serial termination is common. In other devices, if prototype tests show that a parallel termination is sufficient (rather than a Thévenin), the designer can reduce power consumption and overall costs. Also, a driver with instantaneous wave-switching capability will help avoid ambiguous states, such as slow transitions through a threshold region.

As discussed, input sensitivity can also be a problem. For advanced line drivers, bus contention, crosstalk, ground, and V_{CC} noise pulses should be no wider than 1 ns *(Figs. 5 and 6, again)*. If the cost can be absorbed, a small capacitor on the noisy line will help bypass high-frequency noise to ground. The flip side of this problem is a very slow rising or falling input to an advanced line driver. Either case can cause oscillations at the output. Consequently, designers should

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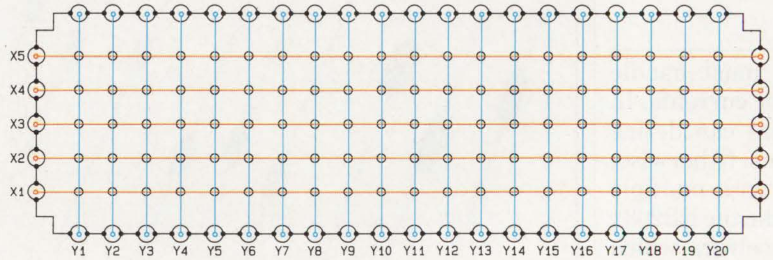

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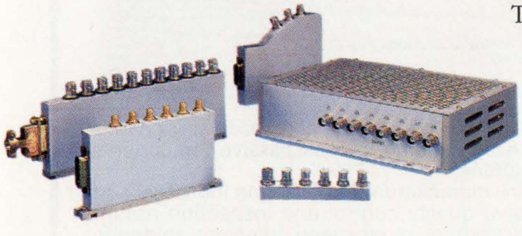

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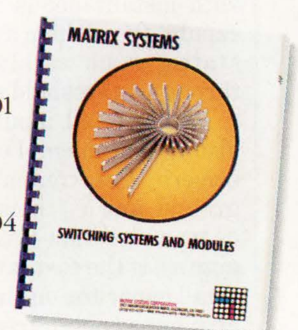

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DESIGN APPLICATIONS

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heed the dv/dt specification for the device's inputs. Some CMOS devices, such as the ACL family, have a dynamic hysteresis circuit that prevents this problem.

Finally, as system frequencies increase, so does the need for analog simulation to detect possible noise or other design problems. Isolating one source of signal integrity problems from other sources is difficult, because the sources are interrelated in most cases.

Spice simulation is a perfect tool for identifying multiple sources of signal problems. However, Spice is an analog simulation program that uses numerical analysis techniques. Therefore, it requires powerful computing capability and a large memory to ensure reasonable accuracy and execution times. But this investment can save time and money overall by detecting problems early in the design phase.

Engineers performing Spice simulations must be proficient in both semiconductor device physics and electronics. Device physics helps the engineer develop the right transistor-level models; electronics knowledge is obviously needed to better understand the circuitry, packaging, pc-boards, cables, sockets, connectors, the backplane, and so forth. The hardest part of the simulation is accurately modeling the silicon and packaging and correctly converting the electrical circuit from the mechanical elements.

For this reason, many companies have Spice specialists to assist digital designers with simulations. Companies without such specialists can contact IC houses to see what help they can provide.□

Yong-In S. Shin, who provides technical support for Philips-Signetics' customers based in Asia, received his BSEE and MSEE from Brigham Young University, Provo, Utah.

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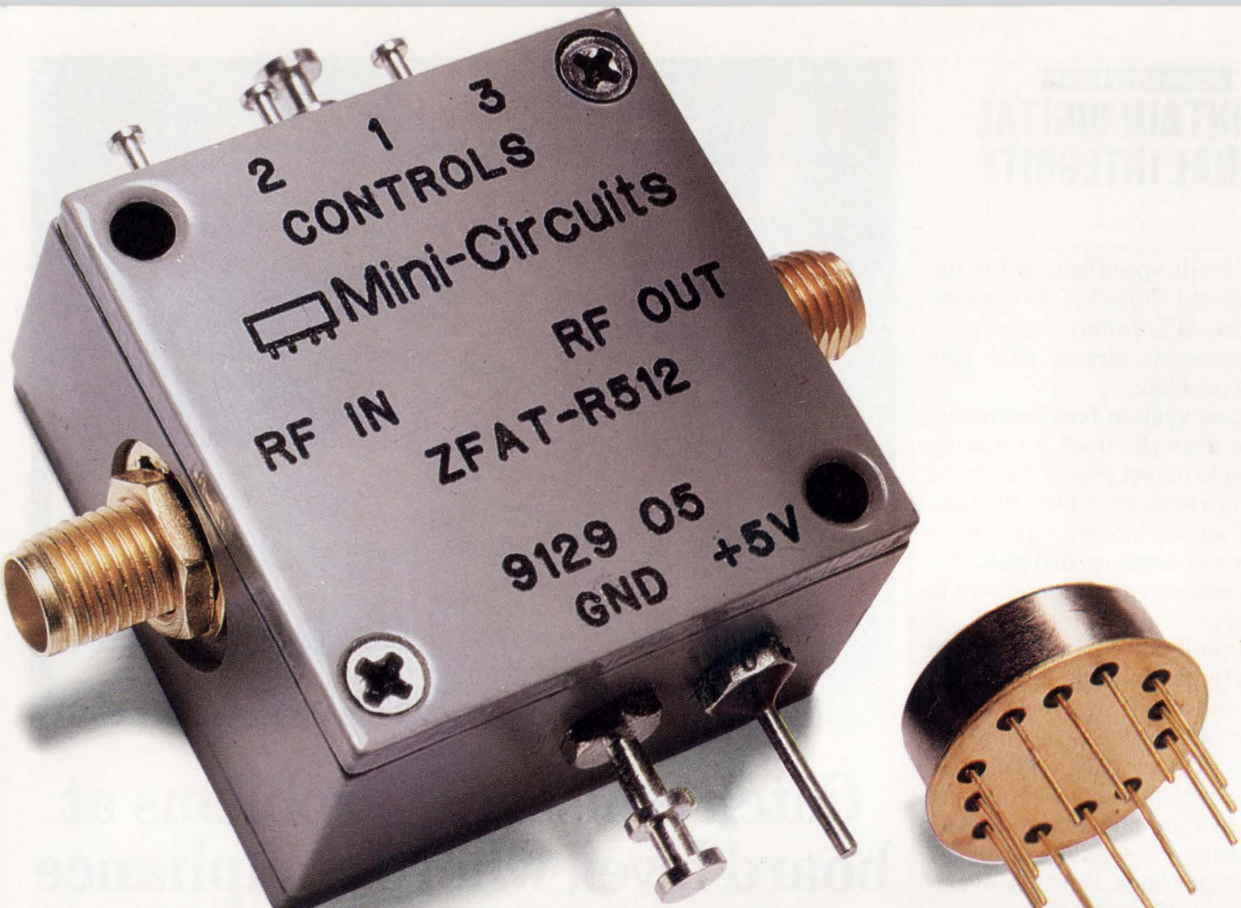

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CIRCLE 521

TRIAC CONTROLLER IS SENSITIVE, LOW-COST

HAROLD J. WEBER
P. O. Box 6161, Holliston, MA 01746; (508) 429-6563.

One of the more popular types of triac power-control circuitry uses a phase delay network for triggering. Adapting such a circuit so that a logic-level dc signal can turn an ac load on and off typically requires using a small slave triac, a high-voltage transistor, and a handful of passive components. The circuit shown adds just a single inexpensive plastic transistor to the basic relaxation oscillator type of triac triggering arrangement, yet allows a logic level input to fully control the output *(Fig. 1)*.

With the transistor turned on, the triac is gate-triggered in the usual manner: C_1 charges through R_1 until the breakover voltage of the diac is reached. The diac then fires, delivering a high-current pulse to the triac, abruptly turning the triac on. With the transistor turned off, the charging of the capacitor is spoiled, and no high-current pulses are delivered to the triac.

Because the diac's breakover voltage is about 30 V, a current will always flow through it, limited only by resistor R_1. To keep that trickle of current from triggering a sensitive triac, resistor R_2 is added to divert it.

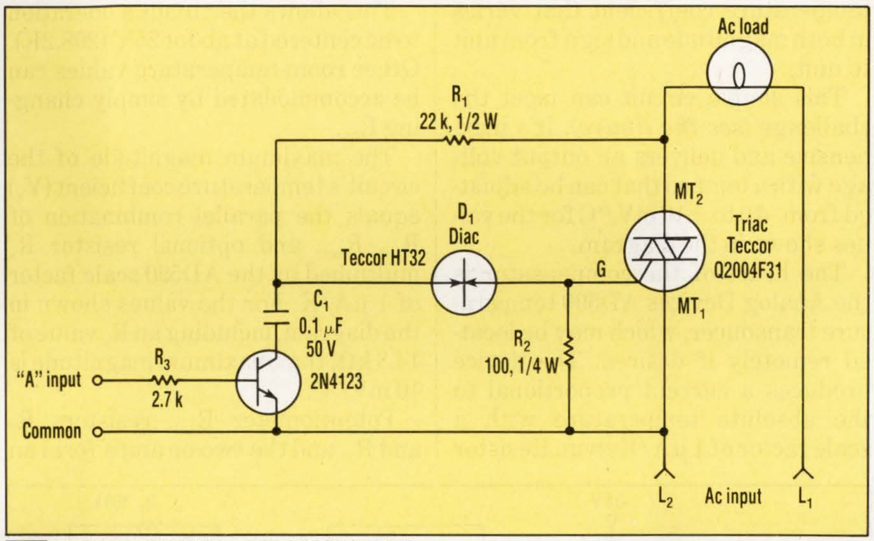
If the dc control signal at "A" is negative instead of positive, as assumed here, the 2N4123 npn transistor can be replaced by an equivalent pnp device—a 2N4125, for example.

In addition to simple on/off operation, this approach to triac control can provide three levels of power—off, half power, and full power—from a two-bit logic input *(Fig. 2)*. The circuit's operation is summarized in the truth table in Figure 2. If input B = 0, the output of inverter IC_{1B} (K) is driven high, applying a dc signal to the base of Q_1. That turns on the triac for the full ac cycle as seen in Figure 1.

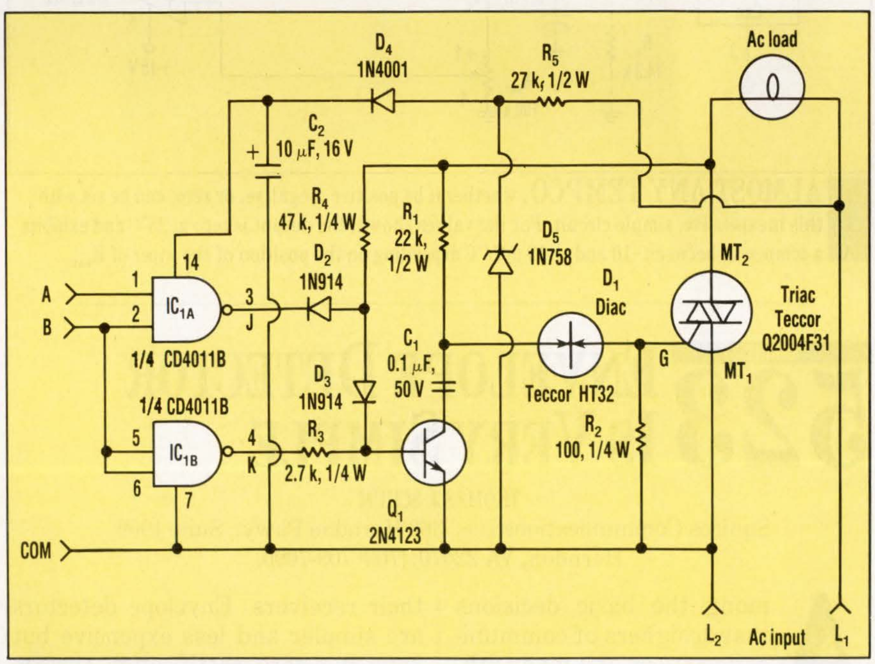
Half-power operation is obtained when inputs A and B equal 0 and 1, respectively. That keeps the inverter from turning Q_1 on but causes the output of gate IC_{1A} (J) to stay high. Consequently, the positive half-cycle pulses of ac power can be coupled through resistor R_4 and diode D_3 to its base.

If both inputs A and B equal 1, no triggering action takes place through the inverter, and the positive half cycles are diverted to the (now low) output of gate IC_{1A} through diode D_2. As a result, the transistor remains off during the entire power cycle, and the triac isn't triggered at all.

The circuitry of Figure 2 includes a line-operated power supply—consisting of R_5, rectifier D_4, Zener diode D_5, and filter capacitor C_2.□



1. THE SINGLE TRANSISTOR connected between the capacitor and the common side of the ac line allows a logic-level signal to control this triac power circuit. Resistor R_2 is also provided to prevent false triggering of the triac by the trickle current through the diac.



2. THREE POWER LEVELS are supplied by the two logic inputs of this enhanced circuit, as indicated in the truth table. R_5, D_4, D_5, and C_2 form a power supply for the logic IC. They can be omitted if another source of low voltage is available.

CIRCLE
522 ADJUST TEMPCO IN SIZE AND SIGN

MICHAEL A. WYATT
Honeywell Inc., 13350 U.S. Hwy. 19, M.S. 931-4,
Clearwater, FL 34624; (813) 539-5653.

Zeroing out temperature variations on a production line is a challenging task when the device to be compensated has a temperature coefficient that varies in both magnitude and sign from unit to unit.

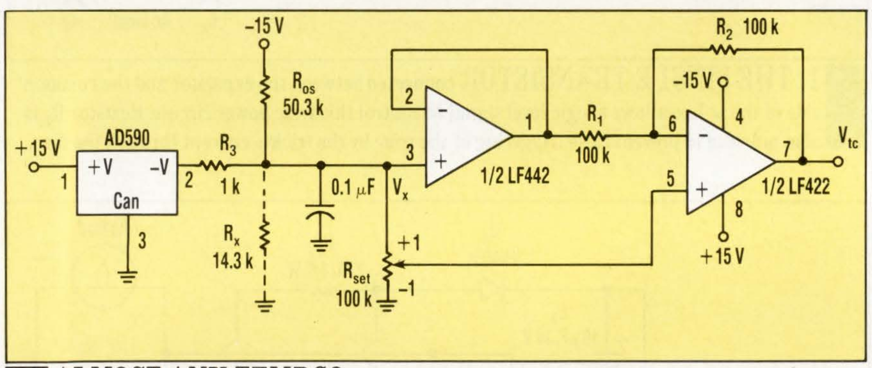
This simple circuit can meet the challenge *(see the figure)*. It's inexpensive and delivers an output voltage with a tempco that can be adjusted from –10 to +10 mV/°C for the values shown in the diagram.

The heart of the compensator is the Analog Devices AD590 temperature transducer, which may be located remotely if desired. The device produces a current proportional to the absolute temperature with a scale factor of 1 μA/Kelvin. Resistor R_{os} and the –15-V supply to which it's connected sink a current equal to the room-temperature AD590 current of 298.2 μA.

This allows the circuit's operation to be centered at about 25°C (298.2K). Other room-temperature values can be accommodated by simply changing R_{os}.

The maximum magnitude of the circuit's temperature coefficient (V_x) equals the parallel combination of R_{os}, R_{set}, and optional resistor R_x multiplied by the AD590 scale factor of 1 μA/K. For the values shown in the diagram, including an R_x value of 14.3 kΩ, that maximum magnitude is 10 mV/°C.

Potentiometer R_{set}, resistors R_1 and R_2, and the two op amps form an amplifier with a gain that varies linearly from –1 to +1 as the potentiometer wiper moves from bottom to top. That amplifier buffers and scales V_x so that the compensator's output, V_{tc}, can be adjusted over the range of –10 to +10 mV/°C (if R_x is omitted, the range is approximately –33 to +33 mV/°C).□



ALMOST ANY TEMPCO, whether it be positive, negative, or zero, can be set with this inexpensive, simple circuit. For the values shown, the output is zero at 25°C and exhibits a tempco of between -10 and +10 mV/°C depending on the position of the wiper of R_{set}.

IFD WINNER

IFD Winner for January 23, 1992

Jerald Graeme, Burr-Brown Corp., P.O. Box 11400, Tucson, AZ 85734; (602) 746-7412. His idea: *"Feedback Linearizes Current Source."*

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Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $150 Best-of-Issue award and becomes eligible for a $1,500 Idea-of-the-Year award.

CIRCLE
523 ENVELOPE DETECTOR IS VERY SIMPLE

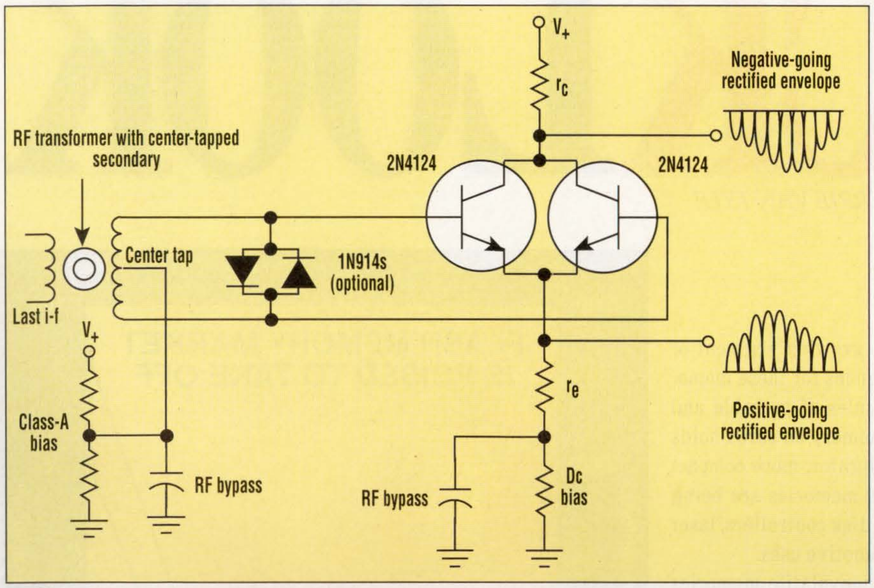
THOMAS J. SCHUM
Squires Communications Inc., 360 Herndon Pkwy., Suite 1900,
Herndon, VA 22070; (703) 709-7090.

Among the basic decisions that designers of communications gear and many other types of equipment must make is whether to use envelope detectors or synchronous detectors in their receivers. Envelope detectors are simpler and less expensive but have non-zero rectification thresholds. Synchronous detectors are more complex yet they offer much higher sensitivity. This two-transistor circuit *(see the figure)* provides the best of both worlds: It offers the virtually zero rectification threshold of a synchronous detector, but without the complexity.

The circuit is an amplifying full-wave envelope detector that has two transistors connected in parallel except for their bases, which are driven by RF signals that are 180° out of phase. For biasing purposes, the two transistors are treated as a single class-A device.

This method of driving the transistors out of phase with one another has two main effects. First, thanks to emitter coupling between the transistors, this type of detector smooths the portion of the conduction function near the zero crossing, where control passes from one transistor to the other.

Second, due to collector coupling, the circuit eliminates the positive excursions of the output, allowing only the negative half of the amplified



SIMPLE YET SENSITIVE, this amplifying full-wave detector circuit has an almost zero rectification threshold. It presents a highly linear RF load to the final i-f stage. The gain for the collector output is given (approximately) by r_c/r_e. The emitter output gain is slightly less than unity.

detector operates well on low-level signals that are below the base-emitter reverse breakdown voltage of the transistors—typically less than 5 V pk-pk.

Because the detector can amplify, it can be made extremely rugged by keeping the average input voltage below 0.1 V and by placing clipping diodes across the RF input, as shown in the diagram.

As the RF level goes down, transistor matching becomes increasingly important. However, at normal levels, such as those encountered in conventional diode detector designs, simply using two transistors of the same type is sufficient.

Because the detector threshold is virtually nonexistent, it presents a highly linear RF load to the final i-f stage. That feature, together with the fact that the detector can work with very low level signals, can significantly simplify the design of the last i-f stage.□

ELECTRONIC DESIGN

QUICK LOOK

EDITED BY SHERRIE VAN TYLE

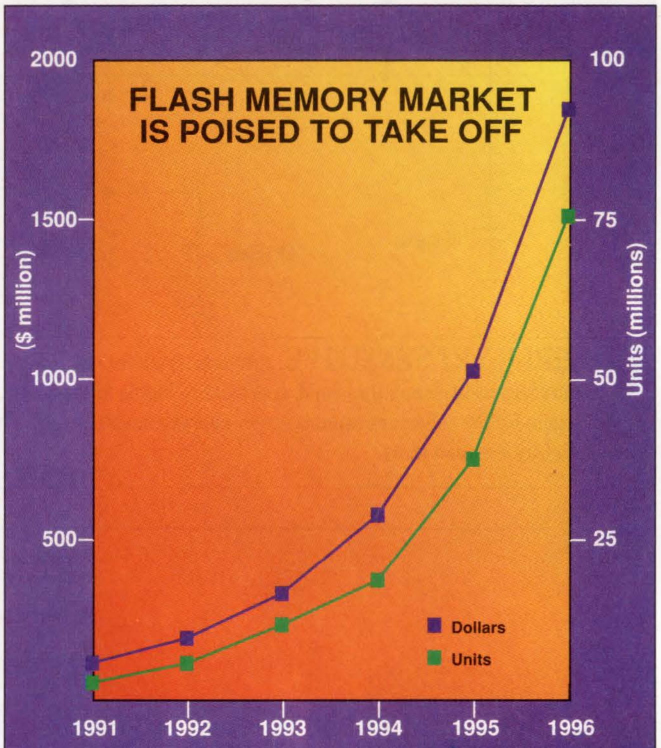
MARKET FACTS

Flash memories represent the fastest growing segment of the nonvolatile memory market. Revenues for these memories are still small, however. With sales of portable and notebook computers surging, flash memory on cards holds the promise of making these machines faster, lighter, more compact and rugged, and less power hungry. More flash memories are being put to work in embedded applications such as in disk controllers, laser printers, telecommunications, robotics, and automotive uses.

Flash accounts for less than 6% of sales of nonvolatile memories worldwide. Yet revenues for flash memories grew 61% over the previous year, according to *The Nonvolatile Memory Market* report from Electronic Trend Publications, a Saratoga, Calif., market research company.

Flash memories, now at 4 Mbytes, are seeing increasing capacity with each new generation. Equally important, the new 3.3-V flash memories will help designers of portable systems. Still pricey, flash products will eventually drop in cost. Flash memory revenues are expected to increase from $121 million in 1991 to $1.85 billion by 1996, a compound annual growth rate of nearly 73%.

Looking at the overall nonvolatile market, more than $2.2 billion worth of nonvolatile memory components were sold worldwide last year. Revenues grew just 3.1% compared with the previous year because of falling prices and flat sales for EPROMs, which still make up the largest market sector.



Source: Electronic Trend Publications (408) 996-7416

QUICK NEWS: EDUCATION

Tricks and techniques for successful linear designs are among analog design topics covered in a one-day application seminar to be held in 34 cities throughout the U.S. and Canada through May and June. Other topics are op amp subtleties, single-supply low-power systems, and high-speed applications. The $20 admission includes lunch, a 700-page design and application handbook, product samples, and a set of Spice models on disk. Contact Analog Devices, One Technology Way, P. O. Box 9106, Norwood, MA 02062-9106; (800) 262-5643 or (617) 937-1430. CIRCLE 451

Seminars on designing with switching power supplies will be held at various sites worldwide throughout May and June. Topics include optimizing control loops, load sharing with parallel power supplies, and spice modeling of switching supplies. Given by Unitrode Integrated Circuits, the seminars emphasize practical aspects of switching supply design, at an intermediate technical level. Seminar participants receive a copy of Unitrode's 340-page manual. Seminar fees vary by location. Contact Unitrode, 7 Continental Blvd., P. O. Box 399, Merrimack, NH 03054-0399; (603) 424-2410; fax (603) 424-3460. CIRCLE 452

A four-day introduction to the C++ programming language is among the classes offered by the Microtec Research Technology Training Center around the U. S. throughout 1992. Others are one-, three-, and four-day exploration of the Microtec Tesearch Toolkit. Courses emphasize needs of real-time and embedded system developers. Lab exercises make up at least half the time in the training courses. Tuition ranges from $300 for a one-day toolkit overview to $1000 for a four-day introductory C++ series. Lunch and refreshments are included. Contact Barbara Vienna, 2350 Mission College Blvd., Santa Clara. CA 95054; (800) 950-5554, (408) 980-1300; fax 982-8266. CIRCLE 453

Xhibition covers distributed computing and the X Window System. To be held at the San Jose, Calif., Convention Center June 15–19, Xhibition showcases distributed databases, three-dimensional applications, and user interface programming with seminar tracks for managers, application developers, and technology planners. For seminar prices or further information, contact Xhibition 92 Registration, 106 Wisteria Way, Mill Valley, CA 94941; (415) 388-7506. CIRCLE 454

OFFERS YOU CAN'T REFUSE

A free newsletter illustrates how to simulate circuits incorporating silicon-controlled rectifiers using Spice. The Intusoft Newsletter gives a practical example of an RF oscillator simulation and covers how to convert data-sheet parameters into Spice model parameters. The newsletter also demonstrates how new Spice models for RF bipolar junction transistors and ferrite beads can be created. To receive a copy, contact Charles Hymowitz, Intusoft, P. O. Box 710, San Pedro, CA 90733-0710; (310) 833-0710; fax (310) 833-9658.
CIRCLE 455

A start-up company garnering support for the PEX three-dimensional graphics standard is offering its PEXtk graphics library free through the MIT X consortium. The PEXtk graphics library targets developers of mechanical CAD, scientific visualization, and other 3D applications. Similar to Silicon Graphics Iris GL, PEXtk makes it easy for developers to port their applications to the PEX protocol. A complete source code version of PEXtk 1.0 is avilable free from the MIT X consortium. For details, contact SHOgraphics, 1890 N. Shoreline Blvd., Mountain View, CA 94043; (415) 903-3880; fax (415) 903-2420.
CIRCLE 456

An application note, Digital Signal Processing Fundamentals, explains how engineers can develop powerful PC-based data-acquisition and analysis systems using DSP technology. The note discusses DSP from a hardware, software, and applications point of view. A second note, Digital Signal Processing Hardware, explains the basics of DSP boards and their use in real-time tasks. To request a copy of DSP Fundamentals (part no. 430201-01) or DSP Hardware (part no. 340223-01), contact National Instruments at 6504 Bridge Pt. Pkway, Austin, TX 78730-5039; (512) 794-0100 or (800) 433-3488; fax (512) 794-8411.
CIRCLE 457

Vortec's free slide rule calculator eases calculating the heat load inside an industrial control enclosure. The slide rule shows the enclosure's BTUH gain or loss based on the interior and exterior temperature differential and the effective square footage of the enclosure. The reverse side of the rule lists Vortec's cooling systems. For the calculator or for more information, contact the company at 10125 Carver Td., Cincinnati, OH 45242; (800) 441-7475.
CIRCLE 458

KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458; fax (408) 253-6085

Let's explore using the product classification matrix to help guide development strategy. How should product development money be allocated over the matrix? Which cells should receive preferential treatment? Should certain cells be avoided? Do the following:

1. Position products that generate revenue on the classification matrix.
2. Identify the profit dollars produced by each product and determine the total for each cell. Look ahead at least two years. Produce a classification matrix for each quarter.
3. Position products currently under development, that are at least partially staffed, on the classification matrix for each quarter.
4. Forecast the expected profit dollars each new product is expected to generate and determine the profit total for each new cell. Look into the future at least two years. Produce a classification matrix for each quarter.
5. Integrate the information from steps 2 and 4. Produce an integrated classification matrix for each quarter.
6. Analyze the trends from quarter to quarter and from year to year.

Here's what I see in most organizations that follow this advice: First, present funds are derived from me-too products; second, most new product efforts are focused on the me-too cell; and third, they don't really like being in this situation. The view of reality produced by this exercise stings; most organizations begin to see their vulnerability! A typical analysis might shown present profit dollars to be distributed as follows:

T = June 1992 Total sales: $100 million
90% me too
10% derivative
0% next-generation
0% first of a kind

The first pass look two years into the future has the following distribution:

T = June 1994 Total sales: $95 million
95% me too
5% derivative
0% next generation
0% first of a kind

Do you see the potential problem? Is this an indication that this product development organization is stuck? Have they gotten too good at hitting singles and following incremental product development strategies? A more enlightened portfolio might look like:

T = June 1994 Total sales $150 million
50% me too
30% derivative
20% next generation
0% first of a kind

In this scenario, the organization developed the insights needed to move from being just a me-too organization to one that has distributed new product development capability. They can give you a me-too, a derivative, or a next generation. They now think in terms of working both the product and the market axis of the product classification matrix. Given a little more time, don't be surprised if a first-of-a-kind product appears. When your organization has its product portfolio distributed across the classification matrix, then you know you can do true accelerated, concurrent engineering.

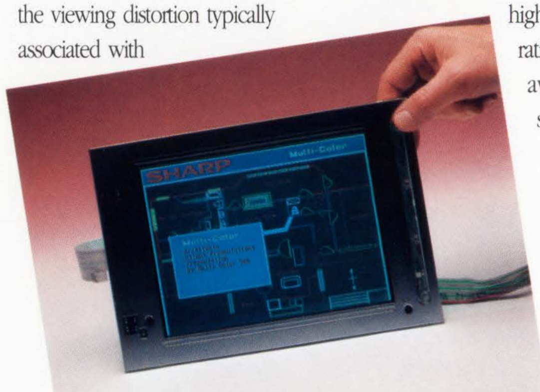
WHAT'S NEW

NO MATTER HOW YOU LOOK AT IT, SHARP'S NEW PASSIVE COLOR DISPLAY REALLY SHINES.

Today's exploding growth in notebook computer sales is matched only by the almost dizzying array of improvements in compatible flat panel displays as manufacturers slim down, lighten up and improve the aesthetics of notebook compatible displays, while expanding screen size.

One of the latest breakthroughs from Sharp is a super-efficient passive matrix color display whose viewing quality leapfrogs anything previously available in its class.

The new LM64C031 passive color LCD provides the compact size, light weight and low power consumption of traditional passive displays — for about half the price of equivalent TFT color models. At the same time, thanks to Sharp's exclusive three-dimensional film compensation process, the display achieves high brightness, superior color saturation and excellent contrast without the viewing distortion typically associated with passive color displays. The product offers VGA-quality resolution, a response speed of 450 ms and contrast ratio of 13:1, with mouse-compatible speeds and even higher contrast ratios to be available soon.

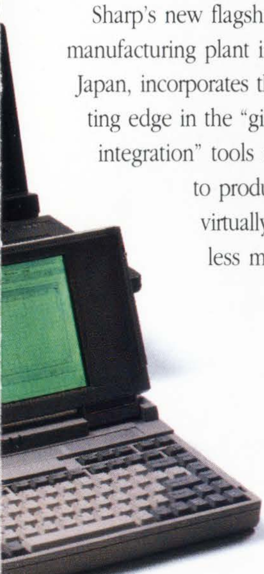


IMAGINATION AT WORK

MAKING IT BIG WITH TFTs TAKES VISION AND ENORMOUS INVESTMENT.

Thanks to its early and continual investment in the manufacturing process, Sharp supplies some 70% of the world's thin film transistor (TFT) displays. TFT's compact, light, energy-efficient package provides color, clarity and full-motion video equal to or better than CRTs.

Sharp's new flagship TFT manufacturing plant in Tenri, Japan, incorporates the cutting edge in the "giant scale integration" tools required to produce virtually flawless matrices of hundreds of thousands of transistors. New advancements in photolithography, chemical vapor deposition and fusion-drawn glass continue to keep Sharp the quality leader in a market expected to grow to $3.1 billion by 1995.



SHARP IN THE U.S.A.

SHARP: NOW A MAJOR U.S. MANUFACTURER.

Sharp has demonstrated an unprecedented commitment to its U.S. customers by augmenting IC research and development activities at the company's new facility in Camas, Washington, with an additional $30 million investment in LCD production.

The first Japanese company with an LCD manufacturing operation in the U.S., Sharp is now able to assure the fastest response and repair time possible, backed by the largest support team in the country.

COMING NEXT ISSUE: COLOR FLAT PANEL DISPLAYS. THEY'RE GETTING MORE COMPACT, MORE ENERGY EFFICIENT, WITH LARGER, CLEARER SCREENS. GET THE BIG PICTURE ABOUT WHAT'S NEW IN TFT AND OTHER COLOR DISPLAYS IN THE NEXT ISSUE OF SHARP INSIGHTS.

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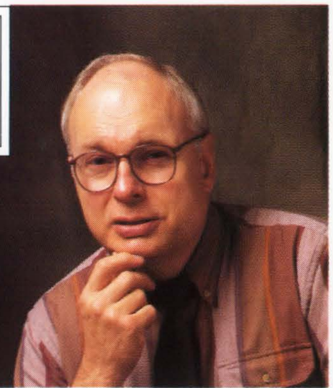
CIRCLE 204 FOR U.S. RESPONSE CIRCLE 205 FOR RESPONSE OUTSIDE THE U.S.

INSIGHTS FROM SHARP

FIRST PERSON

THE CHIPS WHOSE TIME HAS COME.



BY CHUCK HASTINGS
MARKETING/APPLICATIONS MANAGER
FIFO AND SPECIALTY MEMORIES
SHARP MICROELECTRONICS
TECHNOLOGIES, INC.

If some of the gold-rush glamour has worn off the electronics field today, as compared to the entrepreneurial '80s, the same can't be said for the First-In, First-Out (FIFO) memories which serve as data buffers between systems operating at different speeds.

Why? Because these never were glamour parts in the first place — never the parts that show up in the block diagram on system designers' blackboards. As often as not, the lines in between these blocks turn into FIFOs.

Nevertheless, the "unglamourous" FIFOs have proven to be the right parts at the right time. In some ways, their evolution is the gating factor in the convergence of higher system performance with greater design efficiency.

The greater availability of "open system" components gives system designers the freedom to draw parts from off the shelf, instead of designing them from scratch. But it's the FIFOs which compensate for mismatches in data rates, word widths and synchronization between those high-profile intelligent engines.

Similarly, FIFOs serve the trend to greater partitioning of design tasks among people and teams, expediting the eventual interfacing of subsystems and components simply and economically.

Ultimately, the measure of a FIFO like Sharp's new 36-bit bidirectional LH5420 — the first and only true system-level FIFO to date — is how little time, money, board space and special attention it gobbles up during the hardware development process.

As a low-profile supporting player, the feature-packed LH5420 is a huge success — proof that FIFOs are alive and well, and — given the decidedly less glamourous alternatives — just the stuff which the no-nonsense design environment of the '90s is meant to build on.

THE SHAPE OF THINGS TO COME

PRICELESS PREVIEWS.

The latest issue of Sharp's Memory Data Book includes several "sneak previews" of Sharp memory components now under development: a 32M Mask ROM, for example—the world's largest; a 1024 x 36 unidirectional FIFO with the most fully synchronous feature set available; and a 20 ns Static RAM in a 64K x 18 configuration. For your free copy of the '91/'92 Memory Data Book, or for other information about Sharp IC, Opto and LCD components, call your regional Sharp office listed at right.

N. American Headquarters:
Camas, WA
Ph (206) 834-2500, Fax (206) 834-8903

West
Northern CA: San Jose, CA
Ph (408) 436-4900, Fax (408) 436-0924

Southern CA: Carson, CA
Ph (213) 637-9488, Fax (213) 631-2945

Central
Texas: Irving, TX
Ph (214) 929-0999, Fax (214) 929-0958

Texas: Houston, TX
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Illinois: Romeoville, IL
Ph (708) 759-8555, Fax (708) 759-6319

East
Northeast: Burlington, MA
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East Coast: Lawrenceville, GA
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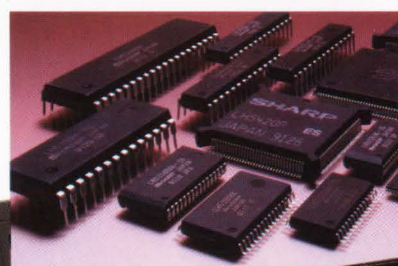
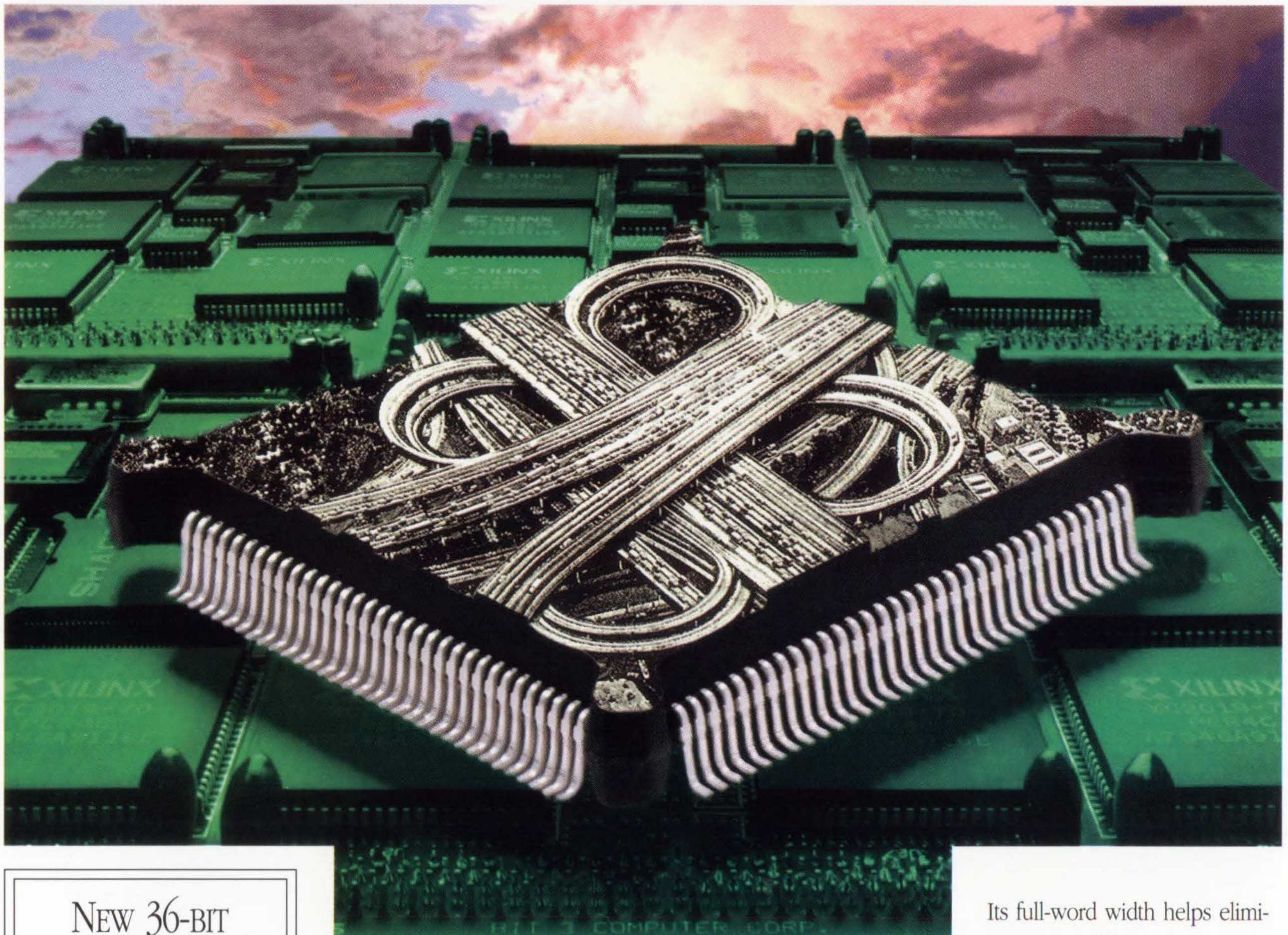


INSIGHTS FROM SHARP



New 36-bit FIFO merges most-asked-for features.

Variously described as "data accordions" or "logical rubber bands," FIFO (First-In, First-Out) memories serve as data buffers between different CPUs running at different speeds, or between controllers and their peripheral equipment. This data-rate-matching capability provides an ideal thoroughfare between independent, intelligent processors of differing word widths and/or clock speeds.

Now, Sharp's new 36-bit synchronous, bidirectional LH5420 represents the evolution of FIFOs from byte-sized to system-wide solutions. No longer a mere piece part, the LH5420 handles system-level problems, allowing even the most high-performance systems to be interconnected by efficient data "superhighways."

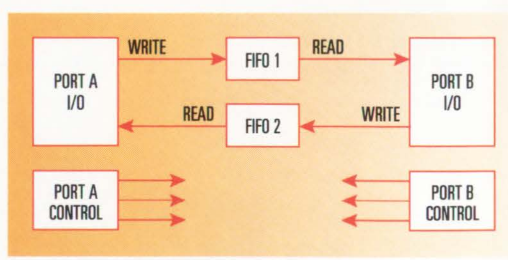
Designed to meet the wish lists of top system designers, the LH5420 offers bidirectional, two-way "funneling/defunneling" from a 32-bit bus to a 16-bit or an 8-bit bus, with two-way parity checking built in. Fully synchronous, the 36-bit LH5420 also is able to provide full-word-width, two-way communications between most 32-bit processors.

By replacing eight or more standard byte-wide FIFOs, the LH5420 saves real estate, simplifies the design process and accelerates system performance. Its full-word width helps eliminate the problems of race conditions, metastabilities and speed differentials of side-by-side partial-word FIFOs.

The newest addition to Sharp's broad line of FIFOs — including both small-capacity ("shallow") and large-capacity ("deep") buffer memories — the LH5420 represents the industry's first system-level FIFO, requiring no external glue to integrate. It is available from Sharp for immediate delivery.

ANSWERING THE WISH LIST.

THE LH5420 COMES PACKED WITH FEATURES WHICH DESIGNERS TOLD SHARP THEY WANTED IN A FULL-WORD-WIDTH FIFO, INCLUDING ON-THE-FLY PARITY CHECKING, TWO-WAY MAILBOX COMMUNICATIONS, SYNCHRONOUS REQUEST/ACKNOWLEDGE SIGNALS AND PROGRAMMABLE ALMOST-FULL AND ALMOST-EMPTY FLAGS. IT IS AVAILABLE WITH CYCLE TIMES OF 25, 30 AND 35 NS, AND IN BOTH PQFP AND PGA PACKAGES.



QUICKLOOK

TALES FROM A SKUNK WORKS

The assumptions and models that govern the management of business and product development in America are subtle, unstated, and often unconscious. Deeply ingrained in our training and industrial infrastructure, these assumptions are antithetical to skunk works and fast cycle teams.

In the early 20th century, complex products were built by skilled craftsmen. As in the days when skilled artisans made suits of armor, so it was with technical devices in the early part of this century. Adolph Hitler thought that he could win World War II despite U. S. industrial strength, because we lacked enough craftsmen to make optical gunsights in large volume. He was wrong.

Why? The name Frederick Taylor is little known today. Yet his contributions created the environment in which we still function. Taylor's methods let the U. S. lead the world. He found that the most complex tasks could be broken into sequences of trivial steps that could be performed by unskilled labor. His revolutionary paradigm allowed the U. S. to produce enormous quantities of optical gunsights, electronics gear, aircraft, and ships. Later it allowed prosperity and high salaries for blue collar workers.

Taylor process products were seldom the best, but they were good enough and were produced (and marketed—that is another story) in such large volumes that their impact was overwhelming. Even in World War II, other nations often had "best of breed" products. They initially had superior rifles, fighters, tanks, battleships, submarines, and torpedoes. But ours were adequate, and they were legion. So we won that war.

As in a science fiction tale, we have encountered aliens with superior technology. This time it is not a weapons technology, but better methods for managing businesses and developing products than Taylor's. We invented these methods, but the aliens perfected and exploited them.

Companies using Taylor's models don't care much about skill, talent, or multidisciplined teams. They want obedient workers and don't want them to think. The bosses think and the workers mindlessly toil.

Foreign companies complain that it is difficult to find skilled workers, but we don't. Eighty percent of U. S. employers are satisfied with the output of our K-12 schools, though the data proves we lag the industrialized world; 98% never look at high school transcripts.

This attitude extends to professionals and middle management. In most U. S. firms engineers and other professionals are expected to do what they are told, while middle managers implement policy set from above. In companies where the traditional models prevail, it is rare for skunk works and their leaders to prosper.

Skunk works and fast cycle teams can't function under the Taylor model—it kills them. They need the active support and shelter of the CEO. As yet only a few leading U. S. firms possess such leadership. These will be the winners.

John D. Trudel lectures and provides business development consulting. Trudel is founder and director of The Trudel Group, 52001 Columbia River Hwy., Scappoose, OR 97056; (503) 690-3300; fax (503) 543-6361. He is also the author of High Tech with Low Risk. *To order* High Tech, *phone Eastern Oregon State College at (503) 962-3755.*

HOT PC PRODUCTS

As many users of PCs, laptop, and notebook computers discover, without a connection device, transmitting isn't possible from public pay phones, multiline, PBX systems, and many hotel telephones. Unlimited Systems' acoustic coupler performs at between 2400 and 9600 baud. The Konexx Koupler runs off a 9-V battery, which supplies at least 50 hours of modem transmission. The coupler has a list price of $149. Contact Unlimited Systems Corp., 5555 Magnatron Blvd., Suite J, San Diego, CA 92111; (619) 277-3300; fax (619) 277-3305. CIRCLE 459

VirusNet, which protects PCs and LANs, is integrated with security, menu, and inventory software. From Safetynet Inc., VirusNet uses a disk scanner to locate viruses on floppy- and hard-disk drives. The scanner also detects and removes such viruses as Michelangelo and Stoned. The software sells for $49. Contact Safetynet Inc., 14 Tower Dr., East Hanover, NJ 07936; (908) 851-0188. CIRCLE 460

DID YOU KNOW?

. . . that despite 40 years of predictions of engineering shortages, no projects have been canceled because of a lack of technical talent and no projects have been failures due to a lack of technical expertise.

Testimony by Billy Reed to the Subcommittee on Investigation & Oversight of the House Science, Space, and Technology Committee

. . . that about 90% of the 14.4% foreign market share in Japan is made up of U.S.-based semiconductor company sales there. In world markets outside Japan, U.S. semiconductor companies have a 56% share vs. 22% for Japan-based companies. A 1 percentage point increase in Japan's $20.9 billion market equals $209 million in additional revenues for U.S. companies and creates about 1000 jobs for American workers.

Semiconductor Industry Association

BEST SELLERS

Which technical books are the most popular in Silicon Valley?

ELECTRONICS:

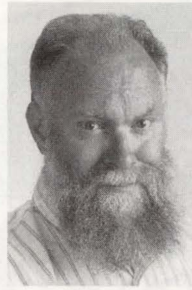
1. *Noise Reduction Techniques in Electronic Systems, 2nd ed.* by Henry W. Ott. John Wiley & Sons, 1988. ***$51.95.***
2. *PSpice & Circuit Analysis* by John Keown. Macmillan Publishing Co. 1991. ***$25.***
3. *Fax: Digital Facsimile Technology & Applications* by Kenneth McConnell. Artech House, 1992. ***$78.***
4. *The Art of Electronics, 2nd ed.*, by Paul Horowitz and Winfield Hill. Cambridge University Press, 1990. ***$59.95.***
5. *Wire and Cable for Electronics: A User's Handbook* by Neil Sclater. T. A. Books, 1991. ***$29.95.***

COMPUTER SCIENCE:

1. *C++ Programming Language, 2nd edition*, by Bjarne Stroustrup. Addison-Wesley, 1991. ***$34.50.***
2. *Tog on Interface* by Bruce Tognazzini, Addison-Wesley, 1992. ***$26.95.***
3. *Object-oriented Design with Applications* by Grady Booch. Benjamin-Cummins, 1991. ***$46.25.***
4. *C++ Primer, 2nd edition* by Stanley B. Lippman. Addison-Wesley, 1991. ***$32.25.***
5. *Programming Perl* by Larry Wall. O'Reilly & Associates, 1990. ***$29.95.***

This list is compiled for *Electronic Design* by Stacey's Bookstore, 219 University Ave., Palo Alto, CA 94301; (415) 326-0681; fax (415) 326-0693.

PEASE
PORRIDGE



BOB'S MAILBOX

Dear Bob:

Congratulations on your Neal Award.

It's one thing to excel in circuit design, but now in your column too! That's a very rare combination. Your column is a refreshing departure from the stuffy, lightweight fare normally encountered. Keep up the good work.

Also, thanks again for plugging our multiplier in that earlier column.

JERALD GRAEME
Manager, Instrumentation Components Design
Burr-Brown Corp.
Tucson, Ariz.

Let's all promote analog stuff, even if it's not linear. –RAP

Dear Bob:

Congratulations on the Neal Award Certificate of Merit. Your columns are great. No matter who won, in my opinion you should have.

Don't belittle such certificates. They come in handy for covering ugly places on walls. And they can buy credibility with persons otherwise not sufficiently intelligent to listen to you.

No money, too bad; you could have used it to buy some superconducting speaker wires!

RONALD A. ROHRER
Director of the Center for Computer Aided Design
Carnegie-Mellon University
Pittsburgh, Pa.

Thanks, but I would have trouble splicing them. –RAP

Dear Bob:

I very much enjoyed your article in the March 5th issue describing Applications Engineers. I think you have described our profession perfectly. When "Field" is added to the title of Applications Engineer, it adds another dimension to the job. You can no longer let the phone ring in the hopes that the customer will give up. They *have* your number (pagers, voice mail, *my home number*). There is nothing quite like getting pinned to the coffee bar in a customer's lobby to be nibbled upon by the ducks.

I envy the inside position of being able to go down the hall to get the right answer to a question. And who can find time to write the Great American App. Note when half the day is spent being chased by the ducks on the customer's factory floor. But at the same time, there is a great sense of satisfaction that comes with being able to solve the customer's problem on the spot while looking for the next design-in opportunity.

Being in the field is a terrible job and a wonderful career all at the same time. I wouldn't trade my position in the "duck pond" for anything! Keep writing your column. I always look forward to a good sanity break.

GREG JURRENS
Compaq Field Applications Engineering Specialist
NEC Electronics Inc.
Houston, Texas

It's fun being an Apps. Engineer, but it's good to be able to take a break occasionally! –RAP

Dear Bob:

Just read Pease Porridge in the February 6th issue. Since the late '60s, I have had 25 W of power amplifier in seven cars with a speaker behind the front grille.

I use this to tell drivers of faulty lights, no right turn where necessary (left turn in your case), "move over dum dum," etc. In case of retribution, I usually look around to see where the voice originates. " 'Allo darlin' " to an old lady makes her day! "Oi mate!" makes pedestrians turn round, etc., etc. Great fun!

DAVE ST. GEORGE
St. George Electronics
London, England

A great idea! Even in California you can do this legally, but don't blast too loud. Check your local ordinances! –RAP

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Call or fax your request today for your fact-filled Cache Data Pack.

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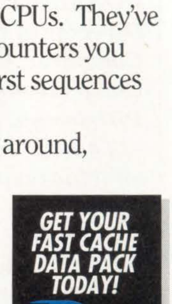


CYPRESS SEMICONDUCTOR

*In Europe fax your request to the above dept. at (32) 2-652-1504 or call (32) 2-652-0270. In Asia fax to the above dept. at 1 (415) 961-4201. 3901 North First Street, San Jose CA 95134. Phone: 1 (408) 943-2600, Telex 821032 CYPRESS SNJ UD, TWX: 910-997-0753. SPARC is a registered trademark of SPARC International, Inc. Products bearing the SPARC trademark are based on an architecture developed by Sun Microsystems, Inc.

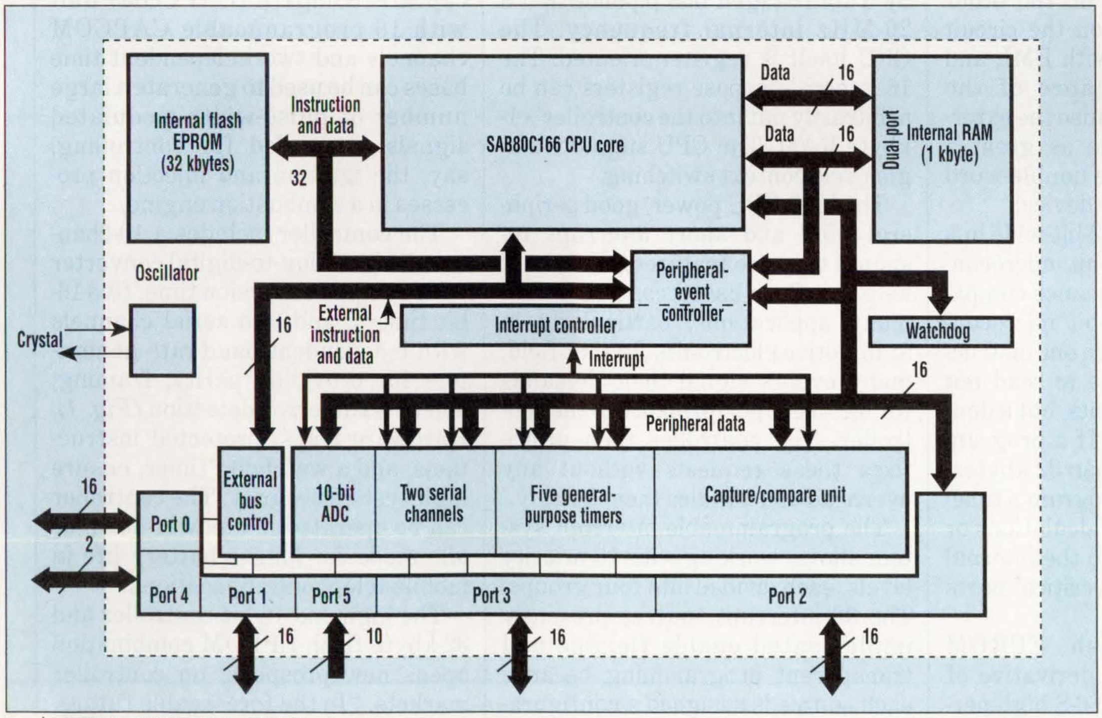
IC Merges 32-kbyte Flash EPROM With 16-Bit Micro

European-Developed Microcontroller Has Extensive Peripheral Set And Can Be Reprogrammed Even When In-System.

John Gosch

Suppose there's a serious error in the firmware that a car maker has programmed into a microcontroller for a series of vehicles. If that error leads to poor brake action or faulty engine control, the damage for the producer could be substantial—settling claims for compensation, as well as recalling the parts. Faulty ROM-based and one-time-programmable (OTP) controllers must be replaced, and EPROM versions erased, reprogrammed, and sent back to the end user.

All this will soon be a thing of the past. Two European companies, Germany's Siemens AG and the Italian-French company SGS-Thomson Microelectronics, have jointly developed a 16-bit microcontroller with an on-chip 32-kbyte flash EPROM. Using a personal computer, the customer can change the firmware via an interface, with the controller remaining in the system. Thus, a systems designer or field engineer can update or correct the firmware without going to the trouble of altering the hardware.



1. BOTH A CPU and a 32-kbyte flash EPROM reside on the SAB88C166-5S/ST10F166 IC from Siemens and SGS-Thomson. The device also incorporates a capture/compare unit, a 10-bit ADC, five 16-bit general-purpose timers, and two serial channels. Hardware traps, protected instructions, and a watchdog timer, ensure high system security.

The new flash-EPROM controller is the first result of a cooperative deal the two companies made in 1990. The device combines the 16-bit microcontroller SAB80C166 from Munich-based Siemens and the 32-kbyte flash EPROM from SGS-Thomson in Milan on the same chip. The German company calls the new controller the SAB88C166-5S; SGS-Thomson has designated it the ST10F166.

In addition to easy updating and correcting the firmware, the flash-based controller can serve as a design-in tool for Siemens' recently announced SAB83C166-5S, a 16-bit microcontroller with a 32-kbyte ROM.

In developing a product, it's necessary to change the program to stabilize the code. Given its large number of programming cycles and short write/erase times, the flash-based controller can be used to quickly optimize the code.

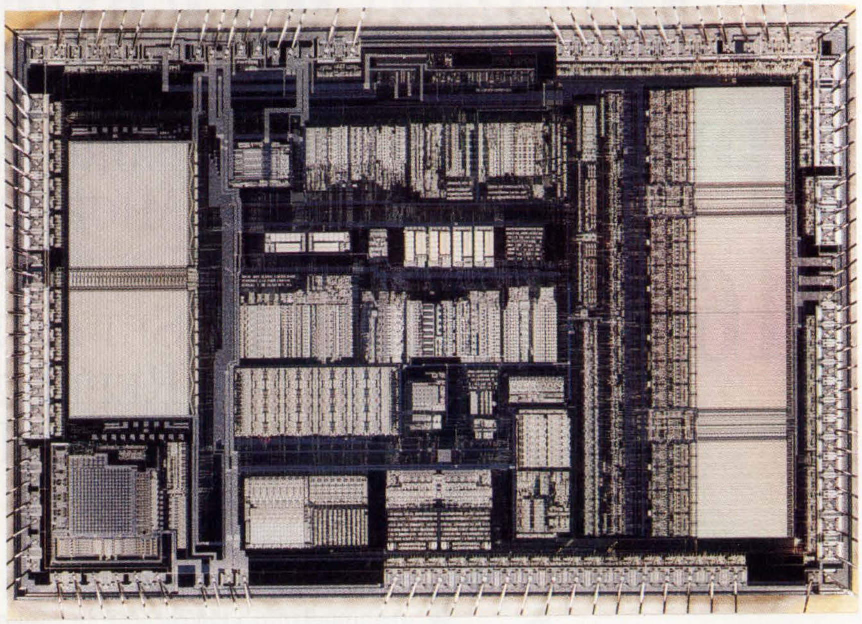
One U.S. chip maker has announced a 32-bit microcontroller also with a 32-kbyte flash EPROM, but that device will not be available before 1993. The 88C166/ST10F166, on the other hand, will be available in sample quantities in a few months.

The 32-kbyte flash EPROM (and the 32-kbyte ROM of the 83C166) meets the growing demand for more memory capacity in microcontrollers. Today's high-level languages, RISC-like instruction sets, and the rising complexity of programs and applications mean that more program lines are needed.

Integrating non-volatile memory into a controller, instead of having memory external to it, offers several advantages. For one, at high frequencies an internal bus to an internal memory reduces EMI. For another, an internal bus can handle a greater word length. Furthermore, an internal memory is space-saving. An external memory, on the other hand, calls for space on the circuit board, needs to cope with EMI, and impairs the performance of the 88C166/ST10F166 because the external bus cannot handle as great a word length as can the double-word internal bus of the new device.

With their internal 32-bit-wide bus systems, the new 16-bit microcontrollers sport a performance comparable to that of a 32-bit microcontroller. That's because in one instruction cycle it is possible to read not only one word with 16 bits, but a double word with 32 bits. If a program needs more memory than 32 kbytes, it's useful to put the program's time-critical parts, such as calculations or operating systems, into the internal memory, and non-time-critical parts into an external one.

The 32-kbyte flash EPROM 88C166/ST10F166 is a derivative of the Siemens' SAB80C166-S high-performance 16-bit microcontroller. The latter, because of its high CPU performance, fast interrupt response time (400 ns), and intelligent peripheral mix, has gained wide acceptance in industrial, automotive, and telecommunications applications.



2. A SINGLE CHIP, the Siemens/SGS-Thomson SAB88C166-5S/ST10F166 controller holds both a 16-bit microcontroller and a 32-kbyte flash EPROM. The device is made in a 1.2-μm CMOS n-well process.

Incorporating the best features of the 80C166, the flash-based controller achieves immediate processing by a four-staged bus pipeline and a 20-MHz internal frequency. The CPU itself is register-oriented. The 16 general-purpose registers can be arbitrarily put into the controller's 1-kbyte RAM. The CPU supports single-cycle context switching.

The high CPU power, good peripheral mix, and short interrupt response time are features that should help the flash-based controller find many applications, particularly in automotive electronics. In that field, many events signal their demands for interrupt performance to the controller. The controller then prioritizes these requests without any overhead and handles them quickly.

The programmable interrupt system allows working with 16 priority levels, each divided into four groups. The 32 interrupt sources presently implemented enable flexible and transparent programming because each source is assigned a configuration register and an interrupt address. The interrupt system is advantageous in disk drives and mobile telephones, where many event-driven tasks must be prioritized.

In embedded control applications, it's necessary to support the high CPU and interrupt performance with an appropriate set of on-chip peripheral systems. The controller's capture/compare (CAPCOM) unit with 16 programmable CAPCOM channels and two independent time bases can be used to generate a large number of pulse-width-modulated signals as needed for controlling, say, the ignition and injection processes in a combustion engine.

The controller includes a 10-channel 10-bit analog-to-digital converter with a 10-μs conversion time, five 16-bit timers, and two serial channels with independent baud-rate generators for providing parity, framing, and overrun error detection *(Fig. 1)*. Hardware traps, protected instructions, and a watchdog timer, ensure high system security. The controller can be operated in a power-down or idle mode for longer battery life in mobile-telephone applications.

The high-end 16-bit controller and 32-kbyte flash-EPROM combination opens new prospects on controller markets. "In the foreseeable future, this concept should win out over OTP and EPROM-only solutions," says Thomas Staudinger, microcontroller product marketing manager in Sie-

mens' Semiconductor Group. "Speaking for flash technology are reprogrammability, in-system programming, and the bank-erase feature," he adds.

Compared to OTP controllers, flash-EPROM versions have several advantages: Flash EPROMs can be programmed up to 1000 times and programming is possible in-system. OTPs, by contrast, can be programmed just once because they're not erasable. If the firmware needs to be changed, OTPs must be replaced. In the long run, Staudinger says that the flash-based controller's price will approach that of OTPs.

Flash-EPROM controllers also beat conventional EPROM versions in several respects. Being electrically erasable, they can be erased in just one second. Furthermore, it's possible to erase specific memory sections in a so-called bank-erase operation. Conventional EPROM controllers, on the other hand, can be erased only with ultraviolet light, and that can take from 10 to 20 minutes. Bank-erasing is not possible.

What's more, EPROM versions have about ten times fewer programming cycles and require a special programming board, which increases the development costs. Another disadvantage is the high price of the EPROM version's ceramic package. In the future, as chip costs decline, the cost of the ceramic package will become an ever greater price-determining factor.

The 88C166/ST10F166 conveniently supports a microcontroller's development and prototyping phases. The developer can change the program up to 1000 times (up to 10,000 times with the next generation of flash-based controllers) and thus optimize the code. Without any waiting periods or mask alterations, the firmware can be stabilized until the mask has no more errors. Write times of 100 μs per word or double word, and erase times of typically 1 second, ensure fast alterations.

With the flash-based controller installed in the system, codes can be altered without new masks and hence without any waiting periods. This makes it possible to react faster to market demands. The flash-based controller also eases logistics problems. The same device can be used for development and production.

The flash memory can be controlled in four different modes. The erase mode, in addition to its erase function, verifies that the cells were properly erased. Another mode is for checking for correct programming, and is part of the programming-mode's task. The read-only mode processes the program, and an external mode is used to communicate with external memories. The 8k-word by 32-bit memory has redundant cells. A redundancy logic feature checks whether the memory's individual cell columns work correctly. In case of a fault, a redundant column is picked.

The memory is divided into four banks: one 2-kbyte, one 6-kbyte and two 12-kbyte banks. The two smaller banks store parameters and data while the two 12-kbyte banks store codes. The banks can be erased separately, a significant feature, especially in automotive electronics for updating the firmware. For example, in engine-control applications, the firmware can be adapted to country-specific regulations just by reprogramming part of the memory. While the two 12-kbyte banks contain the same program for all applications, the small memory banks contain the country-specific firmware.

The flash-based controller can be programmed by a host—for example, a PC—and a programming card through a serial or parallel interface. Suitable programming cards will be available around mid-year. The cards can also be used as test boards. In-system programming is also possible with external memories or an on-chip bootstrap loader. The latter initiates the loading of program algorithms into an internal RAM. The algorithms contain routines for programming, erasing, and verification.

Many users may wish to protect their firmware against unauthorized copying or altering. For this purpose, the controller has a read-protection facility, which can be programmed to ensure code security.

The 88C166/ST10F166 is made in a 1.2-μm CMOS n-well process with two metal layers and a double-polysilicon gate *(Fig. 2)*. Cell programming is based on hot-electron injection, where the control gate and drain are set to a high potential, and the source to ground. The high drain voltage generates "hot" electrons, which the high control gate voltage pulls into the floating gate.

The basis for erasing is the Fowler-Nordheim tunnel effect. To achieve it, the control gate is grounded while the drain is disconnected and the source is at a high potential. The high electric field between the floating gate and the source removes electrons from the floating gate. The memory's data retention time is ten years.

An extensive line-up of tools is available for the controller. In cooperation with Siemens, the German company Tasking recently came out with a high-performance C compiler. In addition, there are tools that support Modula-2 and Forth languages. Users can also resort to a macro-assembler, linker, library manager, and object-to-hex converter. The library is supplemented by support tools, such as debugger boards, simulators for the CPU and the on-chip peripherals, and real-time in-circuit emulators from well-known software and hardware producers.☐

PRICE AND AVAILABILITY

The Siemens/SGS-Thomson SAB88C166-5S/ST10F166 16-bit 32-kbyte flash-EPROM microcontroller comes in a plastic BQFP100 package and will be available in sample quantities during the second half of this year. Volume production will start in early-1993—the device will then be available also in a plastic MQPF100 package. Sample price is about $110 each. In 1993, the price will be $52 each in quantities of 1000 units. The Siemens SAB83C166-5S 32-kbyte ROM-based 16-bit microcontroller will be available in volume quantities around mid-year for about $47 each in quantities of 1000 units.

In the U.S.: Siemens Components Inc., 2191 Laurelwood Rd., Santa Clara, Calif. 95054; (408) 980-4583. SGS-Thomson Microelectronics, 1000 E. Bell Rd., Phoenix, Ariz. 85022; (602) 867-6228. **CIRCLE 512**

In Europe: Siemens AG, Semiconductor Group, P.O. Box 801709, D-8000 Munich 80, Germany. Tel.: (089) 4144-5320. Fax: (089) 4144-8473. SGS-Thomson Microelectronics, I-20041 Agrate Brianza, Via C. Olivetti 2, Italy. (039) 39-6035-597.

CIRCLE 513

HOW VALUABLE?	CIRCLE
HIGHLY	538
MODERATELY	539
SLIGHTLY	540

SOFTWARE CREATES ANALOG, MIXED-SIGNAL IC TESTS

TEST DEVELOPMENT TAKES LESS TIME WITH A DESIGN-TO-TEST ENVIRONMENT THAT LETS DESIGN AND TEST ENGINEERS WORK TOGETHER.

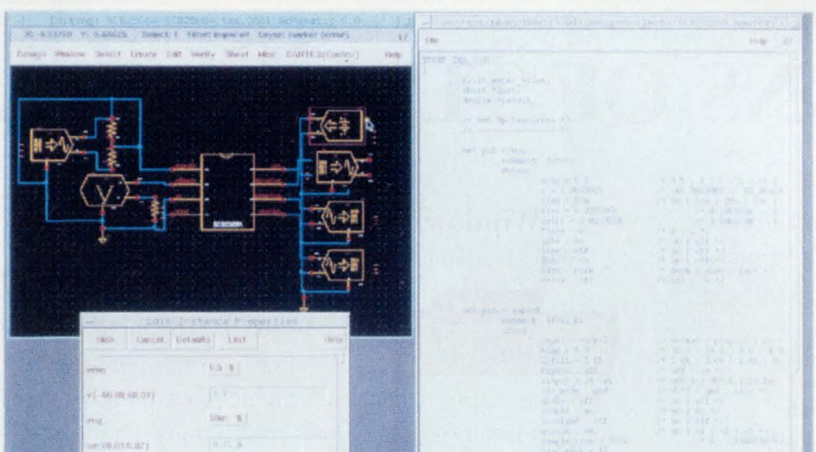
JOHN NOVELLINO

Electronic-design-automation tools have slashed design cycle times to a minimum. There's little room left in the design phase to significantly cut overall product-development time. That leaves the test phase as the bottleneck where great gains in time-to-market can still be made. Although a number of tools are available to help digital engineers reduce test-development time, and even to consider test-development and testability issues in the design phase, until now analog and mixed-signal engineers were left out in the cold.

Into this breach steps Dantes (Design and Test Engineering System), an integrated design and test environment and a toolset for developing tests for analog and mixed-signal ICs. Because the test tools are tightly integrated with the design tools, Dantes lets engineers consider test parameters, tester specifications, and testability issues during the design cycle, rather than at its end. That capability achieves the much talked about but elusive goal of concurrent engineering. The end result: a final test program targeted at a specific tester.

According to the developer, Cadence Design Systems, San Jose, Dantes can cut an analog or mixed-signal test-development cycle from a typical six months to as little as two or three months—a 30% to 60% reduction. In addition, engineers can prioritize test modules, placing high-dropout and short-duration tests first to reduce overall test times.

Because Dantes stores information in a format design and test engineers can understand and use, both disciplines can work on the project at the same time. And passing of information between the design and test phases is transparent, because Dantes is built on a common framework environment, Cadence's Design Framework II. The product is sold as an option to the company's Analog Artist Design System. This tight integration of design and test tools creates a single point of entry into the database, which further cuts development time. The kit's tools address design-for-testability, tester rule checking, resource modeling, environment simulation, and automatic test-program generation. Bascially, the tools help engineers create a group of test-module schematics (TMS) and then compile them into a



1. A TEST-MODULE SCHEMATIC **(upper left) represents a specific test. Dantes matches the TMS against a specific tester's resources (lower left), then generates code for that tester (right).**

full test schematic (FTS). The source-code generator then automatically writes the needed code in the target-tester's language *(Fig. 1)*.

Obviously, Dantes requires an in-depth knowledge of the user's automatic test equipment (ATE). In fact, ATE vendors played an important role in the product's development. For instance, the tester symbol library represents every tester resource. Although the symbols can be considered generic, the specific functions and properties of each symbol are tester-specific.

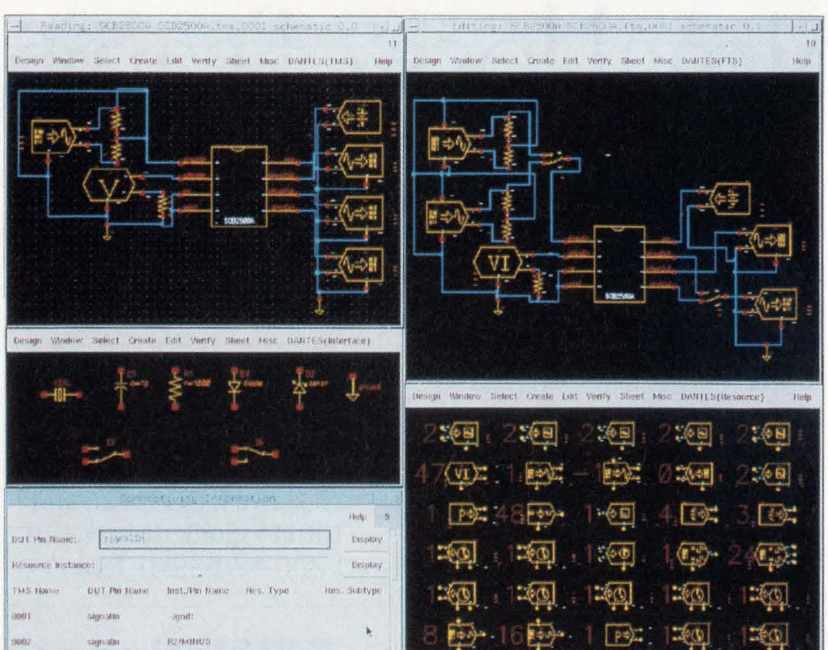
The tester specification file brings that same level of detail to the actual tester to be used. The file includes the type, number, and parameters of every resource, and tester specifications like voltage-supply ranges, and operating frequencies. A rule checker takes the TMS or FTS, compares it to the tester file, and ensures that the schematics don't call for resources or parameters the ATE can't provide. Users can even develop models for the functions in the tester symbol library and for the device under test (DUT). With these models, the tester resource, DUT, and load board can be simulated, so they can be assessed even before the DUT is created. Dantes' mixed-signal simulation net lister automatically partitions and sends separate net lists to the circuit- and logic-simulation engines. Users get full interactivity with both simulators and an integrated waveform display system that shows digital and analog signals in the same window.

Each TMS represents one test module—one set of connections between the tester and DUT. It can also represent more than one test. As such, it contains the needed tester functions and a symbolic abstraction of the DUT. A schematic editor helps to capture the schematics.

After individual test-module schematics are captured, the FTS composer tool i used to create a top-level schematic that includes the TMSs and the relays, DUT connections, and interface circuitry. For each TMS, the FTS composer supplies data such as connectivity for each pin on the DUT or on every tester resource. Windows show the user the type and number of resources remaining and a library of common interface structures. Engineers can also create their own library of frequently used interfaces.

Next, the test sequencer allows users to arrange or rearrange the test order. The optimum sequence depends on test time, setup conditions, and the number of faults expected. Finally, the source-code generator creates the main test program, using the FTS and the sequencer tool *(Fig. 2)*. The software uses parameters entered under each tester symbol to supply setup conditions, such as resource setting, loading, storing, connecting or disconnecting, initializing, and starting. The test program can be optimized later by modifying it in the tester environment. Dantes doesn't try to duplicate capabilities already in the ATE software.

Dantes was developed from a direct request by a Cadence customer, Harris Semiconductor. A few years ago, Harris worked with Cadence, Hewlett-Packard, and Teradyne to create simulation macromodels and schematic-capture interfaces that could help test-development engineers. Based on the results of that work, Harris urged Cadence to develop a unified design-to-test product for analog and mixed-signal ICs and even contributed initial funding for the project. Cadence continued the work with Harris and other Cadence Analog Alliance Partners, who contributed their desired specifications and testing criteria. The project also included Hewlett-Packard, LTX, Teradyne, and Yokagawa—ATE vendors who supplied tester-specific data. The first testers that Dantes works with are the HP 9480, the LTX Synchromaster, the Teradyne A500 series, and the Yokagawa TS-1000.☐



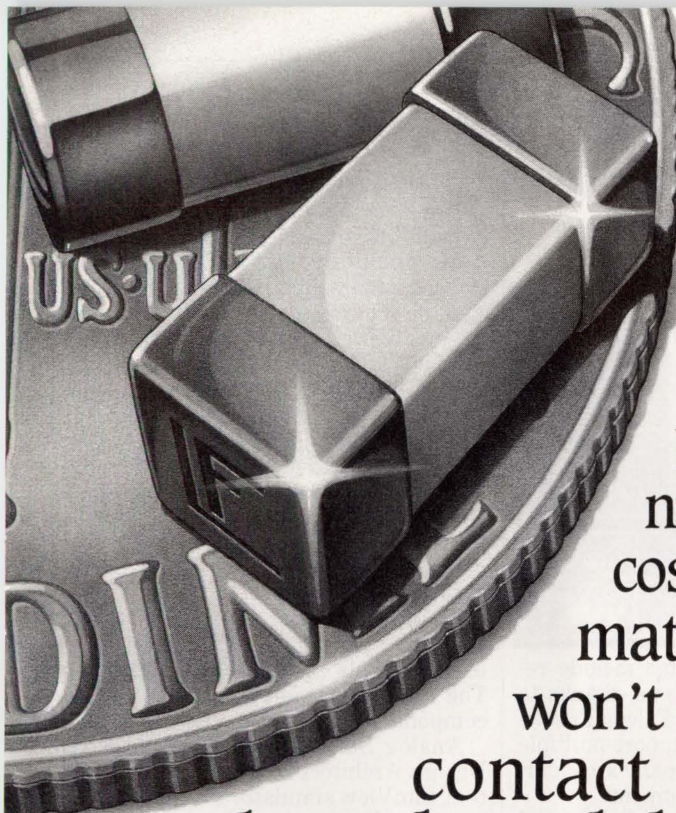
2. THESE FIVE WINDOWS **illustrate tools used to compose a full test schematic. At left, top to bottom, are a test-module schematic, typical load-board components stored in a component library, and connectivity information. A resource counter (bottom right) shows which tester resources remain as the FTS is constructed. The FTS is constructed by copying the individual devices into the composing window (upper right).**

PRICE AND AVAILABILITY

Dantes will be available in the third quarter for $80,000. The first tester models, which must be purchased separately, will be from Hewlett-Packard, LTC, Teradyne, and Yokagowa. Other vendors are scheduled to release models next year.

Cadence Design Systems Inc., 555 River Oaks Pkwy., San Jose, CA 95134; (408) 943-1234. **CIRCLE 514**

HOW VALUABLE?	**CIRCLE**
HIGHLY	541
MODERATELY	542
SLIGHTLY	543



NANO^2™ SMF Fuse
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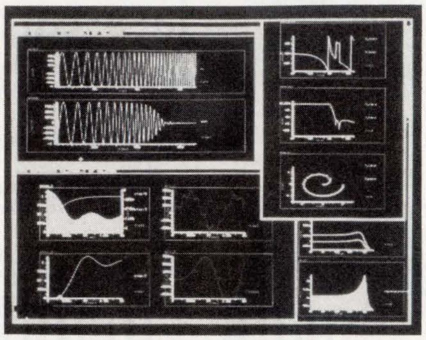
ENHANCED ANALOG/MIXED-SIGNAL SOFTWARE ADDS TWO NEW TOOLS

An analog interface kit and a switched-capacitor simulator are two new tools found in Mentor Graphics' enhanced suite of products for analog and mixed-signal design. All the tools have a common analog user interface, and provide help at the IC, pc-board, and system levels.

The Analog Interface Kit is an interactive, graphical front end for Spice and Spice-like simulators that enables users and third-party Spice vendors to integrate their own analog simulators into the Mentor Graphics environment. It includes a suite of post-processing and analysis capabilities for viewing and analyzing simulation results of analog and mixed-signal designs.

Also being offered is the SCAP tool, touted as the only commercial switched-capacitor simulator that works for both filter and non-filter applications. The tool can simulate circuits such as phase-locked loops, sigma-delta modulators, and a-d converters in a thousandth of the time required by Spice-based simulators.

Enhancements to the company's existing analog-product line include reduced design-iteration time, thanks to full integration into the Falcon Framework. The tools also support multiple platforms and the company's concurrent-engineering environment.



Mentor's analog and mixed-signal design solutions are based on a number of key building blocks. One, the Analog Station, provides a design and analysis environment from schematic editing through circuit simulation to statistical post-processing. It integrates the Design Architect schematic editor and the AccuSim analog-circuit simulator through the Falcon Framework.

The AccuSim analog simulator executes a broad range of analysis functions including dc solutions and sweeps, small-signal ac analysis, transient simulation, noise analysis, ac and dc sensitivity analysis, and dc-transfer functions. The simulator draws on the System Modeling Blocks library, which contains over 120 high-level blocks for top-down design. Blocks include mathematical operations, frequency-domain functions, piecewise-linear functions, and time-domain functions. It also offers more than 40 generic circuit elements from ideal switches to a-d and d-a converters.

The AccuParts analog-parts library gives users a large selection of widely-used symbols and simulation models. The library provides more than 4900 component models.

Analog Station, which includes the Design Architect schematic-entry system, SimView simulator user interface, and AccuSim analog simulator, costs $44,900. The AccuParts library goes for $9900 and the SCAP switched-capacitor simulator sells for $25,000. The Analog Interface Kit costs $11,900.

***Mentor Graphics Corp.**, 8005 S.W. Boeckman Rd., Wilsonville, OR 97070-7777; (503) 685-7000.*

CIRCLE 461

■ *LISA MALINIAK*

XILINX USERS CAN GET SOFTWARE UPGRADE

A three-month upgrade program that began in April lets existing Xilinx users upgrade to Exemplar Logic's design software for only $495. The Exemplar software, called the Complete Optimization/Retargeting Environment (CORE), combines vendor-independent design synthesis with technology-specific optimization software for FPGA design. Previously, Xilinx customers received Exemplar's PDS2XNF and XNFOPT products from Xilinx as part of an integrated front-end software environment. However, Exemplar and Xilinx ended their three-year OEM relationship in March. CORE supports Xilinx's 2000, 3000, and 4000 FPGA families. It accepts multiple design-entry methods, including schematics, net lists, hardware description languages, and Boolean equations. CORE runs on DOS- and Unix-based computers. Without the upgrade deal, pricing starts at $8000. Xilinx customers interested in the upgrade should call Larry Lapides, director of product management, at (800) 552-FPGA.

Exemplar Logic Inc., 2550 Ninth St., Suite 102, Berkeley, CA 94710; (510) 849-0937. CIRCLE 462

MIXED-MODE SYSTEM RUNS UNDER WINDOWS 3.0

Design Center version 5.1 gives engineers a complete PC-based analog and digital circuit-design environment running under Windows 3.0. The system includes PSpice, an analog and digital circuit simulator; Probe, a high-resolution graphical waveform analyzer; and a schematic-capture program. All software is written as full Windows 3.0 applications. Engineers using version 5.1 can simulate and analyze circuits from within the schematic environment. They can also display voltage, current, and digital waveforms by marking pins, wires, and devices directly on the circuit drawing. In addition, selected features sold as options in previous software versions are now standard with version 5.1. These include analog behavioral modeling, Monte Carlo and sensitivity/worst-case analyses, digital simulation in PSpice, and graphical waveform analysis with Probe. Design Center 5.1 is available now, and runs under Windows 3.0. It costs $8200 for IBM and IBM-compatible PCs, and $10,725 for the NEC PC.

MicroSim Corp., 20 Fairbanks, Irvine, CA 92718; (714) 770-3022 or (800) 245-3022. CIRCLE 463

UPGRADED PCB TOOLS LAY OUT COMPLEX BOARDS

The newest version of Scicards pc-board software addresses the needs of complex, high-speed digital and analog board layout. New features include a gridless editor that provides push-and-shove operation with on-line design-rule checking. The editor, optimized for speed, intelligently shuffles trace interconnect to find the best result. On-line design rule checking performs physical and logical evaluation of split planes and metal areas. In addition, many of the interactive design features have faster, more user-friendly graphics. Automatic test-point generation and output facilitate automatic testing of dense surface-mounted and through-hole boards. Users define test points with features and sizes. Then the software automatically inserts the test points during editing and autorouting. Scicards Version 27 runs on many popular Unix platforms, including the HP 700 series workstations. The Scicards pc-board software is available now for $45,000.

Harris/Scientific Calculations Div., 7796 Victor-Mendon Rd., P. O. Box H, Fishers, NY 14453; (716) 924-9303. CIRCLE 464

PC COMPATIBLE'S PERFORMANCE BEATS COMPETITION

A family of workstations and servers from Mips Computer Systems brings PC compatibility to RISC-based systems. The company claims that its ARCSystem family delivers two to four times the performance of 50-MHz 486-based PCs at comparable prices. ARC is the Advanced RISC Computing hardware specification set by the Advanced Computing Environment initiative that includes the Mips R4000 processor.

The family consists of two lines, the Magnum 4000 ARC PCs and the Millennium 4000 ARC servers. The initial members are called the PC-50 and the SC-67. The PC-50s are based on the primary cache version of the R4000 and deliver 40 SPECmarks of performance. The SC-67s are powered by the secondary cache version of the R4000.

Because of the systems' ACE compliance, they run both Unix and Windows NT operating systems. RISC/os 5.0 also runs on the systems, opening the door to 1300 applications.

The Magnum PC-50 comes with 8 to 256 Mbytes of RAM, a SCSI-II interface, and 32-bit Ethernet. The Millennium PC-50 is similar, yet it adds eight peripheral compartments, four EISA slots, and a 390-W power supply. Both SC-67s are similar to their PC-50 counterparts but with the faster CPUs.

Mips Computer Systems Inc., 950 DeGuigne Dr., Sunnyvale, CA 94086; (408) 720-1700. **CIRCLE 465**

■ *RICHARD NASS*

LASER PRINTER HANDLES 8 PAGES/MIN.

The first in a line of non-impact low-cost printers, the Finale 8000 features an 8-page/min. engine. At $1995, the printer is built around Intel's i960 32-bit RISC processor and features six resident emulations, 2 Mbytes of RAM, and an auto-emulation protocol that automatically interprets incoming printer languages and transparently switches emulations. Included are 8 scalable and 14 bit-mapped fonts. An upgrade kit, available in October, contains PostScript Level 2 compatibility, 600 dots/in. gray scaling, and a 4-Mbyte SIMM module.

Samsung Electronics America Inc., 301 Mayhill St., Saddle Brook, NJ 07662; (201) 587-9600. **CIRCLE 466**

NOTEBOOK PC CONTAINS REMOVABLE HARD DRIVE

The NoteMaster 386S/25 notebook PC has a removable, industry-standard 2.5-in. hard drive. A 2.5-in. drive of any capacity fits into the casing supplied by Samsung. Then the drive slides in and out of the portable PC. Users can also buy a receptacle to put into their desktop PCs that lets them use the removable hard drive. Software that accompanies the receptacle alerts the PC that the companion drive is present in the system. The NoteMaster 386S/25 features a 25-MHz 80386SXL processor, a 10-in. back-lit 640 by 480 VGA LCD with 64 shades of gray, and a 3.5-in. floppy drive.

Samsung Electronics America Inc., 301 Mayhill St., Saddle Brook, NJ 07662; (201) 587-9600. **CIRCLE 467**

Sneak Preview of a 1992 Motorola OPTO Customer.

Since we're almost but not quite ready to preview some of our exciting new OPTO products, we hope you'll settle for a sneak peek at one of our new, highly satisfied OPTO customers. Sure we're bragging a bit—but with good reason. With a track record in Optoisolation technology as long and solid as ours, we can be confident that our new OPTO products will not only delight our current customers, but win over new ones, too.

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...and we'll back you in the future!

Space and modesty prevent us from listing the numerous other contributions that over the years have helped earn Motorola a reputation for meeting the needs of our customers with high-quality products and service. And even as you read this, Motorola Optoelectronic engineers are busily working on exciting new optoisolation products to meet ever-changing and growing new needs.

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For details on exciting new OPTO products and features that we're betting will keep or make you a satisfied Motorola customer, look for our next ad. To receive valuable information *now,* send the coupon below, write Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036, or call 1-602-BIG-OPTO.

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Please send me the following:

☐ 1992 Optoelectronics Selector Guide and Cross Reference #SG87/D, Rev.7.
☐ Information on Global Isolators.
☐ Information on the 8-pin surface mount optoisolators.

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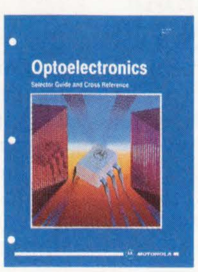

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REAL-TIME UNIX MAXIMIZES FLEXIBILITY, GAINS PORTABILITY

Designed for distributed real-time computer systems, the Aria Unix operating system from Integrated Systems Inc. contains features for advanced distributed and hierarchical real-time architectures. It merges real-time attributes with a set of portable, partitioned Unix services. System designers can allocate these services in various configurations over multiple sites, using an industry-standard interface. Aria offers an extended range of functionality in a deterministic, responsive, and open systems environment. Suitable applications for the operating system include control engineering, communications, manufacturing, and automation.

The scalable, binary Unix kernel is compatible with Unix System V, Release 3.2. By adding or deleting services and utilities, developers can create solutions that are tailored to fit the requirements of a specific site or node. Embedded applications can be written, tested, and debugged using a programming methodology that remains consistent at each level of the system's hierarchy.

The initial product, available in the second quarter, operates on the 68030-based Motorola MVME147S series of single-board computers. Other versions will be come later in the year. The kernel comes with device drivers for the MVME147S, networking software, and debugging tools. It sells for $9000. A site license costs about $35 for large quantities.

Integrated Systems Inc.*, 3260 Jay St., Santa Clara, CA 95054; (408) 980-1500.* **CIRCLE 468**

■ *RICHARD NASS*

SCO UNIX VERSION 4.0 INCREASES MEMORY SUPPORT

In Version 4.0 of the SCO Unix operating system, users get a higher system capacity, more network and device support, and a simpler system to use. Also, the development system has been optimized to improve productivity for software developers. The menu-driven interface makes it easy to use the software without having to learn any Unix commands. Because of support for boot-time loadable drivers, developers can add device support during the installation process without direct involvement from SCO. The time required for installation is greatly reduced when the software is supplied on a CD-ROM or a cartridge tape.

Version 4.0 includes support for 512 Mbytes of RAM, unlimited SCSI host bus adapters, seven disk drives for each adapter, and drives larger than 1.2 Gbytes. When combined with the SCO MPX multiprocessor extension, up to 30 processors can be employed. The development system contains improved tools, updated libraries, new documentation, and enhanced standards compliance. With Version 4.0, users can order one package that supports all systems based on ISA, EISA, and MCA. Users of earlier versions of SCO Unix can take advantage of the built-in upgrade utility.

A two-user license sells for $595, while an unlimited user license costs $1295. The development system is priced at $1295. Version 4.0 upgrade packages are also available.

The Santa Cruz Operation Inc.*, 400 Encinal St., P. O. Box 1900 Santa Cruz, CA 95061; (408) 425-7222.* **CIRCLE 469**

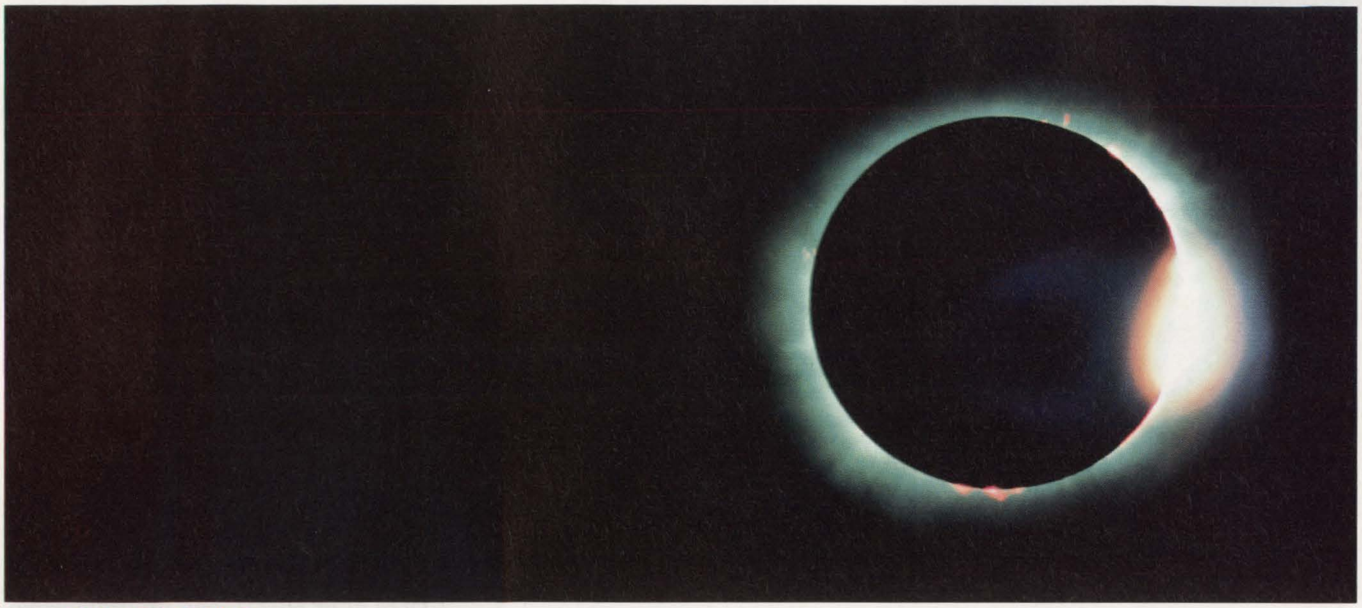
■ *RICHARD NASS*

RUN MULTIMEDIA SOFTWARE ON A PC

Interactive multimedia presentations can be displayed on a desktop or portable PC at a relatively low cost using the Ask-Me 2000 software package. Applications can be displayed on any standard VGA display or on a touch screen to get user feedback. The easy-to-use software is suitable for presentations, engineering simulations, or training purposes.

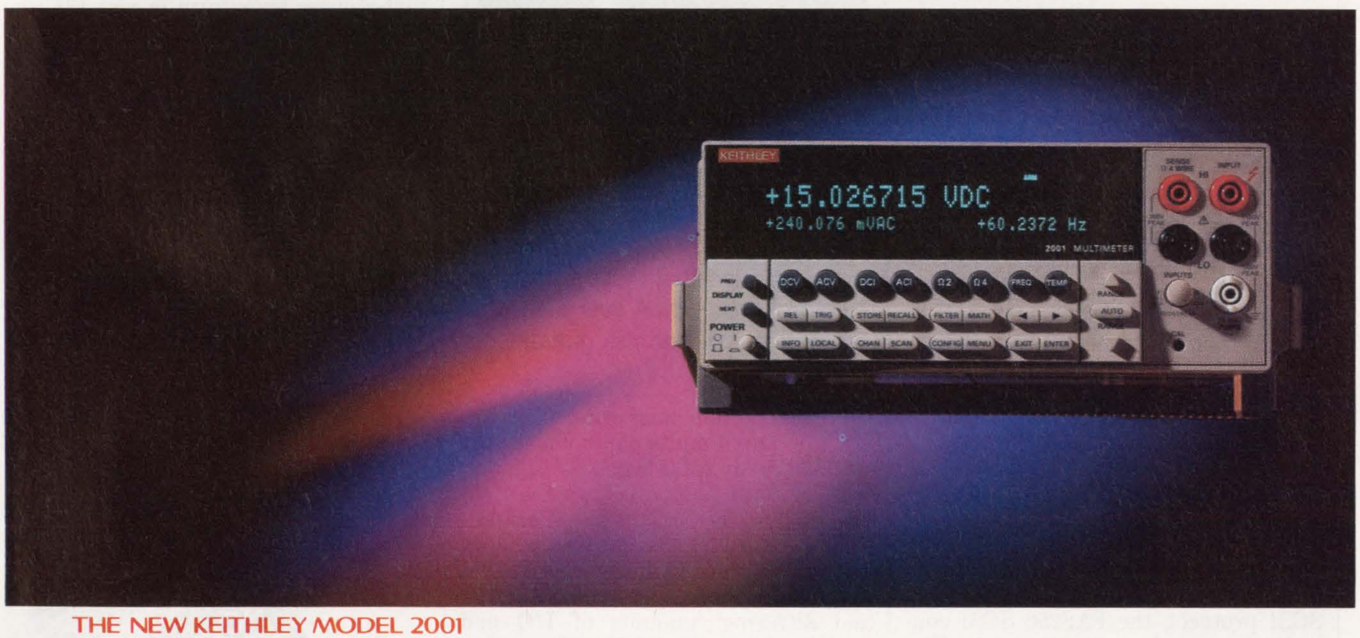
Ask-Me 2000 is compatible with most popular paint and animation programs as well as most audio- and video-capture boards. The software lists for $495.

Ask Me Information Center, NSC Tower 7900 Xerxes Ave. South, Suite 820, Bloomington, MN 55431; (800) 678-5511. **CIRCLE 470**



SOLAR ECLIPSE

A DMM like this doesn't come along very often, either.



THE NEW KEITHLEY MODEL 2001

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KEITHLEY INSTRUMENTS

CIRCLE 148 FOR U.S. RESPONSE   CIRCLE 149 FOR RESPONSE OUTSIDE THE U.S.

MEGABIT VRAMS TRIM PACKAGE SIZE AND POWER

Now available in a thin, small outline package (TSOP), a 1-Mbit video RAM has trimmed power consumption too. The M5M442256ATP, organized as 256 kwords by 4 bits, draws just 1 W, maximum when active, while drawing only 325 mW for random read operations and 200 mW for serial read/write operations. Also available is the MSM482128, organized as 128 kwords by 8 bits. The by-4 VRAM comes in a 28-lead standard or reverse TSOP (the reverse TSOP allows the use of top and bottom board mounting with minimal board relayout) as well as the previous 28-lead ZIP and SOJ packages. The by-8 VRAM comes in 44-lead standard and reverse TSOPs and a 40-lead SOJ package. In thousands the VRAMs sell for $8 apiece.

Mitsubishi Electronics America Inc., 1050 East Arques Ave., Sunnyvale, CA 94086; (408) 730-5900. CIRCLE 471

FAST AND WIDE SCSI IC DELIVERS 20 MBYTES/S

By using a 16-bit data path and the fast-SCSI protocol, the FAS256 SCSI controller can deliver 20 Mbytes/s. The chip provides the host and peripherals with a complete SCSI interface and maximizes SCSI data transfers by employing a command pipeline and hardware-based command sequences to minimize host-processor intervention. The chip also provides automatic handling of SCSI-2 messages, thus further offloading the host CPU. Asynchronous data transfers are possible at sustained rates of up to 7 Mbytes/s, while the synchronous transfers can reach 20 Mbytes/s. On-chip asynchronous FIFO registers buffer the data and thus provide some elasticity for the system during data transfers. Samples of the FAS256 sell for $50, while in lots of 5000 the chip sells for $38 apiece.

Emulex Corp., 3545 Harbor Blvd., P. O. Box 6725, Costa Mesa, CA 92626; Gary DesRochers, (714) 662-5600. CIRCLE 472

EEPROM-BASED MCUS RUN 8051 SOFTWARE

A family of four EEPROM-based microcontrollers, software compatible with the popular Intel 8051 instruction set, allows users to electrically erase and reprogram the microcontroller in seconds while the circuit is still in the system. The four microcontrollers are actually small multichip modules that fit the already established 8051 pinout.

Included in the series are the SAB 80C515H-3J, 80C517H-3J, 83C515AH-5J, and 83C517AH-5J. The first two run at 12 MHz, pack 8 kbytes of EEPROM program storage, 256 bytes of RAM, and differing amounts of I/O and counter-timers. The 80C515H has eight 8-bit a-d converter inputs and comes in a 68-lead PLCC package, while the 80C517AH has 12 analog inputs, a seventh 8-bit parallel port, a second serial port and a 21-channel pulse-width modulated output capability (the 80C515H handles only 4 channels), which pushes the PLCC lead count up to 84 pins. The 83C515AH and 517AH both operate at 18 MHz and pack 32 kbytes of EEPROM storage.

One key difference between the 83C515AH and the 83C517AH microcontrollers is extra on-chip RAM—the first chip includes an extra 1-kbyte of data storage, while the 83C517AH packs an extra 2 kbytes. Prices, for single-unit samples of the microcontroller modules start at $345 for the 80C515H up to $390 for the 83C517AH. Samples are available now.

Siemens Corp., 2191 Laurelwood Rd., Santa Clara, CA 95054; Mike Rampelberg, (408) 980-4518. CIRCLE 473

REDUCED PRICES EASE DSP CHIP SET CHOICE

Now that yields are up and volume production has begun, prices for the multichip DSP chip set from Array Microsystems can be reduced by up to 20%. As a result, a DSP solution that consists of one digital array signal processor (a66110 or 66111), one programmable array controller (a66210 or 66211) and three of the recently released reconfigurable array store (a66311) chips sells for $1340/set in thousands. The chip configuration runs at 40 MHz and provides double buffering that permits real-time input and output when the chips implement a 1024-point complex fast-Fourier transform in just 131 μs. The recently released array-store chip is a multiport memory that contains 64 kbits of fast pipelined static RAM that can be configured to form four 1-kword by 16-bit, or two 1 k by 32, or two 2-k by 16, or one 2-k by 32-bit memories to support the storage needs for FFTs as large as 2048 points on a single chip.

Array Microsystems Inc., 1420 Quail Lake Loop, Colorado Springs, CO 80906; Doug Mitchell, (719) 540-7900. CIRCLE 474

MELCHER Industrial Power Supplies

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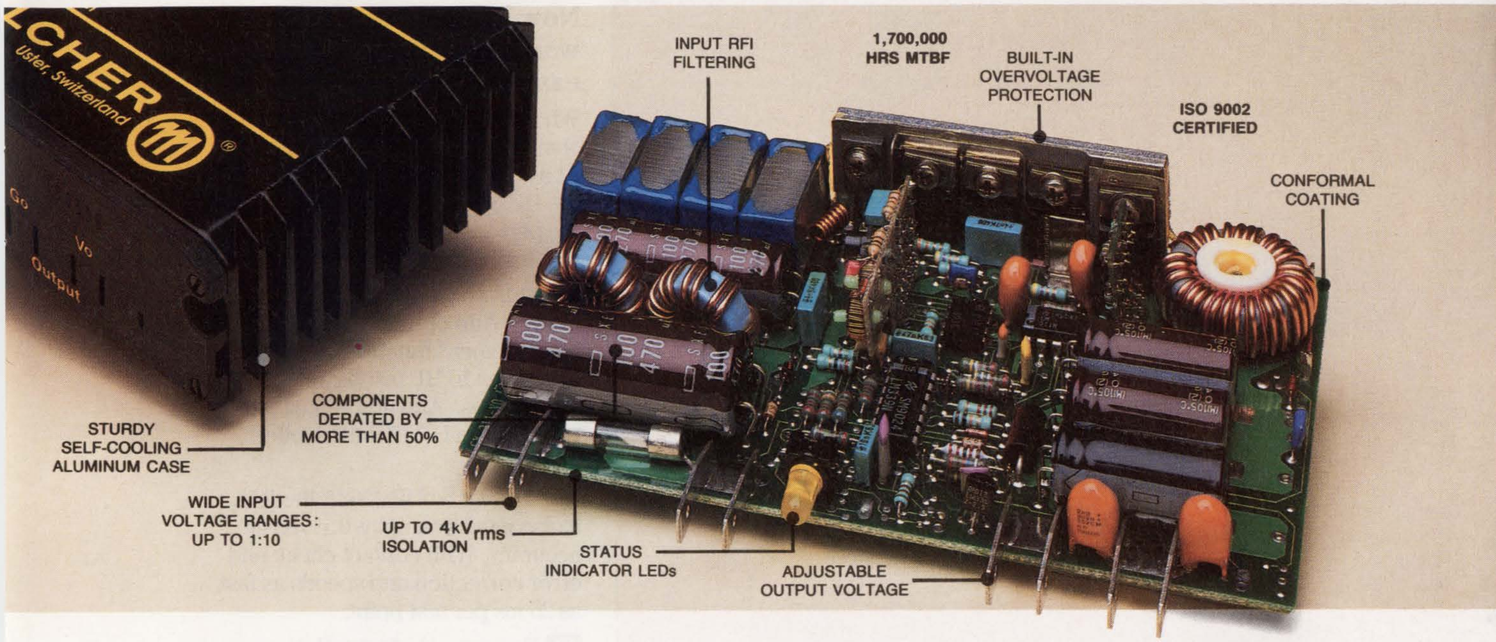

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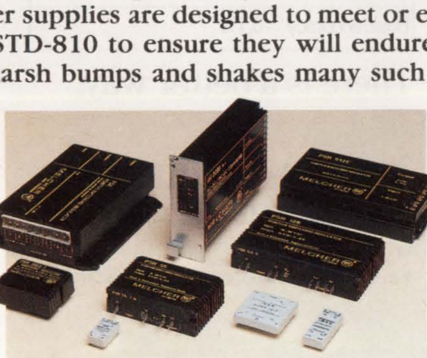

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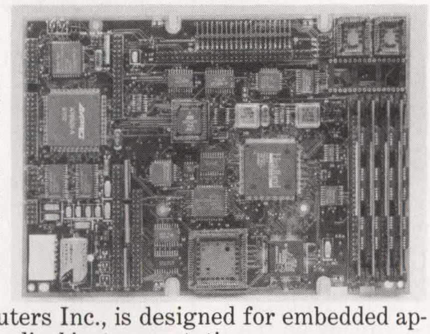
TINY SBC HAS FULL PC/AT FUNCTIONALITY



All the functions usually found on a full-size PC/AT motherboard have been squeezed down to a 5.75- by 8-in. single-board computer (SBC). The Little Board/386SX, from Ampro Computers Inc., is designed for embedded applications such as medical instrumentation.

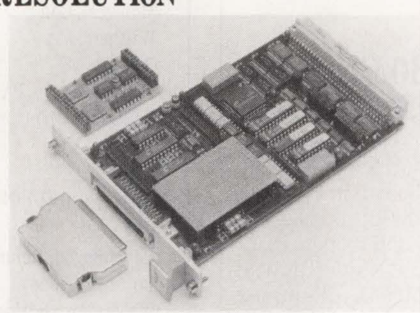
The 5-W board can hold up to 16 Mbytes of RAM. It has two serial ports, one parallel port, floppy and IDE hard disk-drive controllers, a SCSI interface, solid-state disk sockets, and a watch-dog timer. The board is compatible with the recently announced PC/104 embedded PC specification.

The Little Board/386SX is built with MiniModule expandability. That means that users can stack modules directly on the board to configure it for a specific function. The available modules include display controllers, communication interfaces, and I/O expansion. In quantities of 100, the board sells for $720.

***Ampro Computers Inc.**, 990 Almanor Ave., Sunnyvale, CA 94086; (408) 522-2100.* CIRCLE 475

■ *RICHARD NASS*

ADC MODULE FOR VMEBUS HAS 14/16-bit RESOLUTION



The VADI-3 from PEP Modular Computers is a high-resolution 14/16-bit analog-to-digital converter module. The single-height, single-slot VMEbus module is universally adaptable to all standard sensor types through various signal conditioning piggybacks. The VADI-3 is ideal for measuring low-frequency signals and temperatures in physical, chemical, and biological processes.

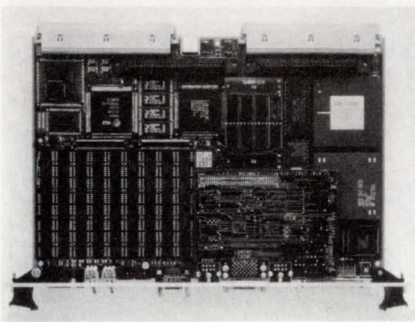
The board offers a conversion time of 125 milliseconds per channel. Depending on version, up to four channels can be selected in parallel. The word output rate is up to 4 kHz. The converter uses a charge-balancing or Sigma-Delta technique, combining the advantages of integration with a constant conversion time.

The board has fully opto-isolated analog and digital sections. The temperature sensor compensates for component temperature drift via software. A programmable 24-bit timer is used for internal and external triggering. The board's power consumption is typically 2.8 W. The VADI-3 is now available. The price in OEM quantities (including piggybacks) is $950.

PEP Modular Computers, P.O. Box 1652, D-8950 Kaufbeuren, Germany. Phone (0049) 8341-43020.
CIRCLE 476

SPARC-COMPATIBLE CPU BOARDS FIT VME FORM FACTOR

Two Sparc-based CPU boards, designed for embedded applications, are built to the standard 6U VME form factor. The two system boards, from Force Computers, incorporate the same Sparc chipset technology as Sun's SparcStations and run the same standard SunOS and Sparcware applications.



The CPU-2E fully implements a Sun SparcStation 2 for embedded SunOS and real-time applications. The board features Open Boot firmware, which allows dynamic reconfiguring of the computing environment and the use of a wide variety of peripherals with automatic booting of driver code to the operating system. The firmware also includes a Forth-based monitor and debugger. Force claims that the CPU-2E offers the first commercial implementation of the proposed IEEE P1014R source synchronous block-transfer method (SSBLT) protocol.

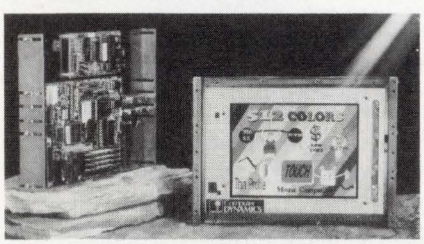
A memory card and two SBus I/O modules can be added using three built-in connectors. The memory-card adapter allows users to add 16 or 32 Mbytes to the 16 or 32 Mbytes already on the baseboard. The CPU-2E starts at $7995.

The CPU-2S is a high-speed, cost-effective solution for embedded control applications that don't require a system bus. With built-in SBus and SCSI expansion capabilities, the board simplifies system design and integration. The front panel contains connectors for two serial ports and keyboard, audio, and Ethernet ports. The board can hold a maximum of 32 Mbytes of main memory. Prices for the CPU-2S start at $7495.

***Force Computers Inc.**, 3165 Winchester Blvd., Campbell, CA 95008; (408) 370-6300.* **CIRCLE 478**

■ *RICHARD NASS*

LOW-COST COLOR LCD HOLDS 386SX SBC



A PC-powered color LCD operator interface, based on a 386SX processor sells for under $3000. The DisplayPac-cLCD consists of a full-color LCD, a PC-compatible single-board computer, and a capacitive touch screen all in one package. As a lower-cost alternative to active-matrix TFT displays, the DisplayPac-cLCD offers 512 colors and 640-by-480 VGA resolution. The operator interface features up to 16 Mbytes of DRAM, a VGA-flat-panel controller, a battery-backed real-time clock, and SBX expansion interfaces.

Computer Dynamics, 107 S. Main St., Greer, SC 29650; (803) 877-8700. **CIRCLE 479**

VME-TO-NATO BOARD HAS 32-BIT DATA, ADDRESS

Time to market can be reduced using the NATO Hawke VME-to-NATO interface board. The board is a 32-bit VMEbus link that bridges NATO-4146C and MIL-STD-1397 types B, C, and H interfaces for the Naval Tactical Data System. It supplies full-duplex differential I/O and on-board development tools that offload system designers from having to write I/O routines. Users can program the board's EPROM to emulate expensive obsolete peripherals, such as reel-to-reel tape drives, mechanical teletypes, and paper-tape reader punches. For system analysis, verification, and diagnostics, the NATO Hawke can monitor, collect, and time-tag I/O channel data for an entire combat system. The board is built with a VIC-068 chip to guarantee compatibility with the VME specification. Commercial versions of the interface board sell for $4931. A ruggedized version costs $5250.

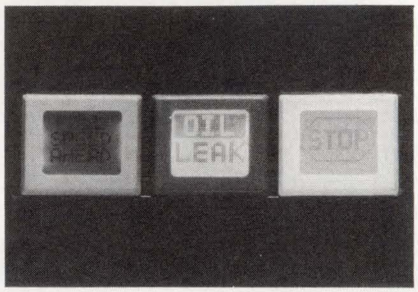
Sabtech Industries Inc., 5411 East La Palma Ave., Anaheim, CA 92807; (714) 693-3500. **CIRCLE 480**

NEW PRODUCTS

COMPONENTS

GRAPHIC LCD SWITCH MODULE SMOOTHS MAN-MACHINE LINK

Designed to put a simple man-machine interface at the operator's fingertips, the D880 graphic, multifunction liquid-crystal-display keyswitch uses a low-power graphic LCD as its keycap. The wide, 864-pixel display field offers users



many options to choose from in characters and icons.

Operator instructions such as sequencing, timing, system status, along with dynamic updating are made available on a keypad. Thanks to a three-color light-emitting diode backlight, the legends may be enhanced with the use of changing color alerts, blinking, or audio signals.

A custom IC driver is behind the supertwist LCD display, both of which rest atop a single-pole, single-throw, momentary-contact switch with dimensions of less than 1 in.^{2}. The display's pixels are in a 24-by-36 matrix. Eighteen characters (three lines of six characters each) can be displayed using a 5-by-7 font.

C. Itoh Technology also offers its DK800 development system for the switches. The development system is made up of a complete set of tools for quick implementation of the D880 switch. Included are a controller for driving up to 48 switches, a 4-by-4 printed-circuit board with three mounted sockets, and a power supply, along with cabling and software. The controller communicates with any computer.

The D800 graphic switch carries a price tag of $37.50 in lots of 250. Switches are delivered from stock. The DK800 development system sells for $899. Delivery takes four weeks.

C. Itoh Technology Inc., Electronic Component Div., *P.O. Box 19657, Irvine, CA 92713-9657; (800) 347-2484, ext. 4529.* **CIRCLE 481**

■ *DAVID MALINIAK*

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DRIVE TESTER HANDLES FAST SCSI STANDARD

The PR4050 portable SCSI disk drive qualifier/tester now handles 10-Mbyte/s synchronous data transfers, making it suitable for testing to the Fast SCSI standard. The unit tests disk or tape drives and optical memories while they are connected to the system bus. It can passively monitor drive performance while the system is operating, actively test drives in place with the system halted, or in some cases actually test the drive while the system operates normally. With hardware and an operating system designed for SCSI testing, the PR4050 runs complex diagnostic tests automatically. Prices start at $8750, and OEM pricing is available. Delivery is from stock.

Pioneer Research, 1745 Berkeley St., Santa Monica, CA 90404; (800) 233-1745 or (310) 829-6751 ext. 202.

CIRCLE 482

INSTRUMENT SIMULATES CABLING CONFIGURATIONS

Although telecommunication users are increasingly switching to ISDN systems, existing cable installations often exhibit deficiencies at ISDN transmission rates that were not a problem at audio frequencies. Local-line interfaces must compensate for these deficiencies. For such applications, the ILS-2 ISDN Line Simulator is a powerful tool. The instrument makes it easy to simulate the effects of cable junctions, bridged taps, and interference on the line. The ILS-2 can simulate practical network conditions based on the test configurations described in ESTI specifications. These configurations are used mostly for the local-line U interfaces of network terminations, regenerators and exchanges. Either of the two common line codes, 2B/1Q and 4B/3T, can be selected. The ILS-2 is available now, with prices given on request.

Wandel & Goltermann, P. O. Box 1262, D-7412 Eningen, Germany; 00 49 7121-861851; fax 00 49 7121-88404.

CIRCLE 483

TOKEN-RING CONTROLLER CHIP TARGETS ISA/EISA ADAPTER CARDS

The DP8025 single-chip Token-Ring controller from National Semiconductor implements the system bus interfaces, an IEEE 802.5-compliant and IBM-certified ring interface, and the MAC and LLC functions per the IEEE 802.5 specification. Licensed to National by IBM, the controller includes transmit and receive buffers, a MAC/LLC microcode PROM, address-ID PROM, and system-interface and line-interface passive components. Developed and qualified by IBM, the 1-W controller implements three selectable bus interfaces (ISA, Micro Channel, or 68XXX), and the analog and digital ring interface. The 5-V CMOS chip supports a zero-wait-state Micro Channel interface for PS/2 computers. Chip-selectable bit rates are 16 and 4 bits/s.

An internal microcontroller executes the MAC and LLC functions, which are implemented in PROM. The controller microcode is provided to developers. The chip interfaces to standard 32-kword-by-9-bit RAMs for shared buffer memory. Configurable RAM size and page size minimizes the system-development effort. Network operating systems supported include Banyan's Vines, IBM's OS/2 LAN Server, Microsoft's LAN Manager, and Novell's NetWare. National will supply driver-development support for major platforms. The DP8025 comes in a 175-pin flip-chip C4 pin-grid array and costs $129 each in quantities of 100. Production quantities will be available in the third quarter.

National Semiconductor Corp., *P. O. Box 58090, Santa Clara, CA 95052-8090; (800 272-9959.* **CIRCLE 484**

■ *MILT LEONARD*

CONTROLLER 'TALKS' TO REMOTE SENSORS

For supporting data acquisition, data logging, or process point control, the Sensor Modem 500 series from Nota Bene Technology communicates with up to 800 remote digital or analog measurement devices and/or control points per station. Signal access is through local RS232/ RS485 wide-area dedicated-lines, radio, or switched-dial networks. The controller can act as a master or slave. The standard I/O package includes 10 optically isolated digital inputs, two relay-driver outputs, and four bipolar analog inputs. Optional features include high-density expansion modules and a Basic compiler for user applications. A selectable 8-bit parallel port connects a printer or I/O expansion bus.

Compatible with standard PC communication programs, the controller enables users to upload and download setpoints, captured data, and programs from any location. Local and remote operator-terminal emulation is provided for set-up, calibration, and maintenance. Internal signal-conditioning circuitry accommodates more than 100 types of sensors, and a variety of signal voltage and current levels. The base unit costs $750 each; expansion modules are $150 to $250 each. Delivery is from stock to four weeks after order.

Nota Bene Technology Inc., *11210 Arrowood Circle, Dayton, MN 55327; (612) 421-9225* **CIRCLE 487**

■ *MILT LEONARD*

FREQUENCY SYNTHESIZER DOES 50 MHZ TO 1.1 GHZ

The UMA1014T single-chip frequency synthesizer from Philips Semiconductors generates RF carrier frequencies in the 50 MHz to 1.1 GHz range, suiting it for use in a wide range of communication equipment such as cordless phones, private mobile radio and radio-based local area networks. Single 5-V supply rail operation and low power consumption also suit the UMA1014T for use in battery-powered equipment.

An on-chip oscillator circuit connects directly to a crystal or the output of a temperature-controlled crystal oscillator to supply a reference frequency in the 1-MHz to 16-MHz range. The device also includes the prescalers and programmable dividers to frequency-divide the reference and RF frequency inputs, eliminating interfacing problems with external prescaling. The 1014T's 16-pin small-outline plastic package minimizes the required pc- board area. Its current consumption of 13 mA in the active mode and 2.5 mA in the power-down mode contribute to extended battery life in portable equipment. The synthesizer operates from –40°C to +85°C. Available now, the UMA1014T costs $3 apiece in high volume.

Philips Semiconductors, P. O. Box 218, NL-5600 MD Eindhoven, The Netherlands; Arnold Blekk, 00 31 40-722091. Philips Semiconductors, 2001 W.Blue Heron Blvd., Riviera Beach, FL 33404-5099; Miriam Coleman: (407) 881-3257. **CIRCLE 485**

CHIP PAIRS RDS DEMODULATOR, FILTER

Made in advanced BICMOS technology, the TDA7330 is a single-chip filter and demodulator circuit for Radio Data Systems (RDS) transmissions. Needing no filter adjustments, the IC, from SGS-Thomson Microelectronics, requires few external components.

The circuit contains a 57-kHz switched capacitor input bandpass filter, a bit rate clock recovery circuit, dual sideband demodulator circuit, biphase phase-shift keying decoder, differential coding circuits and a signal quality output circuit. The device provides outputs suitable for direct processing by the microcontroller that decodes the RDS data for display and other uses.

Two package variants of the part are offered: type TDA7330 is a 20-lead DIP and type TDA7330D is an SO-20L surface mounting package. For applications where the demodulator circuits are already integrated in a dedicated microcontroller, SGS-Thomson offers a stand alone 57-kHz filter circuit, the TDA7332.

The TDA7330 is available now at a price of $2.50 in quantities of 25,000 units. A worldwide standard, RDS is already widely used in Europe and transmissions have begun in the U.S. and in many Far East countries.

SGS-Thomson Microelectronics, 1000 East Bell Road, Phoenix, Arizona 85022. Contact: J.P. Rossomme. Phone: (602)867-6228. **CIRCLE 486**

INTEGRATE PHONE LINES FOR FAX APPLICATIONS

For high-volume fax-switch applications, the MLCP-4 platform can integrate up to four telephone lines. The board can be linked to any analog-expansion-bus-compatible device, allowing users to develop systems that incorporate voice, T1, and voice-recognition technologies. The AEB connection lets the board interface with the public telephone network through a T1 board or an AEB-compatible voice board. Large-scale fax-switch makers can streamline connections with the MLCP-4's T1 capacity to consolidate 24 phone lines into one digital line that can handle 2000 fax pages per hour. Available now, the board costs $3995.

GammaLink, 133 Caspian Ct., Sunnyvale, CA 94089; (408) 744-1430. **CIRCLE 488**

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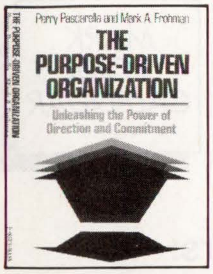

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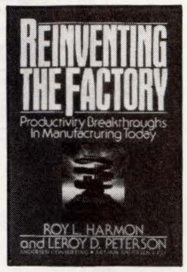

Reinventing the Factory – Productivity Breakthroughs in Manufacturing Today
Roy L. Harmon and Leroy D. Peterson
Andersen Consulting
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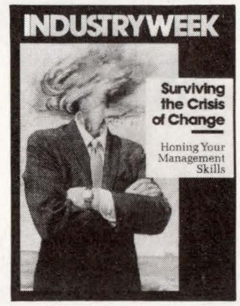

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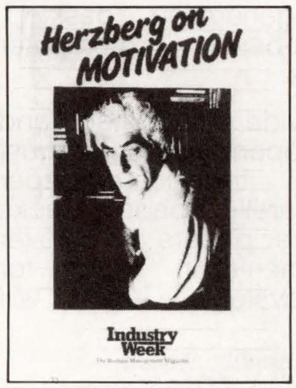

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SVPC™

AUGUST 10 - 12, 1992

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The Silicon Valley Personal Computer Design Conference focuses on providing solutions to key PC, Workstation, and Peripheral design and integration issues. SVPC is aimed at designers and strategic planners who are trying to differentiate their systems, or design or evaluate the next-generation desktop, portable and pen-based computer technologies and systems.

The conference will provide many half- and full-day tutorials on the opening day (August 10), and over 100 technical paper presentations in four parallel paper tracks (August 11 and 12). The papers will cover key design and implementation issues for desktop and portable systems. Topics will include:

Motherboard Design Issues...Portable System Design...Memory-Card Interfacing... Mass-Storage Subsystem Design...Pen-based System Design...Multimedia Hardware Design...Data Communications (Data/Fax Modems, Serial cards, Etc.)...BIOS Implementation and Graphical User Interface Issues...Power Management Schemes...Video and Graphics Subsystems...Local-bus Interface Approaches...Peripheral Subsystem Design...System Buses (ISA, EISA, MCA, SBus, NuBus, Etc.)...Network Interfaces (RF, Token Ring, Ethernet, Etc.).............and many other topics.

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Mr. Roger Ross,
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Mr. Kiichi Hataya,
President, Toshiba America, Information Systems Div.

DON'T MISS THE PRODUCT EXHIBITS

Close to 100 table-top exhibits will show off the latest CPU chips, memories, and ASIC technologies, as well as board-level and software products.

Exhibit hours run noon to 2 pm on Tuesday and Wednesday, August 11 and 12, as well as 5:30 to 7:30 pm on Tuesday evening.

Refreshments will be served in the Exhibits area.

Several exhibitors will hold drawings for product samples -- be sure to leave a business card at their tables.

Interested in Exhibiting or Becoming a Corporate Sponsor? Contact Ken Majithia, (408) 924-3930 (ph) (408) 997-8265 (fx)

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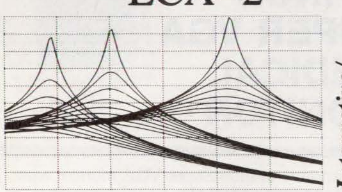

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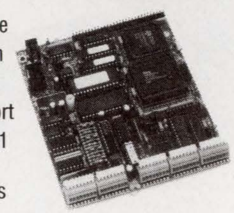

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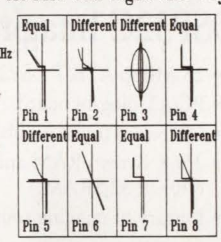

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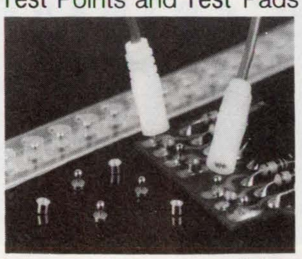

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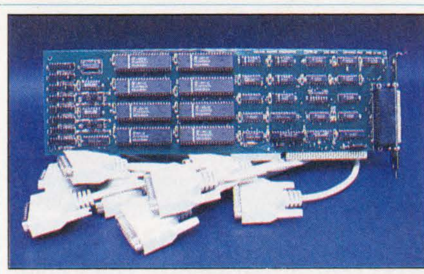

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