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CLAS 4000 LOGIC ANALYSIS SYSTEM

29000 MICROPROCESSOR ANALYSIS PACKAGE

USER'S MANUAL

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PREFACE

This manual describes equipment connections and operation of Disassembler Utility software for the Gould Microprocessor Analysis Package (MAP). The MAP is an accessory tool for the Configurable Logic Analysis System 4000(CLAS 4000).

Procedures are included in this manual for connecting MAP hardware components to the CLAS 4000, loading the utility software, and invoking the disassembly operation. These procedures also describe the use of menu-driven display screens to disassemble information recorded by the CLAS 4000.

The MAP user should be familiar with basic operating features of the CLAS 4000 driven by the *Macintosh™ computer which uses windows, icons, and pull-down menus to control system operations. Refer to the CLAS 4000 User's Manual, Publication Number 0192-0225-10, for system operating procedures.

If you require assistance on this product, please call Gould Inc., Design and Test Systems Division Customer Service on the toll-free, hot-line number: **(800) 538-9320**; then dial **2** to contact the DTD Marketing Department.

The content in this manual reflects the MAP software level which was valid at the time of publication, but is subject to change without notice.

Copies of this manual and other Gould Inc., Design and Test Systems Division publications may be obtained from the Gould Inc., DTD sales office or distributor serving your locality.

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CONTENTS

CONTENTS (Cont'd)

6. SPECIAL OPERATING FEATURES

ILLUSTRATIONS

TABLES

Chapter 1

INTRODUCTION

OVERVIEW

This manual describes the Gould Microprocessor Analysis Package (MAP). The MAP is a tool that expands the test-debug capability of the Configurable Logic Analysis System 4000 (CLAS 4000). The MAP disassembles captured information to convert executed object code into mnemonic code and display the result on the video screen.

The MAP contains interface hardware and software components to be installed on the CLAS 4000 by the user. Typical MAP hardware is shown in Figure 1-1.

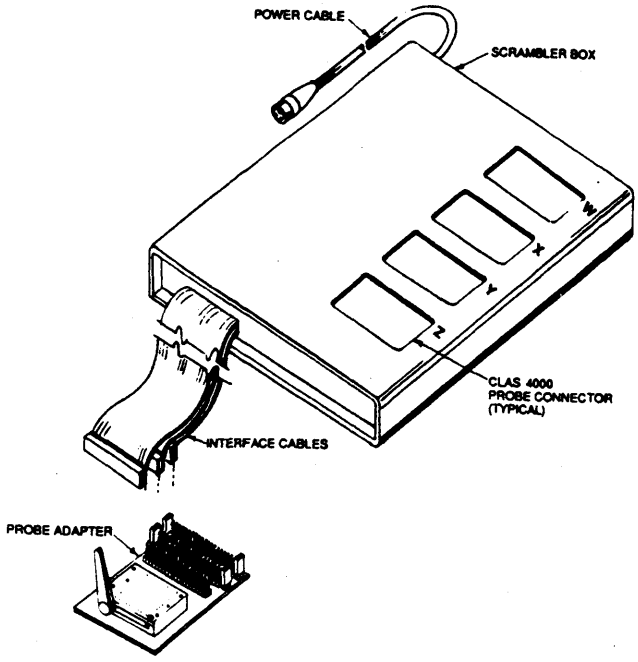


Figure 1-1. Typical MAP Components

Included in this manual is a microprocessor-to-logic analyzer pinout diagram, microprocessor-to-logic analyzer connection data, screen displays of preprogrammed menus, and screen displays of captured data presented in various disassembled formats.

HOW TO USE THIS MANUAL

The content in this manual is organized to present Standard MAP Features in Chapters 1 through 3 and Unique MAP Features in Chapters 4 through 6.

Standard MAP Features

The Standard MAP Features (Chapters 1 through 3) describe common characteristics of the MAP package which are the same for all microprocessor types. The information presented in these chapters is intended to guide the user through the standard operating capabilities of the MAP. If specific information is needed for a particular microprocessor type, refer to information contained in Chapters 4 through 6.

The Standard Features include the following types of information:

- Overview of MAP Hardware and Software Components (Chapter 1)

- Loading and Invoking the Disassembler (Chapter 2)

- Analyzer Setup (Chapter 2)

- Disassembler Operation (Chapter 3)

- Selecting Format Options (Chapter 3)

- Realignment of Data Screen (Chapter 3)

- Configuration Options (Chapter 3)

- Unloading the Disassembler (Chapter 3)

Unique MAP Features

The Unique MAP Features (Chapters 4 through 6) describe microprocessor dependent characteristics of the MAP Package which are different for each microprocessor type. Refer to these chapters for detailed information about connections for MAP components , microprocessor pin assignments, and unique disassembler operations for the microprocessor type.

The Unique Features include the following types of information:

- MAP Components (Chapter 4)

- MAP Specification (Chapter 4)

- Target System Connections (Chapter 5)

- CLAS 4000 Equipment Connections (Chapter 5)

- Variations in Disassembler Operation (Chapter 6)

MAP HARDWARE COMPONENTS

Hardware Interface Requirements

The MAP hardware components consist of the Microprocessor Probe Adapter (which is used to interface target system pins) and MAP Scrambler Box with attached cables (which is used to interface CLAS 4000 probe connections to the microprocessor probe adapter). These components are used to connect pins on the target system microprocessor to assigned analyzer channel inputs on the CLAS 4000. The MAP hardware interface allows the CLAS 4000 to capture data related to bus activity directly from the target microprocessor pin location.

SCSI Port Expansion and MAP Power Module

The MAP Scrambler Box may require input power supplied from the CLAS 4000 chassis. This power interface is provided by the SCSI Port Expansion and MAP Power Module (Product No. A70042).

The SCSI module contains four conditioned +/- 5Volts power output connectors for interfacing the MAP hardware and other accessories. The module also allows multiple SCSI devices to be connected in a daisy-chain network to the CLAS 4000 chassis. The SCSI module is optional equipment and is not included as a component in the MAP package. Contact your local Gould Sales office for additional information on this component. When required for MAP operation, this equipment is described in the Installation Connections section of Chapter 5.

MAP DISASSEMBLER SOFTWARE

The MAP software is a Disassembler Utility supplied on a single, 3.5-inch diskette which contains seven types of files as follows:

- Disassembler Executable File (filename ends in .BIN)
- Disassembler Setup File (filename ends in Setup)
- CLAS 4000 Resource File (filename ends in Disassembler)
- Sample Data File (filename ends in Sample Data)
- Sample Timing File (filename ends in Sample Timing)
- Sample Symbol File (filename ends in Sample Symbols)
- Sample Label File (filename ends in Sample Labels)

Disassembler Executable File

The Disassembler Executable File contains the compiled and linked software for disassembly of a specific microprocessor type on the CLAS 4000. The file format is structured so that it can be downloaded to, and executed on the CLAS 4000. This file must reside in the **Disassemblers** folder which is contained within the **CLAS4000Folder** folder.

Disassembler Setup File

The Disassembler Setup File contains information that is unique to each Disassembler. The setup information identifies the base format and clocking setup conditions for the Disassembler. The format can be *modified* by the user without affecting disassembly processing, but any *deletion* from the base setup parameters will render the disassembler unusable.

CLAS 4000 Resource File

The Resource File contains all of the Disassembler Specific Macintosh code and resources to initialize the Disassembler Parameters, an About Box, and an optional Disassembler Parameter Box.

Sample Files

The Sample Files contain examples of recordings that are unique to each Disassembler. These files are provided to demonstrate the capabilities and operating features of the Disassembler.

-The Sample Data File contains a recording of state data. The associated setup parameters are included to allow the user to manipulate the recorded information.

-The Sample Timing File contains ALL of the available channels from the probe with pin numbers and timing labels (e.g. "A7 DACK") in place of "Status 7". This is an asynchronous recording intended for timing evaluation only and is not used for disassembly.

-The Sample Label File presents a table which contains at least four labels (e.g. Reset, Begin, Init, and Idle) for the code address group.

- The Sample Symbol File provides status information decoded for microprocessor cycle periods which can be used for pattern definition.

Using the Disassembler

The disassembler evaluates object code recorded from the target system and displays this information in a pseudo-assembly language form. The displayed information conforms to the chip manufacturer's mnemonic code for the microprocessor instruction set.

The displayed information indicates the captured state of external bus activity that occurred at the microprocessor pins. The user can manipulate the disassembled information to accomplish selective review for the various disassembly modes.

The Disassembler evaluates recorded data to identify the processor cycles. It then attempts to identify the program flow to decode the instructions. The Disassembler assumes the first recorded instruction to be valid and all other instructions to be recorded continuously.

If the first recorded information is not the start of an instruction, or if all available information is not recorded due to selective Trace Control, the disassembly may not be entirely accurate. In this case, it is necessary to re-synchronize the Disassembler to obtain the proper display. The procedure for realignment of the display is described in Chapter 3.

Certain microprocessor types contain internal cache and program memory. These features must be disabled to obtain a meaningful display of external microprocessor activity at the assigned pin/channel location. Other types of microprocessors use the external cache which eliminates the need for user intervention to enable and disable these circuit features. When applicable for MAP operation, this information is provided in Chapter 6.

BASIC MAP OPERATING FEATURES

All MAP packages provide the following basic operating capabilities:

- Capture of Address, Data, and Control signals associated with microprocessor program execution, and display cycle-by-cycle or summary by instruction sequences.

- Trigger on combinations of Bus Cycle Types; Input, Output, Memory Read/Write, Instruction Fetch, and Interrupts.

- Display captured information in various listings using manufacturer's software architecture (e.g. generate a listing with non-executed instructions deleted, or generate a listing with read/write status deleted, etc.).

Chapter 2

LOADING AND INVOKING THE DISASSEMBLER

COPYING FILES TO HARD DISK

General

The CLAS 4000 application is driven by software contained in the folder named **CLAS4000Folder**. This folder is installed on the Macintosh hard disk to implement CLAS 4000 operations.

The utility diskette supplied with the MAP components contains the **CLAS4000Folder** with the Executable File, Setup File, Resource File and Sample Files described in Chapter 1. These files are used to control disassembly processing for the CLAS 4000. These files must be copied to the hard disk as described in the Installation procedure which follows.

The contents of the diskette must be placed in the correct directories on the Macintosh before the user can boot the application.

Installation

If this is the first CLAS 4000 utility to be installed (i.e., there is no CLAS4000Folder on the hard disk), copy the entire folder to the root directory of the hard disk. The main CLAS 4000 Application should already be present in this directory.

If the CLAS4000Folder already exists, the **Resource**, **Setup**, and **Sample** files must be placed in the **CLAS4000Folder** directory.

The **Executable** file must be placed into the **subdirectory** of the CLAS4000Folder titled **Disassemblers**. This is necessary because the Disassembler interface routines require a hard coded directory structure. The **CLAS4000Folder** must be in the root directory to work properly.

If you are a first time user of the CLAS 4000 interfaced to the Macintosh computer, refer to the Macintosh User's manual. This manual describes procedures for copying files to the hard disk and using folders to organize stored information.

LOADING THE DISASSEMBLER

There are several ways to load the Disassembler utility. The first method is to double click the mouse on the **Setup File** in the CLAS4000Folder while in the Macintosh Desktop Window. This action loads the CLAS 4000 Disassembler Setup parameters.

The second method is to **Load** the Disassembler with a setup from the CLAS 4000**File** Menu. This should be used if the current setup is not appropriate for the disassembler. (The channel setup for Address, Data, and Status fields, must be defined in the setup file in the same manner that was shipped with the disassembler; otherwise, the data display information will be garbled.) To accomplish this, simply load the next setup along with that of the disassembler. Running the Analyzer will then produce data in the appropriate format for display.

The third method for loading the Disassembler is used when the setup is already compatible with the Disassembler. The loading occurs by selecting the **Load Utility** menu item under the CLAS4000 empty utility menu icon (see Figure 2-1). This action downloads the executable code and inserts the disassembler in the setup.

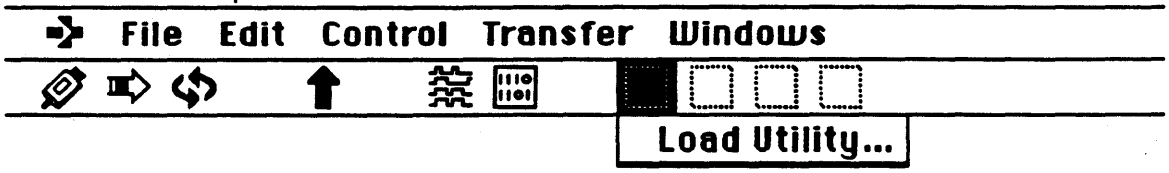


Figure 2-1. Load Utility Menu Icon

The fourth method is used to load the Disassembler from the CLAS 4000 Application which is accomplished as follows:

1. Select **Load** from the **File** menu, then select **Next Setup**.

2. Select **Load** from the **File** menu, then select **Last Setup** with Data (timing labels and transfer).

3. Select **Load Utility** to obtain the Disassembler Files dialog box.

The **Disassembler Files** dialog box (Figure 2-2) appears after selecting the **Load Utility** menu item. This box identifies all of the disassemblers contained in the currently selected folder.

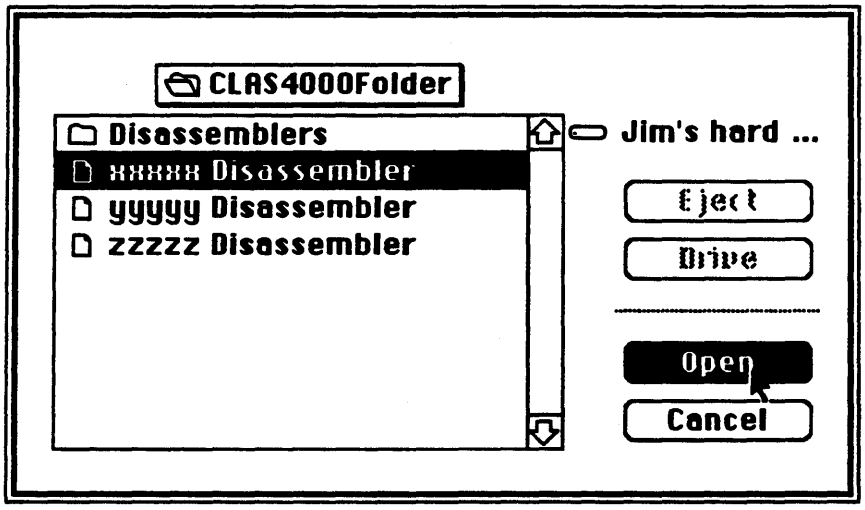


Figure 2-2. Disassembler Files Dialog Box

INVOKING DISASSEMBLY PROCESSING

The Disassembler is loaded and invoked by selecting the Disassembler filename from the Files dialog box and clicking the mouse on **Open,** or double clicking the mouse on the Disassembler filename. The utility is automatically loaded into memory and initialized.

ANALYZER SETUP FOR DISASSEMBLY

Setup Requirements

The CLAS 4000 is setup for disassembly by loading a Disassembler compatible setup into the application. The screens for Channel setup, along with the screens for Clock setup and Trace Control, are initialized with the unique information for the particular Disassembler that was loaded.

These screens can be altered by using the CLAS 4000 standard setup method for each screen. However, accurate disassembly can be assured only when the above screens contain the setup information that was downloaded by the Disassembler. Additional columns of information can be appended to the right side of the Setup screen , but none can be deleted.

Loading Symbols

Symbols are loaded into the Channel Setup Edit Symbol dialog box. The symbols may be either typed or loaded from a file. If they are loaded from a file, the file must be of standard text using the following formats:

Symbol String<tab 0X>Hex Value <CR>
Symbol String<tab 0X>Hex Value<tab> <CR>
Symbol String<tab 0X>Hex Value <tab> Care Value <CR>

Where:

Symbol String, Hex Value, and Don't Care Value are ASCII representations of standard Hexadecimal numbers which are no greater than the fields where they will be inserted (i.e.,10, 8, 8 respectively).

The Care Value is optional and if used, must be set to 1 for each 'Care' Bit .

Each line is followed by a Carriage Return <CR> indicating the end of the record.

One symbol is used per line for as many lines as are required to express the complete symbol table.

An example Symbol Table File prepared by the user with standard text in the required format is shown in Figure 2-3.

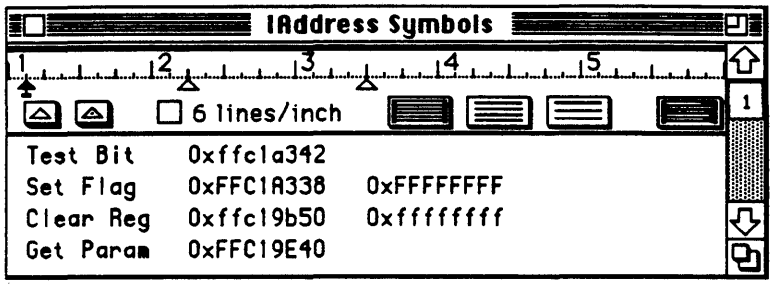


Figure 2-3. Example Symbol Table File

Symbols may be used for either the Address Field or Status Field. Sample files for each symbol type are included on the diskette that is supplied with the system.

Address Symbols (Figure 2-4) are used to add labels to Disassembler displays as described in Chapter 3.

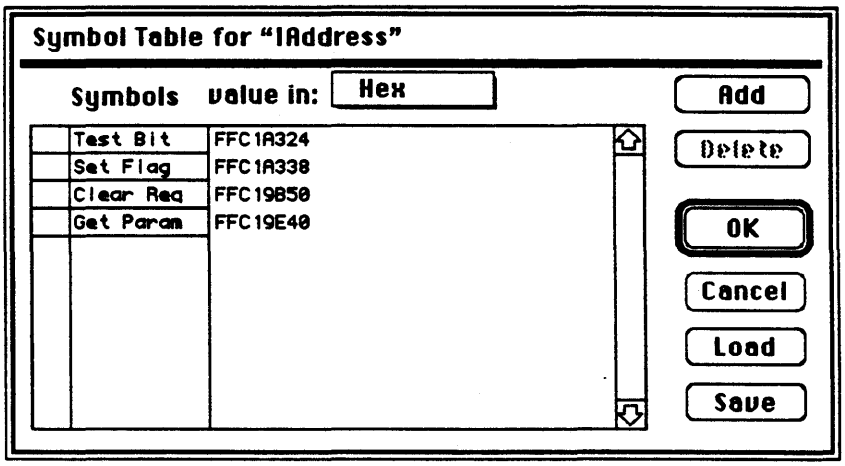


Figure 2-4. Symbol Table for Address

Status Symbols may be used to define Trace Control Patterns relative to microprocessor bus cycle types. To use this feature, the Symbol Table is either entered or loaded in the Channel Setup Symbol Edit Mode for the desired recording (i.e., Next, Last, or Reference). The selection of Next is normally used.

The desired symbol can then be selected in the Trace Control Pattern Definition window by double clicking the mouse on the Status Pattern or using the Edit button to obtain the Symbol Selection Table shown in Figure 2-5.

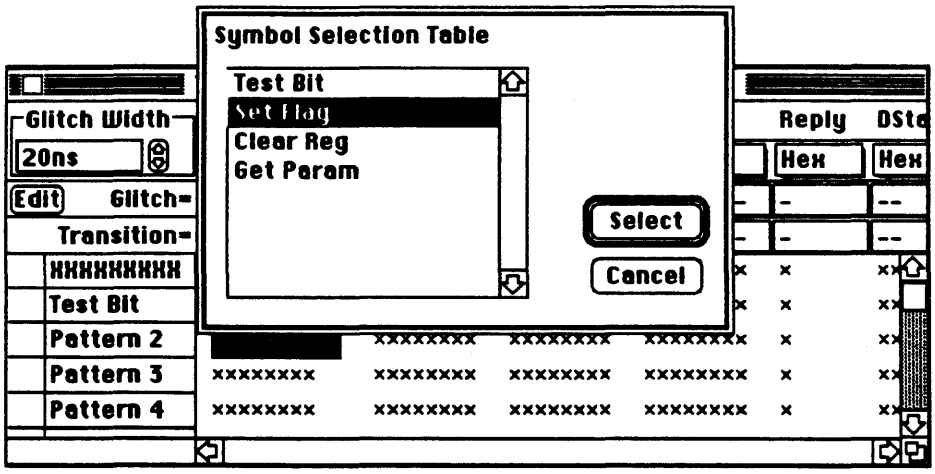


Figure 2-5. Symbol Selection Table

Chapter 3

DISASSEMBLER OPERATION

DISASSEMBLING THE DATA

After loading is completed, the empty utility icon is replaced with the Disassembler menu icon (Figure 3-1) and its associated menu selections.

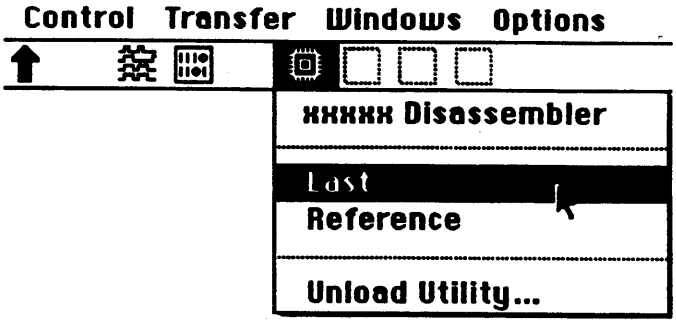
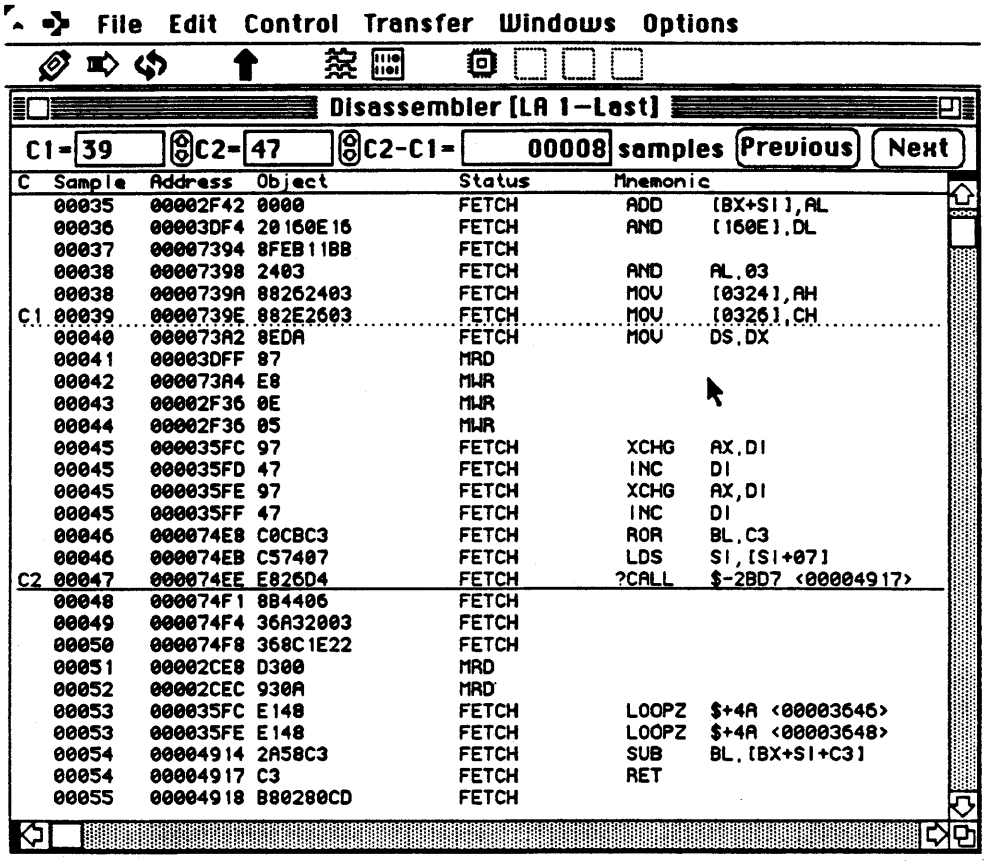


Figure 3-1. Disassembler Menu Icon for Last Data Recorded

The Disassembler Display Window (Figure 3-2) presents typical disassembled information. The display window is entered by selecting either the **LAST** or the **REFERENCE** item from the Disassembler menu. This selection determines what data is to be disassembled. Selecting the Title Choice from the Disassembler Menu displays the revision level of the Disassembler software.



C	Sample	Address	Object	Status	Mnemonic	
	00035	00002F42	0000	FETCH	ADD	[BX+SI],AL
	00036	00003DF4	20160E16	FETCH	AND	[160E],DL
	00037	00007394	8FEB11BB	FETCH		
	00038	00007398	2403	FETCH	AND	AL,03
	00038	0000739A	88262403	FETCH	MOV	[0324],AH
C1	00039	0000739E	882E2603	FETCH	MOV	[0326],CH
	00040	000073A2	8EDA	FETCH	MOV	DS,DX
	00041	00003DFF	87	MRD		
	00042	000073A4	E8	MWR		
	00043	00002F36	0E	MWR		
	00044	00002F36	05	MWR		
	00045	000035FC	97	FETCH	XCHG	AX,DI
	00045	000035FD	47	FETCH	INC	DI
	00045	000035FE	97	FETCH	XCHG	AX,DI
	00045	000035FF	47	FETCH	INC	DI
	00046	000074E8	C0CBC3	FETCH	ROR	BL,C3
	00046	000074EB	C57407	FETCH	LDS	SI,[SI+07]
C2	00047	000074EE	E826D4	FETCH	?CALL	$-2BD7 <00004917>
	00048	000074F1	8B4406	FETCH		
	00049	000074F4	36A32003	FETCH		
	00050	000074F8	368C1E22	FETCH		
	00051	00002CE8	D300	MRD		
	00052	00002CEC	930A	MRD		
	00053	000035FC	E148	FETCH	LOOPZ	$+4A <00003646>
	00053	000035FE	E148	FETCH	LOOPZ	$+4A <00003648>
	00054	00004914	2A58C3	FETCH	SUB	BL,[BX+SI+C3]
	00054	00004917	C3	FETCH	RET	
	00055	00004918	B80280CD	FETCH		

Figure 3-2. Typical Disassembler Display Window

Disassembly Processing

When the Disassembler Display Window is entered for the first time, the contents area of the window is empty and a pause occurs for completion of disassembly processing before the window is filled with disassembled data. During this time, a Status Box will indicate progress of the disassembly.

If the user wishes to abort the disassembly, hold down the **Apple** key and type a **period**. The disassembler will present disrupted data on the screen.

A spinning cursor is displayed to the user while the disassembler is busy decoding the data for display. The spinning cursor is also displayed if a new recording is taken while viewing the current disassembly display. The old contents of the screen will remain visible until the screen is updated with the new decoded data. To avoid having disassembly processing occur when it is not needed, the user can simply close the disassembler window.

If it is suspected that noise causes errors to occur in a data recording, increase or decrease the threshold voltages beyond the noise levels to remove the disturbance.

The disassembler also disassembles data on the screen when a message is received that the format patterns have been changed. This condition would occur after the user loads another symbol table into the Channel Setup Symbol definition screen, or when a pattern is edited from the list. It precedes the disassembly by downloading the symbol table.

The disassembler columns may be moved by clicking the mouse on the column heading and shifting in the desired direction. However, the disassembler columns can not be reordered; otherwise, this window operates in the same manner as the state display. The display pane splitters operate in the same manner, as well as the cursors, the markers, and most of the menu commands.

Using Disassembler Options Menu

When the Disassembler Display Window is entered, the **Options** menu item (Figure 3-3) is added to the menu bar. The **Options** menu contains choices for selections that are used to manipulate the Disassembler Display Window as described in subsequent paragraphs.

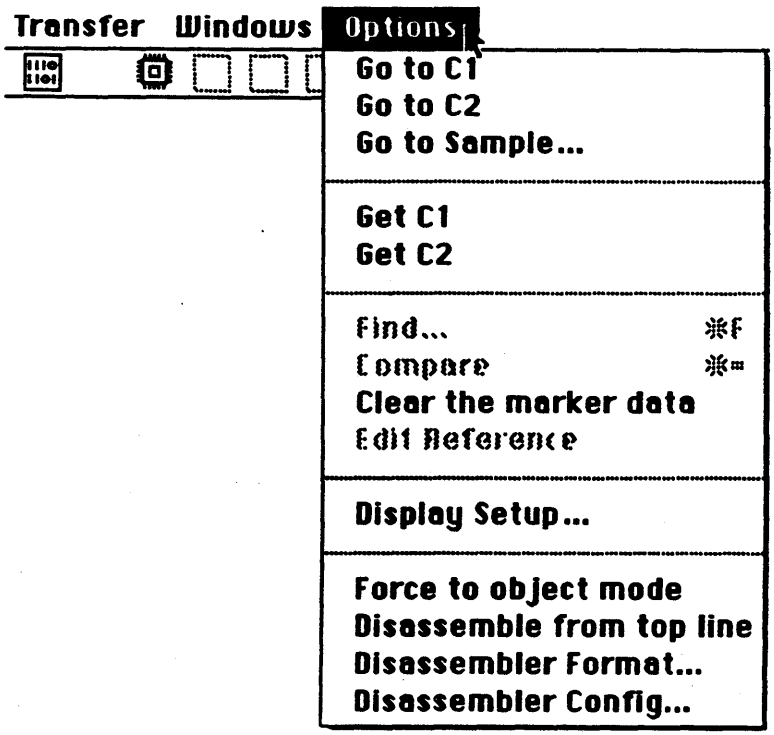


Figure 3-3. Disassembler Options Menu

Some of the Options Menu commands that are available in the State Window display are not available in the Disassembler Window display and vice-versa as described below.

The following commands are available in the Disassembler Window but not in the State Window:

Force to Object Mode
Disassemble from Top Line
Disassembler Format
Disassembler Configuration (when required by the specific disassembler)

The following commands are available in the State Window but not in the Disassembler Window:

Find*
Compare*
Edit Reference

***NOTE:** Despite the fact that Find and Compare commands are not available in the Disassembler Window, the results are displayed in the Disassembler Window whenever they are used in the State Window.

The user can change the displayed area of the Disassembler Window by using the **Go to...** cursor menu items. The display window can also be manipulated either by using the scroll bars or by dragging the cursor. If the display window has been manipulated by the scroll bar, and the user wishes to return to the area in the recording where either cursor is located, choose the **Go to C1** or **Go to C2** menu item to accomplish this action.

Go to Sample Number Dialog Box

The **Go to Sample...** menu selection allows the user to view the display contents beginning with the sample number selected. After selecting the **Go to Sample...** item, a dialog box (Figure 3-4) appears so that the user may select the specific sample number.

NOTE: The function for this selection is independent from the cursor movement. It merely changes the display to show the information beginning from the selected sample number. The cursors remain in their original positions.

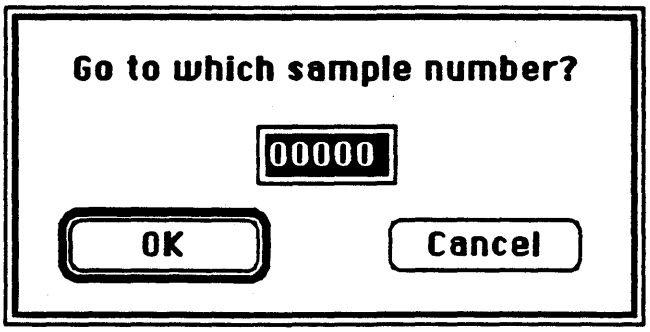


Figure 3-4. Go to Sample Number Dialog Box

The **Get C1** or **Get C2** menu items position the cursor to the top of the currently displayed area.

NOTE: Entering the sample number for the squares labeled **C1=** or **C2=** is another method for repositioning the cursor locations in memory. The **Clear the marker data** command simply clears any search, compare, or marker information that was previously defined by the user.

The **Disassembler Format. . .** command allows the user to define his preferences on such things as font size, the choice to display step (level) data, and time stamp information. This command works exactly the same for both the State and Disassembler Windows.

The **Force to object mode** command re-displays the current data in object format, with the smallest instruction per line. This is useful when the data has a break in sequence, or when the recording did not start on an instruction boundary.

The **Disassemble from top line** command re-disassembles data from the top display line. This is used in conjunction with the **Force to object mode** command to re-synchronize the Disassembler's internal instruction counter with the data flow.

The last two commands are designed to be used together. When synchronization is lost, the user should **Force data to object mode**, move down to a probable opcode location, and then return to normal disassembly mode using the **Disassemble from top line** command. The Disassembler is setup to allow the user to do this as many times as needed.

SELECTING THE DISASSEMBLER FORMAT

The **Disassembler Format** menu presents the Disassembler Specific Format Dialog Box (Figure 3-5). This dialog box allows the user to choose the desired Disassembly and Display modes. The mode shown in Figure 3-5 is used to display disassembly results.

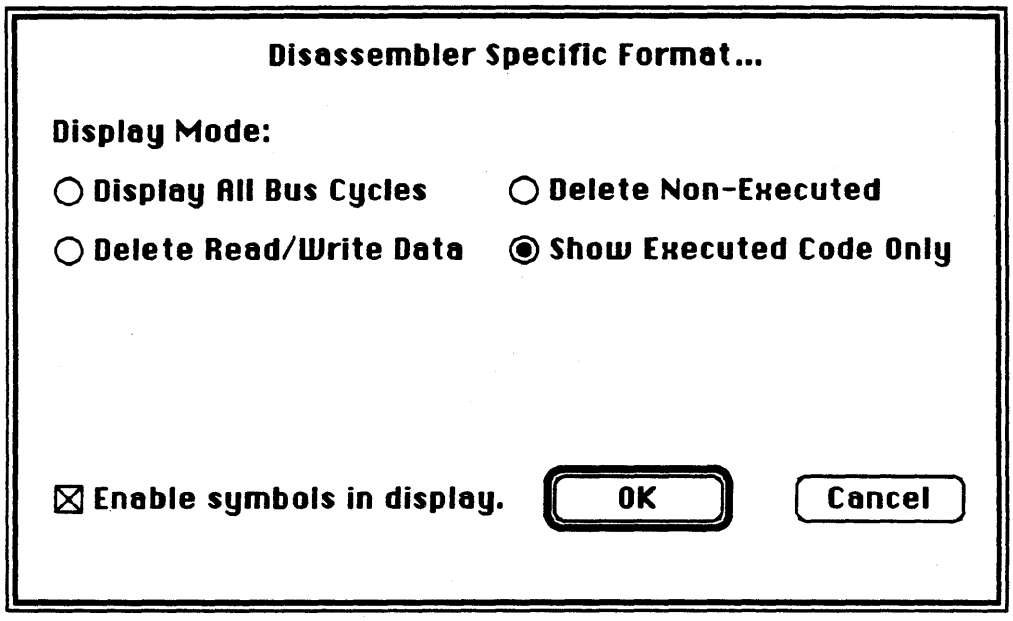


Figure 3-5. Disassembler Specific Format Dialog Box

Click the mouse on the assigned button to select a choice for Disassembler Display Mode. The display modes are filters that specify what portion of the disassembled data is displayed. Typical display modes are as follows:

Display All Bus Cycles
Delete Non-Executed Instructions
Delete Read/Write Data
Show Executed Code Only (removes both non-executed instructions and read/write data)

ENABLE SYMBOLS

Upon selecting the option for **Enable symbols in display**, a column is inserted in the disassembler Display Window between the Status and Mnemonic column that is titled Labels.

The first column (Address) must be in Symbol Display Mode and a Symbol Table must be loaded.

The symbol is inserted at locations where an address matches a symbol from the Symbol Table or when a decoded instruction references a specific Address (see Figure 3-6).

NOTE: A Sample Address Symbol Table is included on the diskette supplied with the system.

Disassembler [LA 1-Last]

C1=0 C2=25 C2-C1= 00025 samples Previous Next

C	Sample	IAddress	DAddress	Code	Data	DRx	CRx	Label	Mnemonic	
C1	00000	FFC0978C		14420000		Idle	Scode		ld	r2,r2,$0000
	00001	FFC09790		F400C001		Wait	Scode		jmp	r1
	00003	FFC09794		24620000		Idle	Scode		st	r3,r2,$0000
	00004	FFC1A324		492200FF		Idle	Scode	Test Bit	mask	r9,r2,$00FF
	00005	FFC1A328		7D4900DC		Idle	Scode		cmp	r10,r9,$00DC
	00006	FFC1A32C		D86A0003		Idle	Scode		bb1	(3),r10,Set Flag
	00008	FFC1A338		58400000		Idle	Scode	Set Flag	or	r2,r0,$0000
	00009	FFC1A33C		143F0024		Idle	Scode		ld	r1,r31,$0024
	00010	FFC1A340		63FF0028		Wait	Scode		addu	r31,r31,$0028
	00012	FFC1A344		F400C001		Idle	Scode		jmp	r1
	00015	FFC19B50		D86A0003		Idle	Scode	Clear Re	bb1	(3),r10,$FFC19B5C
	00016	FFC19B54		58400000		Idle	Scode		or	r2,r0,$0000
	00017	FFC19B58		C00000BA		Idle	Scode		br	Get Para
	00019	FFC19E40		143F002C		Idle	Scode	Get Para	ld	r1,r31,$002C
	00020	FFC19E44		171F0020		Wait	Scode		ld	r24,r31,$0020
	00022	FFC19E48		173F0024		Wait	Scode		ld	r25,r31,$0024
C2	00026	FFC19E4C		63FF0030		Idle	Scode		addu	r31,r31,$0030
	00027	FFC19E50		F400C001		Idle	Scode		jmp	r1
	00029	FFC0403C		5C40FFF8		Idle	Scode		or.u	r2,r0,$FFF8
	00030	FFC04040		58422000		Idle	Scode		or	r2,r2,$2000
	00031	FFC04044		CBFFFF78		Idle	Scode		bsr	$FFC03E24
	00033	FFC03E24		14420004		Idle	Scode		ld	r2,r2,$0004
	00034	FFC03E28		F400C001		Wait	Scode		jmp	r1
	00036	FFC03E2C		F4E06001		Idle	Scode		addu	r7,r0,r1
	00037	FFC04048		D002FFE8		Idle	Scode		bb0	(0),r2,$FFC03FE8
	00039	FFC03FE8		5C40FFF8		Idle	Scode		or.u	r2,r0,$FFF8
	00040	FFC03FEC		58422020		Idle	Scode		or	r2,r2,$2020
	00041	FFC03FF0		CBFFFF8D		Idle	Scode		bsr	$FFC03E24

Figure 3-6. Symbol Column Insertion in Data Display Window

SELECTING DISASSEMBLER CONFIGURATION

The **Disassembler Config...** menu selection is available when the current disassembler has parameters that will not fit into the choices available above. These conditions are defined inside the disassembler resource file, and will vary from one disassembler to another.

Typically, this menu is used to specify operating modes of the target microprocessor or to provide the value of internal registers which cannot be determined from recorded data. This information is described in Chapter 6 when required for a specific Disassembler.

UNLOADING THE DISASSEMBLER

The Disassembler is unloaded by clicking the mouse on the **Unload Utility** menu item on the icon menu bar (See Figure 3-1). This action will cause the Disassembler to unload. The Setup information is purged from the CLAS 4000 and the Utility icon becomes grayed to indicate the utility is inactive. If a setup containing a disassembler is loaded on top of another disassembler, the old one is automatically unloaded.

Chapter 4

29000 MAP SPECIFICATIONS

PHYSICAL DIMENSIONS AND WEIGHT

Height:	2.5 inches (6.4 cm)
Width:	8.5 inches (21.6 cm)
Depth:	9.25 inches (23.5 cm)
Cables:	13.5 inches (34 cm) long
Weight:	3.4 lbs., (1.5 kg) with Probe Adapter and attached cables

ELECTRICAL CHARACTERISTICS

Loading (Signal Inputs)

Input Impedance:	Probe load for all signals except DREQN and IREQN is 1 megohm shunted by 8pf. Maximum current for signals is +/- 5uA
	Probe load for DREQN and IREQN is one TTL for each signal

Loading (Ground/Reference Input)

Input Resistance:	Less than 1 ohm referenced to target system ground and approximately 18K ohms referenced to logic analyzer ground
Ground Difference Immunity:	+/- 0.25 Volt maximum between logic analyzer ground and target system ground

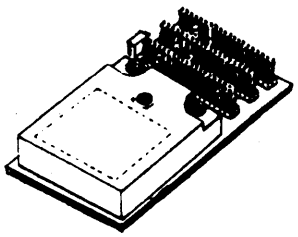
POWER

Supplied from CLAS 4000:	May require SCSI Port Expansion and MAP Power Option to provide 5 Volts DC

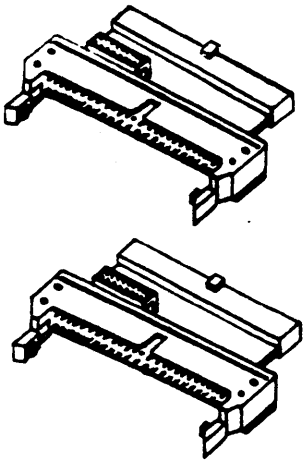
MAP COMPONENTS

The 29000 Microprocessor Analysis Package (Product No. A70043) consists of the following components which are shown in Figure 4-1:

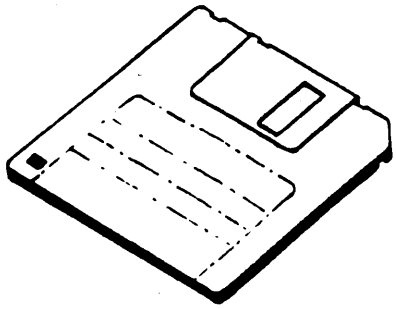
- 29000 Scrambler Box (with attached signal cables and power cord)
- Probe Adapter Assembly
- Two Clock Probe Interface Adapters
- One 29000 Disassembler Diskette
- Users Manual



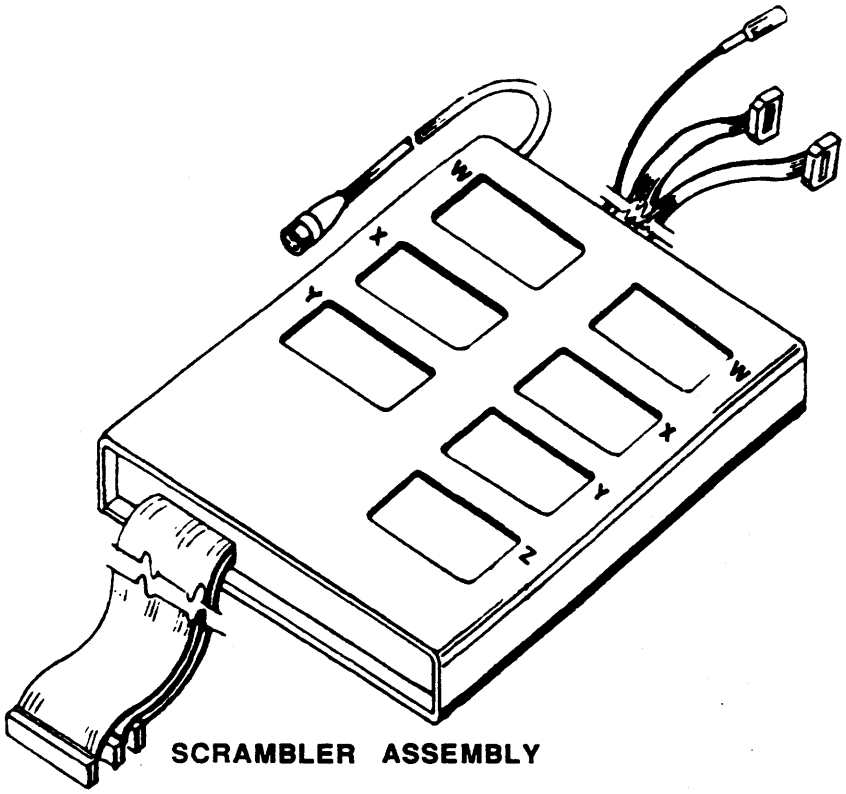
MICROPROCESSOR PROBE ADAPTER
P/N 0192-0380-10



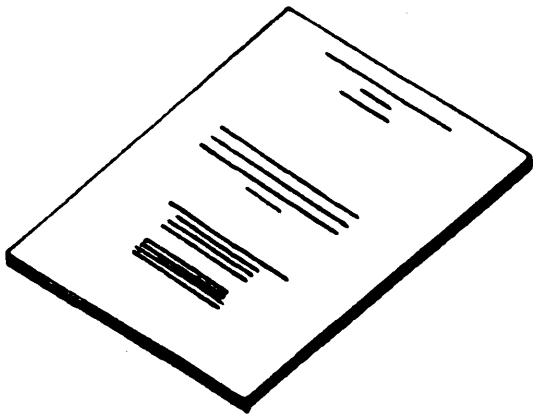
CLOCK PROBE INTERFACE ADAPTER
P/N 0192-1055-10



SOFTWARE DISKETTE
P/N 0192-0480-10



SCRAMBLER ASSEMBLY



USER'S MANUAL
P/N 0192-0286-10

Figure 4-1. 29000 MAP Components

29000 MICROPROCESSOR PIN ASSIGNMENTS

Pin locations for the 29000 microprocessor are shown in Figure 4-2. Signal names for pins may be obtained from the reference manual mentioned below or from Table 5-1.

Additional information, including cross references for microprocessor machine code and instructions may be obtained by consulting the following reference manuals issued by Advanced Micro Devices:

AM29000 32-Bit Streamlined Instruction Processor User's Manual

AM29000 Streamlined Instruction Processor, Publication No. 09075

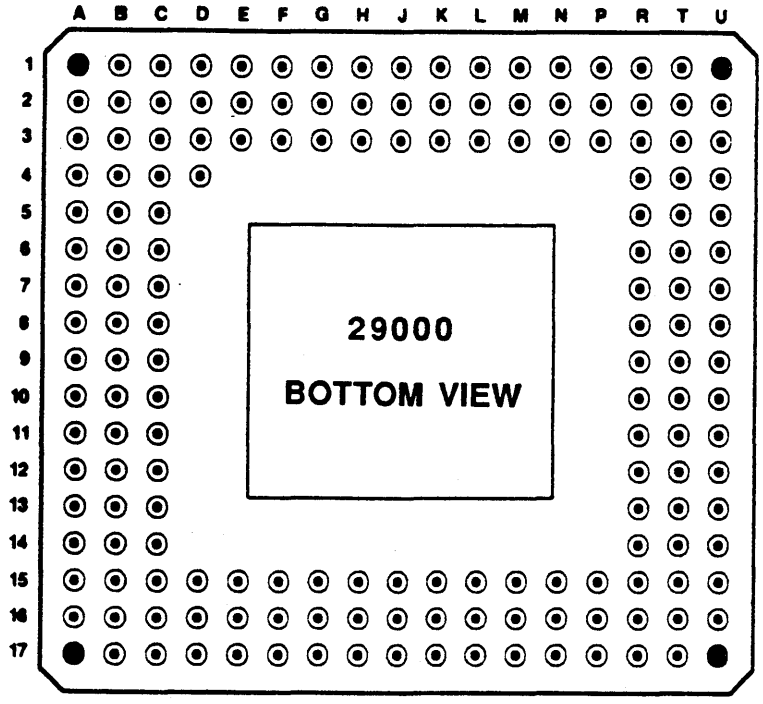


Figure 4-2 29000 Microprocessor Pin Locations

Chapter 5

INSTALLATION

SCRAMBLER BOX TO TARGET SYSTEM CONNECTIONS

The 29000 microprocessor chip must be removed from the target system and the Probe Adapter is installed in its place. The microprocessor chip is then inserted into the probe adapter via the Zero Insertion Force (ZIF) socket. The Probe Adapter is connected to the Scrambler Box with three attached cables as shown in Figure 5-1. The Probe Adapter contains one jumper connection (W1) which is described in Chapter 6 (see description of INCLK Signal Loading).

Procedure

Use the following procedure to connect Scrambler Box to the target system:

1. Remove the 29000 microprocessor chip from target system socket and install the base of probe adapter into the target system socket. Observe the location of pin A1 on probe adapter which must mate with pin A1 on the target system socket for correct alignment of pins.

2. Install the microprocessor chip on probe adapter via the ZIF socket. Ensure pin locations on the microprocessor chip are aligned with corresponding pins on the probe adapter .

3. Verify the three ribbon cables from scrambler box are securely fastened to probe adapter at connectors T1, T2, and T3. (The MAP package is shipped with these cables connected to the probe adapter; however, they could become loose during transit.)

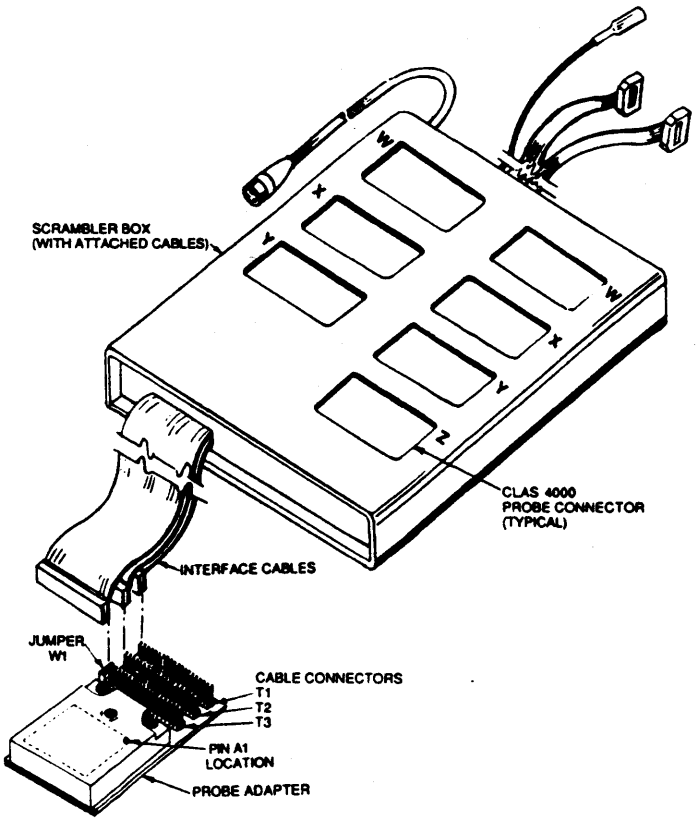


Figure 5-1. Scrambler Box to Probe Adapter Connections

SCRAMBLER BOX TO CLAS 4000 CONNECTIONS

The clock interface cables attached to the Scrambler Box must be connected to the CLAS 4000 and input probes for the CLAS 4000 are connected to the Scrambler Box as shown in Figure 5-2. Probe connectors on top of the Scrambler Box are labeled W, X, Y, and Z to identify the location for a corresponding analyzer probe.

The two Clock Probe Interface Adapters supplied with the MAP package must be installed on the Z Channel connector at Data Boards A and B. These adapters are used to connect both the analyzer probe cable and Scrambler Box clock interface cable to the Z connector.

The two Scrambler Box Clock Interface cables contain16-pin connectors which plug into mating connectors on the Clock Probe Adapters. The 100 MHz coaxial cable on the Scrambler Box attaches to a jack on the CLAS 4000 Control Board Panel.

The 29000 MAP Scrambler Box receives +5 Volts power input from the CLAS 4000. The power is supplied from the SCSI Port Expansion and MAP Power Module (Product No. A70042). This option must be installed on the CLAS 4000 chassis to power the MAP Scrambler Box for Pipeline/Burst Access mode. (This option is not required for Simple Access mode.)

Procedure

Use the following procedure to connect the the Scrambler Box to the CLAS 4000:

1. Ensure AC power is off at CLAS 4000 prior to connecting the Scrambler Box.

2. Remove analyzer probe cables from Z Channel location on Data Boards A and B. Install a clock probe adapter at each of the Z Channel connectors. Connect analyzer probe cables to the adapter.

3. Connect two clock input signal cables and coaxial cable from Scrambler Box to CLAS 4000 as follows:

   a) Locate the clock interface cable which is labeled POWER/GROUND THRESHOLD. Connect this cable to the mating connector on Clock Probe Adapter at Data Board A.

NOTE: This cable supplies signals that control the synchronization of clocks and must be connected to the adapter at Data Board A.

   b) Connect the other clock input cable to Clock Probe Adapter at Data Board B.

   c) Connect the 100 MHz coaxial cable to one of the CLK OUT jacks on CLAS 4000 Control Panel.

NOTE: The 5-Volt power requirement for scrambler box is determined by the clocking scheme setup. Refer to description of 29000 Clocking Considerations in Chapter 6. If power is not required for the user's setup, omit Step 4. If power is required, perform Step 4.

4. Connect the Scrambler Box power cord to one of the 5-Volt SCSI connectors at lower front panel of CLAS 4000 chassis.

5. Remove flying leads and grabbers from analyzer probe connectors (if attached) and connect seven probes, W, W, X , X, Y, Y, and Z into corresponding Scrambler Box locations as follows:

   a) Connect W and X probes from Data Board A to corresponding W and X probe locations on right side of Scrambler Box (see orientation in Figure 5-2).

   b) Connect W and X probes from Data Board B to corresponding W and X probe locations on left side of Scrambler Box .

c) Connect Y probe from Data Board A to Y probe location on right side of Scrambler Box.

d) Connect Z probe from clock probe adapter at Data Board A to Z probe location on Scrambler Box .

e) Connect Y probe at Data Board B to Y probe location on left side of Scrambler Box.

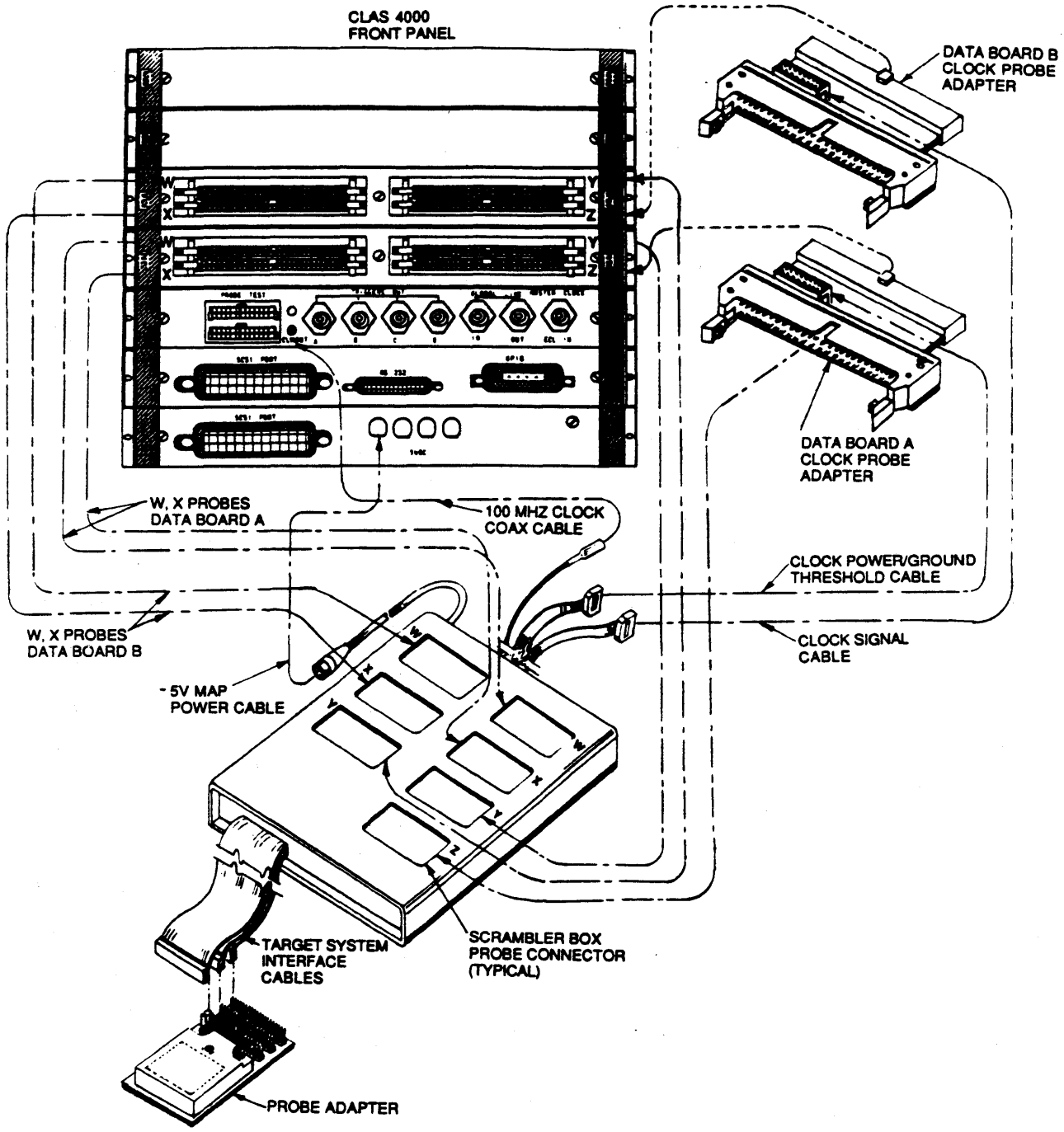


Figure 5-2. Scrambler Box to CLAS 4000 Connections

MICROPROCESSOR PINOUTS TO LOGIC ANALYZER

Signals for the following lines (143 total) are transferred from the 29000 microprocessor in the target system under test to the Scrambler Box :

32 Data Lines	(D0 - D31)
32 Address Lines	(A0 - A31)
32 Instruction Lines	(I0 - I31)
47 Status and Control Lines	

These signals are also transferred from the Scrambler Box to the assigned Logic Analyzer channel in the CLAS 4000.

The list in Table 5-1 identifies the assigned Signal Name/Function for each 29000 pin, the Target Head pin connections, MAP Scrambler Board pin connections, and the corresponding Logic Analyzer channel connections. Schematic diagrams for circuit connections are provided in Chapter 6.

The following conventions are used in Table 5-1:

- The abbreviation GND indicates ground.

- The asterisk (*) character following the signal name indicates active-low logic level.

Table 5-1. 29000 MICROPROCESSOR-TO-LOGIC ANALYZER CONNECTIONS

PGA Pin#	Signal of 29000	Cable-Conductor	Probe Pin#	Channel # CLAS 4000	Data Bd.#
M16	A00	T3-20	J01-03	CH00	1
M17	A01	T3-26	J01-05	CH01	1
R15	A02	T2-11	J01-07	CH02	1
T16	A03	T3-04	J01-09	CH03	1
T17	A04	T3-10	J01-11	CH04	1
P15	A05	T2-09	J01-13	CH05	1
R16	A06	T3-08	J01-15	CH06	1
R17	A07	T3-14	J01-17	CH07	1
P16	A08	T3-12	J01-19	CH08	1
P17	A09	T3-18	J01-21	CH09	1
L16	A10	T2-20	J01-23	CH10	1
L17	A11	T2-26	J01-25	CH11	1
K16	A12	T2-24	J02-03	CH12	1
K17	A13	T2-01	J02-05	CH13	1
J17	A14	T2-47	J02-07	CH14	1
J15	A15	T1-02	J02-09	CH15	1
J16	A16	T2-03	J02-11	CH16	1
H17	A17	T2-43	J02-13	CH17	1
H16	A18	T2-49	J02-15	CH18	1
G17	A19	T2-30	J02-17	CH19	1
G16	A20	T2-28	J02-19	CH20	1
F17	A21	T3-28	J02-21	CH21	1
G15	A22	T3-46	J02-23	CH22	1
E17	A23	T3-32	J02-25	CH23	1
F16	A24	T3-24	J03-03	CH24	1
F15	A25	T2-45	J03-05	CH25	1
D17	A26	T3-36	J03-07	CH26	1
E16	A27	T3-30	J03-09	CH27	1
D16	A28	T3-34	J03-11	CH28	1
C17	A29	T3-40	J03-13	CH29	1
B17	A30	T3-44	J03-15	CH30	1
D15	A31	T2-41	J03-17	CH31	1
B4	D00	T1-46	J09-03	CH00	2
B5	D01	T1-45	J09-05	CH01	2
A4	D02	T1-50	J09-07	CH02	2
C6	D03	T1-43	J09-09	CH03	2
A5	D04	T1-39	J09-11	CH04	2
B6	D05	T1-49	J09-13	CH05	2
A6	D06	T1-47	J09-15	CH06	2
C7	D07	T2-37	J09-17	CH07	2
B7	D08	T1-31	J09-19	CH08	2
A7	D09	T1-27	J09-21	CH09	2
B8	D10	T1-33	J09-23	CH10	2
A8	D11	T1-29	J09-25	CH11	2

Table 5-1 (Cont'd.)

PGA Pin#	Signal of 29000	Cable-Conductor	Probe Pin#	Channel # CLAS 4000	Data Bd.#
A9	D12	T1-37	J10-03	CH12	2
B9	D13	T1-35	J10-05	CH13	2
A10	D14	T2-50	J10-07	CH14	2
B10	D15	T2-48	J10-09	CH15	2
A11	D16	T2-46	J10-11	CH16	2
B11	D17	T2-44	J10-13	CH17	2
A12	D18	T2-40	J10-15	CH18	2
B12	D19	T2-36	J10-17	CH19	2
A13	D20	T2-42	J10-19	CH20	2
A14	D21	T2-29	J10-21	CH21	2
C12	D22	T2-32	J10-23	CH22	2
B13	D23	T2-38	J10-25	CH23	2
B14	D24	T2-33	J11-03	CH24	2
A15	D25	T2-23	J11-05	CH25	2
C13	D26	T2-34	J11-07	CH26	2
A16	D27	T3-48	J11-09	CH27	2
B15	D28	T2-27	J11-11	CH28	2
B16	D29	T3-42	J11-13	CH29	2
C15	D30	T2-31	J11-15	CH30	2
C16	D31	T3-38	J11-17	CH31	2
A3	I00	T1-48	J03-19	CH32	1
A2	I01	T1-42	J03-21	CH33	1
C4	I02	T1-41	J03-23	CH34	1
B3	I03	T1-44	J03-25	CH35	1
C3	I04	T1-34	J04-03	CH36	1
B2	I05	T1-38	J04-05	CH37	1
B1	I06	T1-36	J04-07	CH38	1
D3	I07	T1-32	J04-09	CH39	1
C2	I08	T3-47	J04-11	CH40	1
C1	I09	T3-49	J04-13	CH41	1
D2	I10	T3-43	J04-15	CH42	1
D1	I11	T3-45	J04-17	CH43	1
E2	I12	T3-39	J04-19	CH44	1
E1	I13	T3-41	J04-21	CH45	1
F3	I14	T1-30	J04-23	CH46	1
F2	I15	T3-35	J04-25	CH47	1
F1	I16	T3-37	J05-03	CH48	1
G3	I17	T1-28	J05-05	CH49	1
G2	I18	T3-31	J05-07	CH50	1
G1	I19	T3-33	J05-09	CH51	1
H1	I20	T3-29	J05-11	CH52	1
H3	I21	T2-39	J05-13	CH53	1
H2	I22	T3-27	J05-15	CH54	1
J1	I23	T3-25	J05-17	CH55	1
J2	I24	T3-23	J05-19	CH56	1
K2	I25	T3-19	J05-21	CH57	1
K1	I26	T3-21	J05-23	CH58	1

Table 5-1 (Cont'd.)

PGA Pin#	Signal of 29000	Cable-Conductor	Probe Pin#	Channel # CLAS 4000	Data Bd.#
L1	I27	T3-17	J05-25	CH59	1
L2	I28	T3-15	J06-03	CH60	1
M1	I29	T3-13	J06-05	CH61	1
M2	I30	T3-11	J06-07	CH62	1
N1	I31	T3-09	J06-09	CH63	1
T9	BGRT*	T1-15	J12-03	CH36	2
T8	BINV*	T1-19	J06-11	CH64	1
T2	BREQ*	T1-18	J12-05	CH37	2
T2	CDA*	T1-16	J12-07	CH94	1 & 2
R2	CDA*	T1-16	J12-07	CH38	2
P2	CNTL0	T3-03	J12-09	CH39	2
P1	CNTL1	T3-05	J12-11	CH40	2
R9	DBREQ*	T2-13	J12-13	CH41	2
T10	DREQ*	T2-06	J06-13	CH65	1
U13	DREQT0	T2-14	J06-15	CH66	1
U12	DREQT1	T2-08	JO6-17	CH67	1
R4	DBACK*	T1-11	J12-15	CH42	2
T3	DERR*	T1-10	J12-17	CH43	2
R3	DRDY*	T1-22	J12-19	CH44	2
R3	DRDY*	T1-22	J12-19	CH90	1 & 2
T7	INTRN0	T1-21	J11-19	CH32	2
U6	INTRN1	T1-05	J11-21	CH33	2
T6	INTRN2	T1-03	J11-23	CH34	2
U5	INTRN3	T1-09	J11-25	CH35	2
U8	IBREQ*	T1-23	J06-19	CH68	1
U9	IREQ*	T1-17	J06-21	CH69	1
U15	IREQT	T2-21	J12-21	CH45	2
U4	IBACK*	T1-04	J06-23	CH70	1
U3	IERR*	T1-O6	J12-23	CH46	2
T1	INCLK	T1-12	J12-25	CH47	2
T4	IRDY*	T1-13	J06-25	CH71	1
T4	IRDY*	T1-13	J06-25	CH91	1 & 2
T11	LOCK*	T2-10	J07-03	CH72	1
N17	MPGM0	T3-22	J07-05	CH73	1
N16	MPGM1	T3-16	J07-07	CH74	1
T12	MSERR	T2-12	J13-03	CH48	2
R14	OPT0	T2-15	J07-09	CH75	1
T15	OPT1	T2-17	J07-11	CH76	1
U16	OPT2	T3-02	J07-13	CH77	1
U02	PEN*	T1-14	J07-15	CH78	1
P03	PWRCLK	T1-20	J13-05	CH49	2
R10	PDA*	T2-16	J13-07	CH50	2
U10	PIA*	T2-02	J07-17	CH79	1

Table 5-1 (Cont'd.)

PGA Pin#	Signal of 29000	Cable-Conductor	Probe Pin#	Channel # CLAS 4000	Data Bd.#
U11	R/W*	T2-04	J13-09	CH51	2
R01	RESET*	T3-01	J13-11	CH52	2
T13	STAT0	T2-18	J13-13	CH53	2
U14	STAT1	T2-25	J13-15	CH54	2
R12	STAT2	T2-22	J13-17	CH55	2
T14	SUP/US*	T2-19	J07-19	CH80	1
N03	SYSCLK	T1-24	J13-19	CH56	2
N03	SYSCLK	T1-24	J13-19	CH92	1 & 2
N02	TEST*	T3-07	J13-21	CH57	2
U07	TRAP0*	T1-25	J13-23	CH58	2
R07	TRAP1*	T1-01	J13-25	CH59	2
T05	WAR*	T1-07	J14-03	CH60	2
C14	VCC	T2-35	J14-05	CH61	2
M14	GND	T2-05			
A01	GND	T1-40			
A17	GND	T3-50			
N15	GND	T2-07			
U01	GND	T1-08			
M03	GND	T1-26			
U17	GND	T3-06			
J01 TO J14 ALL ODD PINS SHORT TO GND.					

Chapter 6

SPECIAL OPERATING FEATURES

GENERAL

This chapter describes special operating features for the 29000 MAP Disassembler as related to unique characteristics of the AM29000 microprocessor. Example screens are provided for Setup Display Windows and Data Display Windows.

Reference: AMD Am29000 32-Bit Streamlined Instruction Processor User's Manual

INSTRUCTION PROCESSING

Branch Instructions

The Am29000 calculates branch addresses for direct branches (both CALL and JMPx) in one of two ways. The first method sign-extends the concatenated values of the RC and RB instruction fields, shifts the whole thing left two bits (32-bit word alignment), and adds the result to the current PC. The second method zero-extends the concatenated values of the RC and RB instruction fields and shifts the whole thing left two bits (32-bit word alignment) to produce an absolute address value.

The disassembler displays the calculated value instead of the actual displacement value contained in the instruction.

Although the Am29000 allows placement of two consecutive branch instructions, the delayed branching feature of the Am29000 may produce unexpected results unless the programmer specifically designed the code to take advantage of this feature. See pages 7-24 and 7-25 of the Reference Am29000 Users Manual for further information on this effect.

As an aid to programmers, the disassembler places an exclamation point (!) in front of any branch instruction that immediately follows another branch instruction.

Trap Instructions

Trap instructions (EMULATE, ASxxx) contain an eight-bit vector number that is used to create a vector address in one of two ways. If the Vector Fetch bit in the Configuration Register is set, the vector number replaces bits 9 - 2 of the Vector Area Base register and the result is used to fetch the actual trap vector from memory (indirect method). If the Vector Fetch bit is reset, the vector number replaces bits 15 - 8 of the Vector Area Base register and the result is used to fetch the first trap instruction from memory (direct method).

The disassembler can not determine the state of the Vector Fetch bit directly, so it assumes the bit is cleared (Indirect Mode). The user may select Direct Mode by first selecting the 'Disassembler Configuration' menu entry from the 'Options' menu, and then clicking the mouse on the selection button next to the desired mode (see description of 29000 Disassembler Configuration).

The disassembler displays the calculated value (surrounded by angle brackets if indirect), followed by the actual eight-bit vector number as a decimal number in parenthesis.

The Am29000 causes a Protection Violation trap to occur if the processor is in User mode and attempts to execute a trap with a vector number of 0 - 63. The disassembler marks such trap instructions with an exclamation point (!) prior to the mnemonic.

REGISTER ASSIGNMENTS

Registers are identified by the designators IP, SP, GRxxx and LRxxx, corresponding to the 29000 absolute register numbers according to the following table:

ABSOLUTE #	IDENTIFIER	
0	IP	(Indirect Pointer)
1	SP	(Stack Pointer)
2 - 63	--	Global Register 2 - 63 (Unimplemented)
64 - 127	GRxxx	Global Register 64 - 127
128 - 255	LRxxx	Local Register 0 - 127

ILLEGAL OPCODE

If the 29000 Disassembler encounters an illegal opcode, the message -ILLEGAL- is displayed in the mnemonic field. If the opcode is legal, but one or more of the operands is illegal, the mnemonic will be displayed, along with any operands that were legally decoded. If an illegal opcode is encountered, the Comment column will contain the message '## Illegal Operand'.

Instructions that reference Global registers 2 - 63 (unimplemented), will correctly display the global register in question, but will also be marked '!! Illegal Operand'.

The instruction coding for 'ASEQ xx,GR1,GR1' is generally considered and used as a NOP (see Reference Am29000 User's Manual, page 7-13), since it does not perform any action (GR1 will always be equal to GR1).

The disassembler, therefore, will display the psuedo-mnemonic of 'NOP' whenever this instruction encoding is found.

MESSAGES

Trap Messages

The messages presented below are displayed in the Comment column for lines that contain either trap instructions, or the first instruction of a trap routine. The messages are derived from the trap vector list in the Reference Am29000 User's Manual, pages 3-45 and 3-46.

Trap	Message
0	@@ Illegal Opcode
1	@@ Unaligned Access
2	@@ Out of Range
3	@@ Coprocessor Not Present
4	@@ Coprocessor Exception
5	@@ Protection Violation
6	@@ Instr Access Exception
7	@@ Data Access Exception
8	@@ User Instr TLB Miss
9	@@ User Data TLB Miss
10	@@ Super Instr TLB Miss
11	@@ Super Data TLB Miss
12	@@ Instr TLB Prot Violation
13	@@ Data TLB Prot Violation
14	@@ Timer
15	@@ Trace
16	@@ *INTR0
17	@@ *INTR1
18	@@ *INTR2

Trap Messages (Cont.)

19	@@ *INTR3
20	@@ *TRAP0
21	@@ *TRAP1
22-23	@@ Reserved Trap
24-31	@@ Reserved Emulation Trap
32	@@ MULTIPLY
33	@@ DIVIDE
34	@@ MULTIPLU
35	@@ DIVIDU
36	@@ CONVER
37-41	@@ Reserved Emulation Trap
42	@@ FEQ
43	@@ DEQ
44	@@ FGT
45	@@ DGT
46	@@ FGE
47	@@ DGE
48	@@ FADD
49	@@ DADD
50	@@ FSUB
51	@@ DSUB
52	@@ FMUL
53	@@ DMUL
54	@@ FDIV
55	@@ DDI
56-63	@@ Reserved Emulation Trap
64-255	@@ Assert/EMULATE Trap

Status Messages

The Status column messages are interpreted as follows:

Message	SUP/US	*IRDY	R/W	DREQT1	DREQT0
U Fetch (User)	0	0	x	x	x
U Data Wr	0	1	0	0	0
U I/O Wr	0	1	0	0	1
U CP Wr	0	1	0	1	x
U Data Rd	0	1	1	0	0
U I/O Rd	0	1	1	0	1
U CP Rd	0	1	1	1	x
S Fetch (Supervisor)	1	0	x	x	x
S Data Wr	1	1	0	0	0
S I/O Wr	1	1	0	0	1
S CP Wr	1	1	0	1	x
S Data Rd	1	1	1	0	0
S I/O Rd	1	1	1	0	1
S CP Rd	1	1	1	1	x

BURST MODE

When the Am29000 is operating in 'Burst' Mode, it generates one address and then clocks in one or more data/instruction words without changing the address.

If the disassembler detects Burst Mode operation, it artificially generates the missing addresses. Artificial addresses are marked as such by an asterisk (*) in the most significant digit. The first address of a Burst is not marked in this fashion (it is the actual address output by the processor), and can be used to obtain the missing digit.

If a recording begins in the middle of a Burst Mode access, the disassembler can not know how many accesses have occurred since the start of the burst; therefore, the generated address may be incorrect.

29000 DISASSEMBLER CONFIGURATION

The Am29000 Vector Area Base (VAB) Register is a 32-bit register in the Am29000 that contains the upper 16 bits of all trap vector addresses. The 29000 Disassembler allows the user to specify the value currently being used by the 29000 processor to allow accurate tagging of trap execution.

To change from the default trap vector of 0, click the mouse on the Disassembler Configuration menu entry under the Options menu (Figure 6-1) when a disassembler window is active. Enter the most significant 16 bits of the desired trap vector. Note that the lower 16 bits are always zero, as indicated by the 4,0 digits to the right of the 6-digit numerical entry field. The trap vector value is entered in Hexadecimal notation.

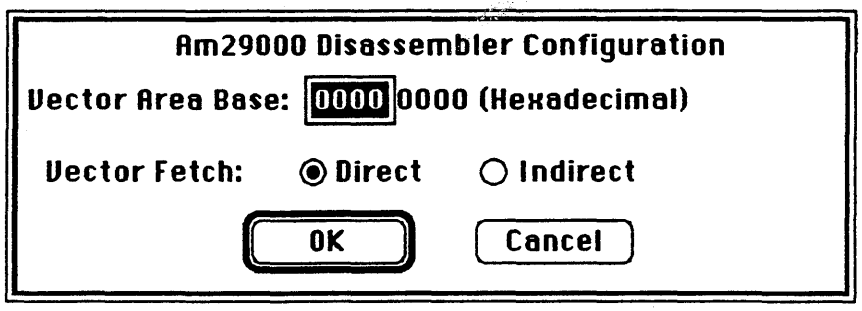


Figure 6-1. 29000 Disassembler Configuration Dialog Box

29000 CLOCKING CONSIDERATIONS

Simple Access (Default) Clock Setup

The 29000 operates in various modes which may require alteration of the clock setup condition. The default setup condition supplied on diskette is intended for simple access for both instructions and data. In this default mode, all Address, Data and Status is latched on the rising edge of the target System Clock (Channel 92) and is mastered by ANDing signals for DRDY (Channel 90) and IRDY (Channel 91).

Pipeline/Burst Access (Alternate) Clock Setup

For Pipeline or Burst access, it is necessary to latch the appropriate addresses during the proper IREQ or DREQ cycle. These signals are ANDed on the scrambler board for this contingency, and the result is available on Channel 93. By ORing this signal with the target system clock, the Address Latch signal occurs only during the appropriate part of the address cycle.

The alternate Clock Setup to recognize Pipeline and Burst access for both Instruction and Data is shown in Figure 6-4.

NOTE: To use this signal in the clock setup, +5 Volts must be supplied to the scrambler board via the attached power cord provided with the MAP Package. The +5 Volts can be supplied by the user's power source or by the optional SCSI Port Expansion and MAP Power Module on the CLAS 4000.

Additionally, the CDA signal is available on Channel 94 for clocking the write cycle to a coprocessor. This signal may be either ANDed or ORed with the master clock depending upon how this signal is used in the target system.

INCLK Signal Loading

Some target system configurations may experience input loading of the INCLK signal which is supplied to Analyzer channel 47 of Data Board 2. A single-position jumper connection (W1) is located on the Probe Adapter. Removing this jumper allows the user to disconnect the INCLK signal from the MAP.

EXAMPLE SETUP DISPLAY WINDOWS

Example displays for Channel Setup, Clock Setup, and Trace Setup are presented below.

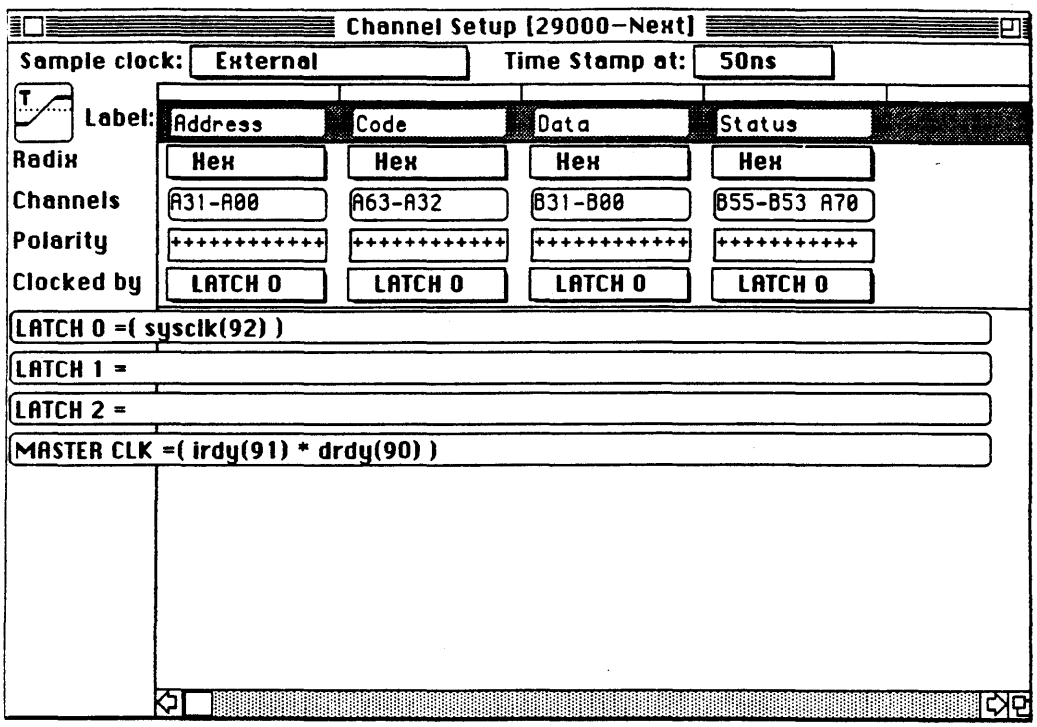


Figure 6-2. Channel Setup, Simple Access Default Clocking Scheme

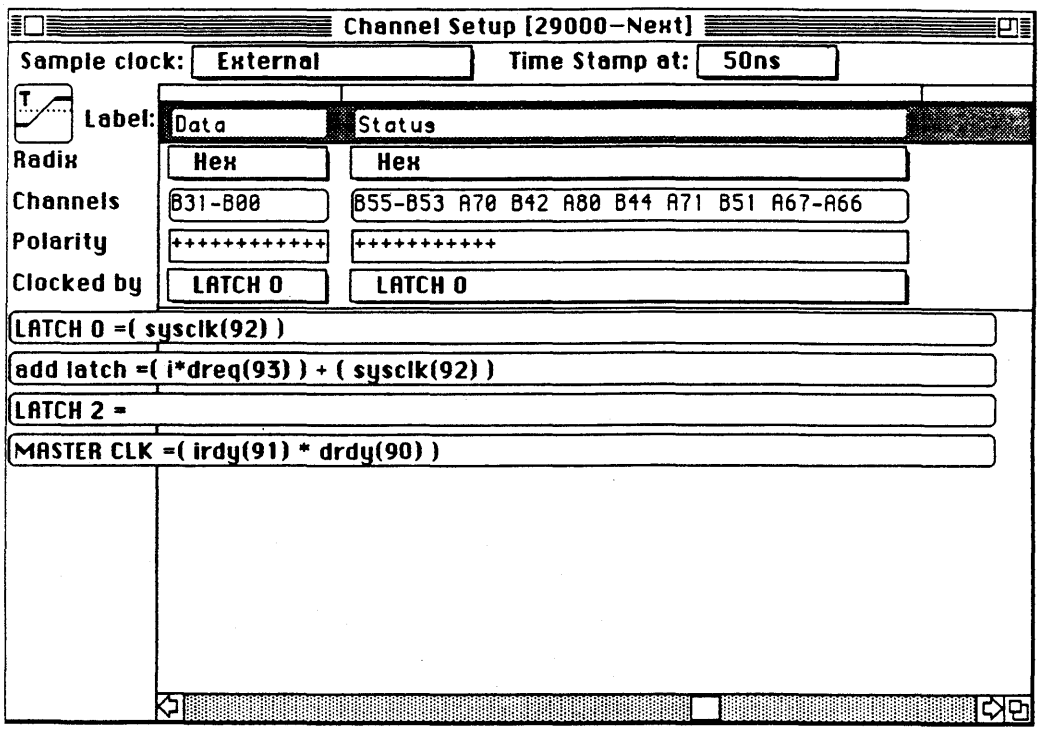


Figure 6-3. Alternate Clock Setup with Values in Status Block

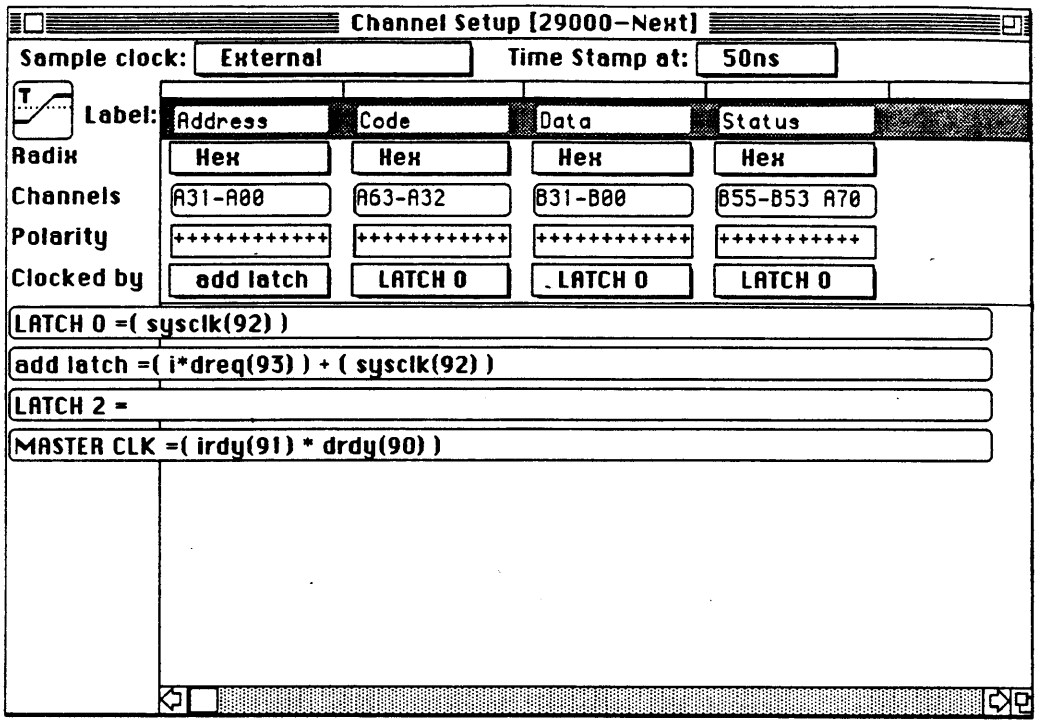


Figure 6-4. Alternate Clock Setup, Pipeline/Burst Access Mode

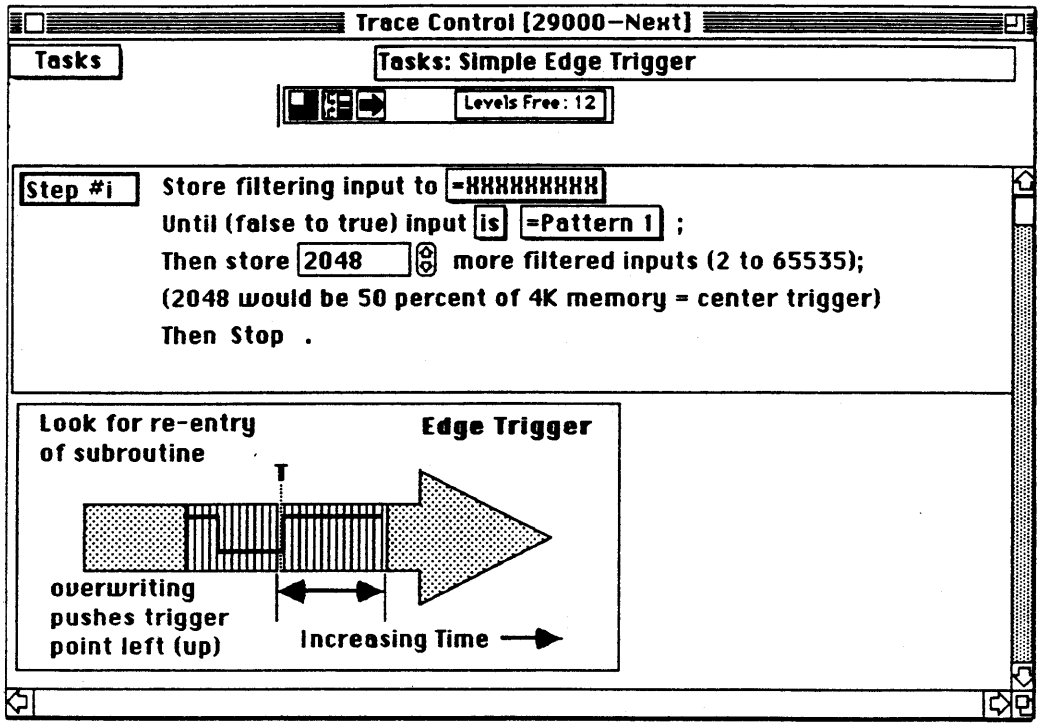
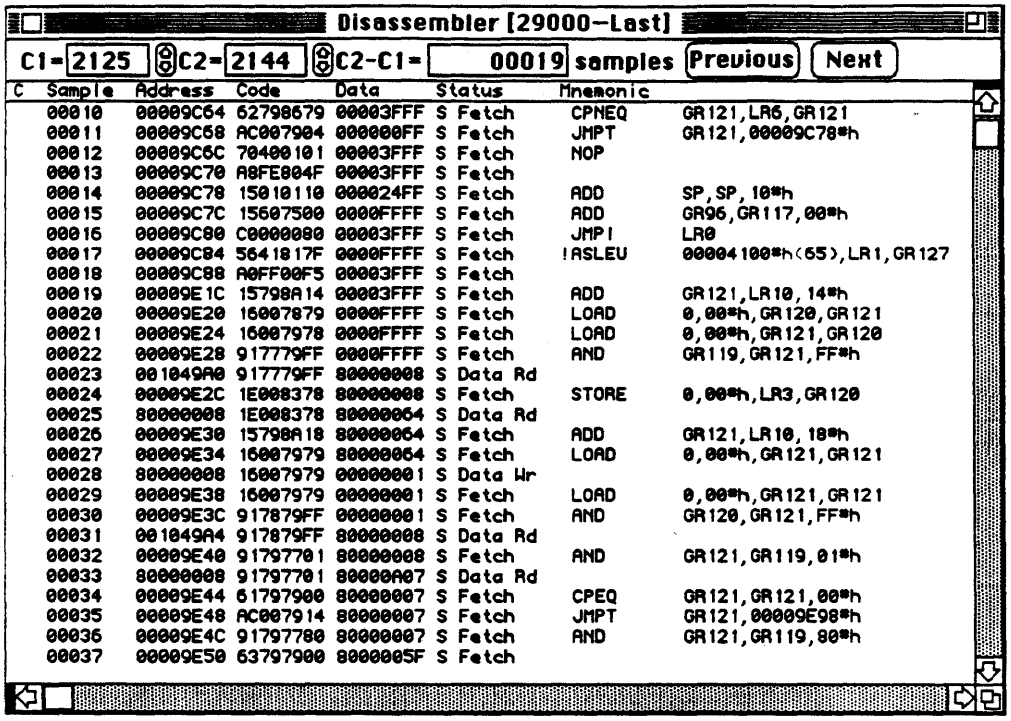


Figure 6-5. Trace Setup, Trigger Sequence Display Window

EXAMPLE DATA DISPLAY WINDOWS

Example displays are presented for All Cycles, Deletion of Non-Executed Instructions, Read/Write Only Instructions, and No Read/Write Instructions Executed.

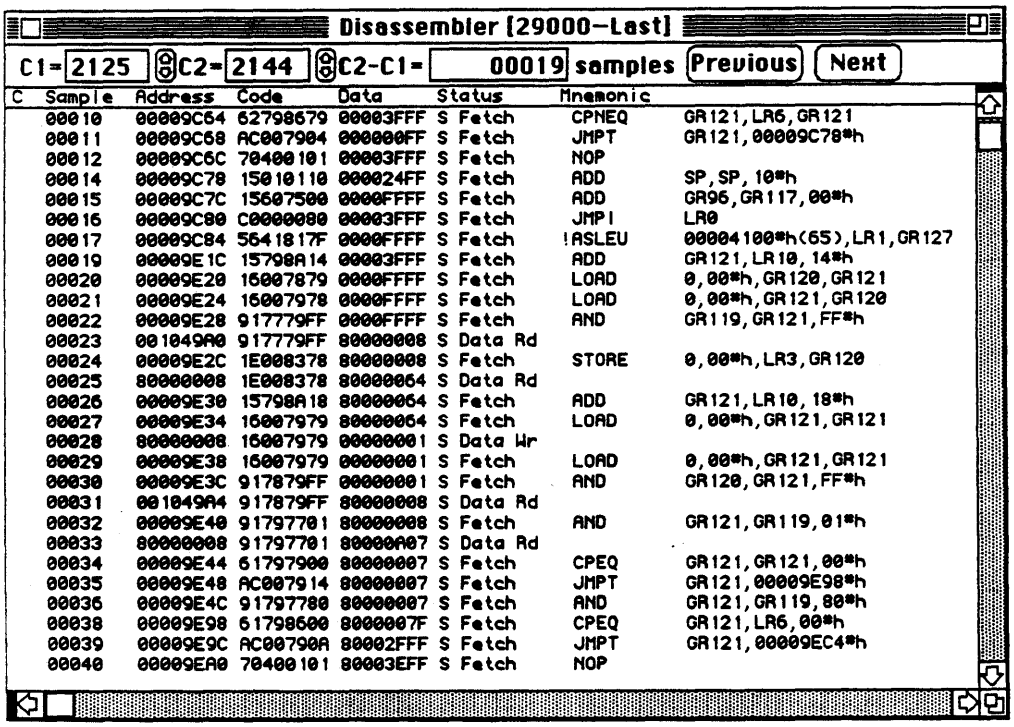


Disassembler [29000–Last]

C1=2125 C2=2144 C2-C1= 00019 samples Previous Next

C	Sample	Address	Code	Data	Status	Mnemonic	
	00010	00009C64	62798679	00003FFF	S Fetch	CPNEQ	GR121,LR6,GR121
	00011	00009C68	AC007904	000000FF	S Fetch	JMPT	GR121,00009C78*h
	00012	00009C6C	70400101	00003FFF	S Fetch	NOP	
	00013	00009C70	A8FE804F	00003FFF	S Fetch		
	00014	00009C78	15010110	000024FF	S Fetch	ADD	SP,SP,10*h
	00015	00009C7C	15607500	0000FFFF	S Fetch	ADD	GR96,GR117,00*h
	00016	00009C80	C0000080	00003FFF	S Fetch	JMPI	LR0
	00017	00009C84	5641817F	0000FFFF	S Fetch	!ASLEU	00004100*h(65),LR1,GR127
	00018	00009C88	A0FF00F5	00003FFF	S Fetch		
	00019	00009E1C	15798A14	00003FFF	S Fetch	ADD	GR121,LR10,14*h
	00020	00009E20	16007879	0000FFFF	S Fetch	LOAD	0,00*h,GR120,GR121
	00021	00009E24	16007978	0000FFFF	S Fetch	LOAD	0,00*h,GR121,GR120
	00022	00009E28	917779FF	0000FFFF	S Fetch	AND	GR119,GR121,FF*h
	00023	001049A0	917779FF	80000008	S Data Rd		
	00024	00009E2C	1E008378	80000008	S Fetch	STORE	0,00*h,LR3,GR120
	00025	80000008	1E008378	80000064	S Data Rd		
	00026	00009E30	15798A18	80000064	S Fetch	ADD	GR121,LR10,18*h
	00027	00009E34	16007979	80000064	S Fetch	LOAD	0,00*h,GR121,GR121
	00028	80000008	16007979	00000001	S Data Wr		
	00029	00009E38	16007979	00000001	S Fetch	LOAD	0,00*h,GR121,GR121
	00030	00009E3C	917879FF	00000001	S Fetch	AND	GR120,GR121,FF*h
	00031	001049A4	917879FF	80000008	S Data Rd		
	00032	00009E40	91797701	80000008	S Fetch	AND	GR121,GR119,01*h
	00033	80000008	91797701	80000A07	S Data Rd		
	00034	00009E44	61797900	80000007	S Fetch	CPEQ	GR121,GR121,00*h
	00035	00009E48	AC007914	80000007	S Fetch	JMPT	GR121,00009E98*h
	00036	00009E4C	91797780	80000007	S Fetch	AND	GR121,GR119,80*h
	00037	00009E50	63797900	8000005F	S Fetch		

Figure 6-6. All Cycles, Display Window



Disassembler [29000–Last]

C1=2125 C2=2144 C2-C1= 00019 samples Previous Next

C	Sample	Address	Code	Data	Status	Mnemonic	
	00010	00009C64	62798679	00003FFF	S Fetch	CPNEQ	GR121,LR6,GR121
	00011	00009C68	AC007904	000000FF	S Fetch	JMPT	GR121,00009C78*h
	00012	00009C6C	70400101	00003FFF	S Fetch	NOP	
	00014	00009C78	15010110	000024FF	S Fetch	ADD	SP,SP,10*h
	00015	00009C7C	15607500	0000FFFF	S Fetch	ADD	GR96,GR117,00*h
	00016	00009C80	C0000080	00003FFF	S Fetch	JMPI	LR0
	00017	00009C84	5641817F	0000FFFF	S Fetch	!ASLEU	00004100*h(65),LR1,GR127
	00019	00009E1C	15798A14	00003FFF	S Fetch	ADD	GR121,LR10,14*h
	00020	00009E20	16007879	0000FFFF	S Fetch	LOAD	0,00*h,GR120,GR121
	00021	00009E24	16007978	0000FFFF	S Fetch	LOAD	0,00*h,GR121,GR120
	00022	00009E28	917779FF	0000FFFF	S Fetch	AND	GR119,GR121,FF*h
	00023	001049A0	917779FF	80000008	S Data Rd		
	00024	00009E2C	1E008378	80000008	S Fetch	STORE	0,00*h,LR3,GR120
	00025	80000008	1E008378	80000064	S Data Rd		
	00026	00009E30	15798A18	80000064	S Fetch	ADD	GR121,LR10,18*h
	00027	00009E34	16007979	80000064	S Fetch	LOAD	0,00*h,GR121,GR121
	00028	80000008	16007979	00000001	S Data Wr		
	00029	00009E38	16007979	00000001	S Fetch	LOAD	0,00*h,GR121,GR121
	00030	00009E3C	917879FF	00000001	S Fetch	AND	GR120,GR121,FF*h
	00031	001049A4	917879FF	80000008	S Data Rd		
	00032	00009E40	91797701	80000008	S Fetch	AND	GR121,GR119,01*h
	00033	80000008	91797701	80000A07	S Data Rd		
	00034	00009E44	61797900	80000007	S Fetch	CPEQ	GR121,GR121,00*h
	00035	00009E48	AC007914	80000007	S Fetch	JMPT	GR121,00009E98*h
	00036	00009E4C	91797780	80000007	S Fetch	AND	GR121,GR119,80*h
	00038	00009E98	61798600	8000007F	S Fetch	CPEQ	GR121,LR6,00*h
	00039	00009E9C	AC00790A	80002FFF	S Fetch	JMPT	GR121,00009EC4*h
	00040	00009EA0	70400101	80003EFF	S Fetch	NOP	

Figure 6-7. Delete Non-Executed Instructions, Display Window

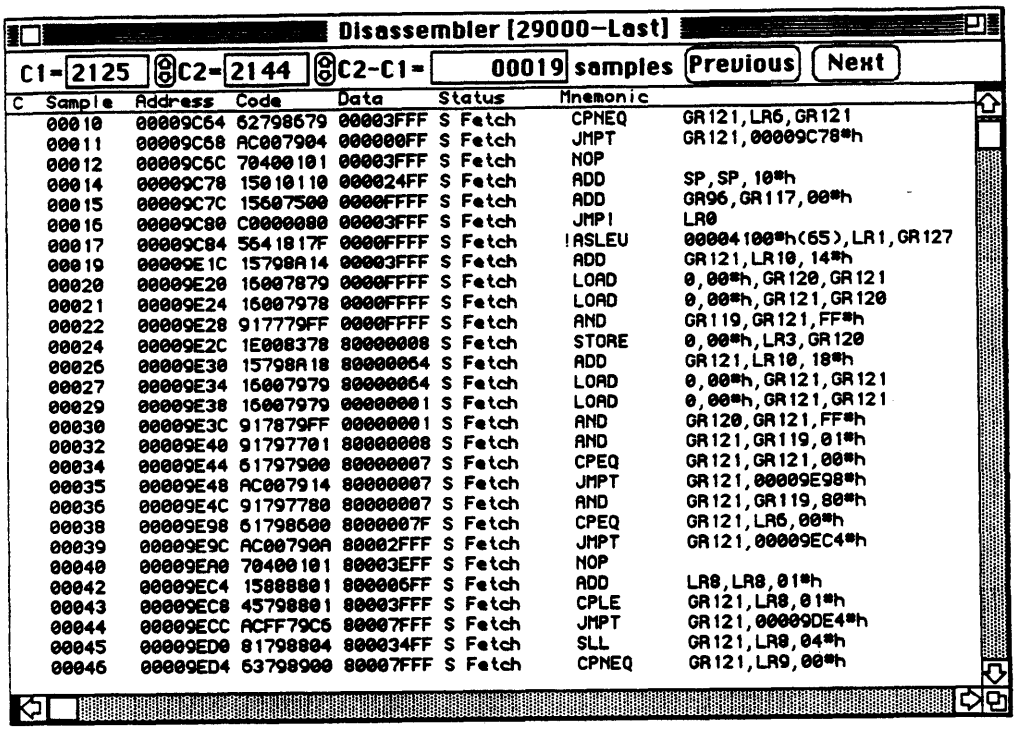


Figure 6-8. Executed Only Instructions, Display Window

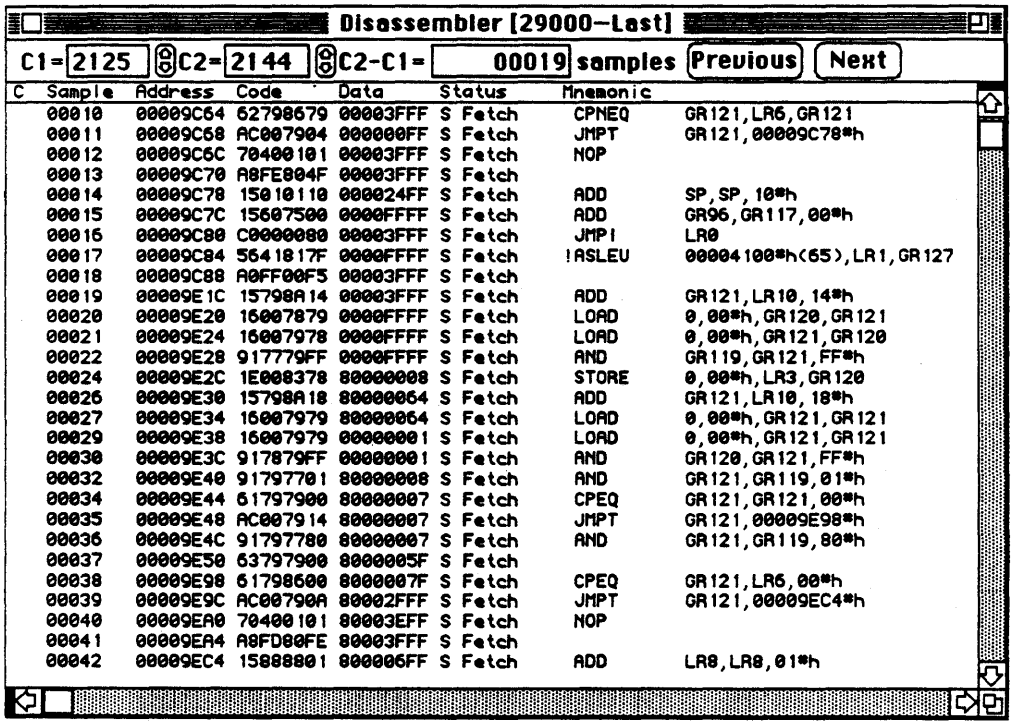


Figure 6-9. No Read/Write Data, Display Window

REVISIONS							
ZONE	REV.	ECO#	DESCRIPTION	DRWN	CHKD	APVD	DATE

P3-20 A00 03-J01
P3-26 A01 05-J01
P2-11 A02 07-J01
P3-04 A03 09-J01
P3-10 A04 11-J01
P2-09 A05 13-J01
P3-08 A06 15-J01
P3-14 A07 17-J01
P3-12 A08 19-J01
P3-18 A09 21-J01
P2-20 A10 23-J01
P2-26 A11 25-J01
P2-24 A12 03-J02
P2-01 A13 05-J02
P2-47 A14 07-J02
P1-02 A15 09-J02
P2-03 A16 11-J02
P2-43 A17 13-J02
P2-49 A18 15-J02
P2-30 A19 17-J02
P2-28 A20 19-J02
P3-28 A21 21-J02
P3-46 A22 23-J02
P3-32 A23 25-J02
P3-24 A24 03-J03
P2-45 A25 05-J03
P3-36 A26 07-J03
P3-30 A27 09-J03
P3-34 A28 11-J03
P3-40 A29 13-J03
P3-44 A30 15-J03
P2-41 A31 17-J03

P1-48 I00 19-J03
P1-42 I01 21-J03
P1-41 I02 23-J03
P1-44 I03 25-J03
P1-34 I04 03-J04
P1-38 I05 05-J04
P1-36 I06 07-J04
P1-32 I07 09-J04
P3-47 I08 11-J04
P3-49 I09 13-J04
P3-43 I10 15-J04
P3-45 I11 17-J04
P3-39 I12 19-J04
P3-41 I13 21-J04
P1-30 I14 23-J04
P3-35 I15 25-J04
P3-37 I16 03-J05
P1-28 I17 05-J05
P3-31 I18 07-J05
P3-33 I19 09-J05
P3-29 I20 11-J05
P2-39 I21 13-J05
P3-27 I22 15-J05
P3-25 I23 17-J05
P3-23 I24 19-J05
P3-19 I25 21-J05
P3-21 I26 23-J05
P3-17 I27 25-J05
P3-15 I28 03-J06
P3-13 I29 05-J06
P3-11 I30 07-J06
P3-09 I31 09-J06

P1-46 D00 03-J09
P1-45 D01 05-J09
P1-50 D02 07-J09
P1-43 D03 09-J09
P1-39 D04 11-J09
P1-49 D05 13-J09
P1-47 D06 15-J09
P2-37 D07 17-J09
P1-31 D08 19-J09
P1-27 D09 21-J09
P1-33 D10 23-J09
P1-29 D11 25-J09
P1-37 D12 03-J10
P1-35 D13 05-J10
P2-50 D14 07-J10
P2-48 D15 09-J10
P2-46 D16 11-J10
P2-44 D17 13-J10
P2-40 D18 15-J10
P2-36 D19 17-J10
P2-42 D20 19-J10
P2-29 D21 21-J10
P2-32 D22 23-J10
P2-38 D23 25-J10
P2-33 D24 03-J11
P2-23 D25 05-J11
P2-34 D26 07-J11
P3-48 D27 09-J11
P2-27 D28 11-J11
P3-42 D29 13-J11
P2-31 D30 15-J11
P3-38 D31 17-J11

P1-21 INTRN0 19-J11
P1-05 INTRN1 21-J11
P1-03 INTRN2 23-J11
P1-09 INTRN3 25-J11
P1-15 BGRTN 03-J12
P1-18 BREQN 05-J12
P1-16 CDAN 07-J12
P3-03 CNTL0 09-J12
P3-05 CNTL1 11-J12
P2-13 DBREQN 13-J12
P1-11 DBACKN 15-J12
P1-10 DERRN 17-J12
P2-21 IREQT 21-J12
P1-06 IERRN 23-J12
P1-12 INCLK 25-J12
P2-12 MSERR 03-J13
P1-20 PWRCLK 05-J13
P2-16 PDAN 07-J13
P2-04 R/WN 09-J13
P3-01 RESETN 11-J13
P2-18 STAT0 13-J13
P2-25 STAT1 15-J13
P2-22 STAT2 17-J13
P1-24 SYSCLK 19-J13
P3-07 TESTN 21-J13
P1-25 TRAP0N 23-J13
P1-01 TRAP1N 25-J13
P1-07 WARN 03-J14
P2-35 VCC1 05-J14
P1-22 DRDYN 19-J12

P1-19 BINVN 11-J06
P2-06 DREQN 13-J06
P2-14 DREQT0 15-J06
P2-08 DREQT1 17-J06
P1-23 IBREQN 19-J06
P1-17 IREQN 21-J06
P1-04 IBACKN 23-J06
P1-13 IRDYN 25-J06

P2-10 LOCKN 03-J07
P3-22 MPGM0 05-J07
P3-16 MPGM1 07-J07
P2-15 OPT0 09-J07
P2-17 OPT1 11-J07
P3-02 OPT2 13-J07
P1-14 PENN 15-J07
P2-02 PIAN 17-J07
P2-19 SUP/USN 19-J07

74F08 U1
1, 2 → 3 DIN → 21-J07

PIN 7 CONNECTED TO GND
PIN 14 CONNECTED TO VCC (+5V)

CH90 01-P04
CH92 03-P04
CH94 05-P04
CH93 04-P04
CH91 02-P04

+5V
.01UF C1
47UF C2
GND

P04-23
P04-24
P04-25
P04-26
P2-05
P1-40
P3-50
P2-07
P1-08
P1-26
P3-06
GND

+5V
P04-21
P04-22

P04-19
P04-20
-5V

CONN. J1-J14: ALL EVEN PINS ARE CONNECTED TO GND

Figure 6-10. 29000 MAP Scrambler Board Schematic Diagram (Sheet 1 of 1)

GOULD DESIGN & TEST

TITLE: 29000 SCRAMBLER BD. SCHEMATIC

MODEL	PART NUMBER	REV
CLASS 4000	0192-0436	50

SHEET 1 OF 1

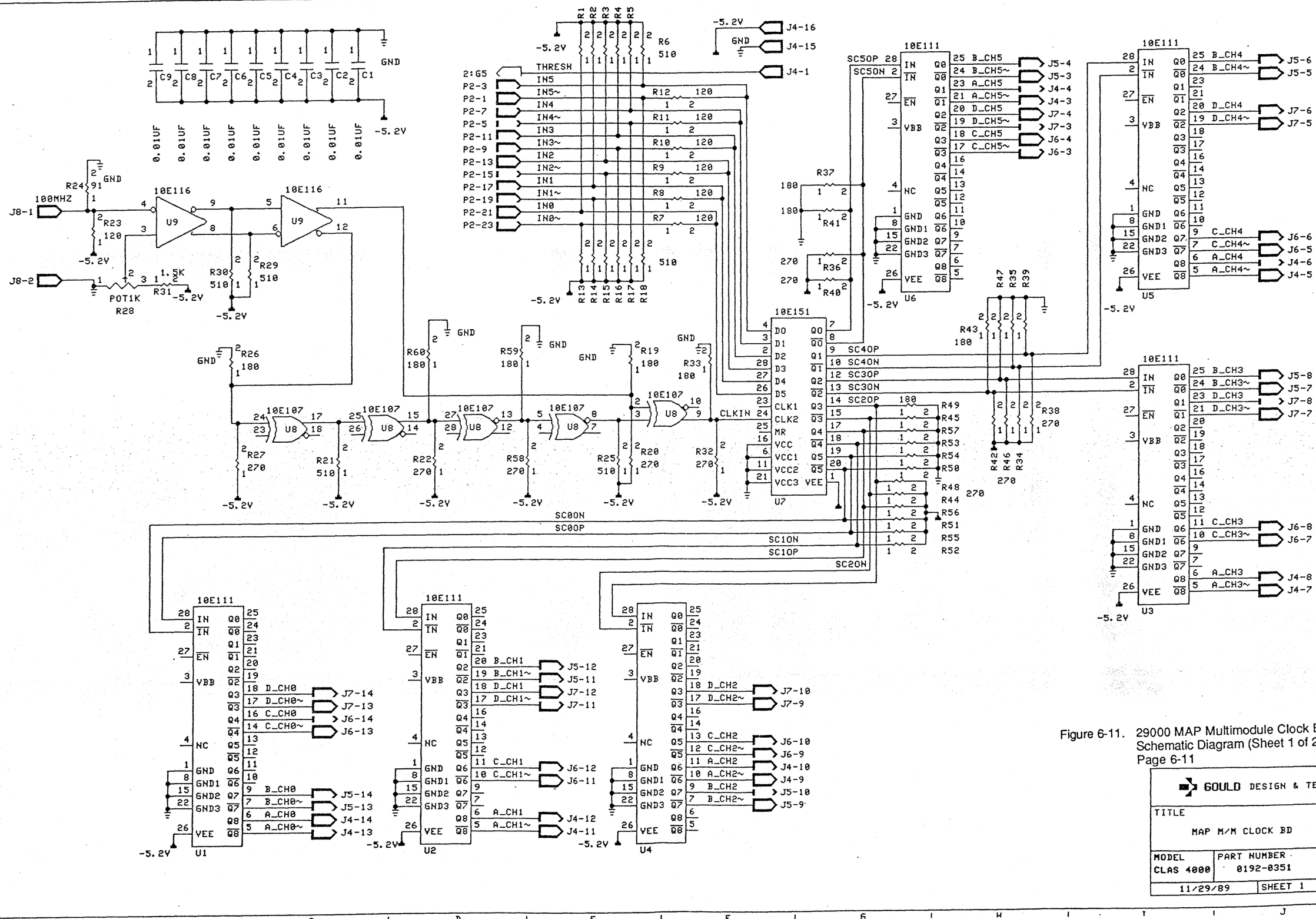
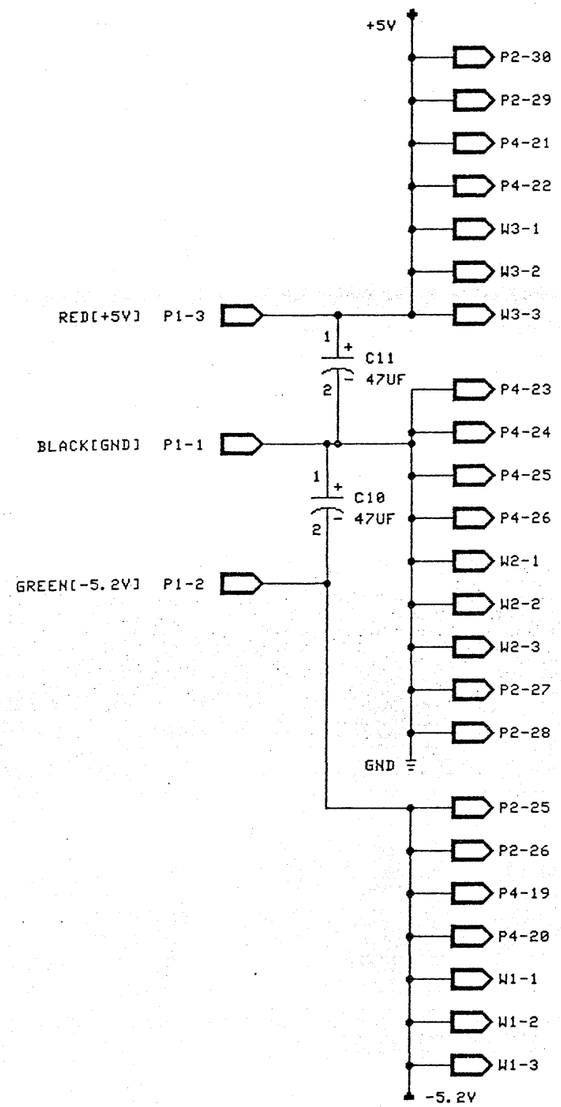
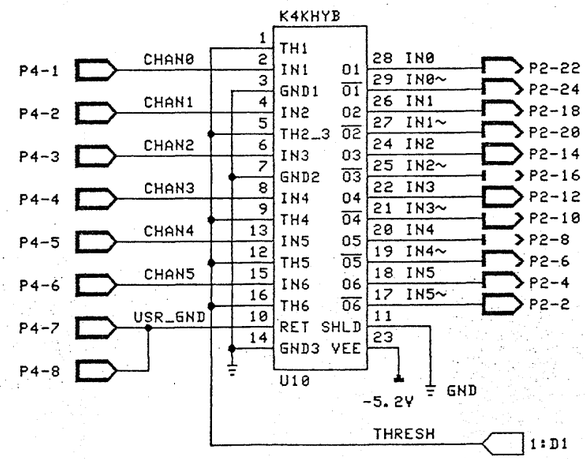


Figure 6-11. 29000 MAP Multimodule Clock Board Schematic Diagram (Sheet 1 of 2)
Page 6-11

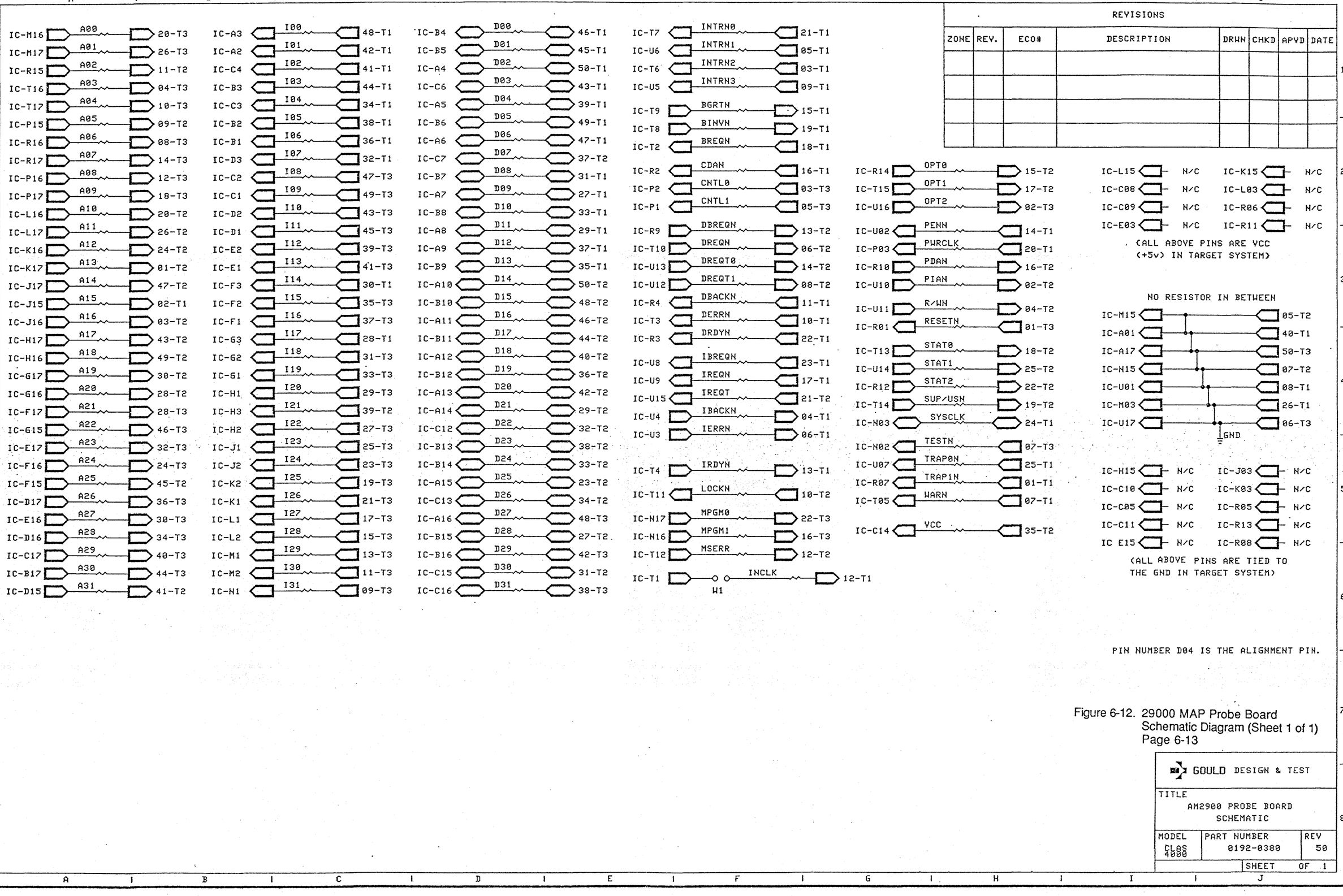
GOULD DESIGN & TEST		
TITLE: MAP M/M CLOCK BD		
MODEL: CLAS 4000	PART NUMBER: 0192-0351	REV: 50
11/29/89	SHEET 1 OF 2	





29000 MAP Multimodule Clock Board
Schematic Diagram (Sheet 2 of 2)
Page 6-12

GOULD DESIGN & TEST		
MODEL	DWG. NO.	REV
CLAS 4000	0192-0351-10	50
	SHEET 2 OF 2	



REVISIONS							
ZONE	REV.	ECO#	DESCRIPTION	DRWN	CHKD	APVD	DATE

Figure 6-12. 29000 MAP Probe Board Schematic Diagram (Sheet 1 of 1)

GOULD DESIGN & TEST		
TITLE: AM2900 PROBE BOARD SCHEMATIC		
MODEL: CLOS 4000	PART NUMBER: 0192-0380	REV: 50
	SHEET OF 1	

29 JAN 90 10:58 /USER/HUSSEIN/29KPRB 1.DRAW