Digital Equipment Corporation
Maynard, Massachusetts

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decsystem10

Maintenance Manual

# MX10 AND MX10-C MULTIPLEXOR

A-MN-MX10-C-MAN1

decsystem10

# MX10 AND MX10-C MEMORY DATA MULTIPLEXOR MAINTENANCE MANUAL

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## CONTENTS



## ILLUSTRATIONS



## TABLES

# CHAPTER 1
# GENERAL INFORMATION

## 1.1 INTRODUCTION

The MX10 and MX10-C Memory Data Multiplexors, manufactured by Digital Equipment Corporation, are offered as options for use in DECsystem-10 computer systems. Utilization of the MPX allows the use of up to eight peripheral type processors, such as the DF10 or DF10-C Data Channels with the memory system. Appendix A describes the MX10-C modification which allows operation with the DF10-C Data Channel in KI10 systems.

The MPX is normally installed in a Data Channel cabinet, where it occupies two logic panel locations. Figure 1-1 shows the front and back layouts of the MPX. The MPX has no operating controls.

Granting of priorities for Data Channel access to the multiplexor (thereby gaining access to a memory unit) is governed by logic contained within the MPX. Eight ports are provided for MPX control cables. In the event of simultaneous memory access requests, the processor whose control cable is terminated in the port designated P0 enjoys highest priority; the processor associated with P7 has lowest priority of access.

A Data Channel gains access to the MPX by sending a request signal over its MPX control cable. The MPX responds with an acknowledgment signal which enables the processor to gate out address information. Because of the necessity for this signal (required only in PDP-10 systems utilizing a multiplexor), arithmetical central processors such as the KA10 and KI10 cannot be connected to the MPX Bus.

After transmission of the acknowledgment signal over the MPX control line to the Data Channel which has requested access, the MPX is transparent to the Data Channel and the address information is transmitted directly to the memory unit over the MPX bus and the memory bus.

The MPX logic contains a BUSY flag which precludes sampling of request signals while it is set, thereby locking out any further requests while the MPX is being controlled by a specific Data Channel. Other requests received simultaneously with the request associated with the port that has been granted access, remain true on the lines and are sampled for priority at the completion of the memory cycle in progress, when BUSY will be reset.

Detailed functional descriptions of the logic contained within the MPX are presented in Chapter 4.

## 1.2 SPECIFICATIONS

Power Requirements
  +10 V and -15 V*
Power Consumption
  85 W
Number of Ports
  8
Size
  Height 10-7/16 in.
  Depth 7-1/4 in.
  Width 19-1/8 in.
Delay
  20 ns
Temperature
  15.6° to 37.8° C
Humidity
  20% to 80%

*The MPX power is supplied by an associated power supply (728 or 728A), which must be installed with the MPX.

## 1.3 REFERENCE MATERIAL

The documents listed in this section contain information essential to an understanding of the DECsystem-10 and which, in some instances, supplements the material contained in this manual. These documents are available from Digital Equipment Corporation, 146 Main Street, Maynard, Massachusetts 01754 or from the nearest DEC District Office.

KA10 Central Processor Maintenance Manual
KI10 Central Processor Maintenance Manual
DECsystem-10 Interface Manual
DECsystem-10 System Reference Manual
MA10 – Core Memory Maintenance Manual
MD10 – Core Memory Maintenance Manual
ME10 – Core Memory Maintenance Manual
MF10 – Core Memory Maintenance Manual
DF10-C – Data Channel Maintenance Manual

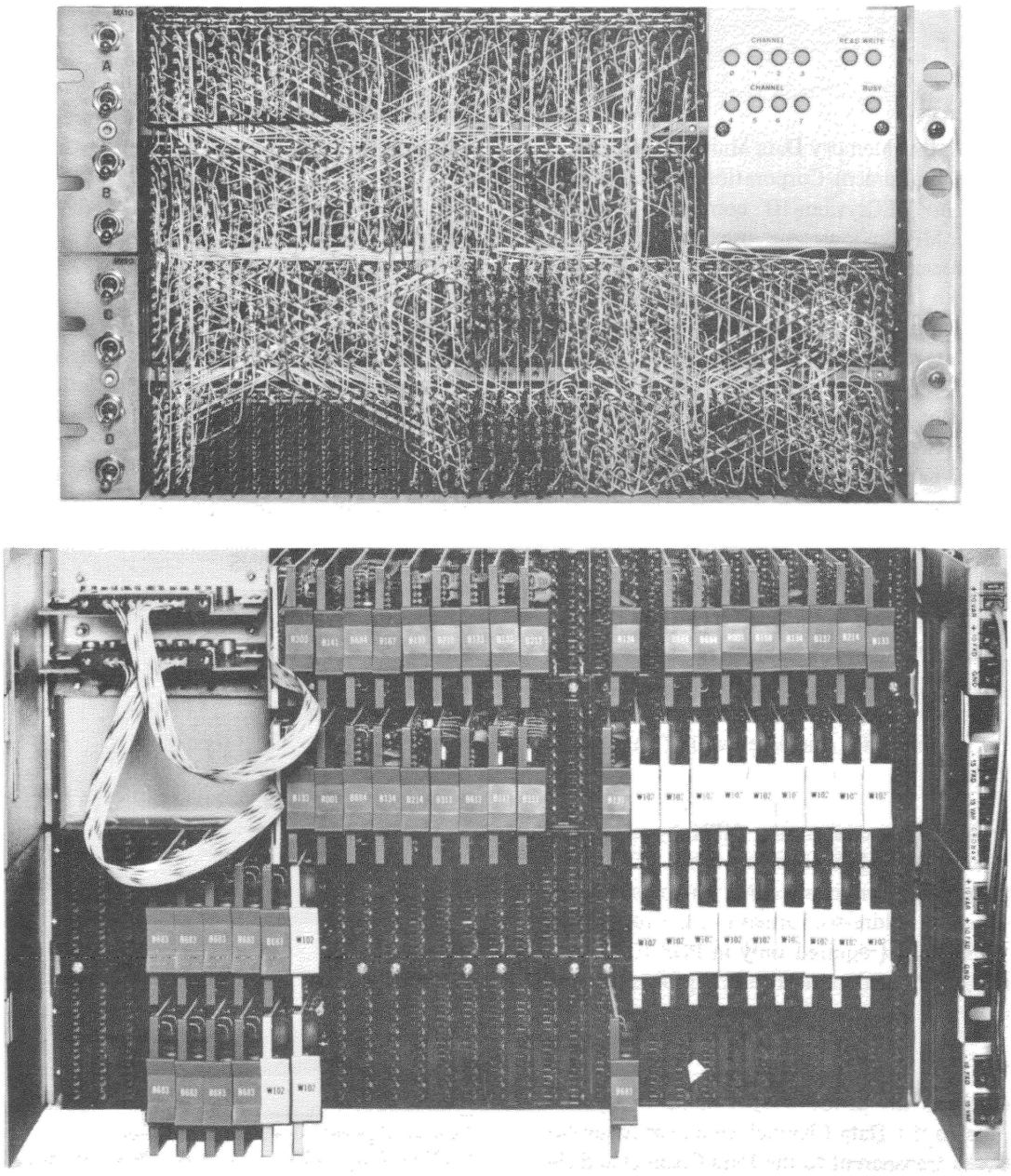

Figure 1-1 MPX Front and Rear Views

# CHAPTER 2
# INSTALLATION

The MPX is normally installed in place of the lower two blank panels in the Data Channel cabinet. Since the MPX is installed in the Data Channel cabinet, all installation requirements pertaining to site selection, environment, etc., are dictated by the Data Channel and are in the *DECsystem-10 Site Preparation Guide,* DEC-10-SITE-D.

## 2.1 INTERCONNECTIONS

Interconnection between the MPX and Data Channels is accomplished by the MPX bus. This consists of two coaxial cable sets identical to the memory bus and a set of multiplexor control cables, one to each Data Channel, which carry the Request and Clear signals from a Data Channel to the MPX and the acknowledge signals in return. The MPX bus, like the memory bus, must be wired through each peripheral processor. Within each Data Channel, from incoming to outgoing connector, through sources and loads, twisted-pair wiring must be used. Each MPX control cable connects between a particular peripheral processor and the multiplexor and must terminate in 100Ω ±10% resistance at both ends.

The maximum length of the MPX bus is nominally 100 feet, which includes the lengths of wire run through each memory and processor and a 30-ns delay (20 ft) through the MPX. Actual length of the bus is dependent upon the location of the MPX in the system with respect to the memory unit and MPX bus. For additional information, refer to Chapter 7 of the *DECsystem-10 Site Preparation Guide,* DEC-10-SITE-D. Figure 2-1 is a block diagram of a hypothetical memory bus arrangement.

Pin assignments for the MPX control cable are shown in Figure 2-2. Figure 2-3 shows interconnections in a hypothetical system.

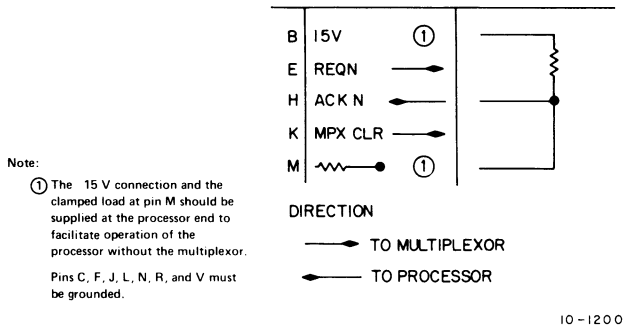


Figure 2-2 Pin Assignments

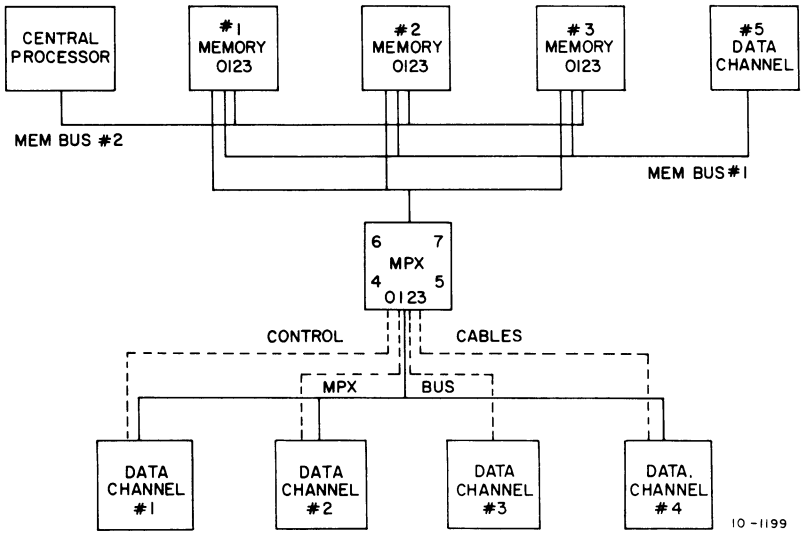


Figure 2-1 Hypothetical Memory Bus Arrangement

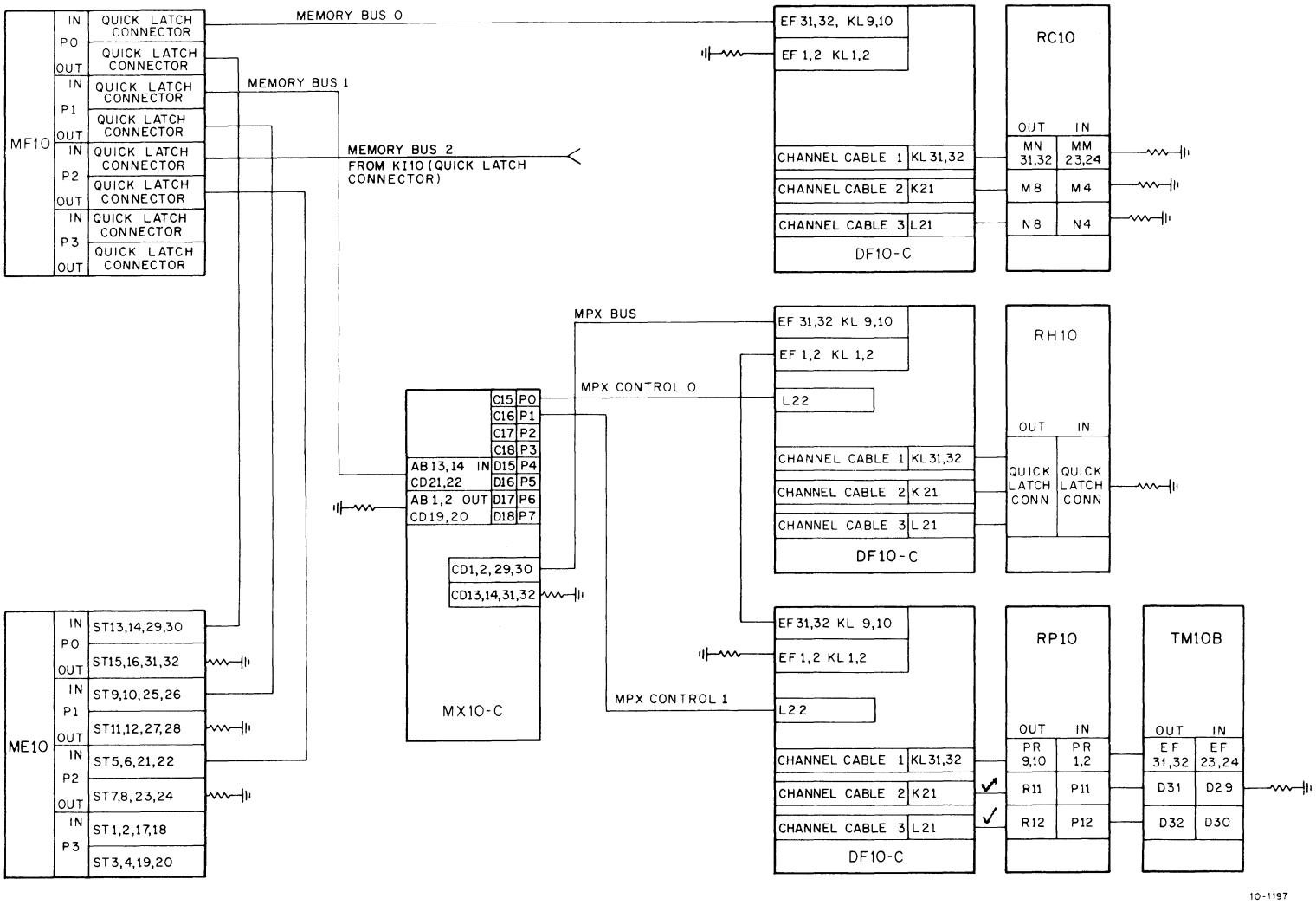


Figure 2-3 System Interconnections

# CHAPTER 3
# OPERATION

Operation of the MPX is completely dependent upon the Data Channel in which it is installed; the MPX has no controls of its own. Input power is provided to the MPX power supply when the associated Data Channel is energized.

## 3.1 INDICATOR PANEL

Several indicator lamps are provided. The indicator panel is shown in Figure 1-1. These indicators in normal operation change status too rapidly to be meaningful but are useful as maintenance aids. The following describes the meaning of a lamp when lit:

| Indicator | Meaning |
|---|---|
| Channel 0 through 7 | Indicates that the Data Channel associated with an MPX port, 0 through 7, has requested control of the MPX and that one or more of the CHN storage flip-flops are set. |
| READ | Indicates that the MPX is in the READ mode and that RDWR1 and RDWR2 are in their 0 states. |
| WRITE | Indicates that the MPX is in the WRITE mode and that RDWR1 and RDWR2 are in their 1 states. |
| BUSY | Indicates that a memory cycle is in progress. This lamp is lighted by BUSY DY (1) and extinguished by FIN DY. |

# CHAPTER 4
# PRINCIPLES OF OPERATION

This chapter describes the operations which take place within the MPX logic during Power Up, Request, Read, Write, and Read-Modify-Write conditions. Reference is made to the noun titles of the Engineering Drawings contained in the MPX Customer Print Set. Locations given refer to the Engineering Drawings and not to MPX logic panels.

## 4.1 POWER-ON CONDITION

This discussion refers to Sheet 2 of the Control drawings. The delay associated with the R303 One-Shot at location 7B is adjusted so that it exceeds the time required for the +10 V and -15 V potentials to reach 90 percent of their final values at power turn-on; this condition causes the multivibrator to go initially to its 1 state. Upon expiration of the 1 second delay, the positive-going transition of the output level is applied to the input of a B611 Pulse Amplifier whose output is inverted through a B611 NAND gate. This positive pulse, designated CLEAR, is applied to another B611 Power Amplifier at location 4D where the FIN pulse is generated, and, after further amplification and a 65 ns delay associated with the B311 also at location 4D, positive and negative FIN DY pulses are developed. In location 3D, the positive assertion of FIN DY resets BUSY (the B212 in location 3D) whose 0 state also causes the B212 at location 2D (BUSY DY) to be cleared.

Generation of these pulses causes the MPX to be placed in a ready condition wherein it can respond to memory access requests from a processor. The BUSY flag has been cleared indicating that a memory cycle is not in progress, while FIN DY, the same pulse that caused clearing of BUSY, also direct-sets the B212 flip-flops, RDWR1 and RDWR2 (location 3-4B). The RDWR1(1) and RDWR2(1) levels are the qualifying conditions for enabling the gates associated with the data transceivers (Sheet 1 of the Data Transceiver drawings) which will allow transfers of data from the multiplexor bus to the memory bus.

FIN, which was generated 65 ns before FIN DY (referring to Sheet 1 of the Control drawings), causes each of the eight B214 Request Storage flip-flops, in locations 2B–7B, to be direct-cleared.

## 4.2 REQUEST OPERATIONS

A processor requests access to the memory system when it places a negative level on its REQ control line.

The REQ N level or levels, if more than one processor is simultaneously requesting access, are NANDed in eight identical B133 gates in the Control logic (Sheet 1, locations 2B to 8B) where, at each gate BUSY (0), the remaining level required for enabling becomes true during the Power-On phase. The positive levels of the enabled gates will collector-set the associated B214 flip-flops (CHN0 through CHN7). It is therefore possible to load more than one of the eight CHN request storage flip-flops during the time BUSY (0). BUSY is set through its delayed-set input by any REQ N ANDed with BUSY (0) at the B133 and B141 gates (located at 3C of Sheet 2 of the Control drawing). Because of this, the MPX logic must assign priorities to each of the eight access ports to preclude more than one processor from simultaneously gaining access to memory. Priorities are assigned in descending order from 0 to 7, where the processor associated with port 0 enjoys highest priority.

Across the top of Sheet 1 of the Control drawing are eight bus drivers, each with its associated gated input circuitry. Negative assertion of the PRCRBR level from the processor must be present at each R001 gate to allow an output from any of the bus drivers. ACK N levels will therefore not be placed on the MPX lines while the processor is in an abnormal power condition. The following assumes that PRCRBR is negatively asserted.

The only condition for the generation of ACK 0 is CHN 0 (1) and BUSY DY (1) asserted at the B134 AND gate at location 7D. BUSY DY (1) is set by BUSY DY (0) which is ANDed with BUSY (1) in a B133 gate (at location 1D of Sheet 2 of the Control drawing).

If CHN 1 (1) is true simultaneously with the CHN 0 (1) condition, an examination of the input gating associated with the generation of ACK 1 (the B134 and B167 gates at 7C of Sheet 1 of the Control drawing) shows that a condition for enabling the B167 AND gate is CHN 0 (0); ACK 1 can never be generated if CHN 0 (1) is true. First priority has been assigned by the logic to the processor associated with P0. Each of the remaining six gates are disqualified by assertion of a CHN (1) of lower designation in the same manner that generation of ACK 1 was inhibited by the assertion of CHN 0 (1). In one instance, a HI ACK level is generated in a B137 AND gate at 4C. This level, dependent upon the CHN 0 through 3 (0) condition, is an enabling requirement for generation of ACK 4 through ACK 7.

### 4.3 MEMORY READ CYCLE

The ACK level associated with the processor having control is placed on the appropriate MPX control line. The Data Channel responds with an REQX CYC signal and the memory address word, including the type of request (i.e., Read, Write, or Read-Modify-Write), over the MPX bus which terminates in the B683 Bus Drivers (as illustrated on the Bus Drivers and Control drawing). These levels exit the bus drivers over the memory bus to the memory system, where a particular memory unit will be selected.

When a memory unit has allowed access, it brings up an ADDR ACK pulse on an MAI line which is applied to a W102 Bus Driver (at location 2B of the Bus Drivers and Control drawing). This pulse exits the bus driver over the multiplexor bus to the Data Channel as ADDRACKX for KA10 systems and as – FMC SELECT/ADDRACK (T) for KI10 systems.

This is to be a Read operation; therefore, MCRD is asserted and ANDed with ADDRACK (at a B133 gate at location 5B of Sheet 2 of the Control drawing) which resets the RDWR1 and RDWR2 flip-flops.

The memory simultaneously asserts RDRS, through a bus driver (location B2 of the Bus Drivers and Control logic), and places the data from the addressed memory location (36 bits) on the memory bus. RDRSX at this time also clears CHN 0 through 7 in the same manner as the assertion of FIN during Power-On.

Because RDWR1 and RDWR2 are both in the 0 state (refer to the Data Transceiver drawing), one condition required for enabling the input gate associated with each W102 Bus Driver has been fulfilled. The remaining condition is the state (0 or 1) of each bit in the addressed memory location as it is strobed into the memory buffer. All 1s placed on the memory bus enable the gates and bring up the MPX lines associated with the bit. In this manner the selected data is read into the Data Channel over the MPX bus.

This completes the memory cycle for the MPX and the Data Channel, although additional operations are necessary within the addressed memory unit before it is again ready for access. The MPX must now prepare to receive and process the next request to be made.

On the Control drawing (Sheet 2, location 6C), assertion of RDRS causes generation of RDRS DY after completion of the 90 ns delay associated with the B311 Delay Line. RDRS DY ANDed with WR BUF (0) (true when ADDRACK and ~MCWR are asserted) produces CLEAR which, in turn, sets up the MPX for the next cycle request in the same manner as described in Paragraph 4.1.

### 4.4 MEMORY WRITE OPERATION

Prior to commencement of the Write operation, the MPX must be in the ready condition as at the termination of Read or Power-Up. Selection of a DF10 through the priority logic takes place as described in Paragraph 4.2.

The memory address word is accompanied by a WRITE RQ level (MXCWR on the MPX bus and MCWR on the memory bus). This level is transmitted through a B683 Bus Driver at location 6C of the Bus Drivers and Control drawing. MCWR causes generation of ~MCWR at a B133 gate shown on Sheet 2 of the Control drawing where, in location 6B, ~MCWR causes the WR BUF (1) condition. The address acknowledge signal ANDed with MCWR in the control logic produces ACK CLR following a 65 ns delay as shown on the Control drawing (Sheet 2, location 4D). Pulse ACK CLR clears CHN 0 through CHN 7 (Sheet 1).

RDWR1 and RDWR2 were set by FIN DY 65 ns after the last clear. This is the condition required in the data transceiver (Sheet 1) for transfer of data from the MPX bus to the memory bus.

At generation of ADDRACK, a memory unit has been selected, has acknowledged the receipt of a legal address, and is awaiting data and a Write Restart (WRRS) pulse.

The Data Channel, upon receipt of ADDRACK, generates WRRS and simultaneously places the data to be written on the MPX bus where it is transmitted through the bus drivers, onto the memory bus, and into the memory unit's buffer.

Assertion of WRRS, after a 65 ns delay, generates WRRS DY and CLEAR in the control logic; once again readying the MPX for the next memory cycle.

### 4.5 READ-MODIFY-WRITE

Operation during the Read-Modify-Write cycle is similar to that for a Read or Write except that the CLEAR pulse is inhibited following the read portion of the cycle, thereby preventing the MPX from disconnecting, and clearing the BUSY flag.

Because both MCRD and MCWR are asserted for the Read-Modify-Write cycle, WR BUF (1) is generated by ADDRACK which clears RDWR1 and RDWR2 (MCRD being true). The read portion of the cycle progresses as before, because of the states of RDWR1 and RDWR2. CLEAR is not generated by RDRS DY at the completion of the Read cycle because of the WR BUF (0) inhibiting level at the B311 gate (located at 5C of Sheet 2 of the Control drawing). RDRS DY sets RDWR1 and RDWR2 to the WRITE states. The MPX therefore remains connected until a WRRS is asserted by the Data Channel and data is placed on the MPX bus for writing as in a normal Write cycle. The cycle then continues as described in Paragraph 4.4.

### 4.6 NONEXISTENT MEMORY OPERATION

When a nonexistent memory situation is detected by the processor, the processor places a clear signal CLR 0–7 on the MPX control cable with which it is associated. These pulses are ORed together in the control logic and cause generation of CLEAR within the logic, causing the disconnection of the MPX from the processor and a return to the ready condition.

# CHAPTER 5
# MAINTENANCE

General preventive and corrective maintenance procedures for the MX10 are contained in Chapter 5 of the DF10 and DF10-C Data Channel maintenance manuals. Specific test procedures are completely dependent upon and integrated with those for the Data Channel.

## 5.1 TEST PROCEDURE (DISK)

The following equipment configuration is required for accomplishment of the Disk Test procedure:

| | |
|---|---|
| DF10 or DF10-C | Data Channel |
| MX10 or MX10-C | Multiplexor (installed in Data Channel cabinet) |
| RC10 | Synchronizer |
| RD10 | Disk |

With the MPX installed in the above configuration, accomplishment of the Disk System Acceptance Test Procedure and Specifications, drawing A-SP-RC10-0-9, will constitute the acceptance test for the MX10 and MX10-C.

## 5.2 TEST PROCEDURE (OFF-LINE)

Accomplishment of this test procedure requires that the MX10 or MX10-C be installed within the DF10 or DF10-C cabinet, respectively, with the MPX bus and control cables connected. The DF10 (off-line) test, drawing DF10-0-7, will be run with the following additional steps.

1. Remove the W990 module from location L22 of the DF10.
2. Connect the MPX control cable to port 0 of the MPX.
3. During step A, 2 of the DF10 Off-Line Control Test, verify that RDRS delay time (defined as RDRS to FIN) is within the limits of 85 ns ± 6 ns and that the FIN delay time (defined as FIN to FIN DY) is within the limits of 76 ns ± 5 ns.
4. Sync (-) on REQ 0 and verify that BUSY, CHN 0, and ACK 0 go true at this time. Also, verify that FIN DY clears BUSY.
5. Relocate the MPX control cable to port 1 and repeat step 4 above. Continue to shift the control cable and repeat step 4 until all ports have been checked.
6. During accomplishment of steps 2 and 4 of the DF10 Data Test, the total cycle time will be increased by two multiplexor delays or 40 ns.
7. Also during step 4 of the DF10 Data Test, with WRITE on a 1, verify the WRRS delay time (defined as WRRS to FIN) which should be within the limits of 85 ns ± 6 ns.
8. During step A, 5 of the DF10 Termination Test, with NO MEM on a 1, verify that CLRN clears BUSY. This procedure should be repeated for the remaining seven ports.

## 5.3 MARGIN TESTS

The frequency of voltage margin testing is dependent upon conditions at the site; monthly testing is suggested. These tests are accomplished while the Diagnostic Program, 5CA FLOAT, is in progress. Table 5-1 lists the voltage margin specifications. The figures in parentheses, shown for Panels A and B under +10 V Low, are because of the B684 Bus Drivers and will be true for Panel A when ports 0, 1, 4, 5, 6, or 7 are used, and for Panel B when ports 2 or 3 are used.

**Table 5-1**
**Voltage Margin Specifications**

| | +10 V | | -15 V | |
|---|---|---|---|---|
| **Mounting Panel** | **Low** | **High** | **Low** | **High** |
| A | 2.5 (5.5) | 17.5 | -18 | -12 |
| B | 2.5 (5.5) | 17.5 | -18 | -12 |
| C | 2.5 | 17.5 | -18 | -12 |
| D | 2.5 | 17.5 | -18 | -12 |

# CHAPTER 6
# SPARE PARTS

## 6.1 GENERAL

Table 6-1 contains a listing of the modules, semiconductor devices, and lamps used in the MX10 and MX10-C with suggested quantities of each type to be stocked by the user at his site.

**Table 6-1**
**Spare Parts**

| DEC Type Number | Description | Recommended Spare Quantity |
|---|---|---|
| | MODULES | |
| B133 | Diode Gate | 1 |
| B134 | Diode Gate | 1 |
| B137 | Diode Gate | 1 |
| B141 | Diode Gate | 1 |
| B167 | Adder Gate | 1 |
| B168 | Diode Gate | 1 |
| B212 | Flip-Flop | 1 |
| B214 | Quadruple Flip-Flop | 1 |
| B311 | Delay Line | 1 |
| B611 | Pulse Amplifier | 1 |
| B683 | Bus Driver | 2 |
| B684 | Bus Driver | 1 |
| R001 | Diode Network | 1 |
| R303 | Integrating One-Shot | 1 |
| W102 | Bus Driver | 1 |
| W990 | Jumper Board | 1* |

**Table 6-1 (Cont)**
**Spare Parts**

| DEC Type Number | Description | Recommended Spare Quantity |
|---|---|---|
| | TRANSISTORS | |
| 15-03099 | DEC 2894-3B-S | 4 |
| 15-01742 | 2N2904 | 4 |
| 15-03100 | DEC 3009B-S | 2 |
| 15-02151 | 2N3605 | 2 |
| 15-02762-02 | DEC 3639-D | 2 |
| 15-05321 | 2N4258 | 4 |
| | DIODES | |
| 11-00113 | D662 | 10 |
| 11-00114 | D664 | 10 |
| 11-02161 | D668 | 6 |
| | MISCELLANEOUS | |
| 12-02116 | Indicator Lamps | 10 |

* MX10-C Version only.

# APPENDIX A
# GLOSSARY
# MNEMONICS–LEVELS–PULSES

## A.1 GENERAL

The following is a listing of the more significant MX10 mnemonic signals with brief descriptions of the function of each. A listing of the KA10 Memory Bus Control signals and the corresponding KI10 Memory Bus Control signals is in Table B-1. Those signals which differ between the two systems are appended by an asterisk in this glossary.

| | |
|---|---|
| ACK 0–7<br>(Acknowledge) | This level is placed on an MPX Control Line by the MX10 to signify to the Data Channel associated with that line that it has been granted access to the MX10. |
| ADDRACK<br>(Address Acknowledge) | In KA10 systems only, this pulse is developed in a memory unit and transmitted to the MX10 over the memory bus to signify that the memory address has been valid and that the memory unit is commencing its cycle. |
| ADDRACKX<br>(Address Acknowledge MPX Bus) | In KA10 systems only, this pulse is generated in the Bus Drivers and Control logic by ADDRACK and transmitted to the Data Channel being serviced, over the MPX bus, to signify that the selected Data Channel has gained access to the memory unit and that the memory cycle is in progress. |
| BUSY | This flip-flop, located in the Control logic, when set, designates the MX10 BUSY state and, when cleared, designates the completion of a memory cycle. |
| BUSY DY<br>(Busy Delayed) | This flip-flop, located in the Control logic, when set, fulfills one requirement for generation of an ACK level, thereby granting MX10 access to a requesting Data Channel. |
| CHN 0–7 (1)<br>(Channel) | These levels are generated by setting the associated flip-flops CHN 0–7 located in the Control logic, and are tested in the priority selection network to determine which Data Channel will be granted access. Each flip-flop is set by a Data Channel requesting access while BUSY (0) is true. |
| CLR 0–7<br>(Clear) | A pulse generated in the selected Data Channel when a non-existent memory situation is detected. |
| FIN<br>(Finish) | This pulse is generated in the Control logic by CLEAR and initiates the operations which place the MX10 in the ready condition. |

FIN DY
(Finish Delayed)

This pulse is derived from FIN (delayed 65 ns) and clears BUSY, signifying the completion of a memory cycle.

HIACK
(High Acknowledge)

This level is generated in the priority selection network of the Control logic and is an enabling condition for generation of ACK 4–7.

IGN PAR PULSE*
(Ignore Parity Pulse)

This pulse is generated in a memory unit which does not have provisions for storing a parity bit and is transmitted to the MX10 over the memory bus.

IGNX PARITY PULSE
(Ignore Parity Pulse MPX Bus)

This pulse is generated in the Bus Drivers and Control logic when IGN PARITY PULSE is asserted. Transmitted to the selected Data Channel over the MPX bus, it causes the Data Channel INOR PAR indicator lamp to light and disables the parity checking network.

MCRD
(Memory Cable READ)

This is the READ request level, developed in the Bus Drivers and Control logic from MCXRD. MCRD is transmitted to the memory unit over the memory bus.

MCWR
(Memory Cable WRITE)

This is the WRITE request level, developed in the Bus Drivers and Control logic from MCXWR. MCWR is transmitted to the memory unit over the memory bus.

MCXRD
(Memory Cable MPX READ)

This is the READ request level developed in the selected Data Channel and transmitted to the MX10 over the MPX bus.

MCXWR
(Memory Cable MPX WRITE)

This is the WRITE request level developed in the selected Data Channel and transmitted to the MX10 over the MPX bus.

RDRS
(READ-Restart)

This pulse is generated in the memory unit and placed on the memory bus simultaneously with the data word read from core.

RDRS DY
(READ-Restart Delayed)

This pulse is derived from RDRS and delayed 65 ns in the Control logic. RDRS DY causes RDWR1 and RDWR2 to be set to their 1 states thereby allowing MPX bus to memory bus data transfers.

RDRSX
(READ-Restart MPX Bus)

This is the pulse, triggered by RDRS, generated in the Bus Drivers and Control logic, that is transmitted to the selected Data Channel over the MPX bus simultaneously with the data word read from core.

RDWR1 and RDWR2
(READ – WRITE)

These flip-flops are located in the Control logic. When in their 1 states, they allow MPX bus to memory bus data transfers, and, when in their 0 states, allow memory bus to MPX bus data transfers.

REQ 0–7
(Request)

Each Data Channel requesting MX10 access places its associated REQ level on its REQ MPX Control Line.

REQ CYC*
(Request Cycle)

This is the level, triggered by REQX CYC in the Bus Drivers and Control logic, which is placed on the memory bus simultaneously with the memory address word and which remains true until ADDRACK is generated by the memory unit.

REQX CYC
(Request Cycle MPX Bus)

This is the level generated in the selected Data Channel after reception of the appropriate ACK level from the MX10. REQX CYC is placed on the MPX bus simultaneously with the memory address word.

WR BUF (0)
(WRITE Buffer)

This level is ANDed with RDRS DY in the Control logic to generate CLEAR at the completion of a memory Read cycle and, when false during a Read-Modify-Write cycle, prevents MX10 termination at the completion of memory READ.

WR BUF (1)
(WRITE Buffer)

This level is ANDed with WRRS DY in the Control logic to generate CLEAR at the completion of a memory Write cycle.

WRRS
(WRITE-Restart)

This is the pulse triggered by WRRSX in the Bus Drivers and Control logic which is transmitted to the selected memory unit over the memory bus simultaneously with the data word to be written into core.

WRRS DY
(WRITE-Restart Delayed)

This is the pulse derived from WRRS and delayed 65 ns which, when ANDed with WR BUF (1) in the Control logic, causes generation of CLEAR.

WRRSX
(WRITE-Restart MPX Bus)

This is the pulse generated in the selected Data Channel which is placed on the MPX bus simultaneously with the data word to be written into core.

# APPENDIX B
# MX10–C MODIFICATION

## B.1 GENERAL

In systems where the KI10 Central Processor is used, 22 memory addressing bits are required. The MX10 was designed to operate with the KA10 Central Processor where 18 memory address bits are used. The modification to the MX10 which allows operation with the KI10, converts signals once used for memory addressing to control signals required by the KI10 memory bus. Table B-1 lists the KA10 and corresponding KI10 memory bus addressing and control signals.

Once the modification is completed, the MX10 is designated MX10-C and is capable of addressing 4192K of memory, through the DF10-C Data Channel.

The entire modification consists of installing a properly configured W990 jumper board in slots D04 and D10 and accomplishing the associated backplane wiring (Drawing D-BS-MX10-0-3). The MX10-C can be changed back to an MX10 by simply rearranging the jumpers on the W990.

Normally, reverting to the MX10 configuration would not be required; however, this feature is provided to give monitor and maintenance personnel a capability for using 18-bit address software.

The DF10-C Data Channel is equipped with a switch that allows operation in either the 18-bit (KA10) or 22-bit (KI10) addressing modes.

Table B-1
Memory Bus Control Signals

| Cable | Pin | KA10 Signal | KI10 Signal |
|---|---|---|---|
| A1 | D | ADR ACK | ADDR ACK (NT) |
| | E | RDRS | RDRS |
| | H | WRRS | WRRS |
| | K | PARITY | PAR PULSE |
| | M | REQ CYC | RQ CYC IMM |
| | P | MADR 22 (0) | RQ CYC FAST |
| | S | MADR 18 (0) | RQ CYC SLOW |
| | T | MADR 18 (1) | MADR 18 (1) |
| A1 | V | MADR 19 (0) | DATA WARNING |
| A2 | D | MADR 22 (1) | MADR 22 (1) |
| | E | MADR 23 (1) | MADR 23 (1) |
| | H | MADR 24 (1) | MADR 24 (1) |
| | K | MADR 25 (1) | MADR 25 (1) |
| | M | MADR 26 (1) | MADR 26 (1) |
| | P | MADR 27 (1) | MADR 27 (1) |
| | S | MADR 28 (1) | MADR 28 (1) |
| | T | MADR 29 (1) | MADR 29 (1) |
| A2 | V | MADR 30 (1) | MADR 30 (1) |
| B1 | D | MADR 19 (1) | MADR 19 (1) |
| | E | MADR 20 (0) | Spare |
| | H | MADR 20 (1) | MADR 20 (1) |
| | K | MADR 21 (0) | SEQ RQ |
| | M | MADR 21 (1) A | MADR 14 (1) |
| | P | MADR 35 (0) | MADR 15 (1) |
| | S | MADR 35 (1) A | MADR 16 (1) |
| | T | FMC SELECT + | MADR 17 (1) |
| B1 | V | FMC SELECT - | ADDR ACK (T) |
| B2 | D | MADR 31 (1) | MADR 31 (1) |
| | E | MADR 32 (1) | MADR 32 (1) |
| | H | MADR 33 (1) | MADR 33 (1) |
| | K | MADR 34 (1) | MADR 34 (1) |
| | M | MADR 35 (1) B | MADR 35 (1) |
| | P | RDRQ | RDRQ |
| | S | WRRQ | WRRQ |
| | T | IGN PARITY | IGN PAR PULSE |
| B2 | V | MADR 21 (1) B | MADR 21 (1) |

MX10 and MX10-C
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Maintenance Manual
A-MN-MX10-C-MAN1

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