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Maynard, Massachusetts

digital

PDP-9
Maintenance Manual

TCO2

Dectape Control

DEC-09-I3CA-D

TCO2
DECTAPE CONTROL
MAINTENANCE MANUAL

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CHAPTER 1
INTRODUCTION AND DESCRIPTION

The Type TC02 DECtape Control, manufactured by Digital Equipment Corporation, is a synchronizing and controlling unit used for transfer of information between Programmed Data Processor PDP-9* and the TU55 DECtape Transport.

The DECtape system, consisting of the TC02 control and up to eight TU55 transports, is a magnetic tape storage facility that stores information at fixed positions on magnetic tape, as in magnetic disc or drum storage devices; rather than at unknown or variable positions, as in conventional magnetic tape systems. This feature allows the replacement of blocks of data on tape in an ordered fashion without disturbing previously recorded information. In particular, during the writing of information on tape, the system reads format (mark) and timing information from the tape and uses this information to determine the exact position at which to record the information to be written. Similarly, in reading, the same mark and timing information is used to locate data to be played back from the tape.

A typical system (Figure 1-1) consists of a PDP-9, one TC02, and up to eight TU55 transports (only one transport can be selected at a time).

The levels of discussion in this manual assumes that the reader has previous knowledge of both the PDP-9 processor and the TU55 DECtape Transport. This manual includes references to the supporting documents listed in Table 1-1.

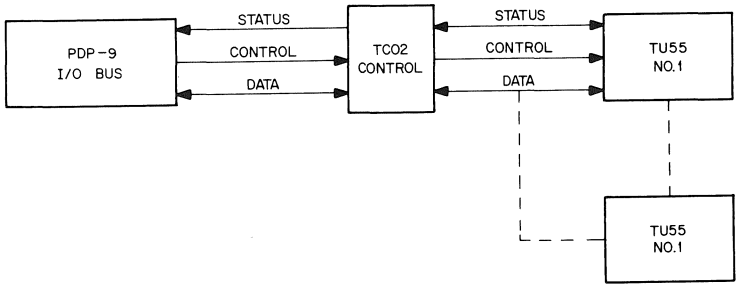


Figure 1-1 System Configuration

1.1 PURPOSE AND SCOPE

This manual describes the DECtape Transport Control TC02, includes maintenance information in a form for easy use and quick reference, and is the major reference covering the TC02 control. Detailed explanations of standard products, such as modules, PDP-9 processor, and TU55 are contained in the standard documents for these products.

*PDP is the registered trade mark for the programmed data processors manufactured by Digital Equipment Corporation, Maynard, Massachusetts.

1.2 EQUIPMENT DESCRIPTION

The TC02 DECtape control logic occupies three Flip-Chip mounting panels. A maintenance control panel (Figure 5-1) occupies the right-hand half of the upper mounting panel. This panel is covered during normal programmed operations.

The TC02 is mounted one mounting panel space up from the bottom of the cabinet, and a maximum of four TU55 transport units can be mounted above the TC02 in the same cabinet. (Additional units must be mounted in another cabinet.)

The standard DEC computer has double doors on front and rear. Power supplies and power controls are mounted inside the rear double doors on a full-width plenum door latched by a spring loaded pin at the top. Module mounting panels are mounted behind the double door in front with the wiring side facing outward. Fans at the bottom of the cabinet provide filtered cooling air. The rear plenum door has blank panels in space not occupied by components. The TC02 and associated DECtape TU55 Transports receive power from the Type 779 Power Supply and the Type 832F Power Control.

1.2.1 Physical Characteristics

Dimensions

TC02 Control:	15-3/4 in. high, 19 in. wide
TU55 Transport:	10-1/2 in. high, 19-1/2 in. wide, 9-3/4 in. deep
Cabinet:	69-1/8 in. high, 22-1/4 in. wide, 27-1/6 in. deep

Weight

TC02:	30 lb
TU55:	65 lb (rack mounted)
Cabinet:	620 lb (with maximum equipment mounted)

Power Requirement

TC02:	115V, 60 cps, 4A. A Type 832F Power Control and a Type 779 Power Supply are included with the TC02 Control (N9M transformer used for 50 cps).
TU55 Transport:	115V ±10%, 60 cps, 2A maximum, 1.5A idle
Cabinet:	115V, 60 cps cource capable of delivering 20A

Tape Characteristics

Reel capacity:	260 ft of 0.75 in., 1 mil thick Mylar tape (empty reel: 2-3/4 in. diameter; loaded reel: 3-3/4 in. diameter)
Density:	350 ± 55 lines per in.
Motion:	Bidirectional
Addressable blocks per reel:	1100_8 (576_{10}) 18-bit words in blocks of 256_{10} words

Word Transfer Rate

One tape line is read or written every 33-1/3 μs.
An 18-bit word is read and assembled or disassembled and written in 200 μs.
In reverse direction, the transfer rate varies by 30% as the effective reel diameter changes.

Addressing

Mark and timing tracks allow searching for a particular block.

Start time:	375 ms approximate
Stop time:	375 ms approximate
Turn around time:	375 ms

Input Signals to Transport from Control

Commands:	FORWARD, REVERSE, GO, STOP, ALL HALT
Unit select:	Select unit 1 through 8
Information:	Analog write signals to the recording head

Output Signal from Transport to Control

Control:	WRITE ENABLE
Information:	Analog read signals from recording head

Environmental Conditions

Thermal Dissipation:	2000W
Operating Temperature:	50° to 90°F ambient
Humidity:	10% - 90% relative humidity*

1.3 SYSTEM DESCRIPTION

The TC02 consists of tape control logic, which under direction of the PDP-9, controls the operation of up to eight TU55 DECtape Transports. The TC02 transfers data between the PDP-9 core memory and the selected tape transport. To transfer data, the TC02 uses the data channel facility of the PDP-9; the WC (word count) register specifies the record length, the CA (current address) register specifies the core memory address of the data transfer.

During both input and output operations, the TC02 receives data and control information from the processor and generates the appropriate signals for the selected transport to execute the programmed commands. Binary information is transferred between the tape transport and the computer as one 18-bit

*Tape manufacturer recommends 60°F - 80°F and 40% - 60% relative humidity for best tape performance.

computer word every 200 μs. In writing the TC02 disassembles the 18-bit computer word into six successive 3-bit words to be written on tape. During reading, the TC02 assembles six successive 3-bit words into an 18-bit computer word. Transfer of an 18-bit word always occurs in parallel. As the start and end of each block are detected, the TC02 generates a DECtape control flag signal (DTCF) to cause a program interrupt in the computer.

The program interrupt is used by the computer program to determine the block number. When it determines that the next block is the one selected for transfer, it selects the read or write control function. Each time a word is assembled, or DECtape is ready to receive a word from the computer, the control produces a data flag (DF) to request a data break. Therefore, when each 18-bit computer word is assembled the data break initiates a transfer. By using the mark-track decoding circuits and the data break facility, the main computer program can continue during tape operation.

1.4 REFERENCED DOCUMENTS

The DEC documents listed in Table 1-1 contain material which supplements the information in this manual. These documents may be obtained from DEC field offices or from the main office in Maynard, Massachusetts.

Table 1-1
DEC Documents

Document No.	Title	Description
C105	Digital Logic Handbook	Specifications and descriptions of the FLIP-CHIP modules.
C100	System Modules	Specifications and descriptions of basic system modules and power supplies.
F95	PDP-9 Users Handbook	Programming and operating information for the computer including brief instructions on TC02 control.
F97	PDP-9 Maintenance Manual	Complete information on the internal operation of PDP-9 logic, memory, basic in/out, and options.
H-TU55	TU55 Maintenance Manual	Transport drive logic and internal operations.

In addition to the documents listed in Table 1-1, a complete set of library programs are available.

CHAPTER 2
OPERATION AND PROGRAMMING

This chapter contains information required for operation and programming of the TC02. Included are a description of the format of information on the DECtape magnetic tape, and the modes of operation used in programming TC02 operations. General operating information for TU55 transport is contained in the TU55 Maintenance Manual.

2.1 DECTAPE SYSTEM

DECtape uses a 10-track read/write head. Tracks are arranged in five nonadjacent redundant channels: a timing channel, a mark channel, and three information channels. Redundant recording of each character bit on nonadjacent tracks materially reduces bit dropout and minimizes the effect of skew. Series connection of corresponding track heads within a channel and the use of Manchester phase recording techniques, rather than amplitude sensing techniques, virtually eliminate dropouts.

The timing and mark channels control the timing of operations within the TC02 control unit and establish the format of data contained on the information channels. The timing and mark channels are recorded prior to all normal data reading and writing on the information channels. The timing of operations performed by the tape drive and some control functions are determined by the information on the timing channel. Therefore, wide variations in the speed of tape motion do not affect system performance. Information read from the mark channel is used during reading and writing data, to indicate the beginning and end of data blocks and to determine the functions performed by the system in each control function.

During normal data reading, the TC02 control assembles 18-bit computer length words from six successive lines read from the information channels of the tape (Figure 2-1). During normal data writing, the control disassembles 18-bit words and distributes the bits so they are recorded on six successive lines on the information channels. A mark channel error check circuit assures that one of the permissible marks is read in every six lines on the tape.

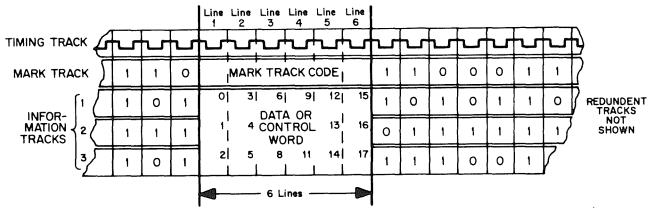


Figure 2-1 Basic Six Line Tape Unit

A tape contains a series of data blocks that can be of any length which is an even number of 18-bit words. Block length is determined by information on the mark channel. Usually a uniform block

length (256_{10} for the PDP-9) is established over the entire length of a reel of tape by a program which writes mark and timing information at specific locations. The ability to write variable-length blocks is useful for certain data formats. For example, small blocks containing index or tag information can be alternated with large blocks of data. The maximum number of blocks addressable is 4096.

Between the blocks of data are areas called interblock zones. The interblock zones consist of 30 lines on tape before and after a block of data. Each of these 30 lines is divided into five 6-line control words.

Block numbers normally occur in sequence from 1 to N. There is one block numbered 0 and one block N + 1. The total length of the tape is equivalent to 849,036 lines which can be divided into any number of blocks up to 4096 by prerecording of the mark track. Normally, 576_{10} blocks of 256_{10} words each are prerecorded for PDP-9 DECtape.

2.2 DECTAPE CONTROL TC02

A maximum of eight TU55 transports can be connected to a TC02. Of the PDP-9 data channels available, DECtape is assigned to channel 0 (core memory locations 30 and 31).

C(30) = Word Count (in 2s complement form)-WC
C(31) = Current Address Register - CA

Data transfers can take place to or from only one transport at a time at a rate of one word every 200 μs (1 block of 256_{10} words every 53 ms), after the desired block has been found. Since the CA is incremented before the data transfer (except in search where the CA is not incremented), the initial contents should be set to the desired initial address minus one. The WC is also incremented before each transfer and must be set to the 2s complement of the desired number of data transfers. In this way, the word transfer which causes the word count overflow is the last transfer to take place.

The number of IOTs (input/output transfer commands) required for the TC02 is minimized by transferring all required control data (unit, function, mode, direction, etc.) from the accumulator (AC) to the control using one set of IOTs, and similarly, transferring all status information (the above plus status bits, error flags, etc.) into the AC from the control by a second set of IOTs.

To provide for automatic parity checking during the READ DATA function, a 6-bit parity check character is computed and recorded by the DECtape control for every block recorded during the Write Data function. The 6-bit parity check character is computed by the complement of the exclusive OR (logical equivalence) of the reverse parity check character and every six bits of every data word.

2.3 DECTAPE FORMAT

The format of the DECtape is shown in Figure 2-2 and provides 10 tracks, 5 tracks redundantly recorded; i.e., three pair of tracks for data and two pair for timing and mark information. A 10-track recording head reads and writes the five duplexed channels.

The prerecorded timing track synchronizes read/write operations. The location of the timing tracks along the edges of the tape permits strobing on the analog sum of the timing track signals

(minimizing tape skew effect) and thus reading the data tracks when they are in the most favorable position. The location of the data tracks in the middle of the tape also minimizes skew effect.

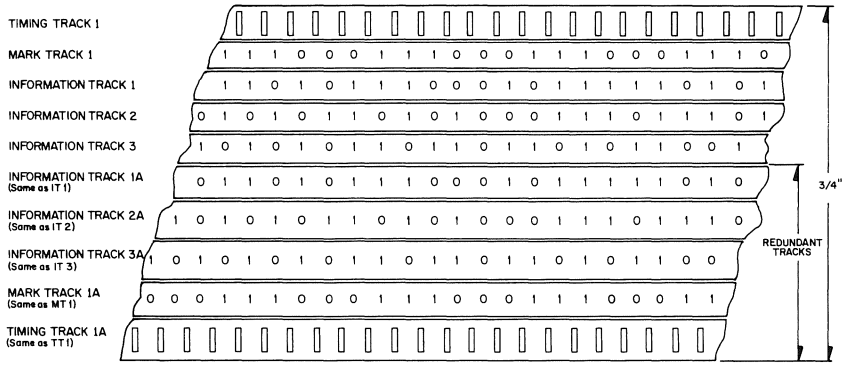


Figure 2-2 Track Allocation Showing Redundantly Paired Tracks

Data is recorded by the Manchester method in which a prerecorded timing track synchronizes read/write operations. When writing on the tape, the write amplifiers supply the maximum current in either one direction or the other (non-return to zero, NRZ). To write a pulse, the polarity of the write current is reversed, and the polarity of the pulse that is produced depends on whether the write current underwent a positive or negative transition. The timing track is prerecorded with alternate positive and negative transitions at fixed time intervals. The negative transition is used only during writing and is a signal to load the write buffer. The positive transition is used during both reading and writing. During writing, this transition is a signal to switch the polarity of the write current in all write heads. If a ZERO is being written, the current, which starts out positive for writing ZEROs, is switched to negative resulting in a negative transition. If a ONE is being written, the current starts out negative and generates a positive transition when switched to positive. During reading, the positive transition of the timing track is a signal to strobe the data and mark track read-amplifier outputs into the read buffer. If a positive transition is sensed at strobe time, a ONE is placed in the buffer; otherwise a ZERO is strobed in.

Because the strobe is a relatively narrow pulse, the system is not affected by noise outside the strobe time. At strobe time, all data signals are negative pulses representing ZEROs or positive pulses representing ONEs. These pulses are all at their peaks. To have any effect, a noise pulse must be large enough to reverse the polarity of a data pulse. Data can be written immediately adjacent to previously written data because the timing is controlled by the timing track that is written on the tape.

Information is stored on the tape in block form (Figure 2-3). Block length is flexible and determined by information on the mark-track. A complete reel of tape (849,036 lines) can be divided into any number of blocks up to 4096. As stated earlier , a uniform block length is established over the entire length of a reel of tape by a program which writes mark and timing information at specific locations. The ability to write variable-length blocks, however, is useful for certain formats, for example, where small blocks containing index or tag information need to be alternated with the large blocks of data.

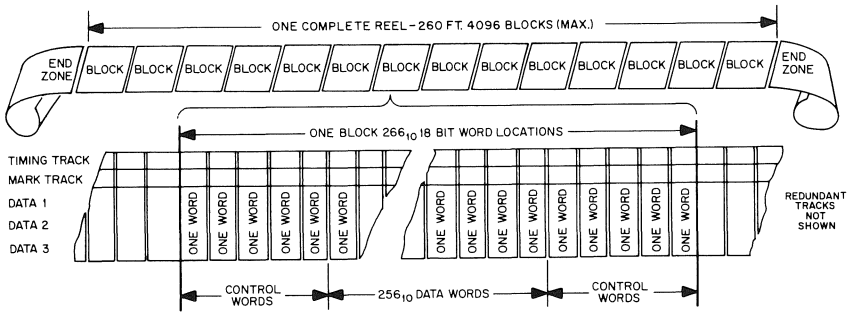


Figure 2-3 Control and Data Word Assignments

Each block contains data and control words as shown in Figure 2-3. These of course are assembled by the TC02. Control words separate the data portions of adjacent blocks and record address and checking information. Each control or data word occupies six lines on tape, i.e., 18 bits (see Figure 2-1).

2.3.1 Mark-Track Format

One of the five DECtape channels is reserved for control information exclusively. The control codes are stored serially, six bits per code. The mark track contains these 6-bit codes (see Figure 2-1), which initiate controls to raise flags in the program, request data breaks, detect block mark numbering and block ends, and protect control portions of tape (see Figure 2-4). The TC02 automatically identifies these codes to control transmission of data. The mark track also provides for automatic bidirectional compatibility, variable block formatting, and end-of-tape sensing.

During all tape processing functions except recording of the timing and mark track, a single mark-track bit is read from each line of tape, regardless of whether the information is being read from or written onto the data tracks; and each tape line in both the information and mark tracks is positioned at the center of the right polarization in the timing track, as shown in Figure 2-1. The six lines on the tape that contain the mark code in the mark track are designated as a mark frame.

A given change of polarization on tape read in one direction produces a pulse opposite in polarity to that produced by the same change when tape is read in the opposite direction. Consequently, a mark code read in reverse of the direction in which it was recorded has the order of bits reversed and the bits complemented. For example, a mark code read forward as 100101 is read as 010110 in reverse. This correspondence is termed the complement obverse or the complement image. Every 6-bit code has one and only one complement obverse which is constructed by complementing all bits and reversing their order. Therefore, the complement obverse of the complement obverse is the original code itself. In octal notation, the complement obverse of any pair of digits is constructed by reversing the order of digits, then performing the following transformation on each:

0 - 7	1 - 3	2 - 5	3 - 1
4 - 6	5 - 2	6 - 4	7 - 0

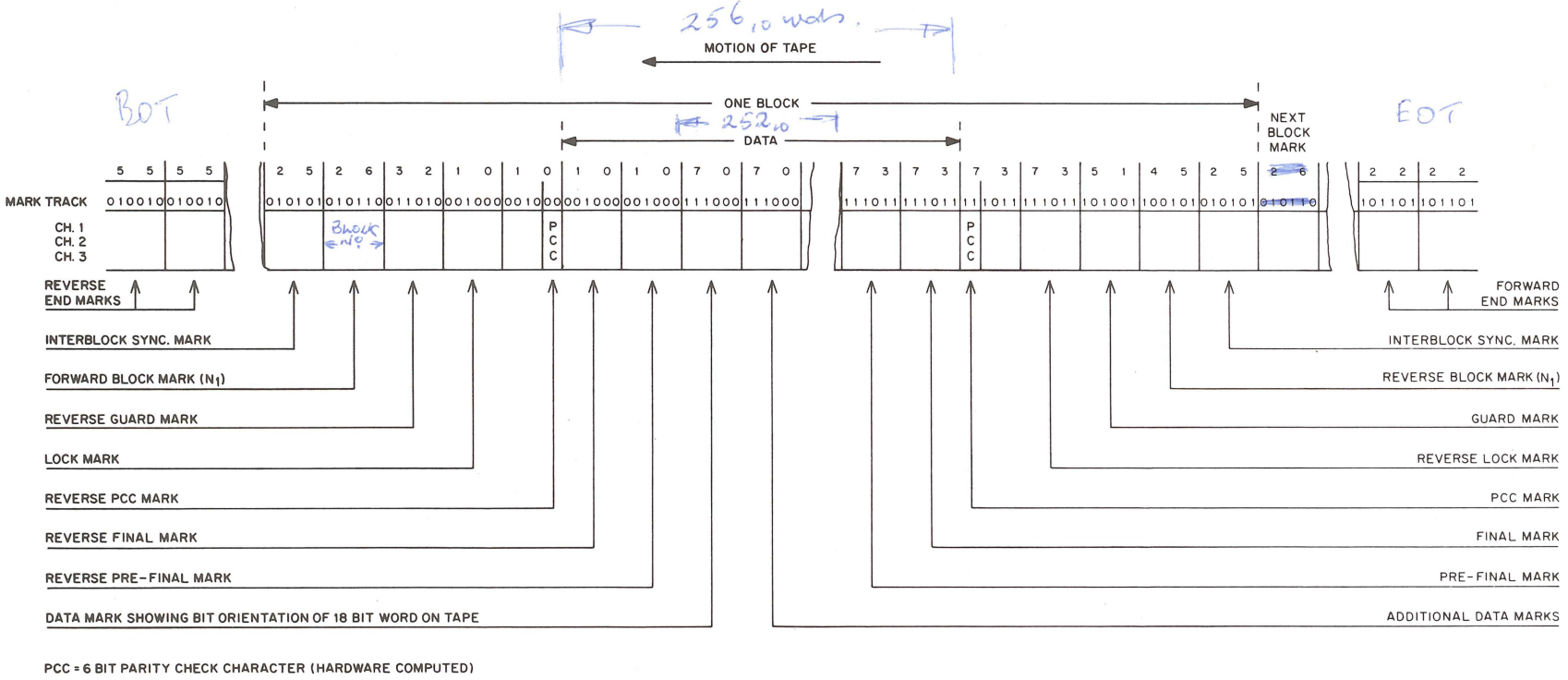


Figure 2-4 Mark-Track Format

The transformations indicate that there are eight octal codes which are their own complement obverses: 07, 13, 25, 31, 46, 52, 64, and 70. All other possible combinations of two octal digits (there are 56) are different from their complement obverses. As shown in Table 2-1, the complement obverse of any mark is designated by the minus sign (e.g., mark G = 51 has the complement obverse -G = 32).

Since the DECtape system allows reading and writing in both directions of tape motion, the mark track must be coded to present the same information when entering a block from either direction. The marks at the end of a block are the complement obverses of the marks at the beginning, in reverse order. For example, if the control reads the marks E, M, -G as the first three marks beginning a block in forward motion, then it will read G, -M, -E, in that order, as the last three marks of the same block. In reverse motion, however, the control sees the complement obverse of the contents of the mark track; thus the first information, when reading the block in reverse, is -(-E), -(-M), -(G), which is identical to E, M, -G.

All marks used in the standard DECtape format are listed in Table 2-1. Only 10 valid codes exist even though a given code may have different designations. Some of these marks are not required for the operation of the Type TC02 DECtape control.

Table 2-1
Mark Track Coding

Mark	Octal Code	Function
C (Check)	73	Signifies the end of a mark frame whose first two lines were the forward parity check group.
-C (Reverse Check)	10	Signifies that the 6-bit reverse longitudinal parity check group is contained in the control unit read/write buffer and that the beginning of the data portion of a block is in the forward direction.
E, -D (Data)	70	In both forward and reverse tape motion, the data mark occupies all mark frames in the data portion of the block except for the final and prefinal marks. The number of data marks is limited only by the length of tape.
E, (Interblock)	25	The first and last mark of every block (no-op mark).
End (Forward End)	55	Indicates the end zone of tape in forward direction. The forward end mark is positioned approximately 10 ft from actual tape end.
-END (Reverse End)	22	Indicates the end zone of tape in reverse direction. The reverse end mark is positioned approximately 10 ft from end of tape.
F (Final)	73	Signifies that the last word read from the data portion of the block is in the read/write buffer and data buffer. Signals that the next frame begins with the 6-bit forward longitudinal parity check group.
-F (Reverse Final)	10	Signifies that the last word read from the block, in the reverse direction, is in the read/write buffer and data buffer.

Table 2-1 (Cont)
Mark Track Coding

Mark	Octal Code	Function
G (Guard)	51	Performs same function as -L (reverse lock).
-G (Reverse Guard)	32	
L (Lock)	10	Indicates the first of four octal 10 marks.
-L (Reverse Lock)	73	Protects subsequent records in the event of mark-track errors.
M (Forward Block)	26	Signifies the start of a block and indicates that the block number is contained in the TC02 control.
-M (Reverse Block)	45	
P (Prefinal)	73	In the forward tape direction, the prefinal mark is the next to last mark in the data portion of a block. It is the first of four marks using octal code 73.
-P (Reverse Prefinal)	10	In the reverse tape direction, signifies the next to last mark in the data portion of a block.

The standard mark track uses the serial code of 6-bit characters to divide the tape into words. Codes are written on the mark track opposite word locations to identify the type of information stored at that location on tape. Block addresses are written for both forward and reverse directions and identified by two types of mark codes (the second is the complement obverse of the first). A checksum is written at each end of the block. The hardware computed checksum is the 6-bit logical equivalent (i.e., the complement of the exclusive OR) of each six bits written on tape plus the reverse checksum previously recorded. By including the reverse checksum in the computation, the block may be read in either direction at a later time without an error. The control uses the final marks to establish synchronism and raise block-end flags. Data marks locate data words.

2.4 DECTAPE INSTRUCTIONS

The seven basic IOT instructions used in the programming of the PDP-9 for TC02 operations are listed in Table 2-2, with octal code assignments and a description of the instruction operation. These instructions apply to two functional groups within the TC02, designated as status A and status B, and are used to clear, read, and load the status A and B registers. These two registers are used to govern tape operations and provide status information to the computer programs.

Table 2-2
TC02 DECtape Instruction List

Mnemonic	Octal Code	Description
DTCA	707541	Clear status A register. The DECtape control and error flags are undisturbed (DTF and EF).
DTRA	707552	Read status A register. The AC is cleared and the content of status A register is ORed into the accumulator.
DTXA	707544	XOR status A register. The exclusive OR of the content of bits 0 through 9 of the accumulator and status A is loaded into status A register, and bits 10 and 11 of the accumulator are sampled to control clearing of the error and DECtape flags, respectively. Any time this command is given with AC bits 0 through 4 set to 1, the select delay of 120 ms will be incurred, while the new mechanical motion begins.
DTLA	707545	Load status A register. Combines action of DTCA and DTXA to load AC0 through 9 into status A register. Bits 10 and 11 control clearing of error and DECtape flags, respectively.
DTEF	707561	Skip on error flag. The state of the error flag (EF) is sampled. If it is set to 1 the content of the PC is incremented by one to skip the next sequential instruction.
DTRB	707572	Read status B. The AC is cleared and the content of status B is ORed into the accumulator.
DTDF	707601	Skip on DECtape flag. The state of the DECtape flag (DTF) is sampled. If it is set to a 1, the content of the PC is incremented by one to skip the next sequential instruction.

2.5 STATUS A AND B REGISTERS

All 10 command bits (0 through 9) of status A register may be sensed, set, or changed via IOTs. Bits 10 and 11 of the AC are not retained by status A but enable or disable the clearing of the DECtape and ERROR flags. The bits in status B register may be sensed and cleared by IOTs.

To issue a DECtape command, the command bits 0 through 9 of status A register are set as desired by bits 0 through 9 of the AC with bits 10 and 11 set to 0. Bit 11 of B register is set when a DTF occurs and must be cleared before the next DTF to avoid a timing error. When any error occurs, bit 0 of B register and the corresponding bits 1 through 5 will be set depending on the error. This bit must be cleared to avoid further interrupts on the same condition. All error flags (status B register) are cleared by issuing a DTXA instruction with AC bit 10 set to 0.

2.5.1 Status A Register Functions

Figure 2-5 is the format for the status A register. This register contains three unit select bits, two motion bits, one mode bit, three function bits and three bits which control the flags. The bit assignments for the status A register are provided in Table 2-3.

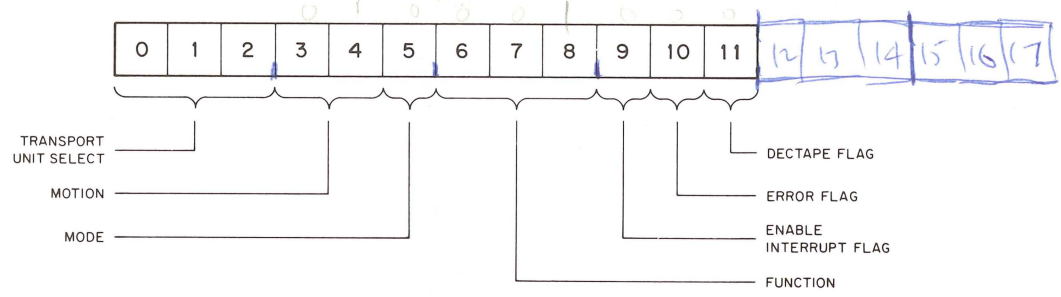


Figure 2-5 Status A Register, Format

Table 2-3
Status A Bit Assignments

Function	AC Bit	Conditions
Transport Unit Select	0-2	Octal Code / Unit 000 / 8 001 / 1 010 / 2 011 / 3 100 / 4 101 / 5 110 / 6 111 / 7
Motion	3	0 = Forward (FWD) 1 = Reverse (REV)
	4	0 = Stop motion (STOP) 1 = Start motion (GO)
Mode	5	0 = Normal mode (NM) 1 = Continuous mode (CM)
Function	6,7,8	Octal Code / Operation 000 / Move 001 / Search 010 / Read data 011 / Read all 100 / Write data 101 / Write all 110 / Write timing and mark track 111 / Unused (causes select error)
Enable the interrupt ENI	9	1 = Enable DECtape control flag DTF and EF to cause program interrupt
Error flag EF	10	0 = Clear all error flags 1 = Error flags undisturbed
DECtape flag DTF	11	0 = Clear DECtape flag 1 = DECtape flag undisturbed

2.5.2 Status B Register Functions

Figure 2-6 shows the format of the information in the status B register. This register contains 6 bits of error status information, and the DECtape flag bit. Table 2-4 lists the function of the bit assignments.

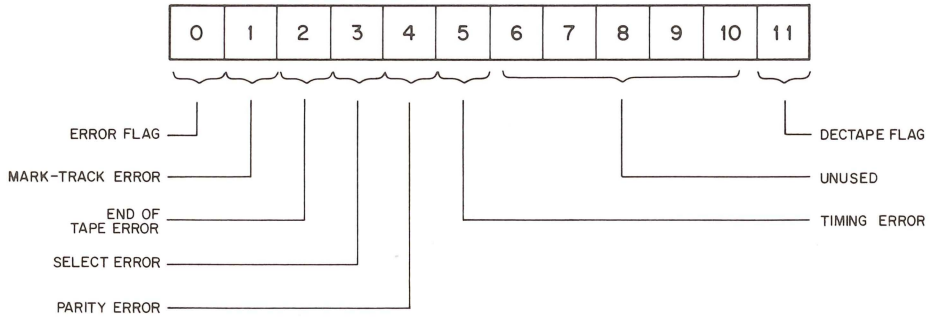


Figure 2-6 Status B Register, Format

Table 2-4
Status B, Bit Assignment

Function	AC Bit	Conditions
Error Flag (EF)	0	1 = Detection of any nonoperative condition by the control as listed in the error functions described in AC bits 1 through 5 of this table. These conditions stop transport motion except for parity errors.
Mark-Track Error (MKTRK)	1	1 = Information read from mark track is erroneously decoded.
End of Tape Error (END)	2	1 = the end zone on either end of tape is over the read head.
Select Error (SE)	3	This error occurs 5 μs after loading status A register to indicate one or more of the following conditions. (a) The unit select code specified does not correspond to any transport select number or is set to more than one transport. (b) Specifies a write function when the WRITE ENABLE/WRITE LOCK switch is in the WRITE LOCK position. (c) Specifies an unused function code (111) bits 6 through 8 of the status A register. (d) Specifies any function except Read All with the maintenance control panel RDMK/WRTM/NORMAL switch in the RDMK position. (e) Specifies any function except Write Timing and Mark Track with the RDMK/WRTM/NORMAL switch in the WRTM position. (f) Specifies the Write Timing and Mark-Track function with the RDMK/WRTM/NORMAL switch in a position other than WRTM.

Table 2-4 (Cont)
Status B, Bit Assignment

Function	AC Bit	Conditions
Parity Error (PAR)	4	1 = Error occurs during a Read Data function if the longitudinal parity over entire data block including reverse checksum and checksum, is not equal to 1. If a parity error is to be set at the end of a block, it will be set at the same time the DTF is set. During CM if a word count overflow does not occur at the end of a block, the parity error is set at the end of the block in which the parity error occurs. The parity error cannot be set after the DTF is set.
Timing Error (TIM)	5	1 = Program fault caused by one of the following conditions: (a) A data break request is not answered within 66 μs ±30% of the data break request. (b) The DTF was not cleared by the program before the control attempted to set it. (c) The read data or write data function was specified after the current data block has been entered to prevent incomplete data block transfers.
	6,7,8,9, 10	Unused
DECtape Flag (DTF)	11	1 = DECtape operation complete

2.6 CONTROL MODES AND FUNCTIONS

The TC02 control unit operates in either the normal mode (NM) or continuous mode (CM) as determined by the mode bit (5) in the status A register. In the normal mode, the data transfer and flag indications are controlled by the format of the information on tape. In the continuous mode, data transfer and flag indications are controlled by a word count (WC) read from core memory and by the tape format.

The normal mode differs from the continuous mode primarily in the time at which the DECtape flag (DTF) is set. The DECtape flags which occur in the normal mode are inhibited in the continuous mode until a word count overflow has occurred. In both modes, data break requests occur only when a word count overflow has not occurred during the currently specified function.

2.7 CONTROL FUNCTIONS

The seven functions available with the TC02 and their octal numbers, as specified by the bits 6 through 8 of the AC are as follows.

Function	Octal No.
Move	0
Search	1
Read Data	2
Read All	3
Write Data	4
Write All	5
Write Timing and Mark Track	6
Unused at present (select error if given)	7

All functions take place in either direction and in either normal mode (NM) or continuous mode (CM). NM differs from CM only in the fact that the DECtape flag (DTF) occurs at more frequent intervals in NM. The DTF settings which occur in NM are eliminated in the CM until word count overflow (WC) has occurred.

2.7.1 Move

The Move function simply sets the selected unit in motion (forward/reverse). NM and CM have no meaning and are ignored in this function alone. When the tape enters either end zone* (i.e., beginning of tape (BOT) and end of tape (EOT)), and the unit in question is selected:

a. The error flag (EF) is set.

b. The EOT bit (bit 2 of status B register) is set.

c. An interrupt occurs.**

A program check on the forward/reverse motion bit (AC bit 3) of the status register will determine whether EOT or BOT occurred. If the unit is deselected, however, the tape runs off the reel with no flags raised and no interrupt. In order to stop a selected unit at any time, the GO bit (AC bit 4) must be set to 0.* Once a unit is deselected, status information pertaining to that unit is no longer accessible unless it was saved by the program prior to deselection.

2.7.2 Search

The Search function provides the capability of random access of data blocks on DECtape. This function is used to locate the number of the block to or from which data transfer will occur. In normal mode at each block mark until EOT occurs, the DTF is raised and an interrupt occurs. The block number is automatically transferred by the hardware into the memory location specified by the

---

* If either end zone is entered during turn around or during stopping of tape, the EOT bit is not set and no interrupt occurs.

**All references to the occurrence of interrupts assume both that the program interrupt is on, and the DTF and EF have been enabled to the program interrupt or API (i.e., bit 9 of status A register is set to a 1). If either of these is not true, flags are raised and status bits are set (and may be sensed and/or cleared), but no interrupt occurs.

CA (current address). The CA must have been set previously by the program, but the contents are not incremented. The WC is incremented at each DTF, and the program must clear the DTF bit in the status register and check the block number until the desired one is found.

In continuous mode, the WC is set to the 2s complement of the number of blocks to skip. At each block mark, the block number is read into the memory location specified by the CA which is not incremented. The DTF is raised only at the block mark at which the WC overflows. At that time, an interrupt occurs. Continuous mode provides a virtually automatic DECtape search.

2.7.3 Read Data

The Read Data function is used to transfer blocks of data into core memory with the transfer controlled by the standard tape format. The standard block length is 256 18-bit words. For this and all following functions, the CA register initially must be set to the transfer memory location - 1 because the CA register is incremented just before each word transfer. The WC register is also incremented prior to each word transfer so must be set to the 2s complement of the number of words to be transferred prior to the transfer. Data may be transferred in forward or reverse but it is transferred into (from) ascending addresses in memory.

Any number of words equal to or less than 1 block may be transferred in NM. The DTF is raised and an interrupt occurs at the end of each block. The DTF must be cleared before the beginning of the next block (i.e., 1.7 ms) to avoid an erroneous timing error. When partial blocks are transferred, data transmission ends with WC overflow (i.e., the word which causes the WC overflow is the last one transferred). The remainder of the block is read and parity checked, however, before the DTF and interrupt occur. Tape motion continues until the GO bit is reset to 0 by the program. If the GO bit is not reset to a 0 or a new function specified before the end of the next block, a timing error will occur. READ DATA in NM is intended primarily for single, 256-word, block transfers. If any other number of words is to be transferred, it is advantageous to use CM. If the programmer chooses to use NM for any other number of words, however, the program must check for WC overflow of each interrupt since there is no other way to determine when to stop the tape or change to another function. When the WC overflow occurs, it is essential that the function be changed or the GO bit set to 0. Otherwise transfer begins again (the IOT to clear the DTF implicitly specifies the same function again) at the next block (or next word for the ALL BITS functions) since WC = 000000_8 is valid.

Any number of words may be transferred in CM. However, the DTF and an interrupt occur only once after a WC overflow and an end of block. The comments concerning tape continuation apply in CM as well as NM.

2.7.4 Read All

The Read All function allows information to be read from an unusually formatted tape essentially reading all data channels recorded on DECtape regardless of the mark-track value. During the Read All function the DECtape control does not distinguish between different marks recorded on the mark track -- except to check for mark-track errors (MKTK) and end of tape (END).

In normal mode (NM), the DTF is raised and causes an interrupt at the end of each 18-bit word transfer. Data transfer stops after WC overflow, but tape motion continues until the GO bit is set to 0 or a new function is specified (in both NM and CM). If the DTF is not cleared after each word transfer, a timing error occurs at the end of the next word (i.e., 200 μs later).

For continuous mode, the DTF is raised and causes an interrupt at WC overflow only. If this interrupt is ignored no more data transfers occur but tape motion continues to EOT.

2.7.5 Write Data

The WRITE ENABLE switch on the TU55 must be in WRITE ENABLE position for all Write functions. All the details of the Read Data function description apply with the following exceptions.

In normal mode, the DTF is set to a 1 at the end of each block. If WC0 did not occur in the block just ended and a new function is specified, the next block will be written (provided the DTF has been cleared). If WC overflow did occur in the block just ended and no new function is specified, the tape continues to move but the writers are disabled. In both CM and NM, when partial blocks are written, data transfer from core to DECtape stops at WC overflow. The 000000s are written in the remaining data words of the block and the parity check character is computed over the entire block and recorded.

In continuous mode, the DTF is set at the end of the block in which WC overflow occurred. Therefore, if no new function is specified, the tape continues to move but the writers are disabled.

2.7.6 Write All

All the details of the Read All function description apply. The Write All function is used to write an unusual format (such as block numbers on DECtape after timing and mark tracks have been recorded). The word which causes WC overflow is the last one written in NM or CM. The tape continues to move but the writers are disabled.

NOTE

Change of function must be delayed for 90 μs to insure recording of last word. Alternative method: set WC to 1 greater than desired number of word transfers and change function within 40 μs after WC0.

2.7.7 Write Timing and Mark Tracks

This function and only this function may be performed with the selector switch on write timing and mark track (WRTM) on the maintenance control panel. Whereas the timing track is actually hardware recorded during execution of this function, the mark track is generated and recorded by program. The value written in the mark track is determined by bits 0, 3, 6, 9, 12, and 15 of the 18-bit word being written (i.e., the same bits assigned to channel 1).

CM may be conveniently used for this function since the hardware WC provides an automatic counter and interrupt at WC overflow only; in NM, the DTF and interrupt occur at every word until

WC overflow. In NM, after WC overflow, if the GO bit or DECtape flag are not cleared, a timing error occurs and no more data is recorded. After WC overflow in CM, if the GO bit is not set to 0, zeros are written on down tape.

2.7.8 Enable and Interrupt Feature

The enable-to-the-interrupt feature allows the program to remove DECtape from the program interrupt line (even if the interrupt is ON). This is primarily of value in the automatic priority interrupt system.

When command bit 9 in the status register is set to a 1, the TC02 is connected to the interrupt system. If this bit is 0, the DTF in the TC02 cannot cause an interrupt even if the interrupt facility in the PDP-9 is ON. Similarly, any of the five error conditions will cause an interrupt if bit 9 is set to 1 in the status register, but cannot cause a program interrupt if bit 9 is a 0.

Whether this bit is set or not does not influence the setting of status bits 0 through 5 of the status B register upon receipt of an error flag (EF) or DTF. Similarly, the result of the I/O skip instruction is independent of the condition of this bit.

2.7.9 Error Conditions

Five types of errors can be detected in using DECtape: timing, parity, selection, end-of-tape, and mark-track errors.

For all errors the EF is raised, a bit is set in the status register, and an interrupt occurs (if the enable-to-interrupt bit has been set). The DTEF instruction skips on the inclusive OR of those error bits; hence, each status bit must be checked to determine the kind of error. For all but the parity error, the selected transport is stopped and the EF is raised at the time of error detection. No DTF occurs. For a parity error, the GO bit remains 1 (i.e., motion continues) and the EF is raised simultaneously with the DTF in NM. Only 1 interrupt occurs, hence the program must check the EF.

A parity error in CM raises the EF at the end of the block in which the parity occurs, causing an interrupt (if enabled). If no program action is taken, for example, stop transport or reverse and reread, data transfer continues and the DTF is raised and causes an interrupt at WC overflow and end of final block read.

2.8 PROGRAMMED OPERATION

Before using DECtape tape for data storage, the reel of tape is prerecorded in two passes. In the first pass, the timing and mark tracks are placed on the tape. During the second pass, the forward and reverse block numbers are written. Prerecording uses the WRTM control function and the manual switch on the maintenance control panel of the type TC02 control to (1) write on the timing and mark tracks, (2) to activate a clock which produces the timing track recording pattern, and (3) to enable flags for program control.

Unless the WRTM control function and the switch are used simultaneously, writing on the mark and timing channels is inhibited. A red indicator lights on the maintenance control panel when the manual switch is in the WRTM position.

The seven basic IOT instructions are generated, as required, by the PDP-9 program to clear, read, and load the Status A and Status B elements. The IOT skip instruction is available to test the status of the TC02 control. Since all data transfers between the TC02 and the PDP-9 memory are controlled from the computer, the program sets the word count (WC) and current address (CA) registers using the memory reference instruction in the process of initializing a block transfer. Before and after a DECtape operation, the program can check for error conditions.

The DECtape system is started with the search function to locate the block number selected for transfer. When the correct block is found, the transfer is accomplished by setting the WC, CA, and the status A and status B registers. When searching, the DECtape control reads only block numbers. These are used by the operating program to locate the correct block number. In NM, the DTF is raised at each block number. In CM, the DTF is raised only after the WC reaches zero. The CA is not incremented during searching, and the block number is placed in core memory at the location specified by the contents of the CA. Data is transferred to or from PDP-9 memory from locations specified by the CA which is incremented before each transfer.

When the start of the data position of the block is detected, DF is raised to initiate a data break request to the computer each time the DECtape system is ready to transfer an 18-bit word. Transfers occur between the DECtape and successive core memory locations specified by the CA. The initial transfer address-1 is stored in the CA by an initializing routine. The number of words that are transferred is determined by the tape format in NM or by the tape format and WC in CM. At the conclusion of the data block transfer, the DTF is raised and a program interrupt occurs. The interrupt subroutine checks the DECtape error bits to determine the validity of the transfer and either initiates a search for the next information to be transferred or returns to the main program.

During all normal writing transfers, a checksum (the 6-bit logical equivalent of the words in data block) is computed automatically by the control and is automatically recorded as one of the control words immediately following the data portion of the block. The same checksum is used during reading to determine that the data playback and recognition takes place without error.

Any one of the eight tape transports may be selected for use by the program. After using a particular transport, the program can stop the drive currently being used and select a new drive, or can select another transport while permitting the original selection to continue running. This allows rapid searching, since several transports may be used simultaneously. Caution must be exercised because, although the original transport continues to run, no tape-end detection or other sensing take place. All functions provide for automatic and sensing, but this feature stops tape in the selected tape drive only.

For programming examples that illustrate possible ways to code DECtape functions on the PDP-9, see the PDP-9 Users Handbook, Chapter 5, page 5-13.

CHAPTER 3
PRINCIPLES OF OPERATION

This chapter provides a description of the basic functional elements of the DECtape Control Type TC02, descriptions of data and control information transfers, and detailed descriptions of TC02 control operations. For information on the PDP-9 and TU55 transport, refer to the documents listed in Table 1-1.

3.1 FUNCTIONAL DESCRIPTION

The I/O bus interface shown in Figure 3-1 is completely described in paragraph 3.3.2.1. When operations are initiated, and the device number, to which the command in the I/O bus is addressed, is sent, the major registers are cleared. Information then is transferred into the TC02 registers from the computer or read from the DECtape into the TC02 registers for assembly of a computer word.

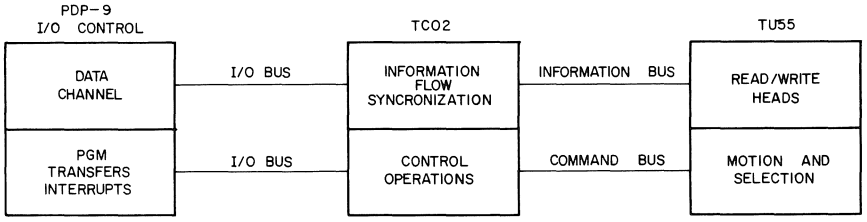


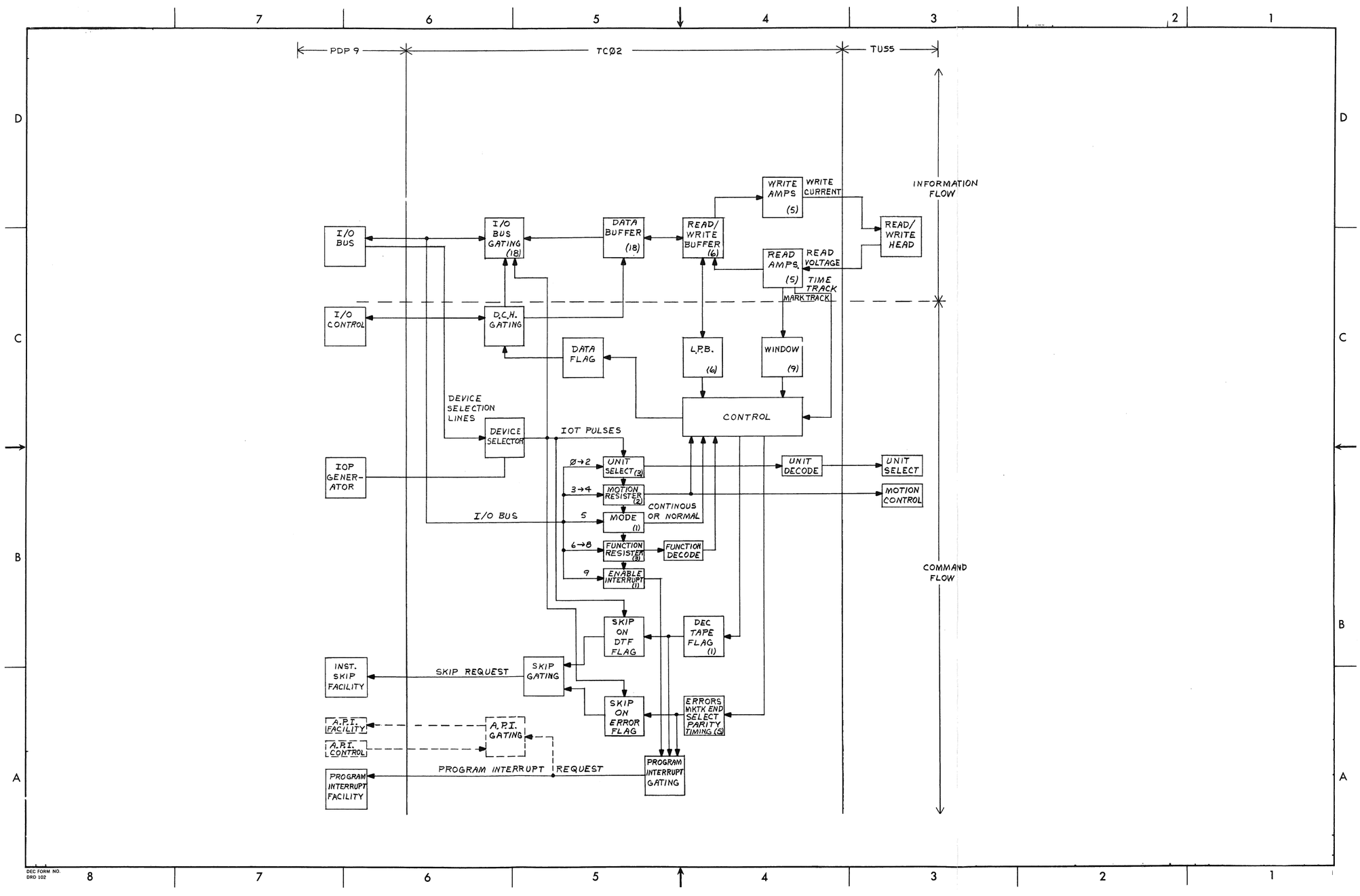
Figure 3-1 Information and Command Flow

Once the tape unit is selected, the read or write operation is established, and proper motion is determined.

The basic functional elements of the PDP-9 processor, TC02 control, and TU55 transport interface blocks are shown in Figure 3-2. Numerals in the lower right-hand corner of the blocks indicate the bit capacity of the element. Numerical subscripts on the signal flow lines indicate the bit assignments of the signals. Numerals in the lower left-hand corner indicate the engineering drawing that shows the detailed elements of the function. Blocks that represent the Status A and Status B functions are indicated by A and B, respectively, at the top right-hand corner of the block.

3.1.1 Information Flow

Information flow for write operation, indicated on Figure 3-2, involves transfer from the I/O bus through gating, a data buffer, read/write buffer, and write amplifiers to the write heads. For reading, data is transferred through the read amplifiers and back through the same elements. The following list defines the characteristics and functions of each of these elements.



DEC FORM NO. DRD 102

Figure 3-2 Type TC01 DECtape Control Functional Block Diagram

a. Data Buffer (DB). - The data buffer is an 18-bit register used as a storage buffer to synchronize data transfers as a function of tape timing between the memory buffer register of the computer and the read/write buffer.

b. Read/Write Buffer (RWB). - The read/write buffer is a 6-bit register consisting of two 3-bit registers which transmit data between the data control and the read/write heads. During read operations, one bit from each of the three data channels on tape is read into the read/write buffer and shifted left.

c. Write Amplifiers. - The five write amplifiers receive timing signals, mark-track, and data information from the read/write buffer and provide the necessary current to the tape heads to write the data on tape.

d. Read Amplifiers. - The five read amplifiers transfer information from the tape heads to the read/write buffer, and mark track to the window register, and timing signals to control.

3.1.2 Command Flow Registers

The registers and signals which control the transport operations and the data flow are described as follows.

a. Longitudinal Parity Buffer (LPB). - The longitudinal parity buffer is a 6-bit register used to perform a parity check on the three information channels. The operation is performed by setting the 6-bits of information read from two consecutive lines on tape into the RWB and complementing each stage of the LPB if the corresponding bit of the RWB contains a zero.

b. Window (W). - The window is a 9-bit shift register through which mark-track information is serially shifted to generate control signals for the DECtape system. Because the mark-track window is three bits longer than is required to contain one mark, additional redundance is provided to check that marks follow one another in the proper order. The bits of the mark-track window are continuously decoded to detect when any of the legal marks appear.

c. Data Flag (DF). - The data flag flip-flop through DCH gating, requests a data break from the processor when a word is ready to be transferred to or from the TC02.

d. Control. - The control logic generates the timing and synchronizing pulses to perform the functions specified in the function register and to coordinate the operations between the PDP-9 processor and TU55 transport.

e. Device Selector. - The device selector decodes the IOT instructions for the DECtape and generates the necessary pulses to load status registers, and generate SKIP pulses.

f. Unit Select Register. - The unit select register is a 3-bit register which is loaded under program control from the accumulator bits 0 through 2, and specifies a particular TU55 transport.

g. Motion Register. - The motion register is a 2-bit register loaded from the accumulator bits 3 and 4, with the appropriate command of GO or STOP (bit 4), FORWARD or REVERSE (bit 3).

h. Mode Register. - The mode register is a 1-bit register that selects either normal or continuous mode.

i. Function Register. - This is a 3-bit register that specifies one of seven possible operations to be performed by the DECtape.

j. Function Decoder. - This decodes the content of the function register bits 1 through 3, and transfers the decoded information to the control.

k. Enable to the Interrupt. - This 1-bit register is loaded from the accumulator, bit 9, to enable or disable the DECtape from the program interrupt.

l. Error Register. - A 5-bit register in which any section can be set by the TC02 control to indicate one of five error conditions.

m. Error Flag (EF). - The error flag is set by one or more errors indicated by the error register.

n. DECtape Flag (DTF). - The DECtape flag is set at the completion of the currently specified operation.

o. Skip Gating. - Skip gating logic generates a pulse from the DTF flag and SKIP IOT to request a skip from the PDP-9. This gating is not affected by the enable to the interrupt.

p. Interrupt Gating. - This requests the program interrupt from the PDP-9 when the EF or DTF is set and the DECtape is enabled to the interrupt.

3.2 SYMBOLS AND ABBREVIATIONS

The listings of Table 3-1 and 3-2 identify the engineering drawing set and the major symbols and abbreviations used and referenced in this chapter.

Table 3-1
Engineering Drawing Identification

Dwg No.	Mnemonic	Description
TC02-0-1	R/W AMPS, SP GEN, TEST CONN	Read/write amplifiers, special generator and test connector
TC02-0-2	LPB & RWB	Longitudinal parity and read/write buffer registers
TC02-0-3	I/O Bus Gating	Input/output bus gating
TC02-0-4	I/O Bus, IOTs	Input/output bus and IOT (input/output transfer) instructions
TC02-0-5	ERRORS, MCP SWITCH	Error flip-flops (status B register) and manual control panel switch
TC02-0-6	CONTROL	Control circuits including DTF and DF flip-flops counter circuits, and major system control signals
TC02-0-7	STATUS A, COMMAND BUS	Status A register (unit selection, motion, functions, and ENI)
TC02-0-8	WINDOW, MK TK, STATE	Window register, mark-track logic
TC02-0-9	MCP & CABLES	Maintenance control panel and cables

Table 3-1 (Cont)
Engineering Drawing Identification

Dwg No.	Mnemonic	Description
TC02-0-10	TP GEN	Timing pulse generator
TC02-0-11	DTB	Data buffer register
TC02-0-15	Timing	Four drawings
TC02-0-16	DCH, API	Data channel, automatic priority interrupt

Table 3-2
Symbols and Abbreviations

Symbol/ Abbreviation	Description	Source Dwg.	Destination Dwg.
0 → DTB	Reset the DTB (buffer)	6	11
0 → DTF	Reset the DTF flip-flop (DECtape flag)	6	16
0 → EF	Reset the EF flip-flop (error flag)	5	16
0 → LPB	Reset the LPB (longitudinal parity buffer)	4	2
0 → STATUS A	Reset status A register flip-flops (USR, MR, FR, ENI)	4	7
0 → WINDOW	Reset the window register	10	8
+1 → CA INHIBIT	Inhibit incrementing the CA (current address register)	16	4
1 → DTF	Set the DECtape flag flip-flop	6	5
(100) → C02	Set C0, Clear C1 and C2	6	10
BMR1	Buffer motion register	7	7,10
BXSA DY	Control flip-flop signal	5	7
C0-2(101)MK BLK MK	With SEARCH to produce 1 → DF	8	6
C0, C1 and C2	Control clock flip-flops	6	5, 6, 8, 9
CK0	Clock counter bit 1	10	10
CK1	Clock counter bit 2	10	1
CLR DF	Clear data flag flip-flop	16	6
COMP RWB 0-2	Complement read/write buffer register 0-2	6	2
C STA	From the processor, produces reset to status A register, initiates XSA DY and BXSA DY delay	4	5,7
C SYNC	Level used to sync counter C0-2	8	6
DATA SYNC	Counter sync-ed with data	10	6, 8, 9
DCH EN IN	Data channel enabled in	17	16
DCH EN OUT	Data channel enabled out	16	4
DCH GRANT	Data channel granted	4	16

Table 3-2 (Cont)
Symbols and Abbreviations

Symbol/ Abbreviation	Description	Source Dwg.	Destination Dwg.
DCH RQ	Request for data channel	16	to processor
DS 0-5	Device selector lines	4	...
DTB 0-5, 6-11, DTB 12-17	DECtape buffer register	11	2, 3, 9
DTB → I/O BUS 0-9 DTB → I/O BUS 10-17	Enables transfer of assembled computer word onto the I/O bus	4	3
DTENA	Used to sync data channel breaks	16	5
DTENB	Used to sync data channel breaks	16	5, 6, 7
DT RQ	Used to sync data channel breaks	16	
DF	Data flag signal		
DTF	DECtape flag	6	3, 4, 5, 9, 16
EF	Error flag	5	3, 4, 16
EF + DTF	Error flag or DECtape flag	16	3
END	End of tape	5	3, 9
ENI	Enable the interrupt	7	3, 16
FWD	Forward motion	7	TU55
FR0	Function register bit 1	7	3, 6, 9
FR1	Function register bit 2	7	3, 5, 6, 9, 16
FR2	Function register bit 3	7	3, 9
FR3	Function register bit 4	7	3, 6, 8, 9
GO	Go command	7	TU55
INT	Generates interrupt request	16	16
I/O ADDR	Address for DCH or API break	16	4
I/O BUS 0-9	Inputs to status A register	3	7
I/O BUS 0-17	Data inputs to DTB	3	11
I/O BUS 10	To control clear to status B register	3	5
I/O BUS 1-4	Generates signal NEW U+M	3	10
IOP 1-4	IOPs from the computer	4	4
IO OFLO	Word count overflow indication	4	6
IO PWR CLR	IO power clear	4	5
IO SYNC	I/O sync signal	4	4, 16
LDTB	Buffer signal	4	11
LPB 0-5	Longitudinal parity buffer bits 0 through 5	2	9, 11
LPB → DTB	Load LPB bits into data buffer	6	11
LPB ≠ 1	LPB bits not equal to 1	2	5

Table 3-2 (Cont)
Symbols and Abbreviations

Symbol/ Abbreviation	Description	Source Dwg.	Destination Dwg.
LPB DTB 0-5	LPB bits to DTB bit locations 0 through 5	6	11
MK BLK END	Flag signal marking end of data block	8	3, 6
MK BLK START	Flag signal marking start of data block	8	3
MK END	Flag signal indicating that the end zone is entered	8	3
MK DATA	Mark data	8	3
MK TK	Mark-track error flip-flop signal	5	3, 9
MOVE		7	5
MR0	Motion register 0 bit	7	3, 9
MR1	Motion register 1 bit	7	3, 9, 10
PAR	Parity error signal	5	3, 9
PROG INT RQ	Program interrupt request	16	4
PWR CLR	Power clear signal	4	5, 6, 10, 16
PWR CLR + ES	Power clear or error stop	5	7, 10
RATE DY		10	9
READ ALL		7	5, 6
RD STATUS	Control pulse initiated by IOP	4	3
READ DATA		7	5, 6, 8
REV	Reverse direction command to the transport	7	TU55
READ D0	Read amplifier output track 0	1	5
READ D1	Read amplifier output track 1	1	2
READ D2	Read amplifier output track 2	1	2
RD MK	Read mark level output from MCP switch	9	5
RD MK TRK	Read mark track	1	5
RD RQ	Read request	16	4
RD T TRK	Read timing track	1	10
RD + WD	Read or write data signal	6	5
ROTATE DTB 00-11	Rotate contents of data buffer bits 0 through 11	6	11
ROTATE DTB 12-17/RWB	Rotate data buffer 12 through 17 and RWB	6	2, 5, 11
RUN		4	7
RWB 0	Read/write buffer bit 0	2	1

Table 3-2 (Cont)
Symbols and Abbreviations

Symbol/ Abbreviation	Description	Source Dwg.	Destination Dwg.
RWB 0-5	Read/write buffer bit 0 through 5	2	9
RWB 1	Read/write buffer bit 1	2	1
RWB 2	Read/write buffer bit 2	2	1
RWB 3 IN	Read/write buffer 3 in	5	2
RWB ∀ LPB	Computes parity check in LPB	6	2
RWB SHIFT LEFT	Shift contents of RWB left and read next line of tape	6	2
SE	Select error enable	5,7	6
SEARCH		7	6, 8, 16
SEL	Select error flip-flop	5	3, 9
SINGLE UNIT		TU55	5, 7
SKP RQ	Skip request	4	
SP	Speed of DECtape	1	10
STA IO BUS	Write content status A register onto bus	4	3, 16
STB IO BUS	Write content status B register onto bus	4	3, 16
ST BLK MK	State in which control senses block numbers	8	5, 9
ST CK	State in which automatic error detection occurs	8	5, 6, 9
ST FINAL	Final data word of block state	8	6, 9
ST IDLE	State in which DECtape transport not up to speed, is stopped, or between blocks	8	4, 5, 6
STOP	Stop command to transport	7	TU55
ST REV CK	State in which reverse checksum is overhead	8	6, 9
SW TM	Switch timing and mark level output of MCP switch	5	6
TIM	Timing error	5	3, 9
T/M ENABLE	Timing mark enable	10	8
TP0	Timing generator signal 0	10	5, 6
TP1	Timing generator signal 1	10	6, 8
UNIT SELECT		7	TU55
UP TO SPEED	Indicates transport is up to operating speed	10	6, 8, 9
USR 0,1,2	Unit select register bits	7	3, 9
WC	Word count flip-flop	7	6, 9

Table 3-2 (Cont)
Symbols and Abbreviations

Symbol/ Abbreviation	Description	Source Dwg.	Destination Dwg.
WCO	Word count overflow pulse	17	7
WREN	Write enable	6	7, 9, 10
WRITE ALL		7	6
WRITE DATA		7	6
WRITE OK	Write enable/write lock sensing from TU55	TU55	5, 6, 7
WR RQ	Write request	16	17
WRTM	Write timing and mark	7	5, 6, 7, 8, 10
XSAD	Amplified XSTA pulse	7	5
XSA DY	Status A register delayed pulse	5	7
XSTA	Load status A register pulse	17	5, 6, 7

3.3 DETAILED DESCRIPTIONS

3.3.1 Basic Read/Write Logic

The basic read/write logic for the Type TC02 DECtape control is shown on the left of Figure 3-3. Each channel of the read/write circuit contains a flip-flop and input gates, a write amplifier governed by the flip-flop outputs and a read amplifier. Read inputs are paralleled with the write amplifier outputs across the head allowing the read amplifier to respond to signals from both the read and write amplifier.

The read amplifier is a high-gain differential amplifier augmented by a transient positive feedback. When a signal of either polarity is sensed by the head, the read amplifier outputs switch immediately and are asserted unambiguously, regardless of noise, which prevents head cross talk resulting from simultaneously writing in the data channels and reading in the timing and mark channels. The read amplifier outputs U and V are standard DEC logic levels of -3V and ground. When input E is more positive than D, V is asserted at ground and U is negative; when D is more positive, the output levels reverse. Because of positive feedback, the read amplifier oscillates in the absence of input signals. The read amplifier output waveforms therefore are rectangular whenever the differential input signal is indeterminate.

The write amplifier is a saturated grounded-emitter push-pull amplifier with its output collectors connected through resistances to pins J and K. If the enable level is asserted negative, the write amplifier is governed entirely by the state of the flip-flop. When the flip-flop is 1, K floats and J is returned through the resistance and the saturated output collection to -13V. When the flip-flop is 0, J floats and K is negative.

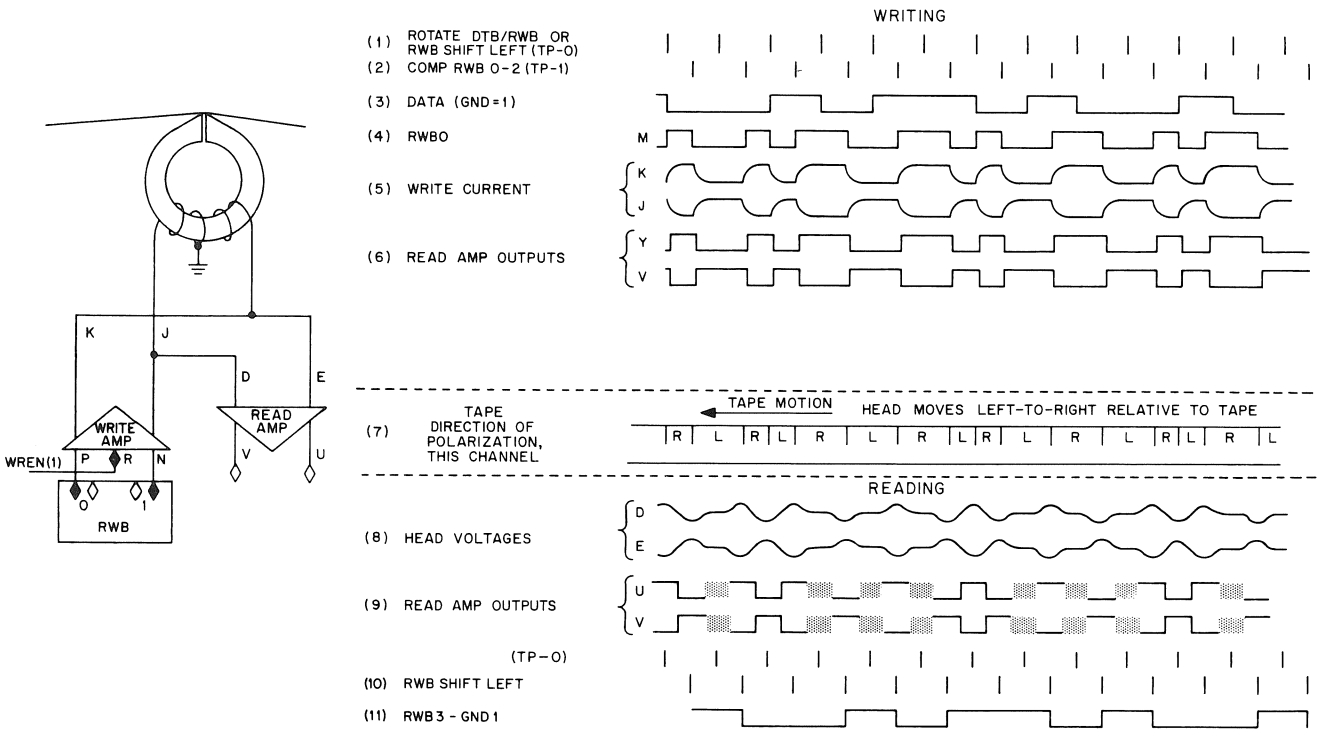


Figure 3-3 Read/Write Logic and Waveforms

In the two tracks corresponding to each channel on tape, information is recorded in a manner that makes read signals from the two head inductors reinforce on playback. The two inductors can be considered as a single head inductor whose winding is center tapped to ground, reading and writing in a single track.

When a write flip-flop contains 0, current flows from ground through the head inductor into K, and the polarization of the head core is oriented clockwise. The tape polarization, as the tape moves across the head, is oriented toward the left regardless of the direction of tape motion. Similarly, when the flip-flop contains a 1, tape polarization is oriented toward the right regardless of the direction of tape motion. When reading, the current induced in the head by a change in polarization flows opposite to the current required to cause the same change. Consequently, the current induced by a left-to-right tape polarization change is a current flowing out of the head toward pin E. The head is a source, and when a terminal is a current source, it is positive. Thus a left-to-right polarization change causes the read amplifier input E to be positive. Consequently, V is ground and U is negative. By the same reasoning, the left-to-right polarization change induces a positive signal at D and results in V being negative and U ground.

The Manchester recording system used in the control requires two pulses to write each bit in a channel. The first pulse, ROTATE DTB/RWB or RWB SHIFT LEFT, loads the write flip-flop with the value of the bit to be written. (See the timing diagrams, Dwg. No. D-TC02-0-15, (sheets 1 and 2) and Dwg. No. D-TC02-0-2. The second pulse, COMP RWB 0 through 2, complements the flip-flop. Depending on the state of the flip-flop, the ROTATE DTB/RWB pulse may or may not cause a polarization change on the tape. The RWB 0 through 2 pulse, however causes a tape polarization change

because as a complement input it changes flip-flop state. When reading, the value of a recorded bit is detected at the head inductor output as the polarization change passes over the head. The RWB 0-2 pulse produces a right-to-left polarization change when the flip-flop is loaded with 1, and produces left-to-right change when loaded with 0.

In Figure 3-3 the ROTATE DTB/RWB or RWB SHIFT LEFT and RWB 0-2 pulses alternate. The first pulse sets the flip-flop to the 1 level, the second complements. This relationship is shown in lines 1 and 2. Line 3 shows bits to be written, and line 4 shows flip-flop receipt of each bit. Line 9 shows direction of tape polarization. If the tape is read in the same direction as it is written, the tape positions corresponding to the time that the write flip-flop was complemented will show a right-to-left change on a 1, a left-to-right change on 0. The head voltages at read amplifier inputs E and D are shown in line 10, the read amplifier outputs on line 11. In reading, the shift pulses in line 12 for RWB coincide with those of line 2 (which complemented the write flip-flop in writing). The right-to-left polarization change representing a 1 results in ground at U at the time of the shift pulse. Consequently, line 13 shows a 1 shifted into the shift register as the first bit that is read.

If tape is read in the opposite direction to which it was written, the polarizations reach the head gap in reverse order; that is, the head senses a left-to-right change where a 1 was written, etc. The contents of the mark channel are selected to take advantage of this condition. Data written in one direction and read in the opposite direction will be complemented.

The read and write amplifiers are shown on Dwg. No. D-TC02-0-1. The READ T TRK and READ MK TRK read amplifiers produce timing and mark-track outputs. The associated write amplifiers are used only to format tape. The READ T TRK read amplifier also provides a SP input for generation of the UP TO SPEED signal (Dwg. No. D-TC02-0-10). The READ D0, READ D1 and READ D2 read amplifiers and corresponding write amplifiers on Dwg. No. D-TC02-0-1 produce the outputs necessary for transfer of data between associated RWB 0, 1, 2 bits and the DECtape.

3.3.2 Initialization Operations

Operations of the TC02 usually begin with a CNT n, FWD, GO, NM, SEARCH command. In addition to the operations involved in filling the command register (status A), certain other operations, such as initial time delay, are common to all DECtape functions.

3.3.2.1 I/O Bus Interface - The I/O bus interface for the TC02 is shown on Dwg. No. D-TC02-0-4. The logic by which IOPs from the computer are decoded to produce control and command signals are shown here, as well as the bus connections. IOPs are shown entering the control and being applied to W103 circuits for decoding and generation of command signals for TC02 logic.

Initially, two pulses are issued on the I/O bus, to provide CSTA to clear the status A register and I/O Power Clear to clear the status B register. I/O power clear is used to clear the registers when power is turned on or the program is restarted. CSTA is used to clear the register under program control.

3.3.2.2 Timing Pulse Generation (Dwg. No. D-TC02-0-10 and 15) - Timing pulses are required for both formatting the tape and for reading information from tape. During WRTM function, the T/M ENABLE level activates the clock and thus allows timing pulses TP0 and TP1 to be generated if the MCP switch is in the WRTM position. This position causes the WRTM/RDMK indicator (Dwg. No. D-TC02-0-9) to light and generates the SWTM level. This level is ANDed with MR1(1) and the WRTM level to produce TM/ENABLE, which starts the 120 kc clock.

On the positive transition of the clock pulse, the CK1 flip-flop is complemented. The positive transitions of the CK1 flip-flop complement the CK0 flip-flop. The outputs of CK1 and CK0 at location D28, result in generation of the 100 ns timing pulses TP0 and TP1 which occur alternately every 16.6 μs. The CK0(1) output also is applied to the timing track write amplifier at location C23 (Dwg. No. D-TC02-0-1) to produce the timing track pattern written on tape.

Timing pulse outputs also require the SWTM output from the MCP switch and the WREN level at location F15 and F19 to be true.

During the write function when the C2 flip-flop (Dwg. No. D-TC02-0-6) goes to zero, the negative transition sets the WREN flip-flop and generates WREN (1) output. The WREN flip-flop is reset again at C2(0) when any one of the ANDed inputs that is associated with the write functions is removed. This flip-flop allows a full data word to be written, even though one of the enabling level inputs have been removed before the end of a word has been reached.

Timing pulses TP0 and TP1 are generated during read operations when the UP TO SPEED (1) flip-flop is set at location D27, Dwg. No. D-TC02-0-10. The inverted output is gated with $\overline{\text{SWTM}}$ level, which is present when the MCP switch is in any position other than WRTM (Dwg. No. D-TC02-0-5). to provide a ground conditioning level to the DCD gates associated with the TP0 and TP1 power amplifiers. When the timing track signals READ TRK are received at location D22, the positive going pulses to the DCD gate, generates the timing signals.

The TP0 and TP1 outputs are applied as feedback to PA, location C10. The outputs of this power amplifier trigger a 10 μs delay during reading and writing data, producing a -3V output to inhibit any extraneous timing signals which may be generated as a result of cross talk between data and timing channels.

3.3.2.3 Tape Unit Selection (Dwg. No. D-TC02-0-7) - The unit select information USR 0-2 in status A register is decoded by the binary-to-octal decoder R151. A ground level on one of the eight outputs enables a SELECT level within the specified TU55 transport. The transport that is enabled by the grounded line responds to the transport control signals and connects its read/write heads to the head signal lines.

The USR 0, 1, and 2 stages of the status A register are set or held reset by the condition 1 or 0, respectively, from I/O bus 00, 01, and 02. The outputs of USR 0, 1, and 2 are displayed on the indicator panel via connector A-11 pins A, B, and C (Dwg. No. D-TC02-0-9). These outputs can also be sent back to the computer over the I/O bus under control of STA → IO bus pulse, which controls transfer of status A register content to the AC.

The binary-to-octal decoder S151 accepts the inputs from the three stages and provides the single grounded output on one of eight lines directly to W023, C32, which is the cable connector for the TU55 transports. (Refer to Logic Handbook, page 66 for complete circuit description and truth table analysis.)

3.3.2.4 Tape Motion Selection (Dwg. No. D-TC02-0-7) - Motion control information from the processor via the I/O bus is set into the status A register stages MT0 and MR1. The outputs of these two stages determine when the selected transport will be activated and the direction of tape travel. The outputs of MR0 produces either FWD (MR0(0)), or REV (MR0(L)). The logic is mutually exclusive so that only one direction signal can possibly be active at a given time.

Both direction signals can be inhibited by several conditions as shown on the logic. The X STA CLEAR STATUS A pulses at A-10 insure that no spurious direction signal will occur when the status A register is cleared. The MR1(0) and B XSA DY (delay) levels at the A-10 OR circuit insure that no direction signal changes occur during a stop operation or before the delay circuit output. The 0 output of BMR1 flip-flop also inhibits motion signals.

The BMR1 flip-flop controls STOP and GO generation by the condition of MR1. MR1(1) provides GO. MR1(0) resets BMR1 and produces STOP at A-09-N. The FWD, REV, STOP, GO signals are sent to the selected transport through C32 (Dwg. No. D-TC02-0-9).

3.3.3 Device Selection Logic

The device selector logic decodes the output of the memory buffer, bits 3 through 8, and generates IOT pulses (Dwg. No. D-TC02-0-4) used to initiate the status A and status B operations (X STA). Status A register is shown on Dwg. No. D-TC02-0-5.

The control operations, which are initiated by computer instructions and which involve status A register are shown on Dwg. No. D-TC02-0-4. These instructions are RSTA (read status A register), CSTA (clear status A register), and XSTA (load status A register). The status A instructions contain an octal 76 in bits 3 through 8 of the memory buffer register and are decoded by device selector W103, location EF11 on Dwg. No. D-TC02-0-4. RSTA at event time 2 (IOP2) is gated with the device selector to produce the 400 ns READ STATUS A pulse. The information on status A register (Dwg. No. D-TC02-0-7) consisting of unit select USR 0-2, motion control MR0 and 1, function register FR0-3, and ENI, enable interrupt, is gates with STA → I/O bus pulse (Dwg. No. D-TC02-0-3) locations D01 and D02 to produce I/O bus 00 through 99, which are loaded into the PDP-9 AC through connector EF01 or EF05.

Instruction Clear Status A is also decoded by the device selector W103 on D-TC02-0-4 and during event time 1. Pulse IOP1 is produced and gated with the decoded output to generate the 400 ns CLEAR STATUS A signal (CSTA). CSTA output produces the 0 → STATUS A at D15 to clear the status A register functions on Dwg. No. D-TC02-0-7, and the CXA pulse at location C18 Dwg. No. D-TC02-0-5. The positive going CXA pulse triggers the 5 μs delay at R302 providing a -3V XSA DY output for the duration of the delay. Clearing status A register selects tape unit 8 by the 000 configuration of the unit select register. The negative XSA DY level at location D23, Dwg. No. D-TC02-0-5,

holds both the STOP and GO levels ground (Dwg. No. D-TC02-0-7) to prevent a change of motion to tape unit previously specified. The positive going end of the XSA DY pulse jams the contents of MR1 into the BRM1 motion flip-flop (Dwg. No. D-TC02-0-7). Either the BRM1(0) output or MR1(0) pulse will provide a ground level at both the FWD and REV outputs of S107, preventing a direction change from occurring to insure that only the newly selected unit receives the new command.

IOT Load status A register is decoded at the device selector and gated with the IOP4 pulse at event time 3 to generate the 400 ns XSTA pulse (Dwg. No. D-TC02-0-4). The ground XSTA pulse output performs an exclusive OR function with the buffered accumulator outputs shown at locations D07 and D08 (Dwg. No. D-TC02-0-3) complementing the data in status A register when the buffered input level goes to ground at least 400 μs before the XSTA pulse is received. This permits specific information in the status register to be changed without affecting the remaining information.

The negative XSTA pulse is amplified by PA S603 (upper left of Dwg. No. S-TC02-0-7) to produce a negative XSAD pulse at S107 and a positive XSAD pulse at the amplifier output.

3.3.4 Status B Register and Skip Instructions

The status B register, Skip Error Flag, and Skip on DTF instructions are decoded by W103s shown on Dwg. No. D-TC02-0-4. These instructions are SEF (Skip on Error Flag), RSTB (Read status B), and SDTF (Skip on DECtape Flag). The SEF and SDTF occur at IOP1 time and the RSTB at IOP2 time.

The Skip pulse causes the program counter in the PDP-9 to be incremented by one and skip to the next sequential instruction.

When a programmed IOP2 pulse appears at event time 2, the RSTB 400 ns produces STB → I/O bus pulse which is a common pulse input to the NAND gates associated with modules shown on Dwg. No. D-TC02-0-3 that have inputs from status B register. A -3V level on any of the gate inputs indicates that an error exists, the DECtape flag is set, etc., and will result in ground outputs for loading into the PDP-9 AC or an OR transfer.

LDTB is generated during a DCH break to load the DECtape buffer (DTB) from memory. RDTB is generated during a DCH break to read the DECtape buffer (DTB) into the memory.

3.3.5 Interrupt Enable

Bit 9 of the AC determines the status of the ENI flip-flop (Dwg. No. D-TC02-0-7). This flip-flop enables (ENI(1)) or disables (ENI(0)) a program interrupt. The output of ENI(1) causes an interrupt request to be sent to the PDP-9 (Dwg. No. D-TC02-0- 16).

3.3.6 New Unit/Motion Select

The buffered accumulator outputs (Dwg. No. D-TC02-0-10) I/O bus 00(1) through -04(1), the unit selection and motion control bits, are sampled by the OR gate locations F17 and F16, to determine whether a new unit or motion has been specified. A ground level on any BAC0-4 input or at buffered memory bit BMB9(0), which indicates a change on bits 0 through 4, will result in a ground level NEW U+M output. This level allows the negative going CXA pulse (produced by XSTA, see

Dwg. No. D-TC02-0-5) to trigger the 120 ms U+M delay. The U+M(0) output from the delay sets the 70 μs RATE DY, which in turn sets the Up-to-Speed flip-flop, location D27. The output of the Up-to-Speed flip-flop, when reset, resets DATA SYNC. UP TO SPEED (1) enables TP ENABLE to allow the READ T TRK (0) inputs at location D22 to generate the timing pulse outputs TP0 and TP1. When the U+M delay is set (1), the negative output prevents the timing track pulses (SP) read from tape during the up-to-speed operation from triggering the RATE DY flip-flop. The SP signals (Dwg. No. D-TC02-0-1) are produced by the READ T TRK amplifier.

When the U+M delay is reset, the ground level output conditions the DCD gate to allow the first SP pulse to set the rate delay flip-flop. The ground level output of the rate delay conditions the DCD gate associated with the Up-to-Speed flip-flop, and thus allow the next SP pulse which occurs within a 70 μs interval (rate delay) to set the Up-to-Speed flip-flop and start the TC02 operations. The Up-to-Speed flip-flop is reset by the positive transition of the BRM1(0) level which indicates a stop motion, and by the ground output of the timing mark enable level (T/M ENABLE) generated at S107 location D22. Resetting this flip-flop produces a 0 → WINDOW pulse which clears the window register (Dwg. No. D-TC02-0-8) while the tape is not up to speed.

3.3.7 Counter Register

The Counter Register (location E15 Dwg. No. D-TC02-0-6) consists of three flip-flops used to control the blocks of information on the tape as shown on the timing diagrams of Dwg. No. D-TC02-0-15, Sheets 1 through 4. The outputs of the C0, C1 and C2 flip-flops provide a count of six for formatting a data word on tape and for the mark-track information. Initially the counter register is set to 100 by the (100) → C0-2 pulse (Dwg. No. D-TC02-0-15, Sheet 1) produced by the C-SYNC ground signal and the positive transition of TP0. This count presets the counter in synchronization with the tape and starts the first count of six. The count sequence is shown on Table 3-3 and Dwg. No. D-TC02-0-15.

Table 3-3
Counter Register Sequence

C0	C1	C2	TP0 Pulse
1	0	0	1 (C-SYNC - TP0)
1	0	1	2
0	0	0	3
0	0	1	4
0	1	0	5
0	1	1	6
1	0	0	7
1	0	1	8
0	0	0	9
0	0	1	10

Table 3-3 (Cont)
Counter Register Sequence

C0	C1	C2	TP0 Pulse
0	1	0	11
0	1	1	12
1	0	0	13
1	0	1	14
0	0	0	15
0	0	1	16
0	1	0	17
0	1	1	18

3.3.8 Window Register

The window register W1-9, shown on Dwg. No. D-TC02-0-8, location E29, F29, F30, F31, F32, provides temporary storage for the mark-track information read from tape during all tape functions except WRTM. At the start of the loading operations all flip-flops are cleared by the 0 → WINDOW pulse generated by resetting the Up-to-Speed flip-flop. When the tape is up to speed, the READ MK TRK information from the read heads conditions the DCD gates associated with W9 flip-flop, and the TP1 timing pulses then shift the mark-track information into the window register. The next TP1 pulse which appears after the W2 flip-flop is set, will set the W1 flip-flop which will remain set until cleared by the 0 → WINDOW pulse. The outputs of the window register are applied as inputs to six separate AND gates which decode the inputs and generate specific mark-track level outputs.

3.3.8.1 Counter Sync Level (C-SYNC) (Dwg. No. D-TC02-0-8) - Initially, when reading mark-track information either in forward or reverse, the first code to be recognized and used for synchronization is a result of the bit information formed by octal 525 or 725. This information appears after the reverse-end-mark codes sequence through the W-register. The bit configuration (Figure 3-4) are decoded by the C-SYNC gating logic (location F22), to produce a series of C-SYNC level outputs which condition the control register.

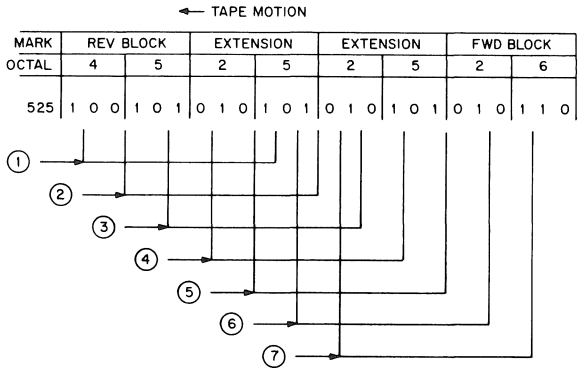


Figure 3-4 Mark-Track Decoding (C-SYNC)

The first code recognized by the C-SYNC gating appears at 1. These nine bits are decoded with the -3V output of S111, location F22, and generate the C-SYNC levels for all operations except write timing mark.

With two extension marks (E) inserted in the mark-track information, the C-SYNC signal will appear six times at the input to the AND gate and produce the C-SYNC level to reset the control clock. Only at the last decoding six, however, will the control clock initiate a count and synchronize the counter with the mark-track information.

3.3.8.2 Start Block Mark (MK BLK MK) (Dwg. No. D-TC02-0-8) - The next bit configuration in the W-register, which is recognized, is the forward or reverse block mark. This information appears during the next TP1 pulse after the C-SYNC level is generated, as shown on Table 3-4 and on timing diagram (Dwg. No. D-TC02-0-15, Sheet 1). The positive transition of the TP0 pulse which preceded the TP1 pulse sets the counter register to 101. The W-register information is gated with the $\overline{\text{WRTM}}$ level and the counter register outputs, C0(1), C1(0), and C2(1) to generate the C0-2(101) MK BLK MK outputs, as shown on Figure 3-5.

Table 3-4
Sequence of Block Marks and Control States

Event No.	Block Mark or State	Block Mark Code (Octal)
1	Tape stopped (ST IDLE(1))	
2	Start tape	
3	UP TO SPEED (1)	
4	C SYNC	725 or 525
5	DATA SYNC (1)	
6	C(101) · MK BLK MK	126
7	SHIFT STATE	
8	ST BLK MK (1)	
9	MK BLK START	210
10	SHIFT STATE	
11	ST REV CK (1)	
12	MK BLK START	010
13	SHIFT STATE	
14	DATA (1)	
15	MK DATA	070
16	MK BLK END	073
17	SHIFT STATE	
18	ST FINAL (1)	
19	MK BLK END	373
20	SHIFT STATE	

Table 3-4 (Cont)
Sequence of Block Marks and Control States

Event No.	Block Mark or State	Block Mark Code (Octal)
21	ST CK (1)	
22	C1(1)	
23	SHIFT STATE	
24	ST IDLE (1)	
25	Start at event number 6	126

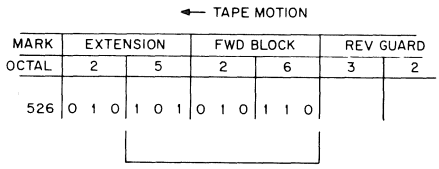


Figure 3-5 Mark-Track Decoding (MK BLK MK)

The octal 2 position of the reverse guard mark, in the forward tape direction, or octal 5 portion of the guard mark in the reverse tape direction is recognized together with the lock marks to generate the next mark-track signal MK BLK START as shown in Figure 3-6, and timing diagram (Dwg. No. D-TC02-0-15, Sheet 1).

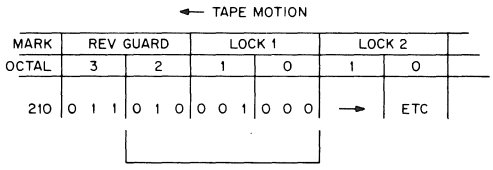


Figure 3-6 Mark-Track Decoding (MK BLK START -210)

The outputs from the W register, except for W2, are ANDed and inverted resulting in the MK BLK START outputs at location F15, Dwg. No. D-TC02-0-8. This occurs at the next 100 count of the control register as shown on the timing diagram. This lock mark is the first of four that are programmed on tape. Each will generate the MK BLK START levels. The bit configuration required for the next three lock marks are shown in Figure 3-7.

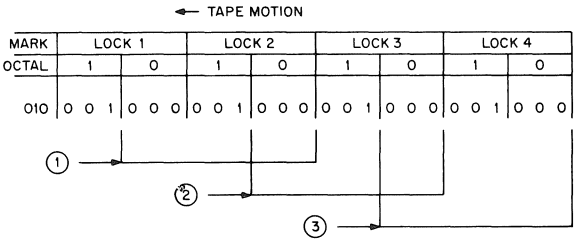


Figure 3-7 Mark-Track Decoding (MK BLK START-010)

The same AND gate which decoded 210_8 W-register configuration will decode the 010_8 and product the additional MK BLK START level.

3.3.8.3 Data Marks - The data mark follows the last lock mark and is decoded by AND gates R002 and S111, locations F20 and F24. The W-register configuration is shown in Figure 3-8.

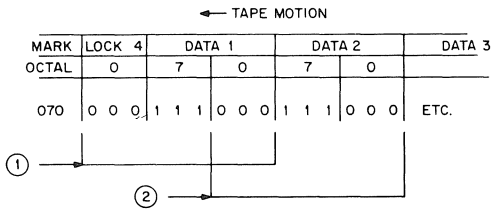


Figure 3-8 Mark-Track Decoding (MK DATA 070)

The -3V inputs are inverted and generate the MK DATA output levels as shown on timing diagram (Dwg. No. D-TC02-0-15, Sheets 1 and 2). After the last data mark has been decoded, AND gate (Dwg. No. D-TC02-0-9, locations E30 and E31) decodes an octal 073, and three octal 373s from the W-register to generate a series of four mark block end signals (MK BLK END), as shown on Figure 3-9 and timing diagram (Dwg. No. D-TC02-0-15, Sheet 2). This is accomplished by not decoding inputs from the W2 and W3 flip-flops.

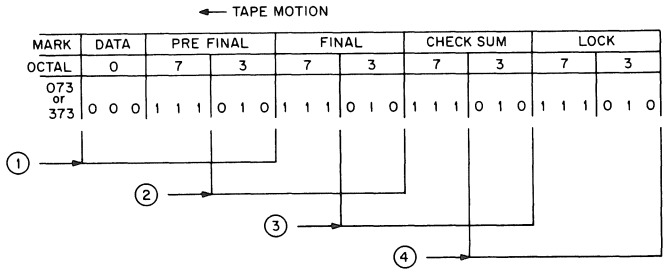


Figure 3-9 Mark-Track Decoding (MK BLK END)

The next two mark-track codes, guard mark (51) and block mark (45), which follow the lock mark, are not decoded and the decoding continues through the same sequence, as previously specified, until the end marks (222) are decoded by AND gate (location F19, 20 and 21, Dwg. No. D-TC02-0-8), which generates the MK END level.

3.3.9 State Register

The state register (Dwg. No. D-TC02-0-8, locations F26, 27, and 28) is a ring counter which indicates the control states of the TC02 as determined by the mark-track decoding sequence. The state register is cleared (forced to the ST IDLE (1)) each time the Up-to-Speed flip-flop is reset. The control states are sequenced through the state register by the positive transition of the SHIFT STATE pulses produced by monitoring both the decoded outputs of the mark-track and by the outputs of the state register at locations E21, F14, and F15. The outputs of the state register are connected to the MCP to provide a visual indication during DECtape operations. Table 3-4 lists in sequence the various block marks and control states that are generated. The first five events occur prior to the generation of the first SHIFT STATE pulse.

At event 6, the first block mark is decoded. The ground MK BLK MK level is inverted by S107 at location F15, and applied to another circuit of F15 to generate SH ST EN. This signal results in the first SHIFT STATE pulse at event time 7, which sets the ST BLK MK flip-flop. At event time 10, the mark-track decoded output MK BL START is gated with the -3V ST BLK MK (1) output and generates the second SHIFT STATE pulse. This pulse sets the ST REV CK flip-flop and resets the ST BLK MK flip-flop. The second MK BL START level produced by the mark-track decoding network is gated with the -3V output of ST REV CK flip-flop at location F14 to produce the third SHIFT STATE pulse at event time 13, which sets the Data flip-flop. The Data flip-flop remains set for all data words and until the MK BLK END level is decoded which allows the SHIFT STATE pulse at event time 17 to set the ST FINAL flip-flop. The second MK BLK END pulse is ANDed with the ST FINAL (1) output producing a SHIFT STATE pulse at event time 20, and sets the ST CK flip-flop. The ST CK (1) -3V output AND gated with the counter register output C1 (1) sets the ST IDLE flip-flop at event time 23, which allows the sequence of events starting at event time 6, to repeat for the next block.

3.3.10 Function Selection (Dwg. No. D-TC02-0-7)

The function command for the selected TU55 transport arrives over I/O bus 06 through 08, which are applied to the FR1-3 flip-flops of status A register. Stages FR1-3 constitute the function register.

The outputs of the function register are decoded by the binary-to-octal decoded S151 at location A-07 to provide one of the seven function levels used to select tape unit operations. This circuit produces a single ground level output on one of the selectable function lines shown on Dwg. No. D-TC02-0-7. The condition of the function register is displayed on the indicator panel via A-11 pins F, H, J, and K (Dwg. No. D-TC02-0-9). The outputs are also gated back over the I/O bus (Dwg. No. D-TC02-0-3) under control of STA → I/O bus pulse.

A description of the logical operations within the TC02 control for each function is described in the following paragraphs.

3.3.10.1 Move Tape (000) - The Move Tape function (MOVE), used to reposition or rewind tape, is implemented by a Load Status Register instruction, which specifies all zeros (0 → STATUS A) in the function register FR1-3. The Move function allows the tape unit selected to move in the direction specified by the motion register (MR0) until the tape end zone is detected, without allowing data transfers to occur.

The MR1(1) level from the motion register allows the BRM1 flip-flop (location C16) to be set at the end of the XSA DY delay and starts the tape motion in the direction specified by MR0. When up-to-speed is reached, the mark-track information is read from the tape. If no select error is detected, the tape motion continues and the mark-track information is read without effect on the operation until the end zone is detected. The decoded end zone generates a MK END level (Dwg. No. D-TC02-0-8), which allows the END flip-flop (Dwg. No. D-TC02-0-5) to be set by the TP0 timing.

3.3.10.2 Search (001) - The Search function is used to locate block numbers on tape. During this function, all information is read from the tape; however, only block numbers are transferred to the PDP-9 where the program performs a comparison of the information received with a specified block number to determine whether the two are the same.

The Search function is initiated by an octal 1 in the function register. When the transport comes up to speed, the timing track pulses READ TRK generate the TP0 and TP1 pulses (Dwg. No. D-TC02-0-10). The control operations performed are similar to the Read function. As shown on control drawing (D-TC02-0-6) the WREN(0) output allows the TP1 pulses to generate RWB SHIFT LEFT pulses, which assemble the information from tape in the RWB. The decoded mark-track information (Dwg. No. D-TC02-0-8) produces a series of C-SYNC levels, the last of which generates the first ROTATE DTB 00-11 and ROTATE DTB 12-17/RWB pulses and rotates the first bits of the block number into the DTB. More shift pulses are then generated at TP1 times to assemble the rest of the block number into the RWB, and the MK BLK MK signal is decoded to shift the state to ST BLK MK. At the C2(0) transition, another ROTATE DTB 00-11 and ROTATE DTB 12-17/RWB pulse load the DTB with the block mark information. Then a 1 → DF pulse (Dwg. No. D-TC02-0-6) is generated to set the data flag (generating a break request) by SEARCH, C0-2(101), and MK BLK MK. In the normal mode, the DTF flip-flop is also set to request a program interrupt to determine whether the block number transferred is the block number desired. In the continuous mode, the DTF is set only if a word count overflow (WC0) pulse is received.

Unless another function is specified, the control continues in the Search function, the mark-track decoding is performed and the data is assembled and shifted in the DTB and RWB. The 1 → DF pulse, which sets the data flag, will not be generated, however, until the next MK BLK is decoded.

During the ST REV CK state, the 0 → LPB and RWB $\forall$ LPB are generated for the parity computation. The parity has no significance, however, during search.

3.3.10.3 Read Data (010) - The Read Data function is normally performed after the program has searched and located the desired block number. Read data is specified by an octal 2 in the function register. After the Search function is completed, the control is normally in the ST BLK MK state. When mark-track information is decoded as a MK BLK START, the SHIFT STATE pulse (Dwg. No. D-TC02-0-8) changes the state to ST REV CK. During the previous states of the Search function, the ROTATE DTB to RWB and RWB SHIFT LEFT pulses were generated. No read data, however, was allowed to be transferred. The ST REV CK level enables the TP1 pulses to generate the 0 → LPB pulses (Dwg. No. D-TC02-0-6) to clear the LPB. The RWB ∀ LPB pulses, which exclusive ORs the 6-bit RWB information into the LPB (Dwg. No. D-TC02-0-2), are also produced during ST REV CK (1). This permits the reverse check word (the last 6 bits read) to be included in the parity computation. The state DATA is entered and the data is assembled and shifted by the RWB SHIFT LEFT and ROTATE DTB 00-11 and ROTATE DTB 12-17/RWB pulses as described in the read and write sequence. Each time ROTATE DTB 00-11 and ROTATE DTB 12-17/RWB pulses are generated, a RWB ∀ LPB pulse allows the parity computation to be performed.

If the WC register (Dwg. No. D-TC02-0-7, location 12) is set, indicating that a word count overflow has not occurred, the 1→DF pulse at the C2(0) transition will set the data flag (DF) requesting the interrupt request to transfer the word in the DTB to the PDP-9. When the request is granted the DCH GRANT pulse produces CLR DF to clear the DF.

This sequence continues until the end of the data portion of a block occurs, which is signified by the ST CK state. When the ST CK flip-flop is reset, the contents of the LPB should contain all ONEs or the parity error will be indicated by the LPB ≠↑ (Dwg. No. D-TC02-0-2) input which sets the PAR flip-flop. At this time, in the normal mode (FR0(0)), the ST CK (0) pulse will generate 1→DTF pulse to set the DTF flip-flop. In the continuous mode (FR0(1)), the DTF flip-flop will be set if a word count overflow had been issued during the previous data block. If the DTF flip-flop is set, the programs must specify a new operation. If it is not set, and the continuous mode is specified, the operation will continue as previously described. When a word count overflow occurs during the middle of a data block, the data transfers will stop.

3.3.10.4 Read All Functions (011) - The Read-All function, specified by an octal 5 in the function register, allows all information to be written in the data tracks on tape, including reverse check, block numbers, etc., to be read and transferred to the PDP-9 processor. Real all can be programmed initially or after a Search function that locates a specific block on tape before reading begins. When the tape has reached speed, only one C-SYNC level is required to set the DATA SYNC flip-flop, and the information on tape is read even though it may not be synchronized. This can occur in the middle of a data word on tape.

The operations within the DTB/RWB during the Read All function are similar to the operations which occur during the Read Data function. The RWB SHIFT LEFT pulses are produced at time TP1 enabled by the WREN(0) output to assemble the information into the RWB. The ROTATE DTB 00-11 and ROTATE DTB 12-17/RWB pulses then occur as C2(0) transition, causing the information in the RWB to be

transferred to the DTB. The same pulse transition also generates an RWB ∀ LPB pulse which allows the parity computation. TP1 pulses again produce RWB SHIFT LEFT pulses followed by another RWB V LPB pulse. At this time, the C0 (0) input will generate 1→DF pulse which sets the DF flip-flop, requesting a data break.

In the normal mode, with the FR0(0) ∧ RD +WD input applied, the 1→DTF pulse will also set the DTF flip-flop requesting the program to specify a new operation. Although the next word is not transferred, the setting of the data flag may result in a timing error requiring a new function to be specified or a similar operation to be performed. In the continuous mode with FR0(1), the DTF flip-flop is set when the WC0 pulse occurs from the PDP-9. The tape motion will continue, but no additional data transfers will occur.

During the Read-All function, although parity is computed, mark-track information is decoded, and the state register changes, these operations have no effect on data transfer.

3.3.10.5 Write Data Function (100) - The Write Data function is used to write data on tape in the data areas assigned by the mark-track coding. The Write Data function is normally initiated following a search operation which determines the block position on tape where the data will be written. The initialization process allows the tape to reach speed, the DATA SYNC flip-flop to be set, and the counter to be synchronized with the mark-track information. Specifying write data before the DATA SYNC flip-flop has been set will result in no operation.

When the Write Data function is specified after a Search function, the control is normally in the START BLOCK MARK state (Dwg. No. D-TC02-0-15, Sheet 1). The START BLOCK MK (1) level is gated with the decoded window register output MK BLK START level (Dwg. No. D-TC02-0-8, location F14) to generate a SHIFT STATE pulse which sets the ST REV CK flip-flop, changing the state of the control. Pulses 0→LPB and RWB ∀ LPB, a sequence of pulses will load and clear the LPB during the reverse check state. The reverse checksum which occurs one 6-bit word before the data state, however, will be included in the parity computation. Pulse 0→DTB, generated during ST REV CK(1) by C0(1) (Dwg. No. D-TC02-0-6) clears the DTB and generates 1→DF pulse at location C15, which sets the DF flip-flop and requests a data break. The ST REV CK(1) level is gated with the ST DATA (Dwg. No. D-TC02-0-6) to generate the WD EN level. This level allows the WREN flip-flop to be set and enable the data to be written. The WREN (1) output, gated with TP1 produces the first COMP RWB 0-2 pulse (Dwg. No. D-TC02-0-6, location D16), which is required for the write sequence (Dwg. No. D-TC02-0-15, Sheets 1 and 2). With the WREN (1) flip-flop set, the RWB SHIFT LEFT pulses are produced at the C2(1) transition (Dwg. No. D-TC02-0-6).

The sequence for the write operation is described in Paragraph 3.3.11. If a word count overflow has not occurred during the previous word, the data flag DF will be set each time the 0→DTB pulse is produced. If a word count overflow is issued during a previous word, the write sequence continues, but the DF flip-flop is not set with the result that all ZEROs are written in the remaining block on tape. (See DF flip-flop DCD gating input to set side shown (Dwg. No. D-TC02-0-6.)

At the end of a data block, the parity check character is loaded into the DTB by the LPB DTB0-5 pulse produced by the positive transition of the second MK BLK END (Dwg. No. D-TC02-0-15, Sheet 2), LPB DTB0-5 is produced by MK BLK END pulse enabled by ST FINAL(1), and WRITE DATA as shown on Dwg. No. D-TC02-0-6. The LPB information is written on tape in the checksum slot the same as a data word.

In the normal mode at the end of a data block, the positive transition of the ST CK (0) level will set the DTF flip-flop and, in the continuous mode, the same transition will also set the DTF flip-flop provided that a word count overflow WC(0) has occurred during the previous data block (see DTF gating, (Dwg. No. D-TC02-0-6). The writers are disabled after the parity is written by the WREN flip-flop, which is reset by the ground WD EN level that is produced when the data state is changed. The control continues to change states if DTF is not set and begins writing again in the block; the operations repeat in the same sequence.

3.3.10.6 Write All Function (101) - The Write All function specified by octal 5 in the function register, allows nonstandard formats to be written on tape, such as the insertion of block numbers or codes at unusual locations on tape.

This function can be preceded by the Search function, which determines the position on tape where the information will be written and can be implemented at any time after the tape has come up to speed (after only one C-SYNC level has been generated) which may cause the writing to be displaced by a half word.

The positive transition of the WRITE ALL level sets the W INH flip-flop as shown on Dwg. No. D-TC02-0-15, Sheets 3 and 4, and the logic of Dwg. No. D-TC02-0-6. This prevents the WREN flip-flop from being set and inhibits writing at this time. The timing sequence for the Write All function is shown on the timing diagram. The positive transition, when counter flip-flop C0 is set, will reset W INH flip-flop provided that the WC flip-flop was previously set. The 0→DTB pulse is also generated at this time resulting in a 1→DF pulse requesting a data break to write the first word.

If the Write All function is specified before the middle of the area assigned on tape for a data word, the first word will be written in the next data area which follows. If the function is specified after the middle of the current data word position, the next data word position will be skipped before the data word is written. The write sequence then continues. Parity is computed during this function, but the LPB→DB0-5 pulse which is required to write parity is not produced. The state register continues to shift but has no effect on the operation.

In the normal mode, the DTF(1) will generate an interrupt request when enabled by ENI(1) (see INT logic, Dwg. No. D-TC02-0-11). During the continuous mode, when a word count overflow occurs, the WC(0) level will set the DTF flip-flop. The WC(0) level, at this time, will also set the W INH flip-flop inhibiting the writing of future words on tape, but the tape motion will continue.

3.3.10.7 Write Timing and Mark Track (110) - The Write Timing and Mark-Track function is used to format a new tape by recording the timing and mark tracks prior to the recording of data.

This function is enabled only with the WRTM/RDMK/NORMAL switch on the TC02 control panel in the WRTM position and with the WRITE ENABLE/WRITE LOCK switch of the TU55 transport in the WRITE ENABLE position. The control panel switch generates a SWTM level which is gated with MR1(1) and the WRTM level to produce the TM ENABLE levels (Dwg. No. D-TC02-0-10). The TM ENABLE level activates the 120 kc clock, producing the CK1 and CK0 outputs which generate the TP0 and TP1 timing pulses. The CK0 and CK1 and TM ENABLE outputs are applied to the T TRK write amplifier (Dwg. No. D-TC02-0-10) to generate the pattern to be written on the timing track. The TM ENABLE level (Dwg. No. D-TC02-0-10) resets the Up-to-Speed flip-flop resulting in a 0 WINDOW level, which prevents mark-track information from being decoded (Dwg. No. D-TC02-0-8). It also resets the DATA SYNC flip-flop preventing synchronization of the control operations.

The WRTM and SWTM levels are gated with associated outputs to produce the WRITE SET level (Dwg. No. D-TC02-0-6). At the C0(0) transition, the WREN flip-flop is set and enables the data track amplifiers (Dwg. No. D-TC02-0-1) to write the information contained in the RWB. The first word that is written on tape, however, will be within the 10 ft of tape designated for the reverse end code and will not be read during the Read Tape function.

The WREN(1) level allows the RWB SHIFT LEFT pulse, the ROTATE DTB 00-11 and ROTATE DTB 12-17/RWB pulses, and the COMP RWB 0-2 pulses to perform the write operation as described in Paragraph 3.3.11. The WREN(1) at C0(1) transition (Dwg. No. D-TC02-0-15, Sheet 1) generates the 0→DTB pulse, which clears the DTB and sets the DF flip-flop requesting the first word.

The programming format for the mark track requires that the mark-track information appear in bits 0, 3, 6, 9, 12 and 15 of the data word. The information received by the mark-track write amplifiers (Dwg. No. D-TC02-0-1) is from RWB0 (Dwg. No. D-TC02-0-2). Therefore, the only data bits which appear in this buffer are bits 0, 3, 6, 9, 12 and 15. This information also appears in data track 1 on tape, which also receives information from RWB0.

When the WRTM function is completed, the TM ENABLE levels are held active by the SWTM and WREN(1) inputs. Enough TP0 pulses are produced to cause the C0(0) transition necessary to reset the WREN flip-flop and turn off the write amplifiers.

3.3.11 Read and Write Sequences

The sequence of events that occur during the Read and Write functions are summarized in Tables 3-5 and 3-6, respectively. The times of each event are specified in terms of control clock pulses and timing pulses TP1. Illustrations of the bit contents of the RWB and DTB section after each event has occurred are shown in the diagrams in the last column of the tables. The DTB and RWB registers are shown on Dwg. No. D-TC02-0-2 and D-TC02-0-11, respectively.

The events for the read operation in Table 3-5 are programmed to assemble an 18-bit data word in the DTB for subsequent transfer to the PDP-9 during a data break. At the start of the assembly, the first three bits 0 through 2 of the data word are strobed from the read amplifiers into the right half of the RWB. Bits 0 through 2 are then shifted left into the left half of RWB and the second three bits (3 through 5) of the data word are strobed into RWB3-5. Next, the first 6 bits of the 18-bit data word is

Table 3-5
Sequence of Events During Read Operation(1)

Event No.	Event	Time of Event	Initiating Input(2)	Resulting Operation(3)
1	Begin assembly of first 3 bits of data word	TP1 · C2(1)	RWB SHIFT LEFT (6C15)	First three bits from R/W amplifier outputs strobed into RWB 3-5. RWB: 0 1 2 3 4 5 Word Bits: x x x 0 1 2
2	Complete assembly of next 3 bits of data word	TP1 · C2(1)	RWB SHIFT LEFT (6C15)	Bits 0 through 2 shifted left to RWB 0-2 and bits 3 through 5 from R/W amplifier outputs strobed into RWB 3-5. RWB: 0 1 2 3 4 5 Word Bits: 0 1 2 3 4 5
3	Perform parity check of first 6 bits of data word. Rotate 6 bits of data word from RWB to DTB	C2(0) (i.e., transition from 1 to 0)	RWB ∀ LPB (6C13) ROTATE DTB 00-11 ROTATE DTB 12-17/ RWB (6C10)	Compute parity of RWB contents (i.e., bits 0 through 5). Rotate RWB 0-5 into DTB 12-17 DTB 0-5: x x x x x x DTB 6-11: x x x x x x DTB12-17: 0 1 2 3 4 5 RWB 0-5: x x x x x x
4	Begin assembly of next 3 bits of data word	TP1 · C2(1)	RWB SHIFT LEFT (6C15)	Word bits 6 through 8 from R/W amplifier outputs strobed into RWB 3-5. Contents of DTB same as in event 3. RWB: 0 1 2 3 4 5 Word Bits: x x x 6 7 8
5	Complete assembly of next 3 bits of data word	TP1 · C2(1)	RWB SHIFT LEFT (6C15)	Bits 6 through 8 shifted left into RWB 0-2 and word bits 9 through 11 from R/W amplifier outputs strobed into RWB 3-5. Contents of DTB same as in event 3. RWB: 0 1 2 3 4 5 Word Bits: 6 7 8 9 10 11

Table 3-5 (Cont)
Sequence of Events During Read Operation(1)

Event No.	Event	Time of Event	Initiating Input(2)	Resulting Operation(3)
6	Perform parity check of next 6 bits of data word Rotate contents of RWB and DTB (Repeat for last 6 bit segment of data word)	C2(0) transition from 1 to 0 COMP RWB	RWB ∀ LPB (6C13) ROTATE DTB 00-11 ROTATE DTB 12-17/ RWB (6C10)	Compute parity of RWB contents (i.e., bits 6 through 11 in event 5). Rotate DTB 12-17 into DTB 6-11, and RWB 0-5 into DTB 12-17. DTB 0-5: x x x x x x DTB 6-11: 0 1 2 3 4 5 DTB 12-17: 6 7 8 9 10 11 RWB 0-5: x x x x x x
7	Transfer complete assembled word in DTB to PDP-9		1 DF	
8	Begin assembly of next 3 bits of data word	TP1 · C2(1)	RWB SHIFT LEFT (6C15)	Word bits 6 through 8 from R/W amplifier outputs strobed into RWB 3-5. Contents of DTB same as in event 3. RWB: 0 1 2 3 4 5 Word Bits: x x x 6 7 8
9	Complete assembly of next 3 bits of data word.	TP1 · C2(1)	RWB SHIFT LEFT (6C15)	Bits 6 through 8 shifted left into RWB 0-2 and word bits 9 through 11 from R/W amplifier outputs strobed into RWB 3-5. Contents of DTB same as in event 3. RWB: 0 1 2 3 4 5 Word Bits: 6 7 8 9 10 11
10	Perform parity check of next 6 bits of data word Rotate contents of RWB and DTB plus 1→DTF	C2(0) transition from 1 to 0 COMP RWB	RWB ∀ LPB (6C13) ROTATE DTB 00-11 ROTATE DTB 12-17/ RWB (6C10)	Compute parity of RWB contents (i.e., bits 6 through 11 in event 5). Request DCH transfer. Rotate DTB 12-17 into DTB 6-11, and RWB 0-5 into DTB 12-17 DTB 0-5: 0 1 2 3 4 5 DTB 6-11: 6 7 8 9 10 11 DTB 12-17: 12 13 14 15 16 17 RWB 0-5: x x x x x x

Table 3-6
Sequence of Events During Write Operation(1)

Event No.	Event	Time of Event	Initiation Input(2)	Resulting Operation(3)
1	Request data word	C0(1)· WREN(1)	0→DTB (6D7) 1→DF (6C2)	Clear data buffer and set DF flip-flop to request data word "n" from PDP-9. DTB 0-5: 0 0 0 0 0 0 DTB 6-11: 0 0 0 0 0 0 DTB 12-17: 0 0 0 0 0 0 RWB 0-5: last 6 bits of word "n-1"
2	Data word "n" transferred from PDP-9 to DTB	Asynchronous with TC02	LTDB	18-bit data word "n" transferred to DTB. DTB 0-5: 0 1 2 3 4 5 DTB 6-11: 6 7 8 9 10 11 DTB 12-17: 12 13 14 15 16 17 RWB 0-5: last 6 bits of word "n-1"
3	Rotate contents of RWB and DTB and write bits 0 through 2 of word "n"		ROTATE DTB 00-11 ROTATE DTB 12-17/ RWB	DTB 0-5 rotated into RWB 0-5, DTB 6-11 into DTB 0-5, and DTB 12-17 into DTB 6-11 RWB 0-2 provides bits 0, 1, 2 as inputs to write amplifiers. DTB 0-5: 6 7 8 9 10 11 DTB 6-11: 12 13 14 15 16 17 DTB 12-17: x x x x x x RWB 0-5: 0 1 2 3 4 5
4	Complement bits 0 through 2 and write complemented bits Computes parity of bits 0 through 5 of word "n"	TP1· WREN(1)	COMP RWB 0-2(6D5) RWB ⊻ LPB (6B3)	Complement contents of RWB 0-2 to provide complement bits $\overline{0}, \overline{1}, \overline{2}$ as inputs to write amplifiers. Contents of DTB remain same as in event 3. RWB 0-5: $\overline{0}$ $\overline{1}$ $\overline{2}$ 3 4 5 Compute parity of RWB contents (i.e., bits 0 through 5) at end of event 3.

Table 3-6 (Cont)
Sequence of Events During Write Operation(1)

Event No.	Event	Time of Event	Initiating Input(2)	Resulting Operation(3)
5	Shift contents of RWB to left and write RWB bits 3-5	C2(1)· WREN(1)	RWB SHIFT LEFT (6B7)	Contents of RWB 0-5 shifted left and bits 3,4,5 provided as inputs to write amplifiers. Contents of DTB remain same as in event 3. RWB 0-5: 3 4 5 x x x
6	Complement bits 3 through 5 and write complemented bits. (Repeat from event 3 to write next 2 groups of 6 bits for a complete data word)	TP1· WREN(1)	COMP RWB 0-2 (6D5)	Complement contents of RWB 0-2 to provide complement bits 3,4,5 as inputs to write amplifier. Contents of DTB remain same as event 3. RWB 0-5: $\overline{3}$ $\overline{4}$ $\overline{5}$ x x x
7	Request next data word	C0(1)· WREN(1)	0→DTB (5D8) 1→DF (5D2)	Clear data buffer and set DF flip-flop to request data word "n+1" from PDP-9. DTB 0-5: 0 0 0 0 0 0 DTB 6-11: 0 0 0 0 0 0 DTB 12-17: 0 0 0 0 0 0 RWB 0-5: 12 13 14 15 16 17
8	Data word "n+1" transferred from PDP-9 to DTB	Asynchronous with TC02	LTDB	18-bit data word "n+1" transferred to DTB. "n+1" bits DTB 0-5: 0 1 2 3 4 5 DTB 6-11: 6 7 8 9 10 11 DTB 12-17: 12 13 14 15 16 17 "n" bits RWB 0-5: 12 13 14 15 16 17

accumulated in the LPB. At the same event time the first 6 bits of the data word from the RWB rotate into the DTB 12-17. The same sequence is followed to strobe two more groups of six bits through the RWB and to perform a parity check on them. The 18-bit word is completely assembled in the DTB and is ready for transfer to the PDP-9.

The read sequence in the following table is assumed to start at the reading of a word in the middle of a data block. The numeral-letter-numeral designations indicate the location of an initiating input on an engineering drawing contained in Chapter 6.

The events for the write operation in Table 3-6 are programmed to request an 18-bit data word from the PDP-9, store it temporarily in the DTB, and transfer it in 3-bit segments to the write amplifiers. The first six bits of the 18-bit data word are stored in one section of the DTB (DTB 0-5), and the next six bits in DTB 6-11, and the final six bits in DTB 12-17. A rotation transfers six bits at a time into the RWB and makes the first three bits (0-2) available to the write amplifiers. Each 6-bit group of the data word is included in the accumulated parity check to be written at the end of the block. In addition, bits 0 through 2 are complemented and supplied to the write amplifiers. Then the contents of RWB are shifted left so that bits 3 through 5 replace bit 0 through 2 in RWB 0-2. Bits 3 through 5 are now available to the write amplifiers in normal and complement form in the same manner as bits 0 through 2.

3.3.12 Longitudinal Parity Buffer Operation

The longitudinal parity buffer (LPB) (Dwg. No. D-TC02-0-2) performs the parity check of information in the data tracks. Essentially the parity check reads the number of binary ZEROs in each 6-bit group of data word bits and forms a parity bit, which is recorded in the checksum control word at the end of the data block. The checksum is computed by complementing the bits of the LPB when the respective bit of the RWB is a 0. The LPB register outputs are gated as shown on Dwg. No. D-TC02-0-3 to produce the LPB=1 and LPB$\neq$1 levels. If all LPB register flip-flops are not set during a read data operation, the LPB$\neq$1 level will set the parity flip-flop PAR (Dwg. No. D-TC02-0-5) indicating that a parity error has occurred.

At the end of a write data operation, the contents of the LPB is gated into DTB 0-5 to be written after the last data word.

The signals that control the LPB operations are defined in the following paragraphs and are produced by the logic shown on Dwg. No. D-TC02-0-6. The timing sequence for these signals are shown on Dwg. No. D-TC02-0-15, Sheets 1 and 2. The 0$\rightarrow$LPB pulse clears the LPB at the beginning of each block. Six pulses are generated by TP1 during the reverse check state, ST REV CK(1) to initialize the LPB register for computation of the parity character. However, only the last pulse is required for the operation. Note that one RWB $\forall$ LPB pulse is generated after the last 0$\rightarrow$LPB just as the data portion of the block is entered (in Read Data or Write Data). This is done to include the reverse checksum in the computation of the checksum for the entire block. This allows the tape to be read in the opposite direction from which it was written yet have the proper checksum.

The RWB → LPB pulse is used to perform the parity computation from the RWB to the LPB. The parity is computed at the same time ROTATE DTB 00-11 and ROTATE DTB 12-17/RWB pulses are generated during a read operation, and at the same time that the COMP RWB 0-2 pulse is produced during the write operation.

A LPB→ DTB 0-5 pulse is required at the end of the ST FINAL block to initiate the formation of a parity bit for recording the checksum control word at the end of the data block.

The enabling conditions used for the generation of the LPB→ DTB 0-5 pulse are a WRITE DATA level from the function decoder, and ST FINAL (1) level from the state counter. When a ground MK BLK END pulse from the mark-track decoding network appears at the gate S603, LPB→ DTB 0-5 pulse is produced. This pulse is transferred to the RWB register (Dwg. No. D-TC02-0-2) and DTB register bits 12-17 (Dwg. No. D-TC02-0-1) to gate information received from LPT 0(1) through LPB 5(1) into DTB.

3.3.13 Power Clear and Error Stop Logic

The power clear pulses (I/O PWR CLR) generated by the PDP-9 processor (Dwg. No. D-TC02-0-4) are inverted and applied to the PA (Dwg. No. D-TC02-0-5, location C2), with the EF signal to generate the PWR CLR + ES pulses. The EF signal is produced by monitoring the outputs of the error flip-flops MK TK (1), SEL(1), TIM(1), and END(1). When a (1) condition exists on any input to the NOR gate, as a result of an error, the EF level will be produced. The ground PWR CLR pulses are used to reset the DATA SYNC flip-flop, WREN flip-flop, DTF flip-flop, and the DF flip-flop when power is initially applied or removed from the PDP-9. In addition the ground PWR CLR + ES signal will continually set the U+M delay (Dwg. No. D-TC02-0-10) to prevent Up-to-Speed flip-flop from being set during the detection of an error or when the PWR CLR pulses are received.

3.3.14 Increment CA Inhibit (+1→ CA INH)

The +1→ CA INH signal (Dwg. No. D-TC02-0-16) is generated during the search function to prevent the incrementing of the current address. When the current address (CA) is not incremented, the block number is placed in core memory at the same location for each block number transferred.

3.3.15 Interrupt Request

The INT level (Dwg. No. D-TC02-0-16) from the control is used to initiate a program interrupt in the PDP-9 processor. The interrupt enable is determined by the status of the ENI flip-flop (Dwg. No. D-TC02-0-7). When ENI is set, either an error flag EF(1) input or DECtape flag DTF(1) will result in the request for an interrupt on the API or PI.

3.3.16 Error Flags (EF)

Five flip-flops (Dwg. No. D-TC02-0-5) produce error signals at the occurrence of any of the errors listed under the Status B functions. When a specific type of error occurs, the error detection circuits set the appropriate flip-flops to a 1 state.

The error input conditions that initiate a specific type of error signal are as shown on Figure 3-10. All error flip-flops are cleared by a ground pulse as shown on Dwg. No. D-TC02-0-5. These pulses are produced either by I/O PWR CLR or when an I/O BUS 10(0) level from the PDP-9 and a XOR STATUS (XSTA) pulse from the device selector appear simultaneously at the gate input.

When any error signal except PAR appears at one of the inputs to the NOR gate (Dwg. No. D-TC02-0-5, location D2), the gate produces an EF(1) output level. This output is used in forming the PWR CLR + ES signal. The same output is also passed through an inverter to produce an error flag EF(1) or EF(0) level. EF(1) and EF(0) levels are also provided when a PAR error signal appears at the input of an inverter.

The EF(1) level resulting from any of the error signals is passed through another inverter to produce a corresponding complementary EF(1) level. Ground level EF(1) serves as an input to the BEF flip-flop (Dwg. No. D-TC02-0-16) for generating an INT (Interrupt) level while the -3V EF(1) level is used as an input to a gate (Dwg. No. D-TC02-0-4) to generate SKIP RQ.

EF(1) and the set outputs from the error flip-flops enable inputs to the I/O BUS 00-05, and are pulsed onto the bus by STB I/O BUS, which is generated from the command RSTB (read status B register).

3.3.16.1 Mark-Track Error (MK TRK) - A MK TRK error signal is produced by MK TRK flip-flop (Dwg. No. D-TC02-0-5) when information read from the mark channel is in error. When MK TRK errors are detected by the input gating, the gating output enables the DCD input gate of the flip-flop. The ground C0(0) pulse from the control clock indicates that a 6-bit character has been read from the mark track and is in the window register. This C0(0) pulse sets the MK TRK flip-flop under certain enabling conditions.

One input to the MK TRK gating circuit represents one of four mark-track codes - MK BLK START, MK DATA, MK BLK END, MK END. These codes appear at times throughout reading of DECtape.

Other inputs to the gating circuit prevent MK TK error indications during a MOVE function and during the ST IDLE and ST BLK MK intervals. These intervals are indicated by -3V ST IDLE (0) and ST BLK MK (0) levels. The MK TK decodings are not valid during the ST IDLE and ST BLK MK intervals because the control may not be synchronized with the DECtape at these times.

3.3.16.2 Select Error (SEL) - A select error signal is produced by the SEL flip-flop (Dwg. No. D-TC02-0-5) when any of the select errors are detected. After the input gate is enabled by a select error condition, the flip-flop is set by a ground XSA DY pulse at the gate input.

The following conditions will result in setting the SEL flip-flop.

1. WRTM $\wedge$ $\overline{\text{SWTM}}$: MCP switch is not set on WRTM while PDP-9 program is attempting to write timing and mark data on new tape.
2. $\overline{\text{WRTM}}$ $\wedge$ SWTM: MCP switch is set on WRTM while the PDP-9 program has specified another function.
3. FR1(1) $\wedge$ $\overline{\text{WRITE OK}}$: DECtape transport control switch is set on WRITE LOCK while PDP-9 program is attempting to write.

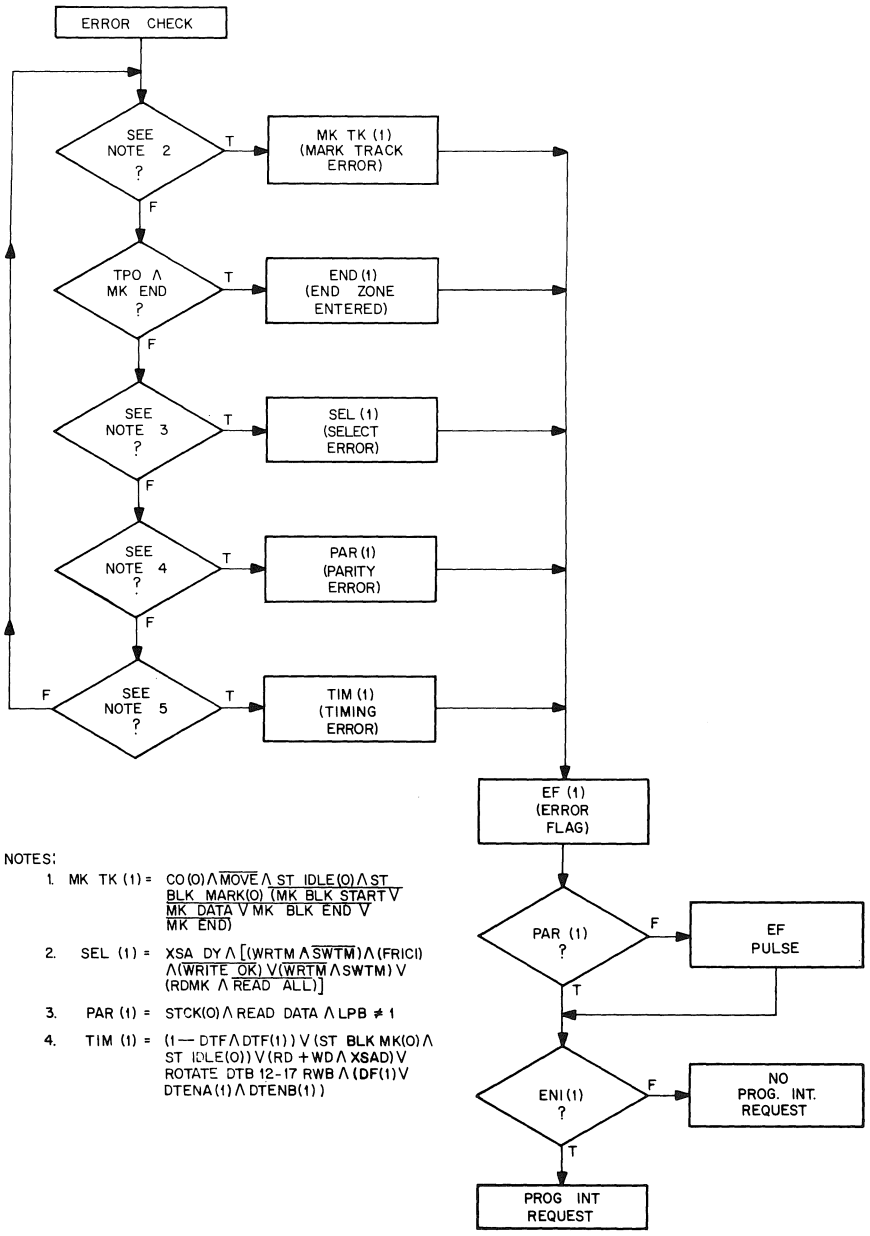


Figure 3-10 Error Check Flow Diagram

4. RD MK ∧ $\overline{\text{READ ALL}}$: MCP switch is set on RD MK but Real All function is not specified by the PDP-9.

In addition to the conditions listed, the single unit comparator circuits shown on Dwg. No. D-TC02-0-5 monitor the single unit line from the TU55 transports and generates a select error (SE) output if the line indicates either no units or more than one unit have been selected. This is effectively accomplished by noting the resistance of the Single Unit line and generating a ground select error level (SE) if the resistance is not within the specified limits.

With no units connected, the voltage at pins E and K of comparator W520 is -9V. The voltage at pin D and pin L is held constant at -7.5V and -5V, respectively, by the resistance network consisting of R1, R2, and R3. When this condition exists, pin D being more positive than pin E will cause a ground level SE output at pin H indicating a select error. When one unit is selected, the resistance of the line which is effectively in parallel with resistor R5, results in a voltage at pin K which is between the constant voltage at pin D of -7.5V and pin E of -5V. This voltage condition prevents the difference amplifiers from conducting, and the output at pin H and N will be -3V indicating a no-error condition. If more than one unit is selected on the line, the resistance in parallel with R5 will be decreased resulting in a voltage at pin K more positive than the -5V at pin L and the difference amplifier will conduct, resulting in a ground SE output at pin N.

3.3.16.3 Parity Error (PAR) - A PAR error signal is produced by PAR flip-flop during a Read Data function if the LPB check at the end of the data block does not equal 1. This condition enables the DCD gate to the flip-flop. Then a ground ST CK (0) pulse at the gate input sets the flip-flop. A ST CK (0) pulse occurs at the end of a data block.

3.3.16.4 Timing Error (TIM) - A timing error (TIM) is produced by the TIM flip-flop (Dwg. No. D-TC02-0-5) when any of the TIM error conditions listed in Table 2-4 are detected.

One operation that produces a timing error is to ROTATE DTB 12-17/RWB when a DF (1) exists as shown on Dwg. No. D-TC02-0-5. An error occurs because the data in DTB is no longer the same as it was at the instant the DF was set. The illegal operation is indicated to the TIM flip-flop when a ROTATE DTB 12-17/RWB ground pulse appears at the DCD input gate at a time when the gate is enabled by a DF (1) ground level. The error is also indicated in this way whenever DTENA (1) or DTENB (1) exists, when the ROTATE pulse arrives.

Another TIM occurs when a 1→DTF ground pulse appears at the input to the DCD gate of PA S603 at a time when this gate is enabled by a DTF (1) ground level. This illegal condition indicates that the TC02 is attempting to set the DTF at the end of a current operation, but that the program did not clear the DTF at the end of the last operation. The error is indicated to the TIM flip-flop by collector triggering the TIM (1) output with the ground level generated by the amplifier.

A third TIM occurs when -3V levels appear simultaneously at each input to the 4-input NAND gate (Dwg. No. D-TC02-0-5, location C3). This condition is illegal because it indicates that an attempt is being made to read data or write data (RD+WD) while passing over the data position on

the tape. The -3V ST BLK MK (0) and ST IDLE (0) input levels indicate that the head is not passing over the ST BLK MARK and ST IDLE blocks and therefore is passing over the data position. The -3V XSAD input is a standard 100 ns pulse which is generated 400 ns after receipt of an XOR STATUS A pulse. When all inputs to the NAND gate are -3V, the resulting ground level is used for collector triggering the 1 output of the TIM flip-flop.

3.3.16.5 End Error (END) - In normal operation the window register contains an end zone code (222) when the end zone of the DECtape is reached. At this time, the ground level at the window decoder output serves to enable the DCD input gate to the END flip-flop. When the next TP0 appears at the gate input, the flip-flop is set. A ground level at the 0 output of the END flip-flop indicates an error that is not expected by the program but is legitimate if used to indicate the end of a normal operation (e.g., rewind).

3.3.17 DECtape Flag (DTF)

The DECtape flag (DTF) network in the top center of Dwg. No. D-TC02-0-6 provides appropriate DTF output control levels which indicate the completion of specific operation.

DTF flip-flop is cleared by either collector triggering its 0 output with a ground level from NAND gate S123 (Dwg. No. D-TC02-0-4) or by the appearance of a PWR CLR ground pulse at the direct clear input. A ground level for clearing through the 0 output is provided when a -3V I/O BUS 11 (0) level from the PDP-9 and a -3V XSTA pulse appear simultaneously at the input to the NAND gate. When cleared, a ground 1→DTF pulse from one of three input gating circuits will set the flip-flop to a 1 state.

The inputs to gating circuit location C6 indicate the conditions listed below.

a. FR3 (1): selection of any one of the SEARCH, READ ALL or WRITE ALL functions by the function register.

b. WRTM: selection of WRTM function by function register.

c. FR0 (1): selection of CM of operation.

When a FR3 (1) or WRTM ground level and a -3V FR0 (1) level appear at the gating circuit input, with the DT ENB (1) and the I/O OFLO pulse, the resulting ground level provides the 1→DTF. This sets the DTF during CM and Search, Real All, Write All or WRTM.

One of the DCD input gates to PA S603 is enabled when a -3V WRTM + FR3 (1) and a -3V FR0 (0) (indicating NM) appear simultaneously at the inputs to the NAND gate. Then when a ground CLR DF pulse is applied to the DCD gate, the PA generates the desired 1→DTF pulse. This sets the DTF during NM and Search Read All, Write All or WRTM.

Another input gating network controls the generation of a 1→DTF pulse at the start of the parity check in the NM or CM. In the NM, either a ground level Read Data or Write Data input from the function decoder plus a FR0 (0) level input enables DCD gate 6C4. Then the appearance of a ground ST CK (0) from the state register at the start of the parity check causes the desired 1→DTF pulse to be generated. In the CM, an enabling input is applied to the DCD input gate when the RD + WD,

FR0 (1), and WC (0) inputs are at -3V. This sets the DTF at the end of the Data Block in Read Data or Write Data taking into account the NM or CM and WC0 to produce the DTF settings as defined earlier.

CHAPTER 4
INSTALLATION

This section contains general information on the installation and maintenance of the TC02 DECtape control. The installation procedures refer to a single cabinet installation of both TC02 control and two TU55 DECtape transports. Installation information for mounting additional TU55 transports or TC02 control in an existing cabinet is available upon request.

4.1 INSTALLATION PROCEDURES

The TC02 DECtape control and associated TU55 transports are shipped with the cabinet attached to the PDP-9, as a single unit cabinet mounted and crated, or as individual units to be installed in an existing cabinet. The installation information in this chapter refers primarily to cabinet mounted units as the requirements for separate units vary according to the needs of the specific system.

Upon receipt of the unit, an initial visual inspection should be performed to insure that no obvious physical damage has been incurred during shipment.

4.1.1 Site Preparation

No special site preparation is required for the installation of the TC02 unit. Adequate clearance must be provided for proper installation and for servicing. Figure 4-1 shows the installation dimensions required by the unit.

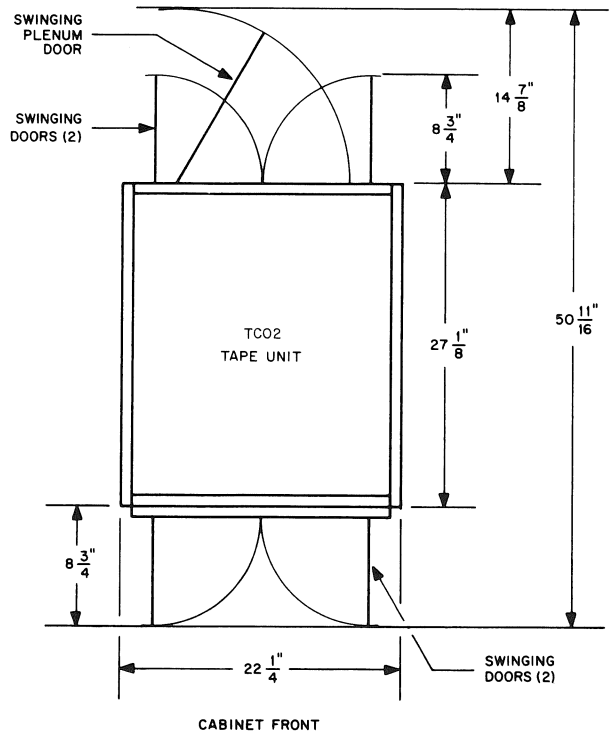


Figure 4-1 TC02 Unit Single Cabinet Installation Dimensions

When the cabinet is not physically attached to the PDP-9 console, both the power and signal cables enter through holes provided in the base of the cabinet. Casters are mounted on the cabinet base to enable the unit to be easily positioned and to allow sufficient clearance for the cables. No sub-flooring is normally required.

4.1.2 Environmental Conditions

The environmental conditions for the proper operation of the TC02 control unit are limited by the magnetic tape used with DECtape. The acceptable environmental conditions for the magnetic tape are an ambient air temperature between +60°F and +80°F with a relative humidity level between 40% and 60%. The TC02 DECtape control operating environment is the same as that required by the PDP-9 processor.

The installation site must also be as free as possible from excess dirt and dust, corrosive fumes and vapors, and strong magnetic fields.

4.1.3 Power and Cable Requirements

The TC02 control and associated TU55 transports operate from single phase line voltage of 105V to 125V, 60 cps. The maximum current requirement is dependent on the number of TU55 transports included in the system. The maximum current requirement for the TC02 control is 4A, and each transport requires approximately 2A maximum. A Hubble, 3-terminal, 220V twist-lock flush receptical rated at 30A with ground neutral should be installed near the site of the cabinet to allow connection to the power cable supplied.

Figure 4-2 shows the internal and external cable interconnections as viewed from the rear of the cabinet. All other interconnections between TC02 panel assemblies are facilitated by the panel wiring which is exposed to the front of the cabinet.

Panel locations EF01 through EF04 are connected by panel wiring to panel locations EF05 through EF08. This allows the interconnecting cables to the PDP-9 processor to be attached to the bottom of the TC02 unit and the cables to additional peripheral units to be connected next to these.

4.1.4 DECtape Signal Connectors

A description of the cable connectors are listed in the Digital Logic Handbook, Doc. No. C-105 by the identification number shown on the system drawings of Chapter 6.

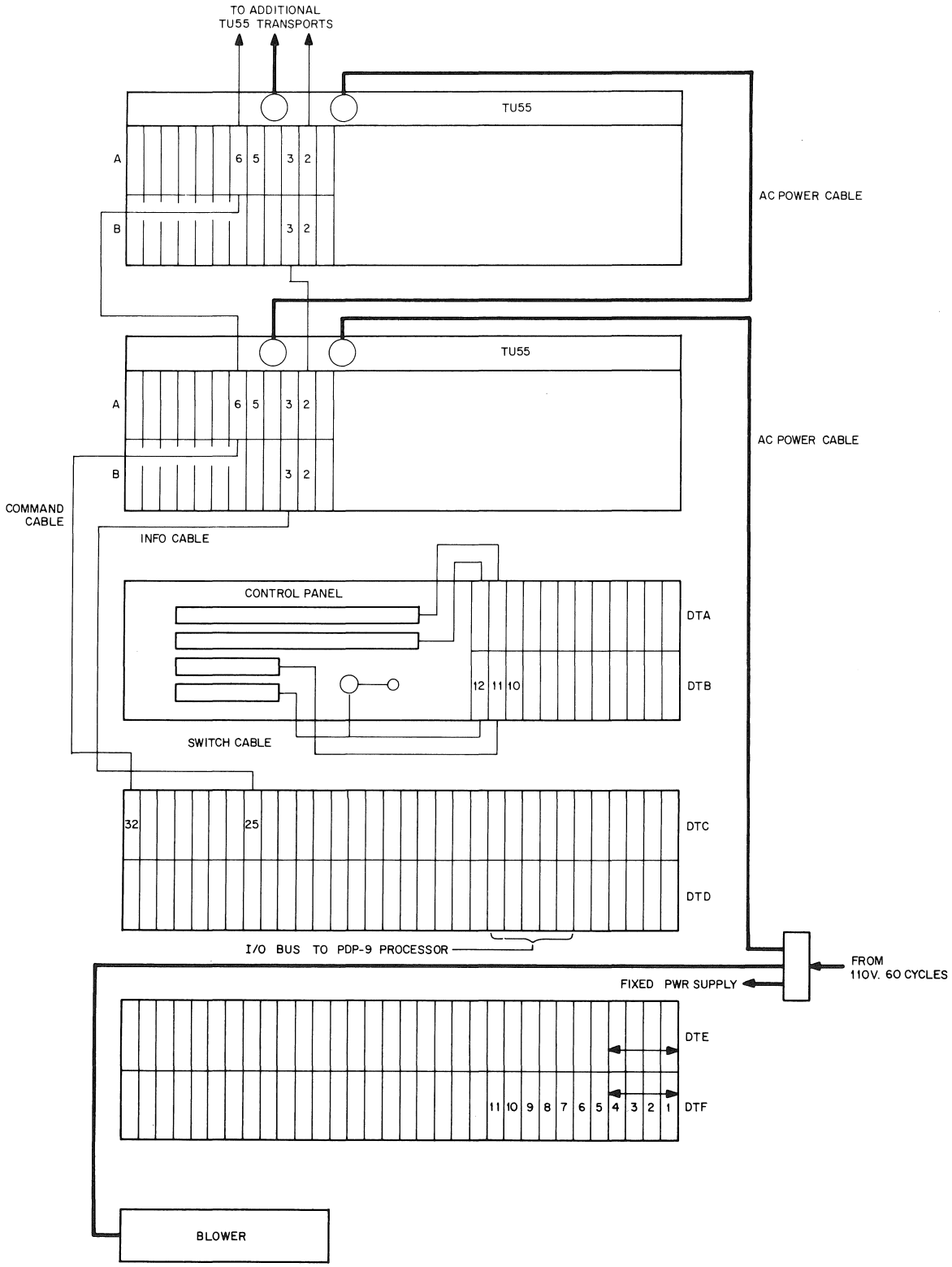


Figure 4-2 TC02 Control, Cable Diagram

CHAPTER 5
MAINTENANCE

The information contained in the following paragraphs is required for servicing the TC02 DECtape control. Information pertaining to the TU55 transport is contained in the TU55 DECtape Instruction Manual listed in Paragraph 1.4.

The maintenance procedures contain a description of the switches and indicators on the maintenance control panel and general preventive maintenance instructions. When used in conjunction with the PDP-9 operating program and the TC02 maintenance programs, the control panel provides a visual indication of the operating state and content of the TC02 control.

5.1 MAINTENANCE EQUIPMENT

Table 5-1 is a list of the equipment recommended for servicing the TC02 control in addition to the standard hand tools normally required.

Table 5-1
Maintenance Equipment

Equipment	Manufacturer	Model
Multimeter	Triplett or Simpson	630-MA or 260
Oscilloscope	Tektronix	Series 540 or 580, with Type CA differential amplifier or equivalent
Head Cleaner kit (8705)	Potter	P/N A 425 484
Variable Power supply	DEC	(from PDP-9)
Module extender*	DEC	W980
*Furnished with the PDP-9 Processor		

5.2 MAINTENANCE CONTROL PANEL

The maintenance control panel is located at the cabinet front, behind the access doors. The panel contains a switch used in the operation of the TC02 and indicators which display the status and information in the control.

Table 5-2 lists the function and panel designation of the switch and indicators shown on Figure 5-1. The number of indicators for each designation is enclosed in parenthesis.

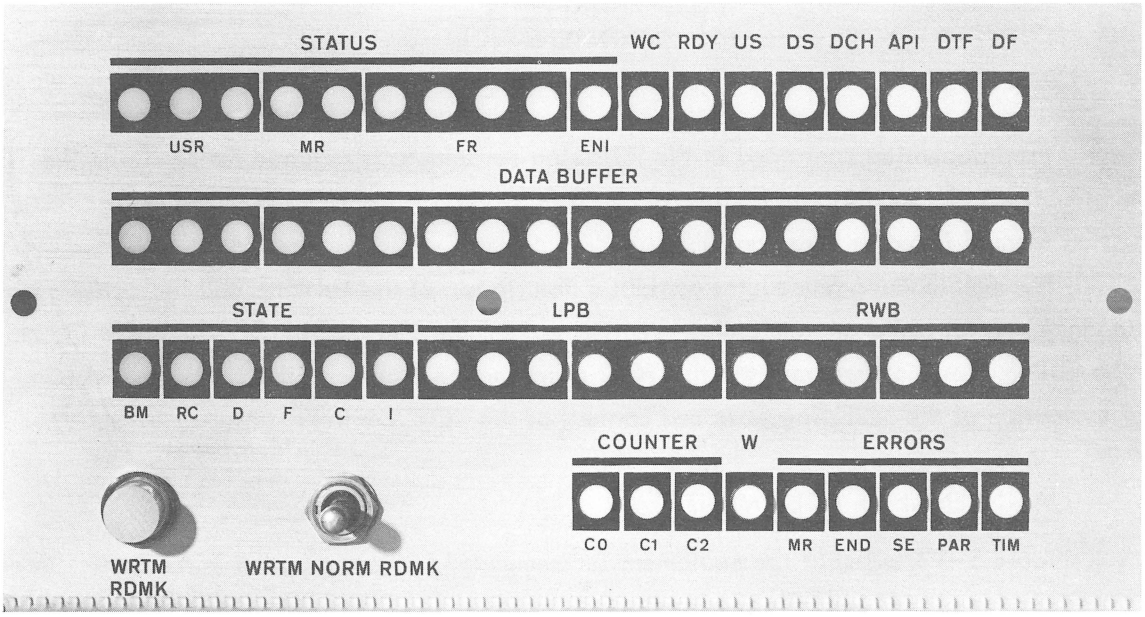


Figure 5-1 Maintenance Control Panels (Switch and Indicators)

Table 5-2
Switch and Indicators
(Maintenance Control Panel)

Designation	Function
STATUS (Indicators)	
USR (3)	Indicates the contents of the unit select register.
MR (2)	Indicates the status of the motion control registers which selects; stop, go, forward, reverse.
FR (4)	Indicates the contents of the function register.
	FR (0) Normal/Continuous Mode.
	FR (1-3) Octal code of the selected function.
ENI (1)	Lights to indicate that the TC02 is enabled to the PDP-9 program interrupt.
US (1)	Lights to indicate that the selected TU55 transport has reached the required speed for reading or writing.
ERRORS (Indicators)	
MR (Indicator)	
(1)	Lights to indicate that a mark-track error has been detected.
END (Indicator)	
(1)	Lights to indicate that the end of tape has been detected.

Table 5-2 (Cont)
Switch and Indicators
(Maintenance Control Panel)

Designation	Function
SE (Indicator)	
(1)	Lights to indicate that a function select error, or no transport selected, or more than one transport selected.
PAR (Indicator)	
(1)	Lights to indicate that a parity error has been detected.
TIM (Indicator)	
(1)	Lights to indicate a program timing fault.
STATE (Indicators)	
BM (1)	Lights to indicate that the Block Mark state is activated.
RC (1)	Lights to indicate that the Reverse Check state is activated.
D (1)	Lights to indicate that the Data State is activated.
F (1)	Lights to indicate that the Final State is activated.
C (1)	Lights to indicate that the Check State is activated.
I (1)	Lights to indicate that the Idle State is activated.
DATA BUFFER (Indicators)	
(0-2)(3-5)(6-8)(9-11) (12-14)(15-17)	Indicates the content of the data buffer register.
RWB (Indicators)	
(0-2)(3-5)	Indicates the content of the read/write buffer register.
DTF (Indicator)	
(1)	Lights to indicate that the DECtape flag is set.
DF (Indicator)	
(1)	Lights to indicate that a data flag is set requesting a data break.
W (Indicator)	
(1)	Lights to indicate that the write enable level is activated.
LPB (Indicators)	
(0-2)(3-5)	Indicates the content of the longitudinal parity buffer.
COUNTER (Indicators)	
C0, C1, C2	Provides indication of the count function of the counter register used for mark-track decoding.
DCH (Indicator)	Lights during DCH request.
API (Indicators)	Lights during API request.
US	Up-to-Speed flip-flop
DS	Data Sync flip-flop

5.3 DEC MODULES

The standard DEC modules used on the TC02 control are described in Digital Logic Handbook Doc. No. C-105 except for modules described in the following paragraphs. One spare module of each type is generally recommended to facilitate maintenance of the TC02 control.

5.3.1 Module Locations and Complement

The position of the modules within the mounting panels, as viewed from the wiring side, is shown on the Module List Drawings of Chapter 6. Each module is represented by a rectangle with the module type designation at the top. Each rectangle in turn is subdivided to show the circuits that are contained on the module. In general, the circuits are identified by the logic signal(s) available at the circuit outputs.

Table 5-3 lists the type and quantity of modules used in the TC02.

Table 5-3
TC02 Module Complement

Number Required	Type	Description	Revision
3	G853	Speed and Unit Circuit	
5	G882	Manchester Read/Write Amplifier	D
12	R002	Diode Network	A
5	R113	Diode Gate	B
3	R201	Flip-Flop	D
1	R302	Delay (One-Shot)	S
2	R303	Integrating One-Shot	
1	R401	Variable Clock	M
9	S107	Inverter	D
9	S111	Diode Gate	D
9	S123	Diode Gate	
2	S151	Binary-to-Octal Decoder	C
21	S202	Dual Flip-Flop	D
3	S203	Triple Flip-Flop	C
11	S205	Dual Flip-Flop	D
4	S602	Pulse Amplifier	H
7	S603	Pulse Amplifier	E
4	W018	Connector Board	A
3	W103	PDP-9 Device Selector	D

Table 5-3 (cont)
TC02 Module Complement

Number Required	Type	Description	Revision
2	W104	PDP-9 I/O Bus Module	
3	W107	High Impedance Follower	A
1	W520	Comparator	B
8	W850	I/O Cable Connectors	A

5.3.2 Circuit Description

The following circuit description is provided to supplement the information in the Digital Logic Handbook C-105, and the circuit diagrams of the modules of the system follow.

MANCHESTER READER/WRITER G882 (Figure 5-3)

The Manchester Reader/Writer G882 is a standard size FLIP CHIP module for use in reading and writing one channel of Type TU55 DECtape. Each module contains two write amplifiers and one high-gain differential read amplifier. The read amplifier saturates with a 1 mV input.

Module Characteristics

The terminals for the module are shown in Figure 5-3. The input and output characteristics are as follows.

Reader Inputs E, D - are differential signals centered at ground. The input impedance is approximately 400 ohms to ground. A nominal input signal is a sine wave between 5 kc and 30 kc.

Reader Outputs U,V - are standard DEC levels of -3V and ground. The outputs can drive 10 mA of load at ground.

Writer Inputs - N, R, and P are standard DEC levels of -3V and ground. The input load of 2 mA is shared by the inputs at ground level.

Writer Outputs - J and K, are nominal 180-mA current pulses from ground to -15V. The power requirements of the module are +10(A)/18 mA and -15(B)/235 mA. The marginal check limits in both cases are ±20%.

Both the reader and the writer circuits are returned to a common C, F ground.

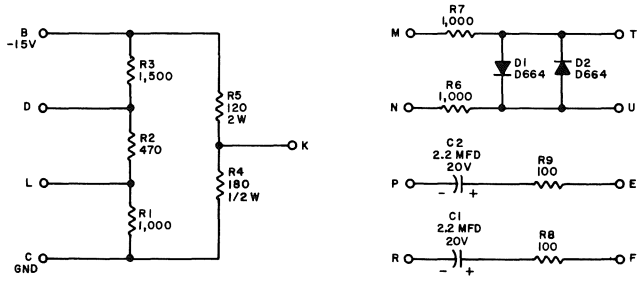
5.3.3 Module Replacement Procedure

When necessary to remove modules, the procedure is as follows.

a. Turn off all power to the Type TC02 DECtape Control.

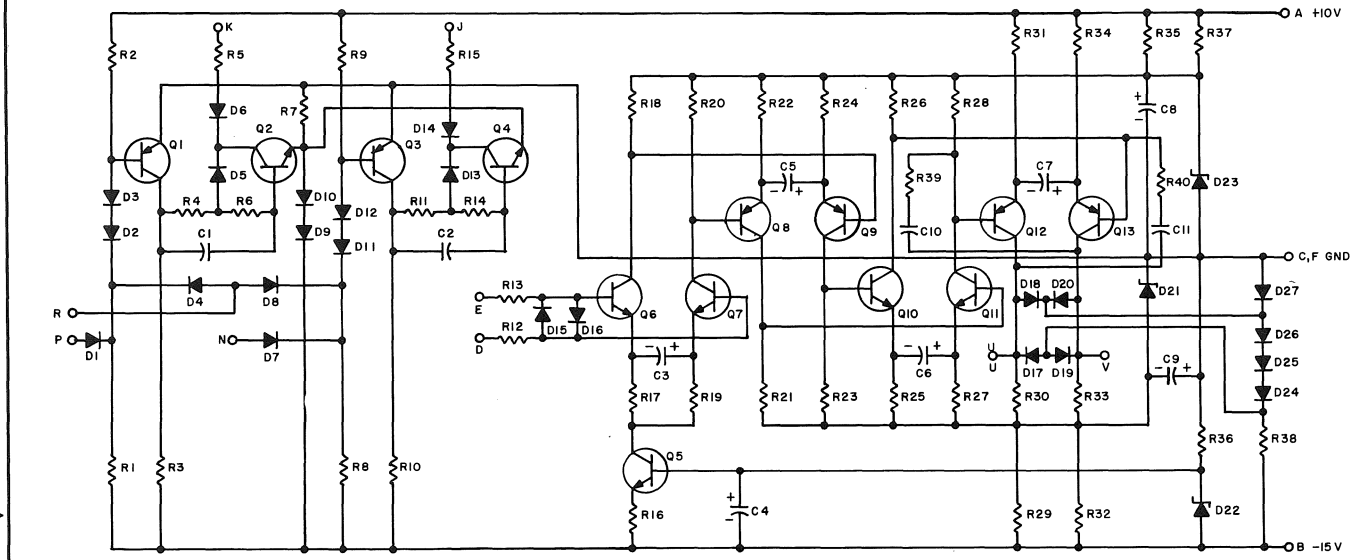
b. Gently pull the module from the mounting panel. Use a straight even pull to avoid damage to plug connections and the printed-wiring board.

Access to adjustment controls on the module or access to signal tracing points can be gained by removing the module, connecting a Type W980 Module Extender into the mounting panel, and inserting the module into the extender.



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%

Figure 5-2 G853 Speed and Unit Circuit



Q8, Q9, Q12, Q13	TRANSISTOR DEC3638B	1502979
Q6, Q7, Q10, Q11	TRANSISTOR DEC3009B-S	1503100
Q5	TRANSISTOR DEC3009A-S	1501999
Q2, Q4	TRANSISTOR DEC3500-S	1503209
Q1, Q3	TRANSISTOR DEC2894-3B-S	1503099
R39	RES. 120 1/4W 5% CC	1300247
R36, R38	RES. 470 1/2W 10% CC	1300318
R30, R33 R17 THRU R21, R23, R25 THRU R28,	RES. 3K 1/4W 5% CC	1300432
R12, R13	RES. 220 1/4W 5% CC	1300271
R6, R14, R35, R37	RES. 560 1/4W 5% CC	1301890
R5, R15	RES. 68 2W 5% CC	1302308
R4, R11	RES. 750 1/4W 5% CC	1301401
R3, R7, R10, R16, R22, R24, R29, R31, R32, R34	RES. 1.5K 1/4W 5% CC	1300391
R2, R9	RES. 100K 1/4W 5% CC	1302466
R1, R8	RES. 7.5K 1/4W 5% CC	1301422
D23	DIODE 1/4M 6.8AŽ	1100102
D22	DIODE IN748 3.9V	1100121
D21	DIODE IN756A 8.2V	1103441
D5, D6, D13, D14	DIODE D670	1102162
D2, D3, D11, D12, D24 THRU D27	DIODE D662	1100113
D1, D4, D7 THRU 10, D15 THRU D20	DIODE D664	1100114
C10, C11	CAP. 1,200MMF 100V 5% D.M.	1002430
C5	CAP. 2.2MFD 20V 10%	1002627
C4, C6, C7, C8, C9	CAP. 3.9MFD 10V 10% S.TANT	1000084
C3	CAP. .47MFD 20V 10% S.TANT	1005965
C1, C2	CAP. 680MMF 100V 5% D.M.	1000026
	PARTS LIST	A-PL-G882-0-0
REFERENCE DESIGNATION	DESCRIPTION	PART NO.

PARTS LIST

PINK DIST. 324 434 435 359

Figure 5-3 G882 Manchester Read/Write Amplifier

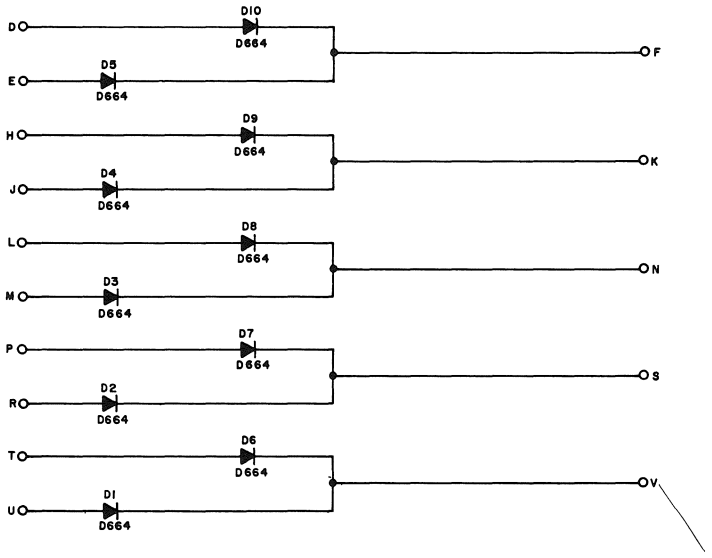


Figure 5-4 R002 Diode Network

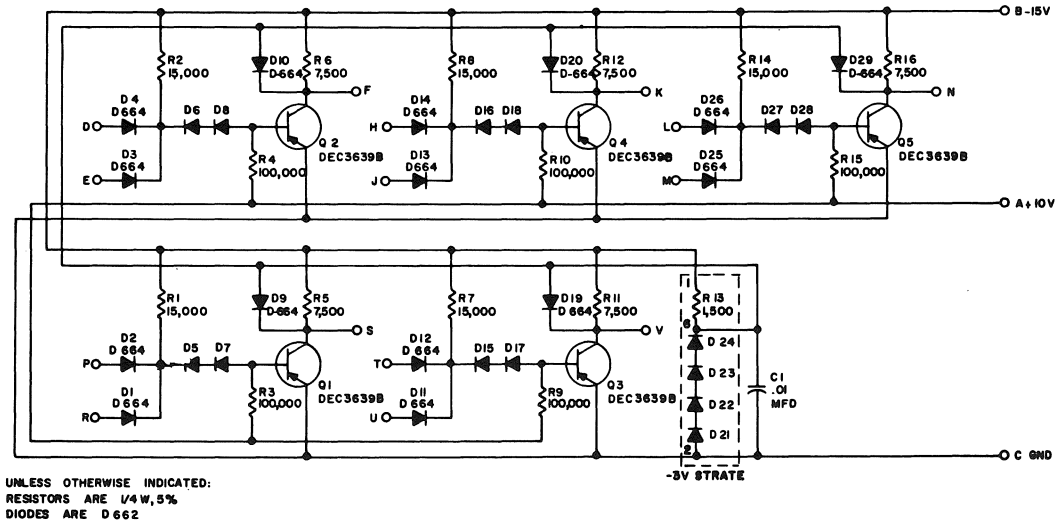


Figure 5-5 R113 Diode Gate

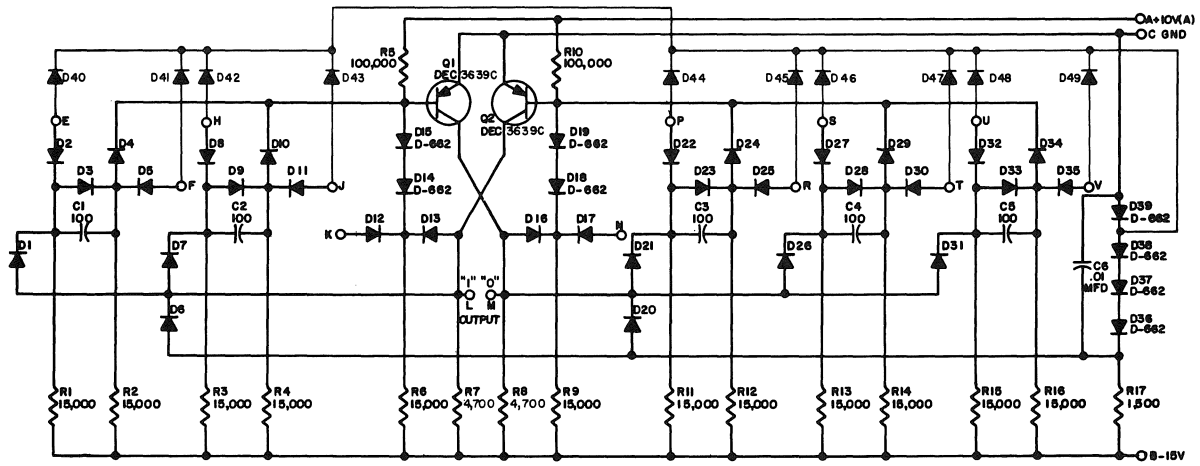


Figure 5-6 R201 Flip-Flop

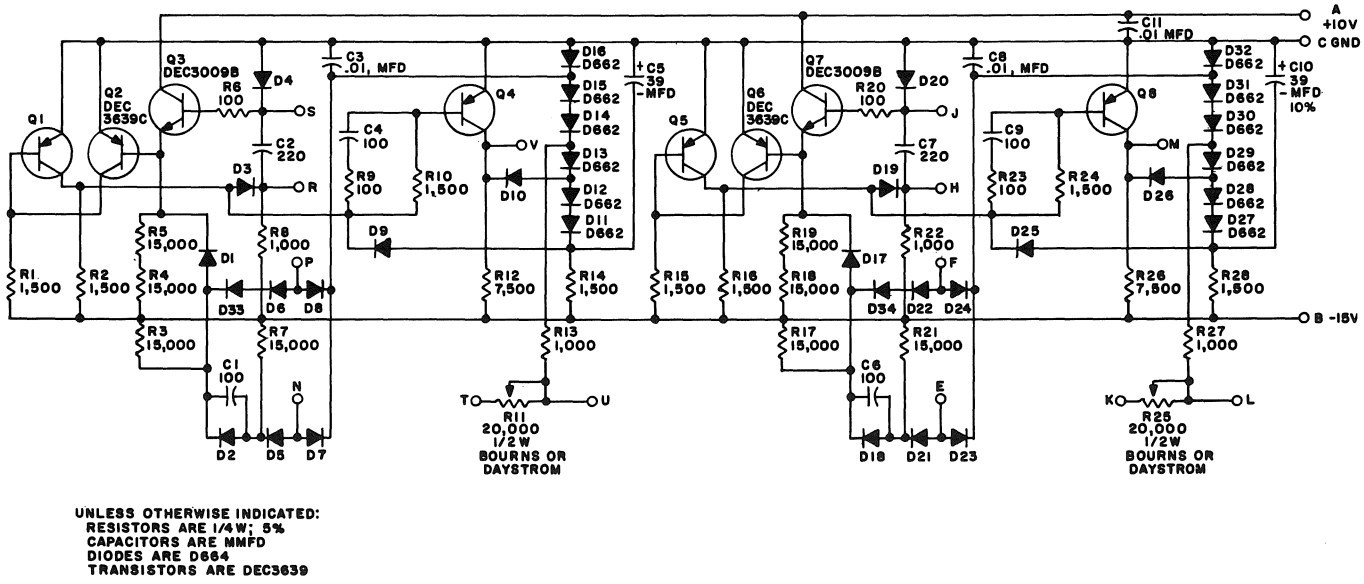


Figure 5-7 R302 Delay (One-Shot)

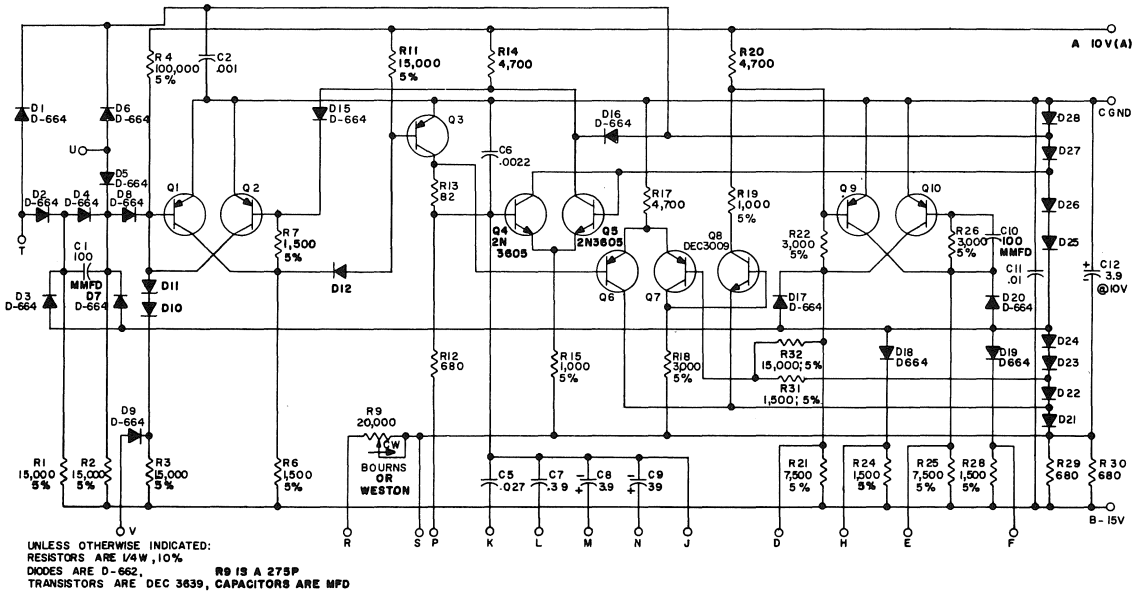


Figure 5-8 R303 Integrating One-Shot

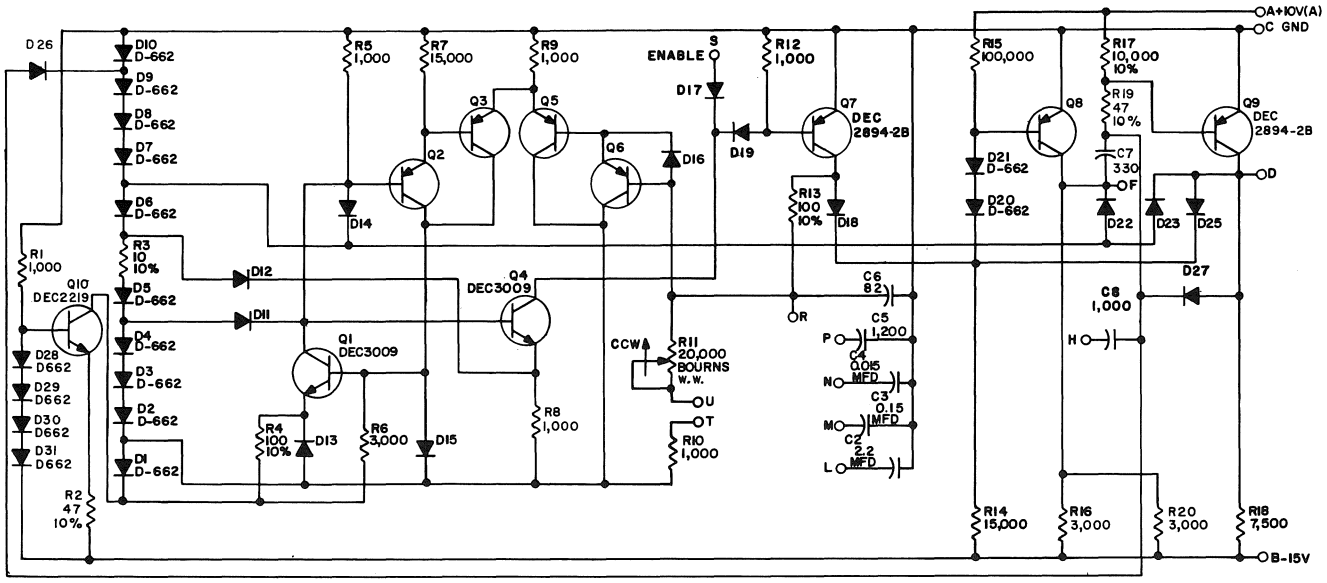
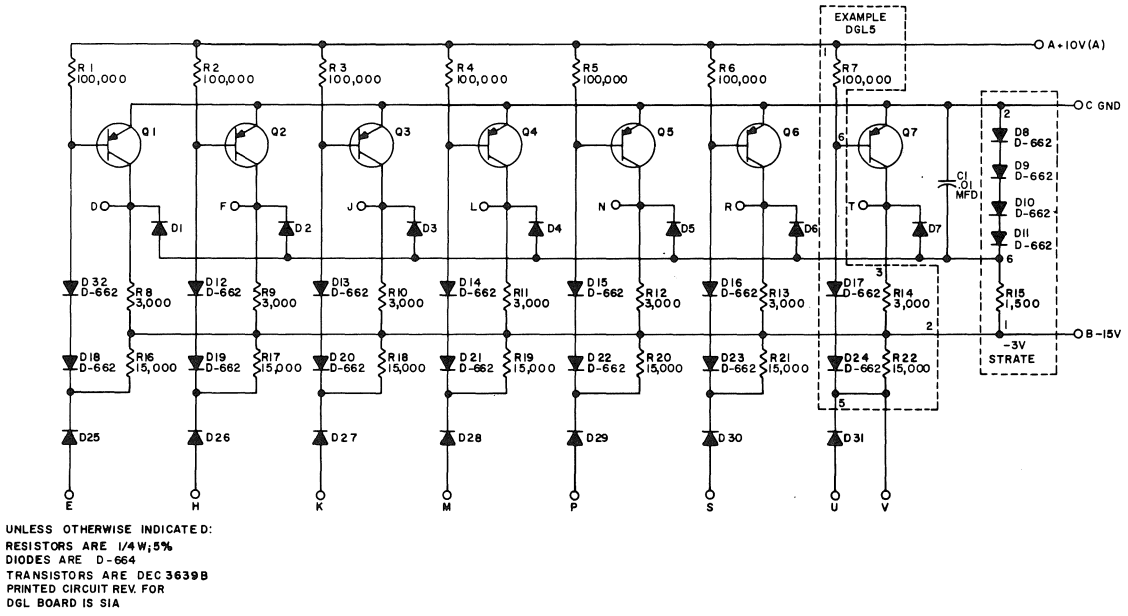
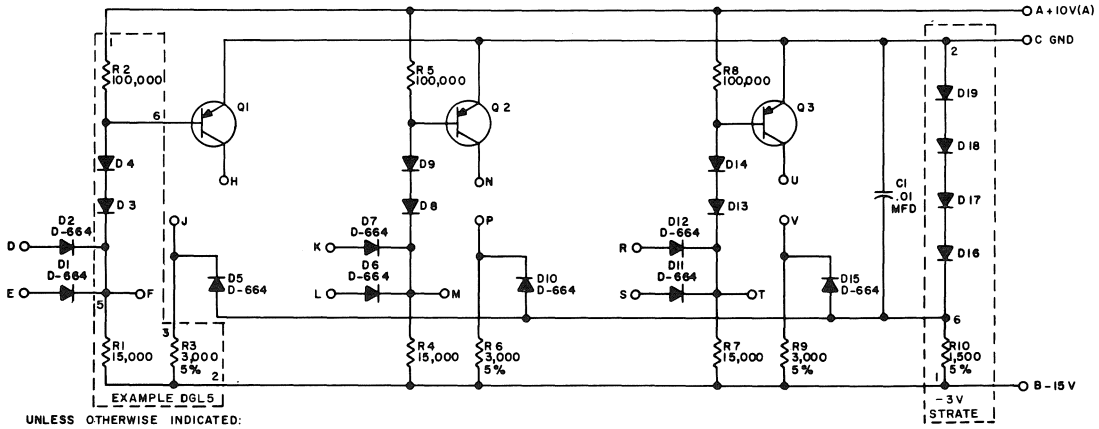


Figure 5-9 R401 Variable Clock



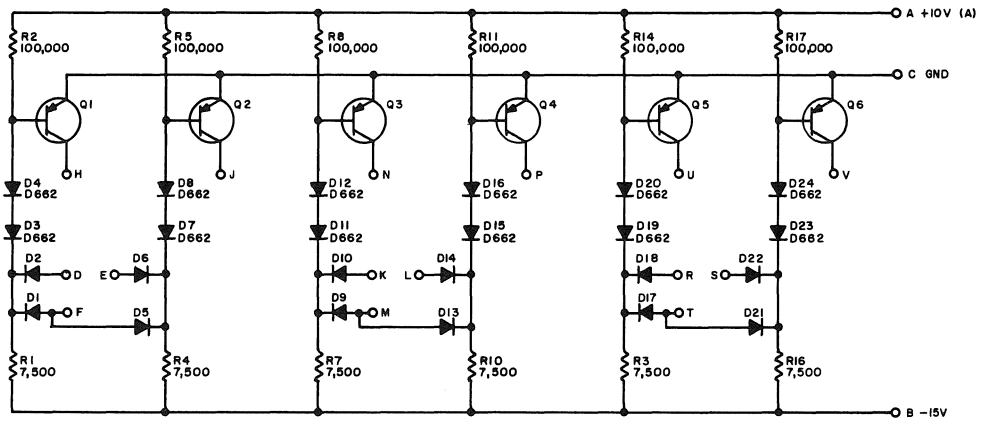
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W;5%
DIODES ARE D-664
TRANSISTORS ARE DEC 3639B
PRINTED CIRCUIT REV. FOR
DGL BOARD IS SIA

Figure 5-10 S107 Inverter



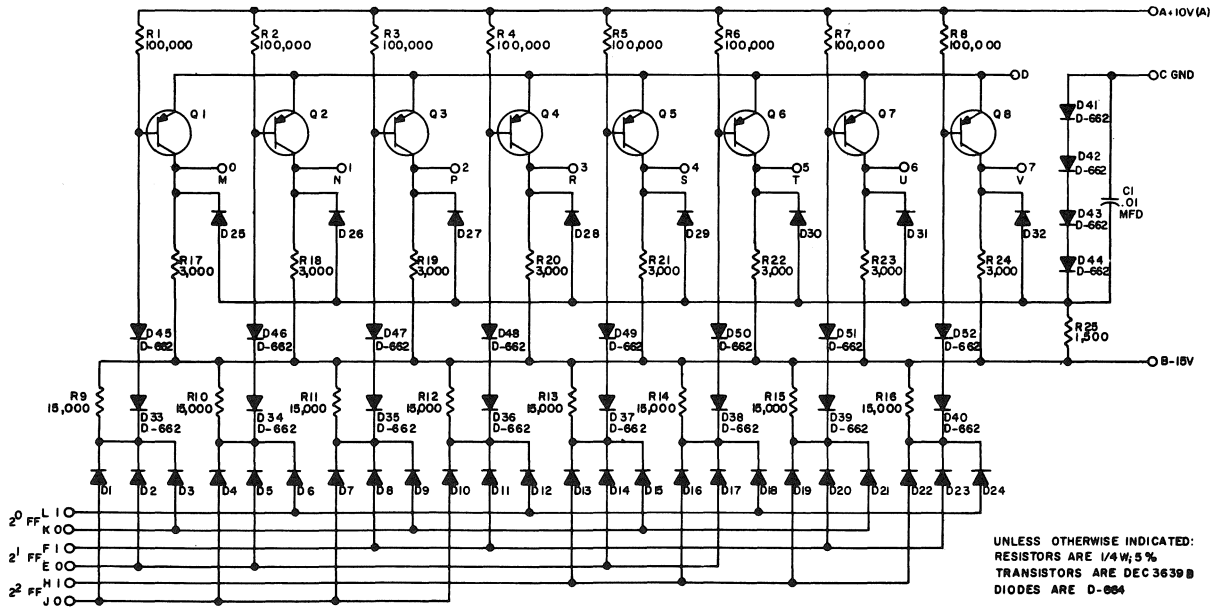
UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 3639
RESISTORS ARE 1/4W;10%
DIODES ARE D-662
PRINTED CIRCUIT REV. FOR DGL BOARD IS SIA

Figure 5-11 S111 Diode Gate



UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC3639
RESISTORS ARE 1/4W, 5%
DIODES ARE D664

Figure 5-12 S123 Diode Gate



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
TRANSISTORS ARE DEC 3639
DIODES ARE D-664

Figure 5-13 S151 Binary-to-Octal Decoder

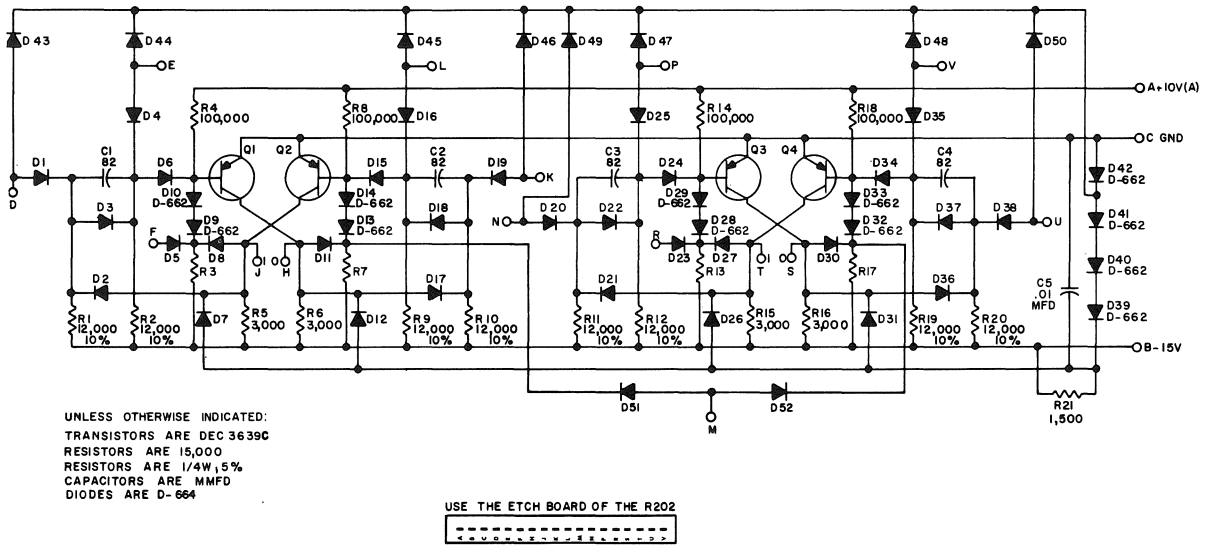


Figure 5-14 S202 Dual Flip-Flop

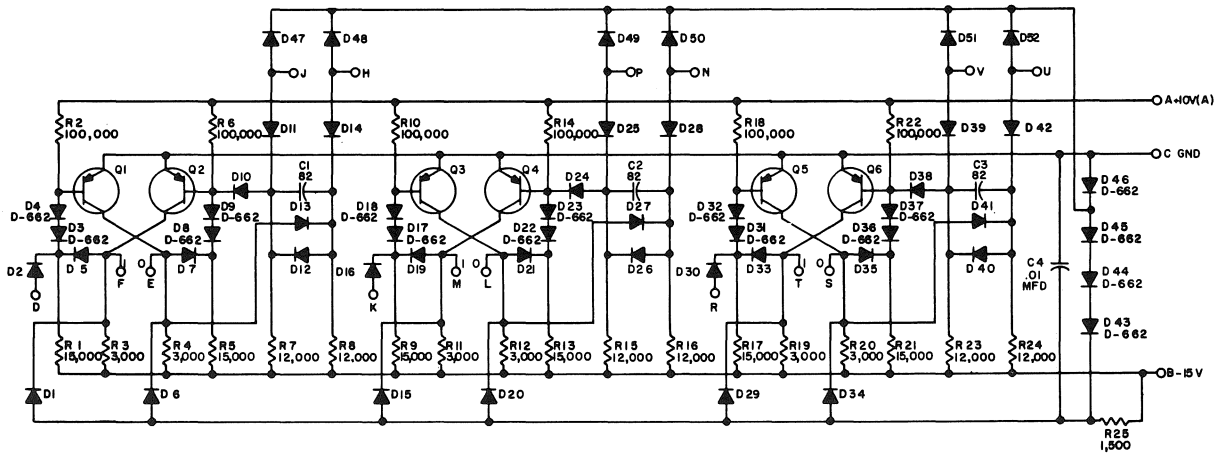


Figure 5-15 S203 Triple Flip-Flop

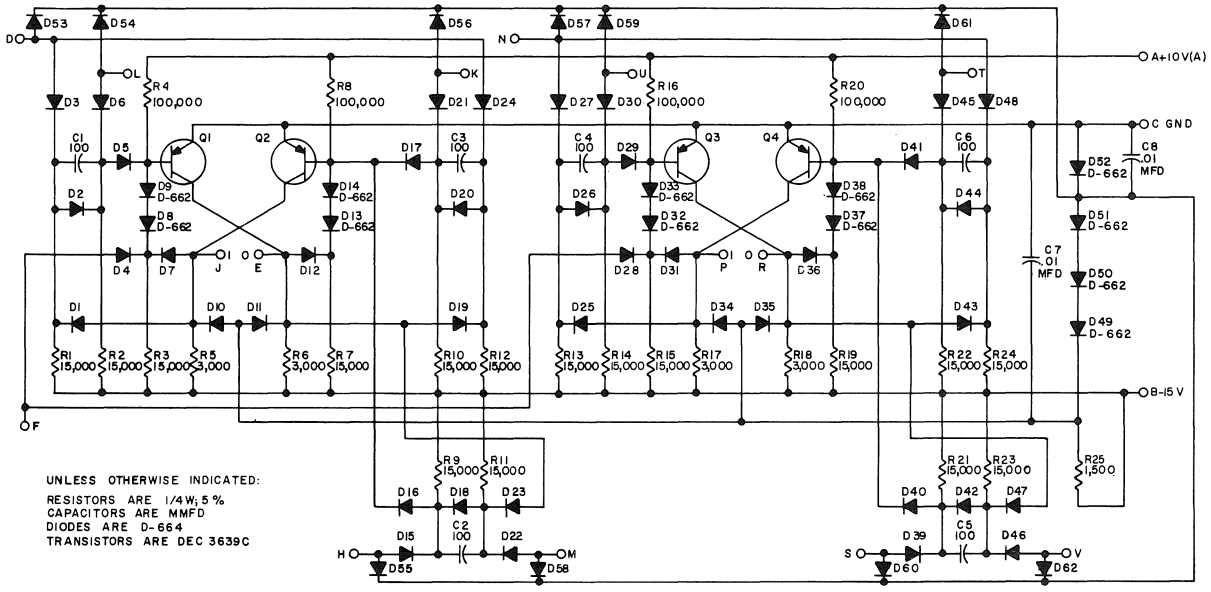


Figure 5-16 S205 Dual Flip-Flop

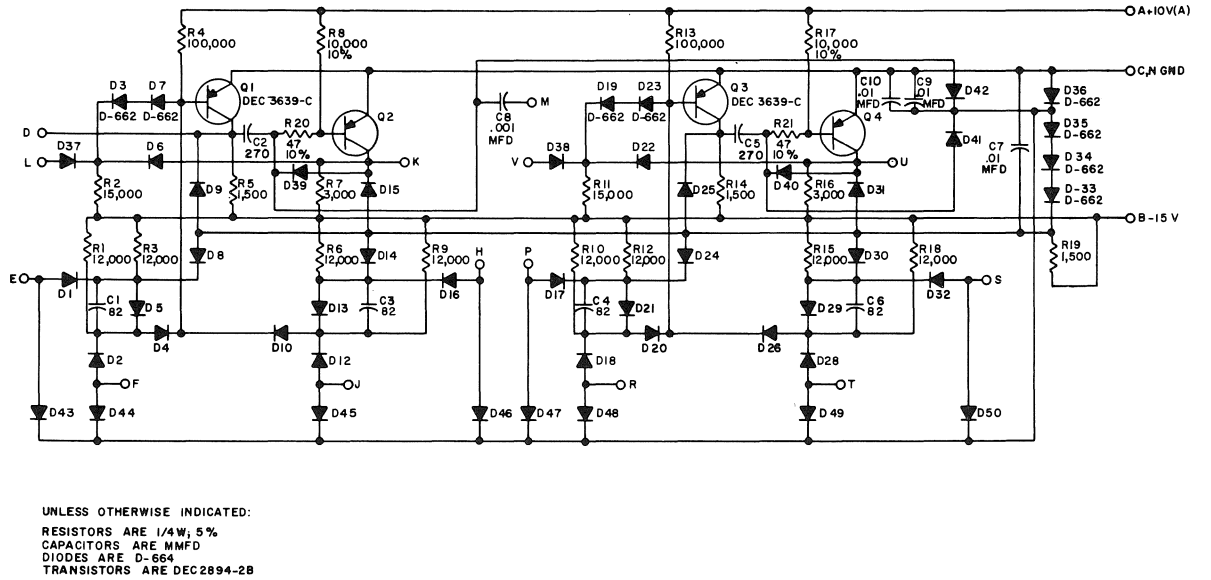
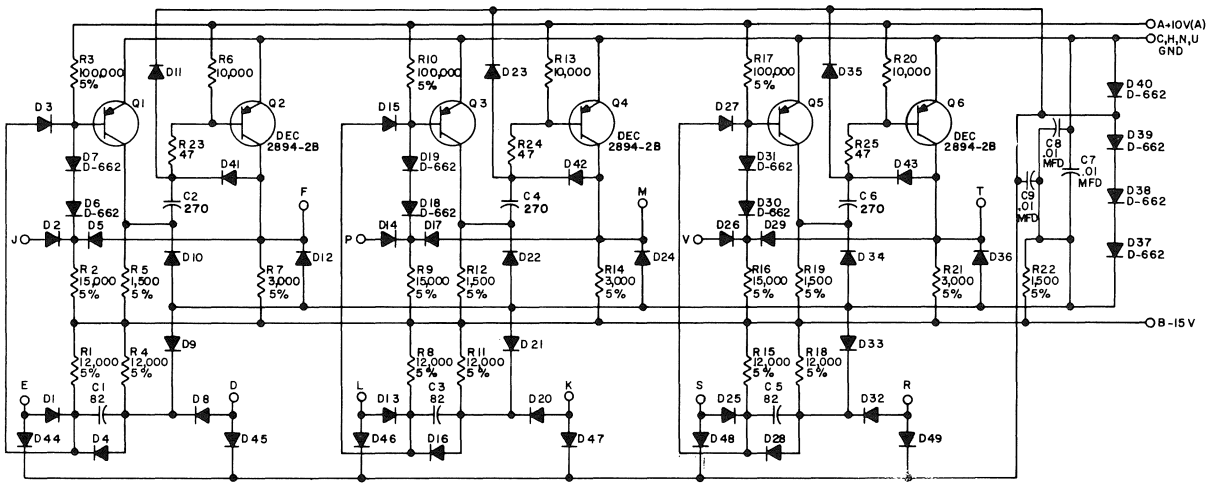


Figure 5-17 S602 Pulse Amplifier



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 10%
CAPACITORS ARE MMFD
DIODES ARE D-664
TRANSISTORS ARE DEC 3639-C

PARTS LIST A-PL-S603-0-0

Figure 5-18 S603 Pulse Amplifier

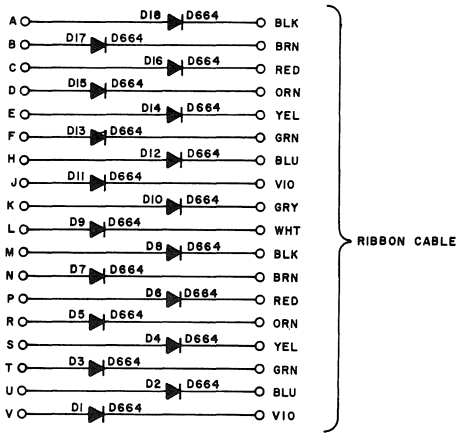
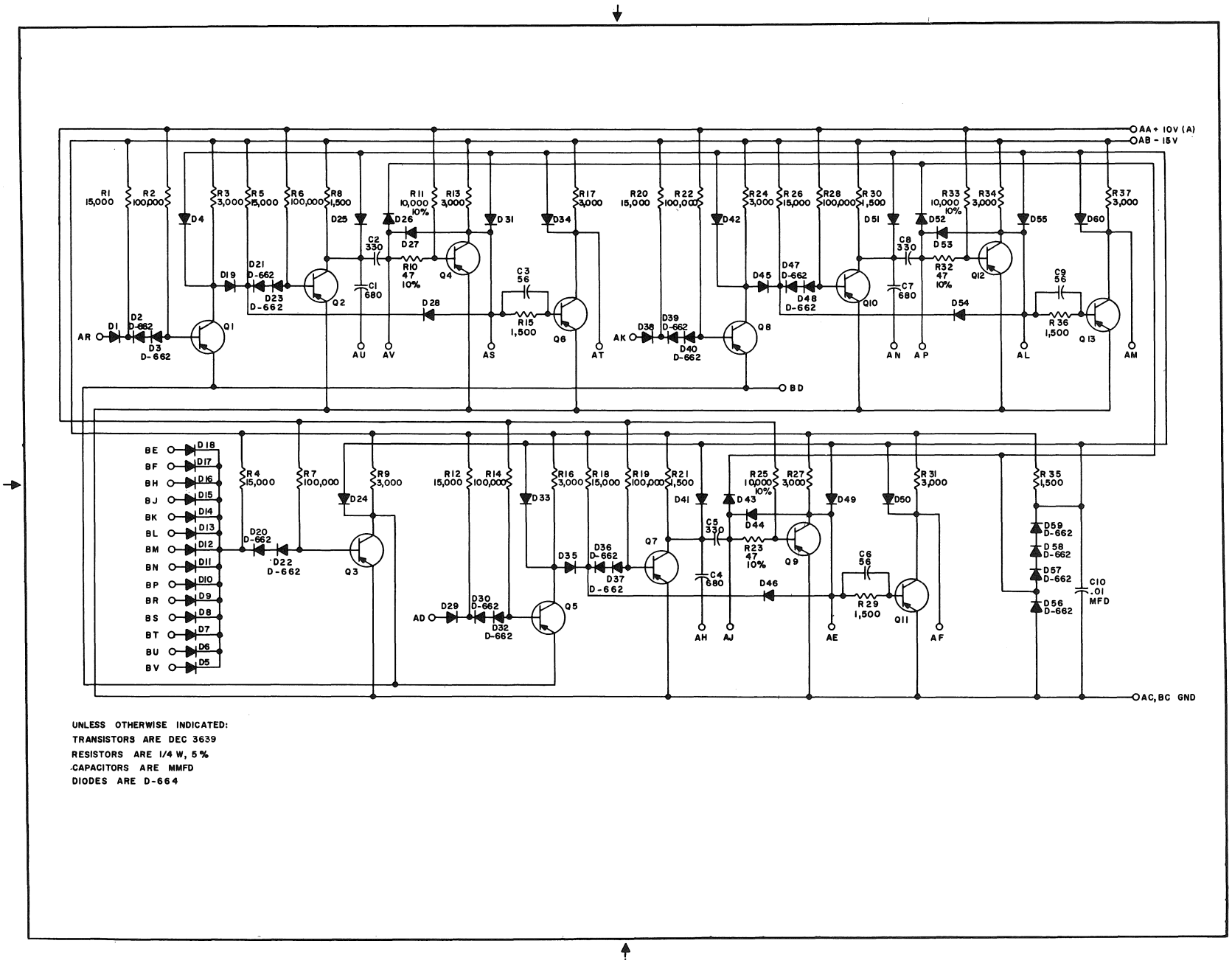


Figure 5-19 W018 Connector Board



UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 3639
RESISTORS ARE 1/4 W, 5%
CAPACITORS ARE MMFD
DIODES ARE D-664

Figure 5-20 W103 PDP-9 Device Selector

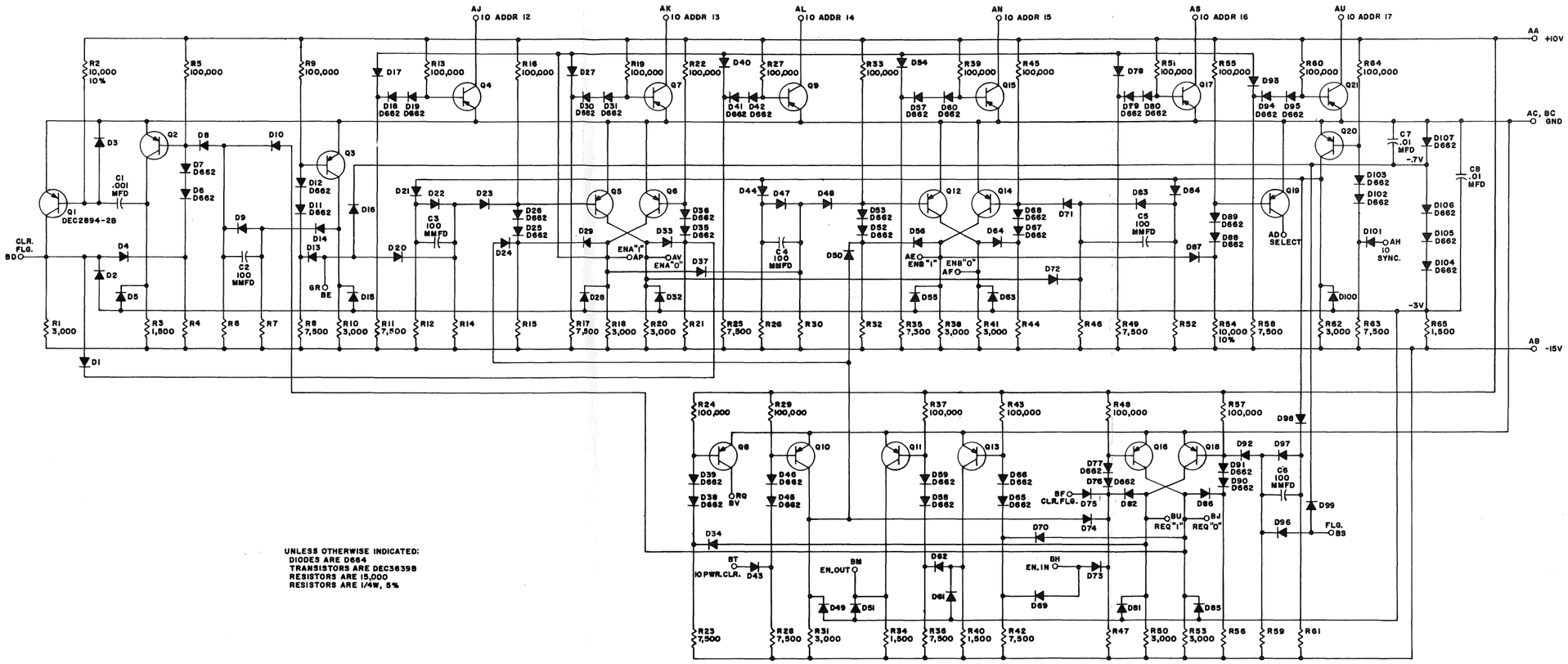
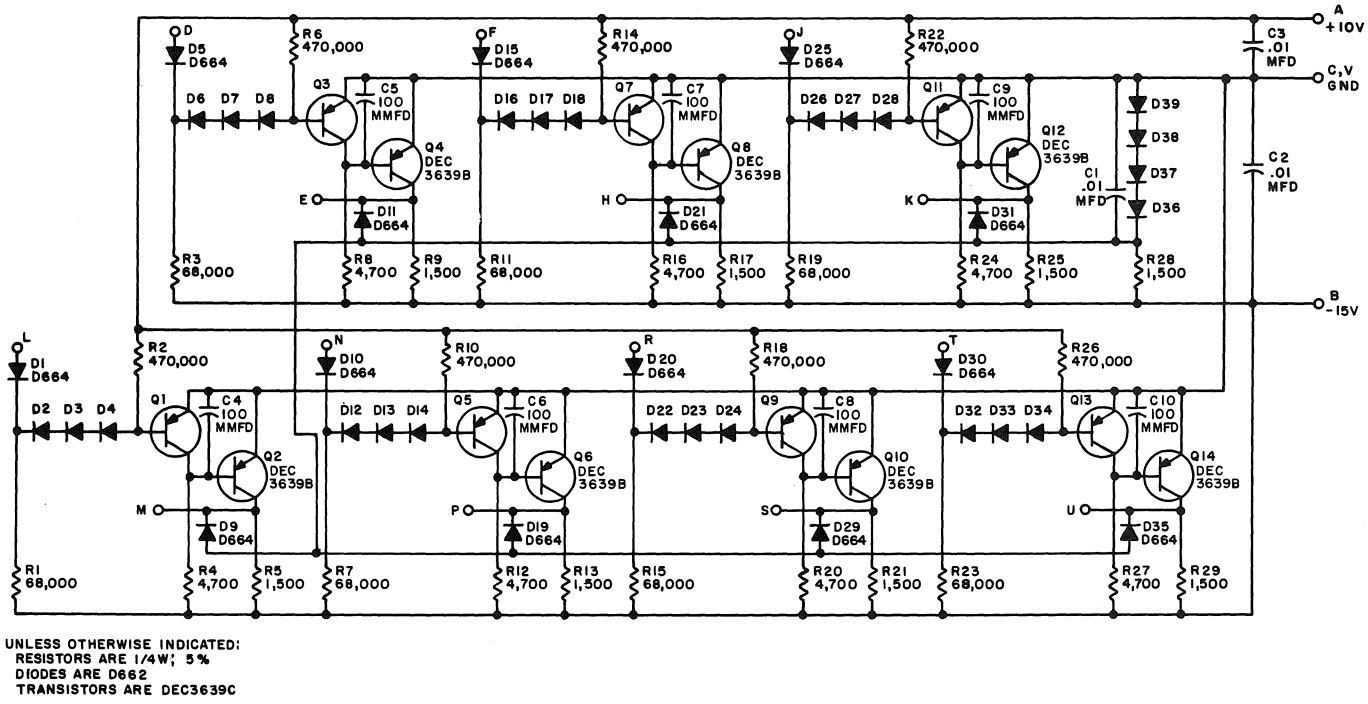
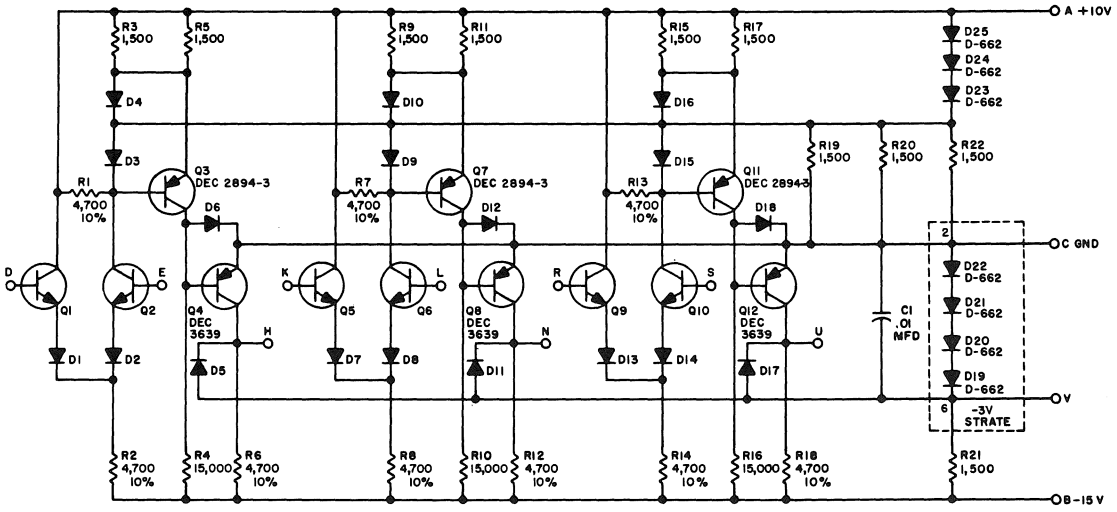


Figure 5-21 W104 PDP-9 I/O Bus Module



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
DIODES ARE D662
TRANSISTORS ARE DEC3639C

Figure 5-22 W107 High Impedance Follower



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
DIODES ARE D-664
TRANSISTORS ARE DEC 3009B

Figure 5-23 W520 Comparator

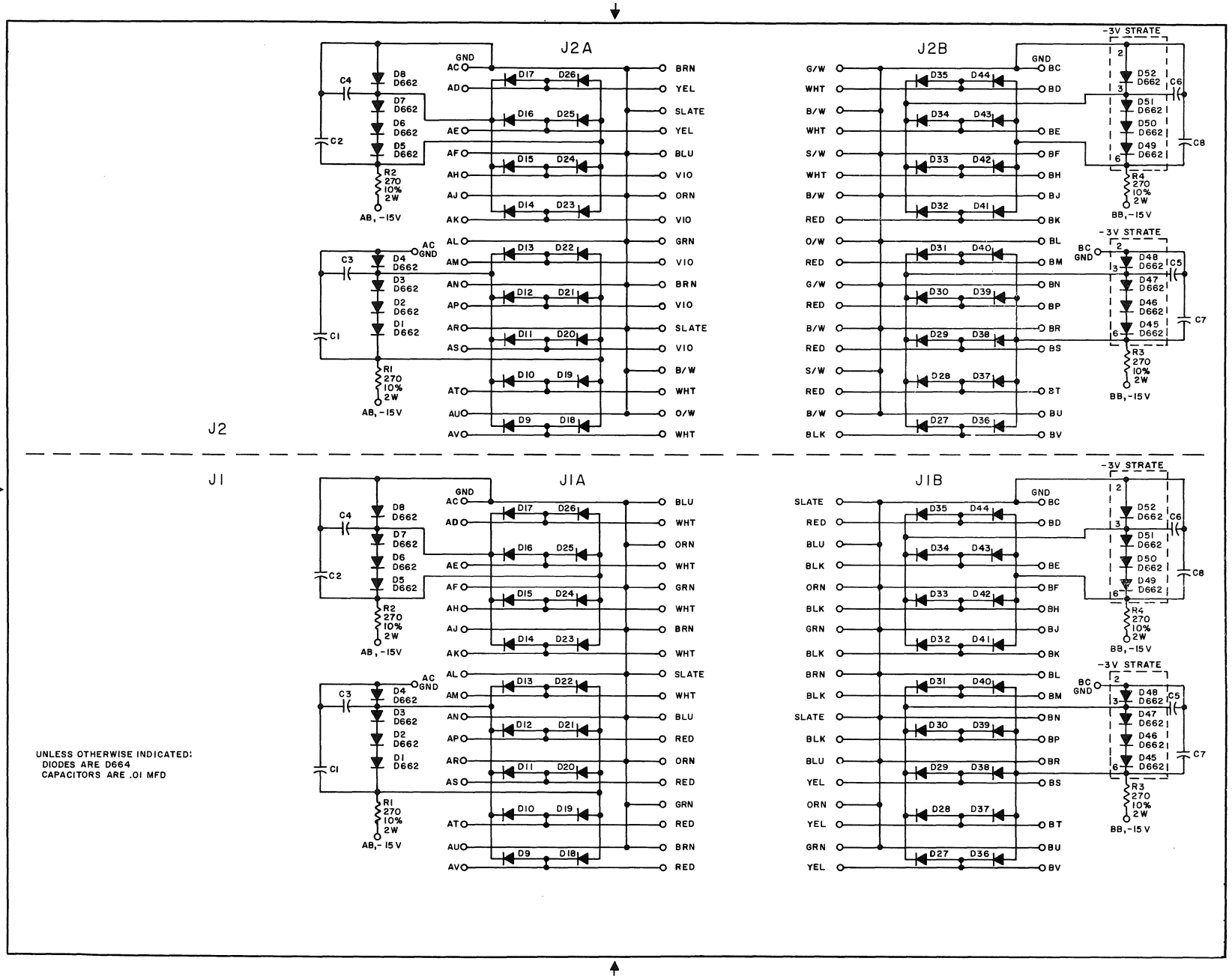


Figure 5-24 W850 I/O Cable Connectors

5.4 POWER SUPPLY 779

Power Supply 779 is a dual power supply unit designed for installation on a plenum door. One of the supplies furnished +10V and -15V suitable for logic power; the other is a lightly filtered, center-tapped 30V floating supply suitable for furnishing power to solenoids, etc. The -5V outputs of the power supply are connected in parallel to supply logic power to both the TC02 and TU55 transports. The schematic diagram of this power supply is shown in Figure 5-25 and the electrical characteristics are listed in DEC System Module Handbook, C-100.

Input voltages:	115 Vac, 60 cps (105V to 125V)
Output voltages:	+10V; -15V; center-tapped 30V (+15V -15V)
Maximum output current:	8A (limited by curve)
Line load regulation: (under all line and load conditions)	+10V regulated to 9-11V; all +15V supplies regulated to 14-16V
Ripple:	1V at +10V; 500 mV at -15V; 2.5V at 30V
Size frequency regulation:	±3%
Maximum voltage between output and chassis:	300V

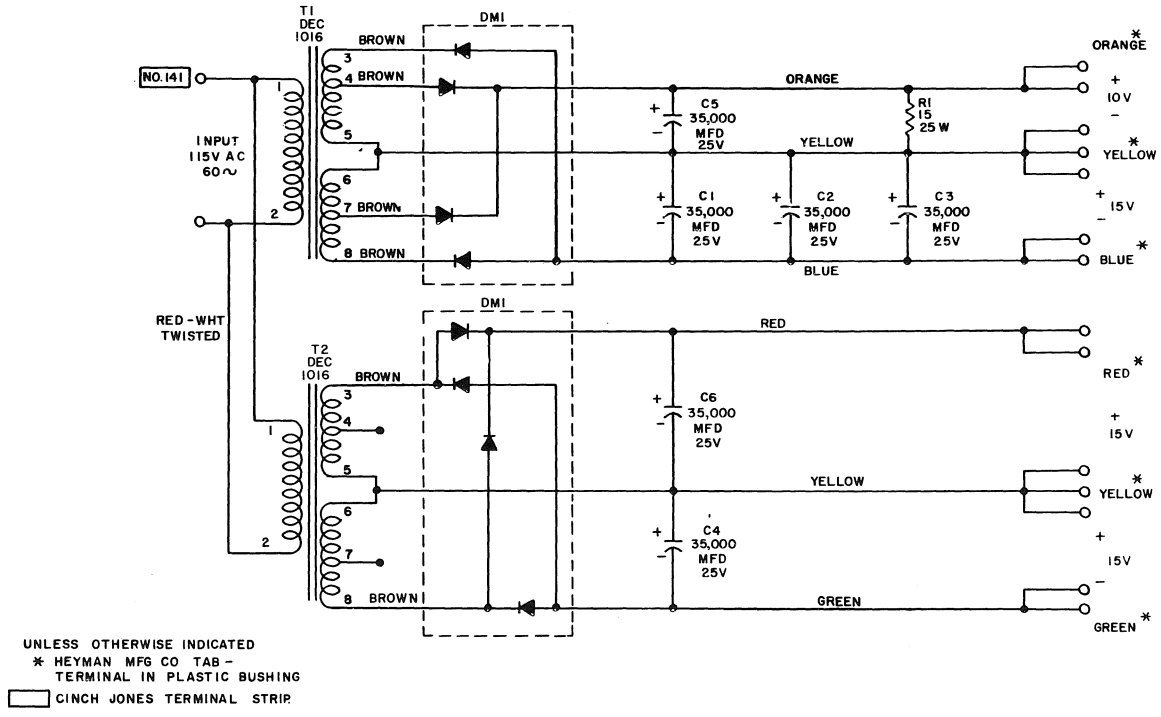


Figure 5-25 Power Supply Type 779, Schematic Diagram

5.4.1 Mechanical Characteristics

Pertinent mechanical characteristics of Power Supply 779 are as follows.

Panel width:	16-5/8 in.
Finish:	Chromate conversion, coating
Power input plug:	Jones No. 141 strip
Power output plug:	Heyman tab terminals

5.4.2 Power Supply Checks

The use of a multimeter permits output voltage measurements to be made on the Type 779 power supply without disconnecting the power supply. An oscilloscope should be used to measure the peak-to-peak ripple content of each dc output voltage. Because the power supply is not adjustable, a unit that does not meet the following tolerances should be considered defective and steps should be taken to correct the deficiency!

Nominal Voltage Outputs (volts)	Output Voltage Range (volts)	Maximum Peak-to-Peak Output Ripple Voltage (volts)
+10	9-11	1
-15	14-16	0.5

±15 (for center tapped 30V circuit)

5.4.3 Marginal Checks

Marginal checks are performed to aggravate borderline circuit conditions within the control logic and thus produce observable faults. By recording the bias voltage levels at which circuits fail, progressive deterioration can be plotted and expected failure dates can be predicted. This procedure provides a means for planned replacement. Marginal checks are also useful as a troubleshooting aid to locate marginal or intermittent components (e.g., deteriorating transistors).

Marginal checks are performed by operating the logic circuits from an adjustable external power supply located in the PDP-9 or DEC Type 734B Dual Variable Power Supply. Raising the bias level above +10V increases the transistor cutoff required to be overcome by the preceding transistor, thus causing a below-par transistor to fail. Lowering the bias level below +10V reduces the transistor base bias and noise rejection. This procedure provides detection of high-leakage transistors and simulates high-temperature conditions for checking thermal runaway. Raising and lowering the -15V supply has little effect on the logic circuits because the collector load voltage of most modules is clamped at -3V. It does, however, increase and decrease the output pulse amplitude of the pulse amplifier circuits (e.g., the delay circuits) and then provides a sensitivity check of the circuits which follow.

CAUTION

Increasing the -15V power to a value more negative than -18V will cause damage within the logic circuits.

The panel for conducting marginal checks of the Type TC02 DECtape Control is located at the left-hand side of the wired panel assembly. When switched on (up), switches 1A through 1F apply power from the marginal check bus; when switched off (down), normal power is applied. The "up" position of the top switch on each panel selects the marginal check voltage of +10V. The "down" position selects the fixed voltage of +10V. The lower switch of each panel performs the same function with the -15V.

A color-coded connector on the right side of each panel connects the normal and marginal operating voltages to the marginal check panel. The normal and marginal power buses are common to all panels. The normal power bus is connected to the Type 779 Power Supply, the marginal power bus to the marginal check power supply on the PDP-9.

A marginal check if performed as follows.

a. Set selector switch on marginal-check power supply to +10 mc and adjust the power supply output for +10V.

b. Set the top normal/marginal check switch on the panel to be tested to its "up" position.

c. Start DECtape operation in a normal program or in a routine which fully utilizes the circuits in the rack to be tested. If no suitable program is available in the normal system application, select an appropriate maintenance routine. The maintenance programs provide basic exercises of specific functions and scope loops for these functions as well as a routine which redundantly exercises all functions.

d. Decrease the marginal-check power supply output voltage until normal system operation is interrupted. Record the marginal-check voltage. If desired, locate and replace the marginal transistors at this time.

e. Restart DECtape operation and increase the marginal-check power supply output voltage until normal operation is interrupted. Record the marginal-check voltage. If desired, locate and replace the marginal transistors at this time.

f. Set the top normal/marginal check switch in step c to its "down" position.

g. Repeat steps a through f for the center normal/marginal switch on the panel being tested.

h. Set selector switch on the marginal-check power supply to -15mc and adjust the power supply output for -15V.

i. Repeat step c.

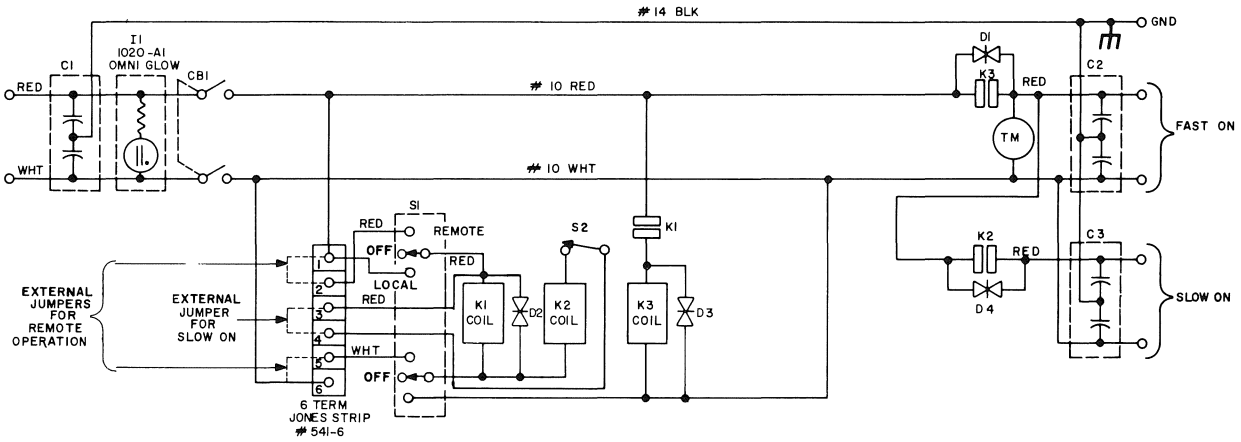
j. Set the bottom normal/marginal switch on the panel being tested to its "up" position.

k. Repeat steps d and e and then return the bottom normal/marginal switch to its "down" position.

l. Adjust the output of the marginal-check power supply to 0V and set the selector switch to its "off" position.

5.5 POWER CONTROL PANEL (Type 832F)

The Power Control Panel is mounted on the plenum door at the rear of the cabinet and is used in conjunction with Type 779 Power Supply. The schematic diagram of the panel is shown on Figure 5-26 .



NOTES
D1,D2,D3,D4 THYRECTOR G.E. 20SP4B4,115V
C1 CAPACITOR 2 X.1 MFD 1000 VDC #YAT 10011-1
CORNELL DUBLIER.
C2 & C3 CAPACITOR BATHTUB-DEC PURCH. SPEC# CAF-0001
2 X.1 MFD 600 VDC CORNELL DUBLIER.
S1 TOGGLE SWITCH DPDT **7563K6 3POS CENTER OFF**
S2 TOGGLE SWITCH DPST 7590K9
K1 RELAY #1040-8-687 NORMALLY OPEN 115 VAC COIL 3-5 SEC DELAY QUICK OPERATE, SLOW RELEASE.
K2 RELAY #1040-8-58 NORMALLY OPEN 115 VAC COIL 3-5 SEC DELAY SLOW OPERATE, QUICK RELEASE.
K3 RELAY # EM-1 115 VAC EBERT ELECTRONICS.
CB1 CIRCUIT BREAKER #190-230-101 30 AMPS. 250V, 60 CYC-CURVE 4
TM HOBBS TIME METER TYPE MII906 120V 60 CYC-CURVE 4

Figure 5-26 Power Control Panel Type 832F

5.6 PREVENTIVE MAINTENANCE

Preventive maintenance consists of procedures performed prior to the initial operation of the equipment and periodically during its operating life. These procedures include visual inspections, cleaning, mechanical checks, and circuit element checks. Marginal checks are also conducted when considered necessary to aggravate border-line conditions or intermittent failures so that they can be detected and corrected. A log book should be available for recording specific data which indicates the rate of performance deteriation and provides information for determining when components should be replaced.

Except for marginal checks all preventive maintenance procedures should be performed once a month or every 200 operating hours, whichever occurs first.

NOTE

The heads on each TU55 should be cleaned daily using the head cleaner listed in Table 5-1.

5.6.1 Mechanical Checks

The following mechanical checks should reveal any substandard conditions in the mechanical operation of the control unit.

a. Clean the exterior and the interior of the control by means of a vacuum cleaner or by using clean cloths moistened in a nonflammable solvent.

b. Clean the air filter at the bottom of each cabinet. Remove the filter by removing the fan and housing which are held in place by two knurled and slotted screws. Wash the filter in soapy

water, dry in an oven or by spraying with compressed gas, and spray with Filter-kote (Research Products Corp., 1015 E. Washington Ave., Wisconsin, 53703).

c. Clean all rotary switches with a spray cleaner such as Contactene.

d. Lubricate door hinges and casters with a light machine oil. Wipe off excess oil.

e. Visually inspect the TC02 for completeness and general condition.

f. Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security. Repair or replace any defective wiring.

g. Inspect switches, controls, knobs, jacks, connectors, transformers, fans, capacitors, lamp assemblies, etc. Tighten or replace as required.

h. Inspect switches for binding, scraping, misalignment, and positive action. Adjust, align, or replace as necessary.

i. Inspect all racks of logic to assure that each module is securely seated in its connector.

j. Inspect power supply capacitors for leaks, bulges, or discoloration. Replace any capacitors exhibiting these signs of malfunction.

CHAPTER 6
ENGINEERING DRAWINGS

This chapter contains the logic block diagrams and module location diagrams of the TC02 DECtape Control. The equivalent drawings for the TU55 DECtape transport are contained within the TU55 Instruction Manual.

6.1 SYMBOLS AND DESIGNATIONS

The block and signal symbols used on the logic diagrams are defined in the Digital Logic Handbook, C-105 together with a description of standard DEC logic levels. The signal designations assigned are defined in Table 3-2 of this manual.

6.2 DRAWING LIST

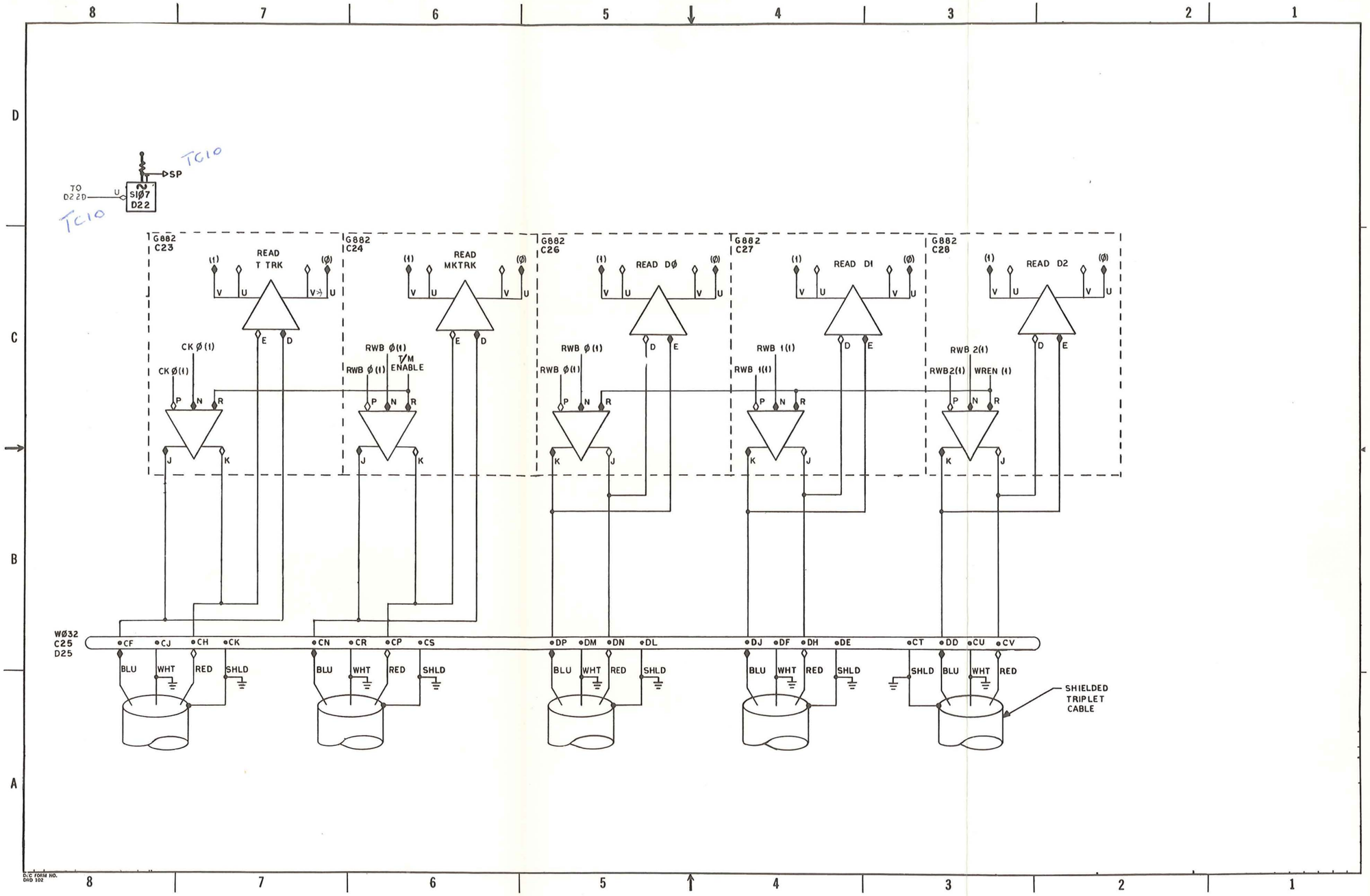
Table 6-1 lists the pertinent engineering drawings referenced in this manual. These drawings relate to the discussions in this manual and do not necessarily reflect the latest revisions incorporated in the equipment. When discrepancies exist between the drawings contained in this manual and the drawings shipped with the device, the latter should be assumed to be the correct drawing set.

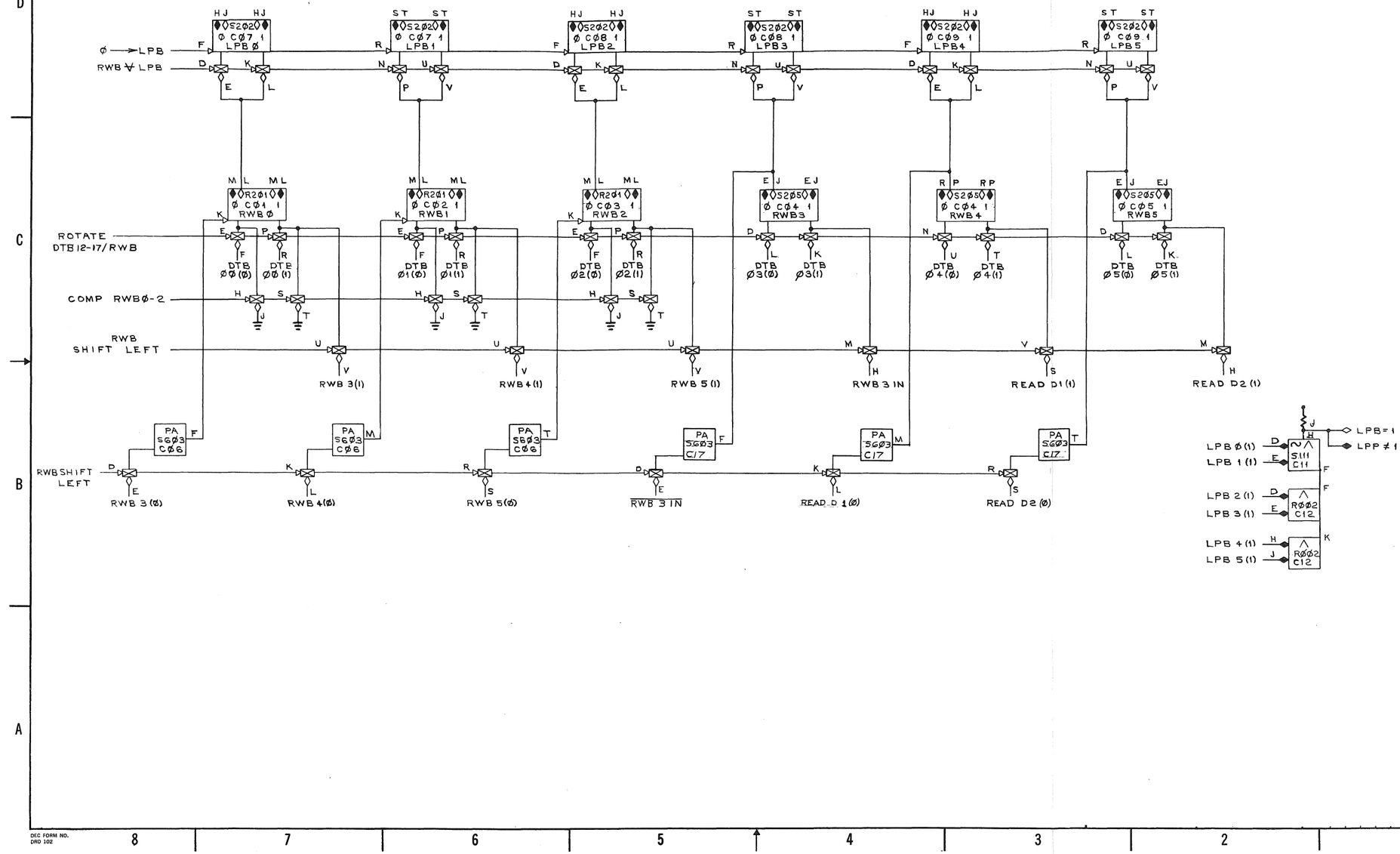
Table 6-1
Engineering Drawing List

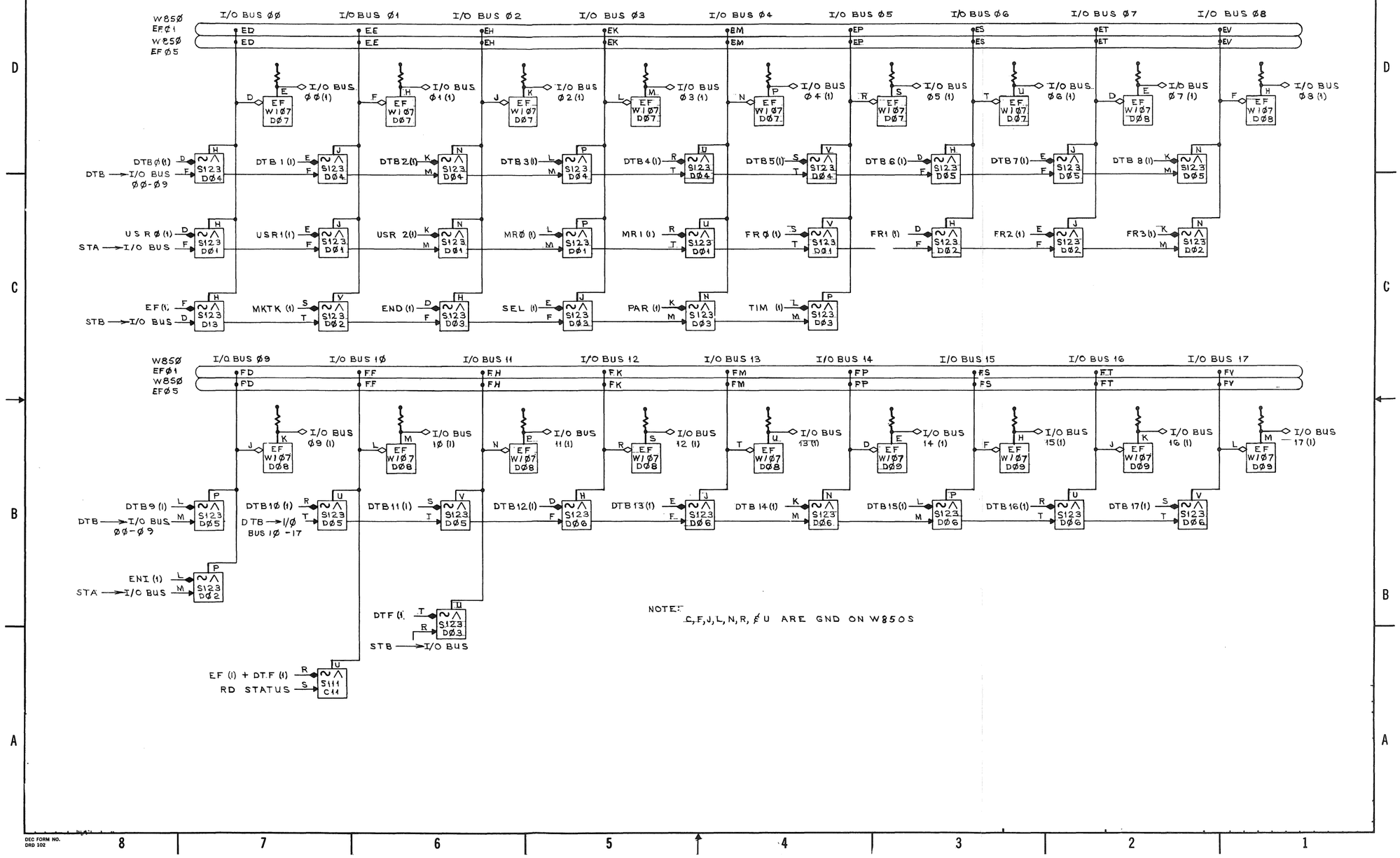
Number	Title	Revision	Page
D-TC02-0-1	R/W AMPS, SP GEN, TEST CONN	C	6-3
D-TC02-0-2	LPB and RWB Registers		6-5
D-TC02-0-3	I/O Bus Gating	B	6-7
D-TC02-0-4	I/O Bus, IOTs	A	6-9
D-TC02-0-5	Errors, MCP Switch	B	6-11
D-TC02-0-6	Control	B	6-13
D-TC02-0-7	Status A, Command Bus	A	6-15
D-TC02-0-8	WINDOW, MK TRK, STATE	A	6-17
D-TC02-0-9	MCP and Cables		6-19
D-TC02-0-10	TP GEN	B	6-21
D-TC02-0-11	DTB Register	A	6-23
D-TC02-0-13 (Sheet 1)	Module List Panels A-F	F	6-25
D-TC02-0-13 (Sheet 2)	Module List Panels A-F	F	6-27
D-TC02-0-15 (Sheet 1)	Timing	A	6-29
D-TC02-0-15 (Sheet 2)	Timing	A	6-31

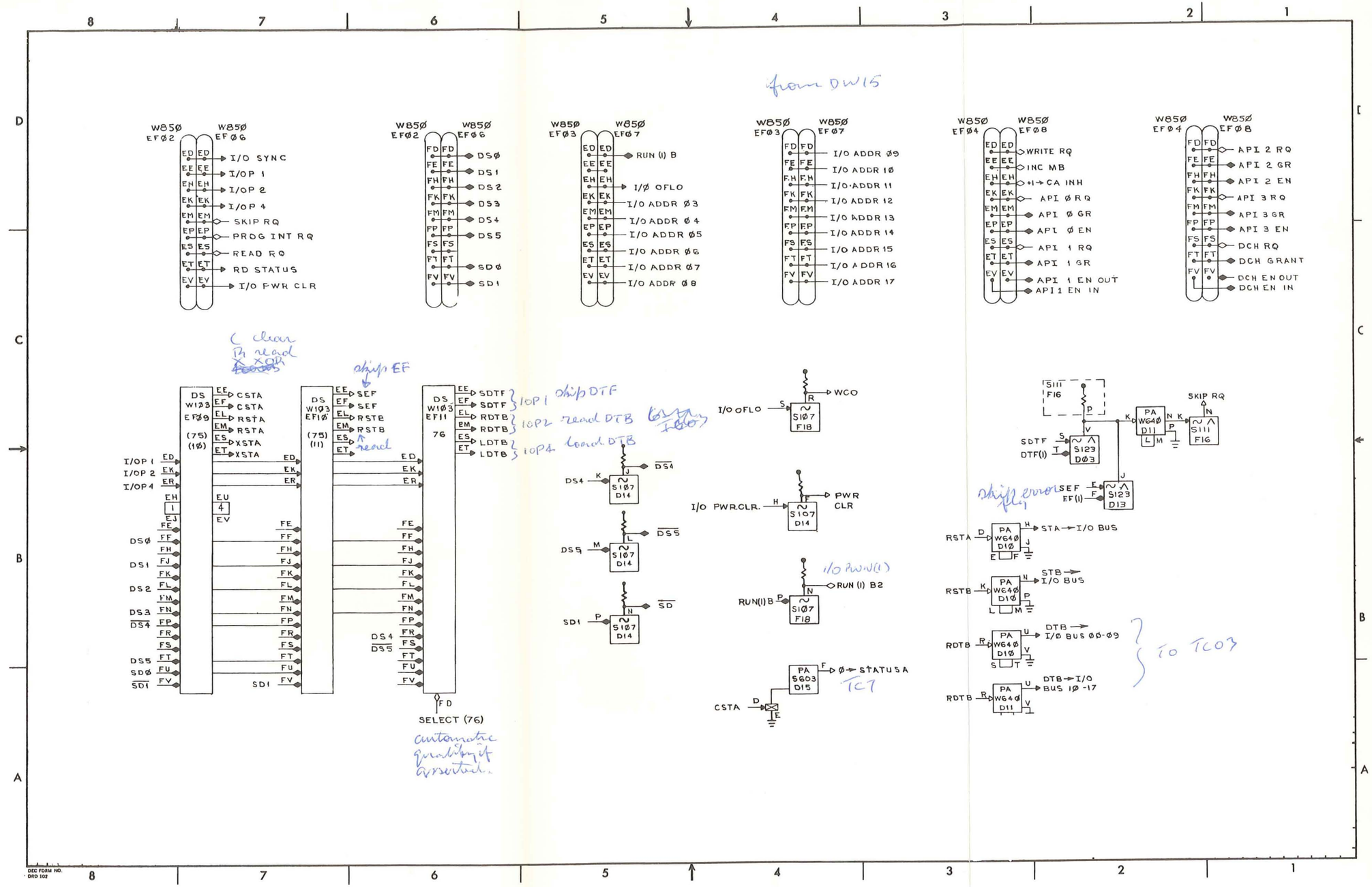
Table 6-1 (cont)
Engineering Drawing List

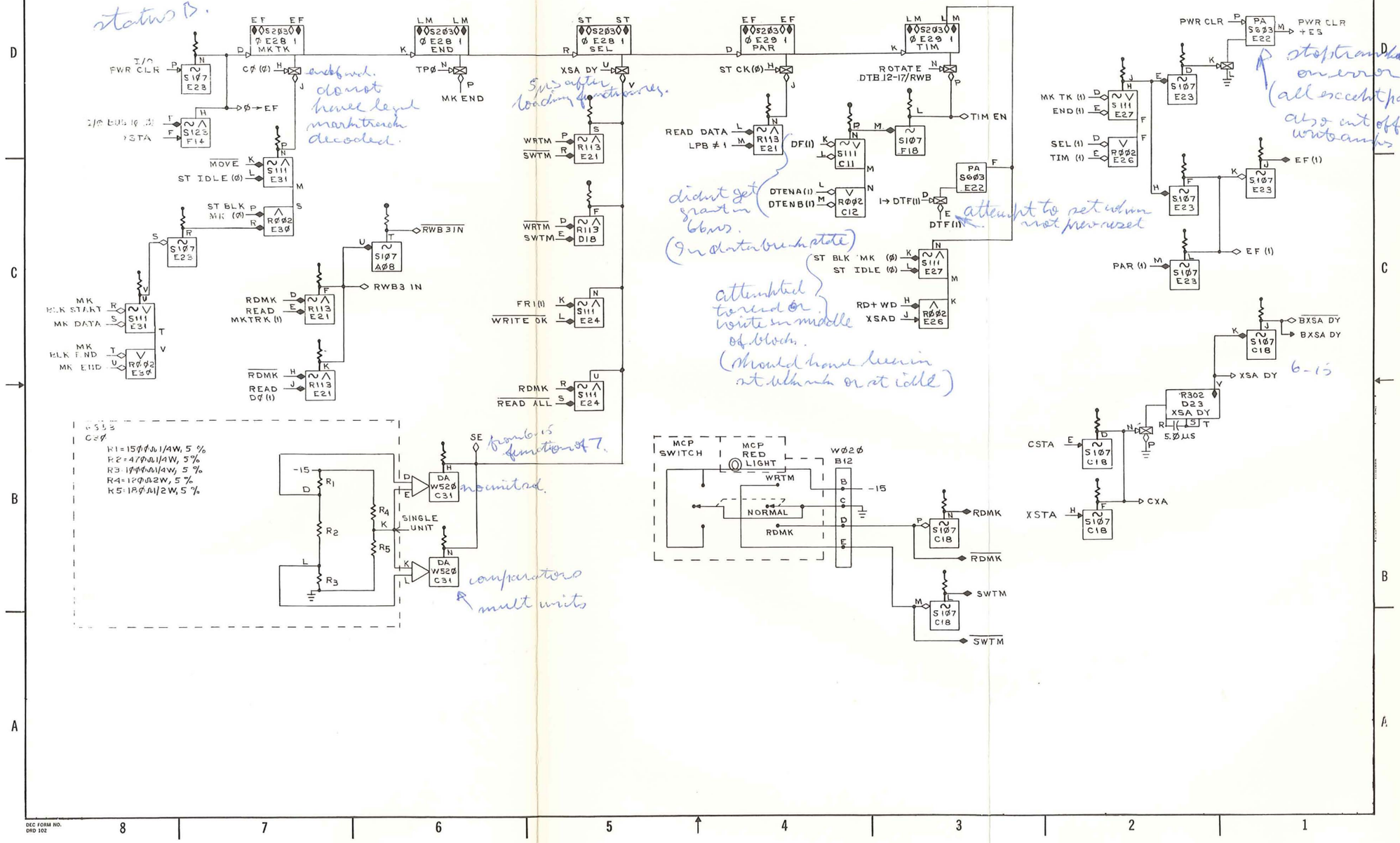
Number	Title	Revision	Page
D-TC02-0-15 (Sheet 3)	Timing	A	6-33
D-TC02-0-15 (Sheet 4)	Timing	A	6-35
D-TC02-0-16	DCH, API	C	6-37
D-TC02-0-17	Test Connectors	A	6-39
D-7007236-0-0	TC02 Bussed Wiring Assembly	A	6-41


TO D22D
U
SIØ7 D22
SP
TC10
TC10
G882 C23
READ T TRK
G882 C24
READ MKTRK
G882 C26
READ DØ
G882 C27
READ D1
G882 C28
READ D2
CK Ø (1)
RWB Ø (1)
T/M ENABLE
RWB 1 (1)
RWB 2(1)
WREN (1)
WØ32 C25 D25
CF CJ CH CK
CN CR CP CS
DP DM DN DL
DJ DF DH DE
CT DD CU CV
BLU WHT RED SHLD
SHIELDED TRIPLET CABLE

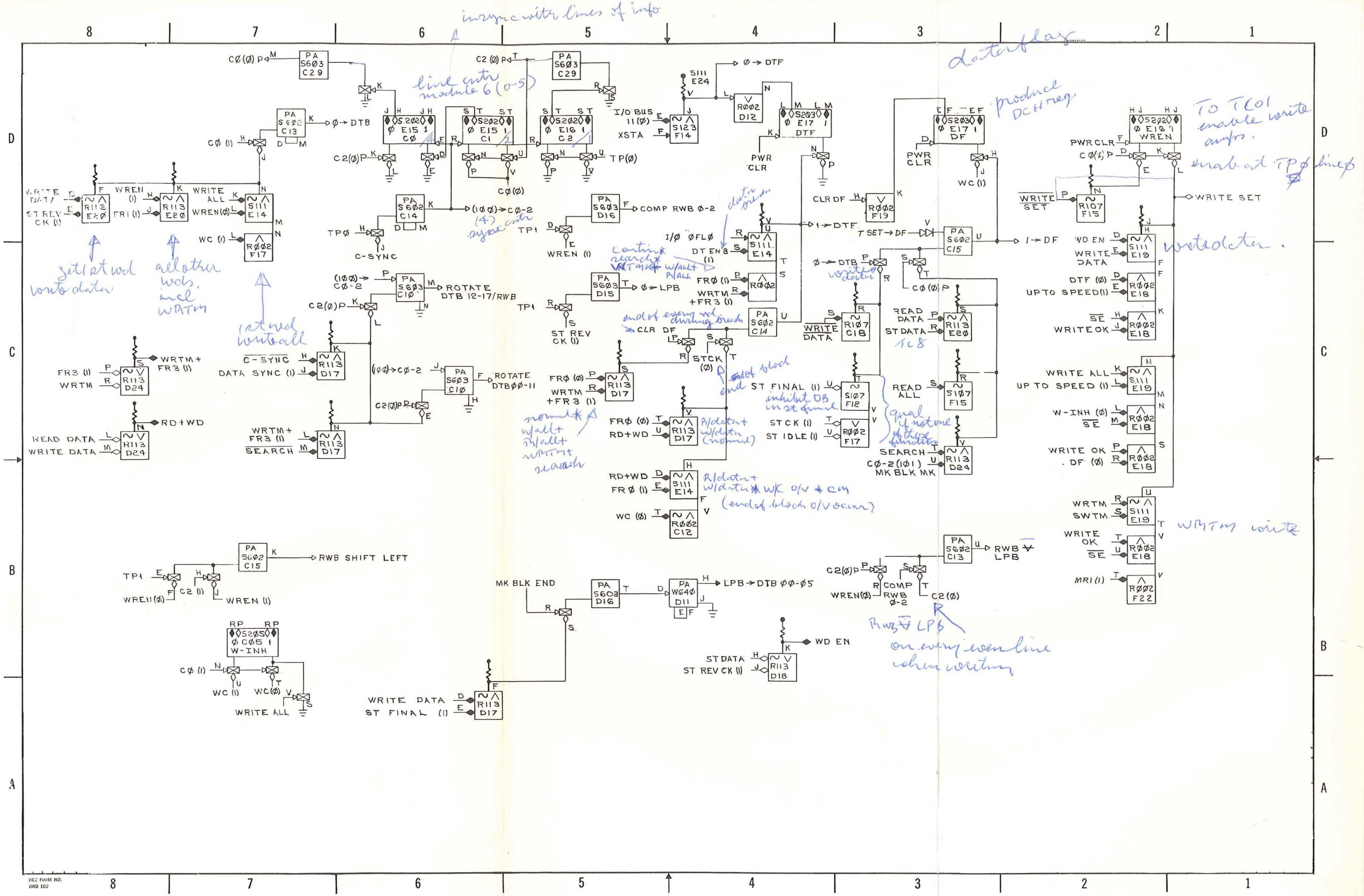

Ø → LPB
RWB ∀ LPB
ROTATE DTB 12-17/RWB
COMP RWBØ-2
RWB SHIFT LEFT
RWB SHIFT LEFT
RWB 3 (Ø)
RWB 4 (Ø)
RWB 5 (Ø)
RWB 3 IN
READ D 1 (Ø)
READ D2 (Ø)
RWB 3 (1)
RWB 4 (1)
RWB 5 (1)
RWB 3 IN
READ D1 (1)
READ D2 (1)
LPB Ø (1)
LPB 1 (1)
LPB 2 (1)
LPB 3 (1)
LPB 4 (1)
LPB 5 (1)
LPB = 1
LPP ≠ 1


W85Ø EFØ1
W85Ø EFØ5
I/O BUS ØØ
I/O BUS Ø1
I/O BUS Ø2
I/O BUS Ø3
I/O BUS Ø4
I/O BUS Ø5
I/O BUS Ø6
I/O BUS Ø7
I/O BUS Ø8
ED
EE
EH
EK
EM
EP
ES
ET
EV
I/O BUS ØØ (1)
I/O BUS Ø1 (1)
I/O BUS Ø2 (1)
I/O BUS Ø3 (1)
I/O BUS Ø4 (1)
I/O BUS Ø5 (1)
I/O BUS Ø6 (1)
I/O BUS Ø7 (1)
I/O BUS Ø8 (1)
EF W1Ø7 DØ7
EF W1Ø7 DØ8
DTBØ (1)
DTB 1 (1)
DTB2 (1)
DTB3 (1)
DTB4 (1)
DTB5 (1)
DTB 6 (1)
DTB7 (1)
DTB 8 (1)
DTB → I/O BUS ØØ-Ø9
USRØ (1)
USR1 (1)
USR 2 (1)
MRØ (1)
MR1 (1)
FRØ (1)
FR1 (1)
FR2 (1)
FR3 (1)
STA → I/O BUS
EF (1,
MKTK (1)
END (1)
SEL (1)
PAR (1)
TIM (1)
STB → I/O BUS
S123 DØ4
S123 DØ1
S123 DØ2
S123 DØ3
S123 DØ5
S123 DØ6
S123 D13
W85Ø EFØ1
W85Ø EFØ5
I/O BUS Ø9
I/O BUS 1Ø
I/O BUS 11
I/O BUS 12
I/O BUS 13
I/O BUS 14
I/O BUS 15
I/O BUS 16
I/O BUS 17
FD
FF
FH
FK
FM
FP
FS
FT
FV
I/O BUS Ø9 (1)
I/O BUS 1Ø (1)
I/O BUS 11 (1)
I/O BUS 12 (1)
I/O BUS 13 (1)
I/O BUS 14 (1)
I/O BUS 15 (1)
I/O BUS 16 (1)
I/O BUS 17 (1)
EF W1Ø7 DØ8
EF W1Ø7 DØ9
DTB9 (1)
DTB1Ø (1)
DTB11 (1)
DTB12 (1)
DTB 13 (1)
DTB 14 (1)
DTB15 (1)
DTB16 (1)
DTB 17 (1)
DTB → I/O BUS ØØ-Ø9
DTB → I/Ø BUS 1Ø -17
ENI (1)
STA → I/O BUS
DTF (1,
STB → I/O BUS
EF (1) + DTF (1)
RD STATUS
S111 C11
NOTE:
C, F, J, L, N, R, & U ARE GND ON W85OS

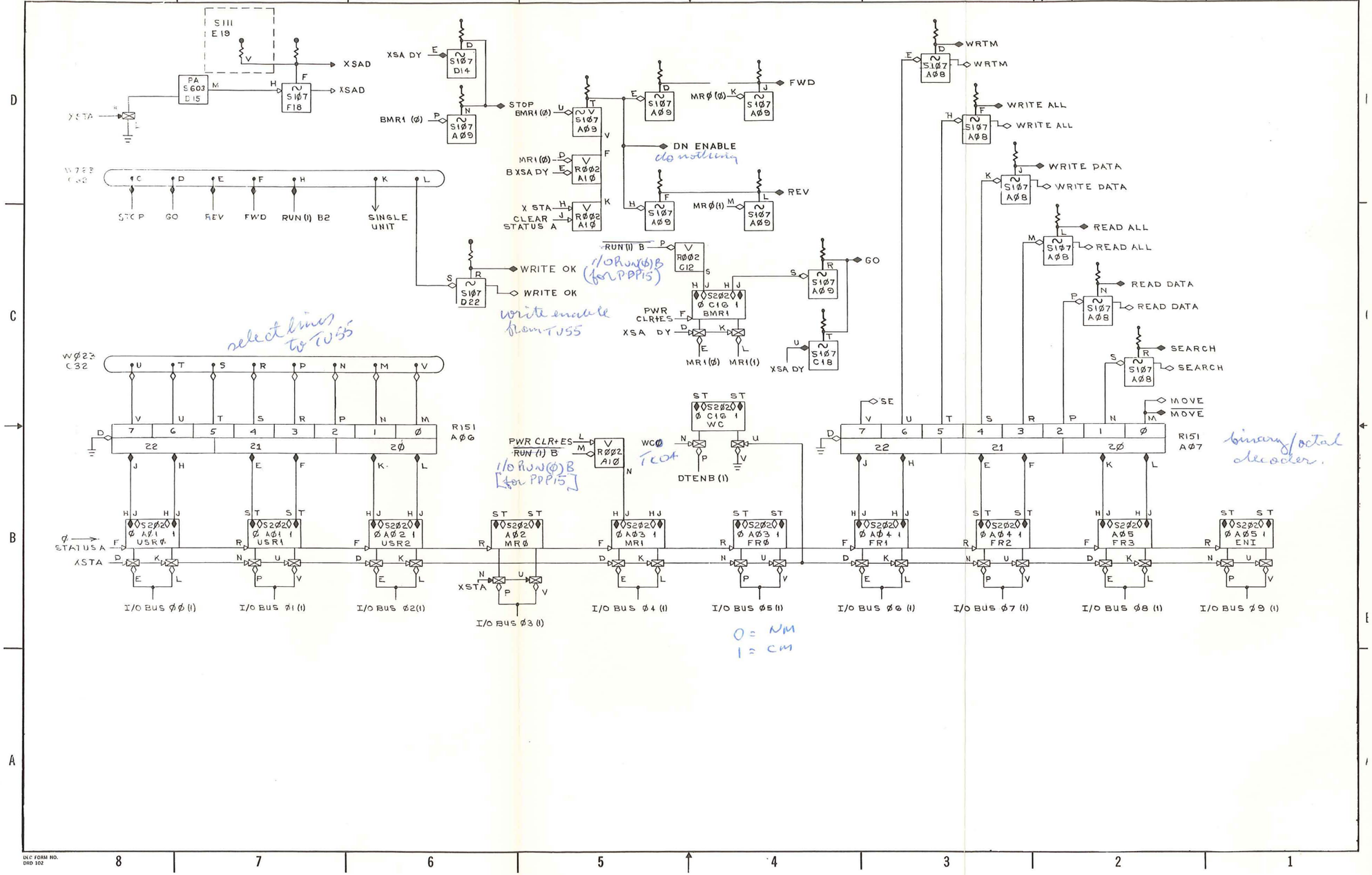

W85Ø EFØ2
W85Ø EFØ6
ED ED I/O SYNC
EE EE I/OP 1
EH EH I/OP 2
EK EK I/OP 4
EM EM SKIP RQ
EP EP PROG INT RQ
ES ES READ RQ
ET ET RD STATUS
EV EV I/O PWR CLR
W85Ø EFØ2
W85Ø EFØ6
FD FD DSØ
FE FE DS1
FH FH DS2
FK FK DS3
FM FM DS4
FP FP DS5
FS FS SDØ
FT FT SD1
FV FV
W85Ø EFØ3
W85Ø EFØ7
ED ED RUN (1) B
EE EE
EH EH I/Ø OFLO
EK EK I/O ADDR Ø3
EM EM I/O ADDR Ø4
EP EP I/O ADDR Ø5
ES ES I/O ADDR Ø6
ET ET I/O ADDR Ø7
EV EV I/O ADDR Ø8
W85Ø EFØ3
W85Ø EFØ7
FD FD I/O ADDR Ø9
FE FE I/O ADDR 1Ø
FH FH I/O ADDR 11
FK FK I/O ADDR 12
FM FM I/O ADDR 13
FP FP I/O ADDR 14
FS FS I/O ADDR 15
FT FT I/O ADDR 16
FV FV I/O ADDR 17
W85Ø EFØ4
W85Ø EFØ8
ED ED WRITE RQ
EE EE INC MB
EH EH +1 → CA INH
EK EK API Ø RQ
EM EM API Ø GR
EP EP API Ø EN
ES ES API 1 RQ
ET ET API 1 GR
EV EV API 1 EN OUT
API 1 EN IN
W85Ø EFØ4
W85Ø EFØ8
FD FD API 2 RQ
FE FE API 2 GR
FH FH API 2 EN
FK FK API 3 RQ
FM FM API 3 GR
FP FP API 3 EN
FS FS DCH RQ
FT FT DCH GRANT
FV FV DCH EN OUT
DCH EN IN
from DW15
clear
IN read
OUT read
skip EF
DS W103 EFØ9 (75) (1Ø)
DS W103 EF1Ø (75) (11)
DS W103 EF11 76
EE CSTA
EF CSTA
EL RSTA
EM RSTA
ES XSTA
ET XSTA
EE SEF
EF SEF
EL RSTB
EM RSTB
ES
ET
read
EE SDTF
EF SDTF
EL RDTB
EM RDTB
ES LDTB
ET LDTB
IOP1 skip DTF
IOP2 read DTB
IOP4 load DTB
I/OP 1
I/OP 2
I/OP 4
ED EK ER
EH 1
EJ FE
EU 4 EV
DSØ DS1 DS2 DS3 DS4 DS5 SDØ SD1
FE FF FH FJ FK FL FM FN FP FR FS FT FU FV
FD
SELECT (76)
automatic generation of assertion
I/O OFLO
S107 F18
WCO
DS4
S107 D14
DS4
DS5
SD1
SD
I/O PWR.CLR.
PWR CLR
I/O PWR(L)
RUN(1) B
RUN (1) B2
PA S603 D15
Ø → STATUSA
TCT
CSTA
S111 F16
SKIP RQ
SDTF
DTF(1)
S123 DØ3
SEF
EF(1)
S123 D13
skip error flag
PA WG4Ø D11
PA WG4Ø D1Ø
RSTA → STA → I/O BUS
RSTB → STB → I/O BUS
RDTB → DTB → I/O BUS ØØ-Ø9
RDTB → DTB → I/O BUS 1Ø-17
TO TC03

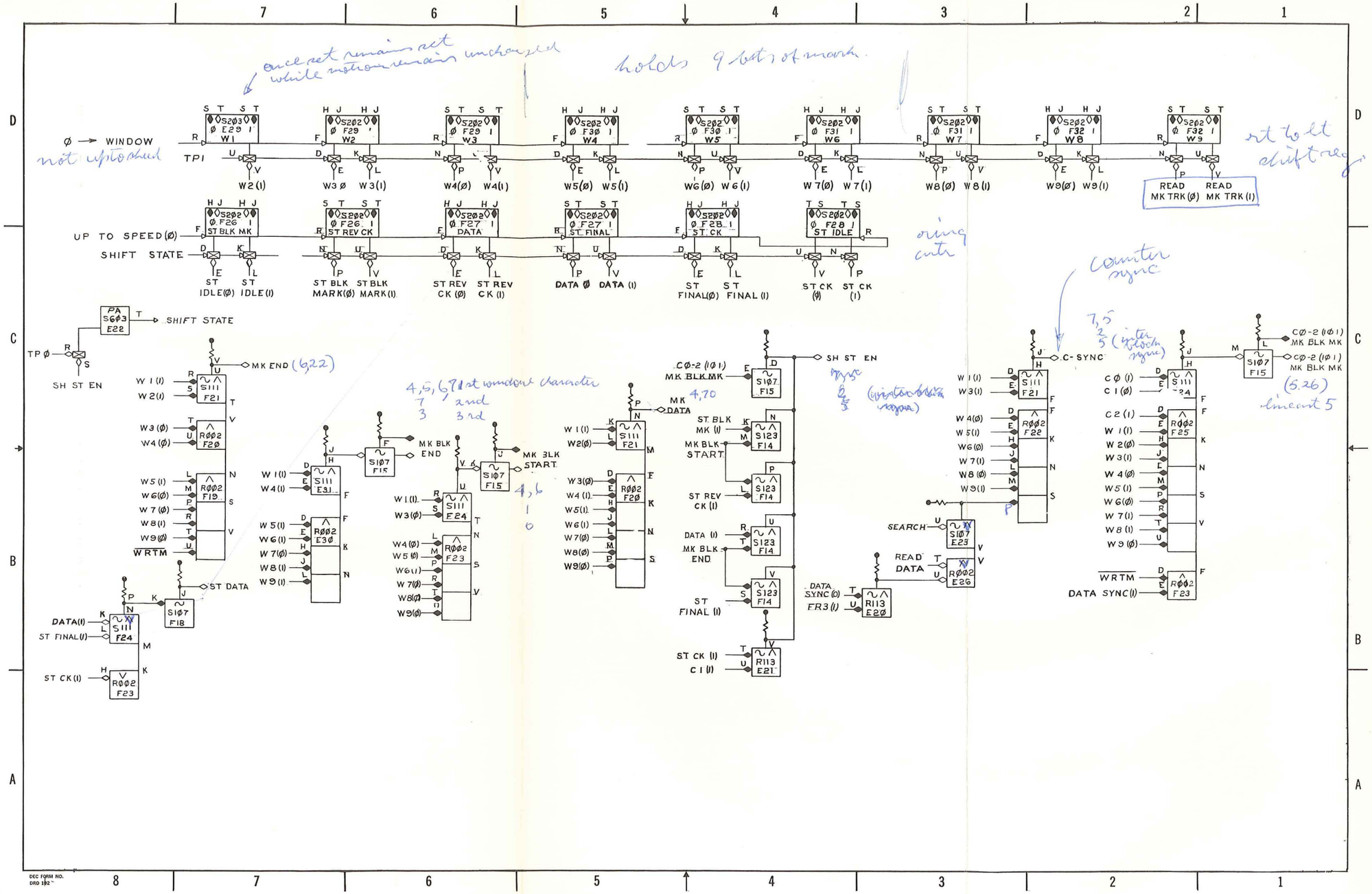


D-BS-TC02-0-5 ERRORS, MCP Switch

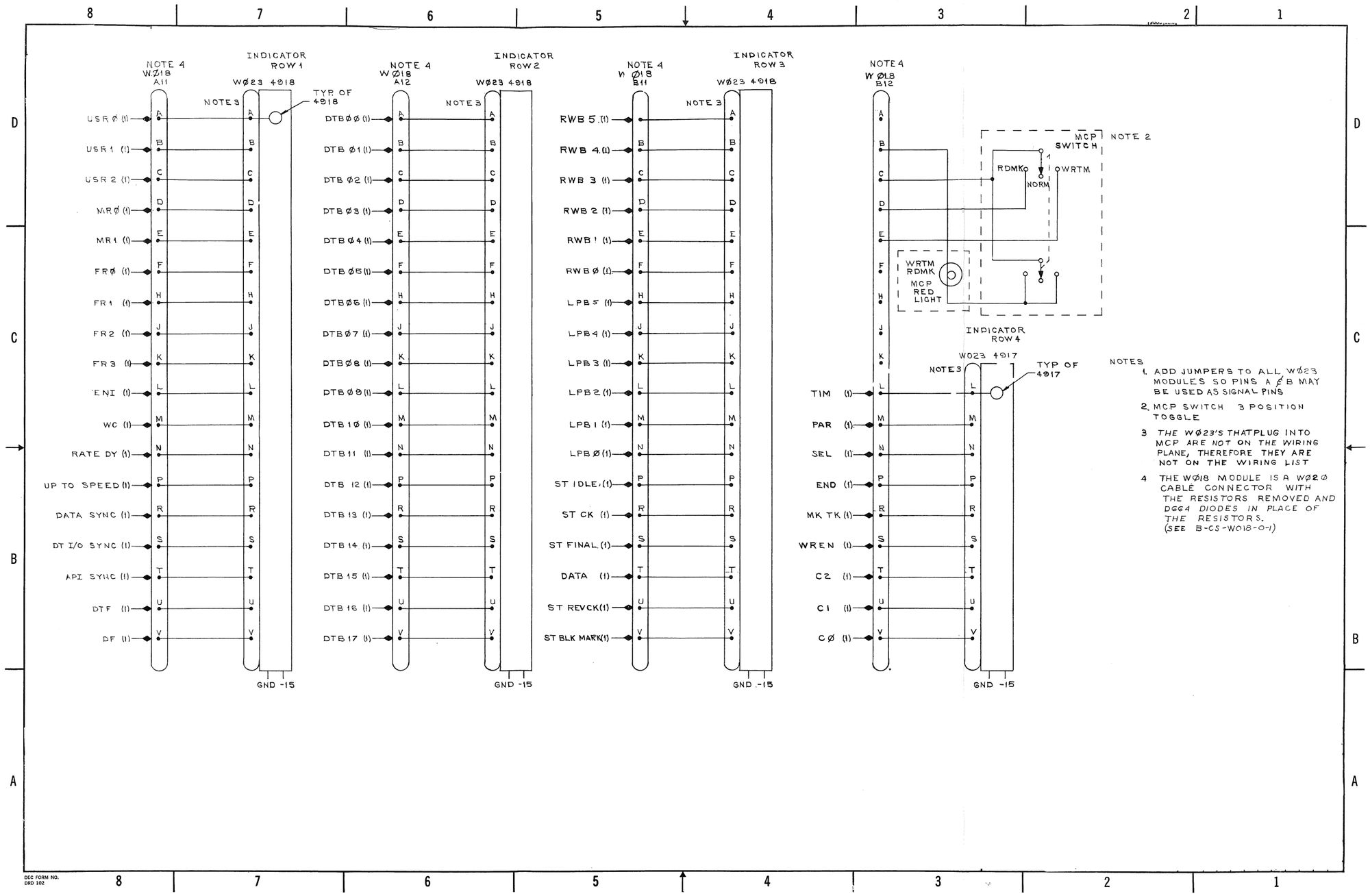


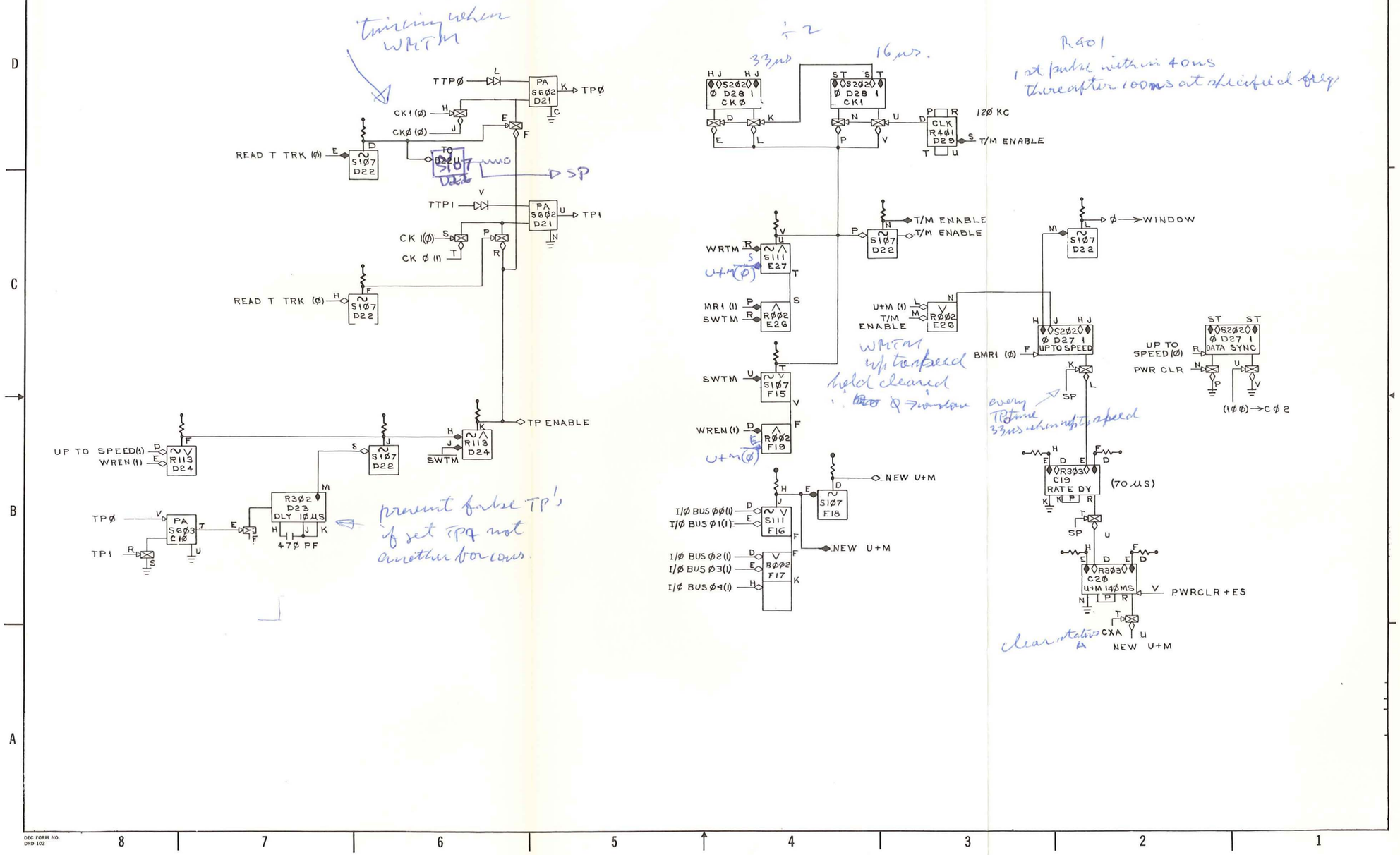
D-BS-TC02-0-6 CONTROL

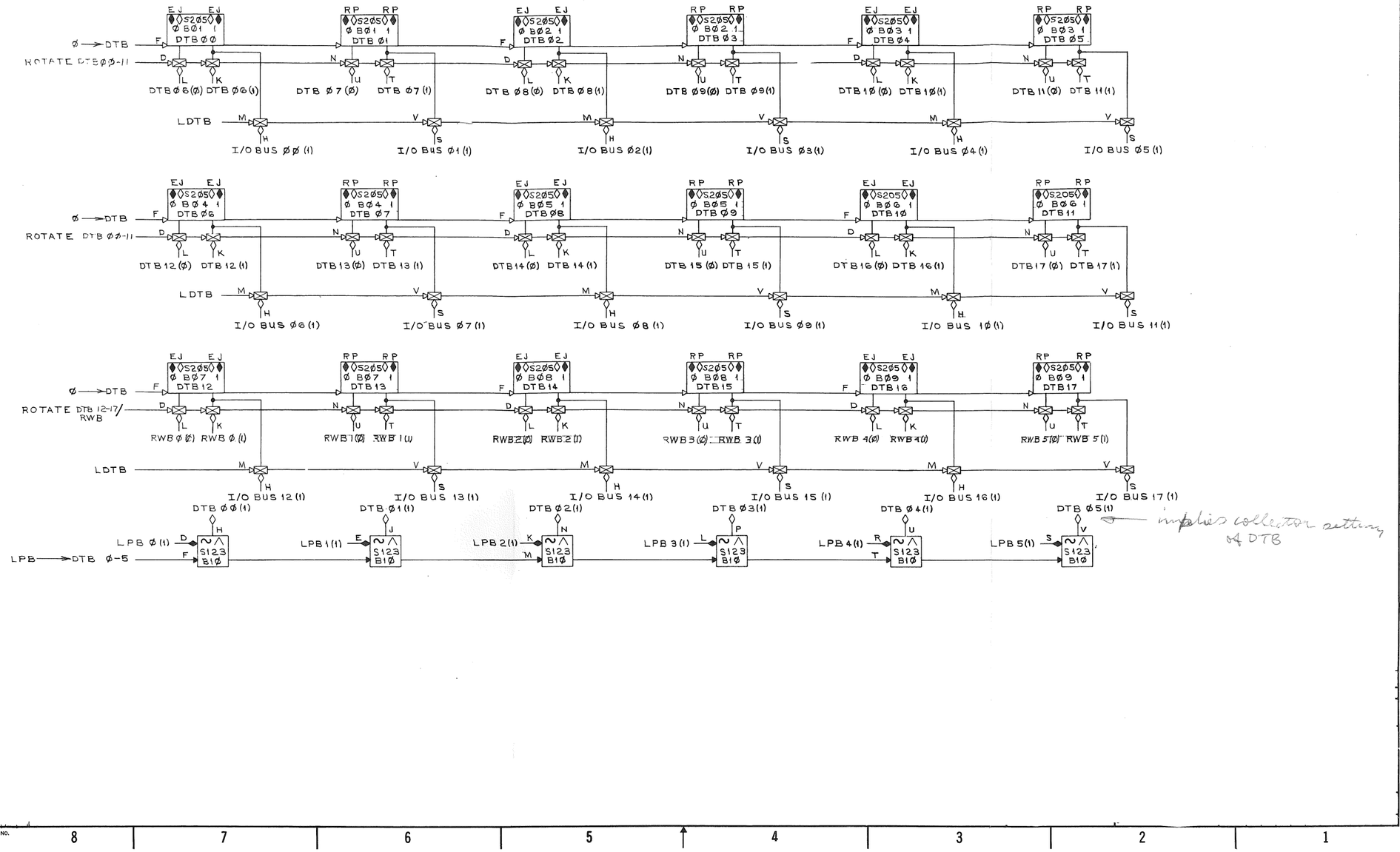

XSAD
XSAD
XSTA
XSA DY
BMR1 (Ø)
STOP
BMR1 (Ø)
MR1(Ø)
B XSA DY
X STA
CLEAR STATUS A
DN ENABLE
do nothing
MRØ (Ø)
FWD
MRØ (1)
REV
STOP
GO
REV
FWD
RUN (1) B2
SINGLE UNIT
WRITE OK
WRITE OK
write enable from TV55
select lines to TV55
RUN (1) B
1/O RUN(Ø)B (for PPP15)
PWR CLRES
XSA DY
MR1(Ø)
MR1(1)
GO
XSA DY
WRTM
WRTM
WRITE ALL
WRITE ALL
WRITE DATA
WRITE DATA
READ ALL
READ ALL
READ DATA
READ DATA
SEARCH
SEARCH
MOVE
MOVE
SE
R151 AØ6
R151 AØ7
binary/octal decoder.
PWR CLR+ES
RUN (1) B
1/O RUN(Ø)B [for PPP15]
WCØ TCØT
DTENB (1)
Ø STATUS A
XSTA
USRØ
USR1
USR2
MR2
MR1
MRØ
FR3
FR2
FR1
FR0
ENI
I/O BUS ØØ (1)
I/O BUS Ø1 (1)
I/O BUS Ø2 (1)
I/O BUS Ø3 (1)
I/O BUS Ø4 (1)
I/O BUS Ø5 (1)
I/O BUS Ø6 (1)
I/O BUS Ø7 (1)
I/O BUS Ø8 (1)
I/O BUS Ø9 (1)
0 = NM
1 = CM

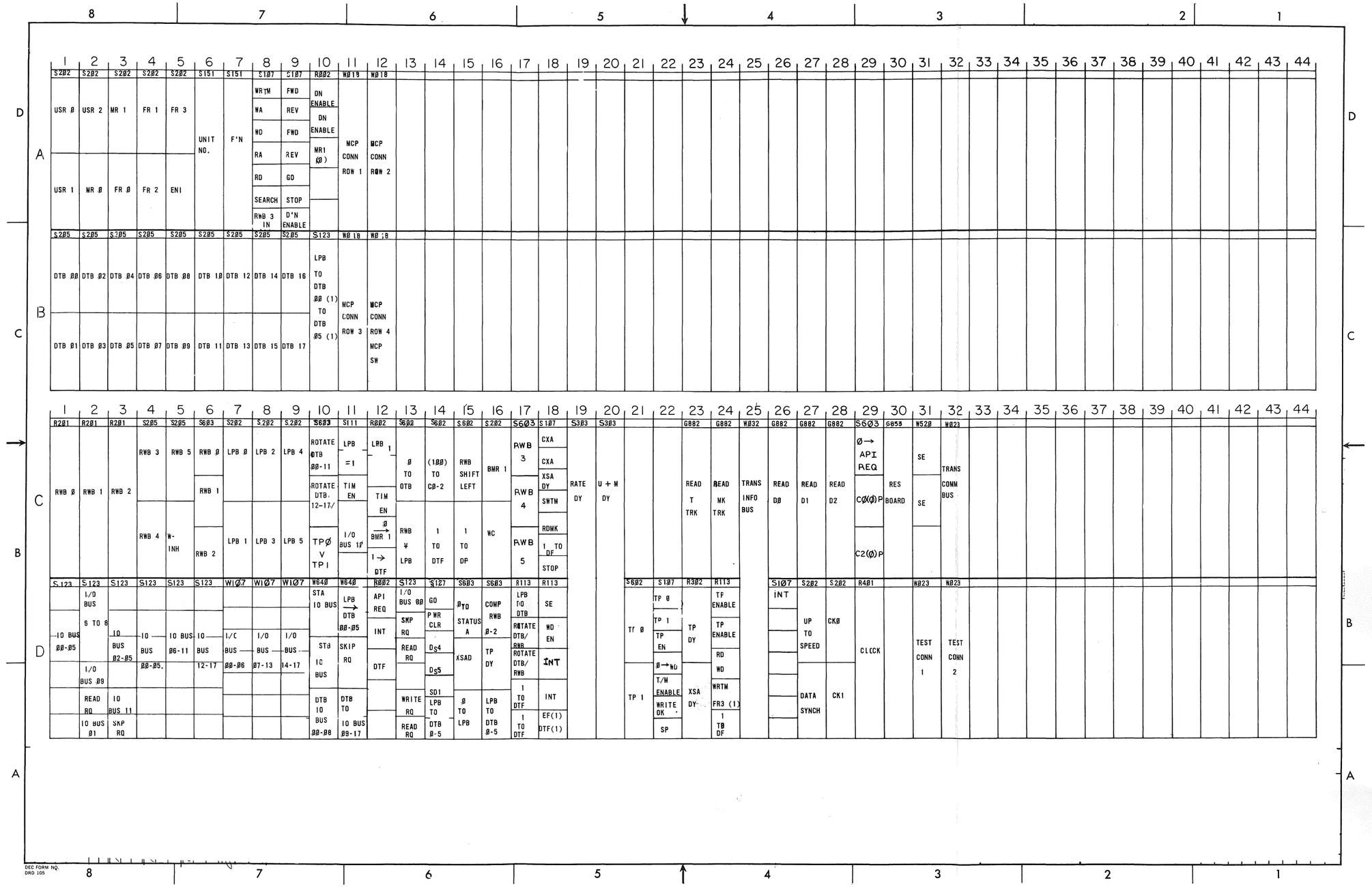


D-BS-TC02-0-8 WINDOW, MK, TK, STATE

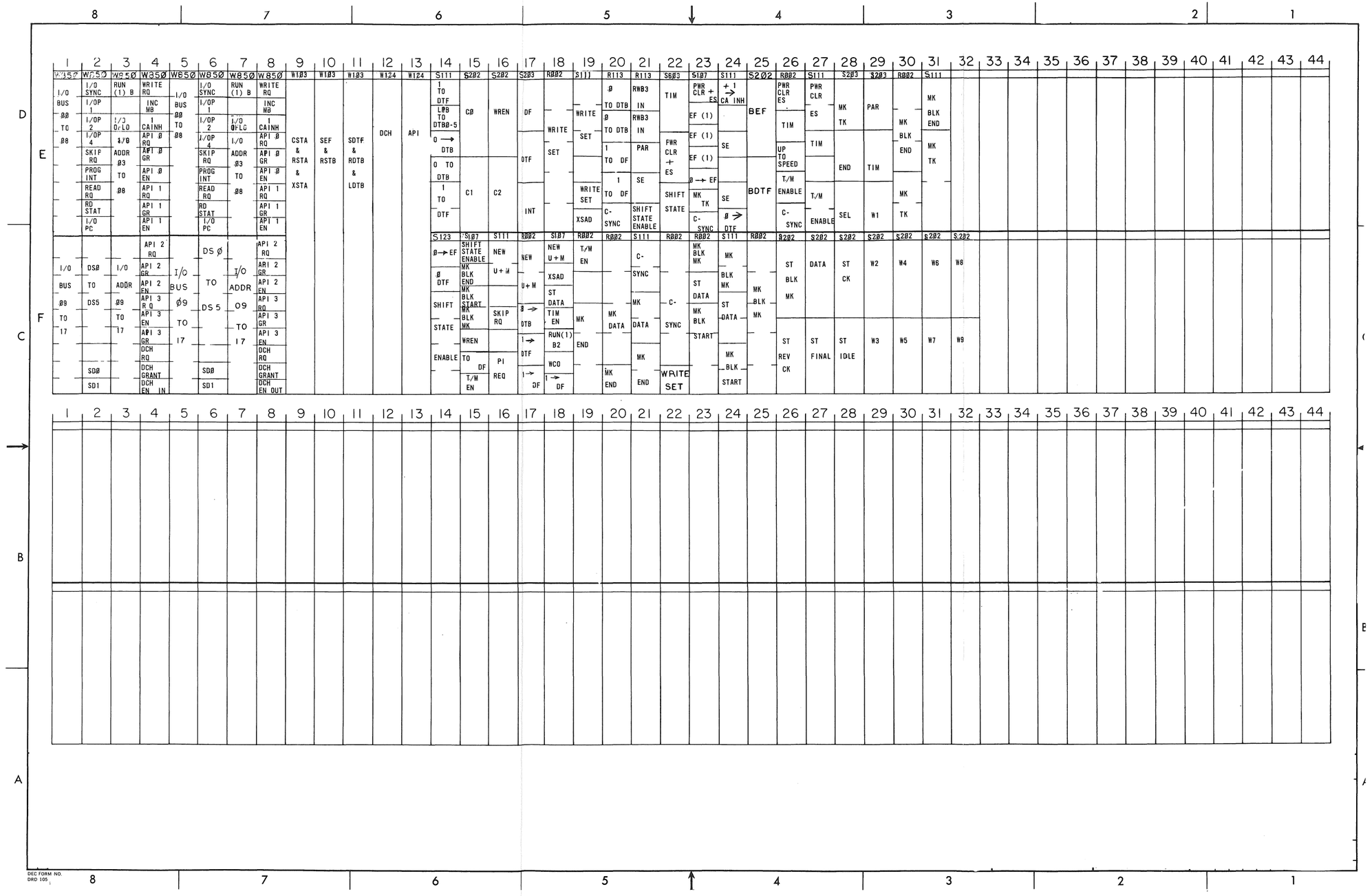

NOTE 4
W018
A11
INDICATOR
ROW 1
W023 4918
NOTE 3
TYP OF
4918
USR Ø (1)
USR 1 (1)
USR 2 (1)
MRØ (1)
MR1 (1)
FRØ (1)
FR1 (1)
FR2 (1)
FR3 (1)
ENI (1)
WC (1)
RATE DY (1)
UP TO SPEED (1)
DATA SYNC (1)
DT I/O SYNC (1)
API SYNC (1)
DTF (1)
DF (1)
GND -15
NOTE 4
W018
A12
INDICATOR
ROW 2
W023 4918
NOTE 3
DTBØØ (1)
DTB Ø1 (1)
DTB Ø2 (1)
DTB Ø3 (1)
DTB Ø4 (1)
DTB Ø5 (1)
DTB Ø6 (1)
DTB Ø7 (1)
DTB Ø8 (1)
DTB Ø9 (1)
DTB 10 (1)
DTB 11 (1)
DTB 12 (1)
DTB 13 (1)
DTB 14 (1)
DTB 15 (1)
DTB 16 (1)
DTB 17 (1)
GND -15
NOTE 4
W018
B11
INDICATOR
ROW 3
W023 4918
NOTE 3
RWB 5 (1)
RWB 4 (1)
RWB 3 (1)
RWB 2 (1)
RWB 1 (1)
RWB Ø (1)
LPB 5 (1)
LPB 4 (1)
LPB 3 (1)
LPB 2 (1)
LPB 1 (1)
LPB Ø (1)
ST IDLE (1)
ST CK (1)
ST FINAL (1)
DATA (1)
ST REVCK (1)
ST BLK MARK (1)
GND -15
NOTE 4
W018
B12
MCP
SWITCH
NOTE 2
RDMK
NORM
WRTM
WRTM
RDMK
MCP
RED
LIGHT
INDICATOR
ROW 4
W023 4917
NOTE 3
TYP OF
4917
TIM (1)
PAR (1)
SEL (1)
END (1)
MK TK (1)
WREN (1)
C2 (1)
C1 (1)
CØ (1)
GND -15
NOTES
1. ADD JUMPERS TO ALL W023 MODULES SO PINS A & B MAY BE USED AS SIGNAL PINS
2. MCP SWITCH 3 POSITION TOGGLE
3 THE W023'S THAT PLUG INTO MCP ARE NOT ON THE WIRING PLANE, THEREFORE THEY ARE NOT ON THE WIRING LIST
4 THE W018 MODULE IS A W020 CABLE CONNECTOR WITH THE RESISTORS REMOVED AND DGGA DIODES IN PLACE OF THE RESISTORS. (SEE B-CS-W018-0-1)
DEC FORM NO. DRD 102


timing when WRTM
TTPØ
PA S6Ø2 D21
TPØ
CK1(Ø)
CKØ(Ø)
READ T TRK (Ø)
S1Ø7 D22
SP
TTP1
TP1
CK 1(Ø)
CK Ø (1)
TP ENABLE
UP TO SPEED(1)
WREN(1)
R113 D24
SWTM
R3Ø2 D23 DLY 1ØµS
47Ø PF
TPØ
TP1
PA S6Ø3 C1Ø
present false TP's if set TP4 not another bonus.
÷2
33mS
16mS.
R401
1st pulse within 40mS
thereafter 100mS at specified freq
S2Ø2 Ø D28 1 CKØ
S2Ø2 Ø D28 1 CK1
12Ø KC
CLK R4Ø1 D28
T/M ENABLE
WRTM
U+M(Ø)
S111 E27
MR1 (1)
SWTM
RØØ2 E26
U+M (1)
T/M ENABLE
RØØ2 E26
SWTM
S1Ø7 F15
WREN(1)
RØØ2 F18
U+M(Ø)
WRTM up to speed held cleared
every TP time 33mS when up to speed
SP
NEW U+M
I/Ø BUS ØØ(1)
I/Ø BUS Ø1(1)
S111 F16
I/Ø BUS Ø2(1)
I/Ø BUS Ø3(1)
I/Ø BUS Ø4(1)
RØØ2 F17
NEW U+M
Ø → WINDOW
S2Ø2 Ø D27 1 UP TO SPEED
BMR1 (Ø)
R3Ø3Ø C19 RATE DY
(70 µS)
SP
R3Ø3Ø C2Ø U+M 14ØMS
PWRCLR + ES
CXA
NEW U+M
clear status A
S2Ø2 Ø D27 1 DATA SYNC
UP TO SPEED (Ø)
PWR CLR
(1ØØ) → CØ2

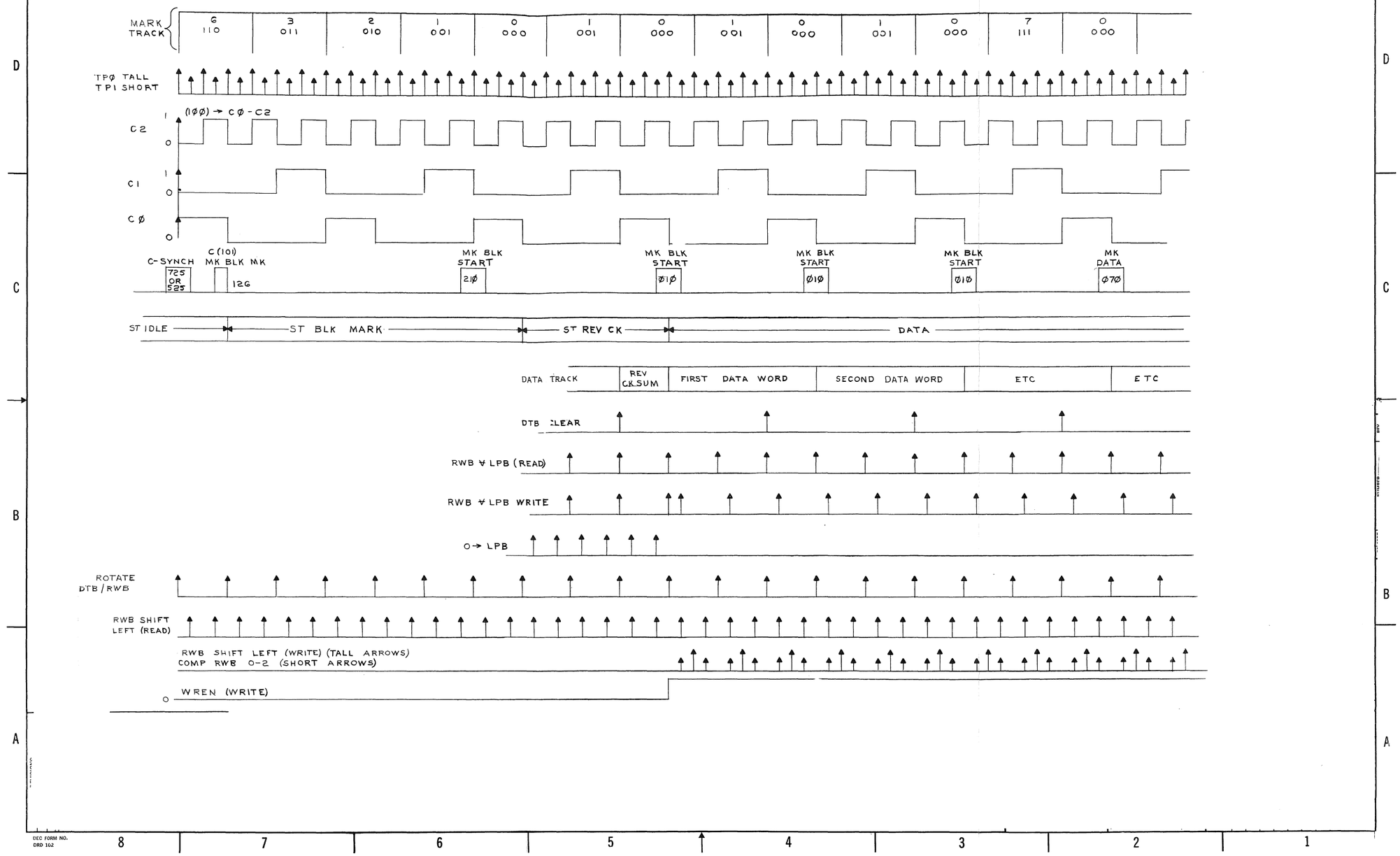

Ø → DTB
ROTATE DTB ØØ-11
DTB ØØ
DTB Ø1
DTB Ø2
DTB Ø3
DTB Ø4
DTB Ø5
DTB Ø6(Ø) DTB Ø6(1)
DTB Ø7(Ø) DTB Ø7(1)
DTB Ø8(Ø) DTB Ø8(1)
DTB Ø9(Ø) DTB Ø9(1)
DTB 1Ø(Ø) DTB 1Ø(1)
DTB 11(Ø) DTB 11(1)
LDTB
I/O BUS ØØ (1)
I/O BUS Ø1 (1)
I/O BUS Ø2(1)
I/O BUS Ø3(1)
I/O BUS Ø4 (1)
I/O BUS Ø5 (1)
Ø → DTB
ROTATE DTB ØØ-11
DTB Ø6
DTB Ø7
DTB Ø8
DTB Ø9
DTB 1Ø
DTB 11
DTB 12(Ø) DTB 12 (1)
DTB 13(Ø) DTB 13 (1)
DTB 14(Ø) DTB 14 (1)
DTB 15 (Ø) DTB 15 (1)
DTB 16(Ø) DTB 16(1)
DTB 17 (Ø) DTB 17 (1)
LDTB
I/O BUS Ø6 (1)
I/O BUS Ø7 (1)
I/O BUS Ø8 (1)
I/O BUS Ø9 (1)
I/O BUS 1Ø (1)
I/O BUS 11 (1)
Ø → DTB
ROTATE DTB 12-17/ RWB
DTB 12
DTB 13
DTB 14
DTB 15
DTB 16
DTB 17
RWB Ø (Ø) RWB Ø (1)
RWB 1(Ø) RWB 1 (1)
RWB 2(Ø) RWB 2 (1)
RWB 3 (Ø) RWB 3 (1)
RWB 4(Ø) RWB 4(1)
RWB 5(Ø) RWB 5 (1)
LDTB
I/O BUS 12 (1)
I/O BUS 13 (1)
I/O BUS 14 (1)
I/O BUS 15 (1)
I/O BUS 16 (1)
I/O BUS 17 (1)
DTB ØØ (1)
DTB Ø1 (1)
DTB Ø2 (1)
DTB Ø3 (1)
DTB Ø4 (1)
DTB Ø5 (1)
implies collector setting of DTB
LPB → DTB Ø-5
LPB Ø (1)
LPB 1 (1)
LPB 2 (1)
LPB 3 (1)
LPB 4 (1)
LPB 5 (1)
S123
B1Ø
DEC FORM NO. DRD 102



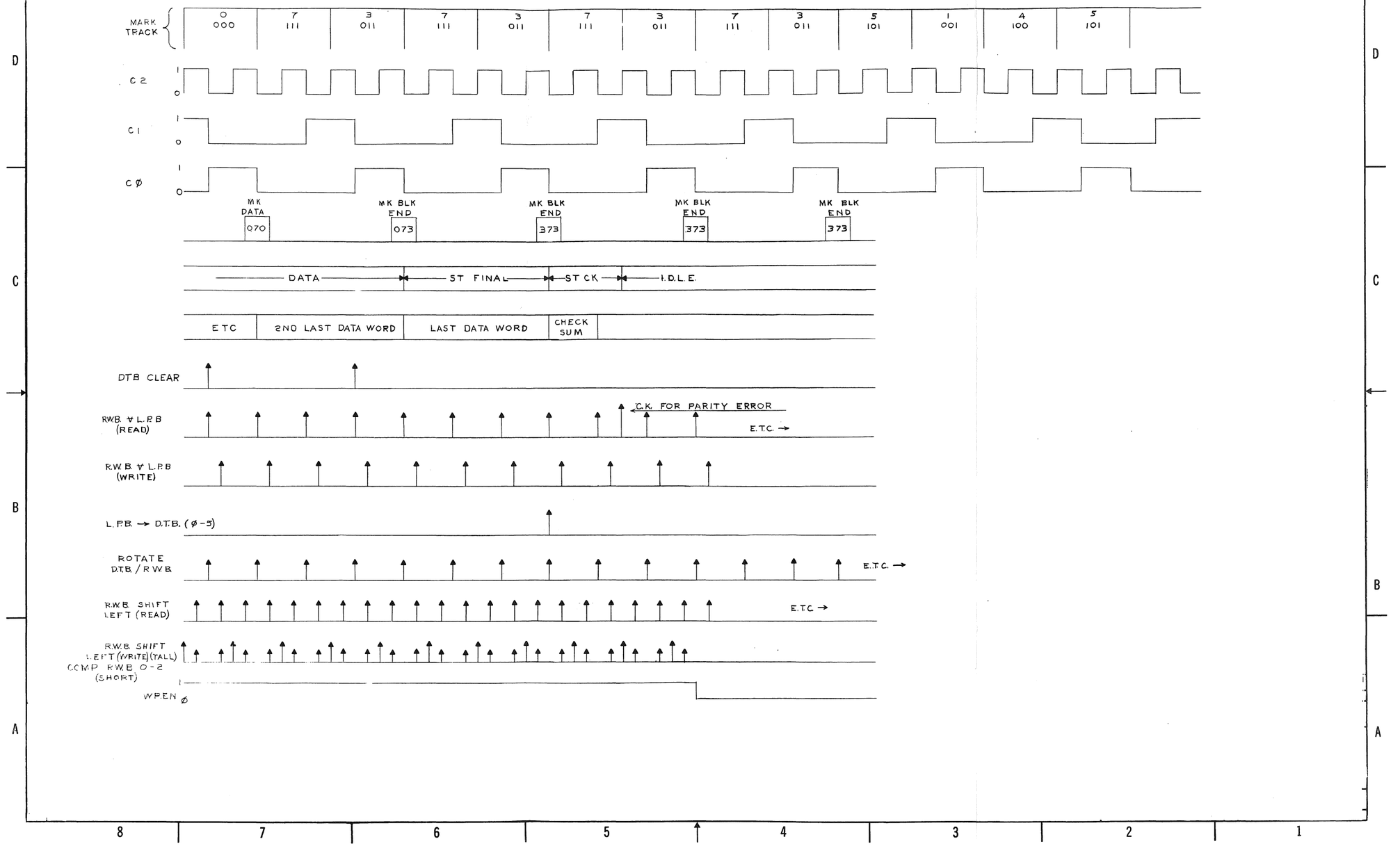
D-MU-TC02-0-13 Module list Panels A-F
(Sheet 1)



D-MU-TC02-0-13 Module list Panels A-F
(Sheet 2)

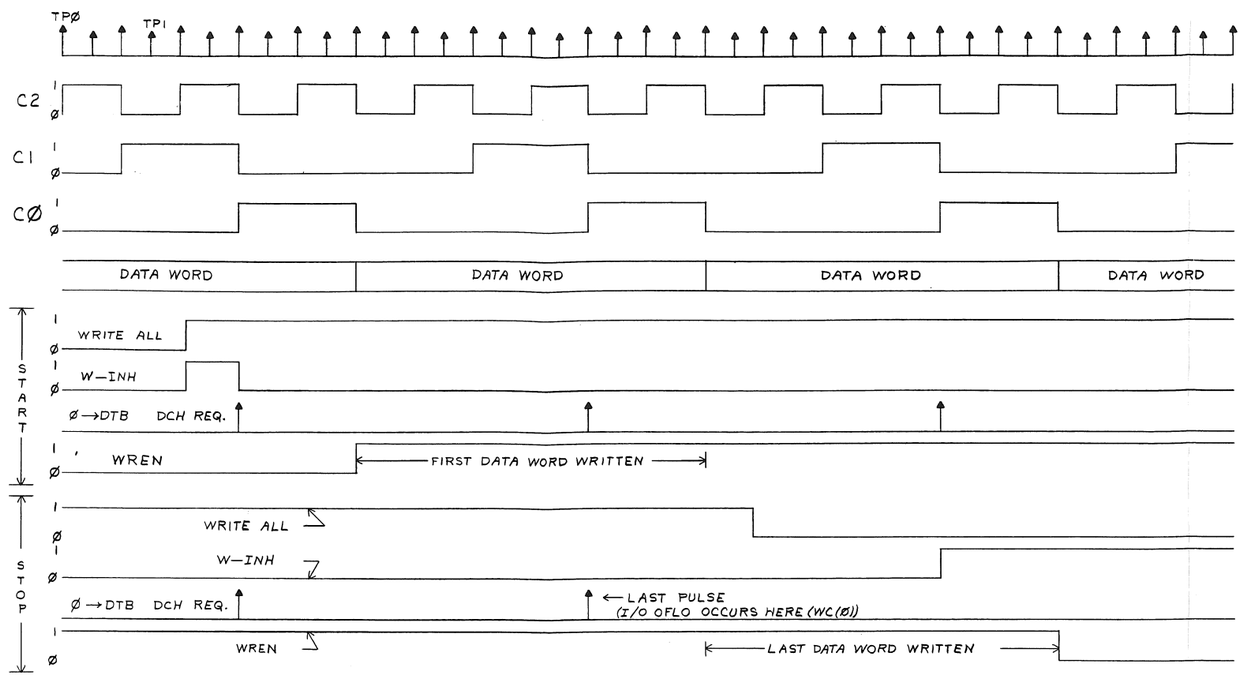


D-TD-TC02-0-15 Timing
(Sheet 1)



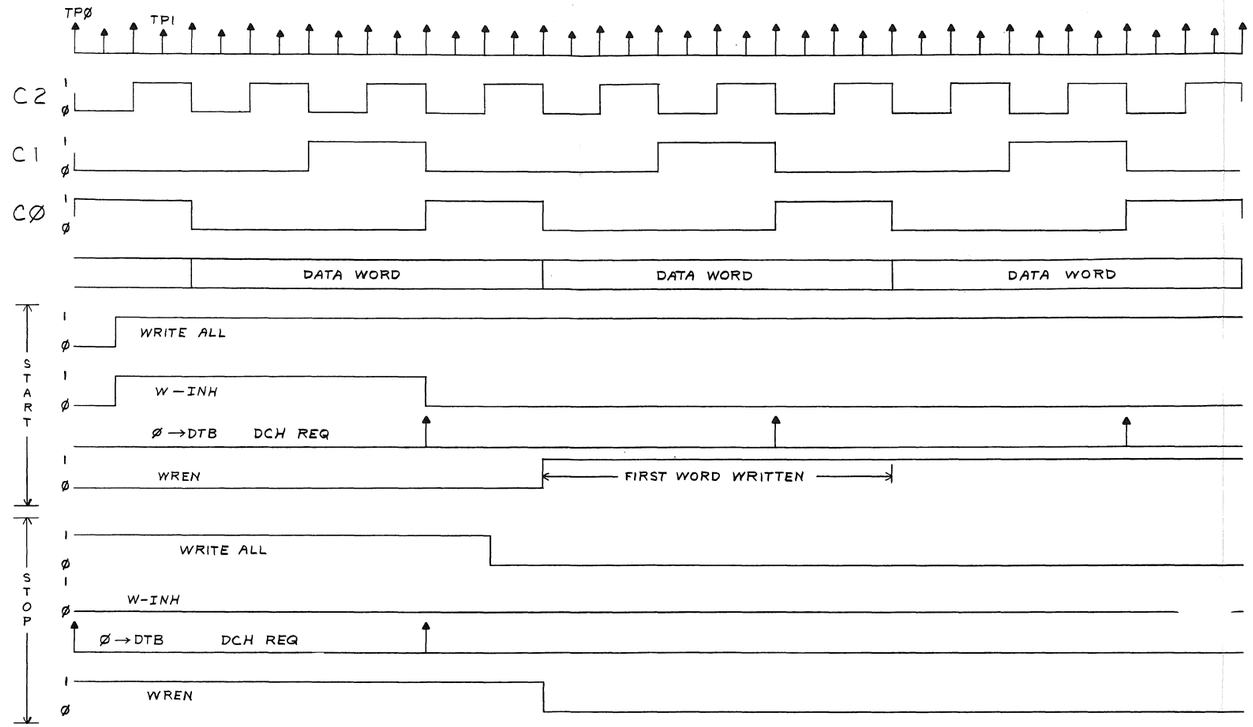
D-TD-TC02-0-15 Timing
(Sheet 2)

WRITE ALL COMMAND WHEN CØ=Ø

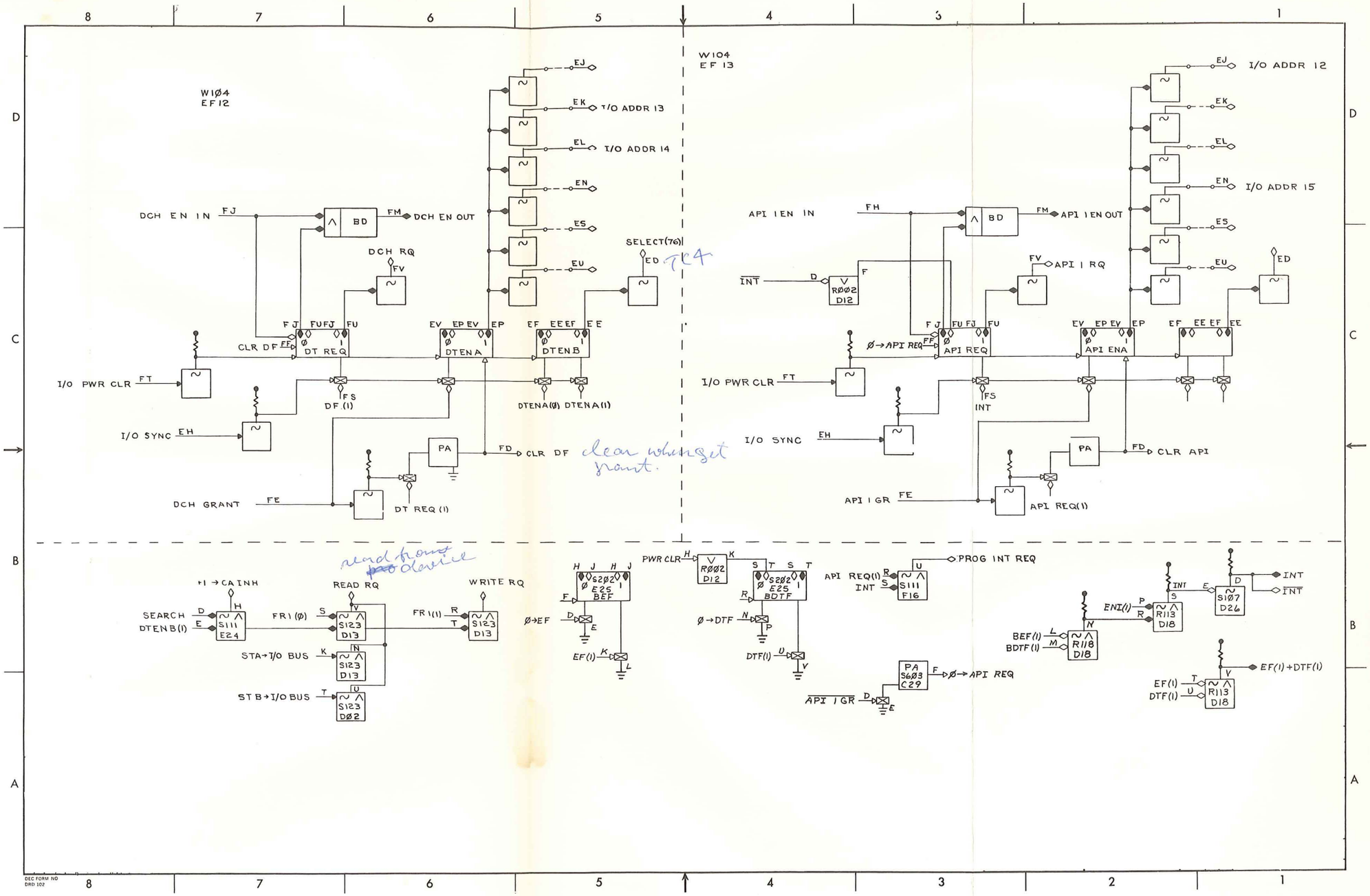


D-TD-TC02-0-15 Timing
(Sheet 3)

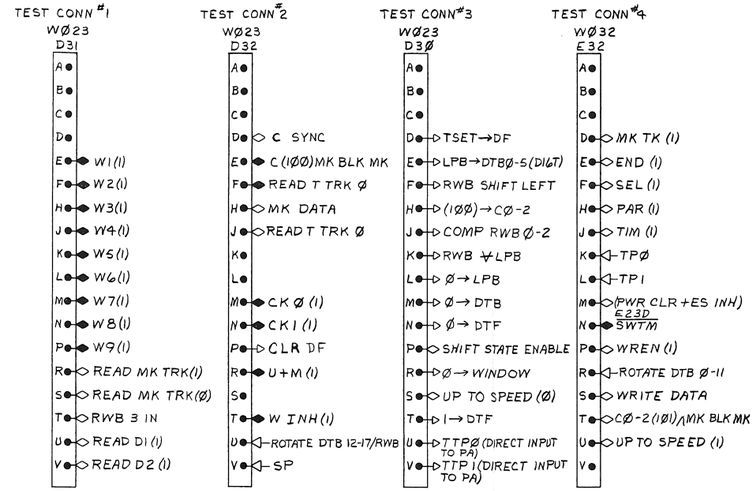
WRITE ALL COMMAND WHEN CØ=1

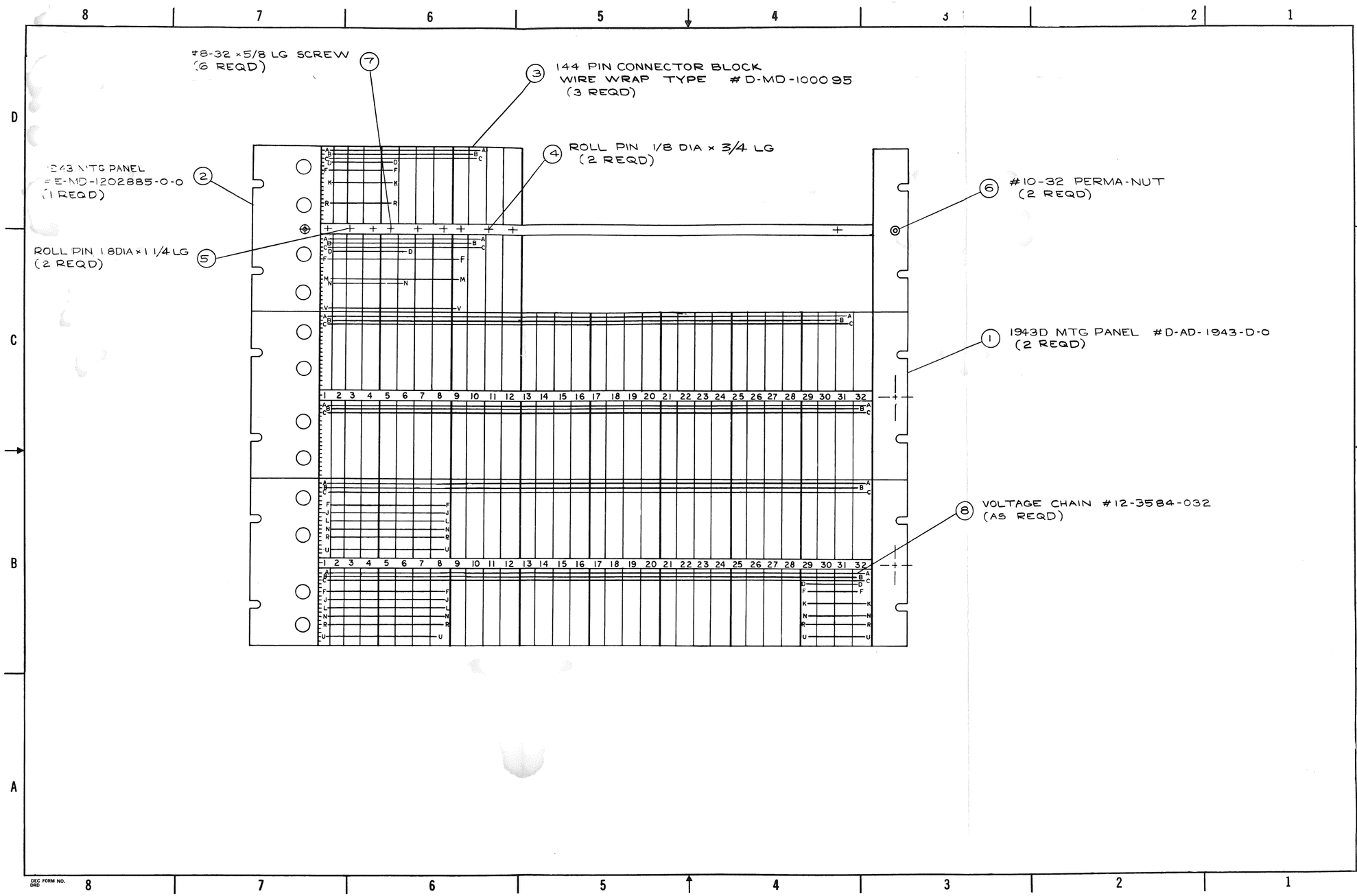


D-TD-TC02-0-15 Timing
(Sheet 4)



D-BS-TC02-0-16 DCH, API


TEST CONN #1
WØ23
D31
A
B
C
D
E W1 (1)
F W2 (1)
H W3 (1)
J W4 (1)
K W5 (1)
L W6 (1)
M W7 (1)
N W8 (1)
P W9 (1)
R READ MK TRK (1)
S READ MK TRK (Ø)
T RWB 3 IN
U READ D1 (1)
V READ D2 (1)
TEST CONN #2
WØ23
D32
A
B
C
D C SYNC
E C (1ØØ) MK BLK MK
F READ T TRK Ø
H MK DATA
J READ T TRK Ø
K
L
M CK Ø (1)
N CK1 (1)
P CLR DF
R U+M (1)
S
T W INH (1)
U ROTATE DTB 12-17/RWB
V SP
TEST CONN #3
WØ23
D3Ø
A
B
C
D TSET → DF
E LPB → DTBØ-5 (DIGT)
F RWB SHIFT LEFT
H (1ØØ) → CØ-2
J COMP RWB Ø-2
K RWB ∀ LPB
L Ø → LPB
M Ø → DTB
N Ø → DTF
P SHIFT STATE ENABLE
R Ø → WINDOW
S UP TO SPEED (Ø)
T 1 → DTF
U TTPØ (DIRECT INPUT TO PA)
V TTP 1 (DIRECT INPUT TO PA)
TEST CONN #4
WØ32
E32
A
B
C
D MK TK (1)
E END (1)
F SEL (1)
H PAR (1)
J TIM (1)
K TPØ
L TP1
M (PWR CLR + ES INH) E23D
N SWTM
P WREN (1)
R ROTATE DTB Ø-11
S WRITE DATA
T CØ-2 (1Ø1) ∧ MK BLK MK
U UP TO SPEED (1)
V


#8-32 x 5/8 LG SCREW (6 REQD)
7
3
144 PIN CONNECTOR BLOCK WIRE WRAP TYPE # D-MD-100095 (3 REQD)
4
ROLL PIN 1/8 DIA x 3/4 LG (2 REQD)
1943 MTG PANEL # E-MD-1202885-0-0 (1 REQD)
2
ROLL PIN 1 8DIA x 1 1/4 LG (2 REQD)
5
6
#10-32 PERMA-NUT (2 REQD)
1
1943D MTG PANEL # D-AD-1943-D-0 (2 REQD)
8
VOLTAGE CHAIN # 12-3584-032 (AS REQD)
DEC FORM NO. DRD

Digital Equipment Corporation
Maynard, Massachusetts

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