AR11
user's guide

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AR11
user's guide

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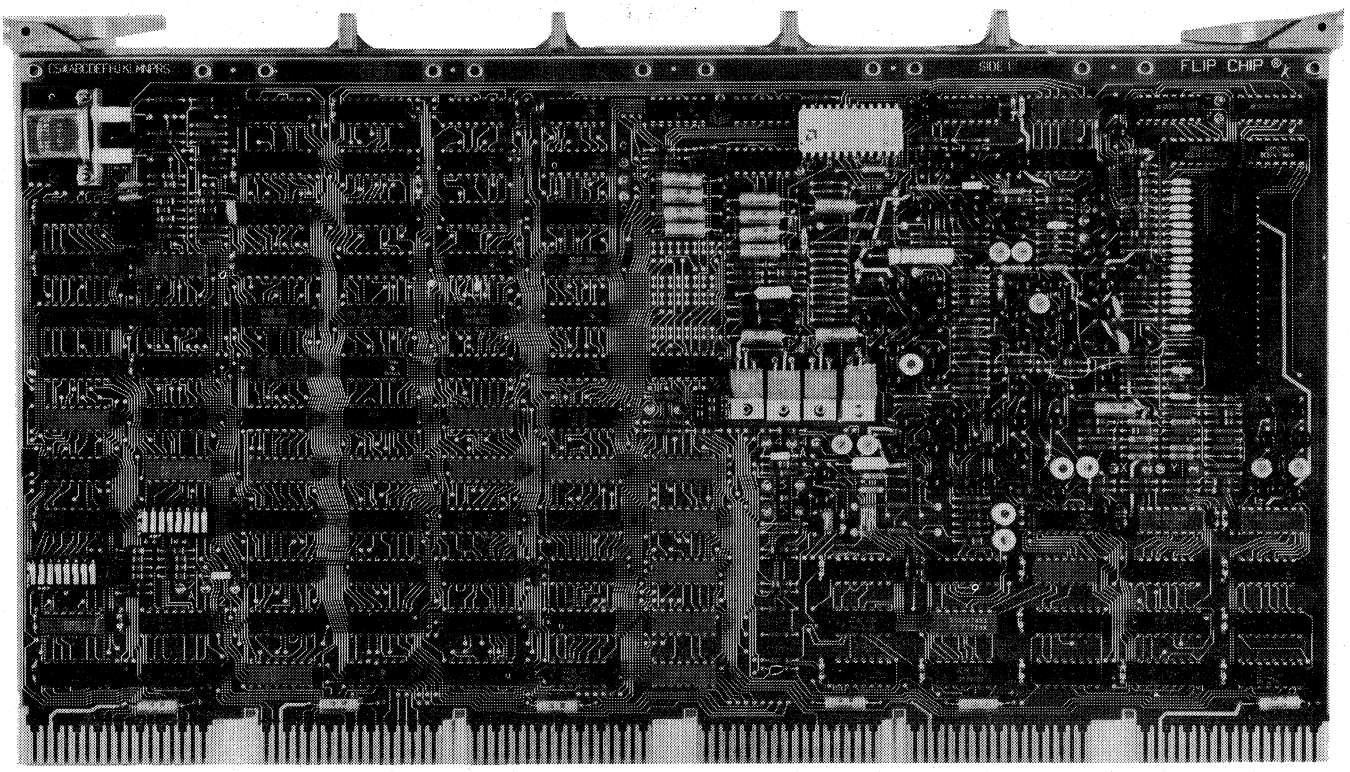

7047-1

AR11 Module

CHAPTER 1
AR11

1.1 INTRODUCTION

The AR11 is a one-module real-time analog subsystem that interfaces with the PDP-11 family of computers via a "hex" small peripheral controller slot. The flexibility of the system makes it well suited to a variety of applications, including biomedical research, analytical instrumentation, data collection, monitoring, data logging, industrial testing, engineering, and technical education.

1.2 SCOPE OF MANUAL

This manual contains the information necessary to use the AR11 effectively. Chapter 1 describes the AR11 and the interrelationship of its parts from a functional standpoint. Chapters 2 through 4 cover the A/D converter, real-time clock, and display control, respectively. Each chapter contains a detailed functional description, interfacing information, and programming information. Register addresses, vector addresses, and programmer's reference information are listed in Appendix A.

1.3 DESCRIPTION

The AR11 includes a 16-channel, 10-bit A/D converter with sample-and-hold, a programmable real-time clock with one external input, and a display control with two 10-bit D/A converters. It also includes all the Unibus interfacing logic necessary for control in a small peripheral controller slot, plus a transformerless dc-to-dc converter allowing use of only +5 V power. The system programming is a subset of the LPS11 and is supported under BASIC, FORTRAN, and appropriate Lab Application-11 modules.

1.3.1 Packaging

The AR11 is housed on one "hex" size module and uses only +5 V power at 3.5 A typical, 5 A maximum. Since the AR11 is a hex size module, it can occupy one of the center two slots of the DD11-B or any processor SPC slot with physical room for a hex module. Access to the AR11's input/output signals is through a single Berg Connector mounted in the upper right-hand corner of the module. A Berg cable mating housing* and enough pins† (including 50 percent spares) for construction of a mating cable are included in the AR11 option.‡ A BC11L-20 cable (Berg connector to open end) or a BC08 cable (Berg to Berg) plus an H322 distribution panel may also be used to connect input/output signals to the AR11. Berg cable pin assignments are shown in Table 1-1.

1.3.2 Bus Control

The AR11 bus control provides a single interface between the PDP-11 Unibus and the AR11's A/D converter, real-time clock, and display control. The bus control decodes eight sequential device addresses used by the AR11, permitting the PDP-11 to address the various status and data registers and transfer data. The relationship between the bus control and the functional parts of the AR11 is shown in Figure 1-1.

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* DEC part number 12-10918-15.
† DEC part number 12-10089-4.
‡ Cable should be constructed using a Berg HT66/HT68 crimping tool or its equivalent.

Table 1-1
Berg Cable Pin Assignments

Pin	Signal
A	Scope control – WRITE THRU L
B	Scope control – DISP CH02 L
C	Scope control – ERASE L
D	Scope control – INTENSIFY
E	Scope control – NON-STORE L
F	Scope control – X OUT
H	Scope control – ERASE RET L
J	Scope control – Y OUT
K	Analog ground
L	A/D CH 17 input
M	Analog ground
N	A/D CH 16 input
P	Logic ground
R	A/D CH 15 input
S	Logic ground
T	A/D CH 14 input
U	EXT AD ST L
V	A/D CH 13 input
W	Analog ground
X	A/D CH 12 input
Y	Analog ground
Z	A/D CH 11 input
AA	Analog ground
BB	A/D CH 10 input
CC	Analog ground
DD	A/D CH 7 input
EE	Analog ground
FF	A/D CH 6 input
HH	Analog ground
JJ	A/D CH 5 input
KK	Analog ground
LL	A/D CH 4 input
MM	Analog ground
NN	A/D CH 3 input
PP	-14 V HQ
RR	A/D CH 2 input
SS	+14 V HQ
TT	A/D CH 1 input
UU	+5 V output
VV	A/D CH 0 input

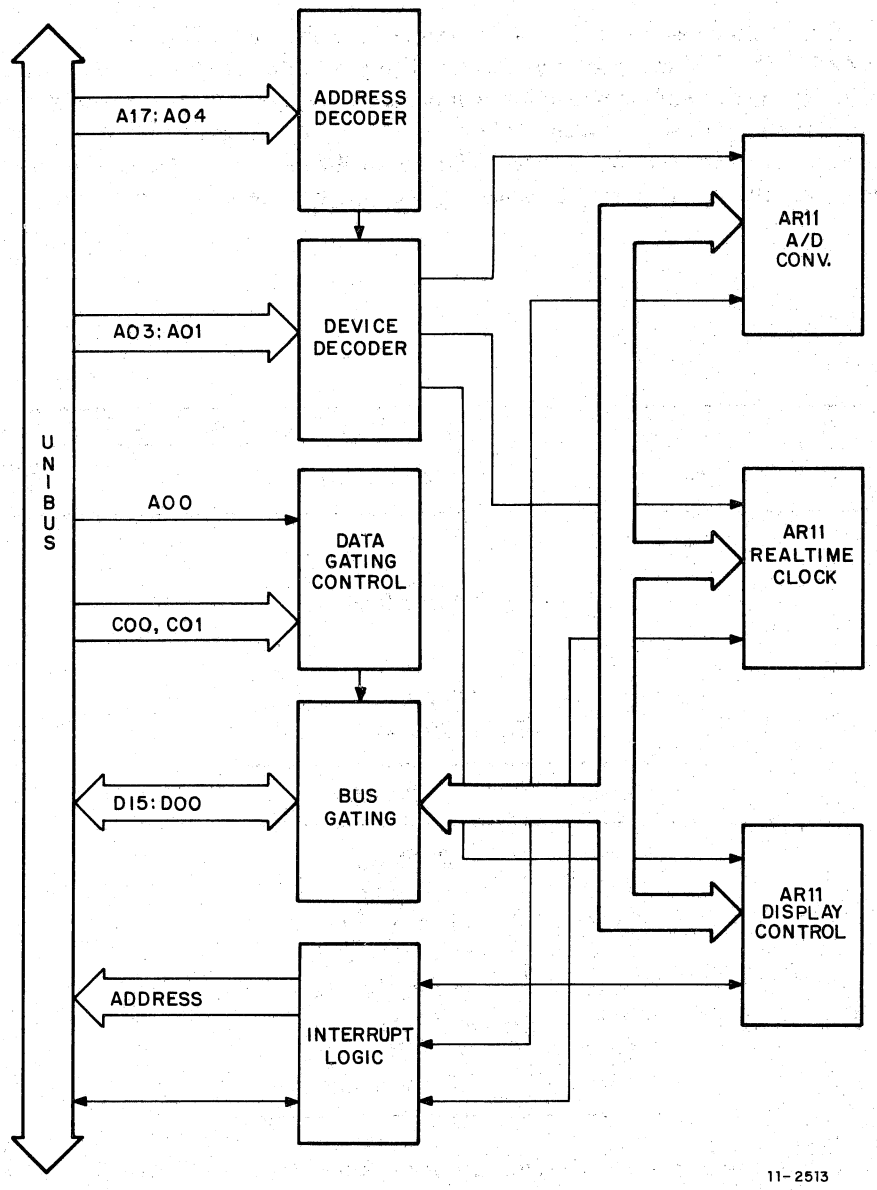


Figure 1-1 AR11 Block Diagram

1.3.3 Addresses

The AR11 registers form a contiguous block of eight addresses in Unibus address space. Eighteen address lines are used to address the AR11. The Address register is shown in Figure 1-2. Bits 11–04 are switch settable (switch pack labeled A) and bit 12 is jumper settable (jumper W2 on module), allowing the user to set the starting address of the block. The starting address may be set between 770000 and 777760 in increments of 20 by means of the switch pack, with W2 connected, and between 760000 and 767760 with W2 disconnected and W2A connected. Addresses of the various registers are shown in Table 1-2, assuming the switches are set for the normal starting address of 770400.

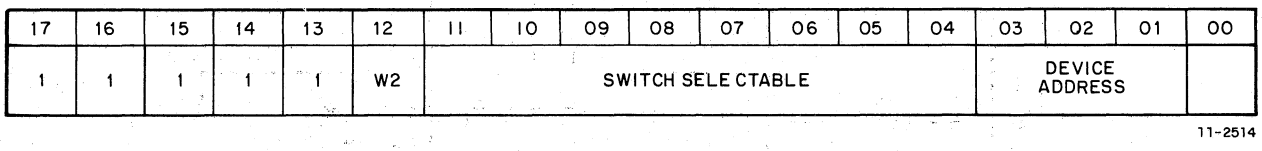


Figure 1-2 Address Register

Table 1-2
AR11 Addresses

Address	Register
770400	A/D Status
770402	A/D Buffer
770404	Clock Status
770406	Clock Buffer/Preset
770410	Display Status
770412	X Buffer
770414	Y Buffer
770416	Clock Counter

The relative location of the various registers always remains the same. The A/D Status, A/D Buffer, Clock Status, and Clock Buffer/Preset registers have exactly the same addresses as the corresponding LPS11 registers. The Display Status, X Buffer, and Y Buffer registers occupy address space corresponding to the LPSDR, not the LPSVC display control. The Clock Counter register may be addressed and read directly in the AR11 but not in the LPS11.

1.3.4 Interrupts

Interrupts may occur at any time from any AR11 device (A/D converter, clock, display control). Upon receipt of the interrupt, the Unibus interface generates a bus request (BR) on the request line of appropriate priority. When control of the bus is granted (BG), the interrupt vector address is sent to the processor via the Unibus, and the processor interrupts to the vectored routine.

The starting address of the interrupt vectors may be set in increments of 20 by means of a switch pack (labeled V) located on the module.

When two interrupts occur simultaneously, it is necessary to arbitrate between them to determine which has higher priority and should be executed first. For this purpose, the Unibus has four levels of priority: 7 (highest), 6, 5, and

4. Within each level, the device that is located closest to the PDP-11 processor has highest priority. The AR11 A/D converter and clock interrupts are both fixed on priority level 6, with the A/D converter closer to the processor (higher priority) than the clock. The display control interrupt is fixed on level 4.

Normal AR11 interrupt vectors and priority levels are shown in Table 1-3.

Table 1-3
AR11 Interrupts

Device	Vector	Priority Level
A/D Converter	340	6
Clock	344	6
Display Control	350	4

The A/D converter and clock vectors are identical to those of the LPSAD-12 and LPSKW. The AR11 display control vector (350) is the same as the LPSDR input vector. The relative location of the three vectors always remains the same.

CHAPTER 2
ANALOG-TO-DIGITAL CONVERTER

2.1 GENERAL DESCRIPTION

The analog-to-digital converter enables the AR11 user to sample analog data at specified rates and to store the equivalent digital value for subsequent processing. The basic subsystem consists of a 16-channel multiplexer (16 single-ended inputs), sample-and-hold circuitry, and a 10-bit A/D converter. The analog inputs can be programmed for unipolar (0–5 V) or bipolar (±2.5 V) operation.

2.2 FUNCTIONAL DESCRIPTION

The A/D converter is a 10-bit successive approximation converter, where the data is right-justified in offset binary. It is controlled by the A/D Status register.

An A/D conversion may be started in three ways: under program control, on overflow of the real-time clock, or on an external input. These methods give the system the flexibility to serve in most applications requiring data acquisition.

The user can choose 1 of 16 single-ended channels of analog input under control of the A/D Status register. In addition, he can program for unipolar or bipolar input.

When a conversion is complete, a flag is set and, if the A/D interrupt is enabled, the processor will interrupt (vector) to the proper subroutine for data manipulation. The user can run in the interrupt mode or wait for the appearance of the A/D Done flag.

The multichannel throughput rate is 30 kHz. A second conversion can be started before the results of the first conversion are read; this overlapping achieves the high throughput. The single-channel throughput rate with clocked or external starts is 35 kHz.

2.3 A/D CONVERTER SPECIFICATIONS

Characteristics	Specifications
Input Voltage Range	0 to +5 V −2.5 to +2.5 V } Program Selectable
Resolution	10 bits (1 part in 1024)
Accuracy at 25° C	0.1% of full scale
Number of Channels	16 (single-ended)
Switching	Break before make

Characteristics	Specifications
Linearity	1/2 LSB (0.05% of full scale)
Differential Linearity	Guaranteed: No skipped states; 95% of states ±1/2 LSB Typical: 99% of states ±1/2 LSB; 85% of states ±1/4 LSB
Throughput Time	
Programmed Start	Multiplexer Sample-and-Hold 8 μs typical Clock Synchronization 0–2 Hold Delay 2 Conversion 20 30–32 μs
Single-Channel External or Clock Start	Clock Synchronization 0–2 μs Hold Delay 2 Conversion 20 Sample-and-Hold reacquisition 4 26–28 μs
Throughput Rate	PDP-11/10 with optimal coding:
Programmed Start	30 kHz
Overflow or External Start	35 kHz
Input Impedance	10M min., $-5\ V \leqslant V_{in} \leqslant +5\ V$
Input Bias Current	100 nA max., unselected channel −2 μA max., selected channel } $-5V \leqslant V_{in} \leqslant +5V$
Sample-and-Hold Tracking	Small signal bandwidth: 700 kHz Large signal slew rate limit: 1 V/μs
Sample-and-Hold Aperture	100 ns max. delay 1 ns jitter
Repeatability	rms noise 1/4 LSB maximum 1/15 LSB typical
Crosstalk	80 dB at 1 kHz, rolling off at 20 dB per decade
Temperature Stability	Gain: 50 ppm/° C max. (20° C/LSB) Linearity: 25 ppm/° C max. (40° C/LSB)
Warmup Time	5 minutes
Control	Controlled by programmed instructions, clock counter overflow, or external input
Output Format	Parallel, 10-bits, right-justified, offset binary, double buffered

2.4 USER INTERFACING

Analog input signals are interfaced through the Berg connector located in the upper right-hand corner of the AR11 module. Pin assignments for connector lines related to the A/D converter are shown in Table 2-1.

Table 2-1
A/D Berg Cable Pin Assignments

Signal	Pin	Signal	Pin
Channel 0 in	VV	Analog Ground	MM
Channel 1 in	TT		
Channel 2 in	RR	Analog Ground	KK
Channel 3 in	NN		
Channel 4 in	LL	Analog Ground	HH
Channel 5 in	JJ		
Channel 6 in	FF	Analog Ground	EE
Channel 7 in	DD		
Channel 10 in	BB	Analog Ground	CC
Channel 11 in	Z		
Channel 12 in	X	Analog Ground	AA
Channel 13 in	V		
Channel 14 in	T	Analog Ground	Y
Channel 15 in	R		
Channel 16 in	N	Analog Ground	W
Channel 17 in	L		
+5 V out	UU	Logic Ground	S
EXT AD ST L	U		

2.4.1 Analog Inputs

2.4.1.1 Connections – Two types of analog signals may be used as AR11 inputs: grounded and floating. A grounded signal is one in which the signal level is referenced to the ground of the instrument which is producing the signal. An example of this is shown in Figure 2-1. Since the instrument may be located some distance from the computer, there may be some voltage difference between the instrument ground and the computer ground. The voltage seen by the AR11 input is the sum of this unwanted ground difference voltage and the desired signal voltage.

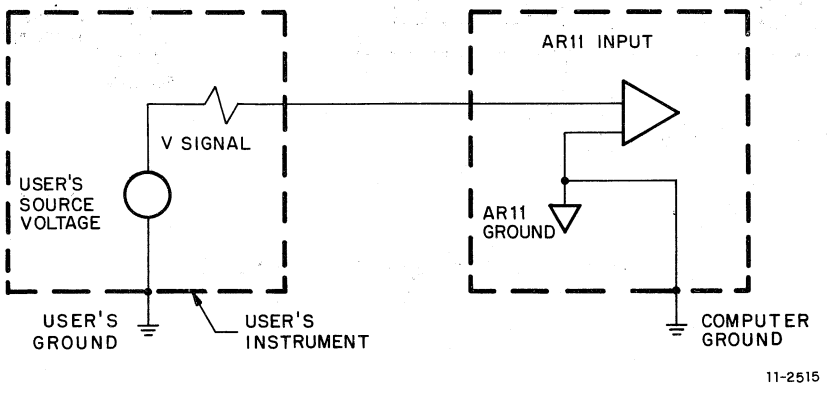


Figure 2-1 AR11 Input Referenced to User's Ground

In cases where the input voltage is referenced to the user's ground, a wire *should not* be run from the user's ground to the AR11 analog ground. Such a wire can cause undesirable ground loop currents which affect results not only on the input channel in question, but also on other channels. The ground difference should be minimized by plugging the instrument into an ac socket as close to the computer as possible.

A floating signal is one in which the signal voltage is measured with respect to a point which is not connected to ground. Examples of this type of analog input are shown in Figure 2-2.

The return of a floating signal must be connected to one of the AR11's analog input grounds (Table 2-1). Although there are only 8 analog input grounds for the 16 analog input channels, these grounds may be shared among channels, as illustrated by the battery-powered sources in Figure 2-2, in which multiple inputs from a single battery-powered instrument share a common return line. Note that the identifying characteristic of a floating source is that connecting the signal return to the AR11 ground does not result in a current path between the AR11 ground and the instrument ground.

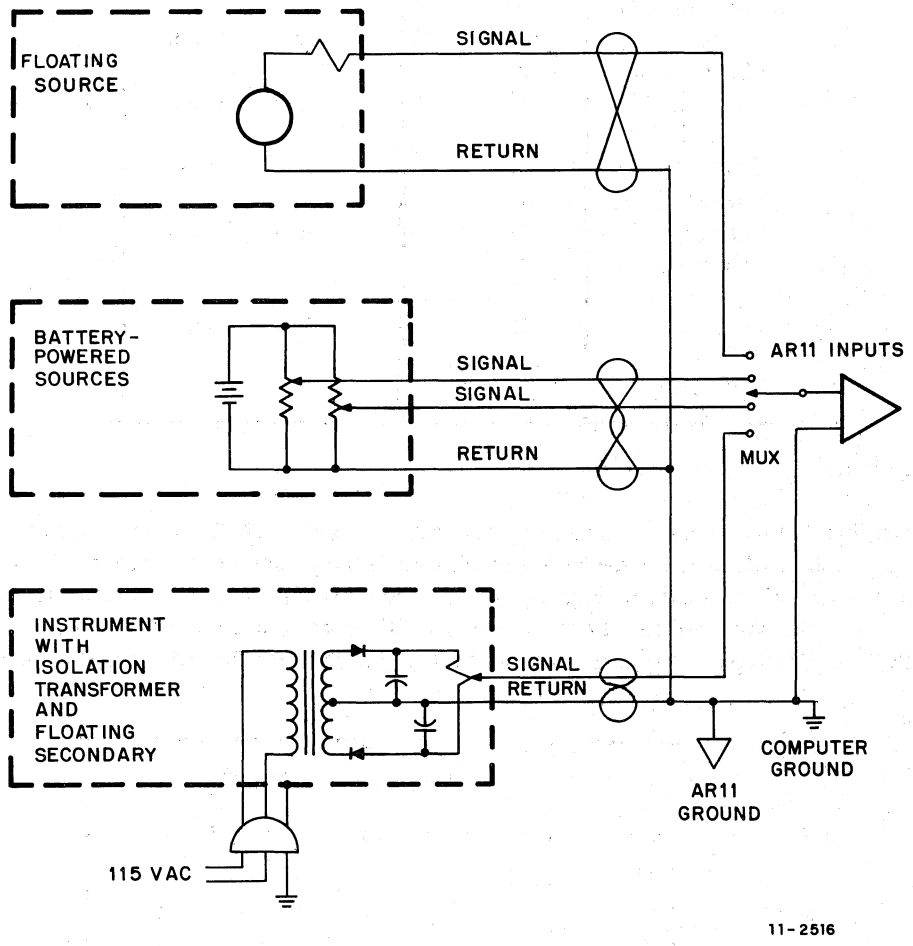


Figure 2-2 Floating AR11 Input Signals

2.4.1.2 Twisting – The effects of magnetic coupling on the input signals may be reduced for floating inputs by twisting the signal and return lines in the input cable. If the inductive pickup voltages of the two leads match, the net effect seen at the AR11 input is zero. Use of twisted pairs has no effect with a single-ended nonfloating signal (referenced to ground at the instrument end).

2.4.1.3 Shielding – The effects of electrostatic coupling on the input signals may be reduced by shielding the signal wires. This is especially important if the instrument or transducer has high source impedance. The shield should be connected to ground at one end of the cable only, so that it does not carry any current.

2.4.1.4 Input Settling with High Source Impedance – All solid state multiplexers have an unavoidable side effect of injecting a small amount of charge into their input lines when changing channels, causing a transient error voltage which is discharged by the input signal's source impedance.

When starting conversions under program control, an 8-μs interval is allowed for the AR11 multiplexer and sample-and-hold circuitry to settle to the correct value of the newly selected channel before the conversion begins. This is normally sufficient time for the input transient to settle out. However, more time may be needed when switching into an input channel with high source impedance. The adequacy of the 8-μs delay may be easily checked by running the AR11 Recovery Test diagnostic, as described in the *AR11 Maintenance Manual.* If this test indicates a settling problem (first conversion on the channel different from subsequent conversions), it will be necessary to either reduce the signal's source impedance or preset the multiplexer channel and provide a software delay before starting the conversion.

2.4.2 +5 Volt Supply

The +5 V supply output, pin UU of the AR11 Berg connector, may be used to power potentiometers whose wipers provide AR11 input signals, as shown in Figure 2-3. Such potentiometers may be repeaters, measuring mechanical shaft positions, or panel-mounted, for use as program parameter inputs.

The AR11 input channel should be run with unipolar range (0 to +5 V) so that full travel of the potentiometer's wiper corresponds to 0000–1777 A/D output (ignoring the effect of the potentiometer's end resistance).

No more than 20 mA of current should be drawn from the +5 V output. Use of 5K potentiometers is recommended, as this value will limit current from the +5 V output to 16 mA, even with potentiometers on all channels, while presenting a maximum signal source impedance of 1.25K to the AR11 input.

Depending on which PDP-11 processor is used, significant ripple (up to 3 percent) may exist on the +5 V output, and appropriate digital filtering or averaging should be considered on potentiometer channels utilizing this reference voltage. If absolute gain accuracy is important for the application, it will be necessary to adjust the processor power supply for exactly +5 V at pin UU.

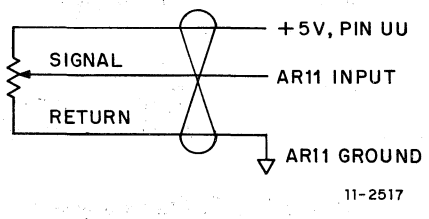


Figure 2-3 Use of +5 V Supply Output

2.4.3 External Starts

The external start signal line, EXT AD ST L (pin U of the Berg connector), is a TTL-compatible input, which sees one TTL unit load. Conversions start on the high-to-low transition of this signal.

In most cases, the source of the external start signal is a grounded (nonfloating) signal generator or logic circuitry located in a grounded instrument. As is the case with the analog input signals, the return path for the external start signal is through the grounds, and a separate return wire *should not* be run. The ground difference between the signal source and the computer should be minimized to prevent spurious start pulses due to ground noise.

In the case of a floating pulse generator only, the pulse generator's logic ground should be connected to the AR11's logic ground, pin S of the Berg connector.

2.4.4 Jumper

The A/D section of the AR11 is equipped with one jumper (W1), which may be connected at the user's option. The AR11 is shipped with a nominal multiplexer sample-and-hold settling delay of 8 μs, which is sufficient to guarantee interchannel settling to within 1/2 LSB when switching between two bipolar channels or two unipolar channels (5 V maximum interchannel voltage difference) with low source resistance. If it is necessary to switch between a unipolar channel and a bipolar channel (7.5 V maximum interchannel voltage difference), the user may choose one of the following techniques:

1. Connect W1, changing the settling delay from 8 μs to 11 μs.

2. Preset the multiplexer channel and provide at least a 3-μs software delay before setting the A/D start bit.

2.5 PROGRAMMING

The AR11 derives its address from the bus control logic, with the first two addresses (defined in Appendix A) being assigned to the A/D converter. The first interrupt vector address in the system is also assigned to the A/D converter. The bus request level for the A/D converter is priority 6.

2.5.1 A/D Status Register

The A/D Status register is illustrated in Figure 2-4 and described in Table 2-2.

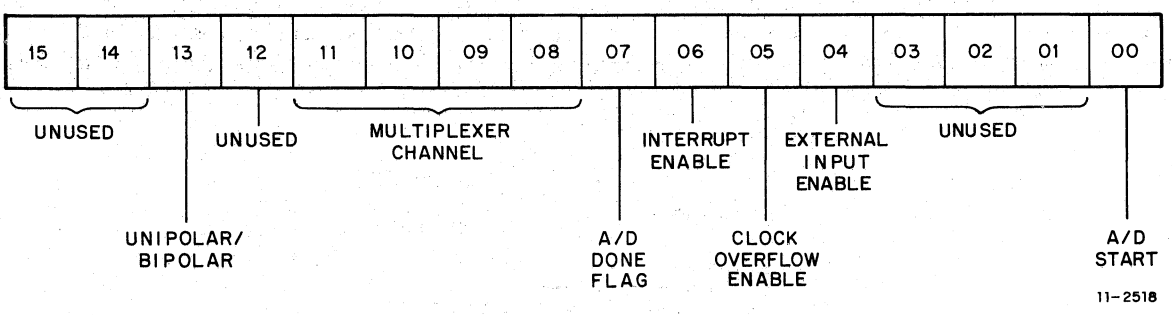


Figure 2-4 A/D Status Register

Table 2-2
A/D Status Register

Bit	Name	Meaning and Operation
15, 14	Unused	
13	Unipolar/Bipolar	Determines the input range of the A/D converter. Bit 13 = 1, Unipolar, 0 to +5 V Bit 13 = 0, Bipolar, -2.5 to +2.5 V Read/write.
12	Unused	
11–8	MUX Channel	Defines which channel of the multiplexer is to be sampled. Read/write.
7	A/D Done Flag	Set upon completion of A/D conversion. Cleared by hardware when an A/D interrupt is complete or when the A/D Buffer register is read. Read only.
6	Interrupt Enable	When a conversion is complete, the A/D Done flag causes an interrupt if this bit is set. Read/write.
5	Clock Overflow Enable	Permits overflow from real-time clock to cause an A/D start. This allows channel sampling at precisely timed intervals independent of software. Data may then be read by testing the A/D Done flag or by enabling the interrupt. Read/write.
4	External Input Enable	Permits a high-to-low transition on the EXT AD ST L line to initiate an A/D conversion. Read/write.
3–1	Unused	
0	A/D Start	When set, the A/D converter starts converting an analog value. At the completion of the conversion, bit 0 is cleared.

2.5.2 A/D Buffer Register

The A/D Buffer register furnishes the 10-bit converted value, formatted in 10-bit, right-justified, offset binary (Figure 2-5), after an A/D conversion is completed.

Input Volts	0–5 V	±2.5 V	10-Bit Result (Octal)
Most positive	4.995 V	2.495 V	001777
Midrange	2.5 V	0	001000
Most negative	0	-2.5 V	000000

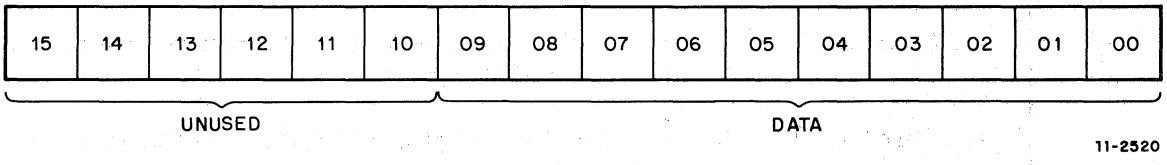


Figure 2-5 A/D Buffer Register (Read Only)

2.5.3 Programming Example

Read 64_{10} (100_8) A/D conversions from channel 0 into locations $4000_8 - 4176_8$ and halt.

```
Location        Instruction             Comment

START:          CLR @ ADSR              ;Clear A/D Status register
                MOV #4000, R0           ;Set up first address
                INC @ ADSR              ;Start A/D conversion on channel 0
                                        ;bipolar

LOOP:           TSTB @ ADSR             ;Check Done flag
                BPL LOOP                ;Wait until flag set
                INC @ ADSR              ;Start next conversion
                MOV @ ADBR, (R0)+       ;Place converted value from A/D
                                        ;Buffer into core location and set up
                                        ;next core location for transfer
                CMP R0, #4200           ;Check if 100₈ conversions have been
                                        ;done
                BNE LOOP                ;No, get next conversion
                HALT                    ;Done

ADSR:           770400                  ;A/D Status register address
ADBR:           770402                  ;A/D Buffer register address
```

CHAPTER 3
PROGRAMMABLE REAL-TIME CLOCK

3.1 GENERAL DESCRIPTION

The real-time clock offers the user several methods for accurately measuring and counting intervals or events. The clock can be used to synchronize the central processor to external events, count external events, or provide interrupts at programmable intervals. It can also be used to directly start the analog-to-digital converter. Many of these operations can be performed concurrently.

The clock operates in two programmable modes: single interval and repeated interval. The user can select from five crystal-controlled frequencies: 1 MHz, 100 kHz, 10 kHz, 1 kHz, or 100 Hz. The clock may also use an external input as a time base. A counter is used to count a preset number of clock ticks before notifying the central processor of an overflow. This allows selection of a complete range of clocking intervals.

3.2 BLOCK DIAGRAM DESCRIPTION

The real-time clock section of the AR11 includes a Clock Status register, a crystal clock and divider chain, a rate control, a Clock Counter register, a Clock Buffer/Preset register, and an interrupt control. Figure 3-1 is a block diagram of the clock.

3.2.1 Clock Status Register

All clock operations are controlled by the Clock Status register. When the Clock Status register enables the Counter, the clock increments an eight-bit Counter at the selected rate (1 MHz to 100 Hz, or external input). The Counter is loaded from the Buffer/Preset register on overflow during repeated-interval mode. If the Buffer/Preset is loaded with a new value while the clock is not running, the Counter is also loaded with the new value.

Overflow of the Clock Counter register causes an interrupt if the interrupt enable bit of the Clock Status register is set. (The vector address of the interrupt is defined in Appendix A.) Flags and interrupts are controlled via the Clock Status register and mode control, and the user can determine by Status register flags whether an interrupt has been caused by an external input or by an overflow. Either method (external input or overflow) may be used to initiate an analog-to-digital conversion.

The Clock Status register also controls how the clock is to function, selecting either single-interval mode or repeated-interval mode.

3.2.1.1 Single-Interval Mode – In this mode, the Clock Counter register counts from a preset value until it overflows (completes its last count, and returns to all 0s). An overflow turns off the Counter, sets the Overflow flag, and, if the interrupt enable bit is set, causes an interrupt. By disabling the interrupt enable and sampling the Overflow flag (bit 7), it is possible to determine when the operation is complete without causing an interrupt; this is useful in timing single experiments. To reinitialize the Counter for a second operation, the Buffer/Preset is loaded with a new value and the enable counter bit of the Clock Status register is set. This mode only operates with crystal-controlled frequencies.

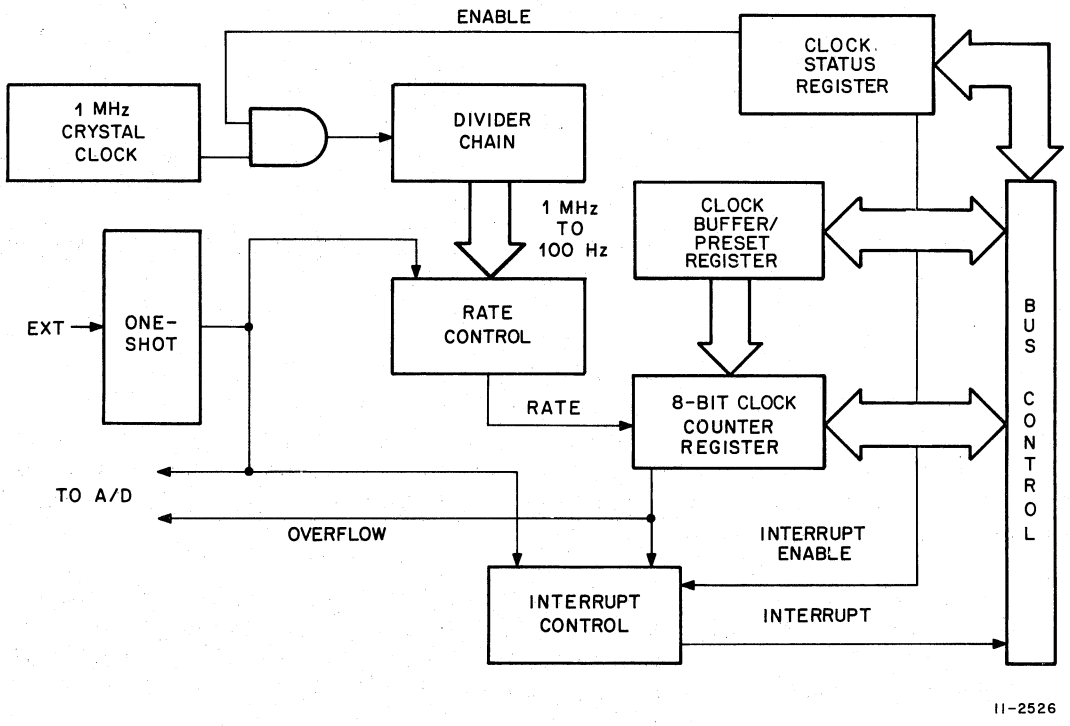


Figure 3-1 Clock Block Diagram

3.2.1.2 **Repeated-Interval Mode** – In this mode, the user need only load the Buffer/Preset and enable the Counter once. After each overflow, the contents of the Buffer/Preset are transferred to the Counter, which continues without losing a single count. If an interrupt occurs, it must be processed before a second interrupt can occur, unless the program permits stacking of interrupts (see *PDP-11 Peripherals and Interfacing Handbook).* This mode permits the user to determine not only the rate of counting, but also the number of counts before overflow, giving him two dimensions in selecting intervals between overflows. The repeated-interval mode can be used to start A/D conversions or experiments and to keep time with a resolution as high as 1 μs.

Using the full eight-bit Clock Counter register allows elapsed time intervals as large as 2.56 seconds or as small as 10 μs. Intervals as small as 1 μs are theoretically possible; however, the program execution time necessary to acknowledge the flags and interrupts exceeds the minimum interval of the clock.

3.2.2 Rate Control and Clock

The rate control provides the time base for the clock. Of the six distinct rates, five are internally generated; the sixth is external to the system. The internal programmable rates are 1 MHz, 100 kHz, 10 kHz, 1 kHz, and 100 Hz crystal-controlled frequencies. The output of an external device can be applied to the external input; the maximum external rate that the device may run at is 1.5 MHz. The same method can be used to count external pulses or peaks, provided that the pulse width is 300 ns or greater. Using the clock as an external counter provides a maximum number of counts of 256 before the counter overflows and program intervention is required.

3.2.3 Clock Buffer/Preset and Clock Counter Registers

The Clock Buffer/Preset register is an eight-bit read/write register which is loaded under program control. The Buffer/Preset must be loaded with the 2's complement of the desired number of counts. The Buffer/Preset should be loaded before the Clock Status register.

The Clock Counter register is an eight-bit read/write register which can be read under program control. The Clock Counter register is loaded by loading the Clock Buffer/Preset register prior to enabling the Counter (via the Clock Status register).

3.2.4 Interrupt Control

Interrupts are caused by an overflow or by the external input. Because the clock has only one interrupt vector, two interrupt enables and two flags are provided. When an interrupt occurs, it is necessary to test these flags to determine the source of the interrupt.

The Overflow flag is set when a Counter overflow occurs. Setting the Overflow flag when the interrupt enable bit is set causes an interrupt.

The external input may also cause interrupts, if an event occurs while the interrupt enable bit is set.

3.2.5 External Input

The functions of the external input include:

External A/D starts
External clock inputs
Causing interrupts
Setting flag (bit 15)

Its use for external clock interrupts is discussed in Paragraph 3.2.4. Setting the clock rate control for external allows the Counter to assume the rate of the external time base. Setting the A/D converter for external start allows remote start of the A/D converter with this signal. The external input EXT AD ST L is available in the AR11 Berg connector, pin U.

3.3 PROGRAMMING

3.3.1 Clock Status Register

The Clock Status register controls all clock operations by defining the manner in which the clock is to be used. It should be loaded after the Clock Buffer/Preset register. All normal program instructions, including byte operations, can be performed on this register. It should be noted that a TST or TSTB instruction does not clear the bit which is being tested.

Maintenance bit 11 of the Clock Status register is a write-only bit which always reads back as 0, as do bits 13, 12, 10, 09, and 05, which are unused (Figure 3-2). Bit 4 always reads back as 1. All of the other bits are read/write bits. Table 3-1 defines the bit assignments for the Clock Status register.

A more detailed discussion of the operations controlled by the Clock Status register is contained in Paragraph 3.2.1.

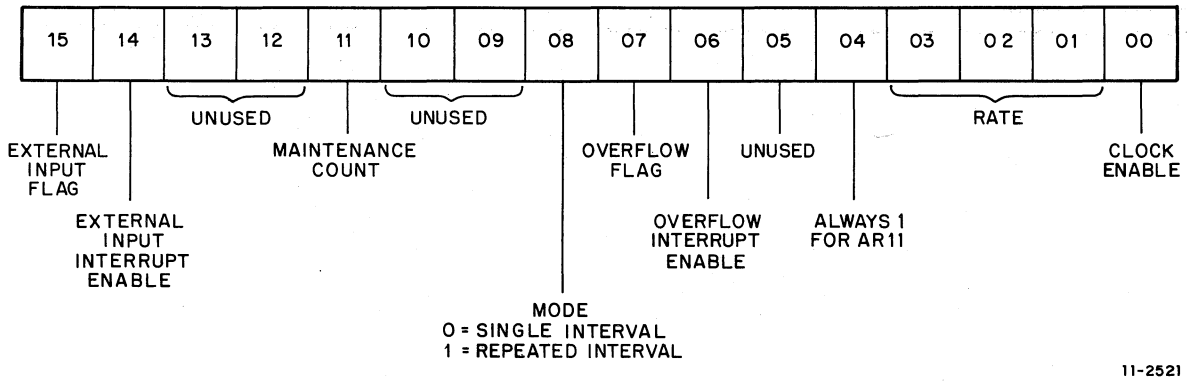


Figure 3-2 Clock Status Register

Table 3-1
Clock Status Register Bit Assignments

Bit	Name	Meaning and Operation
15	External Input Flag	Sets on the high-to-low transition of the external input EXT AD ST L. Read/write.
14	External Input Interrupt Enable	When enabled, setting of the external flag causes an interrupt. Read/write.
13, 12	Unused	
11	Maintenance Count	When loaded with the clock counter enable turned off, this bit simulates a 1-MHz pulse to the counter, providing 1 MHz is selected. By enabling the proper rates, the user can select the base frequency at which the counter operates, e.g., at a rate of 100 kHz, loading this bit 10 times increments the counter by 1. Write only.
10, 9	Unused	
08	Mode	0 Single-Interval Mode – Counter counts from preset value to overflow, sets Overflow flag, and stops. Read/write. 1 Repeated-Interval Mode – Counter counts from preset value to overflow, sets Overflow flag, transfers Buffer/Preset to Counter, and begins again. Read/write.
07	Overflow Flag	Is set by overflow as defined above. Read/write.
06	Overflow Interrupt Enable	When set, the setting of the Overflow flag causes an interrupt. Read/write.
05	Unused	
04	AR11	This bit is always 1 for an AR11 and 0 for an LPS11. Read only.

Table 3-1 (Cont)
Clock Status Register Bit Assignments

Bit	Name	Meaning and Operation
03–01	Rate	Controls the rate of the base frequency. The user may select the following rates: Bits 03 02 01 — Frequency 0 0 0 — No rate selected; stop 0 0 1 — 1 MHz 0 1 0 — 100 kHz 0 1 1 — 10 kHz 1 0 0 — 1 kHz 1 0 1 — 100 Hz 1 1 0 — External input 1 1 1 — No rate selected; stop.* Read/write.
00	Clock Enable	Enables Counter to count at the specified rate. If no rate is specified, clock will not count. It is cleared by overflow in mode 0. When bit 0 is disqualified, loading of the Buffer/Preset also transfers data to Clock Counter. Note that bit 0 has no effect when using the external rate. Read/write.

*This line is wired to pin EL2 on the module and the user may wire to any auxiliary frequency available in TTL form.

3.3.2 Clock Buffer/Preset and Clock Counter Registers

The Clock Buffer/Preset register (Figure 3-3) is an eight-bit register. The Clock Counter register (Figure 3-4) cannot be loaded directly from the processor, but can be read directly. When the enable counter bit of the Clock Status register is 0, loading the Buffer/Preset register also loads the Clock Counter register; when this bit is set, i.e., the clock is running, a transfer to the Buffer/Preset register loads only the Buffer/Preset register. The Buffer/Preset register must be loaded with the 2's complement of the desired number of counts.

3.3.3 Register Addressing, Vector Addressing, and Priority

The clock has three register addresses (Status, Buffer/Preset, and Counter), one vector address, and a fixed priority level of 6. The addresses are defined in Appendix A.

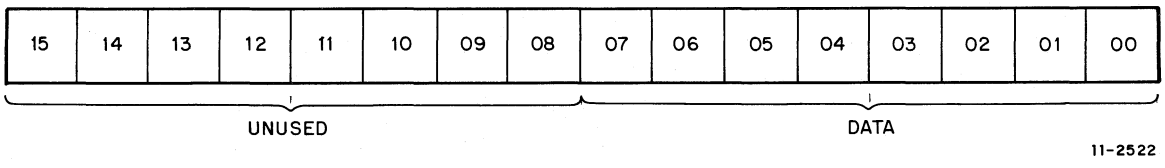


Figure 3-3 Clock Buffer/Preset Register

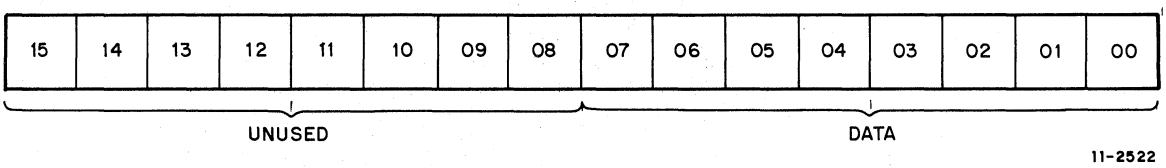


Figure 3-4 Clock Counter Register

3.3.4 Programming Example

This program rings the TTY bell and performs A/D conversions on overflow; overflow occurs every 2 seconds.

Location	Instruction	Comment
INIT:	MOV #70 @ CKBR	; Set to -200_{10}
	MOV #40 @ ADSR	; Enable overflow to start A/D
		; conversion
	MOV #413 @ CKSR	; Start count at 100 Hz with mode 1
LOOP:	TSTB @ CKSR	; Check for Overflow flag
	BPL LOOP	; No, try again
BELL:	TSTB @ TPS	; Test for ready on TTY
	BPL BELL	; No, try again
	MOV #7 @ TPB	; Ring the bell
CONV:	TSTB @ ADSR	; Check for Done flag
	BPL CONV	; No, try again
	JSR PC, READ	; Go to subroutine which reads results
		; of A/D conversion
	BR LOOP	; Do it again
CKBR:	770406	; Buffer/Preset register address
CKSR:	770404	; Clock Status register address
ADSR:	770400	; A/D Status register address
TPS:	777560	; TTY Status register
TPB:	777562	; TTY Buffer register

CHAPTER 4
DISPLAY CONTROL

4.1 GENERAL DESCRIPTION

The display control is an integral part of the AR11 that permits the user to display data in the form of a $1024_{10} \times 1024_{10}$ dot array. Under program control, a bright dot may be produced at any point in this array, and a series of these dots may be programmed sequentially to produce graphical output.

The display control may output to either an X/Y recorder or a CRT display unit. Normal configuration calls for its use with a VR14 display unit. However, it is capable of operating with other equipment, such as the Tektronix 602 and 604 scopes and 603, 611, and 613 storage scopes.

The display control consists of two 10-bit D/A converters, each driven from a 10-bit Buffer register, and circuitry that provides all controls necessary to output the analog signals to an external oscilloscope. D/A output is nominally ±5 V; however, this can be set to ±0.5 V by means of jumpers, and to any range between ±0.5 V and ±5 V by means of resistors. Outputs are capable of driving up to 20 feet of cable at 50 pF of capacitance per foot.

Output operations are accomplished by loading the Display Status register and the X and Y Buffer registers. Through use of Display Status register bits, the user can intensify the contents of the X and Y Buffer registers, provide delays necessary for some scope applications, provide erase, write through, and non-store control functions for storage scope applications, and enable interrupt on completion of scope intensification.

The display control offers four program-controlled modes in which the scope can intensify a point. Jumpers give the display control additional flexibility, allowing the user to select the desired outputs, delay, and intensification pulse polarity, magnitude, and duration.

4.2 BLOCK DIAGRAM DESCRIPTION

Figure 4-1 is a block diagram of the display control, indicating its relationship to the AR11 Unibus control. The principal functional units of the display control are the Display Status register, the intensify control, the X and Y Buffer registers, and the D/A converters.

The Display Status register is a read/write, byte-operable register. It controls all operations of the display control, and permits the user to select or change modes, intensification, and interrupts. The channel 2 bit is principally intended for use with the VR14, but may also be used to provide a "pen up/pen down" capability with an X/Y recorder.

The Display Status register mode control offers the user four distinct modes of operation, making it possible to intensify on command or to intensify upon loading X and Y Buffer registers. Flags and enables let the user interrupt or terminate operations. (This interrupt has a vector address as defined in Appendix A.)

For storage scope applications, the Display Status register can control the write through, erase, and storage modes of operation.

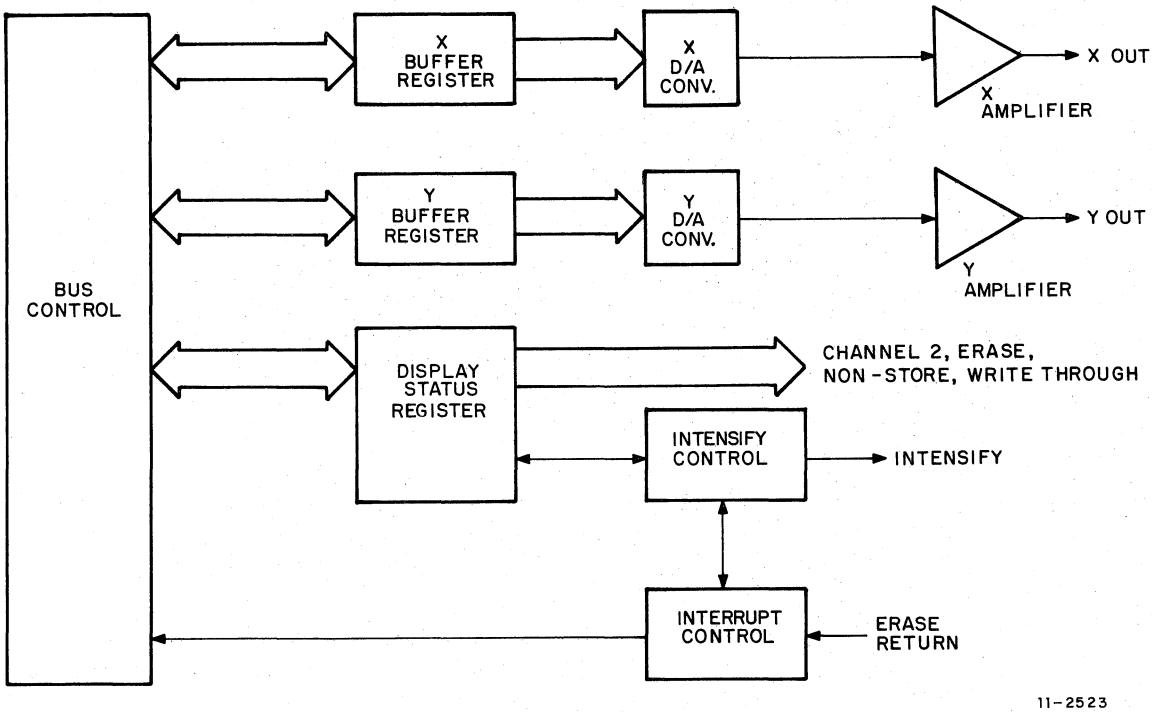


Figure 4-1 Display Control Block Diagram

The intensify control decodes Display Status register information and provides the necessary delayed pulses to the intensification output circuit, which emits an INTENSIFY pulse of proper polarity, magnitude, and duration.

The display control contains X and Y Buffer registers which, when loaded, are converted to analog voltages (jumper selectable gain). The D/A converter outputs are capable of driving 20 feet of cable at 50 pF of capacitance per foot.

4.3 AR11 DISPLAY CONTROL SPECIFICATION

Output Voltage	±5 V, ±0.5 V jumperable
Resolution	1 part in 1024
Accuracy	0.1% at ±5 V; 2% at ±0.5 V
Output Impedance	100 ohms
Output Current Limit	1 mA
Slewing Speed	1/2 V/μs
Settling Time to 0.1%	20 μs
Drive Capability	1000 pF
INTENSIFY Pulse Width	2 μs, 5 μs jumperable
INTENSIFY Pulse Magnitude	3 V, 1.4 V jumperable

INTENSIFY Pulse Polarity	Jumperable
Intensification Delay	20 μs, 80 μs jumperable
Logic Outputs:	
NON-STORE L, WRITE THRU L, ERASE L	TTL open collector
DISP CH02 L	TTL open collector, 1.1K pullup to +5 V
Logic Input (ERASE RET L)	Compatible with Tektronix 603, 611, 613

4.4 USER INTERFACING

4.4.1 Connections

The display control interfaces with the oscilloscope through the Berg connector located in the upper right corner of the AR11 module. Berg cable pin assignments related to the display control are shown in Table 4-1.

Table 4-1
Display Control Berg Cable Pin Assignments

Signal	Pin
WRITE THRU L	A
DISP CH02 L	B
ERASE L	C
INTENSIFY	D
NON-STORE L	E
X OUT	F
ERASE RET L	H
Y OUT	J
ANALOG GROUND (X return)	K
ANALOG GROUND (Y return)	M
LOGIC GROUND	P

As is the case with instruments providing analog input signals to the AR11, the oscilloscope (analog output device) may be either grounded or floating. If the oscilloscope is grounded, either through its power plug or through contact between its chassis and a grounded cabinet, the oscilloscope ground *should not* be connected to any of the AR11 ground pins. Doing so will result in a ground loop which may adversely affect both A/D converter and display control results. If the oscilloscope is floating, its ground should be connected to the AR11 logic ground, pin P of the Berg connector.

Oscilloscope X and Y inputs may be either differential or single ended. Differential inputs should be driven as in Figure 4-2.

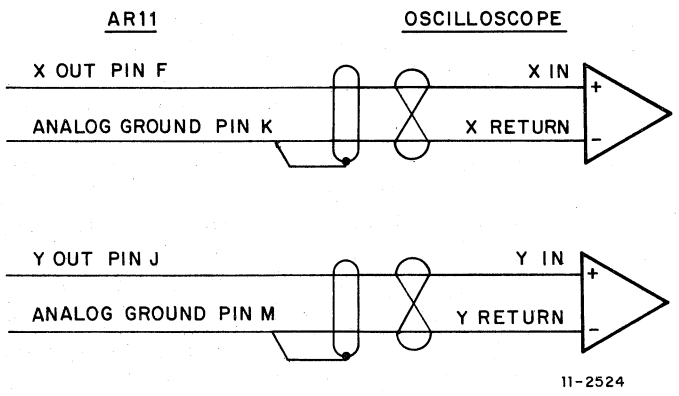


Figure 4-2 Connection to Oscilloscope with Differential Input

In driving oscilloscopes with single-ended inputs, the AR11 analog grounds (pins K and M) are not used. The return path for X and Y signal currents is through ground for a grounded oscilloscope or through logic ground (pin P) for a floating oscilloscope. Since the grounded, single-ended oscilloscope sees an input voltage which is the sum of the AR11 output and the ground difference voltage between the oscilloscope and the AR11, noise and line frequency errors may be minimized by plugging the scope into an ac socket as close as possible to the computer. Running single-ended scopes in a floating configuration will eliminate noise and line frequency errors which are due to ground voltage differences.

4.4.2 Twisting

The effect of magnetic coupling into the scope input lines can be minimized for a differential input scope by running the AR11 output and its return line in a twisted pair. No benefit is derived from a twisted pair with a single-ended scope input.

4.4.3 Shielding

The effect of electrostatic coupling into the scope input lines can be minimized by shielding the input lines from the AR11 to the scope. The shield should be connected to ground at one end only. Grounding the shield at both ends will result in a ground loop which may adversely affect both A/D converter and display control results.

4.4.4 Drive Capability

Careful selection of cabling is essential. The D/A outputs are capable of driving a maximum of 1000 pF (e.g., 20 feet of cable at 50 pF/foot). Output impedance is 100 ohms. Output current limit is 1 mA.

4.4.5 AR11 Setup

4.4.5.1 Gain – The normal range for the AR11 display control outputs is ±5 V. This may be changed to ±0.5 V on the X and Y outputs by jumpering WX and WY respectively. Output ranges between ±0.5 V and ±5 V can be obtained by using resistors in place of jumpers for WX and WY. This is summarized in Table 4-2.

Table 4-2
Gain Jumpers

Gain	Jumpers		Output ($\pm V_{fs}$)
	WX	WY	
1	Out	Out	±5 V
0.1	In	In	±0.5 V
G	R	R	±5 X G V

$G = (R + 888)/(R + 8.88K)$

$R = 888\ [(1-10G)/(G-1)] = 4.44K\ [(2\ V_{fs}-1)/(5 - V_{fs})]$

In many cases, there is a choice between changing the output range of the AR11 and changing the input attenuation of the scope. For example, several Tektronix scopes have standard 1 V (±0.5 V) input ranges which can be readily changed to 10 V (±5 V) by moving the 10:1 attenuation jumpers internal to the scope. This is preferable to changing the ±5 V AR11 output to ±0.5 V using WX and WY, because a higher level signal between the AR11 and scope is less susceptible to noise errors.

4.4.5.2 Intensification Delay – Normal intensification delay is 20 μs. This can be jumpered to 80 μs using W3.

4.4.5.3 Intensification Polarity – Normal polarity is a negative-going pulse. This can be changed to a positive-going pulse by cutting W4 and connecting W4A. Improper polarity will result in erroneous signal blanking and visual retraces.

4.4.5.4 Intensification Magnitude – Normal pulse height is 3 V. This can be changed to 1.4 V by connecting W5.

4.4.5.5 Intensification Duration – Normal duration of the INTENSIFY pulse is 2 μs. This can be changed to 5 μs by connecting W6.

4.4.6 Logic Signals

The AR11 display control has four programmable output logic levels (DISP CH02 L, WRITE THRU L, NON-STORE L, ERASE L), one output pulse (INTENSIFY), and one logic input (ERASE RET L).

4.4.6.1 Electrical Characteristics – WRITE THRU L, NON-STORE L, and ERASE L are open collector contact closures to ground. These lines maintain a maximum output of 0.4 V while sinking 16 mA, and 0.7 V while sinking 40 mA. Maximum allowable output voltage (external pullup voltage) is 15 V. These output lines are compatible with the corresponding inputs of Tektronix 603, 611, and 613 storage scopes.

DISP CH02 L is a TTL-compatible output, consisting of transistor switch to ground and a 1.1K pullup resistor to +5 V. This line maintains a maximum output of 0.4 V while sinking 11 mA, and 0.7 V while sinking 35 mA. It can drive seven TTL unit loads.

The INTENSIFY output pulse is TTL-compatible with jumper W5 disconnected (3 V, as shipped). This line can sink up to 100 mA and source up to 15 mA.

The ERASE RET L input line is specifically designed to interface with the Erase Interval signal of the Tektronix 603 or 611 storage scope or the Busy signal of the Tektronix 613 storage scope. This input can be driven from a standard TTL output.

4.4.6.2 Use of Logic Signals with Scopes – The DISP CH02 L output signal is specifically intended to select channel 2 on the VR14 oscilloscope. This signal is driven by bit 9 of the Display Status register. When bit 9 is set (logical one), DISP CH02 L is low, and channel 2 of the VR14 is selected. Since all Display Status register bits are initialized to 0, the VR14 is initially displaying channel 1, and channel 2 must be specifically programmed.

The WRITE THRU L output signal is intended for use with the Write Thru input of the Tektronix 611 storage scope, Cursor input of the Tektronix 613 storage scope, or similar input of other storage scopes. When bit 11 of the Display Status register is set, WRITE THRU L is low, enabling the write through function of the storage scope. During write through, intensifying a point does not result in the point being stored. The point must be refreshed to be visible on the screen. This function is useful for finding the present beam position or for positioning movable cursors superimposed on a stored display.

The NON-STORE L output signal is intended to control whether or not intensified points are stored. It interfaces with the Non-store input of Tektronix 603, 611, and 613 storage scopes. When bit 10 (Store) of the Display Status register is set, NON-STORE L is high, and intensified points are stored. Since Display Status register bits are initialized to 0, the system is initially in non-store mode.

The ERASE L output signal is intended to interface with the Erase inputs of Tektronix 603, 611, and 613 storage scopes. When bit 12 of the Display Status register is set, ERASE L goes low, signaling the scope to begin an erase operation. The scope acknowledges the ERASE signal by means of an ERASE RET signal (Erase Interval on Tektronix 603 or 611 storage scope or Busy on Tektronix 613 storage scope, connected to ERASE RET L on the AR11). The ERASE RET signal clears bit 12 of the Display Status register, and ERASE L goes high. The ERASE RET signal stays low throughout the erase interval (0.25 second on 603, 0.5 second on 611, 0.9 second on 613). At the completion of the erase operation, the low-to-high transition of ERASE RET L sets the Ready flag, bit 7 of the Display Status register. While ERASE RET L is low (during the erase operation), bit 12 of the Display Status register is held in the zero state, inhibiting further ERASE signals.

4.4.6.3 Other Uses of Logic Signals – The AR11's display control logic outputs can be thought of as general purpose outputs, for uses other than controlling scopes. In this context, the signals can be defined as in Table 4-3, in which the right-hand column refers to bits in the Display Status register.

Table 4-3
Output Signals

AR11 Output Signal	Equivalent Signal Name
ERASE L	BIT 12 L
WRITE THRU L	BIT 11 L
NON-STORE L	$\overline{\text{BIT 10}}$ L
DISP CH02 L	BIT 9 L

Of these signals, BIT 9 L is the most useful for TTL applications, since it has a pullup resistor to +5 V. The other three signals can be made directly TTL-compatible by means of an external pullup resistor to +5 V. If the open collector outputs are used to drive relays or other inductive loads, suitable clamping diodes should be provided to assure that the output voltage does not exceed 15 V on turn-off of the relays, as shown in Figure 4-3.

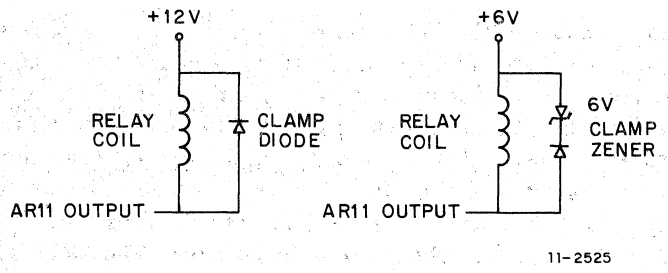


Figure 4-3 Clamping Circuits for Inductive Loads

X/Y Recorder – With an X/Y recorder, one of the logic outputs is used to control a pen up/pen down signal. The X and Y D/A converters provide input to the X and Y channels of the recorder. Typically, recorders have a long mechanical delay between updating of analog inputs and readiness to display the new point (pen down). In general, this can be handled by a software delay (n passes through a loop) or by a real-time clock single-interval delay. Certain X/Y recorders provide an output signal indicating that the pen has settled. If this signal has a low-to-high transition when the pen has settled, it can be connected to the AR11's ERASE RET L input. After the X and Y Buffer registers are loaded, the display control Ready flag should be cleared by setting bit 12 (Erase). When the pen has settled, the low-to-high transition on ERASE RET L resets the Ready flag, causing an interrupt. The interrupt service routine then lowers the pen to plot the point.

Strip Chart Recorder – With a strip chart recorder, the two D/A converters provide analog input to two recorder channels. In some strip chart recorders, the motion of the paper (time axis) is controlled by a logic level which turns on a motor. In other recorders, the motion is controlled by logic pulses to a stepper motor, so that speed is a programmable function of pulse frequency. In either case, a single AR11 logic output can be used to control the paper motion.

4.4.7 Specific Scopes

This section contains information on using the AR11 to drive the VR14 and Tektronix 602, 603, 604, 611, and 613 scopes. The manufacturer's manual for the scope being used should be checked to obtain more detailed information. Scopes other than those discussed in this section should be interfaced by reference to Paragraph 4.4.5 (AR11 Setup) and the scope's manual. Some scopes may call for positive-only input voltage swings, with no means of adjustment for −, 0, or + swings. In this case, it is necessary to utilize only nine of the AR11's ten D/A bits, setting the MSB to one for positive excursions only. This provides nine-bit resolution, which is ample for most small screen display applications. The AR11 has a settling delay of 20 μs or 80 μs, jumper selectable. For scopes other than VR14, 602, 603, 604, 611, and 613, the user must determine whether one of these delays is adequate. If greater settling time than 80 μs is required, a software delay will be necessary.

4.4.7.1 VR14 – The VR14 scope has differential analog inputs with ranges which can be internally adjusted for ±5 V. Proper intensification delay is 20 μs. The intensification pulse is 3 V negative going, with 2-μs duration. The AR11 is compatible with the VR14 as shipped, with no jumper changes required.

4.4.7.2 Tektronix 602 – The Tektronix 602 has single-ended inputs with a nominal range of 0 to 1 V. This should be changed to ±0.5 V by means of the position controls located on the front panel of the 602. The 602's screen is 8 cm (vertical) by 10 cm (horizontal). The user may choose to adjust the 602's vertical gain for ±0.4 V full scale or ±0.5 V full scale. At ±0.4 V full scale, the AR11 presentation is capable of overflowing the screen at top and bottom. At ±0.5 V full scale, the AR11 full scale range does not overflow the screen, but a programmed square (n by n points) appears rectangular. If the 602 is left with ±0.5-V inputs, WX and WY should be connected on the AR11. As an alternative (which is preferable in noisy environments or if the scope is located away from the computer), the 602 inputs should be set for 10:1 attenuation per the instructions in the Tektronix 602 manual. With the 10:1 attenuators installed in the 602, WX and WY are not connected on the AR11, and full ±5 V signals are used. The 20-μs intensification delay and 2-μs intensification duration are sufficient for the 602, so that W3 and W6 are not connected on the AR11. Since the 602 requires a positive-going 1 V intensification pulse, W4 should be cut and W4A and W5 should be connected.

4.4.7.3 Tektronix 603 Storage Scope – The Tektronix 603 X and Y input amplifiers can be used as differential inputs when connected through rear panel BNCs, or as single-ended inputs when connected through the rear panel remote program connector. The differential input configuration gives superior performance in a noisy environment or at a distance from the computer; however, cabling into the BNCs may be somewhat difficult. The internal attenuators should be set to X5 per instructions in the 603 manual. Horizontal gain should be set for 10 V full scale and vertical gain should be set for either 8 V or 10 V full scale, depending on whether a square, overflowing or rectangular, nonoverflowing display is desired. The position controls should be set for zero corresponding to midscreen, so that ±5 V (or ±4 V vertical) results in full-scale deflection. The AR11 is left at ±5 V output (WX and WY not connected). An intensification delay of 20 μs is adequate with the 603, so that W3 need not be connected. W6 should be connected to provide a sufficient dot writing time with the standard 603 CRT. W6 need not be connected if the 603 contains an option 2 CRT. Since the 603 requires a positive-going intensification pulse, W4 should be cut and W4A should be connected. The 603's intensification sensitivity is adjustable between 1 and 5 V. It must be set below 3 V, and W5 should remain disconnected, so that the AR11 intensify output is 3 V. ERASE and NON-STORE should be connected directly. The 603's Erase Interval signal should be connected to the AR11's ERASE RET L. The 603 storage scope has no write through function.

4.4.7.4 Tektronix 604 – The Tektronix 604 is identical to the 603 except that it is not a storage scope. The 604 should be interfaced to the AR11 exactly as in Paragraph 4.4.7.3 except for the following: W6 is not connected (extra dot writing time not needed), and the ERASE, NON-STORE, and ERASE RET signals are not connected.

4.4.7.5 Tektronix 611 Storage Scope – The Tektronix 611 storage scope has single-ended inputs with 1 V range. This should be changed to a 10 V range by means of internal X10 attenuators, per instructions in the 611 manual. The X and Y positioning switches should be in the center position. This sets up the inputs for ±5 V, directly compatible with the AR11 analog outputs (WX and WY not connected). Intensification delay should be set for 80 μs (W3 connected). Intensification duration should be set for 5 μs (W6 connected). The 611 requires a positive-going intensification pulse (W4 disconnected, W4A connected). Since the 611's intensification threshold is nominally 1 V, the AR11s intensification pulse should be left at 3 V (leave W5 disconnected). The 611's ERASE, NON-STORE, and WRITE THRU lines should be connected directly to the corresponding AR11 outputs. The 611's Erase Interval signal should be connected to the AR11's ERASE RET L. The 611 contains a 500-ms timing circuit which controls its erase interval duration. This circuit requires another 500 ms of recovery time after the conclusion of the erase interval. If the user attempts to program another erase operation within 300 ms of the end of the previous erase operation, the timing circuit does not recognize the erase command. Under these conditions, ERASE RET L does not go low (the 611 fails to acknowledge the erase command), so that the display control Ready flag does not get set, and it is possible for the program to hang up in a wait loop. If the user attempts to program another erase operation more than 300 ms, but less than 500 ms after the previous erase operation, the erase command is recognized but the erase interval duration is less than 500 ms, so that there may not be complete erasure.

4.4.7.6 Tektronix 613 Storage Scope – The Tektronix 613 storage scope has differential inputs with 1 V range (and no easily settable X10 attenuator). Consequently, the AR11 must be run with ±0.5 V outputs (WX and WY connected). The 613's horizontal and vertical "origin location" jumpers should each be in location 2 to set up the inputs for ±0.5 V. Intensification delay should be set for 80 μs (W3 connected); intensification duration should be set for 5 μs (W6 connected). The 613 requires a positive-going intensification pulse (W4 disconnected, W4A connected). Since the 613's intensification threshold is nominally 1 V, the AR11's intensification pulse should be left at 3 V (leave W5 disconnected). The 613's ERASE, NON-STORE, and WRITE THRU lines should be connected directly to the corresponding AR11 outputs. The 613's BUSY signal should be connected to the AR11's ERASE RET L. The 613's Hard Copy Busy and Deflection Busy jumpers should be in their normal (inactive) position when used with the AR11 to avoid setting the AR11's display control Ready flag at times other than the end of an intensification pulse or the end of an erase operation. The 613's erase interval timer does not have a recovery delay, so that no restriction is necessary on the interval between back-to-back erase operations.

4.5 PROGRAMMING

Programming is accomplished through the Display Status register and the X and Y Buffer registers. One hardware interrupt vector is associated with the display control, as defined in Appendix A.

4.5.1 Display Status Register

The Display Status register is a read/write register, and is byte operable. It is shown in Figure 4-4 and described in Table 4-4.

Table 4-4
Display Status Register

Bit	Name	Meaning and Operation
15–13	Unused	Always read 0.
12	Erase	Bit 12 = 1; erase data in the storage scope. Read/write.
11	Write Thru	Bit 11 = 1; an intensified point will not be stored even though the user is in the store operation. Read/write.
10	Store	Bit 10 = 1; all intensified points will be stored, providing bit 11 = 0. Read/write.
09	Channel 2	Bit 9 = 0, channel 1; bit 9 = 1, channel 2 (VR14 operation). Read/write.
08	Unused	
07	Ready flag	Bit 7 = 0; the scope is not ready, do not load or intensify points. Bit 7 = 1; the scope is ready. Read only.
06	Interrupt Enable	Bit 6 = 1 and bit 7 in transition from a 0 to a 1 will cause an interrupt. Read/write.
05, 04	Unused	
03, 02	Mode	Read/write. 00 Normal – Intensification with bit 0 only. 01 X Mode – Intensification on loading X Buffer register. Loading bit 0 not required. 10 Y Mode – Intensification on loading Y Buffer register. Loading bit 0 not required. 11 XY Mode – Intensification on loading X or Y Buffer register. Loading bit 0 not required.
01	Unused	
00	Intensify	Bit 0 = 1; any coordinate in X and Y Buffer registers will be intensified after 20 μs or 80 μs internal delay. Write only.

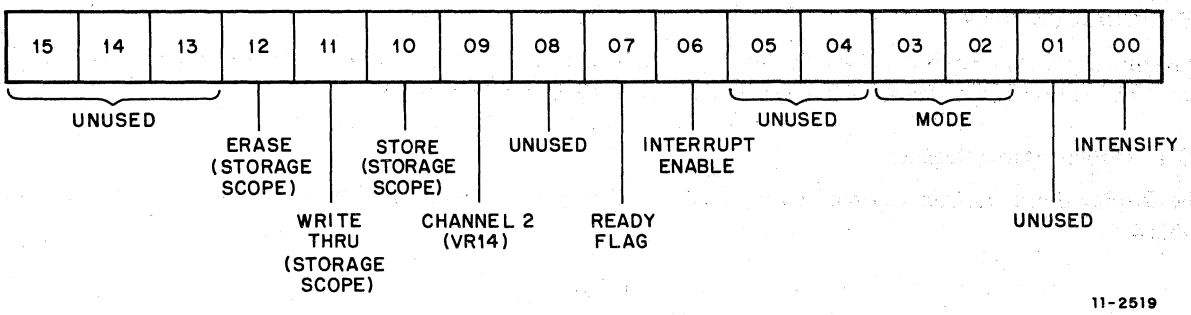


Figure 4-4 Display Status Register

Interrupts occur when bit 6 (interrupt enable) is set and bit 7 (Ready flag) sets. Bit 7 sets when an INTENSIFY pulse occurs or when an erase operation is complete. The Ready flag notifies the user that all delays and operations are complete.

A point may be intensified in any of four control modes, selected by bits 2 and 3. In mode 0, a point is intensified by setting bit 0. Mode 1 intensifies a point upon loading the X Buffer register; mode 2 intensifies a point upon loading the Y Buffer register; mode 3 intensifies upon loading either the X or Y Buffer register.

4.5.2 X and Y Buffer Registers

The X and Y Buffer registers are read/write registers, but are not byte operable. Data format of these registers is shown in Figure 4-5.

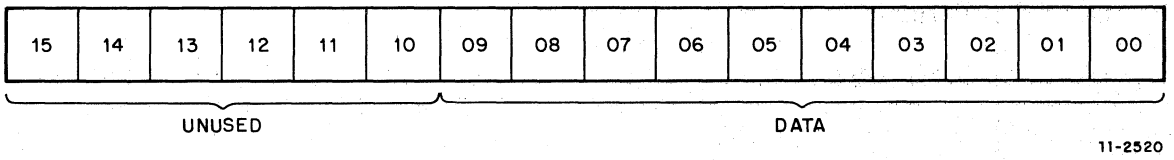


Figure 4-5 X and Y Buffer Registers

When the display control is used with a scope grid, the coordinate scheme shown in Figure 4-6 is used. The display takes the form of a $1024_{10} \times 1024_{10}$ dot array. Under program control, a bright spot is momentarily produced at any point in this array.

4.5.3 Programming Example

This program displays a diagonal line from the lower left corner of the scope screen to the upper right corner.

Location	Instruction	Comment
GO:	MOV #4, @ VCSR	; Mode 1, no interrupt
	INC @ Y REG	; Load Y Buffer register
	INC @ X REG	; Load X Buffer register and intensify
LOOP:	TSTB @ VCSR	; Check if done
	BPL LOOP	; No, try again
	BR GO	; Load the next coordinate
VCSR:	770410	; Display Status register address
YREG:	770414	; Y Buffer address
XREG:	770412	; X Buffer address

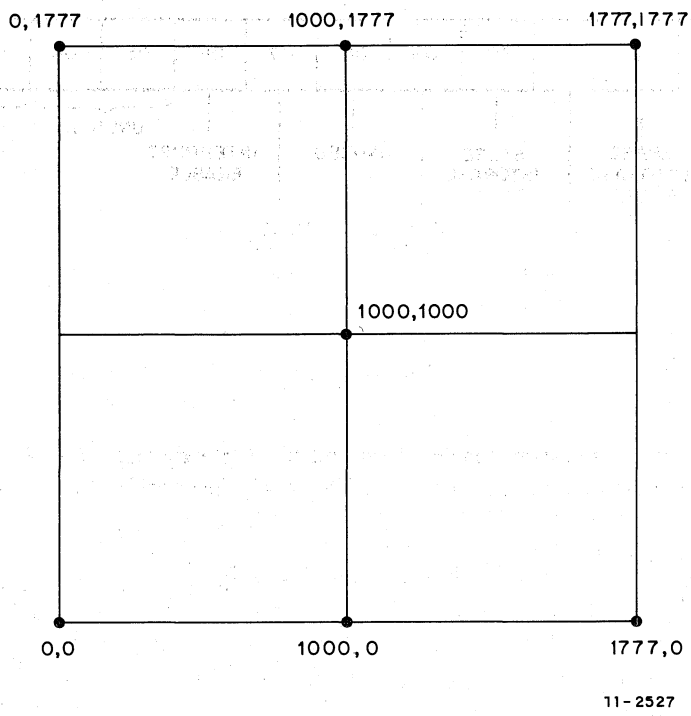


Figure 4-6 Scope Grid Coordinates X, Y

APPENDIX A
PROGRAMMER'S REFERENCE

Standard* Register Addresses

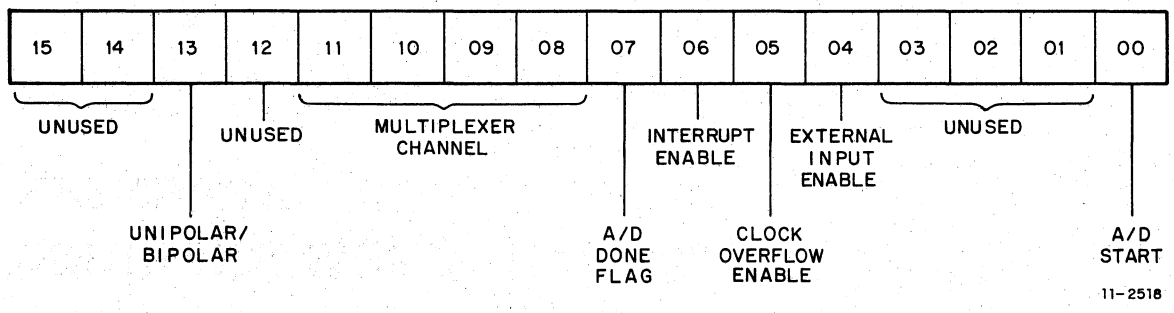
Register	Address
A/D Status	770400
A/D Buffer	770402
Clock Status	770404
Clock Buffer/Preset	770406
Display Status	770410
X Buffer	770412
Y Buffer	770414
Clock Counter	770416

*The register address is jumper selectable in increments of 20 locations; however, the relative location of the various registers remains the same.

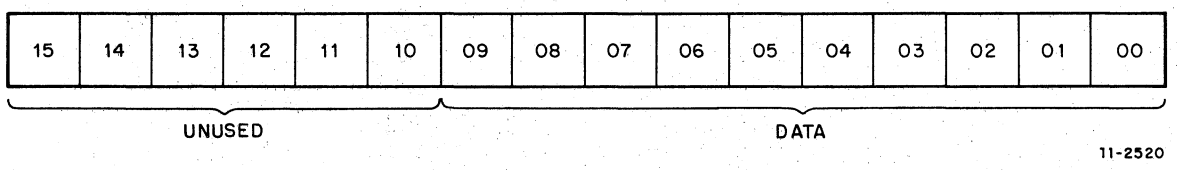
Vector Address

Option	Address*	BR Level
A/D Converter	340	6
Clock	344	6
Display	350	4

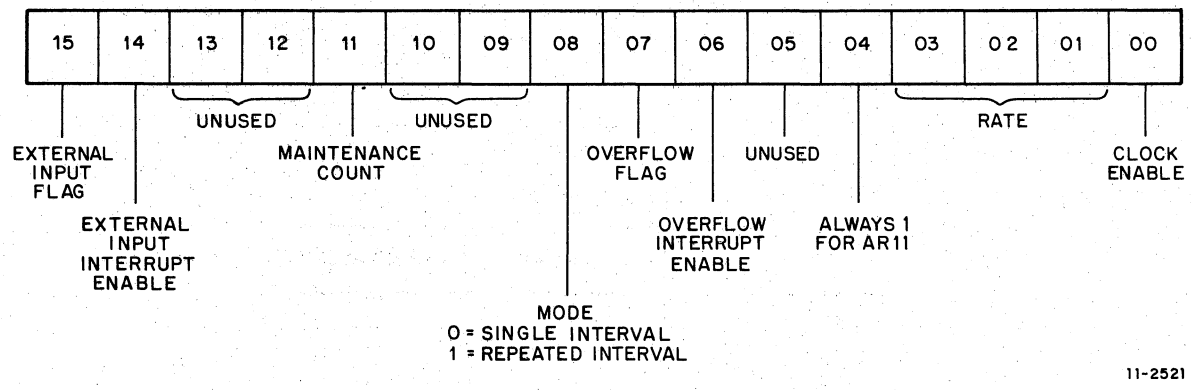
*These addresses are jumper selectable in increments of 20_8.



A/D Status Register



A/D Buffer Register

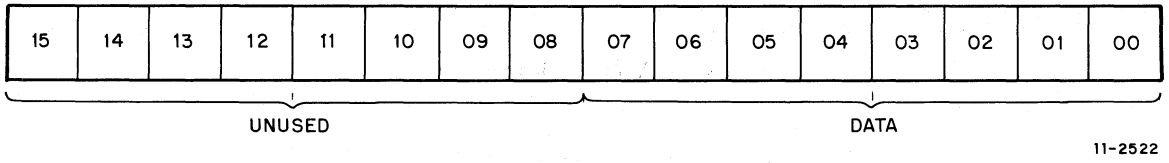


Clock Status Register

Clock Status Register Rate Bits

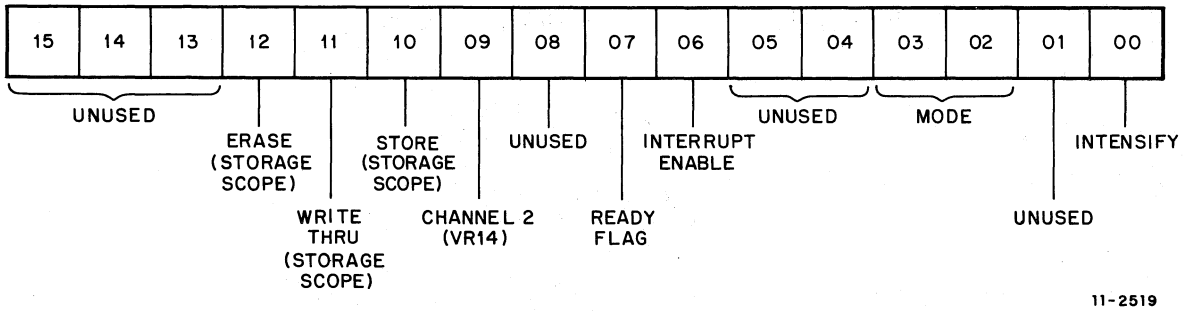
Bit 3	Bit 2	Bit 1	Base Frequency
0	0	0	Stop
0	0	1	1 MHz
0	1	0	100 kHz
0	1	1	10 kHz
1	0	0	1 kHz
1	0	1	100 Hz
1	1	0	External Input
1	1	1	Stop*

*Frequency defined by pin EL2 of module.



Clock Buffer/Preset Register

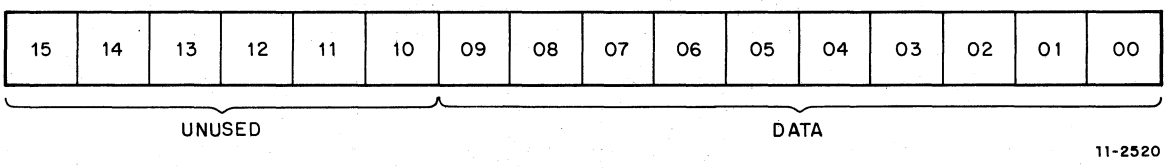
Data is simultaneously loaded into the Clock Counter when bit 0 of the Status register is zero.



Display Control Status Register

Display Control Status Register Mode Bits

Bit 3	Bit 2	Function
0	0	Intensification with bit 0 only.
0	1	Intensification on loading X register.
1	0	Intensification on loading Y register.
1	1	Intensification on X or Y.



X and Y Buffer Register

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