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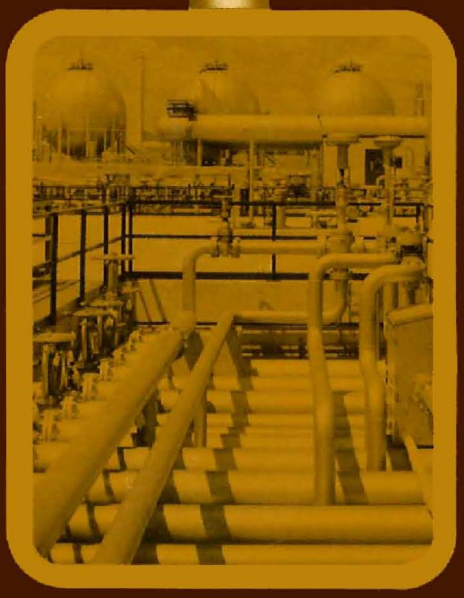
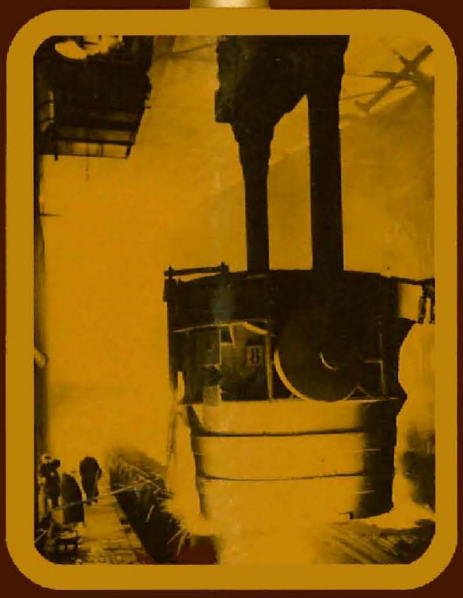
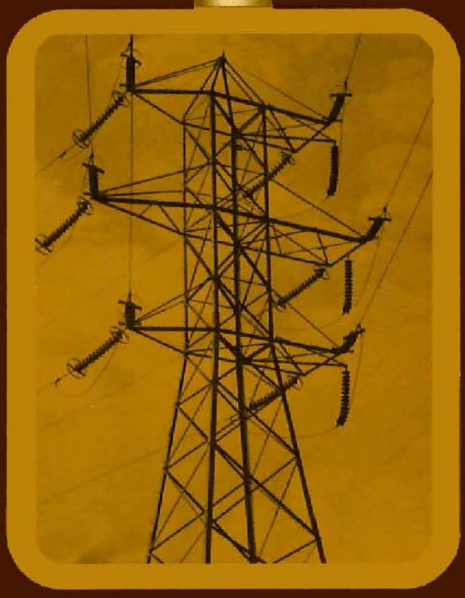
UDC11 universal digital control subsystem maintenance manual







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CHAPTER 1
GENERAL INFORMATION

1.1 GENERAL

The UDC11 Universal Digital Controller I/O Subsystem, manufactured by Digital Equipment Corporation, is a peripheral device to be used with the PDP-11 computer systems in industrial data acquisition and control applications. (Refer to the *PDP-11 Interface Manual* for information on the computers and I/O bus structures.)

1.2 PURPOSE

The UDC11 operates under computer program control as a highly flexible digital input/output device capable of interrogating digital inputs and driving analog and digital outputs connected to functional modules. Up to 252 digital sense and control functional modules, each handling up to 16 individual digital points, can be directly accessed by the UDC11. I/O functions that can be handled by the existing complement of modules include: driver output, relay output, contact sense, contact interrupt, D/A converters, and I/O counters. This complement of functional modules provides the means for controlling and monitoring most devices found in an industrial and process control environment. Selection and inclusion of appropriate functional input and output modules in the UDC11 tailors the subsystem to a specific application.

1.3 FUNCTIONAL DESCRIPTION

The UDC11 consists of one master file, up to 62 file units (DD02), and up to 252 functional modules (Figure 1-1). The interface controller (DD01-D) of the master file coordinates all activities within the UDC11 in response to programmed I/O instructions, address, and data from the computer. Each I/O file unit is set up to respond to a unique 2-digit octal address (6 binary bits), and each module slot in this unit responds to a unqiue 2-bit binary address.

Thus, each module can be accessed directly, using an 8-bit address. Once accessed, data (DATAO) can be loaded into the module for output control, or data (DATAI) can be read into the computer from a module to be sensed. In addition to the direct access feature, the UDC11 contains an interrupt structure, which may be enabled or disabled under program control, and an automatic scan feature to determine the address of an interrupting module. Only those functional modules that require fast program intervention are equipped with and connect to the interrupt structure. A third feature of the UDC11 is a hardware/software scheme for determining when an input contact has changed state, and the direction of that change. Both the interrupt structure and the hardware/software scheme significantly reduce computer processing overhead.

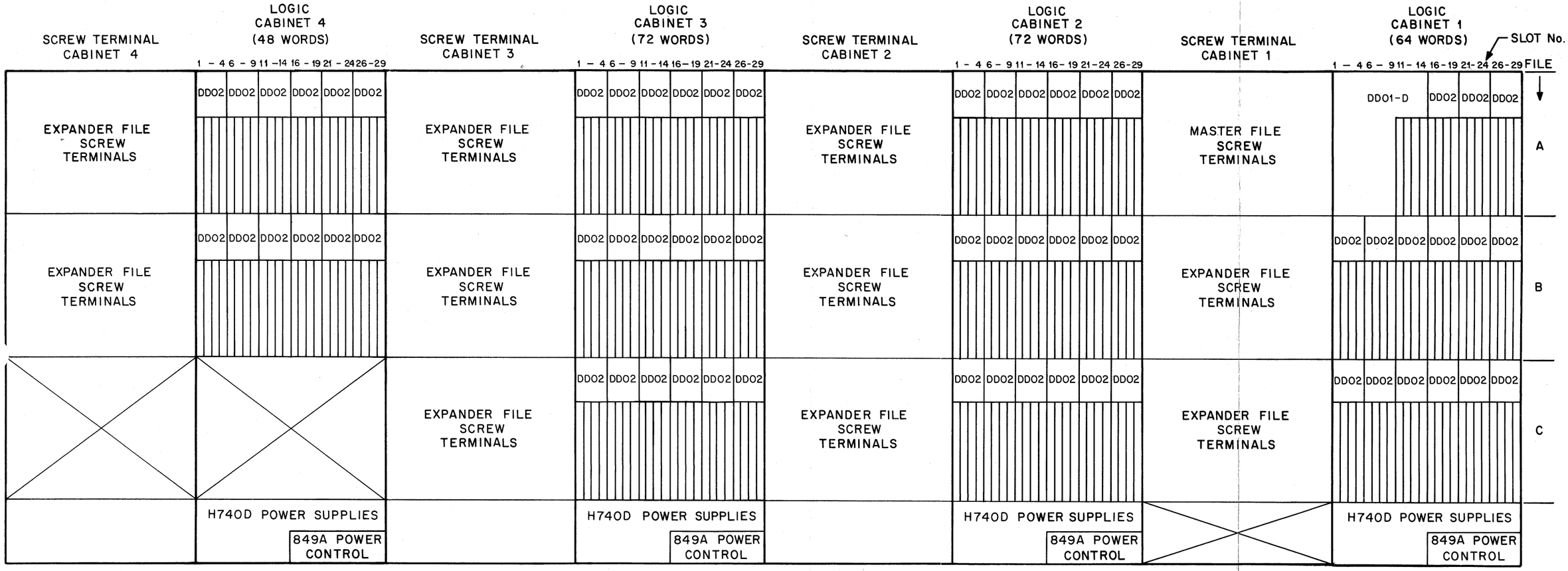

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Figure 1-1 UDC11 Overall Block Diagram

1.4 PHYSICAL DESCRIPTION

1.4.1 System Organization

The UDC11 system is completely modular for ease of system configuration and expansion (Table 1-1). For applications requiring 16 digital words (256 digital points) or less, the system is available in a single-cabinet configuration. Systems requiring greater than 16 digital words but less than 64 digital words are housed in a dual-cabinet configuration – one cabinet to mount the electronics, and one for the screw terminal connectors. Four dual-cabinet configurations are required to implement a maximum system of 252 digital words (4032 digital points).

The system's electronics cabinets are organized in files. The first file in the system is a master file that contains the computer interface, system timing and control, address/scan register, and address decoding hardware for selection of up to four digital words. The master file may also contain three additional file units, each providing address decoding for up to four digital words. The hardware for each 4-word group is implemented by adding up to four functional I/O signal-conditioning modules and the required screw terminal cable assemblies – one for each module. Fully implemented, the master file contains 16 digital words.

Expansion beyond 16 words is accomplished by addition of expander files. Each expander file contains provision for a total of 24 words (384 digital points) in 6 file units.

Industrial packaging and modular design permit the UDC11 to be configured and modified according to application needs. Screw terminals provide a convenient means for connecting customer field wiring to the UDC functional modules. The screw terminals may be housed in the logic cabinet or in a separate cabinet located adjacent to the logic cabinet. Figure 1-2 illustrates the maximum configuration, including the screw terminal cabinets, and locates the major units and functional modules of the UDC11. The major units and modules are described in the following paragraphs.

1.4.2 Logic and Screw Terminal Cabinet (H964AA/AB)

The H964AA/AB Cabinet is a 19 in. industrial-type cabinet that contains the H849A Power Control, H740D Power Supply, two top-mounted forced-air-cooling fans, air filters, and full front and rear doors. The cabinet will house one UDC11 file and, with H964MA mounting hardware, the necessary screw terminals for connection of field wiring. The UDC11 file is mounted at the top, the screw terminals just underneath, and the power elements at the bottom. Cabinet cooling is accomplished by blowing air down from the top of the cabinet and using the hole in the bottom of the cabinet for exhaust. Bottom entry of field wiring is standard. See Figure 4-1 for cabinet dimensions.

1.4.3 Logic and Screw Terminal Cabinets (H964CA, CB, CC, CD)

The H964CA, CB, CC, and CD Cabinets consist of a pair of 19 in. industrial-type cabinets secured to each other. The right-hand side cabinet (as viewed from the wirewrap side) houses the UDC logic, while the left-hand side cabinet contains the necessary screw terminals. The logic cabinet is capable of housing up to three UDC11 files. In addition to the UDC11 files, the logic cabinet contains the 849 Primary Power Control, one H740D Power Supply for each file implemented, two top-mounted forced-air-cooling fans, air filters, and full front and rear doors. The screw terminals are secured to the cabinet with H964MA mounting hardware. Bottom entry of field wiring is standard, although top, rear entry is available as an option.

1.4.3.1 849A Power Control Panel – The power control panel located in the front of the logic cabinet controls the application and removal of system primary power. The power control contains a LOCAL/REMOTE switch, a power ON indicator, a primary power contactor, and a circuit breaker. When the LOCAL/REMOTE switch is placed in REMOTE, application and removal of primary power can be controlled from the computer. For the LOCAL position, primary power is controlled by using the front panel 30A circuit breaker.

Table 1-1
System Organization

Item	Description	Model	Prerequisite
System Cabinets	Single cabinet for UDC system up to 16 digital words (256 digital points). Contains logic power supply, cooling fans and filters. Screw terminals that mount in the same cabinet require separate mechanical assembly (Model H964MA).	H964A □ (bottom entry only of field cables.) A—115V power supply B—230V power supply	 — —
	Mechanical assembly for mounting screw terminals in single cabinets.	H964MA	H964AA or H964AB
	EXAMPLE: Model H964AA designates a single cabinet (bottom entry only of field cables, with 115V power supply).		
	Dual cabinet for UDC11 system. One cabinet houses system electronics and logic (contains logic power supplies, cooling fans, and filters). Second cabinet for termination of input field wiring on screw terminals.	H964C □ A—top or bottom entry of field cables. 115V power supply B—bottom entry only of field cables. 115V power supply C—top or bottom entry of field cables. 230V power supply D—bottom entry only of field cables. 230V power supply	 — — — —
Master File	Basic UDC11 system file DD01-D contains interface and control, address/scan register, and provision for installing four functional I/O modules (64 digital points) and an I/O cable. Master file may be expanded to 16 digital words (256 digital points) by adding three DD02 File Units and appropriate number of functional I/O and signal-conditioning modules.	UDC11	H964A or H964C PDP-11/20 H964A or H964C PDP-11/20

(continued on next page)

Table 1-1 (Cont)
System Organization

Item	Description	Model	Prerequisite
Expander File	Provides expansion capability. Expander file contains mounting hardware, file I/O cable, and provision for installing four digital words and up to five DD02 File Units, each capable of containing four digital words. (Fully implemented expander file contains 24 functional I/O modules – 24 digital words or 384 digital points.)	UDC8-X □ A—second or third file in electronics cabinets. B—first file in each additional electronics cabinet.	UDC11 Master File (DD01-D) plus H964C Dual Cabinet Second H964C Dual Cabinet
File Units	Provides address decoding, control logic, and capacity for mounting up to four functional I/O and signal-conditioning modules (4 digital words or 64 digital points).		UDC11 Master File, Expander Files
Functional I/O Modules	Contact Sense (relay) Contact Interrupt (relay) Contact Sense (solid state) Contact Interrupt (solid state) Single-shot Driver Single-shot Relay Flip-flop Driver Flip-flop Relay Latching Relay DAC I/O Counter	W731 W733 W741 W743 M687 M807 M685 M805 M803 A633 W734	Master File, Expander Files, DD02 File Units
Signal-Conditioning	Common Power Isolated Power Solid-State Driver Buffer – 0V to +10V Buffer – +1V to +5V Buffer – 4 mA to 20 mA Buffer – 10 mA to 50 mA	W400 W402 W403 A233 A234 A235 A236	Functional I/O Module
Screw Terminal/ Cable Assembly	Provides screw terminal connection for one word. Connects to signal-conditioning module.	BC40C	Signal-Conditioning Module

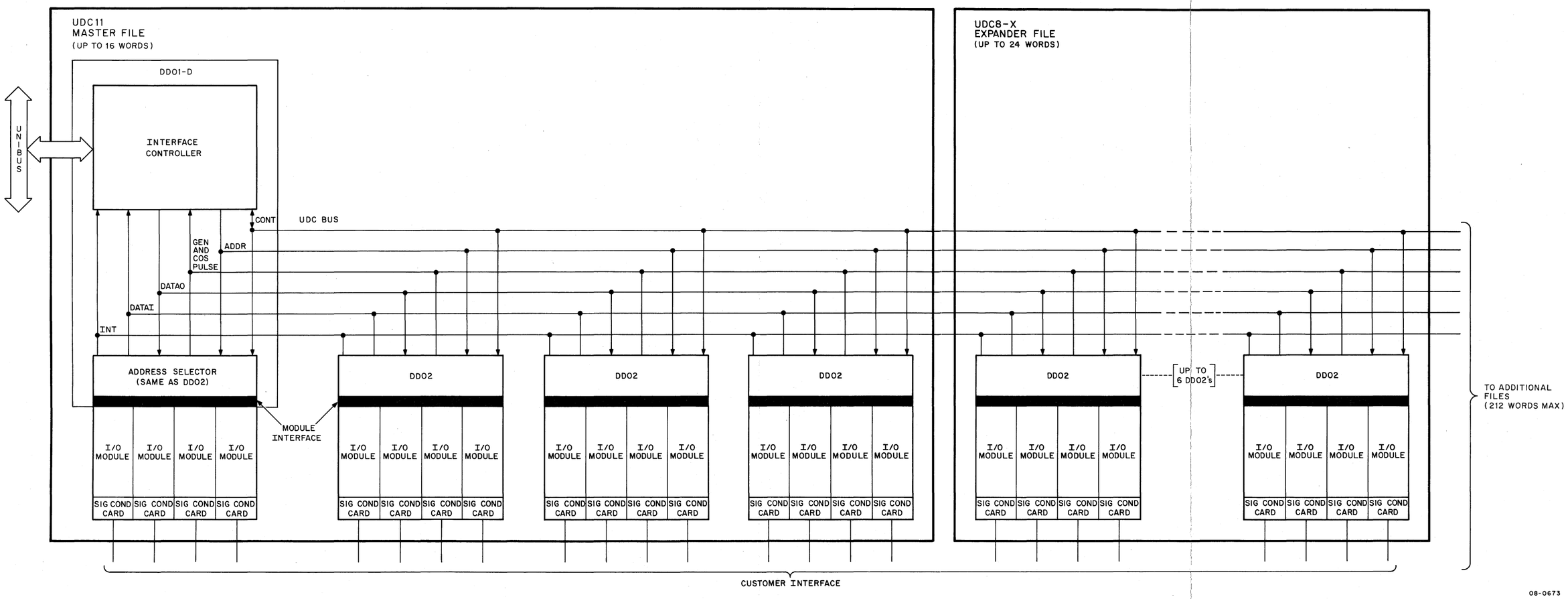

Figure 1-2 UDC11 Maximum Configuration Diagram

1.4.3.2 H740D Power Supply – The H740D Power Supplies are located at the rear of each logic cabinet. They produce regulated +5V at 17A maximum for the file logic circuits and I/O modules. The +5V and power ground outputs are made available at an output connector on the rear of the supply. These outputs are routed to each of the files by separate wire runs. Ground and +5V are connected from file unit to file unit, using jumpers on the rear of the G729 Modules. The supply contains a 15A fuse for +5V.

1.4.4 UDC11 Master File

The master file contains one DD01-D Master Control, space for up to 3 DD02 File Units, power supply harness, I/O bus cables, and bus terminators.

1.4.4.1 Master Control (DD01-D) – The DD01-D Master Control (Figure 1-3) occupies three file unit slots in a UDC11 Master File and offers four insertion slots for functional modules. Only one master control is required for full utilization of the UDC11. The module complement is listed in Table 1-2.

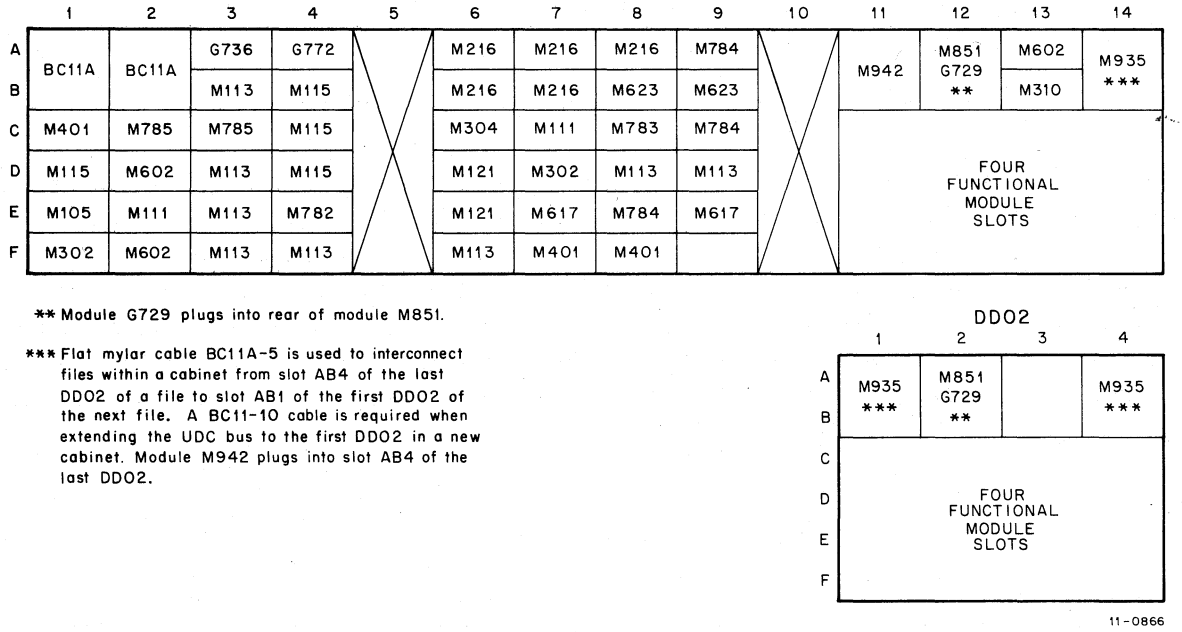

Figure 1-3 DD01-D and DD02 Configuration Diagram

Table 1-2
DD01-D Module Complement

Module	Name	Quantity
G736	Jumper Card	1
G772	Power Connector	1
M105	Address Selector	2
M111	Inverter	2
M113	Ten 2-Input NAND Gates	8
M115	Eight 3-Input NAND Gates	3
M121	AND/NOR Gates	2

(continued on next page)

Table 1-2 (Cont)
DD01-D Module Complement

Module	Name	Quantity
M216	Six Flip Flops	5
M302	Dual Delay Multivibrator	2
M304	One-Shot Delay	1
M310	Delay Line	1
M401	Variable Clock	3
M602	Pulse Amplifier	3
M617	4-Input Power NAND Gate	2
M623	Bus Driver	2
M7821	Interrupt Control	1
M783	Unibus Drivers	1
M784	Unibus Receivers	3
M785	Unibus Transceivers	2
M851	Bus Receiver and 8-Bit Address Decoder	1
M935	Bus Connector	1
M942	Bus Terminator	1

1.4.4.2 File Unit (DD02) – The DD02 File Unit occupies one of six available locations in a file and contains four slots for functional modules. Although 62 file units are required for full utilization of the UDC11, any number of file units (up to 62) can be serviced by one master control. The module complement of the DD02 is listed in Table 1-3. The DD02 is an expander assembly that contains 24 slots arranged in 4 vertical rows of 6 slots. The upper two slots in each row constitute an extension of the UDC bus. The lower four slots in each row constitute a unique address within the address field, into which any of the functional modules may be inserted. The M851 Address Decoder and G729 Address Jumper Modules occupy the second pair of slots in the bus section (AB2) and serve the four I/O slots below.

Table 1-3
DD02 Module Complement

Type/Part No.	Name	Quantity	Location
M935	UDC Bus Extender	1	AB1*
M851	Address Decoder/Bus Receiver	1	AB2
G729	Address Jumper Module	1	AB2 (Piggy-back on M851)

*See Paragraph 4.3.2 for bus extension details.

1.4.5 UDC11 Expander File

The expander file is a housing that contains a DD02 File Unit and may contain up to five additional DD02 File Units, a BC11 Bus Extender, and one M935 Bus Connector per DD02.

1.4.6 Functional Modules and Signal-Conditioning Modules

There are several types of functional modules available for the UDC11. Some serve as input modules for receiving sensory or control data from customer devices; others perform output functions for controlling customer devices. A detailed description and a schematic for each module currently available are contained in Chapter 4.

The functional modules are plugged into slots provided by the master file, expander files, and DD02 File Units (Figure 1-4). Each functional module requires a signal-conditioning module for normalizing input voltages, fusing, arc suppression, and for connection to field wiring. These modules are also described in Chapter 4. The 16 data bits and field power connections on the signal-conditioning module are brought to the screw terminal cabinet via a cable consisting of 18 twisted pairs.

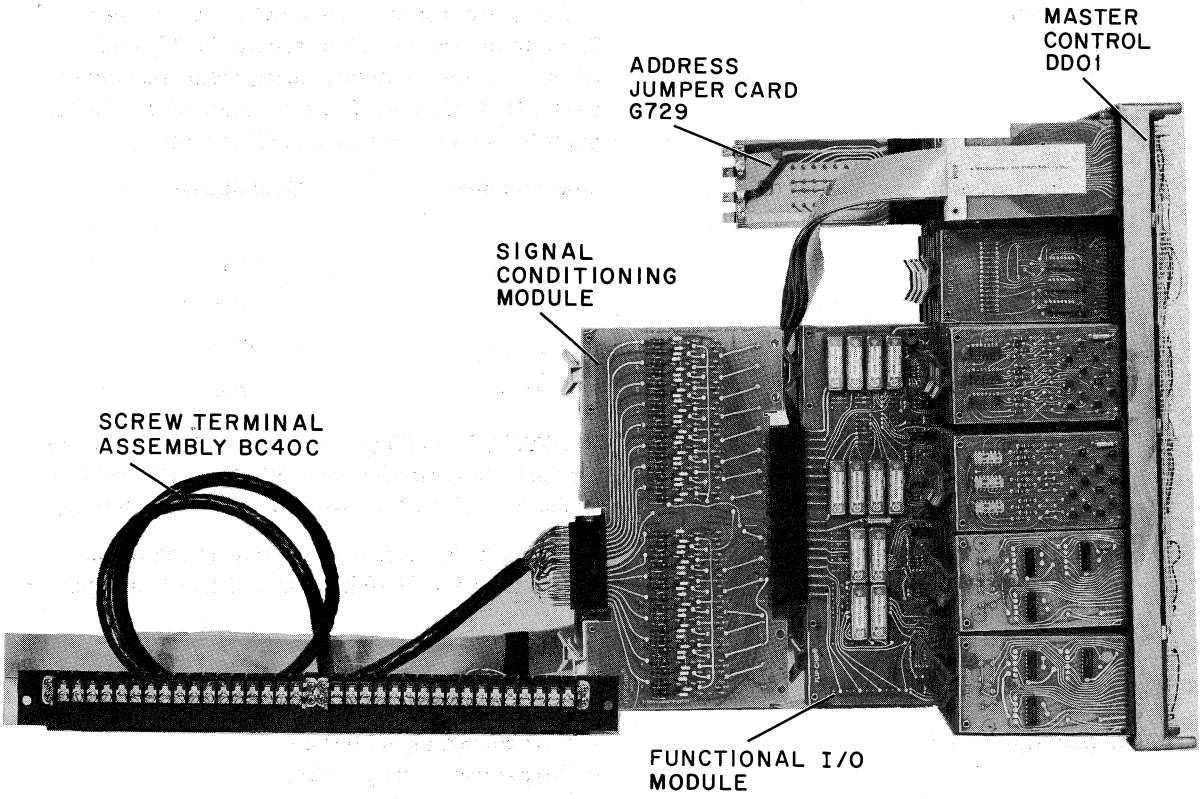

Figure 1-4 UDC11 Assembly Details

1.4.7 Screw Terminal Cable Assembly (BC40C)

Field wiring is connected to screw terminal assemblies (BC40C-4) that make the necessary connections between the signal-conditioning modules and the field-wiring terminations. Each BC40C Assembly makes connections available through 16 of the 18 twisted pairs for control wiring. The two remaining pairs provide paralleled conductors for bringing in external excitation power when using common power signal conditioning. Each circuit is completed through a twisted pair of No. 26 AWG stranded color-coded wires connected to a pair of screw terminals. The terminals will accommodate No. 14 AWG wire, and are arranged in two strips of 17 terminals, each supported in line by a common steel angle support.

1.5 SPECIFICATIONS

1.5.1 General

Operating temperature:	0°C to 50°C
Humidity:	Up to 95% without condensation
Cooling and filtering:	Dust filters and blower fans in each logic cabinet with bottom exhaust
Input cabling:	Top or bottom entry to supplied screw terminals. Screw terminals will accommodate No. 14 AWG wires. However, customer wiring should be limited to No. 18 AWG (max) 2-wire twisted pair per digital point for a fully-wired cabinet (72 words).

Cabinet dimensions:	**Single Cabinet**	**Dual Cabinet**
Height:		
Bottom entry:	72 in.	72 in.
Top entry:	75 in.	75 in.
Width:	21 in.	42 in.
Depth:	30 in.	30 in.

Power:	115/230V, 50 to 60 Hz, single-phase, 500 VA (max) for logic. Possible additional 700W for 48V field excitation in 72 16-bit words of signal conditioning.
Heat dissipation:	1800 Btu/hr for logic power. Possible additional 2500 Btu/hr for 72 16-bit words of signal conditioning.

1.5.2 System Performance

Modes of operation:	a. Programmed digital output b. Programmed analog output c. Programmed digital input d. Interrupt controlled input e. Interrupt controlled counting function
Data format:	(See Paragraph 2.5)
Number of digital inputs and outputs:	252 16-bit words (4032 digital points) maximum.
Type of input and output:	See functional modules described in Chapter 4.
Input and output word (module) selection:	Directly addressable.
Interrupt module identification:	4-bit module Generic code and an 8-bit address
Interrupt scan:	Locates address and module types in a minimum of 1 μs (nominally 5 μs and worst case 20 μs).
I/O data rate:	1×10^5 16-bit word/sec
Computer interface:	Direct interface to PDP-11 Family Computer
System clock rates:	Three clocks are available to each I/O word: a. Line frequency 0.63 Vrms, 60 Hz b. 175 Hz – 1.75 kHz adjustable c. 1.75 kHz – 17.5 kHz adjustable

For functional and signal-conditioning module specifications, see Chapter 4. For controller module replacement schematics, see Volume II.

1.6 REFERENCE DOCUMENTS

The following documents are essential in gaining an understanding of the PDP-11 computer system:

PDP-11 Processor Handbook
PDP-11 Peripherals Interfacing Handbook
PDP-11 Unibus Interface Manual
PDP-11 Papertape Manual
PDP-11/20 Maintenance Manual

The following diagnostic programs are essential in establishing the performance of the UDC11 subsystem:

UDC11 Control Test	MainDEC-11-D8HA-D
UDC11 Function Exerciser	MainDEC-11-D8JA-B

For functional and signal-conditioning module specifications, see Chapter 4. For controller module replacement schematics, see Volume II.

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CHAPTER 2
OPERATION AND PROGRAMMING

2.1 INTRODUCTION

Operation of the UDC11 is controlled entirely by the PDP-11 computer program. All I/O and control programming is done by using the normal single or double operand instructions (MOV, CMP, CLR, INC, etc.) A major programming convenience provided by the UDC11 is that direct programmed I/O can be performed with any one of the 252 functional I/O modules with a single instruction.

2.2 ADDRESS FORMAT

The UDC11 is assigned 256 Unibus addresses (256 words or 512 bytes) from the PDP-11 address map. Three addresses are assigned to the UDC controller, 252 addresses are assigned to functional I/O module slots, and one address is not used. The addresses are:

Bus Address (Octal)	Assignment
771776	UDCR (control and status register)
771774	UDSR (scanner register)
771772	MCLK (maintenance clock)
771770	not used
771766	Functional I/O Modules (252)
771764	
.	
.	
.	
771000	

All information transfers between the processor and the UDC11 flow through these locations. The base address and address format defined in Figure 2-1 must be used to access the UDC and its 256 locations.

Direct programmed I/O to any UDC11 functional I/O module, the UDCR, or the UDSR can be accomplished by a single MOV instruction.

NOTE
UDC11 functional I/O modules, the UDCR, and the UDSR are not byte addressable for output (write) operations.

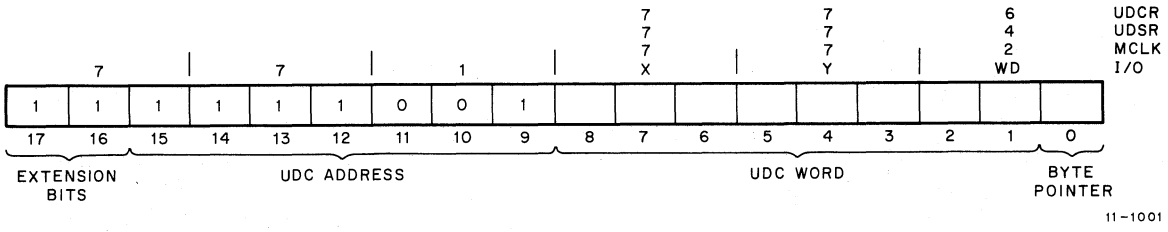


Figure 2-1 Address Format

The UDSR can only be read (input operations) and the MCLK can only be addressed. Whenever MCLK is addressed, a clock pulse is generated in the UDC controller to advance the UDSR in the maintenance mode.

NOTE

In machines not equipped with memory relocation options, the EXT bits are ignored. Therefore, a 1 instead of a 7 should be used as the first digit of UDC addresses when coding programs. Otherwise, a truncation error (T) will occur during assembly.

2.3 UDCR FORMAT

The UDCR, UDC control and status register, contains 16 bits of storage for control, status, and maintenance functions. These bits can be set, reset, or tested directly or indirectly under program control to monitor and control the operation of the UDC11. Figure 2-2 along with Table 2-1 define and explain each bit of the UDCR.

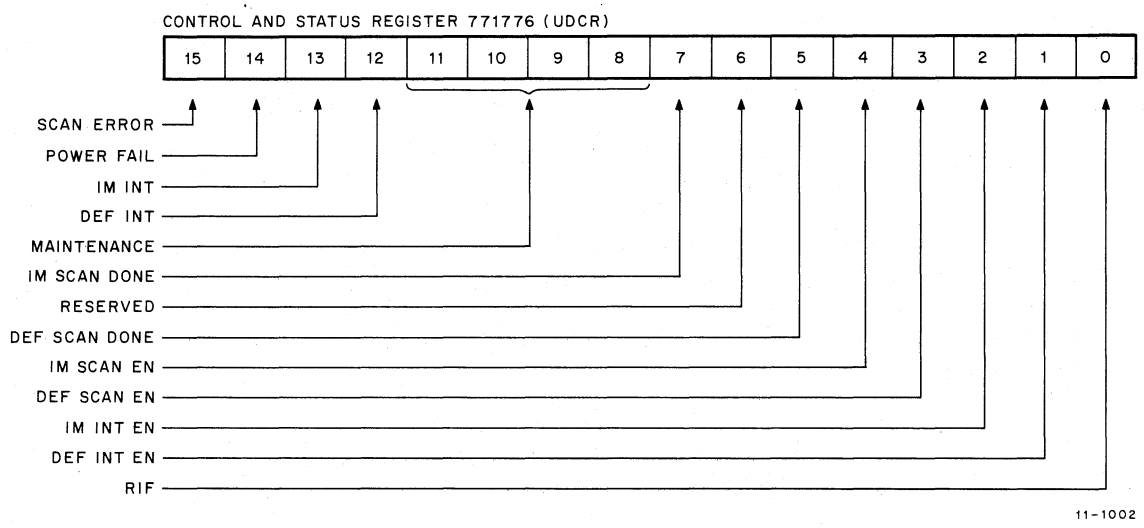


Figure 2-2 UDCR Format

Table 2-1
UDCR Bits

Bit	Name	Description	Operation
15	SCAN ERROR	Reset whenever scanner (IM or DEF) is started, INT EN (IM or DEF) bits are set, or RIF (reset interrupt flag) bit is set. Set when overflow occurs after scanner is started.	When set causes BR6 if IM INT EN bit is set. Also sets UDSR to 377_8.
14	PWR FAIL	Set by power fail in UDC Expander cabinets.	Same as bit 15.
13	IM INT	Set by field interrupt device connected to contact interrupt module (IM) or by counter module (IM). Reset when addressing module as destination with RIF bit set.	Indicates presence of IM request on UDC bus and starts scanner register if IM SCAN EN bit is set. If IM SCAN EN bit is not set the IM INT bit can be tested to see if a request is pending.
12	DEF INT	Set by field interrupt device connected to contact interrupt module (DEF) or by counter module (DEF). Reset when addressing module as destination with RIF bit set.	Indicates presence of DEF request on UDC bus and starts scanner register if DEF SCAN EN bit is set. If DEF SCAN EN bit is not set, the DEF INT bit can be tested to see if a request is pending.
11	M STP WD	Set and reset under program control. When reset, scanner operates normally – WD section of scanner advances one count each time MCLK is addressed. When set, WD section of scanner stops advancing when MCLK is addressed.	Used for diagnostic purposes to generate the STP WD signal.
10	M STP Y	Set and reset under program control. When reset, scanner operates normally – Y section of scanner advances one count each time MCLK is addressed. When set, Y section of scanner stops advancing when MCLK is addressed.	Used for diagnostic purposes to generate the STP Y signal.
09	M STP X	Set and reset under program control. When reset, scanner operates normally – X section of scanner advances one count each time MCLK is addressed. When set, X section of scanner stops advancing when MCLK is addressed.	Used for diagnostic purposes to generate the STP X signal.
08	M MODE	Set and reset under program control. This bit must be reset during normal operation. When set, an IM or DEF request can be produced on the UDC bus by setting the IM INT EN bit or the DEF INT EN bit. When reset, these requests can only come from the contact interrupt modules or the counters.	Used for diagnostic purposes to cause an IM or DEF request on the UDC bus. If either SCAN EN bit is set the scanner is automatically started. The scanner will then overflow causing a BR6 since no address will be found.

(continued on next page)

Table 2-1 (Cont)
UDCR Bits

Bit	Name	Description	Operation
07	IM SCAN DONE	Set at the completion of an IM scan. Reset when reading module data with RIF bit set. Also reset when INT EN (DEF and IM) bits are changed from zero to one.	Indicates that IM interrupt module or counter has been found and is waiting for service. When this bit is set while IM IN EN bit is set, a BR6 is issued by the UDC11.
06	Reserved		
05	DEF SCAN DONE	Set at the completion of a DEF scan. Reset when reading module data with RIF bit set. Also reset when INT EN (DEF and IM) bits are changed from zero to one.	Indicates that DEF interrupt module or counter has been found and is waiting for service. When this bit is set while DEF INT EN bit is set, a BR4 is issued by the UDC11.
04	IM SCAN EN	Set and reset under program control. When set, an I/O interrupt request on the UDC bus will start the scanner. When reset, the immediate bus request will not start the scanner.	Used to enable and disable the scanner to search for the address of the module issuing the immediate bus request.
03	DEF SCAN EN	Set and reset under program control. When set, a DEF interrupt request on the UDC bus will start the scanner. When reset, the deferred bus request will not start the scanner.	Used to enable and disable the scanner to search for the address of the module issuing the deferred bus request.
02	IM INT EN	Set and reset under program control. When set, BR6 is issued at the completion of an immediate scan (IM SCAN DONE bit is set), a scan error, or power failure. When reset, no IM bus request is issued.	Used to enable and disable the interrupt logic for issuing BR6 after an immediate scan or a failure.
01	DEF INT EN	Set and reset under program control. When set, BR4 is issued at the completion of a deferred scan (DEF SCAN DONE bit is set). When reset, no DEF bus request is issued.	Used to enable and disable the interrupt logic for issuing BR4 after a deferred scan.
00	RIF	Set and reset under program control. When set, the SCAN DONE (IM or DEF) bit is reset and the interrupting module flag is reset by addressing the module. When reset while addressing the module, the SCAN DONE bit and interrupting module flag are not reset.	Used to re-enable the scanner and reset the flag of the interrupting module.

NOTE: Initialize resets all bits.

2.4 UDSR FORMAT

The UDSR, UDC scan register, contains 16 bits of storage for identifying the interrupting module. These bits can only be read or tested under program control to determine what type of service the module requires. Table 2-2 and Figure 2-3 define and explain each bit of the UDSR.

Table 2-2
UDSR Bits

Bit	Name	Description	Operation
15	DEF VALID	Set when an IM interrupt request appears on the UDC bus after a DEF scan started and before the BR4 is fully serviced. Reset when either an IM or DEF interrupt request is serviced by reading the module data with the UDCR RIF bit set.	An IM interrupt request displaces a DEF interrupt request; therefore, if DEF INVALID is set when service of BR4 is started, that means that IM scan has started and the BR4 address is invalid.
14	P CL	Hardwired. Set by contact interrupt module jumper. This jumper should be removed if contact closures are not of interest to the user.	When UDSR is read and this bit is set, it indicates that a test should be made for contact closures at the location specified by the UDSR.
13	P OP	Hardwired. Set by contact interrupt module jumper. This jumper should be removed if opening contacts are not of interest to the user.	When UDSR is read and this bit is set, it indicates that a test should be made to isolate those contacts that have opened at the location specified by one UDSR.
		NOTE **If both contact closures and opening contacts are of interest on a given module, both jumpers must be in place. All devices connected to a given contact interrupt module should have the same contact state (or states) of interest in common.**	
12	Reserved		
11 10 09 08	GEN 0 GEN 1 GEN 2 GEN 3	Hardwired. Set by logic on contact interrupt modules or counters. These bits represent a 4-bit binary code that identifies the type of module that interrupted. The following codes are assigned: **Generic Code — 0 1 2 3** Contact Interrupt W733 — 0 0 1 0 Contact Interrupt W743 — 0 0 1 1 I/O Counter W734 — 0 1 0 0 I/O Counter W734 — 0 1 0 1 I/O Counter W734 — 0 1 1 0 I/O Counter W734 — 0 1 1 1	4-bit Generic code of interrupting module specifies the type of service that the module requires.
07-00	SCAN VALUE	Set by stop logic of scanner, scan error, or power fail. Reset when a new scan is slanted and when the UDC11 is initialized.	8-bit address of interrupting module location slot.

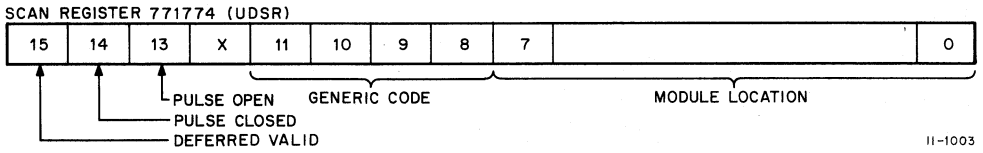


Figure 2-3 UDSR Format

2.5 DATA FORMAT

A 16-bit data word can be transferred between (to or from) a functional module and a preassigned core memory location and between I/O modules with a single MOV instruction. The digital I/O modules are designed to handle all 16 bits, while the DAC module uses only the 12 most significant bits of the data word. Each DAC module contains 4 individual DACS, and therefore, two of the 12 bits of the DAC data word represent the channel number and the remaining 10 bits are the DAC input data. The data format for each type functional module is illustrated in Figure 2-4.

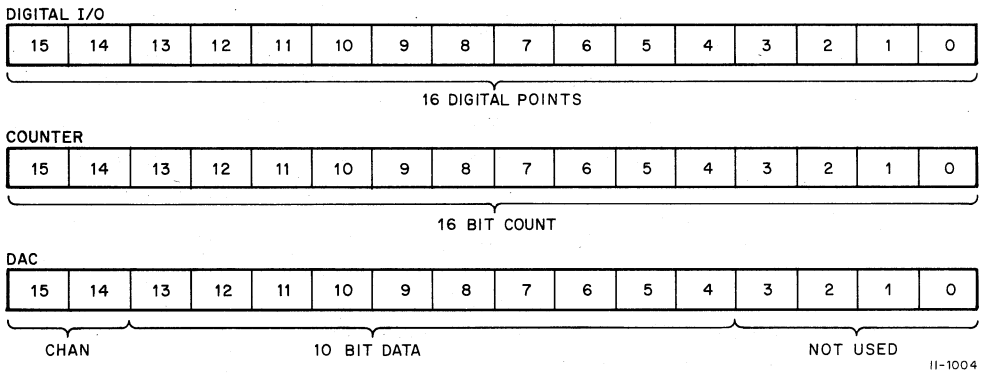


Figure 2-4 Data Format

2.6 INTERRUPT STRUCTURE

The UDC11 control has two major states: that of programmed I/O, and that of searching for a service request (requested by a field device or counter). Since the request search is completely asynchronous and software overhead to test the state of the control before each data transfer is prohibitive, all programmed data transfers will take precedence over the hardware scan to locate a requesting I/O module.

2.6.1 I/O Service Requests

Two types of service requests exist for UDC11 I/O modules. They are hardwired on the module by jumper selection, and are classed as *immediate* and *deferred.* The DD01-D, by program control, selects what type of request it cares to service. Selection is governed by four bits in the control and status register (UDCS 771776).

Bit 04 – IM SCAN EN
Bit 03 – DEF SCAN EN
Bit 02 – IM INT EN
Bit 01 – DEF INT EN

Four bits instead of two are used to afford the programmer additional flexibility in servicing the I/O service requests.

For example:

1. SCAN EN – ON
   INT EN – ON

   Enable interrupt structure to automatically search for address of module issuing the service request and issue a bus request (BRX).

2. SCAN EN – ON
   INT EN – OFF

   Wait for scan done without issuing a bus request using a program loop.

3. SCAN EN – OFF
   INT EN – ON

   Test INT bit to see if request is pending, interrupt on power fail or scan error at BR6, or generate service request in M MODE without starting scanner.

4. SCAN EN – OFF
   INT EN – OFF

   Disable interrupt structure handling one type service request to service the other. INT bit can be tested to determine if request is pending.

The sample program and flowchart (Figure 2-5) illustrate some of the programming techniques that can be used to handle UDC11 interrupts. Both INT EN bits and both SCAN EN bits are assumed to be set when entering this routine.

NOTE
This sample program is typical of a software handler program and is not intended to perform any stand-alone function.

2.6.1.1 Immediate Requests – Immediate scan requests take precedence over deferred scan requests. An immediate request, once posted on the UDC bus, will initiate a scan for its word address. If an immediate scan is in progress at the time of another immediate request, the request will remain posted on the UDC bus. (The second request may or may not be selected during the first scan, depending on its *word priority* and the present location of the immediate scanner when the second interrupt was posted.) Immediate scan takes 20 μs max.

2.6.1.2 Deferred Requests – Deferred requests from the UDC may be scanned for if there are no immediate requests posted. An immediate request will shut down a deferred scan and retain control until the immediate request is found. Deferred scan takes 20 μs max (with no immediate request present).

2.6.2 Processor Interrupts

The DD01-D interrupts the PDP-11 processor when it has located the address of the I/O module requesting service. Each level of UDC11 requests (immediate and deferred) will provide interrupts on separate PDP-11 request levels as follows:

Immediate – BR6
Deferred – BR4

A processor interrupt will also occur if dc power fails in any expander file or if a logic fault causes a scan error. Both occur at BR6 and are enabled at the immediate level.

```
                TSTB    @ #171776           ;TEST UDCR FOR IMED DONE
                BLT     IMED                ;IMMEDIATE ACTION
                BR      DEF                 ;DEFERRED ACTION
IMED:           CMPB    #377, @ #171774     ;TEST UDSR FOR ERROR CODE
                BEQ     FAIL                ;FAILURE ACTION
                  :                         ;IMMEDIATE ACTION
FAIL:           TST     @ #171776           ;TEST UDCR FOR SCAN ERROR
                BLT     SCERR               ;SCAN ERROR ACTION
                  :                         ;POWER FAIL ACTION
DEF:            MOV     #300, @ #177776     ;SET CPU PRIORITY TO LEVEL 6
SCANNER:        MOV     @ #171774, R5       ;SAVE UDSR FOR EXIT
TEST:           TST     R5                  ;TEST DEF
                BLT     TEST                ;INVALID
                MOV     #170377, R4         ;SET UP GENERIC CODE MASK
                MOV     R5, R2              ;GET SAVED UDSR
                BIC     R4, R2              ;CLEAR ALL BUT GENERIC CODE
                CMP     #1000, R2           ;TEST FOR CONTACT INTERRUPT
                BEQ     CONTACT             ;CONTACT ACTION
                CMP     #1400, R2           ;TEST FOR CONTACT INTERRUPT
                BEQ     CONTACT             ;CONTACT ACTION
                  :                         ;TEST FOR OTHER MODULES
CONTACT:        MOV     R5, R4              ;GET SAVED UDSR
                BIC     #177400, R4         ;CLEAR ALL BUT MODULE LOC CODE
                ASL     R4                  ;CONNECT TO MODULE ADDRESS
                MOV     171000 (R4), R3     ;GET MODULE DATA AND STORE
                  :                         ;UPDATE BIT STATUS
                MOV     #340, @ #177776     ;SET CPU PRIORITY TO LEVEL 7
OPTIONAL:       BR      ALT                 ;OPTIONAL PATH
                INC     @ #171776           ;ENABLE MODULE FLAGS
                TST     171000 (R4)         ;RESET MODULE FLAG
                DEC     @ #171776           ;DISABLE MODULE FLAGS
                MOV     #200, @ #177776     ;SET CPU PRIORITY TO LEVEL 6
                  :                         ;TEST STORED DATA WITH CURRENT DATA
                RTI                         ;EXIT WITH IM + DEF INT EN
                 or
                BIC     #2, @ #171776       ;DISABLE DEF INT
                BIT     #10000, @ #171776   ;CHECK IF DEF REQ IS PENDING
                BEQ     DONE
                RTI
DONE:           BIT     #40, @ #171776      ;TEST FOR DEF SCAN DONE
                BNE     DONE
                BR      DEF
ALT             BIC     #6, @ #171776;      ;TEMP KILL BOTH INTERRUPTS
                BIS     #4, @ #171776       ;EN IMED INT
                RTI
```

SAMPLE PROGRAM

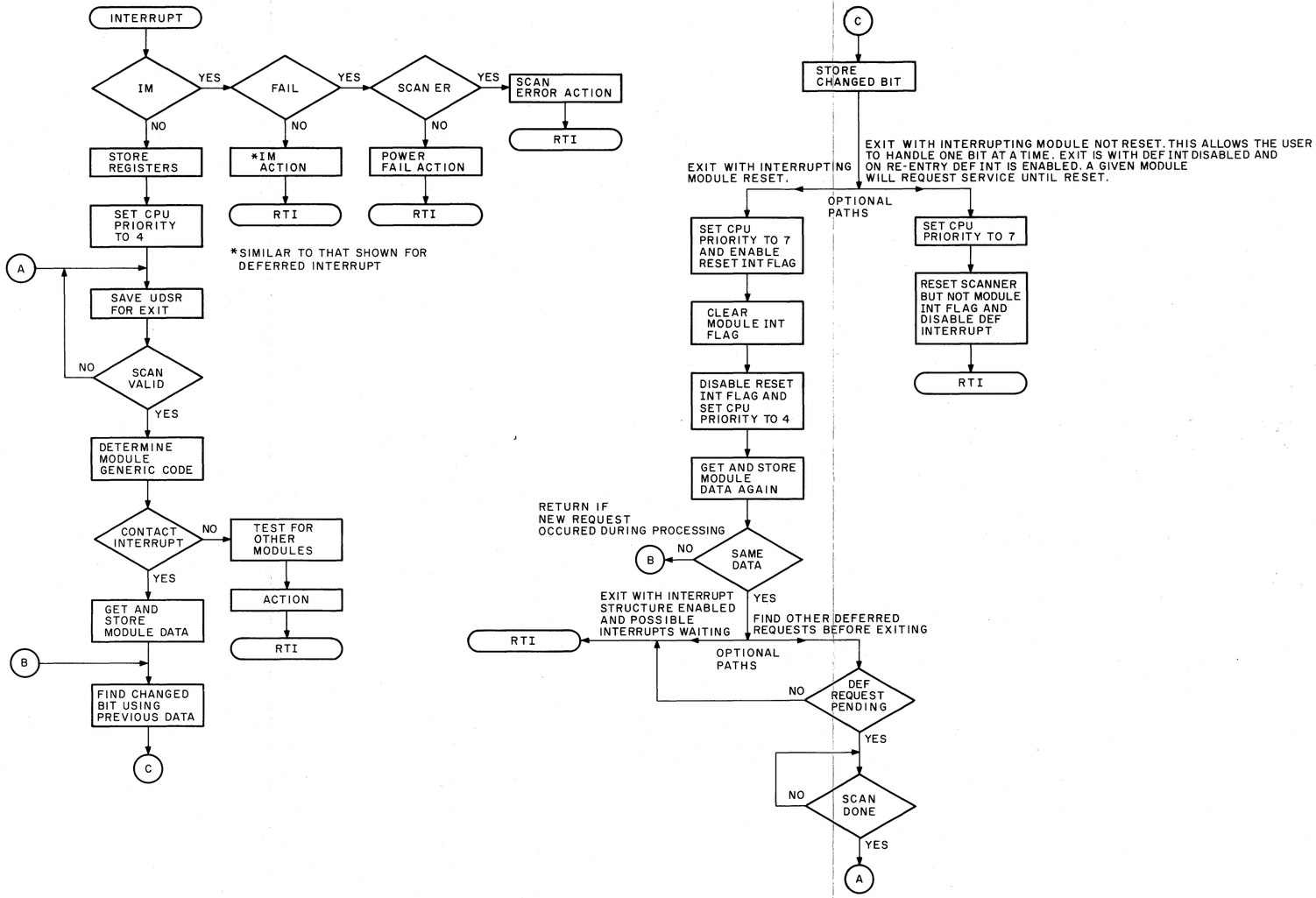


Figure 2-5 UDC11 Program Flowchart

2.6.2.1 Immediate and Deferred Interrupts – Since immediate requests take priority over deferred requests, the programmer must test the state of the DEF INVALID bit (bit 15, UDSR) in the scan register. Thus, if the program is in the process of reading a deferred interrupt and an immediate request has come in, the DEF INVALID bit will be set. The program should then test bit 07 of the UDCR for an immediate scan done (IM SCAN DONE) or wait for BR6.

2.6.2.2 System Security Interrupts – Two interrupts indicating system problems can occur: SCAN ERROR (bit 15, UDCR) and PWR FAIL (bit 14, UDCR). These interrupts occur on the same Unibus request level and with the same vector address as the Immediate UDC interrupt. Either request causes the scan value in the UDSR to assume the address of the status register (UDCR). Thus when the program receives the address of the status register from an immediate interrupt, a reading of the status register should be made to determine what type of interrupt occurred.

CHAPTER 3
PRINCIPLES OF OPERATION

3.1 GENERAL

The UDC11 is capable of handling digital inputs, digital outputs, analog outputs, and service requests. Each type of functional module is associated with one or more of these functions. Therefore, depending on the type of modules used at an installation, some or all of the UDC functions may be employed. Descriptions and simplified schematics of the functional modules are presented in Chapter 4. Block and simplified logic diagrams of the UDC11 are included in this chapter, and all detailed schematic diagrams are included in Volume II of this manual.

3.2 BLOCK DIAGRAM ANALYSIS

A block diagram of the UDC11, showing the DD01-D Interface Controller, one DD02 Address Selector, and one functional module with associated hardware, is presented in Figure 3-1. The UDC11, connected to the Unibus along with other PDP-11 devices, can be directly addressed for programmed I/O operations or can issue a bus request (BR4 or BR6) when field devices request service. The following 256 addresses have been assigned to the UDC11:

771776 – Control and Status Register (UDCR)
771774 – Scan Register (UDSR)
771772 – Maintenance Clock (MCLK)
771770 – Not Used
771766–771000 – I/O Module Slots

NOTE

In machines not equipped with memory relocation options, the EXT bits are ignored. Therefore, a 1 instead of a 7 should be used as the first digit of UDC addresses when coding programs. Otherwise, a truncation error (T) will occur during assembly.

The M105 Address Selectors recognize these addresses (A17–01) and produce gating signals for moving data into (load) and out of (read) the addressed locations. The M105 Address Selectors do not recognize individual I/O module addresses; they only recognize that the address falls in the module address set. The LD SCAD (load scan address) signal is produced by the M105 Address Selector when an I/O module is addressed. This signal gates the address on the Unibus into the DD02 address selectors where the address is then decoded. Not all registers and I/O modules can be loaded and read. Table 3-1 identifies those registers and I/O modules that can be loaded with data and those that can be read.

Any of the single and double operand instructions may be used to perform the programmed I/O operations. The only limitation is that a byte instruction should not be used to load data into any UDC location. However, a byte instruction can be used to read data from any UDC location.

Table 3-1
Loading and Reading Data

Module/Register	Load Data	Read Data
UDCR **	X	X
UDSR		X
MCLK *		
W731 (sense)		X
W741 (sense)		X
W733 (interrupt)		X
W743 (interrupt)		X
M685 (relay)	X	
M687 (single-shot)	X	
M803 (latch)	X	
M805 (flip-flop)	X	
A633 (DAC)	X	
W734 (counter)	X	X

*This location is not a register. When addressed, however, an MCLOCK pulse is generated. The TST instruction should be used to generate the MCLOCK pulse.

**The error and done bits of the UDCR cannot be set under direct program control.

Service requests can be issued by the contact interrupt or the counter modules. If a service request is issued, and no programmed I/O is taking place, the UDSR is clocked (if enabled) until the requesting module is found. The STOP commands from the module inhibit the clock when the address is found. If a programmed I/O takes place while the UDSR is searching for the service request, the clock is inhibited for the duration of the programmed I/O. The address gate (Figure 3-1) passes the UDSR address during the search and the Unibus address during the programmed I/O. When the address of the module requesting service is found by the UDSR, the SCAN DONE bit in the UDCR is set and interrupt vector 234_8 may be issued by interrupt control M782. The vector will point to the handler for servicing the UDC. When the processor grants the bus to the UDC, programmed I/O will normally take place to read or test the UDSR and the UDCR to determine the type of service requested.

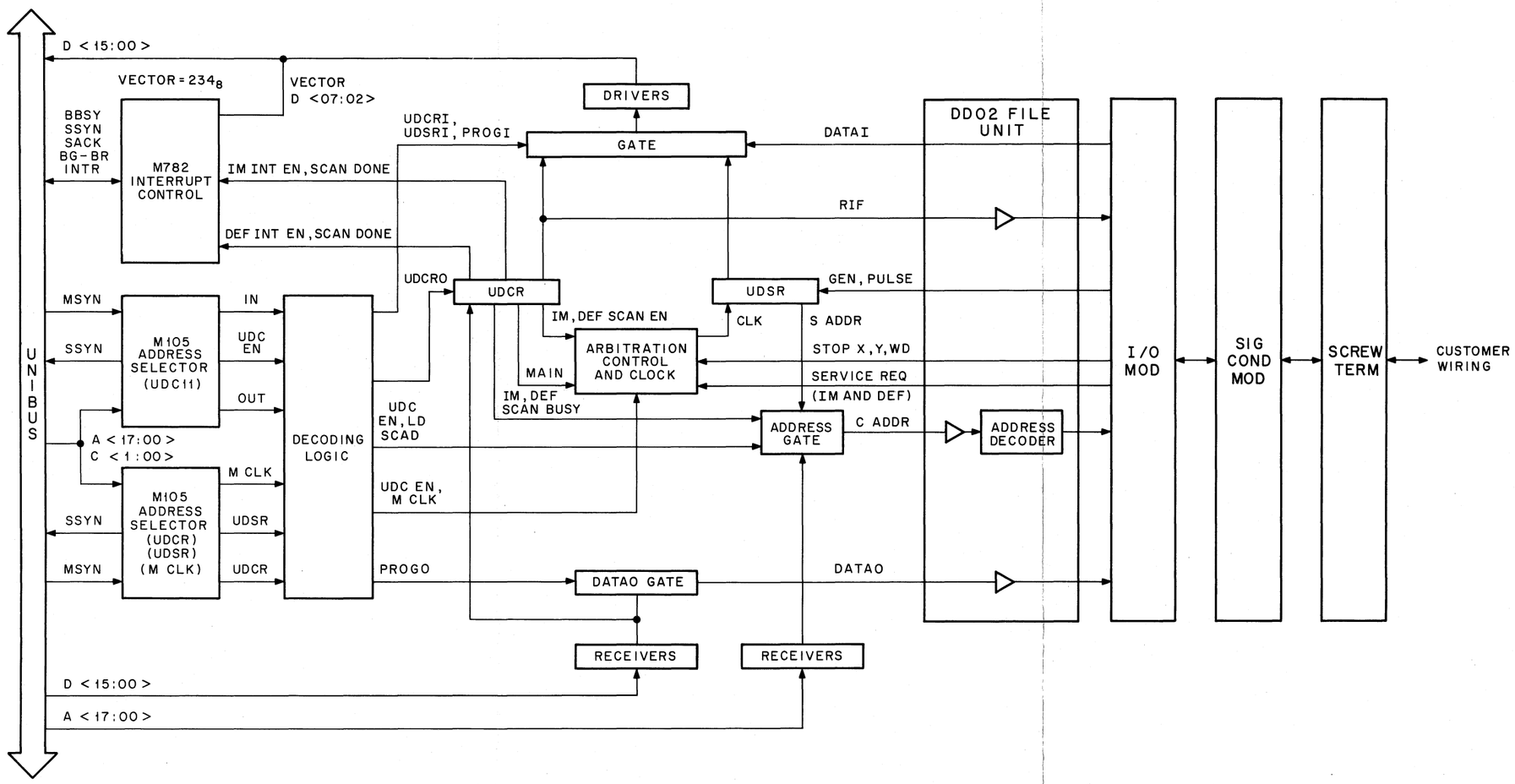
To change the operating mode of the UDC11, the UDCR can be loaded with a new control word before or after the UDC11 is serviced depending on application or programming requirement.

3.3 ADDRESSING

Each address selector module provides gating signals for up to 4 full 16-bit device registers. Because the UDC11 has 256 device registers, two address selector modules are connected to the address lines of the Unibus in a unique fashion to obtain the desired gating signals for addressing 256 locations (Figure 3-2). One address selector to all 256 assigned addresses, bits 01 through 08 are arbitrary, while the remaining bits must have a specific bit pattern (771XXX); the other address selector responds to only 4 assigned addresses, bits 01 and 02 specify one of 4 addresses, and the remaining bits must have a specific bit pattern (77177X where X is 0, 2, 4 or 6).

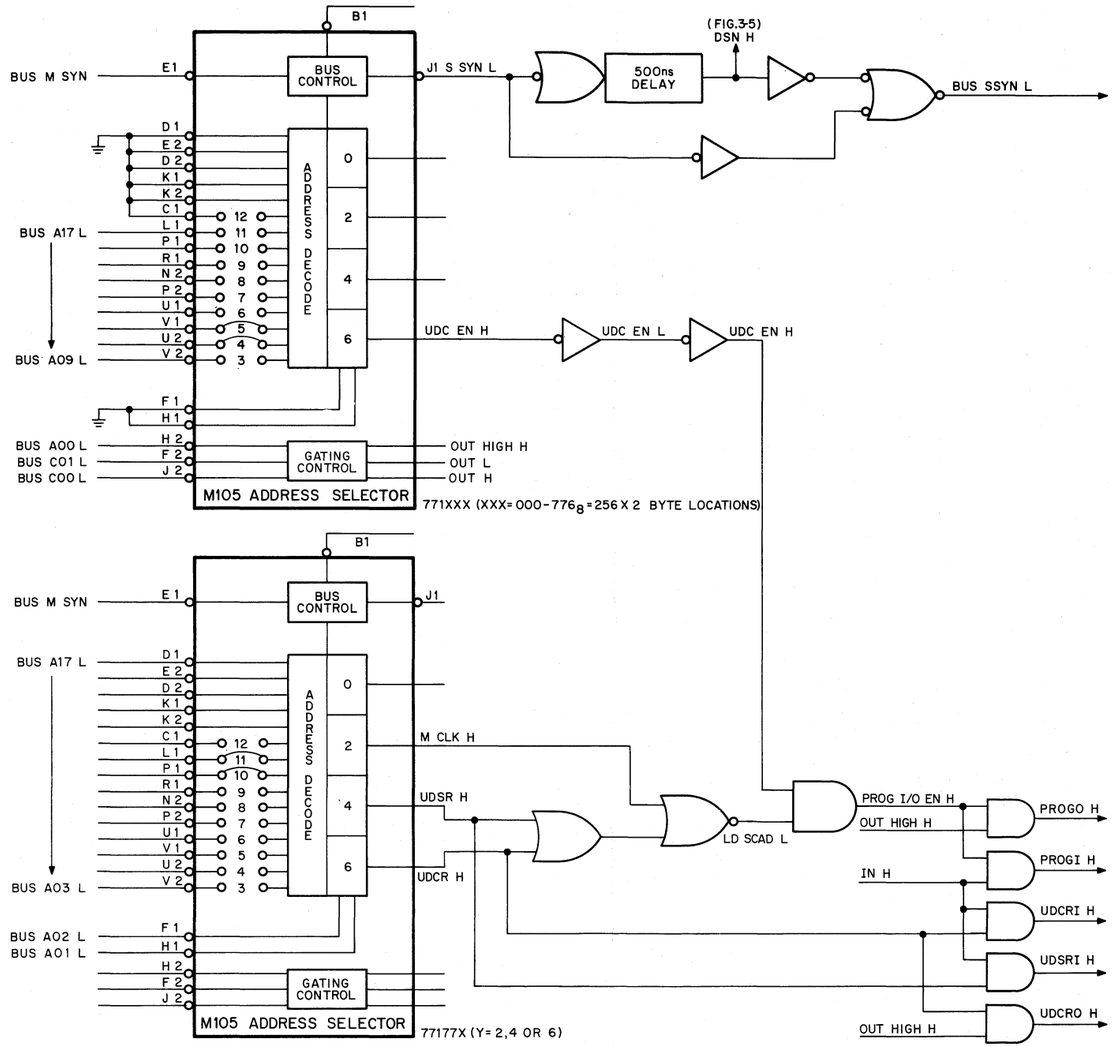
The address selectors produce the following select signals:

a. UDC EN H
b. M CLK H
c. UDSR H
d. UDCR H



11-0869

Figure 3-1 UDC11 Detailed Block Diagram



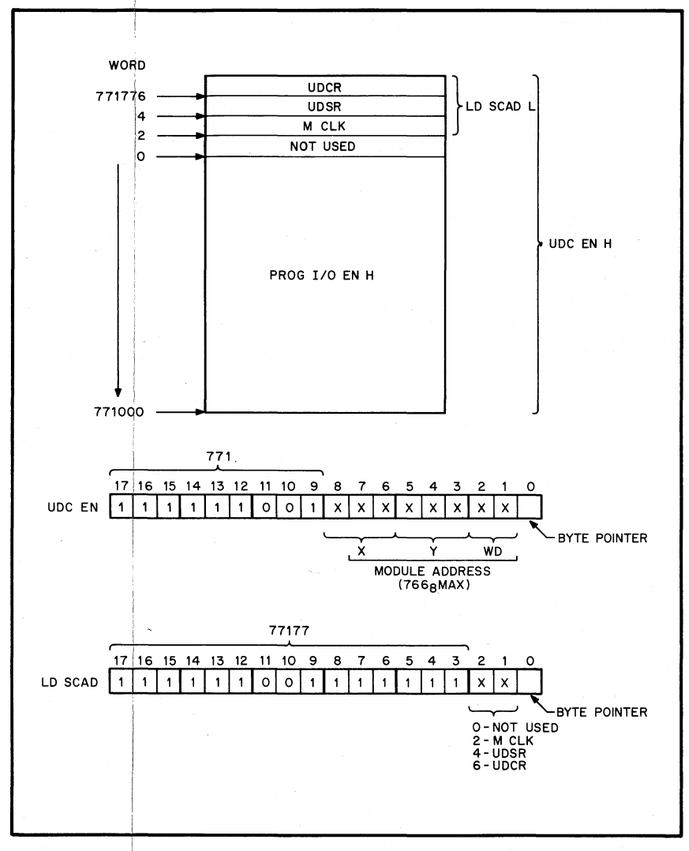


Figure 3-2 Address Selector Logic

These select signals and gating signals OUT HIGH and IN are decoded by combinational logic circuits to obtain the following UDC11 gating signals:

a. PROGO
b. PROGI
c. UDCRI
d. UDCRO
e. UDSRO

The suffix I and O corresponds to data input and data output gating functions, respectively.

3.4 DATA AND ADDRESS GATING

The gating logic is illustrated in Figure 3-3. A set of sixteen 3-input AND/OR gates (A) is used to facilitate gating data from the UDCR, the UDSR or DATAI from an input module onto the data lines of the Unibus. Output data addressed to the UDCR is clocked directly into the UDCR, and output data (DATAO) addressed to an output module is gated through a set of 16 NAND gates (B). The DD02 Address Selector receives and decodes the I/O module address. This address is gated through a set of eight 2-input AND/NOR gates (C). The source of the address is the Unibus or the UDSR depending on whether a programmed I/O is taking place or a service request is being scanned. The programmed I/O always takes precedence over the scan. The scanner address is disconnected when a programmed I/O to an I/O module is executed because the UDC EN L signal goes low and PROG I/O EN H goes high for that period.

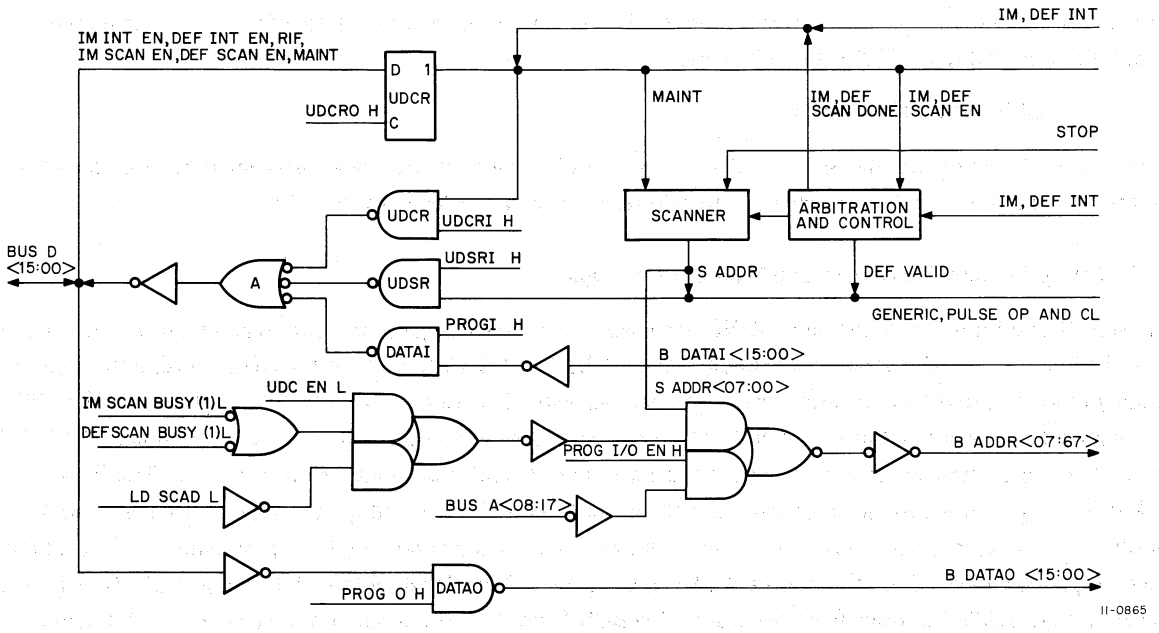


Figure 3-3 Address and Data Gating Logic

3.5 INTERRUPT LOGIC

All service requests are processed by the UDC11 interrupt logic. Included in the interrupt logic are circuits for service request arbitration (immediate or deferred) and scan control, the scanner and clock, and the interrupt control. The interrupt logic can be enabled under program control to service only immediate, only deferred, or

both types of service requests. The following bits of the UDCR establish the operating mode of the interrupt logic during normal operation.

DEF INT EN – bit 01
IM INT EN – bit 02
DEF SCAN EN – bit 03
IM SCAN EN – bit 04

These bits can be read, set, or reset under program control to change the operating mode of the UDC11. When the SCAN EN bits are set, the scanner will search for the module that issued the service request. An immediate request will always take precedence. After the scanner finds the address, one of two UDCR bits will be set depending on whether the request was immediate or deferred. These bits are:

DEF SCAN DONE – bit 05
IM SCAN DONE – bit 07

The SCAN DONE bits can only be read under program control. Setting a SCAN DONE bit if the corresponding INT EN bit is set will cause the UDC11 to issue a bus request (BR). The UDC11 can issue the following two bus requests:

BR4 for deferred requests
BR6 for immediate requests, scan error and power fail

If the interrupt logic is enabled to service both immediate and deferred service requests, and an immediate request comes in while a deferred request is being scanned, then the deferred scan aborts, and an immediate scan starts. If the immediate request comes in after the deferred scan is done but before the data from the deferred request is read, then the following UDSR bit will be set.

DEF INVALID – bit 15

When set, this bit indicates that an immediate request displaced a deferred request and when the user program returns to operate on the deferred request the address in the scanner may not be valid.

3.5.1 Service Request Arbitration and Scan Control Logic

Two sets of two flip-flops, BUSY and DONE, are used in the service request arbitration and scan control logic to store the immediate and deferred scan status (Figure 3-4). The SCAN EN bits of the UDCR enable the logic to handle immediate, deferred, or both types of service requests. The service requests, C IM INT and C DEF INT, can be issued by the contact interrupt and I/O counter modules. Either request, if the corresponding SCAN EN bit is set, will cause the corresponding BUSY flip-flop to be set and the scanner to start its scan. The R IM or DEF INT H signal resets the scanner and starts the clock (Figure 3-5). Although the logic may be enabled to handle one, the other, or both types of service requests, the scan is started only if no programmed I/O is taking place. A programmed I/O is taking place if UDC EN L is low. This signal inhibits AND gates A and B (Figure 3-4) preventing the BUSY flip-flops from being set. The BUSY flip-flop will be set and the DONE flip-flop will be reset for the duration of the scan. The STP CLK, applied to the negative input OR gate (C), will go low when the scanner stops. This causes a fifth flip-flop, the SCAN DONE flip-flop, to be reset. Depending on the type of request issued, the immediate or deferred BUSY flip-flop will be reset and the DONE flip-flop will be set when the scanner stops. The BUSY DONE L (IM and DEF) signal is used in generating the SCAN START signal (gates A and B) to prevent the scanner from being reset during a programmed I/O (Figure 3-5) after the scanner is started. After the scanner stops, two approaches for operating on the service request are available to the programmer:

1. With the appropriate INT EN bit reset, the program can test the DONE bit to determine when the scanner has found the address.
2. If the appropriate INT EN bit is set, the UDC11 will automatically issue the corresponding bus request.

   BR4 for deferred
   BR6 for immediate

In either case a test for immediate and deferred must be made and the data from the module that issued the request may be read. The test must be made since only one interrupt vector is used. If the data is read without RIF bit 00 of the UDCR set, then the DONE flip-flop of the service request arbitration and scan control logic and the module service request flag will remain set. The scanner will then remain locked on the scanned address if it was an immediate scan or if it was a deferred scan with the immediate scan disabled or no immediate request came in during the scan. This feature is helpful where the user program may wish to operate on one bit at a time or make several readings of the data word and reset the module request flag only when all bits have been operated on or all readings have been accomplished. However, if the data is read with the RIF bit set (C RIF L, applied to negative input OR gate B, goes low), then both the DONE flip-flop and the module service request flag will be reset. Another option available to the programmer is to read the data without the RIF bit set and then reset both INT EN bits and again set one, the other, or both INT EN bits. This causes the DONE flip-flops to be reset while the module service request flag remains set. A new scan will then commence.

The DEF INVALID H signal (bit 15 of the UDSR) goes high whenever a deferred scan is done and an immediate scan starts. This bit will remain set until the DONE flip-flops (IM and DEF) are reset by reading the immediate data with the RIF bit of the UDCR set or by resetting and setting the INT EN bits of the UDCR.

3.5.2 I/O Module Address and Scanner Logic

A simplified logic diagram of the I/O module address and scanner logic is shown in Figure 3-5.

A functional I/O module can be addressed under program control (programmed I/O) or under control of the scanner in response to a service request. The programmed I/O will always take precedence over a service request address scan. The Unibus address lines (Bus A ⟨08:01⟩) and the scanner address lines (S ADDR ⟨07:00⟩) are gated through a set of eight 2-input AND/OR gates (A) to the DD02 File Units. The DD02 File Units contain two binary-to-octal converters and one 2-bit decoder. Jumpers are installed in the output lines of the two binary-to-octal decoders to establish a unique X and Y octal code for a specific file unit and its four I/O modules. This then, allows each module in a given file unit to be addressed with a specific 8-bit address by a programmed I/O or by the scanner. The Unibus address lines are gated to the DD02 File Units whenever a programmed I/O to a functional module takes place. During the programmed I/O, the PROG I/O EN H signal applied to the set of eight gates (A) is high (Figure 3-2). The scanner address is gated to the DD02 File Units when a scan is started (IM or DEF SCAN BUSY (1) L is high) and no I/O module programmed I/O is taking place (UDC EN L is high). The scanner address is also gated to the DD02 File Units while the UDCR, UDSR, or the MCLK locations are addressed for programmed I/O operations. This feature allows the scanner to start its scan even though one of the specified locations is being addressed by the program.

The scanner consists of three binary up-counters. These counters are clocked in a unique fashion to search (scan) for the module requesting service. Two 3-bit counters are used to search for the X and Y code (established by jumpers on the DD02 File Unit) and one 2-bit counter is used to search for the WD (word) number (module within the file unit). All modules capable of issuing service requests contain stop logic for controlling the counter clock. The stop logic, if enabled by the appropriate SCAN EN bit (IM or DEF) of the UDCR, stops the counters as the module requesting service sees a match in the X, Y, and WD address code in sequence. This scanning technique results in a maximum scan time of 17 μs (1 μs per count, that is, 7 + 7 + 3). Before the clock starts advancing the counters, all counters are reset by the SCAN START signal. This signal is produced when:

1. The UDC11 is initialized.
2. A module issues a service request (IM or DEF) while the scanner is inactive (associated BUSY and DONE flip-flops, Figure 3-4, are reset) with the appropriate SCAN EN bit set. If a programmed I/O is taking place (UDC EN H is high) at the time the request is issued, then the scanner is reset when the programmed I/O terminates. AND gates B1 and B2 of Figure 3-5 in conjunction with the AND gates shown in Figure 3-4 establish these conditions.

At the same time the counters are reset, the 1-MHz clock is activated (see gates C1 and C2, Figure 3-5). AND gates D1 through D3 produce the CLK X, CLK Y, and CLK WD in sequence because the stop logic on the module issuing the request will inhibit these gates as each X, Y, and WD component of the module address is matched by the scanner. The scanner can also be clocked by addressing the M CLK location (771772_8). Each time this location is addressed (using TST instruction for example) the M CLK H signal goes high causing one clock pulse. The M STP X, M STP Y, and M STP WD of the UDCR can be set under program control to stop each counter at the desired count.

For example, if the M CLK location is addressed five consecutive times and then the M STP X bit of the UDCR is set, the X counter stops at the count of five (101). Addressing M CLK again will then cause the Y counter to advance. This feature is strictly a maintenance tool and should not be used in application programming.

Another maintenance feature is available through the M MODE bit of the UDCR. Setting this bit with the INT EN bit (IM or DEF) set causes a corresponding service request to be issued. See gates E1 and E2, Figure 3-5. Forcing a service request in this way causes the scanner to overflow if no module service request comes in to enable the stop logic.

The overflow logic is not shown in Figure 3-5. Refer to drawing D-BS-DD01-D-02, sheets 1 and 2 in Volume II for details of the overflow logic. If the scanner overflows, the SCAN ERROR bit of the UDCR will be set and the UDSR will be set to 377_8 (see gate F in Figure 3-5). The UDCR can be tested directly, after the UDSR is read, to determine whether the scanner overflowed or power failed. Bits 14 and 15 of the UDCR are the POWER FAIL and the SCAN ERROR bits, respectively. A power failure in the UDC11 will also cause the scanner to be set to 377_8 but will cause the POWER FAIL bit of the UDCR to be set.

3.5.3 Interrupt Control

Figure 3-6 illustrates the interrupt control module (M782). All of the interrupt control logic is contained in this module. The interrupt control logic allows the UDCR to request and gain access to the Unibus on a priority basis. There are only two conditions for which the UDC11 may require the use of the Unibus: in the event of a failure (POWER FAIL or SCAN ERROR bits of UDCR are set), or when the scanner has found a module requesting service (IM or DEF SCAN DONE bit of UDCR is set).

The UDC11 can request use of the Unibus at priority level 6 (bus request 6) or at priority level 4 (bus request 4). The deferred scan done is assigned priority level 4 and the immediate scan done, scan error, and power fail are assigned priority level 6. The jumper card, G736, can be changed to assign a different priority level (4 through 7) to the immediate bus request. Caution must be exercised if a change is desired. Before the interrupt control can request use of the Unibus, one or both of the following UDCR bits must be set to enable the interrupt control logic.

DEF INT EN – bit 01
IM INT EN – bit 02

After a BR4 or a BR6 is issued by the interrupt control, priority permitting, the processor relinquishes the Unibus to the UDC11 by issuing a bus grant (BG) signal. In response to the bus grant signal (BG4 or BG6), the interrupt control issues an interrupt command (INTR) and a vector address that points to the location pair in memory that contains the address and status of the UDC11 I/O handler.

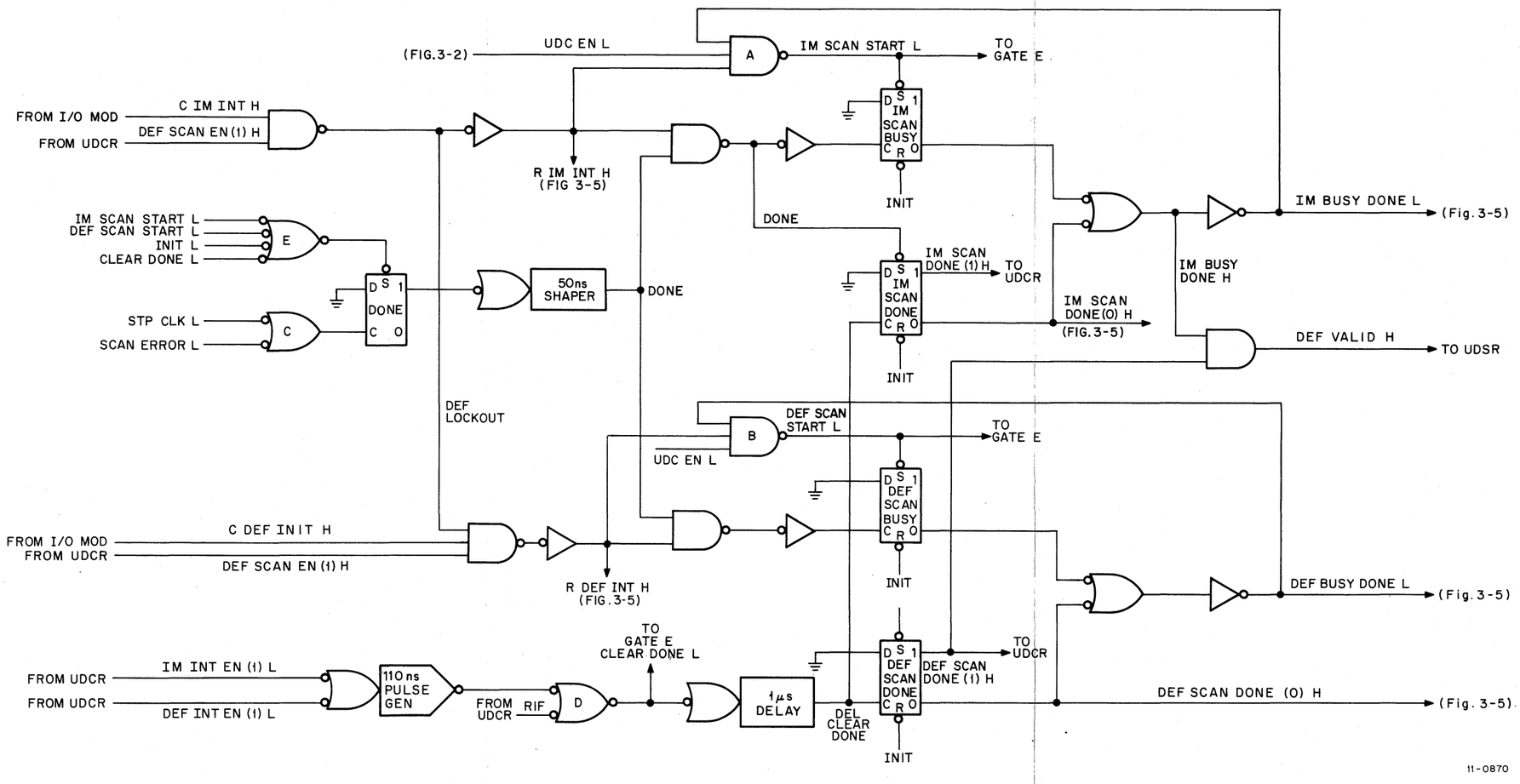


Figure 3-4 Arbitration and Scan Control Logic

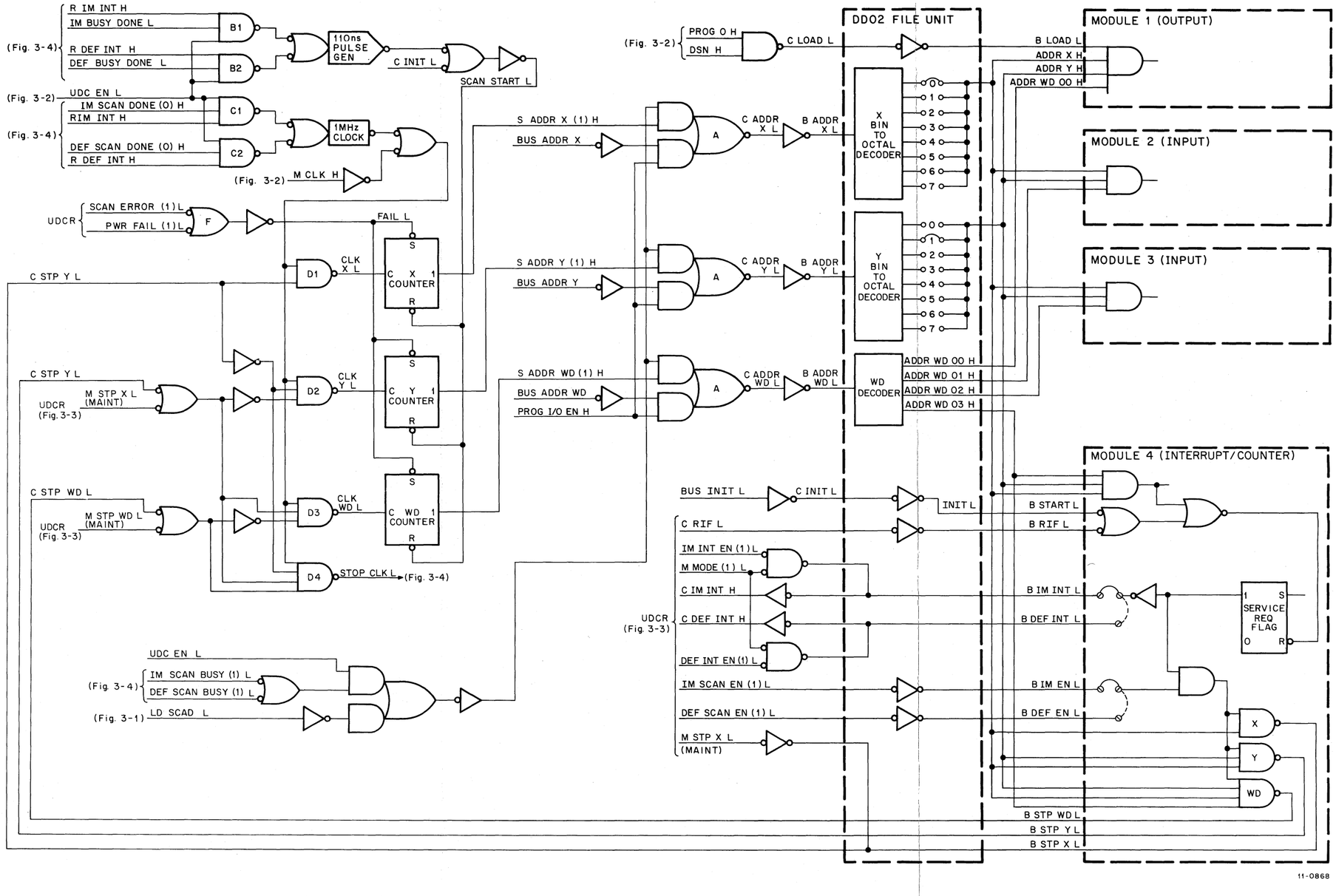


Figure 3-5 Address Scanner

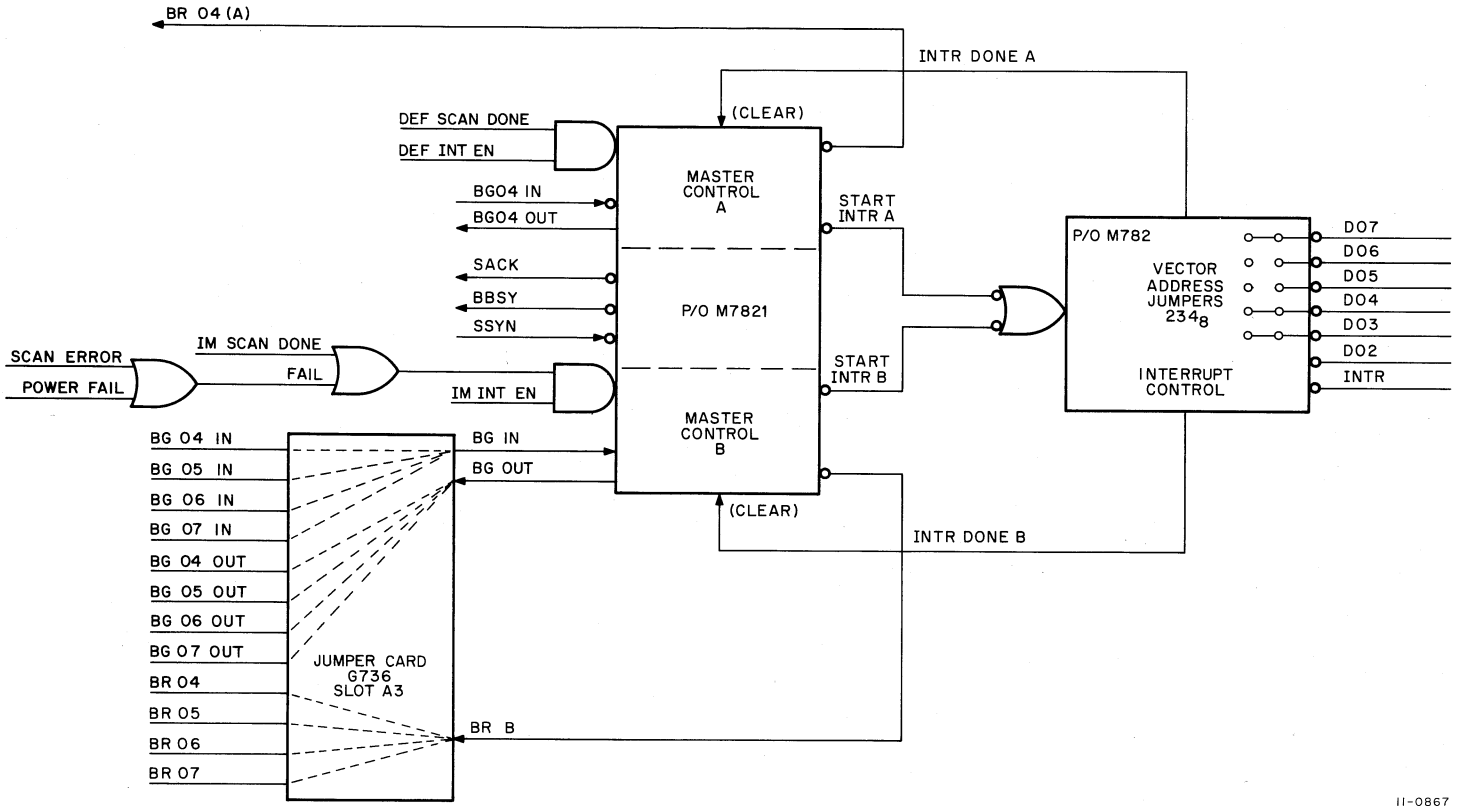


Figure 3-6 Bus Request Logic

CHAPTER 4
INSTALLATION

This chapter contains necessary installation information for UDC systems. The chapter covers the following subjects:

- Site Preparation
- Power Requirements, AC, Fusing, Receptacles
- Installation Checkout, DEC Field Service
- UDC System Configuration, Addressing, I/O Module Placement
- Functional I/O Module Setup
- Signal Conditioning (including Arc Suppression)
- Field Wiring

4.1 SITE PREPARATION

Adequate site planning and preparation can simplify the installation process and result in an efficient, reliable UDC system installation. The customer's planning staff should prepare a list of the actual components to be used in the installation. This list should include such items as tape-storage cabinets, work tables and desks, and any other items pertinent to the customer's computer applications. In selecting the site for the installation, consideration should be given not only to the physical dimensions of the units comprising the system, but also to service and operating space requirements and future expansion. The usefulness of a given area depends on many factors, such as length-width ratio, location of columns, and position of doors, windows, and electrical outlets, so that truly usable area need be distinguished from that which only appears to be usable. Scale drawings of the possible site locations should be prepared and consideration given to factors such as size of entrances into site area (they should be large enough to allow entry of the largest unit of the system), proximity to large inductive machines, and circuit availability of adjacent working area (enough room should be allowed to accommodate the equipment, required personnel, storage facilities, and service area).

While operating, the system can produce anywhere from 5,000 to 50,000 Btus of heat per hour (depending on the size) which must be dissipated. While individual units of the system are cooled by blowers and the equipment is designed to operate over a wide temperature range, it is recommended that air conditioning be installed to ensure reliable long-term operation. An air-conditioned area has the additional advantage of having a positive pressure with respect to the outside area which materially aids in maintaining a dust and dirt free environment. The atmosphere in the immediate vicinity of the equipment should be maintained as free from offensive dust and corrosive air as possible.

An average illumination of about 40 foot-candles measured 30 in. above the floor should be available in the area. Direct sunlight should be avoided since lower levels of illumination are needed to observe the various indicator lights on the control panels and operator consoles.

4.1.1 Space Requirements

Space requirements are determined by the specific system configuration to be installed, and, when applicable, provision for future expansion. To determine the exact area required for a specific configuration, a machine-room floor plan layout is helpful. When applicable, space is provided in the machine room for storage of tape reels, printer forms, card files, system documentation, etc. The integration of the work area with the storage area depends on the work-flow requirement between areas.

In large installations where test equipment is maintained, DEC recommends that the test equipment storage area be within or adjacent to the machine room. Figure 4-1 shows the space requirements for maximum and minimum UDC11 configurations. This does not include the computer cabinet or other peripheral devices.

4.1.2 Environmental Conditions

An ideal computer room environment has an air distribution system that provides cool, well-filtered, humidified air. The room air pressure should be kept higher than the pressure of adjacent areas to prevent dust infiltration.

4.1.2.1 Humidity and Temperature — The UDC is designed to operate in a temperature range of from 50°F (10°C) to 110°F (43°C) at a relative humidity of 20 to 90 percent with no condensation. However, typical system configurations using input/output devices such as magnetic tape units, card readers, etc., require an operational temperature range between 65°F (18°C) and 80°F (27.5°C) with 40 to 55 percent relative humidity. Nominal operating conditions for a typical system are a temperature of 70°F (21°C) with a noncondensation relative humidity of 45 percent.

4.1.2.2 Cleanliness — The following precautions are recommended by DEC to ensure optimum UDC system operation:

1. Do not use steel wool for cleaning floors in the computer room.
2. To prevent air flow interference, do not place material on top of the cabinets.
3. Use a nonconductor type nozzle when vacuuming to minimize the possibility of an electrical accident.
4. Avoid spilling liquids (coffee, soda, etc.) on the equipment and operating controls (e.g., console switches, Teletype® keys and controls).

4.1.2.3 Static Electricity — Static electricity can be an annoyance to operating personnel and can (in extreme cases) affect the operational characteristics of the UDC system and related peripheral equipments. If carpeting is installed on the installation room floor, it should be of a type designed to minimize the effects of static electricity. Flooring consisting of metal panels, or flooring with metal edges, should be adequately grounded.

4.2 POWER REQUIREMENTS

The following information pertains specifically to UDC11 subsystems. For detailed information regarding PDP-11 power requirements including options refer to the PDP-11 Handbooks.

UDC systems are sold in a variety of H964 cabinet configurations. Each cabinet contains a power control (849A) and a power supply (H740D) for each file implemented. The H740D Power Supply is capable of supplying +5V @ 17A. The H738A Power Supply is optional and is available for implementing the A633 DAC's.

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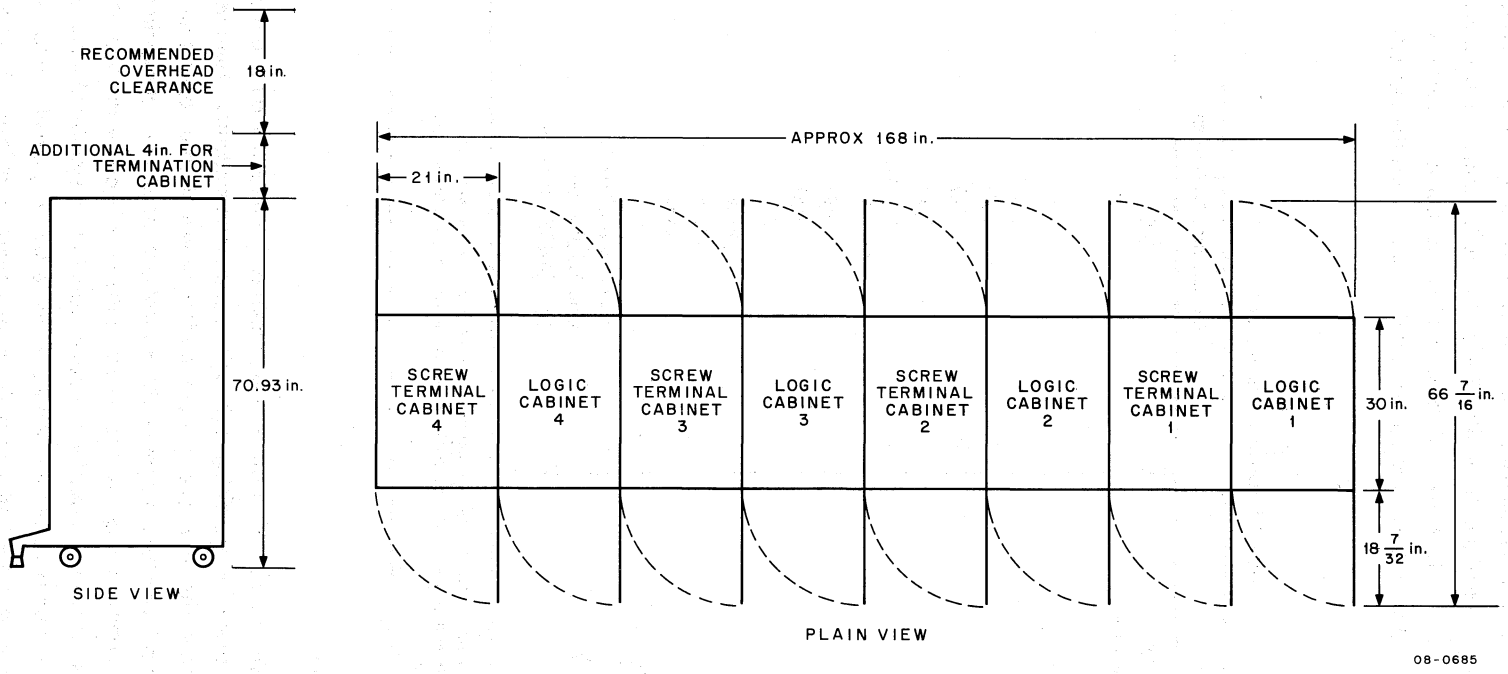


Figure 4-1 Space Requirements for UDC11

4.2.1 Logic Power

The internal control and logic power requirements for each logic cabinet are directly dependent on the number and type of functional modules installed in that cabinet. One H740D Power Supply is provided for each file implemented in a cabinet. As previously described, the H740D Power Supply has a maximum current capacity of 17A. The power requirements for the functional parts of the UDC11 are as shown in Table 4-1. The power consumption for the total number of modules implemented in a file should not exceed the capacity of the H740D Power Supply.

Table 4-1
UDC11 Power Requirements

Item	Consumption (Amps)
Master File	3.0
Expander File	.3
DD02	.3
W731	.200
W733	.650
W741	.300
W743	.450
M685	* .350
M687	* .500
M803	* .350
M805	* .350
M807	* .500
W734	1.0
W400	none
W402	none
W403	none
A633, A233, A234, A235, A236	Power supplied by one H738A per four A633 Modules

*This value assumes that 8 of the 16 circuits on the module are energized. The power requirements are directly proportional to the number of circuits energized at one time.

4.2.2 Primary Power Requirements

Each logic cabinet requires a 30/15A (115/230V) primary power source. Both local and remote control are provided. Local control provides the means for energizing each logic cabinet independently. Remote control is chained from one cabinet to the other; the entire system can therefore be energized by operating the power switch on the computer console. Each cabinet contains all the control circuits and power supplies to establish the type of control desired, and to convert the primary ac power to the dc voltages required by the logic cabinet. Protection for overvoltage and overcurrent is included in the power supplies. A simplified block diagram illustrating the distribution of the power within a cabinet is shown in Figure 4-2. For detailed information concerning distribution and control of ac and dc power, refer to engineering drawings provided in Volume II of this manual.

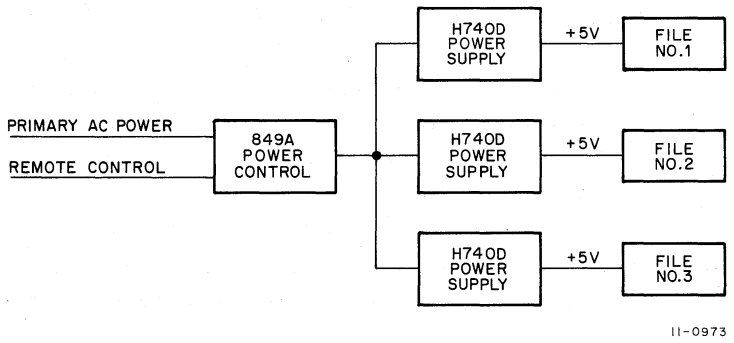


Figure 4-2 UDC11 Logic Cabinet Power Distribution Block Diagram

4.2.3 Primary Power Receptacles

The installation site primary power line must terminate in Hubbell wall receptacles (or equivalent) to be compatible with the UDC11 system power line connector. The Hubbell wall receptacle part numbers are shown in Table 4-2.

Table 4-2
Hubbell Wall Receptacle Part Numbers

Line Voltage	Hubbell Receptacle Part Numbers
115 Vac, 60 Hz, 30A	Receptacle 3330-G (3330 may be used) Cap 3331-G (3331 may be used)
230 Vac, 50 Hz, 20A	Receptacle 7310-G (7310 may be used) Cap 3321-G (3321 may be used)

4.3 INSTALLATION CHECKOUT

4.3.1 Unpacking and Visual Inspection

After unpacking of equipment a visual inspection should be made to ensure against loose modules and connections. An inventory should be performed at this time to ensure all equipment and supporting documentation is present. (Refer to Accessory List.)

4.3.2 I/O Bus Connections

One BC11A Cable is required to connect the PDP-11 Unibus to the UDC11 from the computer or some other peripheral device. This cable is inserted in slot AB01 of the DD01-D Interface Controller. Slot AB02 may require an M930 Termination Module if the UDC11 is the last peripheral on the Unibus. If not, this slot will contain another BC11A Cable to extend the Unibus to the next peripheral device.

4.3.3 UDC Bus and Connections

The UDC bus consists of 60 lines, 31 driven by open collector-drivers at the DD01-D Master Control and 29 driven by open collectors on I/O modules. Bus receivers on M784 Modules in the DD01-D and on the M851 in each DD02 allow the full complement of functional modules to share the bus lines. Special double connector

modules (M935), a set of flat Mylar® cables, and a set of power cables are required to extend the UDC bus and power throughout the UDC. The UDC bus is chained from one DD02 to another within a file with the M935 Bus Connectors. This module connects the bus lines of slot AB14 in the DD01-D to AB01 of the first DD02 File Unit and slot AB04 is connected by an M935 to AB01 of the next DD02. One more DD02 may be thus connected in the first file. Further extension of the UDC bus is accomplished by connecting from the AB04 of the last DD02 in the file to AB01 of the first DD02 in the next file, using a 5-ft flat Mylar (BC41A-5) cable. A 10-ft flat Mylar (BC41A-10) is used to extend the bus between DD02s in different cabinets. Two terminating modules (M942) are also required to construct the UDC bus. These modules must be inserted in slot AB11 of the DD01-D and in slot AB04 of the last DD02 on the bus. If no DD02 File Units are used, the second M942 Module is used in slot AB14 of the DD01-D.

4.3.4 External Cabling

The BC40C Screw Terminal Assembly is the point at which customer control circuits connect to the UDC11 Signal-Conditioning Modules. Each circuit is completed through a twisted pair of No. 26 AWG stranded, color-coded wire connected to a pair of screw terminals. The terminals will accommodate No. 14 AWG wire, and are arranged in two strips of 17 contacts, each supported in line by a common steel angle support. The steel supports are mounted, one above the other, 36 in front and 36 at the rear of the dedicated cabinet. In the single file, single cabinet configuration, the screw terminals are mounted 12 front, 12 rear. The field wiring may enter only from the top or bottom of the cabinet. Field wiring should be twisted pairs per control point. Maximum current per point is 2A, limited by relay contact ratings; large wire is thus unnecessary. The twisted-pair field wiring is used to avoid stray pickups and to minimize the radiation of switching transients by confining their fields largely to the space between the two wires of the twisted pair.

Horizontal bars, located at the top and bottom of the screw terminal cabinet, are to be used for strain relief on incoming cables. In addition, strain-relief members are located at both ends of the screw terminal brackets. The input cables should be routed over these members to provide for strain relief as they branch out to individual screw terminals. As the cables enter the screw terminal cabinet, they should be routed over the strain-relief bar and up/down both sides of the cabinet.

4.3.5 Electrical ac Power Cabling

The 849A power controller supplies ac power to the UDC. The 849A power controller can operate in two modes, remote and local. In the remote mode, an ac power cable is required between the central processor, controlled ac power outlet, and the 849A control socket. This provides ac power to control the circuit breaker when the central processor is turned on and off. In the local mode, the circuit breaker is controlled manually at the front of the 849A.

The ac power for the UDC is normally 115 Vac, 60 Hz, single-phase (220 Vac, 50 Hz, single-phase) three wire. Power for the UDC should be supplied from the same source as is the central processor.

Before connecting ac power to the UDC, measurements should be made at the Hubbell wall receptacles between ac hot and ground, ac neutral and ground, and ac hot and ac neutral to ensure that proper power is available. After determining that proper power is available, make sure the 849A LOCAL/REMOTE switch is in LOCAL and the circuit breaker is off. Plug the 849A ac power cable in and measure the voltage between the cabinet and ac power ground, this measurement should be 0V. Energize the 849A by switching the circuit breaker on and again make the measurement from cabinet to ground, again 0V should be read.

®Mylar is a registered trademark of E. I. DuPont de Nemours and Company.

If the system has more than one UDC logic bay, each 849A power controller (one per logic bay) will have to be connected and checked individually.

NOTE

If the checks of power outlined above show any discrepancies, these problems must be corrected before proceeding. A SHOCK HAZARD may exist.

4.3.6 dc Voltage Checks

Two types of dc power supplies can be used in the UDC system. The H740D Power Supply is used to supply file logic power. One H740D Power Supply is supplied for each file implemented. The H738A Power Supply is used in UDCs containing D to A options (A633) only.

Check the dc output voltage of each H740D Power Supply by measuring the tabs on the right-hand most G729 (+ tab on top, gnd tab on the bottom) in each UDC file. This measurement ensures that +5 Vdc is supplied to all logic and I/O modules in the UDC.

Check the dc voltages supplied by the H738A to the D to A option for +18V, -18V, and +5V at the screw terminals. The screw terminals that are connected to D to A options are the only terminals that are prewired on the screw side.

4.3.7 UDC Functional Checkout

Using the UDC Acceptance Procedure (A-SP-UDC11-0-4) supplied with the documentation, the UDC Exerciser Program (MainDEC-11-D8JA-B), and the UDC Field Test Box proceed to check the functional I/O modules. The UDC Acceptance Procedure details specific steps and procedures used in checking the various functional I/O modules utilizing the test box and the Exerciser Program.

4.3.8 System Pre-Use Requirements

After the system has been connected and checked out as described in Paragraphs 4.3.1 through 4.3.7, there remain steps the customer must perform before putting the UDC into operation:

1. Signal conditioning (Arc Suppression) for output functional I/O modules. Refer to Paragraph 4.6.
2. Field cable connections to the UDC screw terminals.
3. Determination of any special addressing of functional I/O modules that require changing the G729 Address Selection Modules.

4.3.9 UDC Add On Expansion

The UDC can be expanded in four ways:

1. Addition of more functional I/O modules.
2. Addition of DD02s system units.
3. Addition of UDC8-X system files.
4. Addition of other UDC bays.

The latter presumes inclusion of the preceding items.

The additions as they occur will require the following considerations.

1. The addition of I/O functional modules will require an available I/O slot, adequate power from the H740D Power Supply, and mounting of the screw terminals. After the added modules are installed functional checkout is accomplished using items described in Paragraph 4.3.7 for those added modules.

2. The addition of other DD02 system units requires adequate mounting space in the BF01 file, power cabling, and the UDC bus continuation with an M935 from the preceding DD02. Before adding I/O modules, a check of (1) above should be made.
3. Addition of other UDC8-X system files requires adequate space in the cabinet, power cabling and continuation of UDC bus via a BC41A cable.
4. Addition of other UDC bays should be treated as described in Paragraphs 4.3.1 to 4.3.7.

4.4 UDC SYSTEM CONFIGURATION

Configuration of UDC systems is a user task and each system can be set up for optimum performance. In configuring a system, the user should consider the requirements in terms of functional areas. The UDC is basically a digital multiplexer with the added availability of identifying user interrupts. Thus, functionally the UDC can perform the following:

a. Bi-Level Interrupt Identification
   1. Immediate
   2. Deferred
b. Status or State of Operation
c. Control

4.4.1 Bi-Level Interrupt Identification

The UDC control logic contains a hardware scanning feature to search for the address of any interrupting module. Upon recognition of a UDC interrupt, the hardware scanner will sequentially search the UDC address compliment and produce a processor interrupt upon completion of the search. Table 4-3 defines the priorities of all module addresses. The bi-level UDC interrupt structure is useful in that the system programmer can choose two classes of interrupts, those requiring immediate program action and a deferred mode where program action can be performed at a later time.

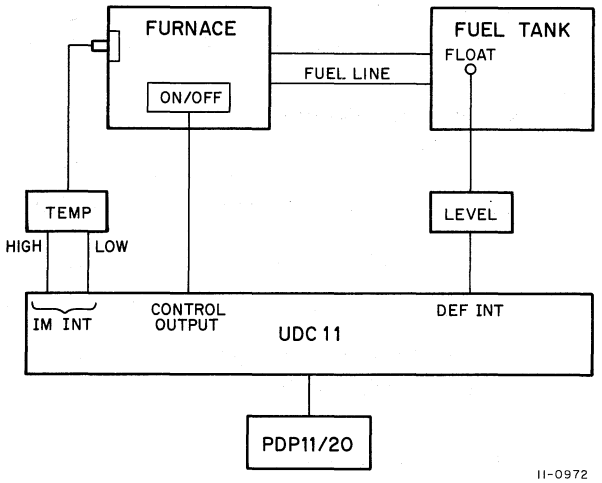


Figure 4-3 Interrupt Class Example

The simple example of a temperature monitoring process illustrated in Figure 4-3 shows this concept more readily.

In this example the furnace has a control unit which will provide ignition or shut down, a temperature sensing element which will provide an interrupt at a preset temperature, and a fuel supply which contains a float switch to indicate low fuel. If furnace temperature is too high or too low, the UDC should be interrupted immediately and turn the furnace off or on depending on the interrupt received. However, the float switch is only an indicator of low fuel supply and this interrupt can be recognized at a later time and thus is placed on the deferred line.

4.4.1.1 Module Interrupt Selection – Each interrupt UDC module can be placed in either immediate or deferred mode. This is accomplished by the proper selection of jumpers on the module and will be covered in Paragraph 4.5, Functional I/O Modules.

Table 4-3
Scanner Counting Characteristics

Address Jumpers		Address Scanner Count (1 μsec per count)																	
X	Y	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
0	0	0	1	2	3												MODULE NUMBERS		
0	1		4	5	6	7													
0	2			8	9	10	11												
0	3				12	13	14	15											
0	4					16	17	18	19										
0	5						20	21	22	23									
0	6							24	25	26	27								
0	7								28	29	30	31							
1	0		32	33	34	35											MODULE NUMBERS		
1	1			36	37	38	39												
1	2				40	41	42	43											
1	3					44	45	46	47										
1	4						48	49	50	51									
1	5							52	53	54	55								
1	6								56	57	58	59							
1	7									60	61	62	63						
2	0			64	65	66	67										MODULE NUMBERS		
2	1				68	69	70	71											
2	2					72	73	74	75										
2	3						76	77	78	79									
2	4							80	81	82	83								
2	5								84	85	86	87							
2	6									88	89	90	91						
2	7										92	93	94	95					
3	0				96	97	98	99									MODULE NUMBERS		
3	1					100	101	102	103										
3	2						104	105	106	107									
3	3							108	109	110	111								
3	4								112	113	114	115							
3	5									116	117	118	119						
3	6										120	121	122	123					
3	7											124	125	126	127				
4	0					128	129	130	131								MODULE NUMBERS		
4	1						132	133	134	135									
4	2							136	137	138	139								
4	3								140	141	142	143							
4	4									144	145	146	147						
4	5										148	149	150	151					
4	6											152	153	154	155				
4	7												156	157	158	159			
5	0						160	161	162	163							MODULE NUMBERS		
5	1							164	165	166	167								
5	2								168	169	170	171							
5	3									172	173	174	175						
5	4										176	177	178	179					
5	5											180	181	182	183				
5	6												184	185	186	187			
5	7													188	189	190	191		
6	0							192	193	194	195						MODULE NUMBERS		
6	1								196	197	198	199							
6	2									200	201	202	203						
6	3										204	205	206	207					
6	4											208	209	210	211				
6	5												212	213	214	215			
6	6													216	217	218	219		
6	7														220	221	222	223	
7	0								224	225	226	227					MODULE NUMBERS		
7	1									228	229	230	231						
7	2										232	233	234	235					
7	3											236	237	238	239				
7	4												240	241	242	243			
7	5													244	245	246	247		
7	6														248	249	250	251	

4.4.2 System Interrupt Response

The system interrupt response is defined as:

MODULE OPERATE TIME + SCAN TIME + PDP-11 INTERRUPT LATENCY TIME + PROGRAM TIME.

a. Module Operate Time

W733 Relay Input Contact Interrupt — 2 ms
W743 Solid State Input Contact Interrupt — 2.5 ms (50 μs with hi-speed option)
W734 I/O Counter — Int on Overflow

b. Scan Time

Table 4-3 will give the search time for each UDC address.

c. PDP-11 Interrupt Latency Time

This time will depend entirely on the system configuration and the status of the system at the time of the UDC interrupt. For a complete discussion of PDP-11 interrupt latency time, see the *PDP-11/20/15/r20 Processor Handbook,* Chapter 2, Paragraph 2.5 Automatic Priority Interrupts.

d. Program Time

Program time can be computed from the service routine being used and information regarding processor cycle time, which is available in the *PDP-11/20/15/r20 Processor Handbook.*

It should be noted that although the operate time of the input modules is quite long, interrupts can be waiting for service due to the receipt of two or more at the same time. Thus, the need for a fast search time and processor service time is evident.

4.4.3 Generic Codes

Each UDC interrupting module contains a 4-bit code that is present at the time the UDC module address is read. This code allows the user to determine what type module has caused the interrupt. The codes for each module are listed below:

Module	Generic Code	
W733	0010	Hardwired on Module
W743	0011	Hardwired on Module
W734	0100 0101 0110 0111	(Selectable on Module by jumper)

4.4.4 Status and Control

The remaining function of a UDC system is to obtain process status information and to provide control. These functions are provided by the remaining non-interrupting functional I/O modules. Placement of these modules is not critical and their location can be specified by convenience. However, it is advisable to segregate high voltage switching elements such as mercury-wetted relay outputs from D/A converter outputs (A633) if at all possible.

4.4.5 User Identification — Functional I/O Modules

After the system is configured and placement of functional I/O modules is complete, the user is encouraged to utilize the I/O module cross reference provided. The cross reference scheme includes a Functional Module I/O Chart (Figure 4-4) and a Functional Module I/O Page (Figure 4-5). The I/O chart is found on the back door of

each UDC electronics cabinet and contains space for information to identify each I/O module in the cabinet. The I/O chart also includes a column entitled Page No.; this column is used to reference the module listed in the I/O chart with detailed module descriptions contained on the Module I/O Page. Module I/O Pages are provided with each UDC system.

dec cab___ File___

WORD ADDR		FILE UNIT (JUMPERS)		WORD	SCREW TERMINAL			MODULE TYPE		PAGE NO.
DEC	OCTAL	X	Y	0-3	FILE	SLOT	TERM	I/O	SIG COND	
				0		S1	T1F			
				1		S2	T2F			
				2		S3	T3F			
				3		S4	T4F			
				0		S6	T5F			
				1		S7	T6F			
				2		S8	T7F			
				3		S9	T8F			
				0		S11	T9F			
				1		S12	T10F			
				2		S13	T11F			
				3		S14	T12F			
				0		S16	T1R			
				1		S17	T2R			
				2		S18	T3R			
				3		S19	T4R			
				0		S21	T5R			
				1		S22	T6R			
				2		S23	T7R			
				3		S24	T8R			
				0		S26	T9R			
				1		S27	T10R			
				2		S28	T11R			
				3		S29	T12R			

08-0686

Figure 4-4 Functional Module I/O Chart

4.4.6 Address Assignments

After a system is installed, addresses may be reassigned to the functional modules. This is accomplished by changing two jumpers (one in the X field and another in the Y field) on the address jumper modules (G729) of the address selectors (Figure 4-6). These jumpers define the first two digits of the addresses of the four module slots in the file unit.

These two digits are straight octal, and the pair may be considered to be the address of the file unit. The 8 x 8 matrix and accompanying diagram presented in Figure 4-7 illustrate this scheme.

The G729 Modules are piggy-back modules that mount on the M851 Address Decoder Modules of the file unit. By installing a jumper in the X field and a jumper in the Y field, the four functional modules that are housed in that file unit will each respond to a unique address 0, 2, 4, or 6 (Figure 4-7). To maintain configuration simplicity, it is recommended that addresses be assigned to the modules continuously from right to left and from top to bottom (viewing cabinet from rear), starting with channel No. 0.

If the channel numbers are re-assigned to the modules, the corresponding screw terminal strips must be relabeled with the word number. See Figure 4-8 for details on the numbering scheme for slots and screw terminals.

In addition, the channel identification chart on the back door of the logic cabinet must be filled in and an information page filled out as addresses are assigned, modules are inserted and customer devices are connected.

The UDC system final factory checkout will be made with address jumpers on G729 Modules installed in such a manner that addresses are sequential, starting with 000, 002, 004, and 006 in the DD01-D Control. Addresses will progress down the bus in order. Addresses may be changed by moving jumpers on G729 Modules, but care must be exercised to avoid duplicating X and Y pairs. The address, slot location, and screw terminal map should be used for cross reference and record-keeping.

The matrix shown in Figure 4-7 enables the user to determine the four addresses that belong to any X and Y combination.

PAGE NO.

MODULE TYPE:

SIGNAL CONDITION TYPE :

WORD ADDRESS		FILE UNIT		WORD NO.	MODULE LOCATION			FIELD WIRING			FIELD PWR.		CONTACT INTERRUPT		INTERRUPT ENABLE	
DECIMAL	OCTAL	X	Y		CAB	FILE	SLOT	FILE	SLOT	TERM	V	I	PULSE OPEN	PULSE CLOSE	IMMED	DEFERRED

GENERIC CODE

WORD NO.

BITS	ARC SUPPERSSION		TIMING S/S	ACTIVE CONTACTS (FORM A OR B)	BIT FUNCTION REMARKS
	RES	CAP			
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					

08-0675

Figure 4-5 Functional Module I/O Page

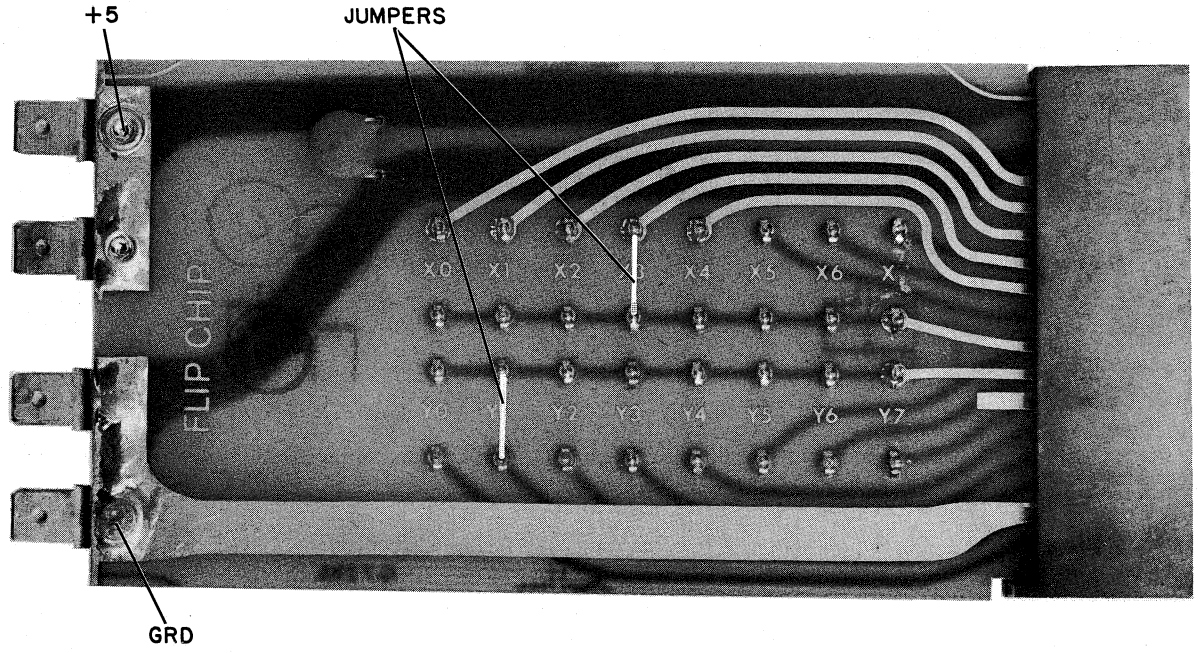
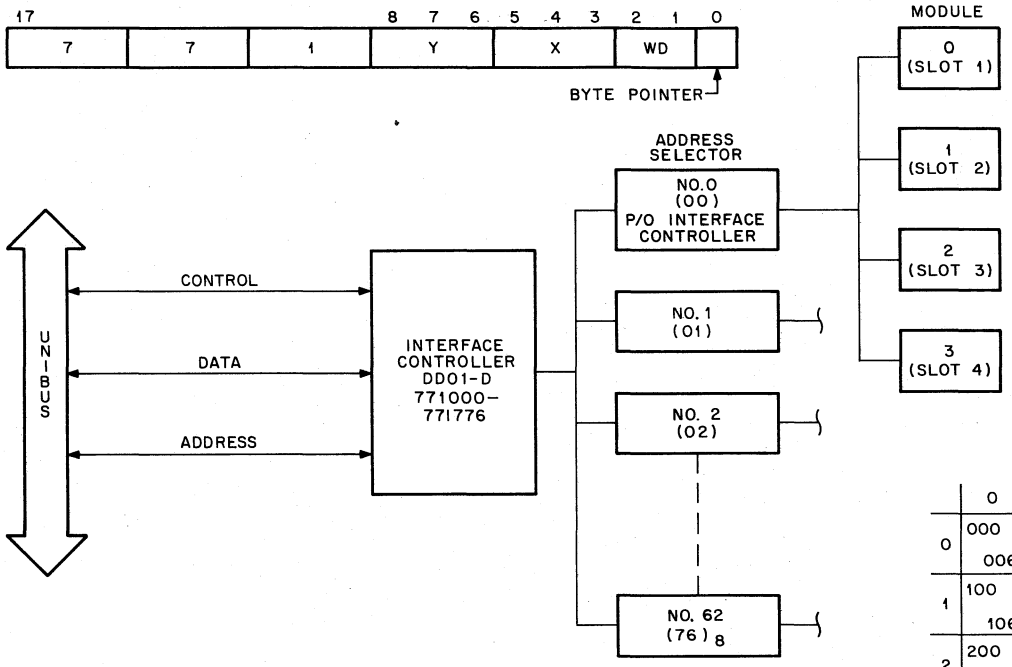


Figure 4-6 G729 Address Jumper Module



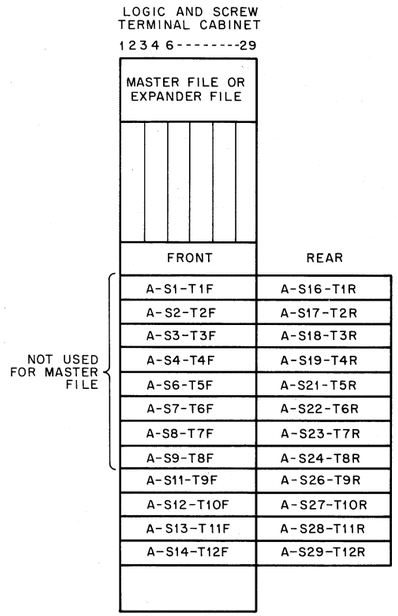
Y

X	0	1	2	3	4	5	6	7
0	000 006	010 016	020 026	030 036	040 046	050 056	060 066	070 076
1	100 106	110 116	120 126	130 136	140 146	150 156	160 166	170 176
2	200 206	210 216	220 226	230 236	240 246	250 256	260 266	270 276
3	300 306	310 316	320 326	330 336	340 346	350 356	360 366	370 376
4	400 406	410 416	420 426	430 436	440 446	450 456	460 466	470 476
5	500 506	510 516	520 526	530 536	540 546	550 556	560 566	570 576
6	600 606	610 616	620 626	630 636	640 646	650 656	660 666	670 676
7	700 706	710 716	720 726	730 736	740 746	750 756	760 766	

11-1018

Figure 4-7 Channel Address Scheme

SINGLE CABINET CONFIGURATION



DUAL CABINET CONFIGURATION

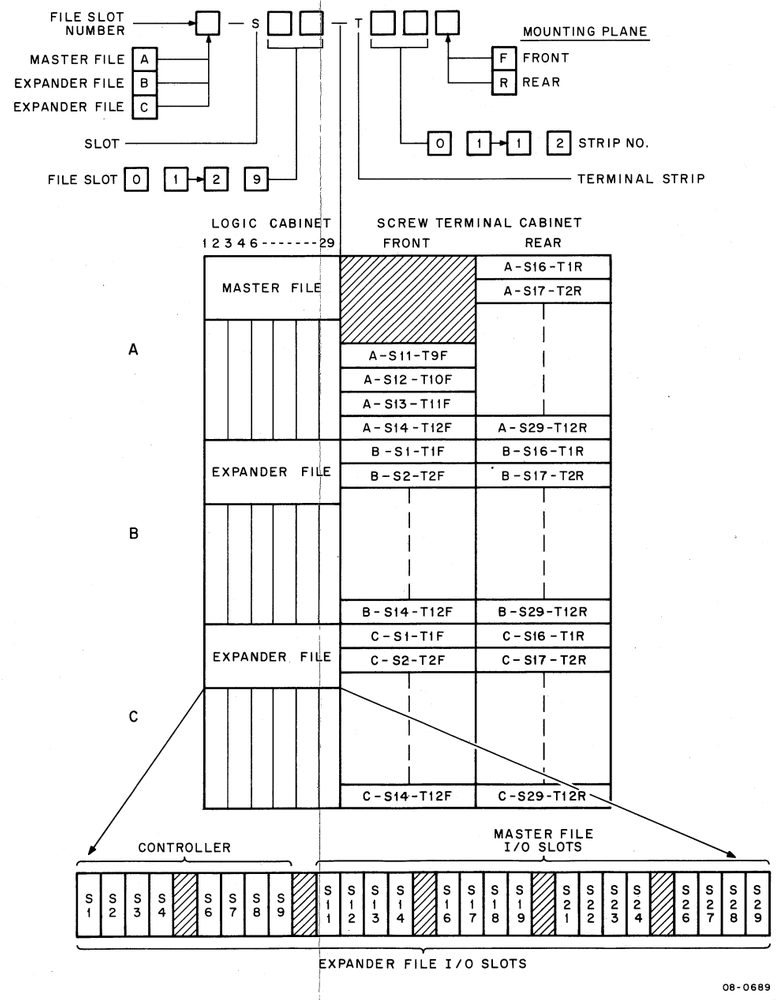
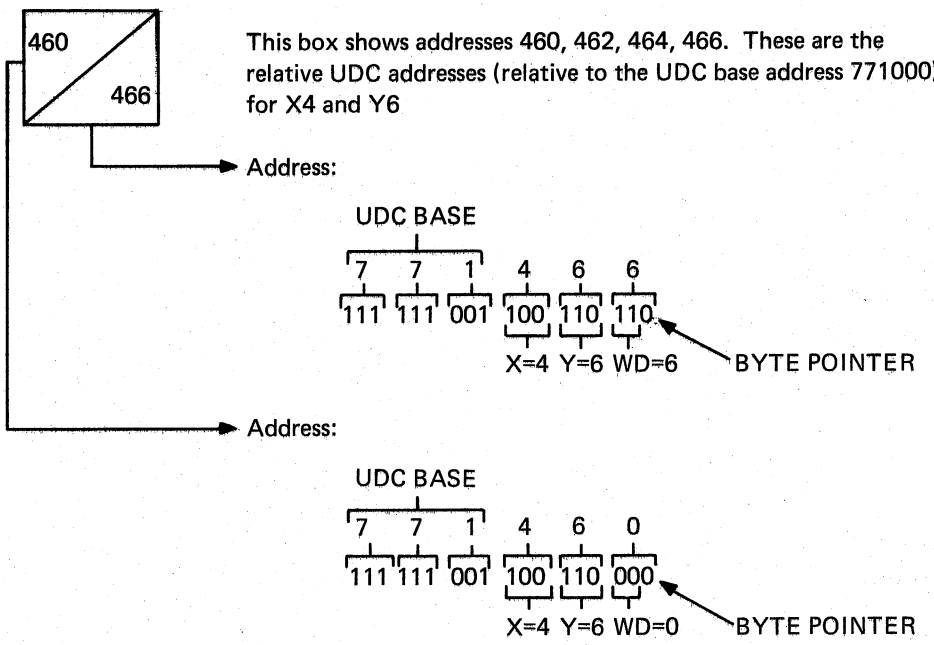


Figure 4-8 Slot and Screw Terminal Numbering Scheme

Example:

X = 4, Y = 6



4.5 FUNCTIONAL I/O MODULE SETUP

The following data sheets provide information on all UDC11 functional I/O modules. The user is advised to carefully read the data sheets on each module type in his system, and he should pay particular attention to the jumper configurations. The following I/O modules are discussed:

a.	Contact Sense (Relay)	W731
b.	Contact Interrupt (Relay)	W733
c.	Contact Sense (Solid State)	W741
d.	Contact Interrupt (Solid State)	W743
e.	Flip-Flop Driver	M685
f.	Single-Shot Driver	M687
g.	Latching Relay Output	M803
h.	Flip-Flop Relay Output	M805
i.	Single-Shot Relay Output	M807
j.	D/A Converter Output	A633
k.	I/O Counter	W734

NOTE

The functional I/O modules are universal modules, that is, they can be used with the PDP-8, PDP-15, and the PDP-11 UDC device. The bit numbering (placarding) on the modules reflects the numbering conventions used in the PDP-8 and PDP-15. However, the bit numbers associated with the callouts on the photographs in this section reflect the actual PDP-11 numbering convention.

W731
CONTACT SENSE RELAY INPUT MODULE

FUNCTIONAL SPECIFICATIONS

Power Requirements:	+5V @ 0.2A maximum
Input Response Time:	2 ms including Input Relay Bounce
Input Isolation:	$10^9 \Omega$ minimum, 250V
Input Voltage:	6V ± 5% @ 15 mA
Field to Logic Transfer:	0V at Input = Logic 0 DATAI
Signal Conditioning:	W400 or W402 required. Provisions for 24 or 48 Vdc operation are available.

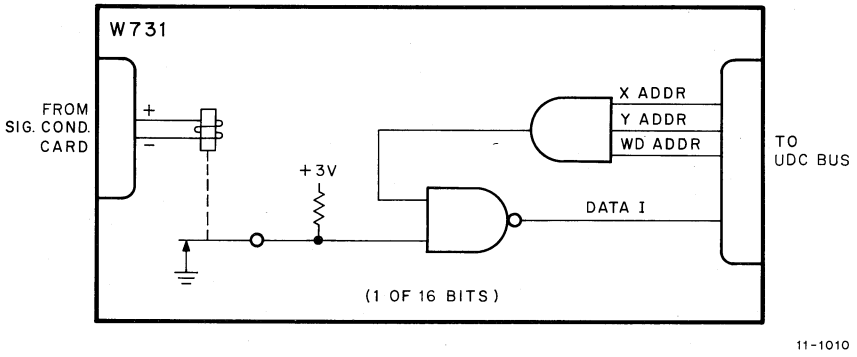


Figure 4-9 Simplified Schematic Diagram (W731)

DESCRIPTION

The W731 Contact Sense Module (Figure 4-9) contains 16 bits of contact sense logic. When addressed by the UDC, information concerning the state of the 16 relays is present at the DATAI gates. This data is the present condition of the 16 relays and can change at any time. It is not stored into any buffer; it is used for monitoring purposes.

W733
CONTACT INTERRUPT RELAY INPUT MODULE

FUNCTIONAL SPECIFICATIONS

Power Requirements:	+5V @ 0.5A maximum
Input Response Time:	1 ms maximum (Relay Bounce filtered)
Input Isolation:	$10^9 \Omega$ minimum, 250V
Input Voltage:	6V ± 5% @ 15 mA
Field to Logic Transfer:	Interrupt on Input Transition, 0V = Logic 0 DATAI
Signal Conditioning:	W400 or W402 required. Provisions for 24V or 48 Vdc operation are available.

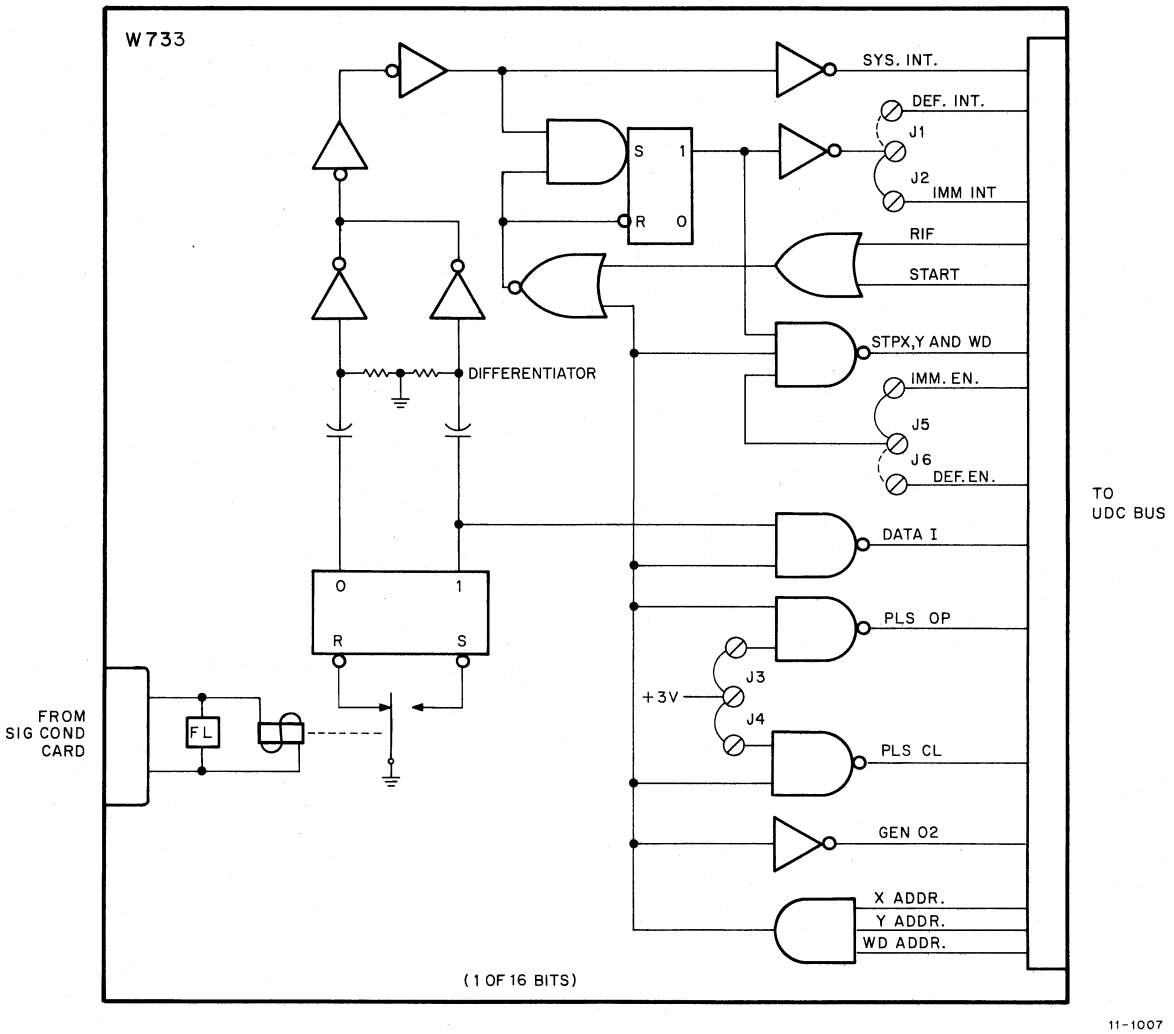


Figure 4-10 Simplified Schematic Diagram (W733)

DESCRIPTION

The W733 Contact Interrupt Module (Figure 4-10) provides electrically isolated, differential inputs for 16 external customer contacts or voltages. Isolation of up to 250V is achieved by a miniature reed relay buffer on each input point. This module provides reliable and troublefree digital sensing in high noise environments. Also, its differential input characteristics are particularly suited for those applications where the ground of the customer's excitation voltage power supply may be different from (i.e., not directly strapped to) computer system ground. However, excitation voltages of 24V or 48V may be used by jumper selection on the signal-conditioning module, which plugs into the W733 Module. The higher excitation voltages of 24V or 48V are recommended for contact wiping action to ensure reliability where field contacts are open, or subject to dust or oxide buildup.

The input circuits of W733 Module consists of 16 miniature Form C reed relay windings. The common contact of each relay is grounded. The N. O. (normally open) Form A contact is connected to the set input, and the N. C. (normally closed) Form B contact is connected to the reset input of an RS flip-flop. The consequence of current flow in the relay winding because of a field contact closure will be to switch ground from the N. C. contact to the N. O. contact of the input reed relay. This action causes the RS flip-flop to set. The bus driver inputs for each bit are provided by address enabling and the RS flip-flop output. Changing the DATAI bus signal to a true level generates a logic 1 on the UDC DATAI lines when the module is addressed.

The change in state of the flip-flop is differentiated, the resulting pulse is open-collector ORed to the System Interrupt Line. The pulse on this line is not used in UDC11 systems. Instead, the UDC11 uses the interrupt levels IMM INT and DEF INT to detect a change of state.

MODULE JUMPER CONFIGURATION

The jumpers on the W733 Module must be configured by the user to meet his application needs. The jumpers and their function are listed in Table 4-4 and are shown in Figure 4-11.

Table 4-4
Jumper Options (W733)

Function	Jumpers Required
IMM INT	J2, J5
DEF INT	J1, J6
PLS OP*	J3
PLS CL*	J4

*PLS OP and PLS CL are logic levels to be used in Software Routines as an aid in determining change of state information.

CUSTOMER INPUTS

Filtering is required for customer contacts when contact bounce duration is greater than the W733 input response time. Multiple interrupt will occur if contacts are not filtered.

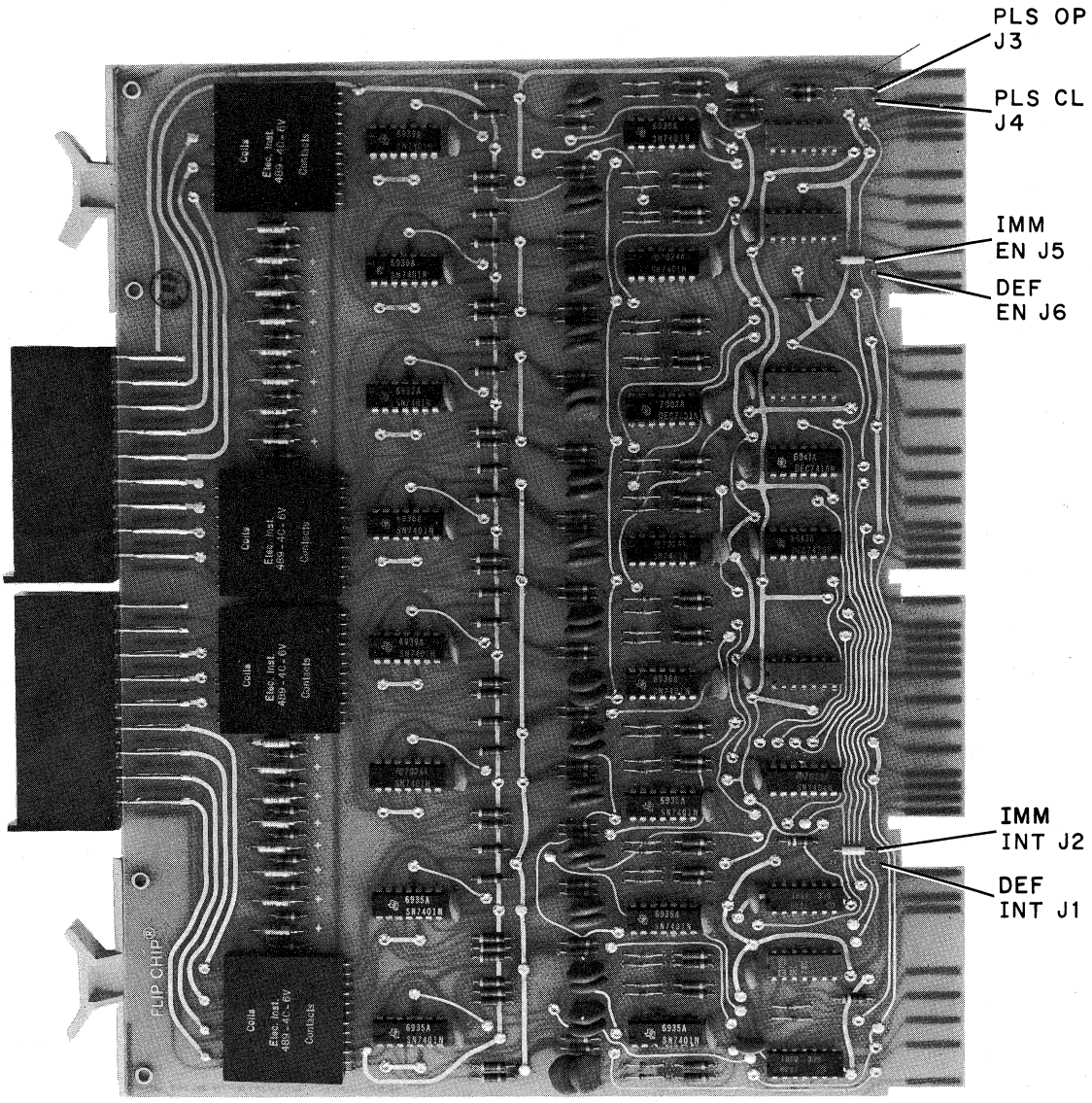


Figure 4-11 Location of Jumpers (W733)

W741
CONTACT SENSE SOLID STATE INPUT MODULE

FUNCTIONAL SPECIFICATIONS

Power Requirements:	+5V @ 0.25A maximum
Input Levels:	+4.6V to 7.0V Differential Input = 1 13 mA to 22 mA -1.0V to +1.4V Differential Input = 0 -2 mA to +2 mA
Input Overvoltage Protection:	±12V maximum sustained input
Failure Mode:	Fails on per point basis
Response Time:	Normal – 2.5 ms maximum. High speed – 50 μs maximum.
Input Rate:	Normal – 200 Hz maximum. High speed – 10 kHz maximum.
Common Mode Input Impedance:	$10^{10}\Omega$ minimum

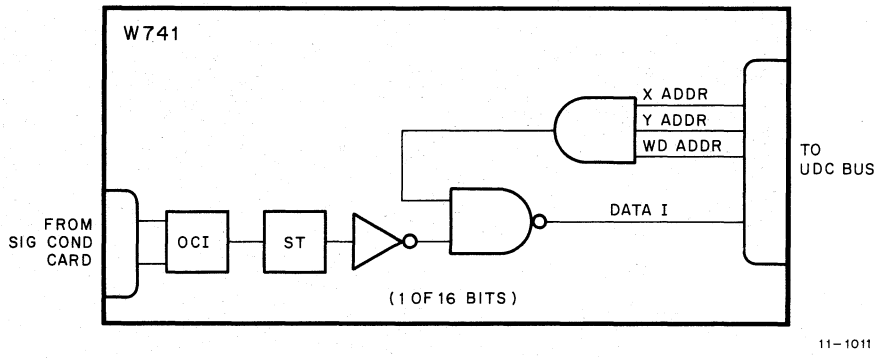


Figure 4-12 Simplified Schematic Diagram (W741)

DESCRIPTION

The W741 Contact Sense Module (Figure 4-12) provides high input isolation with solid state reliability through the use of a light emitting diode-photo transistor isolation element (OCI) and a Schmitt Trigger (ST). The W741 contains 16 bits of sense logic. When addressed by the UDC, information concerning the state of the 16 bits is present at the data out gates. This data is the present condition of the 16 bits, and can change at any time. It is not stored into any buffer; it is used for monitoring purposes. In addition to contact sensing, the W741 may be directly interfaced to T^2L, RTL, and DTL logic.

HIGH-SPEED OPTION

The W741 Module is capable of a fast response time, as indicated in the above specifications. This is accomplished by clipping out the 0.33 μF capacitors shown in Figure 4-13.

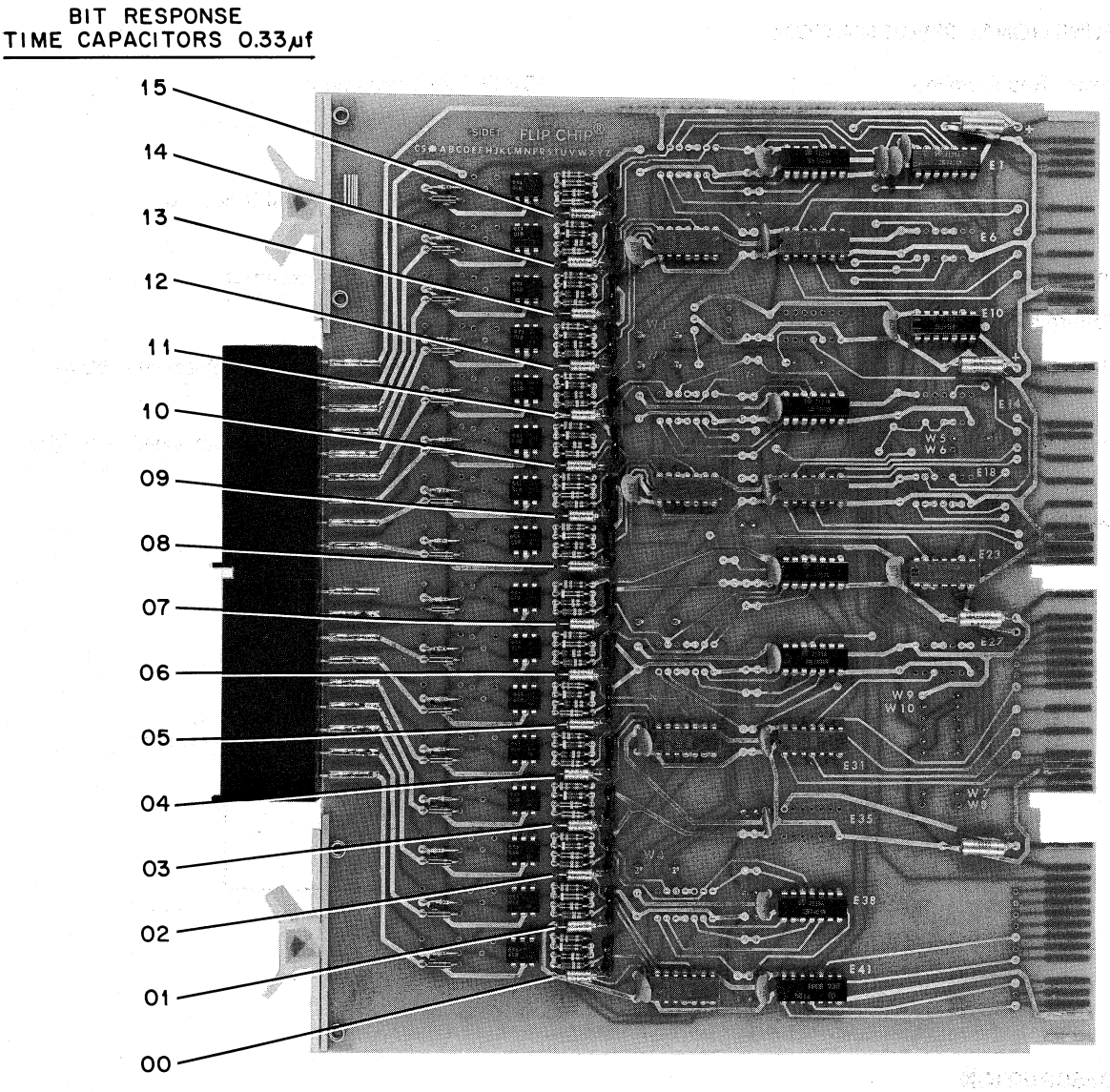


Figure 4-13 Location of Bit Response Time Capacitors (W741)

W743
CONTACT INTERRUPT SOLID STATE INPUT MODULE

FUNCTIONAL SPECIFICATIONS

Power Requirements:	+5V @ 0.25A maximum
Input Levels:	+4.6V to 7.0V differential input = 1 13 mA to 22 mA -1.0V to +1.4V differential input = 0 -2 mA to +2 mA
Input Overvoltage Protection:	±12V maximum sustained input
Failure Mode:	Fails on per point basis
Response Time:	Normal – 2.5 ms maximum. High Speed – 50 μs maximum.
Input Rate:	Normal – 200 Hz maximum. High Speed – 10 kHz maximum.
Common Mode Input Impedance:	$10^{10}\Omega$ maximum

DESCRIPTION

The W743 Contact Interrupt Module (Figure 4-14) provides high input isolation with solid state reliability through the use of a light emitting diode photo transistor isolation element (OCI) and a Schmitt Trigger (ST). The contact interrupt module is similar to the contact sense with the addition of interrupt logic. This logic is activated whenever one of the input points changes state. Via its interrupt and interlocking scan logic, the UDC controller can rapidly identify the interrupting module. The W743 Module may also be directly interfaced to T^2L, RTL, and DTL logic.

MODULE JUMPER CONFIGURATION

The jumpers on the W743 Module must be configured by the user to meet his application needs. The jumpers and their function are listed in Table 4-5 and are shown in Figure 4-15.

Table 4-5
Jumper Options (W743)

Function	Jumpers Required
IMM INT	W5, W7
DEF INT	W6, W8
PLS OP*	W9
PLS CL*	W10

*PLS OP and PLS CL are logic levels to be used in Software Routines, as an aid in determining change of state information.

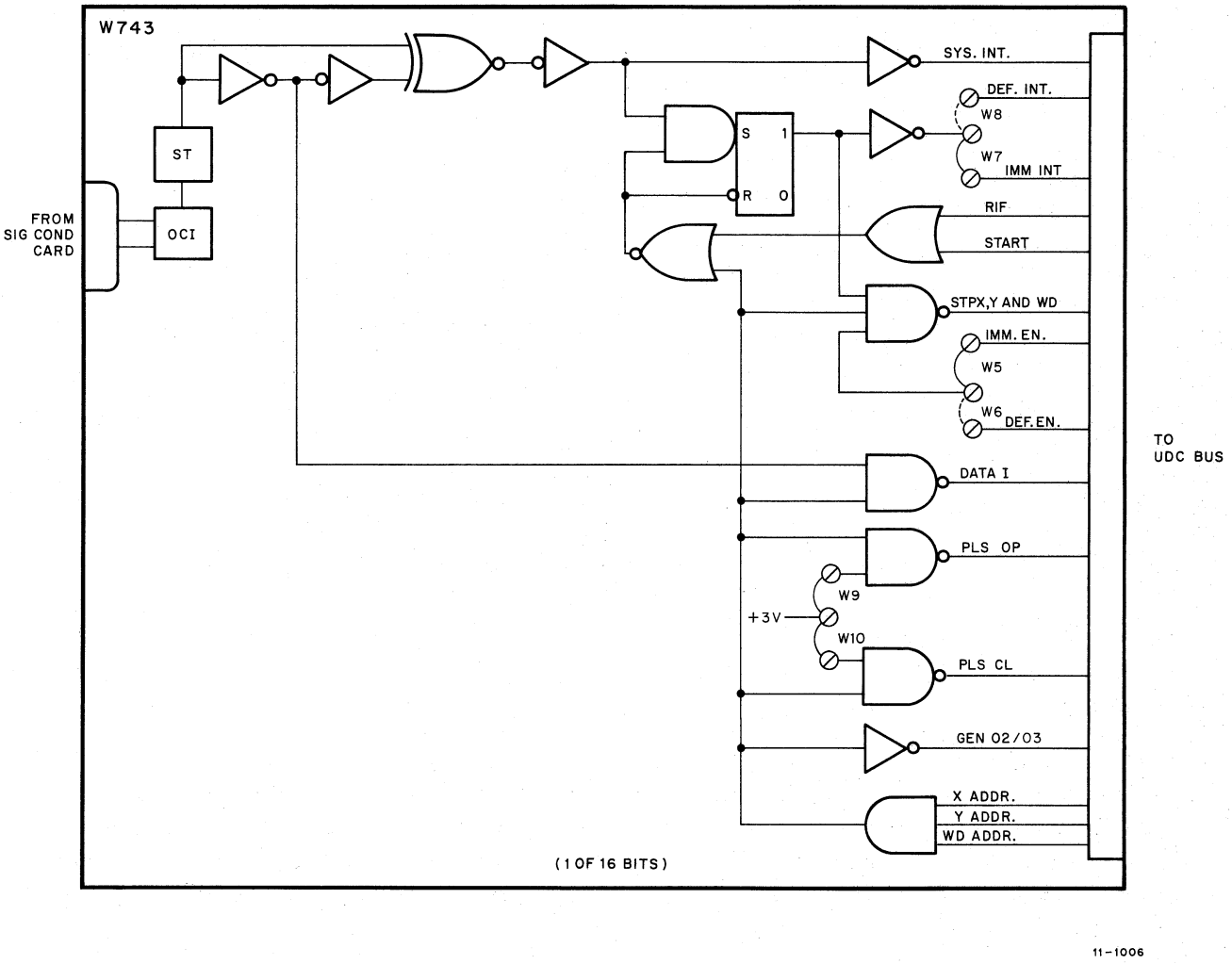


Figure 4-14 Simplified Schematic Diagram (W743)

HIGH-SPEED OPTION

The W743 Module is capable of a fast response time as indicated in the module specifications. This is accomplished by clipping out the 0.33 μF capacitors shown in Figure 4-15.

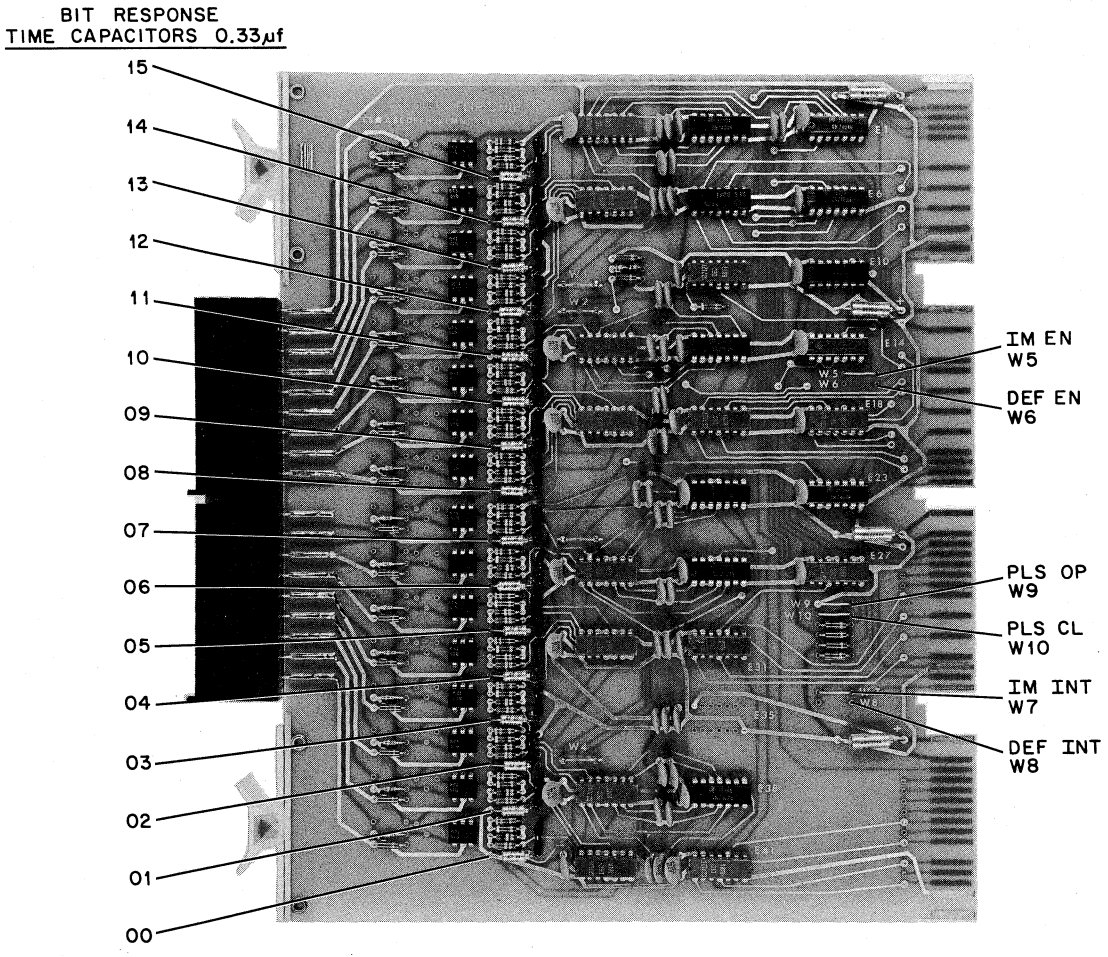


Figure 4-15 Location of Jumpers and Bit Response Time Capacitors (W743)

M685
FLIP-FLOP DRIVER OUTPUT MODULE

FUNCTIONAL SPECIFICATIONS

Power Requirements:	+5V @ 0.625A maximum
Output Circuit:	Solid State – Open collector returned through diode and resistor to +5V.
Output Drive Capability:	Resistive Load – 55 Vdc, 250 mA Inductive Load – 55 Vdc, 250 mA (Diode suppression supplied) Incandescent Lamps: Lamps rated at 40 mA, to 48V Lamps rated at 60 mA, to 28V Lamps rated at 80 mA, to 18V Lamps rated at 100 mA, to 12V T^2L Level Compatible (2 unit loads)
Response Time:	Rise Time – 10 μs (Resistive Load without Field Wiring) Fall Time – 0.5 μs
Logic to Field Transfer:	A logic 1 will provide current sinking ability.
Signal Conditioning:	W403 only

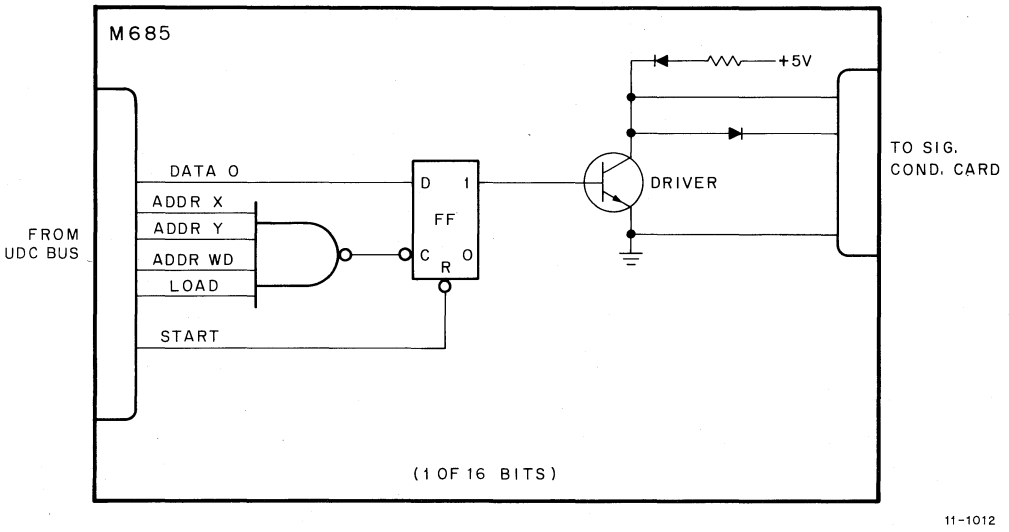


Figure 4-16 Simplified Schematic Diagram (M685)

DESCRIPTION

The M685 Flip-Flop Driver Output Module (Figure 4-16) provides 16 identical solid state buffered outputs. It can be used to drive solid state logic (0 and +5V) or as a current driver for control of solenoid valves, relays, lamps, displays, etc. Each flip-flop in the output register may be set by a MOV instruction.

When used to drive logic circuits, a 0V output will be generated by the flip-flop being set, and a +5V output will be generated by the flip-flop being cleared. This is accomplished by the load to +5V on the collector of the

output circuit. The rise and fall time of this circuit measured at the screw terminals with no external field wiring is 10 μs and 0.5 μs, respectively.

A diode is in series with the +5V load to provide isolation from field voltages when used as a current driver. Each driver circuit is protected from damage by inductive loads. Provided for all 16 circuits is a common ground line, which must be connected to the common side of the field power source.

M687
SINGLE-SHOT DRIVER OUTPUT MODULE

FUNCTIONAL SPECIFICATIONS

Power Requirements:	+5V @ 1A maximum
Output Circuit:	Solid State – Open Collector returned through diode and resistor to +5V.
Output Drive Capability:	Resistive Load – 55 Vdc, 250 mA Inductive Load – 55 Vdc, 250 mA (Diode suppression supplied)
	Incandescent Lamps: Lamps rated at 40 mA, to 48V Lamps rated at 60 mA, to 28V Lamps rated at 80 mA, to 18V Lamps rated at 100 mA, to 12V.
	T^2L Level Compatible (2 unit loads)
Response Time:	Rise Time – 10 μs Fall Time – 0.5 μs (Resistive Load without Field Wiring)
Logic to Field Transfer:	A logic 1 will provide current sinking ability.
Signal Conditioning:	W403 only
Timing Ranges:	0.5 ms to 80 ms – Short Range 80 ms to 2 sec – Long Range (Adjustable on a per bit basis)
Recovery Time:	0.05 ms – Short Range 2 ms – Long Range

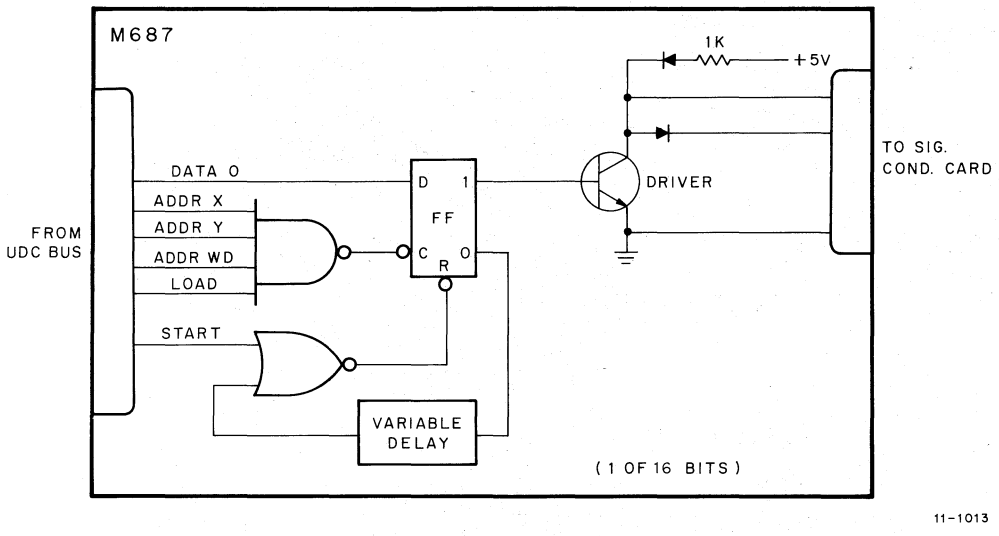


Figure 4-17 Simplified Schematic Diagram (M687)

DESCRIPTION

The M687 Single-Shot Driver Output Module (Figure 4-17) provides 16 individually adjustable solid state pulse outputs. As noted for the M685, the M687 can be used to drive solid state logic or as a current driver. The delay circuit is turned on using a MOV instruction. The pulse duration for each output point is continuously adjustable from 0.5 ms to 80 ms. A connecting jumper allows this range to be increased to between 80 ms and 2.0 sec. The pulse duration will be set to 60 ms when delivered from the factory. The location of the pulse duration trimpots and jumpers are shown in Figure 4-18. The recovery time of the single-shots is 0.05 ms when operating in the low range, and 2.0 ms when operating in the upper range. This recovery time determines the maximum repetition rate per point.

MODULE JUMPER CONFIGURATION

Jumpers are required for range selection of the timeout. The long timeout range is selected when the jumper is installed (Figure 4-18).

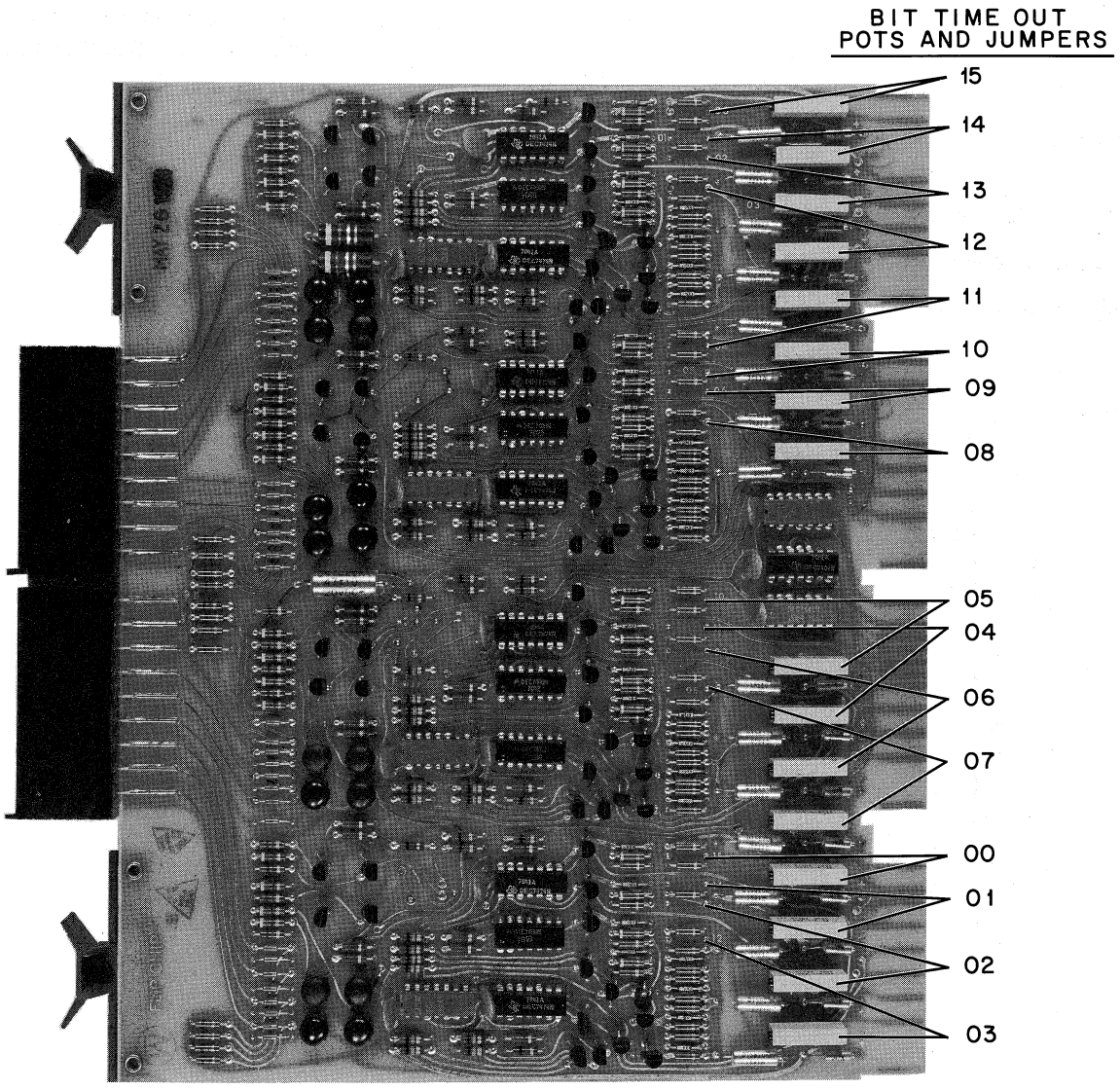


Figure 4-18 Location of Bit Timeout Pots and Jumpers (M687)

M803
LATCHING RELAY OUTPUT MODULE

FUNCTIONAL SPECIFICATIONS

Power Requirements:	+5V @ 0.625A maximum
Relay Type:	Mercury Wetted Form C, Magnetic Latching (N.O. or N.C. contacts available at screw terminals)
Switching Specification:	250V, 2A (100 VA maximum)
Response Time:	3 ms maximum
Logic to Field Transfer:	Logic 1 closes N.O. contacts
Signal Conditioning:	W400 or W402, Arc suppression is required (see Paragraph 4.6).

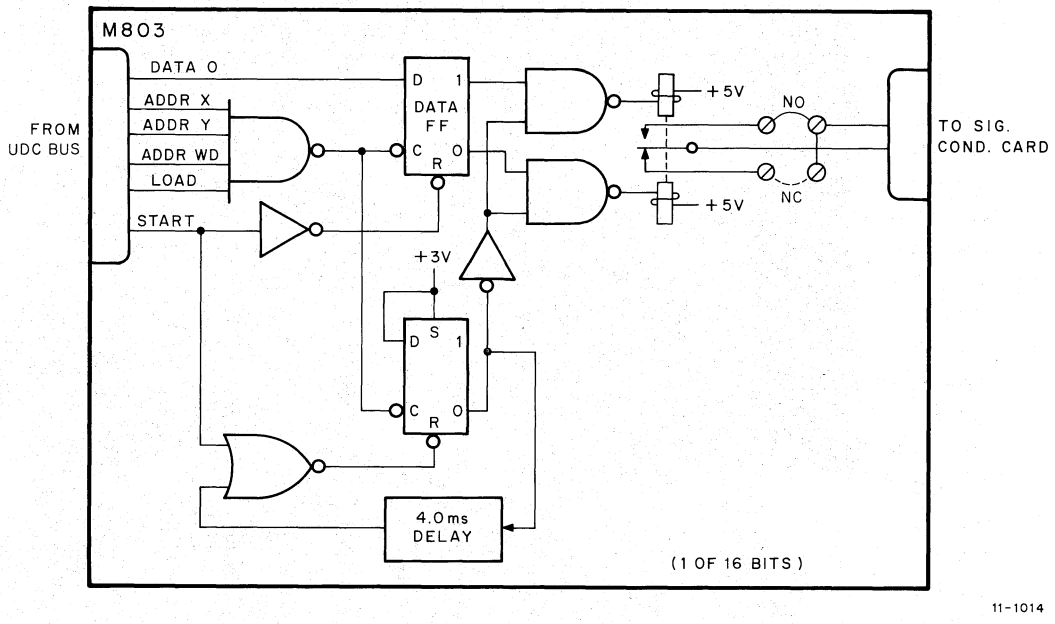


Figure 4-19 Simplified Schematic Diagram (M803)

DESCRIPTION

The M803 Latching Relay Output Module (Figure 4-19) provides *fail-safe* operation of 16 electrically isolated normally open or normally closed mercury-wetted relay outputs. Magnetically latched relays remain set in event of power failure, ensuring continuity and integrity of field circuits.

The register on the module is loaded by the MOV instruction. The MOV instruction generates a 4-ms pulse, which is used to energize the relay coils in accordance with the input data. During this period, the latching relays will change state in approximately 3.0 ms (without bounce) and remain in that state until changed under program control.

MODULE JUMPER CONFIGURATION

The board is manufactured and tested with a jumper in place; the normally open (N.O.) contact and common is therefore the active pair (Form A). The normally closed (N.C.) contact may be used with the common as the active pair (Form B) by removing the existing jumper and inserting it in the adjacent set of split lugs. This jumper change can be made on a per point basis (Figure 4-20).

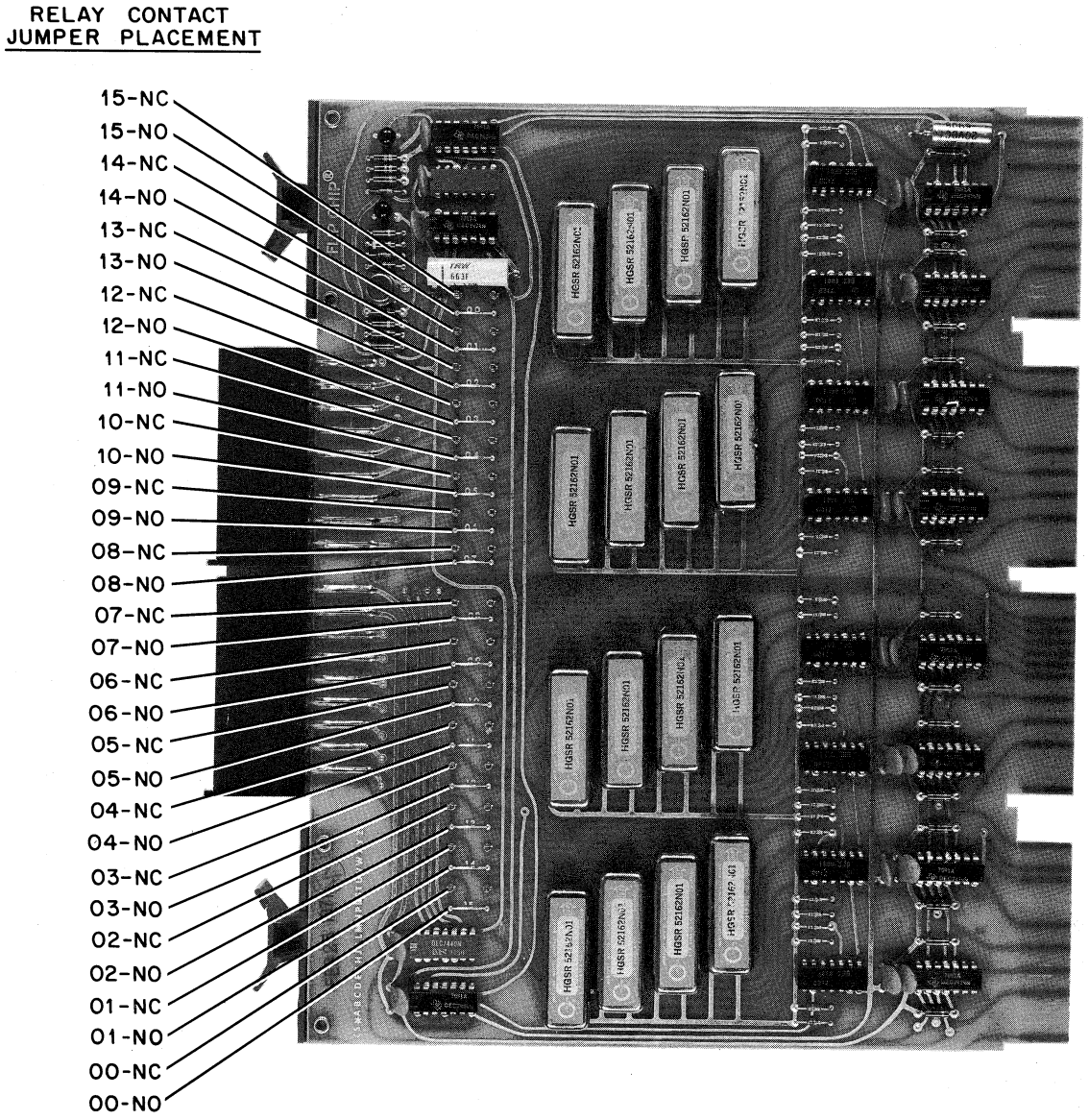


Figure 4-20 Location of Bit Relay Contact Jumpers (M803)

M805
FLIP-FLOP RELAY OUTPUT MODULE

FUNCTIONAL SPECIFICATIONS

Power Requirements:	+5V @ 0.65A maximum
Relay Type:	Mercury Wetted Form C (N.O. or N.C. contacts available at screw terminals)
Switching Specifications:	250V, 2A (100 VA maximum)
Response Time:	3 ms maximum
Logic to Field Transfer:	Logic 1 closes N.O. Contacts
Signal Conditioning:	W400 or W402 – Arc suppression is required (see Paragraph 4.6).

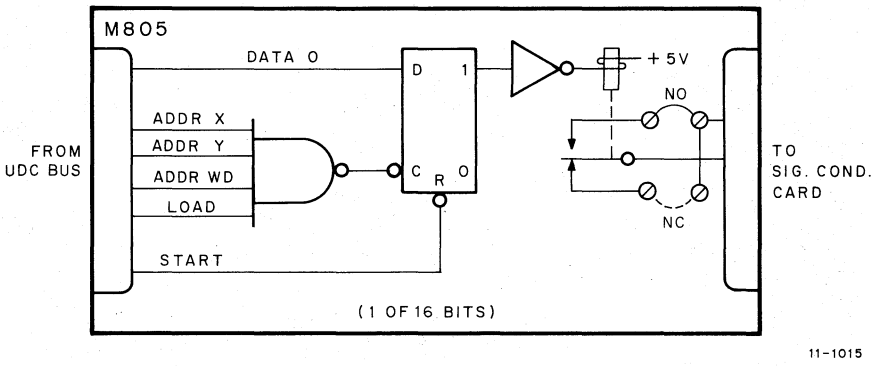


Figure 4-21 Simplified Schematic Diagram (M805)

DESCRIPTION

The M805 Flip-Flop Relay Output Module (Figure 4-21) provides 16 electrically isolated normally open or normally closed mercury-wetted relay output contacts for buffered control of relays, contactors, displays, lamps, etc. The module is supplied with a jumper in place so that the N.O. and common contacts are the active pair (Form A). The N.C. and common contacts may be used as the active pair (Form B) by removing the existing jumper and inserting it in the adjacent set of split lugs. This jumper change can be made on a per point basis.

The relays are driven by a flip-flop register, which is loaded by a MOV instruction. A logical 1 energizes the relay coil in approximately 3.0 ms (without bounce), which remains energized until reset by a logical 0 being loaded or a power failure.

MODULE JUMPER CONFIGURATION

The board is manufactured and tested with a jumper in place; the normally open (N.O.) contact and common is therefore the active pair. The normally closed (N.C.) contact may be used with the common as the active pair (Form B) by removing the existing jumper and inserting it in the adjacent set of split lugs. This jumper change can be made on a per point basis (Figure 4-22).

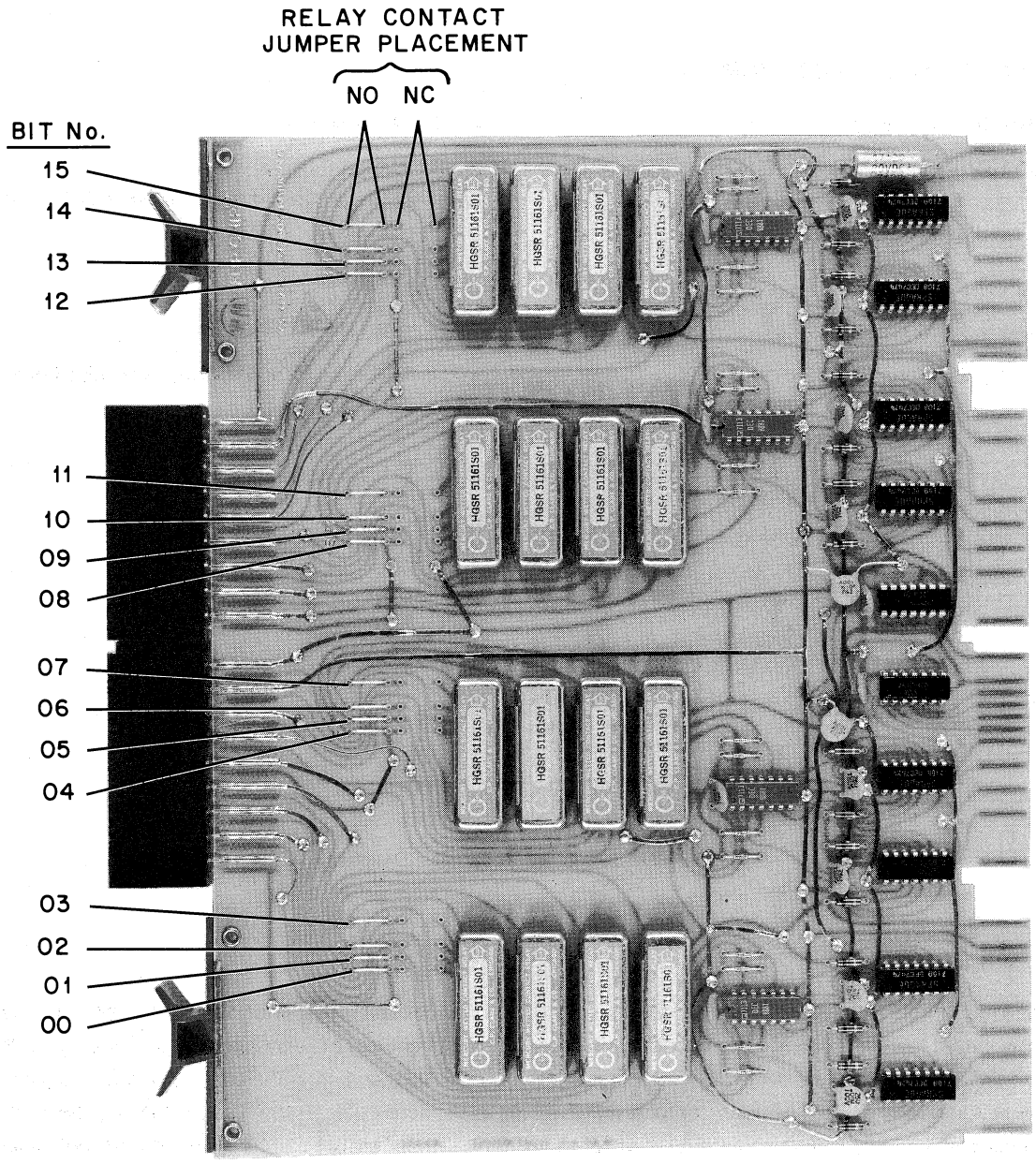


Figure 4-22 Location of Bit Relay Contact Jumpers (M805)

M807
SINGLE-SHOT RELAY OUTPUT MODULE

FUNCTIONAL SPECIFICATIONS

Power Requirements:	+5V @ 1A maximum
Relay Type:	Mercury Wetted Form C (N.O. or N.C. contacts available at screw terminals)
Switching Specification:	250V, 2A (100 VA maximum)
Response Time:	3 ms maximum
Logic to Field Transfer:	Logic 1 closes N.O. contacts
Timing Ranges:	0.5 ms to 80 ms – Short Range 80 ms to 2 sec – Long Range (Adjustable on a per bit basis)
Recovery Time:	Recovery time is always less than response time of relay.
Signal Conditioning:	W400 or W402, Arc Suppression is required (see Paragraph 4.6).

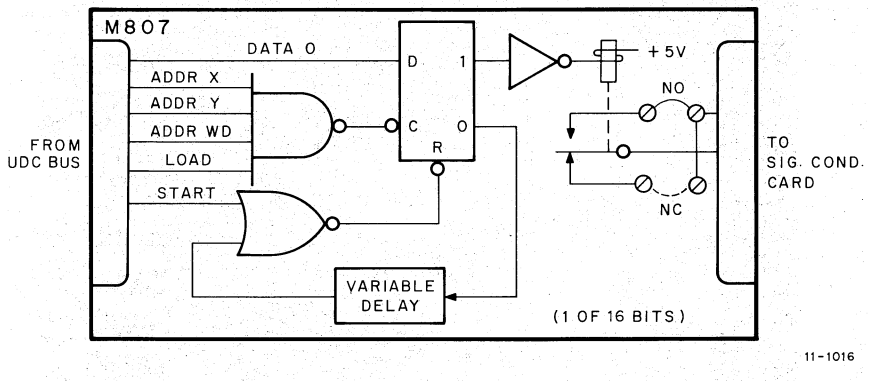


Figure 4-23 Simplified Schematic Diagram (M807)

DESCRIPTION

The M807 Single-Shot Relay Output Module (Figure 4-23) provides 16 electrically isolated, momentary, normally open or normally closed, mercury-wetted contact outputs for initiating alarms, lamps, field relays, etc. The module is supplied with a jumper in place so that the N.O. and common contacts are the active pair (Form A). The N.C. and common contacts may be used as the active pair (Form B) by removing the existing jumper and inserting it in the adjacent set of split lugs. This jumper change can be made on a per point basis.

The relays are driven by single-shots, which are triggered by a MOV instruction. A logical 1 energizes the relay coil for the preset pulse duration, thereby operating the output relay contacts for that period of time. The duration of the contact closure for each output point is continuously adjustable from 0.5 ms to 80 ms. Connecting a jumper in the variable delay circuit allows this range to be increased to between 80 ms and 2.0 sec. The duration will be set to 60 ms when delivered from the factory. The location of the pulse duration trimpots is shown in Figure 4.24.

MODULE JUMPER CONFIGURATION

Time-Out Range – Jumpers are required for range selection of the timeout. The long timeout range is selected when the jumper is installed (Figure 4-24).

Relay Contact – The board is manufactured and tested with a jumper in place; the normally open (N.O.) contact and common is therefore the active pair. The normally closed (N.C.) contact may be used with the common as the active pair (Form B) by removing the existing jumper and inserting it in the adjacent set of split lugs. This jumper change can be made on a per point basis (Figure 4-24).

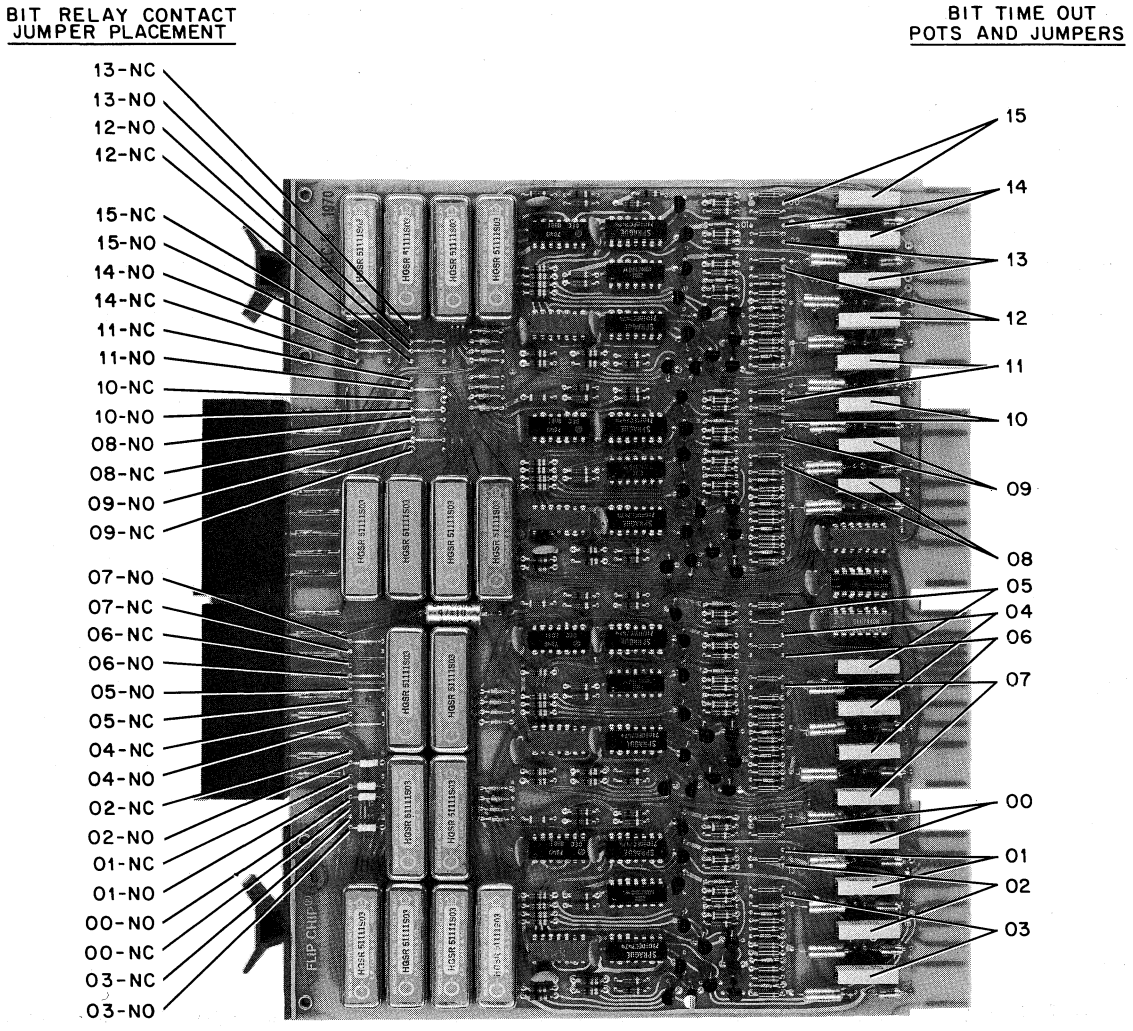


Figure 4-24 Location of Bit Time-out Pots and Jumpers and Relay Contact Jumpers (M807)

A633
D/A CONVERTER OUTPUT MODULE

FUNCTIONAL SPECIFICATIONS

Resolution:	One part in 1024 of full scale
Digital Input (CH0):	000000 = 0 output 020000 = 1/2 full scale output 037760 = Full scale output (-1 LSB)
Analog Output:	0V to -10V at 3 mA maximum
Gain Accuracy:	Adjustable to within ±0.05% of full scale at 25°C
Zero Offset:	Adjustable through zero
Settling Time:	35 μs maximum to within ±0.05% of final value with 150 pF load. 50 μs with signal-conditioning module
Linearity:	±1/2 LSB (least significant bit)
Power:	+5V ± 0.25V 450 mA maximum +18V ± 0.01V 147 mA maximum -18V ± 0.01V 30 mA maximum Power is supplied from an external H738A supply and applied through the screw terminals. One H738A supply will supply the necessary power to four A633 DACs and its signal-conditioning modules.
Signal Conditioning:	Four output signal-conditioning modules are available for use with the A633 DAC Module. A233 0V to +10V output at 15 mA maximum* A234 +1V to +5V output at 15 mA maximum* A235 4 mA to 20 mA into 750Ω maximum* A236 10 mA to 50 mA into 300Ω maximum*

*The outputs from the signal-conditioning modules are single-ended outputs. Therefore, the loads should be of the type that can be grounded to the analog ground, which in turn is connected to system ground in the UDC.

DESCRIPTION

The A633 DAC Module contains four 10-bit D/A converters, with input buffer registers, ladder networks, output voltage amplifier, and a reference supply (Figure 4-25).

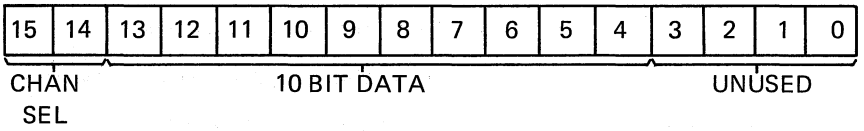
There is also a power low circuit on the module that grounds the input load signal in the event that computer power is low or is lost. This feature is available for the user who cannot afford to lose the analog output during a power failure and has the converter connected to an auxiliary backup supply.

The module operates like any digital output module in the UDC system. The 16-bit input data word is divided into two major parts: the DAC data word (bits 13 through 4) and the channel select code (bits 15 and 14). The 2-bit channel select code determines which D/A channel will be selected.

Bit 15	Bit 14	Channel
0	0	00
0	1	01
1	0	02
1	1	03

The complete 16-bit data word can be loaded on the D/A Module at one time. Channel selection must be updated at each data word transfer. There are no status bits on the module; therefore, enough time must be allowed between conversions for settling time purposes.

DATA FORMAT



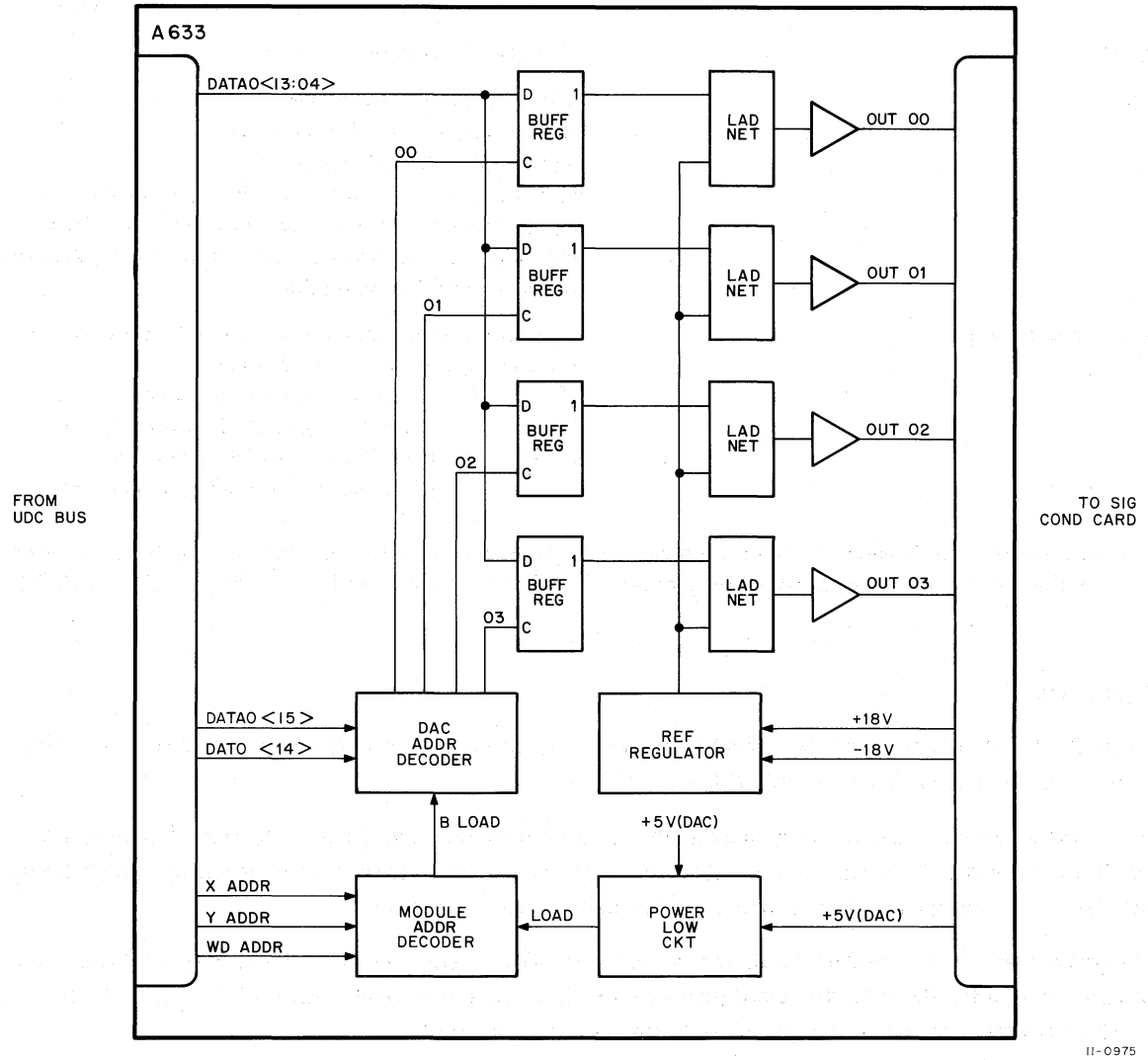


Figure 4-25 Simplified Schematic Diagram (A633)

MODULE JUMPER CONFIGURATION

The only jumpers provided are those needed for use with a battery or backup power supply (Figure 4-26).

Function	Jumper
Battery or Backup Supply	W1
Normal Operation	W2

When the battery or backup supply is used, the start signal is inhibited from clearing the DACs during power restoration.

MODULE ADJUSTMENTS

All module adjustments are made at the factory. However, if there is a need for re-adjustment A-SP-BA633-0-4 DAC Checkout procedure should be consulted.

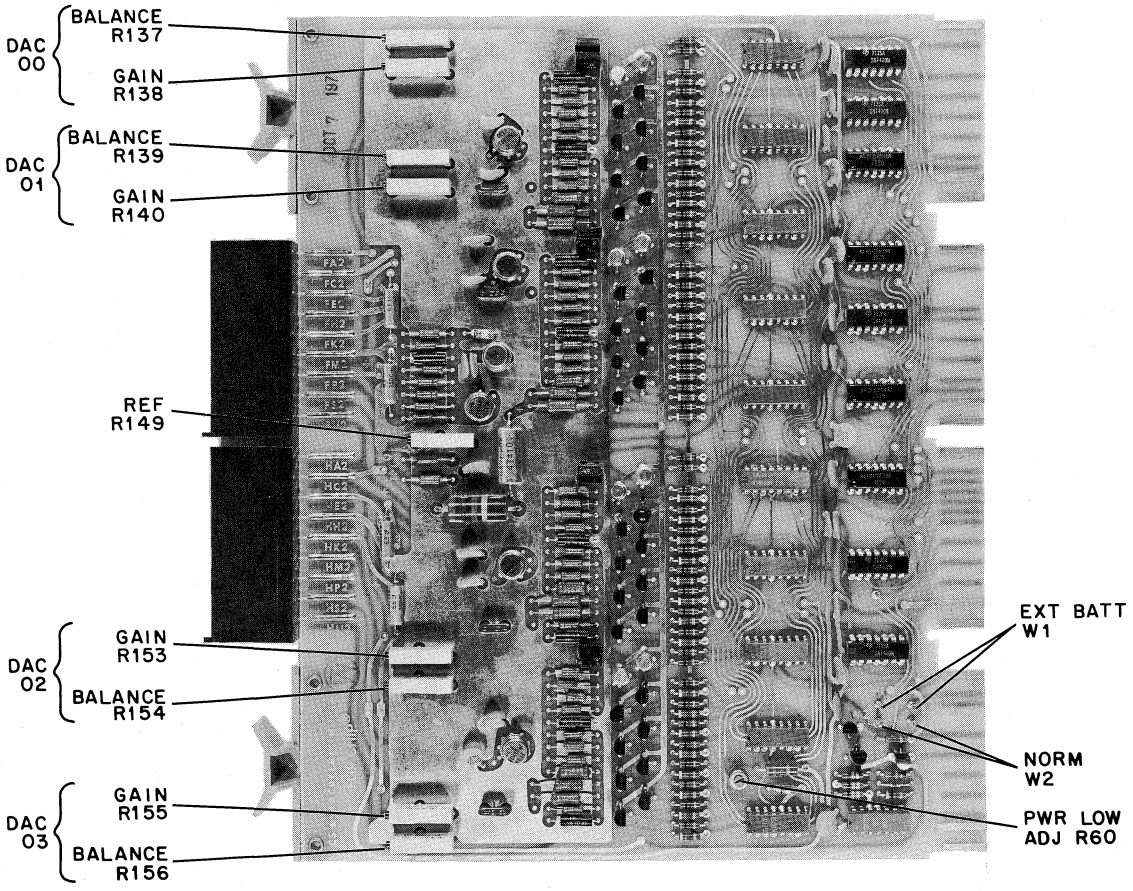


Figure 4-26 Location of Adjustments and Jumpers (A633)

W734
I/O COUNTER MODULE

FUNCTIONAL SPECIFICATIONS

Counter Type:

16-bit asynchronous binary up-counter buffered with anti-coincidence circuitry. READ-WRITE

Power Requirements:

+5V @ 1A maximum

Counter Inputs:

Selectable by PC switch.

PC Switch Pos.	Input
1	Contact Input (CONT) $10^9\ \Omega$ minimum, 250V, input isolation 6V ± 10% @ 18.5 mA input voltage 100 Hz maximum input frequency
2	Voltage Input (CV) "0" = 0.75V maximum "1" = +1.4V to 35V 25 kHz maximum input frequency
3	CL00 UDC internal clock (1.75 Hz to 1.75 kHz adjustable)
4	CL01 UDC internal clock (1.75 kHz to 17.5 kHz adjustable)
5	CLL line frequency clock
6	No input (Ground)

External Enable (EN):

Enabled = 0.7V maximum; not enabled = 1.4 to 35V

Counter Outputs:

Pulse ($\overline{P}$)
Control ($\overline{C}$)
Sign ($\overline{S}$)

Output Drive Capability:

Resistive Load: 55 Vdc @ 250 mA
Inductive Load: 55 Vdc @ 250 mA
(Diode Suppression Supplied)
Incandescent Lamps: Lamps rated at 40 mA, to 48V
Lamps rated at 60 mA, to 28V
Lamps rated at 80 mA, to 18V
Lamps rated at 100 mA, to 12V
T^2L Compatible (2 unit loads)

Pulse (P) Output Characteristics:

Frequency – (at system counting frequency)
CLK 00: 175 Hz to 1.75 kHz, adjustable
CLK 01: 1.75 kHz to 17.5 kHz, adjustable
CLK L: Line frequency

Width – (Adjustable in four ranges)
RANGE 1: 20 μs to 112 μs
RANGE 2: 112 μs to 630 μs
RANGE 3: 630 μs to 3.5 ms
RANGE 4: 3.5 ms to 20 ms

FUNCTIONAL SPECIFICATIONS (Cont):

Logic to Field Transfer: All outputs are enabled when sinking current.

Address Restriction: Due to the fact that the buffer update is inhibited while the W734 Counter is addressed, the module should not be located in address slot 000.

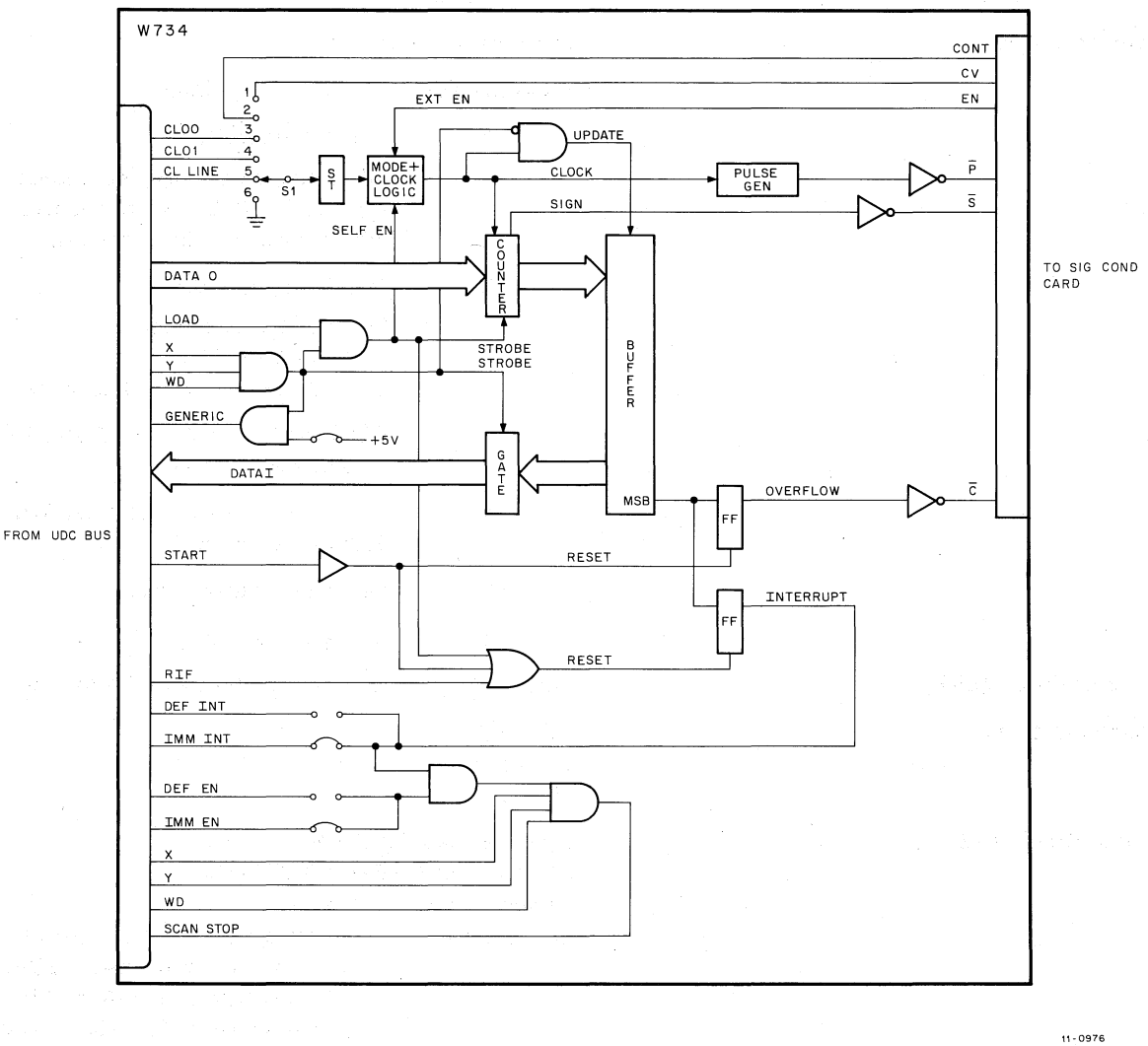


Figure 4-27 Simplified Schematic Diagram (W734)

DESCRIPTION

The W734 I/O Counter Module (Figure 4-27) is a 16-bit asynchronous binary up-counter. An output buffer register is updated after each counter increment. When the module is addressed (under program control), the buffer update is inhibited, preventing any data change. A full 16-bit data word can be parallel loaded into the counter, allowing the counter to be preset under program control. To use the counter as a down counter, the 2's complement of a number must be loaded.

One of five inputs, selectable by a P.C. mounted switch, can be selected for incrementing the counter. Two are external event inputs and three are internal UDC clock inputs. The external event inputs include: a contact sensing input and a voltage input.

An enable/disable jumper is provided to select either an external enable or an internal self enable for starting the counter after each preload. Upon overflow, the counter generates an interrupt and may continue or stop counting. A jumper is provided to inhibit the counter on interrupt.

The counter provides three solid state outputs: pulse, control, and sign. The pulse output is a pulse train whose frequency is determined by the counter clocking frequency (counter input) and whose pulse width is established by a jumper and a potentiometer. The control output goes true whenever the counter is enabled and the sign output is available when the counter is set up (by jumper) for 15-bit plus sign operation.

MODULE CONFIGURATION

Setting the counter up for a specific application is a user task. Therefore, the user should familiarize himself with the various operating modes of the counter.

FUNCTIONAL MODES

ENABLE (External/Self)

Two methods are available for enabling the counter: external and self. In the external enable mode, a signal at the EN screw terminals will enable the counter. If a count signal is present at the time the counter is enabled, it will not be counted. This mode is useful when external event synchronization is required for starting the count. If the counter is set up to operate in the self enable mode, power up, system initialization, or presetting the counter will start the counter. Then, upon OVERFLOW, the counter is disabled or continues counting depending on jumper setup. The counter starts counting from zero or from the count loaded.

OVERFLOW (Halt/Continue)

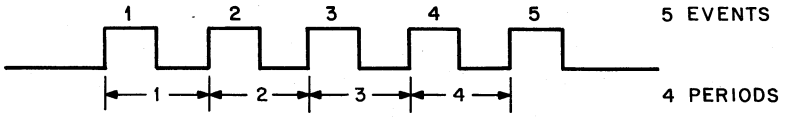
The module can be set up to halt or continue counting on overflow. In either case, an interrupt signal is issued by the counter.

SIGN Output

The module can be set up to provide for a direction bit by selecting the SIGN option. With this option selected, the module becomes a 15-bit counter with a sign bit, and overflow will occur when bit 14 (the 15th bit) overflows. The SIGN ("$\overline{S}$") output is available at the screw terminals as a solid state driver (open-collector) output.

COUNTING MODES

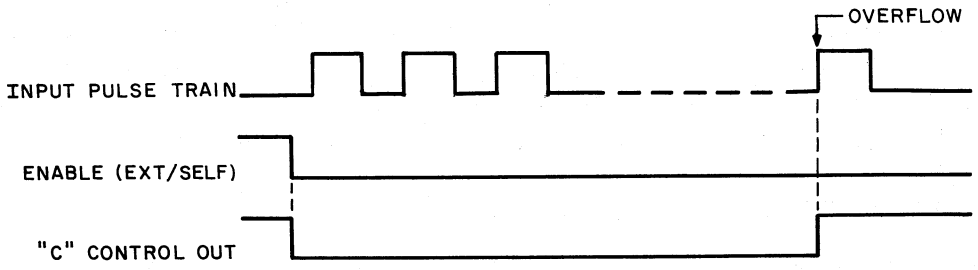
The module is able to count events or periods depending on which jumper is installed. Event and period counting is shown in the following illustration.



The control output ("$\overline{C}$") from the module behaves uniquely for each of the two counting modes.

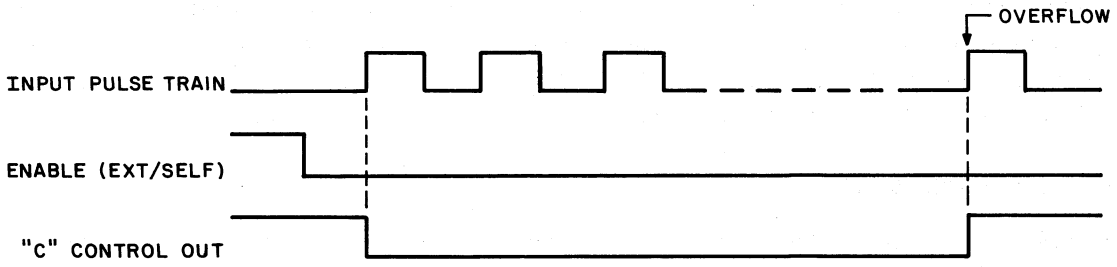
EVENT Counting

In this counting mode, the control output becomes TRUE when the counter is enabled and NOT TRUE on counter OVERFLOW as illustrated in the following timing diagram.



PERIOD Counting

In this counting mode, the control output becomes TRUE at the first count and NOT TRUE on counter OVERFLOW as illustrated in the following timing diagram.



NOTE
OVERFLOW will occur when counter bit 14 or 15 (depending on SIGN option selection) overflows.

OPERATIONAL MODES

The counter must be set up to operate as an interrupting I/O module in a UDC system. Therefore, the desired *GENERIC code* and *interrupt level* (IMM or DEF) must be established and selected. In addition, the desired *counter input* (clock) and output *pulse width* must be selected to place the counter into operation.

INTERRUPT Levels

The desired interrupt level must be chosen by installing the proper jumper on the counter module. Like all UDC interrupt modules, immediate and deferred interrupt level declarations are available for selection.

GENERIC Code

Since the counter can be used for a variety of functions, the following four GENERIC codes have been assigned to the counter module.

GENERIC Code	0123
	0100
	0101
	0110
	0111

One of these codes can be selected by installing the proper jumper(s) on the counter module.

CLOCK Selection

The input clock or counter input is selected by setting P.C. switch S1 to the desired position. The switch positions and the corresponding counter inputs are as follows:

Switch Position	Input
1	CONTACT
2	VOLTAGE
3	CL 00
4	CL 01
5	CL LINE
6	GROUND

Position 6 should be selected if the counter is used as a data storage or transfer buffer without being clocked.

Output Pulse Width

The width of the pulse output ("$\overline{P}$") is continuously adjustable from 20 μs to 20 ms in four ranges. Thus to obtain the desired width, the proper range must be selected by installing the correct jumper and potentiometer R32 must be adjusted. The four ranges are:

RANGE 1: 20 μs to 112 μs
RANGE 2: 112 μs to 630 μs
RANGE 3: 630 μs to 3.5 ms
RANGE 4: 3.5 ms to 20 ms

MODULE JUMPER CONFIGURATIONS

Table 4-6 and Figure 4-28 identify the required jumper for each counter mode. Using the table, the user should make sure that the proper jumpers for the desired modes of operation are installed on the module.

Table 4-6

Jumper Options (W734)

Module Jumpers		W1 or W2	W3	W4 or W5	W6	W7	W8	W9	W10	W11	W12 or W13	W14	W15 or W16	W17	W22 or W18	W19	W29 and W20	W30 and W21	W23	W28 or W24	W25	W27 or W26
FUNCTIONAL MODES																						
EXTERNAL ENABLE																				X		
SELF ENABLE																			X			
HALT ON OVRFL															X							
CONTINUE ON OVRFL																X						
SIGN BIT														X								
COUNTING MODES																						
EVENT COUNT																	X					
PERIOD COUNT																		X				
OPERATIONAL MODES																						
IMM INT		X		X																		
DEF INT			X		X																	
GEN CODES	0100										X		X									
	0101									X			X									
	0110										X	X										
	0111									X		X										
PULSE RANGE	RANGE 1					X																
	RANGE 2						X															
	RANGE 3							X														
	RANGE 4								X													
12 BIT OPERATION																					X	
16 BIT OPERATION																						X

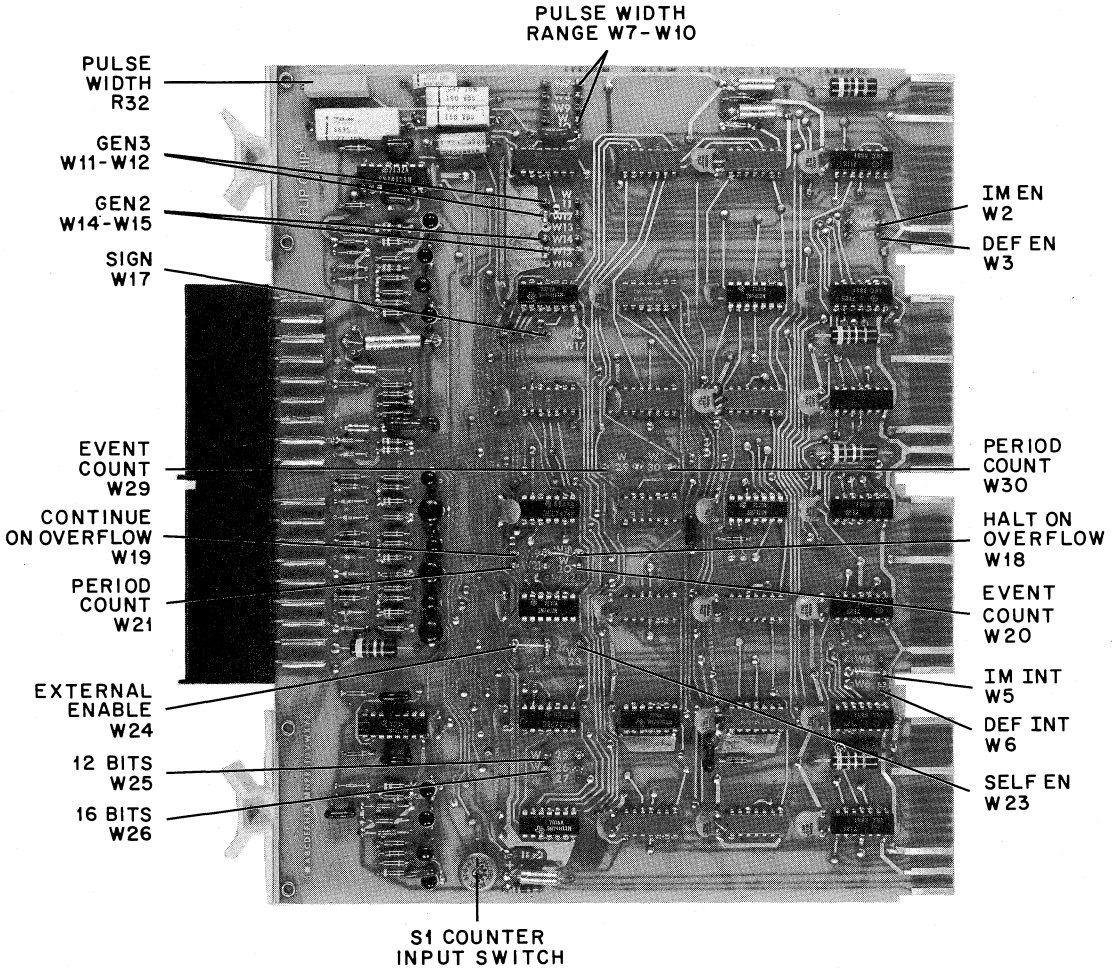


Figure 4-28 Location of Jumpers and Input Switch (W734)

4.6 SIGNAL CONDITIONING

The signal-conditioning modules serve as the interface between the field devices and the functional I/O modules. These modules plug into the end of the I/O module and accept the BC40C cable connector at the handle end. Proper selection of signal conditioning components and complete understanding and utilization of UDC signal conditioning options are essential for proper UDC system operation and implementation.

4.6.1 Field Power

In many cases, power from the field will be applied to functional I/O modules for contact sensing and load switching purposes. Two methods of distributing field power to UDC systems may be used: common and isolated.

4.6.1.1 Common Power – The common power signal-conditioning module (W402) will distribute a single field power source to all 16 bits on the functional I/O module as shown in Figures 4-29 and 4-30.

4.6.1.2 Isolated Power – The isolated power signal-conditioning module (W400) is used when the field power source for each bit is isolated as shown in Figures 4-31 and 4-32.

4.6.1.3 Driver Output – The driver output signal-conditioning module (W403) provides ground continuity for non-isolated solid state driver outputs.

4.6.2 Input Module Signal Conditioning for Contact Sensing

The following input modules may be used for contact sensing purposes:

a. W731
b. W733
c. W741
d. W743

These functional modules require 6V @ 15 mA to drive each of their 16 input circuits. However, the removal of voltage scaling jumpers on the W400 and W402 Signal-Conditioning Modules permits utilization of 24V or 48V as a source power. Table 4-7 defines the jumpers to be cut to permit utilization of higher input voltages. Figures 4-51 and 4-53 identify the location of these jumpers.

Table 4-7
Voltage Scaling Options

Power Source	Jumper
6V	Cut None
24V	Cut A
48V	Cut A and B

4.6.3 Input Module Signal Conditioning for Logic Level Sensing

The following solid state input modules may be used for logic level sensing purposes.

a. W741
b. W743

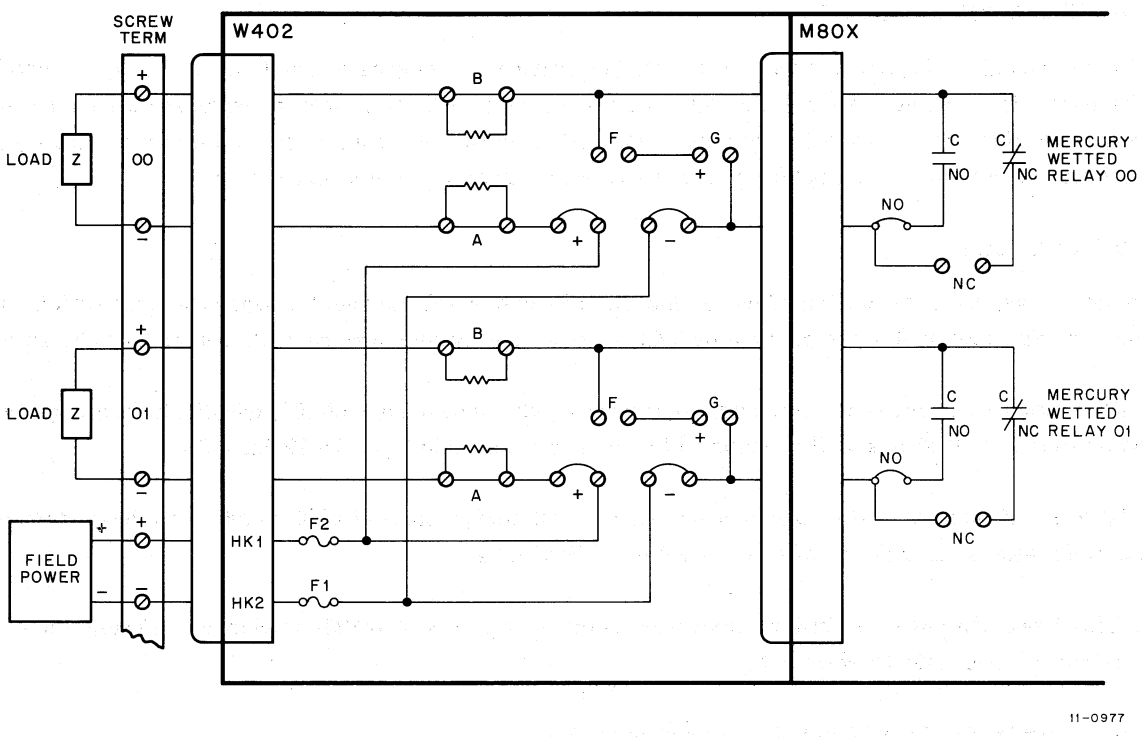


Figure 4-29 Common Power for Load Switching, Wiring Diagram

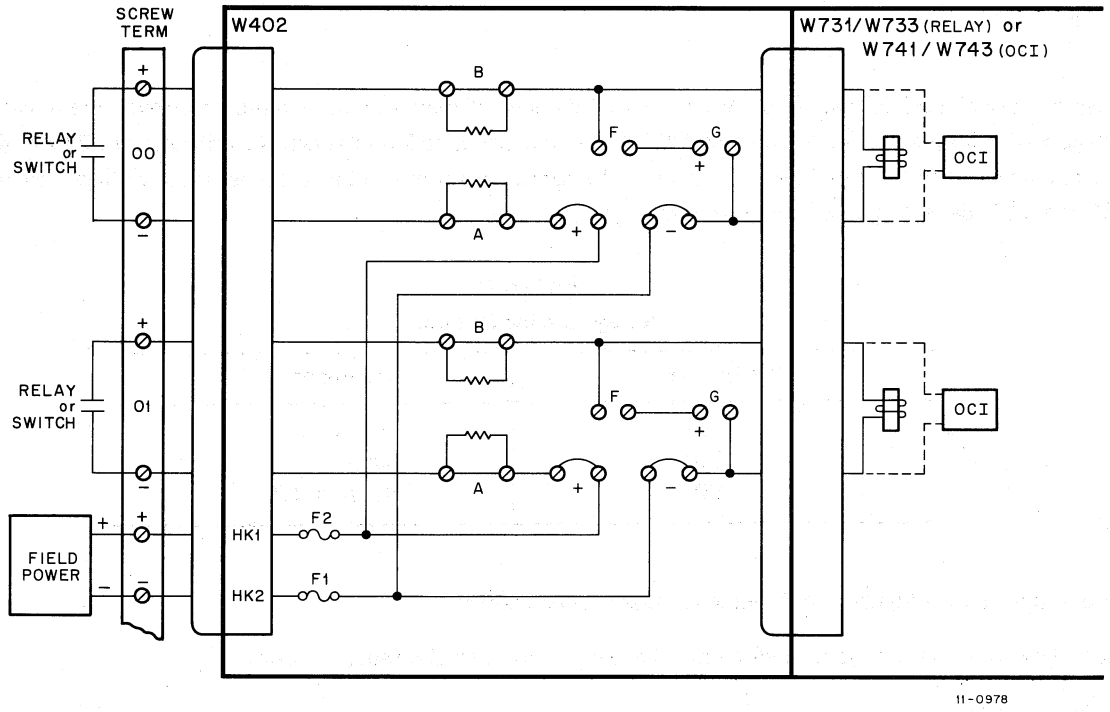


Figure 4-30 Common Power for Contact Sensing, Wiring Diagram

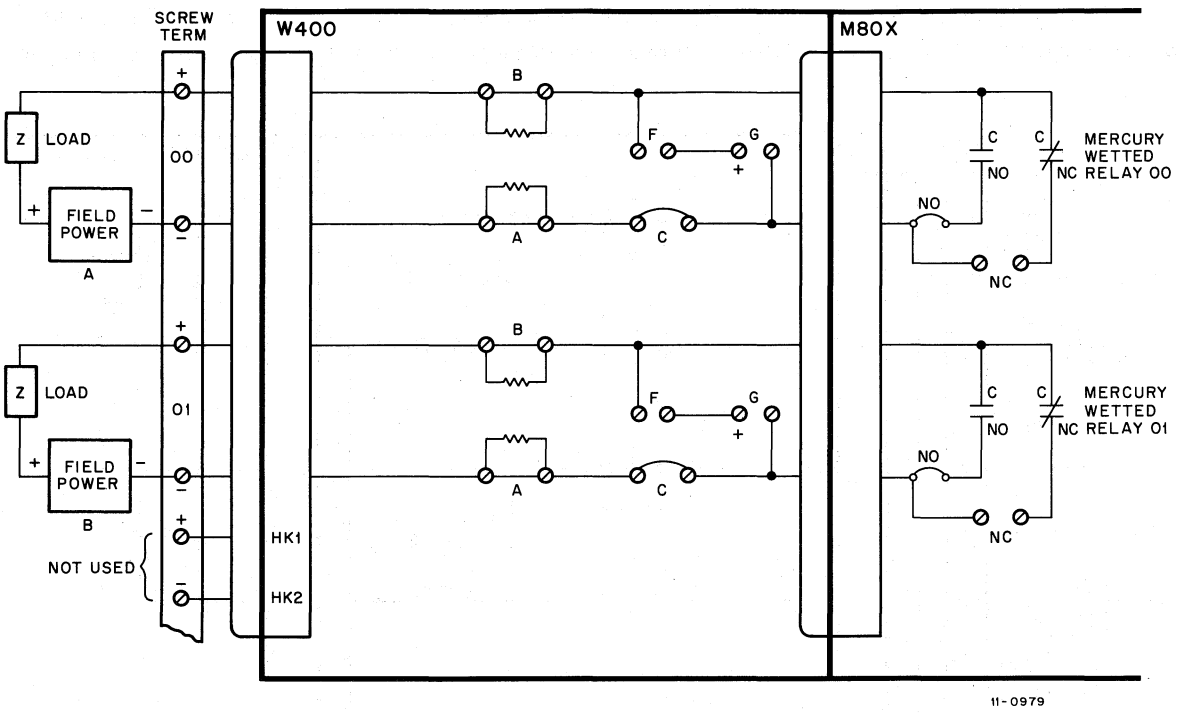


Figure 4-31 Isolated Power for Load Switching, Wiring Diagram

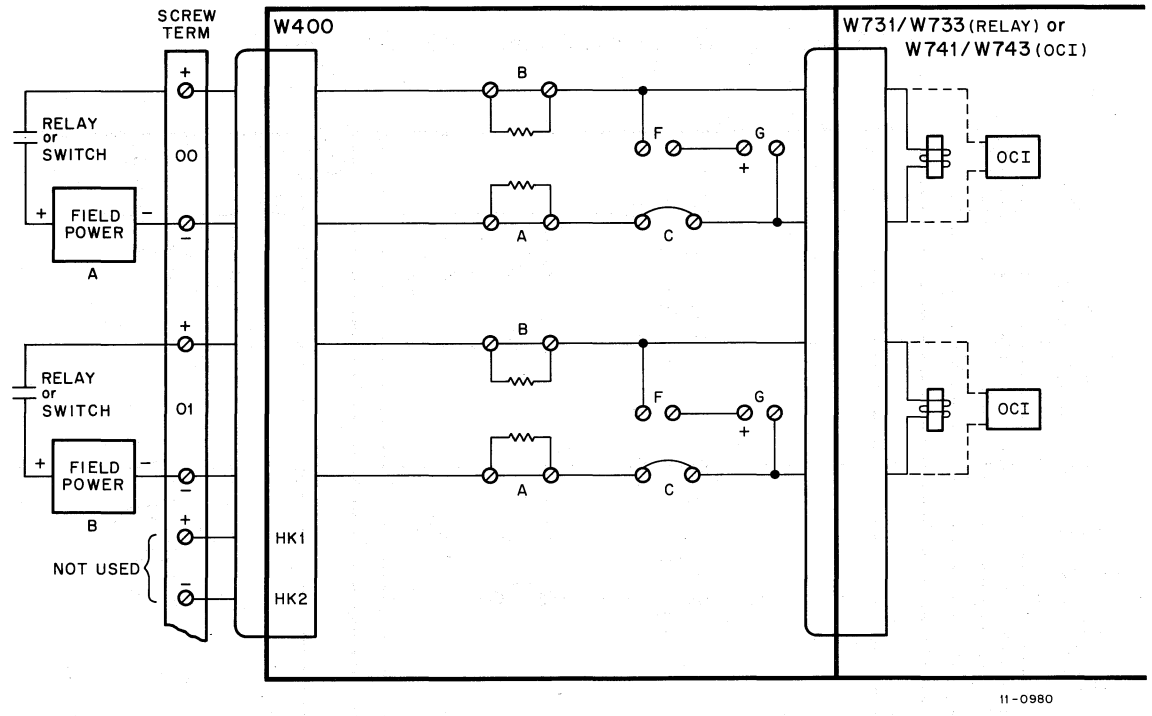


Figure 4-32 Isolated Power for Contact Sensing, Wiring Diagram

TTL, RTL, or DTL logic circuits can be used to supply the logic levels (Figures 4-33 through 4-35). The W400 Signal-Conditioning Module must be used to interface the field logic circuits with the solid state input modules.

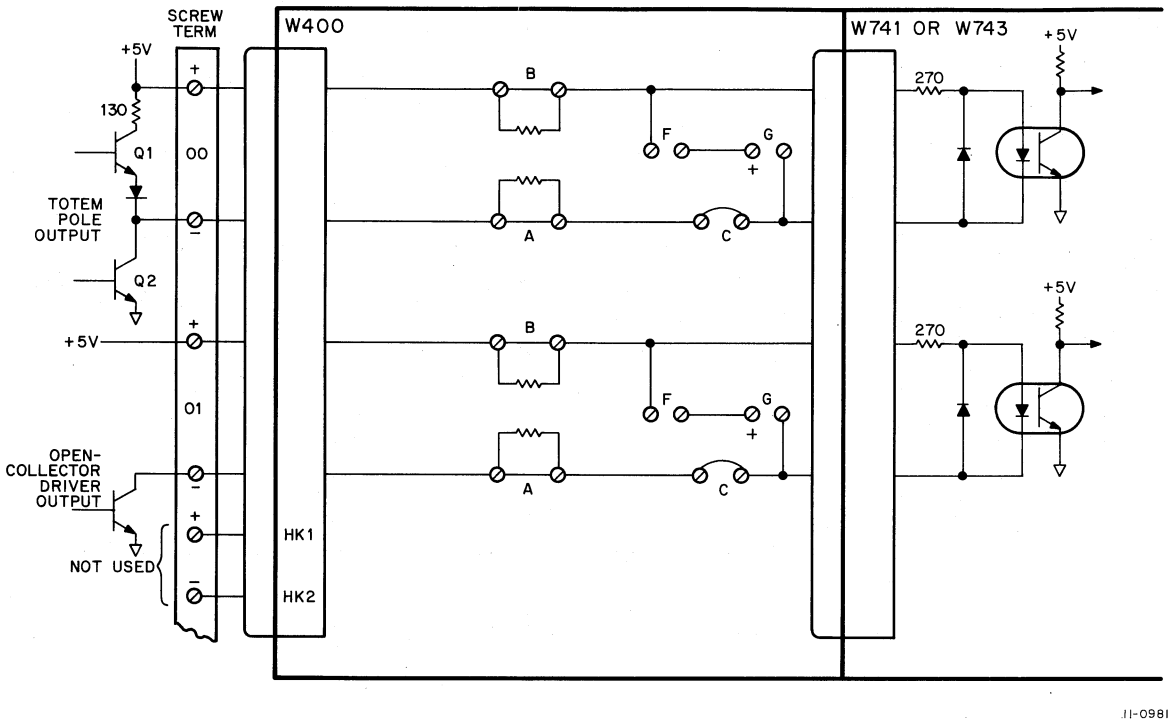


Figure 4-33 Logic Level (TTL) Input, Wiring Diagram

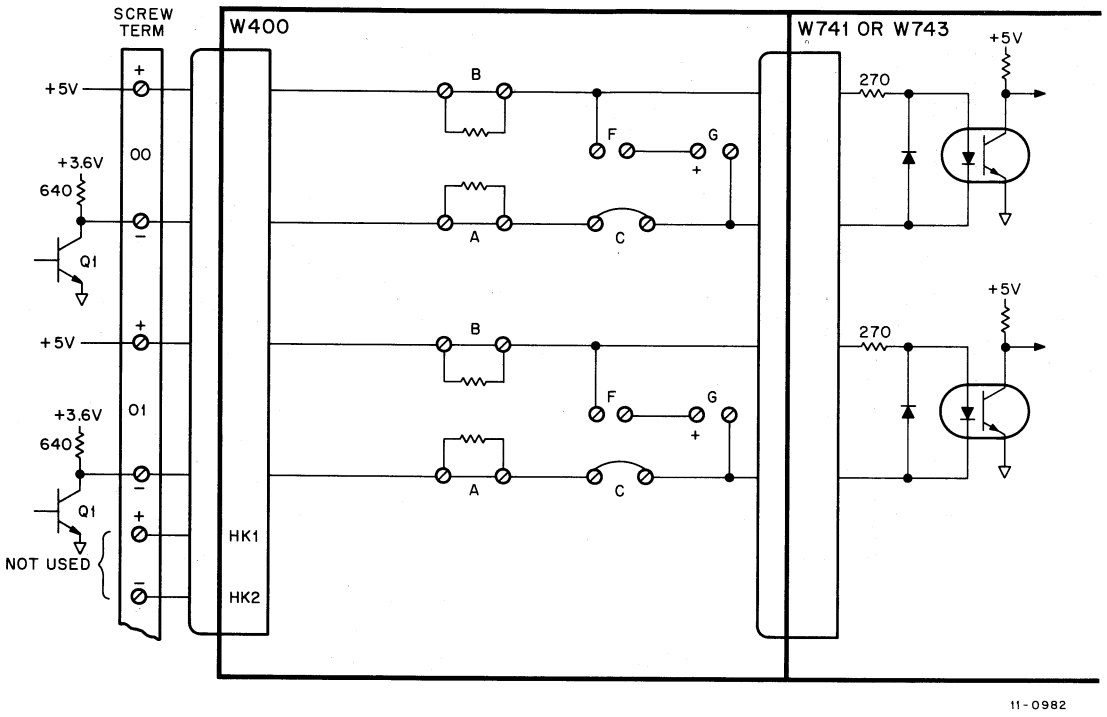


Figure 4-34 Logic Level (RTL) Input, Wiring Diagram

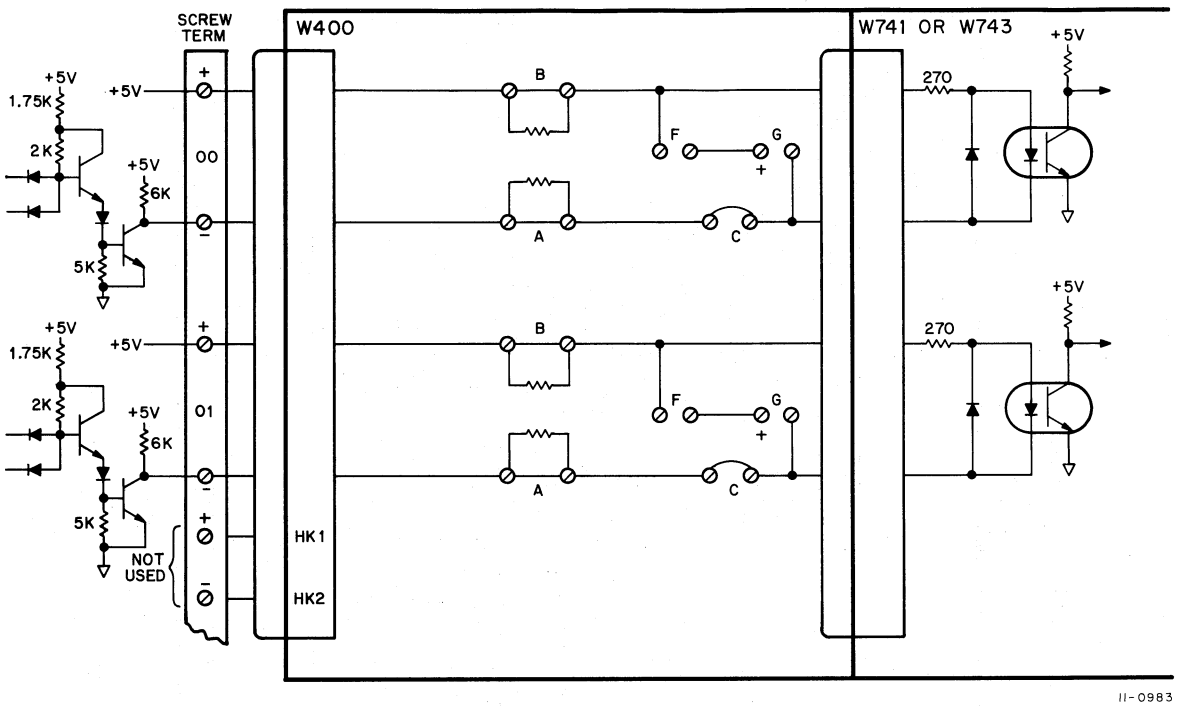


Figure 4-35 Logic Level (DTL) Input, Wiring Diagram

4.6.4 Mercury-Wetted Relay Contact Signal Conditioning

All M800 series functional modules contain 16 mercury-wetted relay outputs. These modules are used for load switching purposes. The contact life expectancy, which can exceed 22 billion operations, depends largely on the use of proper contact protection. Contact protection is required if the contacts are expected to handle energy levels in excess of 40 microjoules. This may be represented by the stored energy of a series inductance just prior to opening its circuit or that in a shunt capacitance immediately prior to closing the discharge circuit. In order to handle this and larger energy levels, the following maximum rates of voltages and current rises have been set.

a. When the contacts close a circuit, the rate of current increase should not exceed 25A/μs.

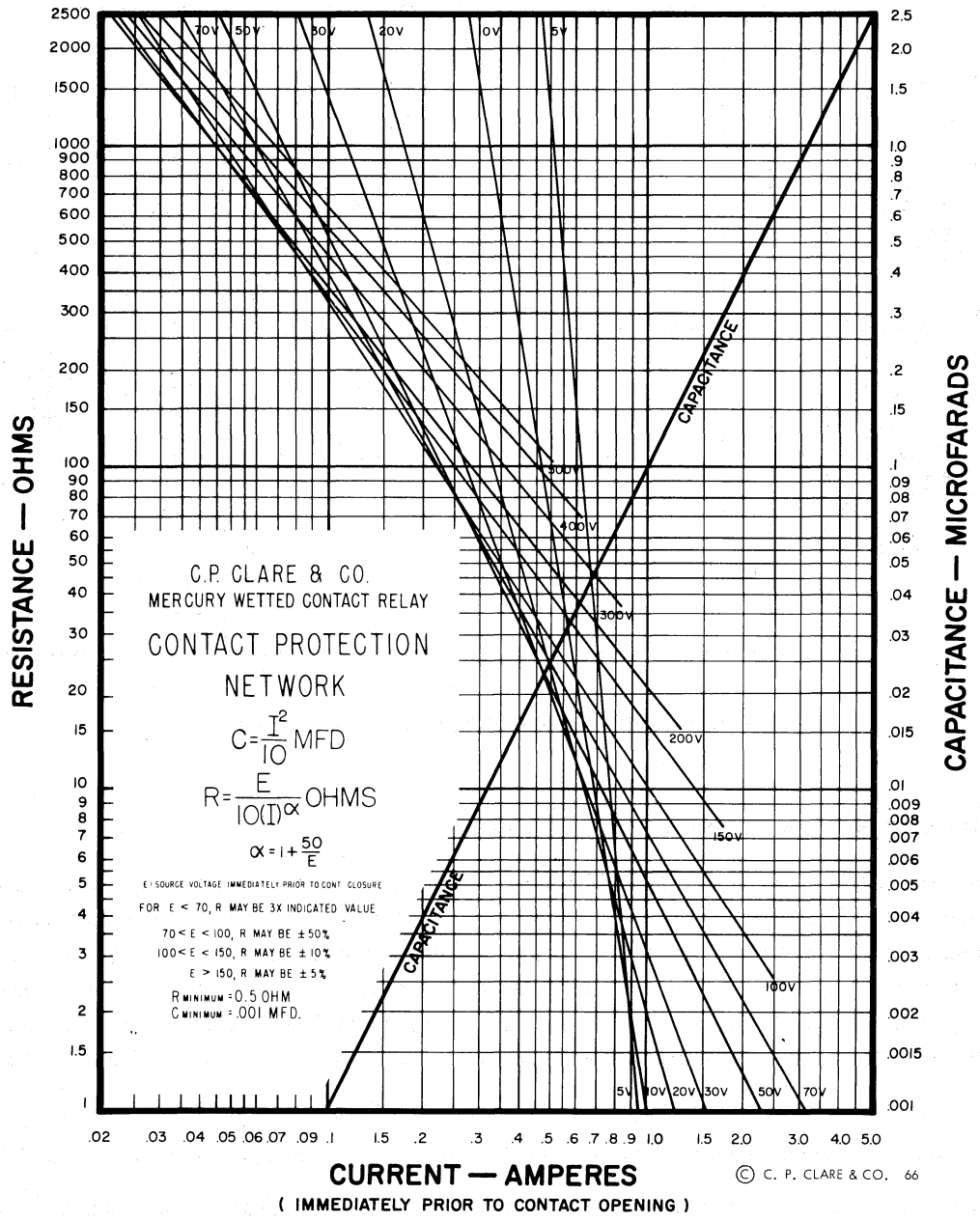
b. When the contacts open a circuit, the rate of change of voltage increase should not exceed 5V/μs.

The arc suppression circuit must bring the rate of current increase and the rate of change of voltage increase to the levels specified above. The arc suppression network comprises a series R-C network across the relay contacts.

4.6.4.1 Location of the Arc Suppression Network – Space is provided on the W400 and W402 Signal-Conditioning Modules for the R-C arc suppression network. The resistor should be installed in field *F* and the capacitor in field *G* (Figures 4-29 through 4-32 and Figures 4-50 and 4-53).

4.6.4.2 Determination of R-C – The values of R and C for resistive loads can be determined by using the nomograph and formula presented in Figure 4-36. This nomograph can also be used for reactive loads. However, further transient protection may be required as discussed in the following paragraphs.

4.6.4.3 Load Consideration – The nature of the load must be carefully considered, especially if the contacts are expected to switch the load current. The types of loads discussed in the following paragraphs are commonly used.



How to Use Nomograph

This nomograph affords a convenient means of determining the necessary contact protection. To determine C, the value of load current is found on the CURRENT axis. Reading directly up to the sloping capacitance line, the value of C is determined from the right hand CAPACITANCE scale. To determine R, read directly up from the load current value to its intersection with appropriate load voltage line. The value of R is then read from the left hand RESISTANCE scale. For AC loads, peak values of current and voltage must be used.

Figure 4-36 Contact Protection Network Nomograph

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Resistive Loads

Proper arc suppression for resistive loads is relatively easy to accomplish. The values for R and C as determined by the use of the nomograph and formula will usually provide adequate protection. However, if long lines are run to the load, line inductance may become significant and transient protection may be required.

NOTE
Use peak values in calculating R and C when ac power is used for load switching.

Inductive Loads (dc)

A voltage transient is generated whenever the mercury-wetted relay contacts open and interrupt the current flow in an inductor. At the instant the contacts open, the inductor behaves like an energy source with a high impedance load into which it can dissipate its energy. The high impedance load takes the form of the opening contacts. The voltage across the high impedance load (the contacts) immediately rises to whatever value is necessary for an arc-over to occur, thereby dissipating the energy stored in the inductor. The design objective for this load is to provide control on the rate of current and voltage rise and suppress or limit the voltage transient so that it remains within the contact ratings. Since the volt-second area under the transient curve will remain constant, the proper transient protection for a given application will depend on how long the transient voltage can remain. Effects and characteristics of arc suppression circuits are illustrated in Figure 4-37.

In Part A, having no arc suppression, damage will occur to the mercury-wetted relay contacts due to the rate of rise of voltage and the voltage transient exceeding the contact rating specifications.

In Part B, the rate of rise is controlled but the transient still exceeds the contact rating specification.

Safe operation is achieved in Part C when both the rate of rise and the transient are controlled.

Inductive Loads (ac)

Arc suppression for ac inductive loads is difficult to determine by calculation due to the complex nature of the mathematics. It is usually easier to use a bench test setup to identify transients and choose the appropriate values for R and C of the suppression circuit. One technique that is useful for extreme loads (above 100 Vac) is to place the main R-C arc suppression circuit across the load as shown in Figure 4-38.

This alleviates the problem of ac leakage current through an R-C arc suppressor that is in parallel with the contacts. But, this technique may result in a condition that exposes the contacts to voltage transients having a rate of rise in excess of 5V/μs due to the inductance of the field wiring. A secondary arc suppressor, R2-C2, must then be installed in parallel with the contacts. Since C2 need only be one-hundredth of the calculated value, the ac leakage is markedly reduced.

An alternate method for protecting the contacts under extreme load conditions is to use a thyristor in parallel with the traditional arc suppression circuit across the contacts as shown in Figure 4-39. All arc suppression components can then be placed in the arc suppression fields (F and G) of the signal-conditioning modules (W400 and W402).

Capacitive Loads

Since capacitors appear as short circuits when power is switched into them and as high energy sources when power is switched out of them into low impedances, current transients can produce problems. The design objective in protecting mercury-wetted relay contacts is to limit the rate of current increase when the contacts close and also

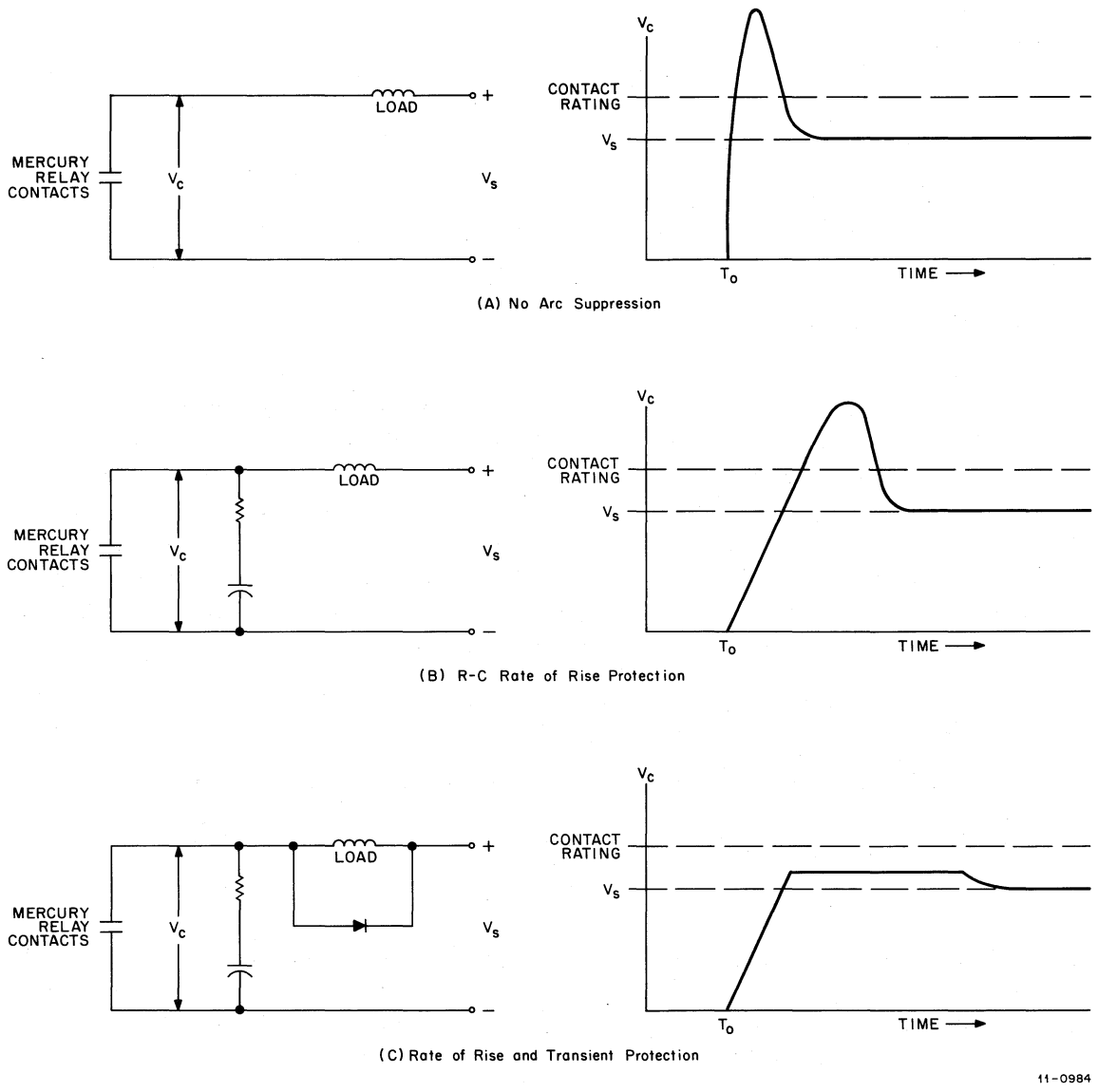


Figure 4-37 Arc Suppression Circuit Characteristics

to limit the absoulte current so as not to exceed contact specifications. The simplest way to obtain this protection is illustrated in Figure 4-40.

4.6.5 Driver Output Signal Conditioning

All M600 series functional modules contain 16 buffered open-collector driver output stages for driving loads. The W403 Signal-Conditioning Module must be used as the interface between the field devices and the driver output modules. Diode suppression for inductive loads is included

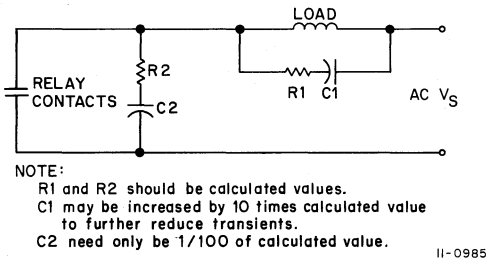


Figure 4-38 Arc Suppression for Extreme Inductive Loads

on the driver output modules; therefore, no external suppression circuit is required. The signal-conditioning module is designed to accommodate both common and isolated field power applications. The only difference between common and isolated power configurations is in the way the loads are connected to the screw terminals. Figures 4-41 through 4-44 illustrate the wiring techniques.

The M600 series functional modules can also be used to drive T^2L logic because the driver collectors are returned to +5V through a diode and resistor. Again, only the W403 Signal-Conditioning Module can be used as the interface. The wiring technique for this application is illustrated in Figure 4-45.

NOTE

For driver output and logic level output configurations described above, field power is not isolated from UDC power as for load switching, contact sensing, and logic level sensing configurations described previously.

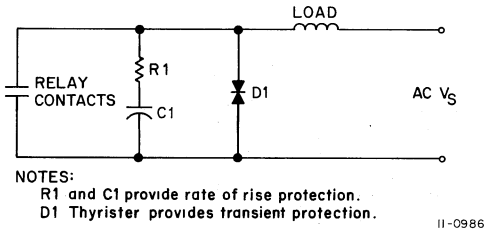


Figure 4-39 Alternate Arc Suppression for Extreme Inductive Loads

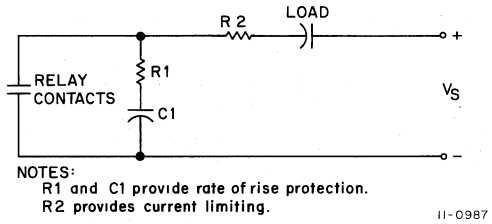


Figure 4-40 Arc Suppression for Capacitive Loads

4.6.6 DAC Module Signal Conditioning

The A633 DAC Module contains four digital-to-analog converters. Four different signal conditioning modules are available for interfacing the field devices with the DAC module. They are:

Module Type	Output Characteristics
A233	0V to +10V @ 15 mA maximum
A234	+1V to +5V @ 15 mA maximum
A235	4 mA to 20 mA, 750Ω maximum
A236	10 mA to 50 mA, 300Ω maximum

The four outputs from the signal-conditioning module are single-ended outputs (Figure 4-46). Therefore, the loads should be of the type that can be grounded to the analog ground, which in turn is connected to system ground in the UDC. Modules A234, A235, and A236 are factory adjusted, but can be adjusted in the field. Refer to A-SP-BA633-0-4 for the procedure.

NOTE

Loads, including screw terminal wiring, having up to 0.1 μF will not cause instability but will effect settling time.

4.6.7 Counter Module Signal Conditioning

The W734 I/O Counter Module is a 16-bit asynchronous binary counter. The external inputs and outputs include:

a. EN Input
b. CONT Input
c. CV Input
d. $\overline{P}$ Output
e. $\overline{C}$ Output
f. $\overline{S}$ Output

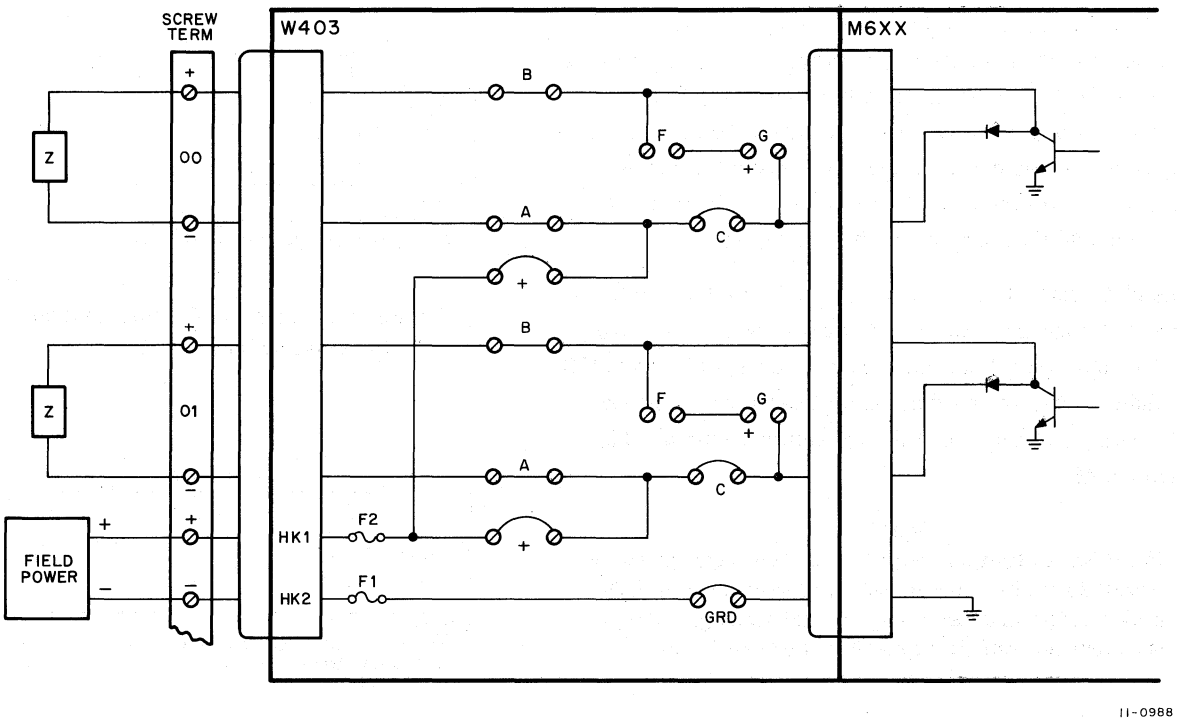


Figure 4-41 Common Power for Driver Output Wiring Diagram

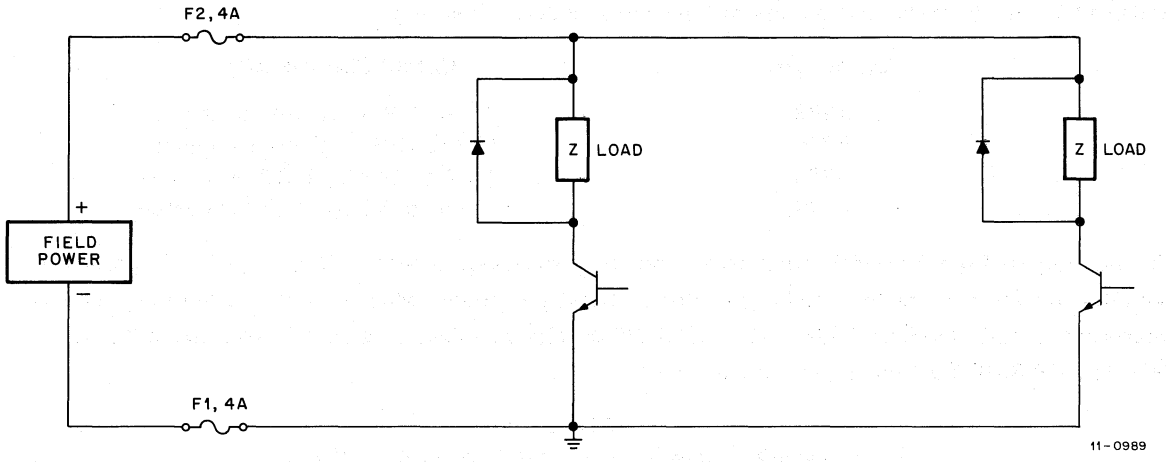


Figure 4-42 Common Power for Driver Output, Schematic Diagram

The W400 Signal-Conditioning Module must be used to interface the field devices (counter inputs and outputs) with the counter. The counter outputs may be connected to accommodate common or isolated field power for driving loads or may be connected to provide logic level outputs (Figures 4-47 through 4-49). No external protection is required for driving inductive loads since diode suppression is included in the counter output circuits.

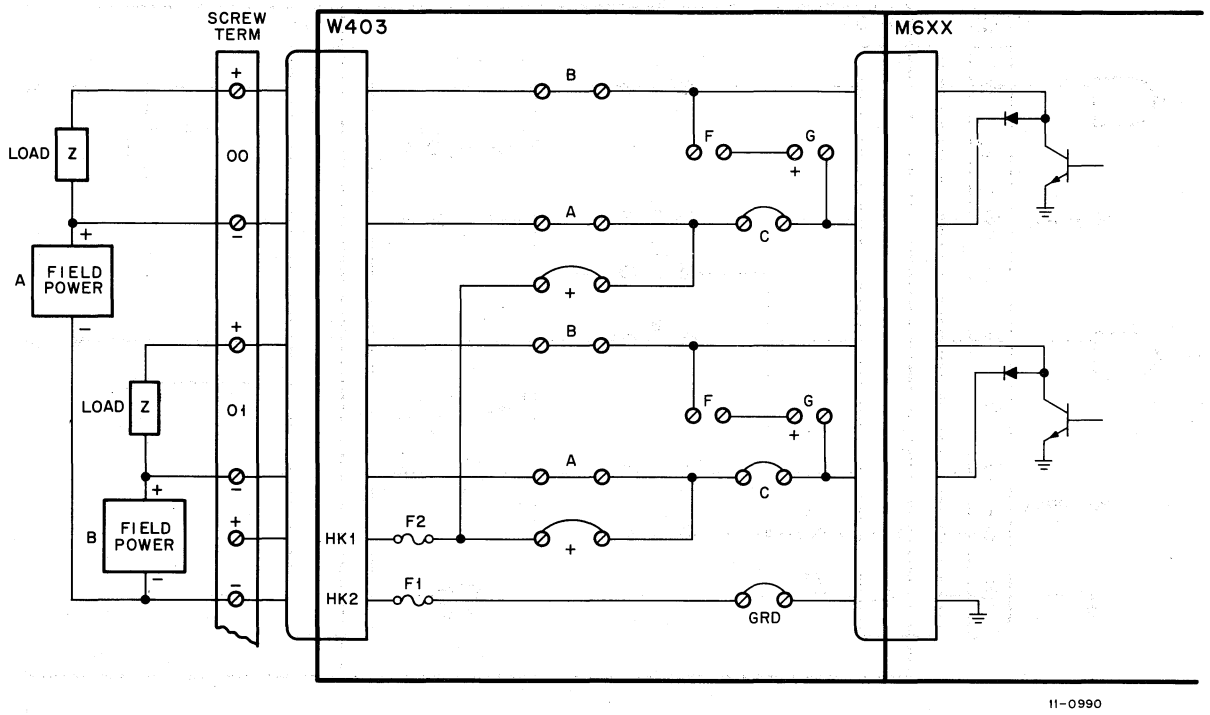


Figure 4-43 Isolated Power for Driver Output Wiring Diagram

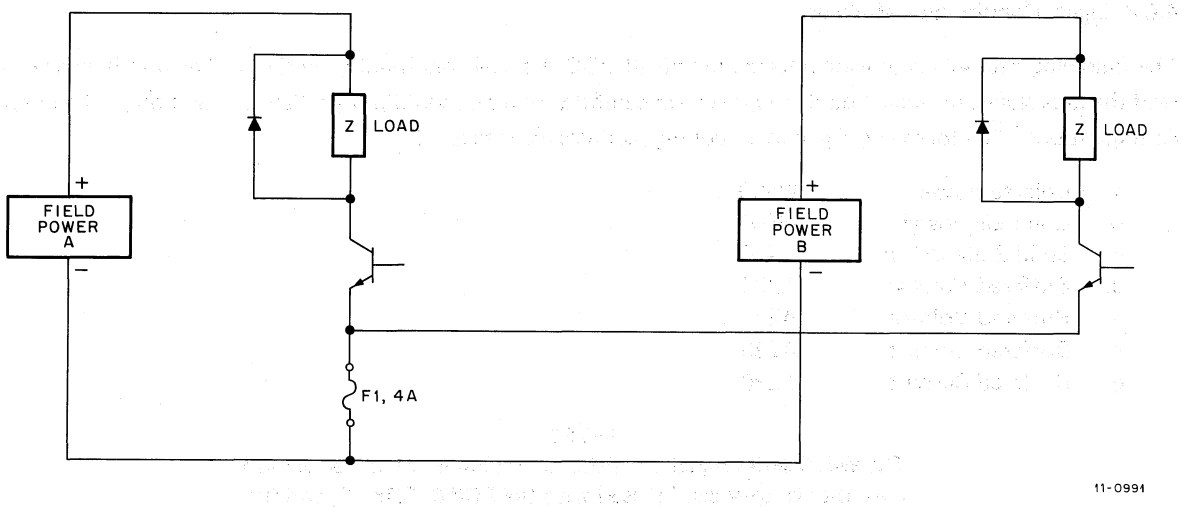


Figure 4-44 Isolated Power for Driver Output, Schematic Diagram

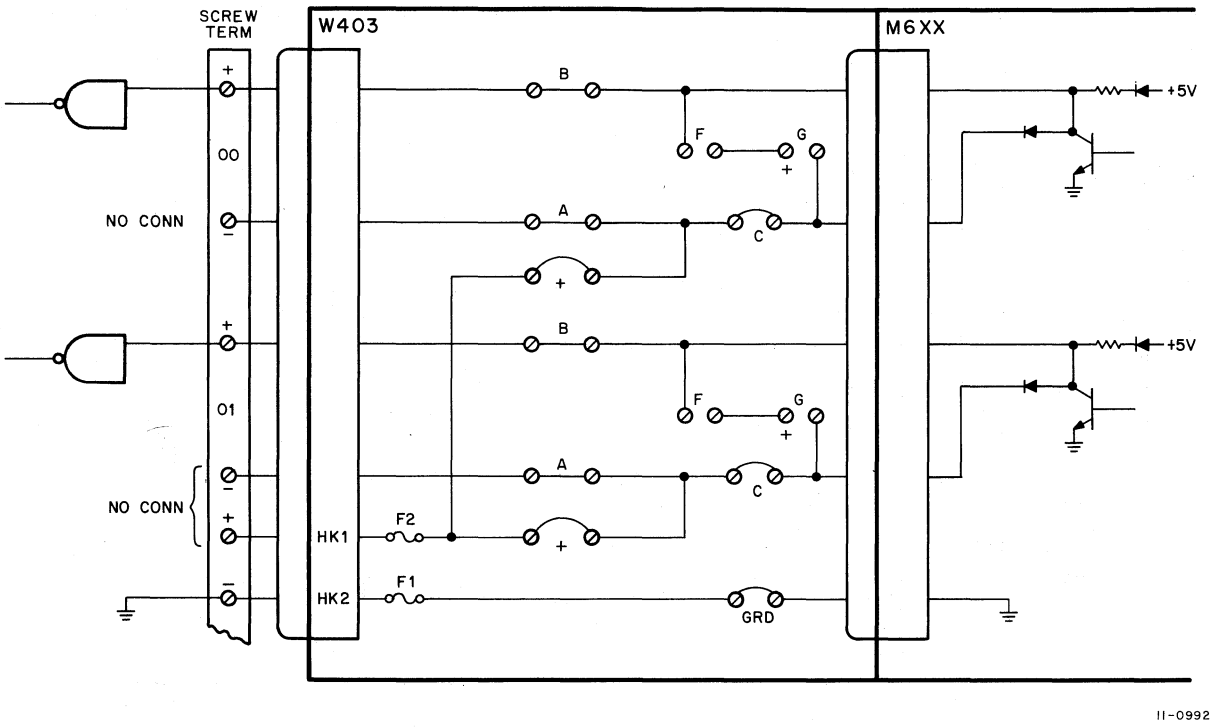


Figure 4-45 Logic Level Output, Wiring Diagram

4.6.8 Signal-Conditioning Modules

The following data sheets provide information on all UDC11 signal-conditioning modules. The user is advised to read the data sheets on each module in his system carefully, and he should pay particular attention to the jumper configurations. The following signal-conditioning modules are discussed:

a.	Isolated Power	W400
b.	Common Power	W402
c.	Solid State Driver	W403
d.	Buffered Voltage	A233
e.	Buffered Voltage	A234
f.	Buffered Current	A235
g.	Buffered Current	A236

NOTE

The W400 series signal-conditioning modules are universal modules, that is, they can be used with the PDP-8, PDP-15, and the PDP-11 UDC device. The bit numbering (placarding) on the modules reflect the numbering conventions used in the PDP-8 and PDP-15. However, the bit numbers associated with the callouts on the photographs in this section reflect the actual PDP-11 numbering convention.

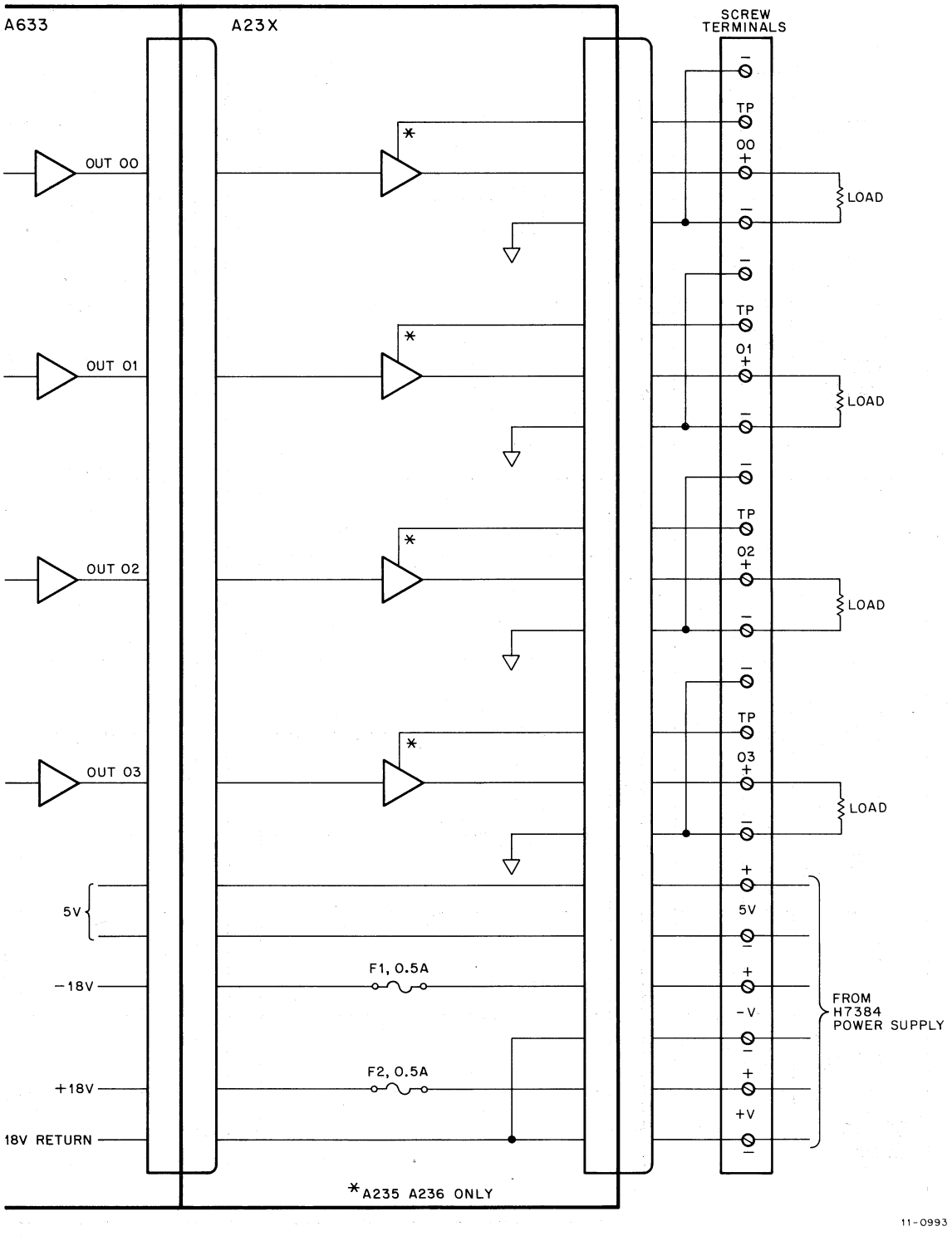


Figure 4-46 DAC Wiring Diagram

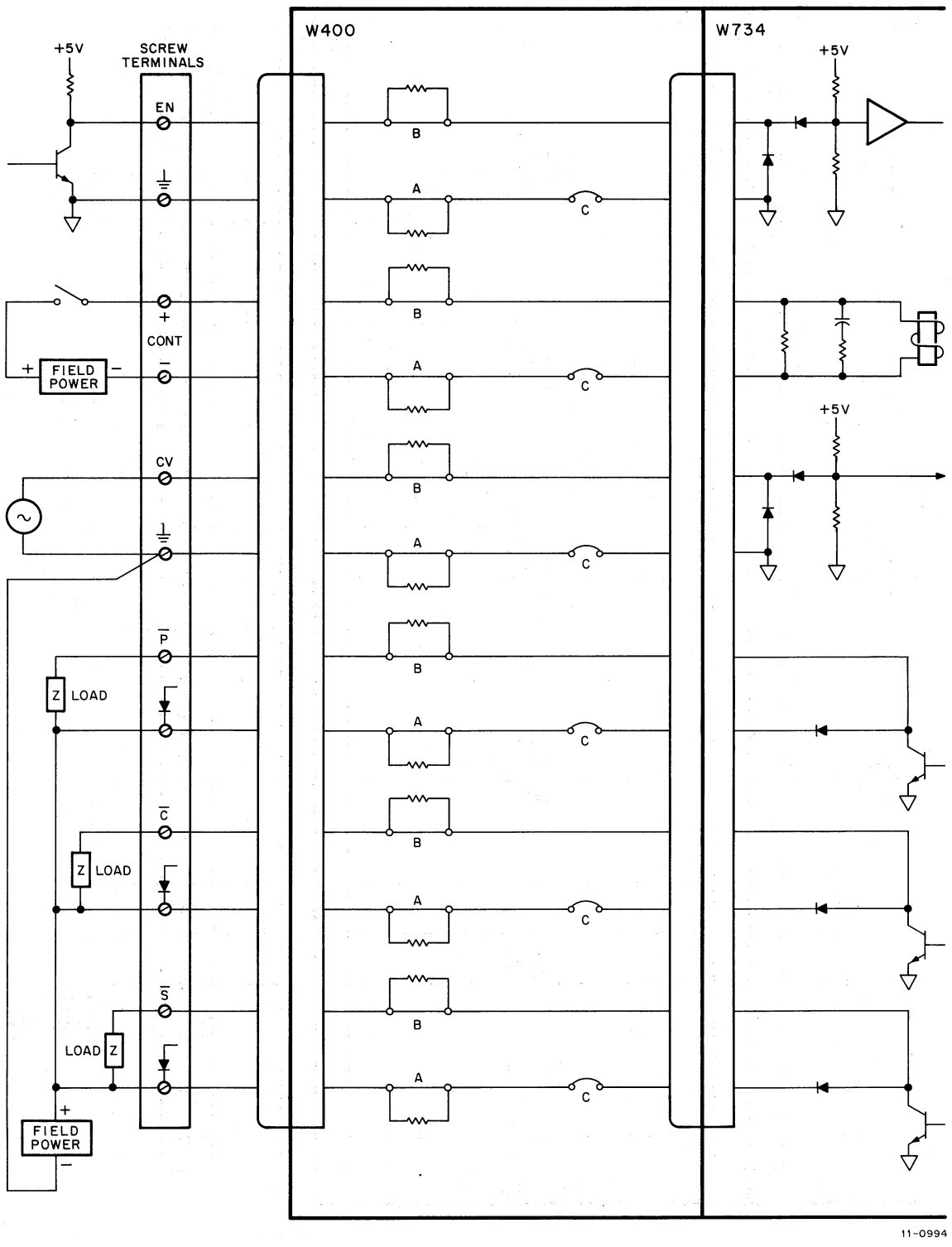


Figure 4-47 Counter Input, and Output (Common Power), Wiring Diagram

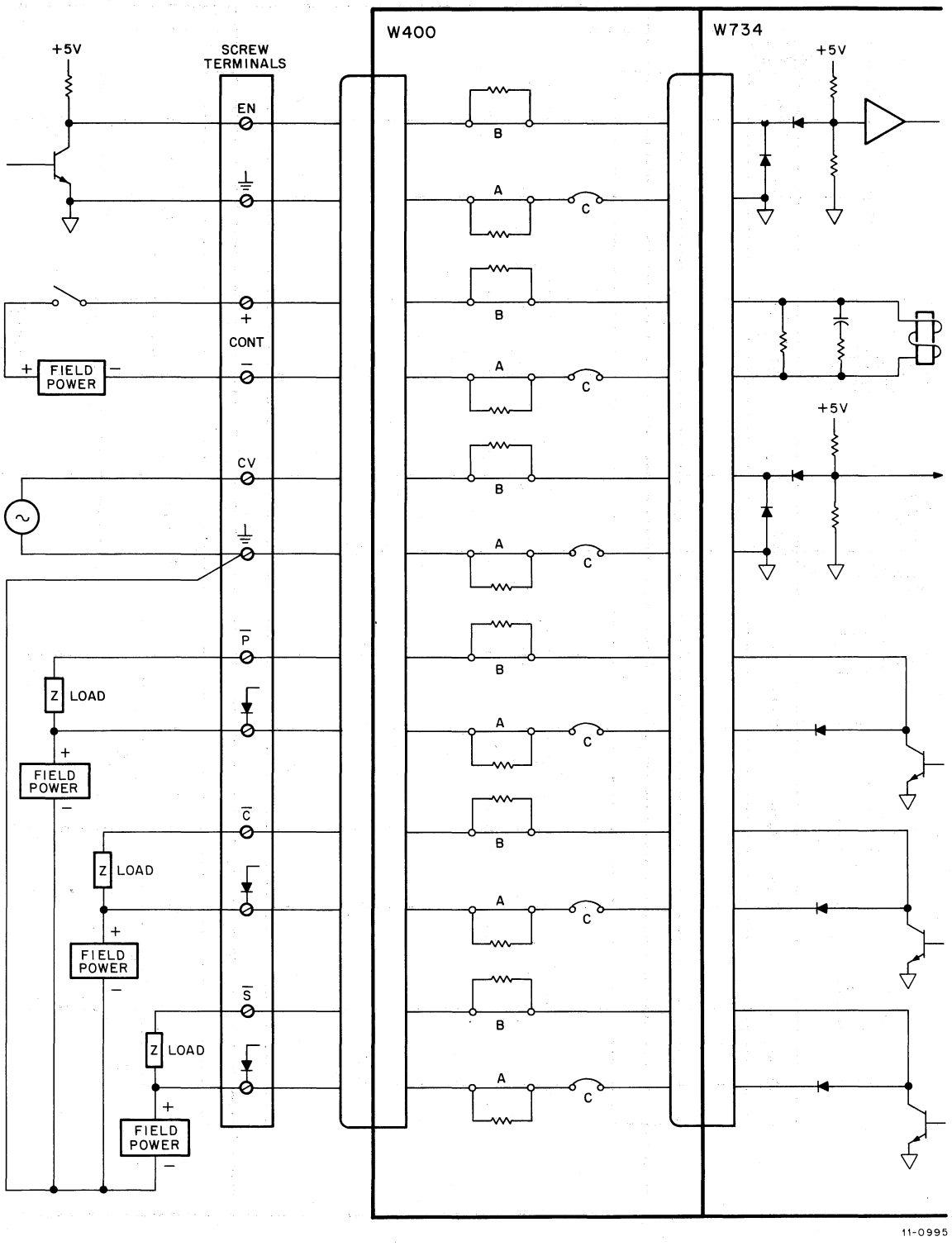


Figure 4-48 Counter Input, and Output (Isolated Power), Wiring Diagram

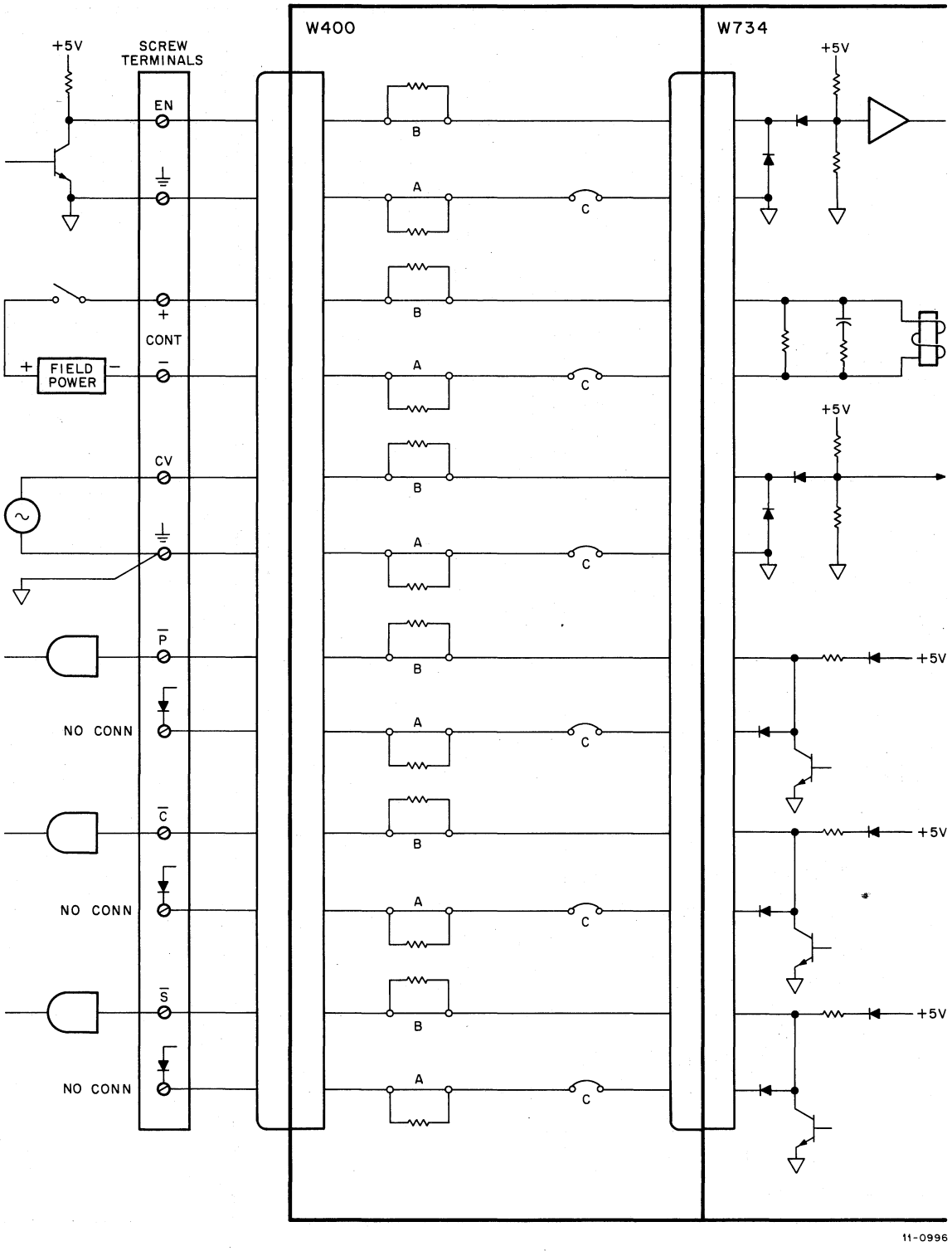


Figure 4-49 Counter Input, and Output (Logic Level), Wiring Diagram

W400
ISOLATED POWER SIGNAL-CONDITIONING MODULE

The isolated power signal-conditioning module (Figures 4-50 and 4-51) is a double-ended module providing the interface between 16 individual points on the functional I/O modules and customer contacts or field signals. Differential pair field wiring from the screw terminals is terminated on a 36-pin connector that connects to the rear of the module.

CAUTION
This module may not be used with Flip-Flop Relay Driver (M685) or Single-Shot Relay Driver (M687) Modules.

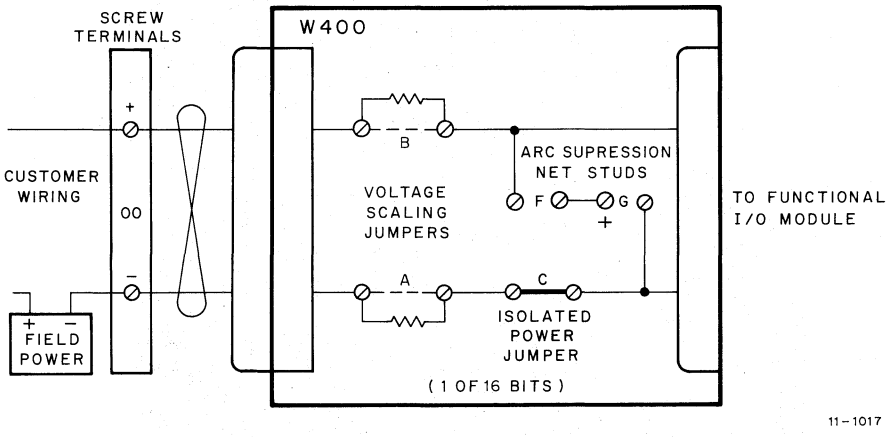


Figure 4-50 Simplified Schematic Diagram (W400)

The isolated power feature is used where each field digital I/O point is supplied with power at the field location. Each pair of control wires is isolated from every other point and from UDC ground.

When used with input modules (Contact Sense, Contact Interrupt), resistor/jumper selection on each circuit scales the field-supplied excitation voltage of 6V, 24V, or 48 Vdc to 6 Vdc at 15 mA per point for proper input circuit operation. The module will be delivered set up for 6V operation.

The mercury-wetted relay contacts of the output single-shot relay, flip-flop relay, and latching relay modules are rated at 2A, 250V (the product not to exceed 100 VA) and require arc suppression. Provision for customer-mounting (split lug fields F and G) of the appropriate RC filter elements for arc suppression for each circuit is provided on the W400 and W402.

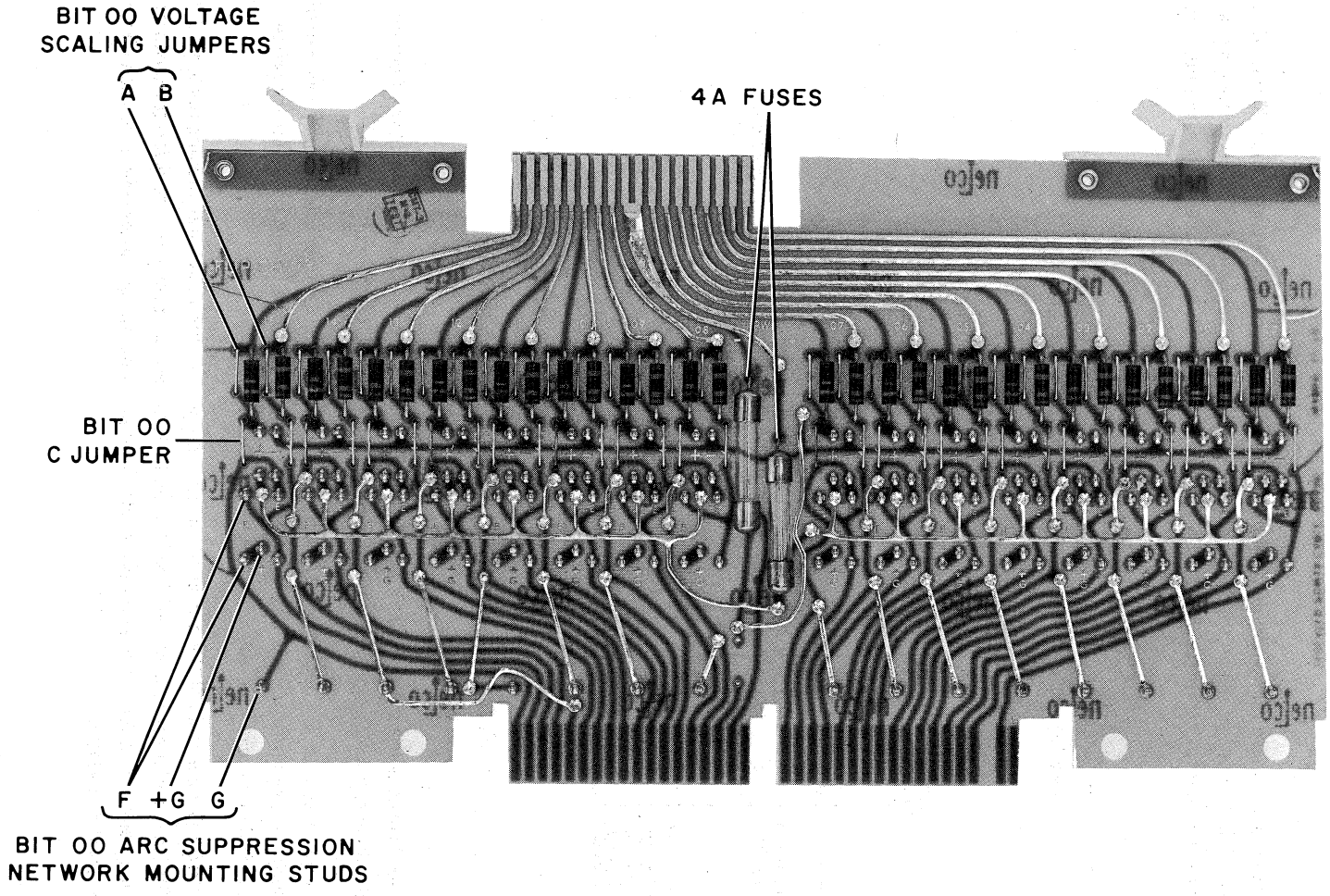


Figure 4-51 Location of Jumpers and Component Mounting Studs (W400)

W402
COMMON POWER SIGNAL-CONDITIONING MODULE

The common power signal-conditioning module (Figures 4-52 and 4-53) is a double-ended module providing the interface between 16 individual points on the functional I/O modules and customer contacts or field signals. Differential pair field wiring from the screw terminals is terminated on a 36-pin connector that connects to the rear of the module.

CAUTION
This module may not be used with M685 Flip-Flop Relay Driver or M687 Single-Shot Relay Driver Modules.

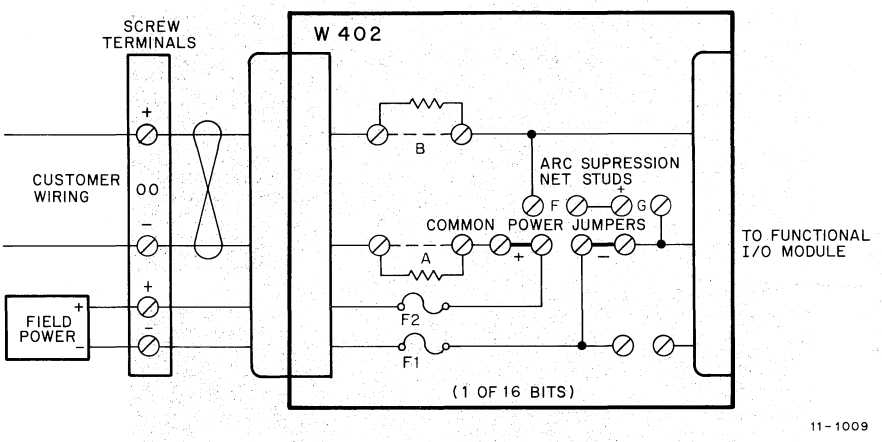


Figure 4-52 Simplified Schematic Diagram (W402)

The common power signal-conditioning module has a power input pair that permits field-supplied excitation or control power to be brought directly to the signal-conditioning module and distributed in parallel (common) to each of the circuits on the functional I/O module. The input is fused for 4A. Therefore, when the combined relay output current exceeds 4A on a module, Module W400 must be used for power distribution and conditioning. When used with input modules (Contact Sense, Contact Interrupt), resistor/jumper selection on each circuit scales the field-supplied excitation voltage of 6V, 24V, or 48 Vdc at 15 mA per point for proper input circuit operation. The module will be delivered set up for 6V operation.

The mercury-wetted relay contacts of the output single-shot relay, flip-flop relay, and latching relay modules are rated at 2A, 250V (the product not to exceed 100 VA), and require arc suppression. Provision for customer-mounting (split lug fields F and G) of the appropriate RC filter elements for arc suppression for each circuit is provided on the W400 and W402.

In applications where it is desired to demultiplex an output signal, the common power module may be used to distribute this signal to the contacts of a relay output functional module. This eliminates the necessity of jumpering one side of all the output contacts together.

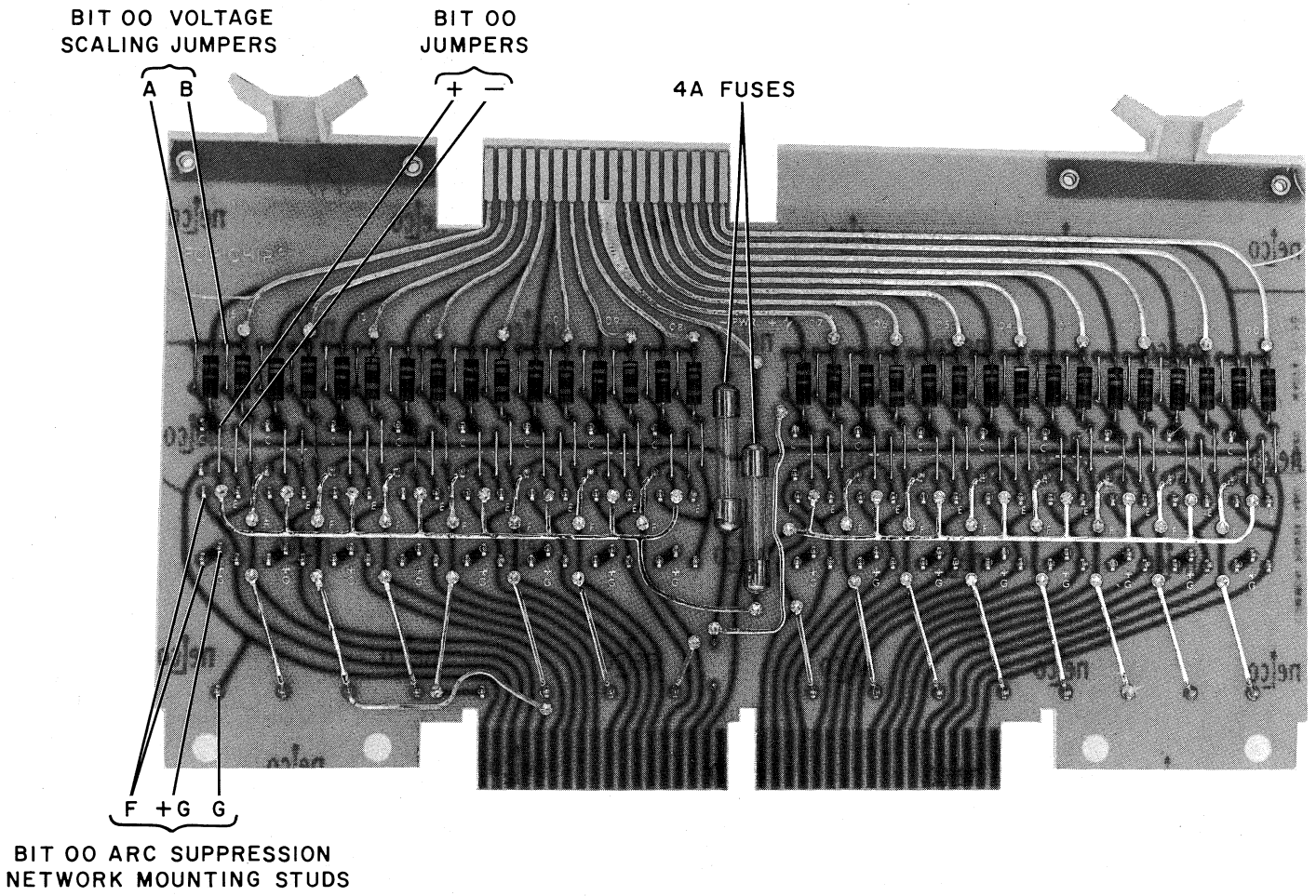


Figure 4-53 Location of Jumpers and Component Mounting Studs (W402)

W403
SOLID STATE DRIVER SIGNAL-CONDITIONING MODULE

This module is a double-ended module providing the interface between 16 individual points on the M685 Flip-Flop Driver or the M687 Single-Shot Driver Output Modules and field circuits (Figures 4-54 and 4-55). Differential pair field wiring from the screw terminals is terminated on a 36-pin connector that connects to the rear of the module. One wire of each pair connects one side of each field load to the open collector switch on the output module. If only logic levels are required, only this line is needed. The other wire of this pair connects the opposite end of the load to a positive common power source. This power is customer-supplied and is brought in to the W403 Module from the BC40C-4 Screw Terminal Assembly, along with the control point pairs. The positive line is distributed to each of the control point pairs. A common return line for all field loads is connected to UDC logic ground. Both positive and negative power loads are fused for 4A.

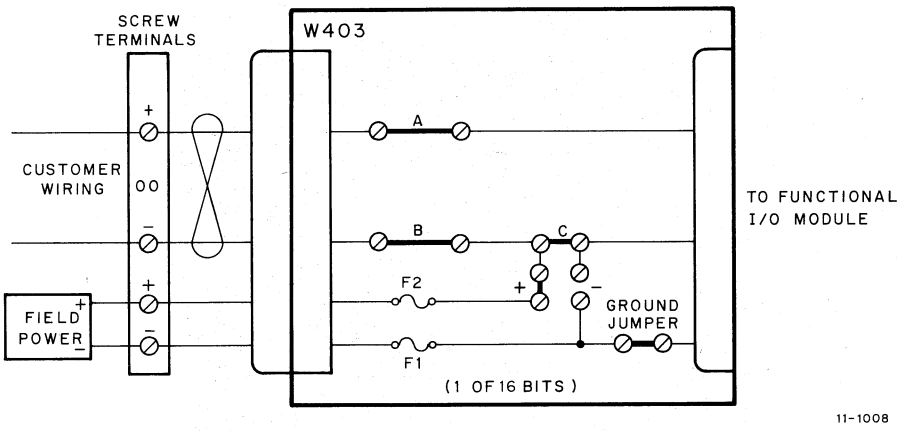


Figure 4-54 Simplified Schematic Diagram (W403)

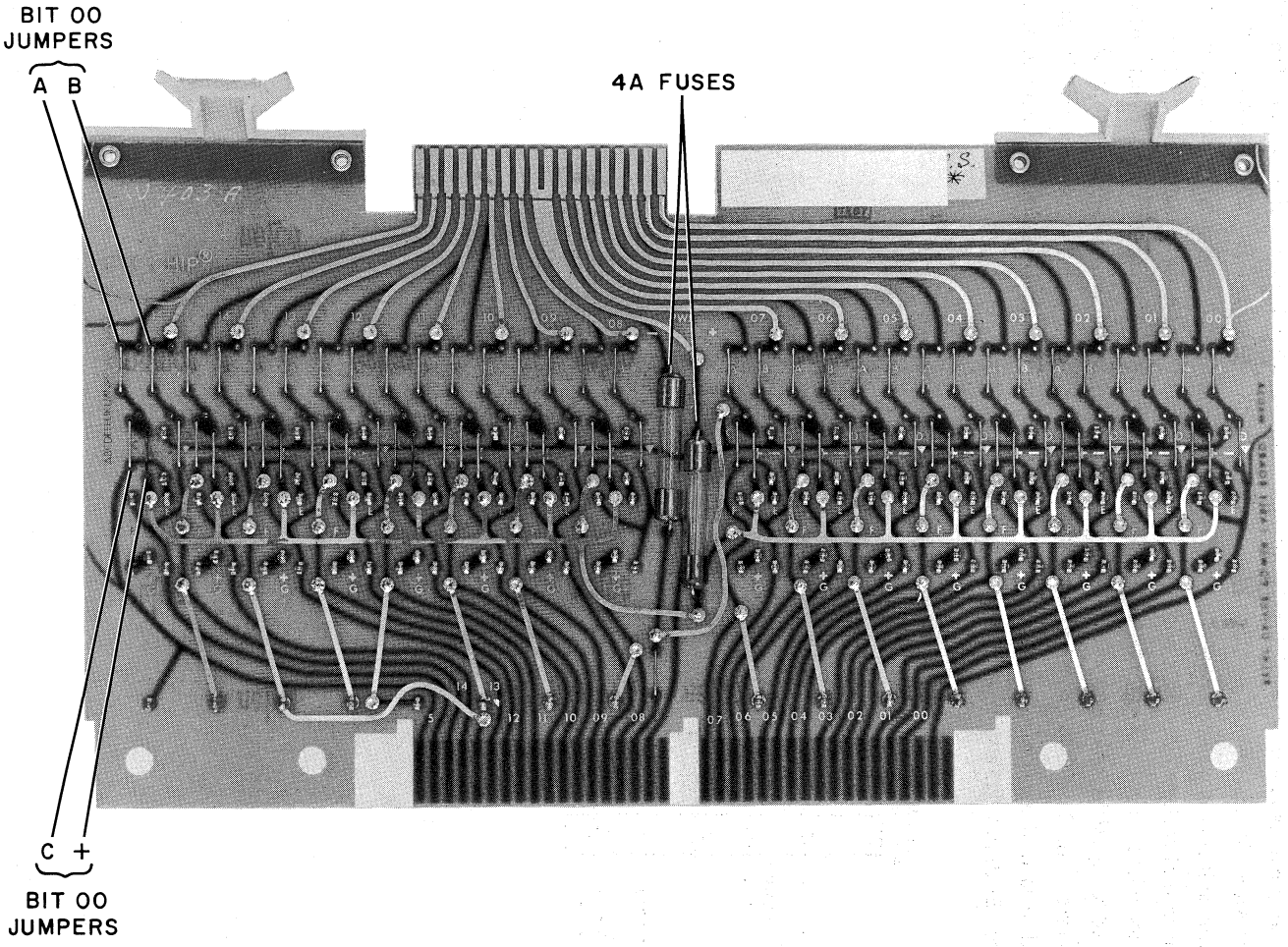


Figure 4-55 Location of Jumpers (W403)

A233
BUFFERED VOLTAGE SIGNAL-CONDITIONING MODULE

FUNCTIONAL SPECIFICATIONS

Analog output:	0 to +10V at 15 mA maximum (see below)
Gain linearity:	-1 ± 0.05%
Zero input offset:	6 mV maximum
Settling time:	35 μs maximum to within ± 0.05% of final value with 150 pF load. 50 μs with DAC A633
Power:	+18V ± 0.05V, 45 mA maximum plus load current -18V ± 0.05V, 45 mA maximum Power is supplied from an external H738A supply and applied through the screw terminals (BC40C Cable Assembly).

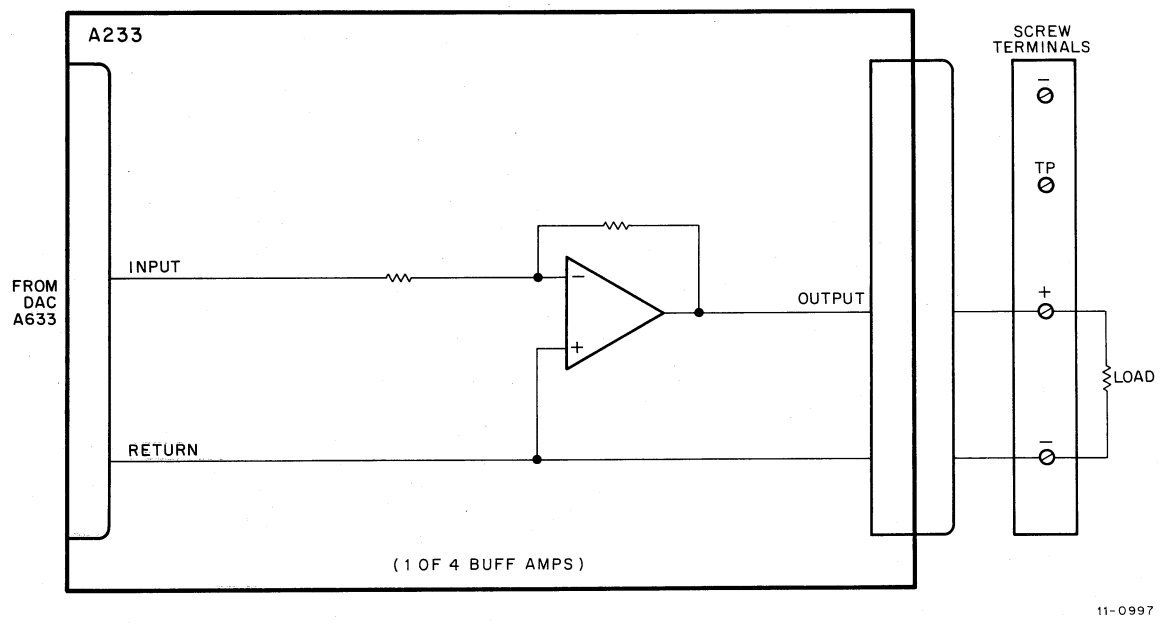


Figure 4-56 Simplified Schematic Diagram (A233)

DESCRIPTION

The A233 Buffered Voltage Signal-Conditioning Module (Figure 4-56) contains four buffered voltage amplifier circuits. This module is used as a signal-conditioning module for the A633 DAC Module. The amplifiers are simple inverting-type amplifiers with a gain of 1. A current buffer is used to provide up to 15 mA of output current.

A twisted-pair cable is recommended to connect the output from the screw terminals to the load. This cable should be of sufficient wire size to prevent excessive losses along the cable.

DATA FORMAT (Channel 00)

Digital Input to A633	DAC Voltage from A633	Voltage Output at Screw Terminals
000000	0.000V	0.000V
020000	-5.000V	+5.000V
037760	-9.990V	+9.990V

A234
BUFFERED VOLTAGE SIGNAL-CONDITIONING MODULE

FUNCTIONAL SPECIFICATIONS

Analog output:	+1V to +5V at 15 mA maximum (see below)
Gain linearity:	-0.4 ± 0.05%
Zero input offset:	Adjustable to give +1V out
Settling time:	35 μs maximum to within ±0.05% of final value with 150 pF load. 50 μs with DAC A633.
Power:	+18V ± 0.05V 48 mA maximum plus load current -18V ± 0.05V 48 mA maximum Power is supplied from an external H738A supply and applied through the screw terminals (BC40C Cable Assembly).

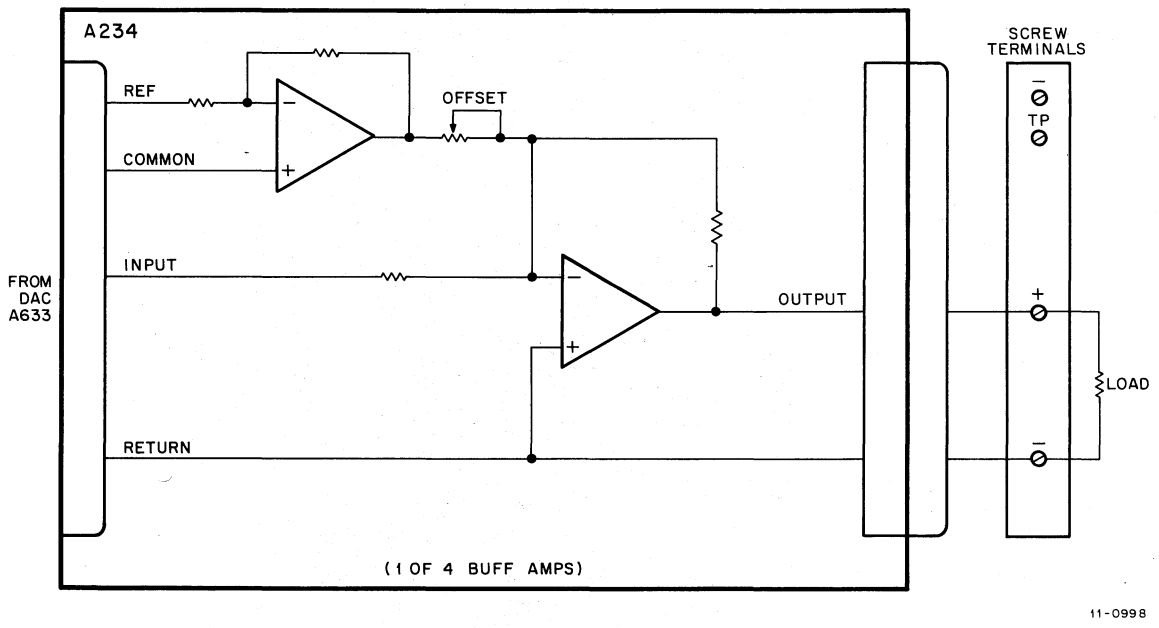


Figure 4-57 Simplified Schematic Diagram (A234)

DESCRIPTION

The A234 Buffered Voltage Signal-Conditioning Module (Figures 4-57 and 4-58) contains four buffered voltage amplifier circuits. This module is used as a signal-conditioning module for the A633 DAC Module. The amplifiers are inverting-type amplifiers with individual offset adjustments. A current buffer is used to provide up to 15 mA of output current.

A twisted-pair cable is recommended to connect the output from the screw terminals to the load. This cable should be of sufficient wire size to prevent excessive losses along the cable.

DATA FORMAT (Channel 00)

Digital Input to A633	DAC Voltage from A633	Voltage Output at Screw Terminals
000000	0.000V	+1.000V
020000	-5.000V	+3.000V
037760	-9.990V	+4.996V

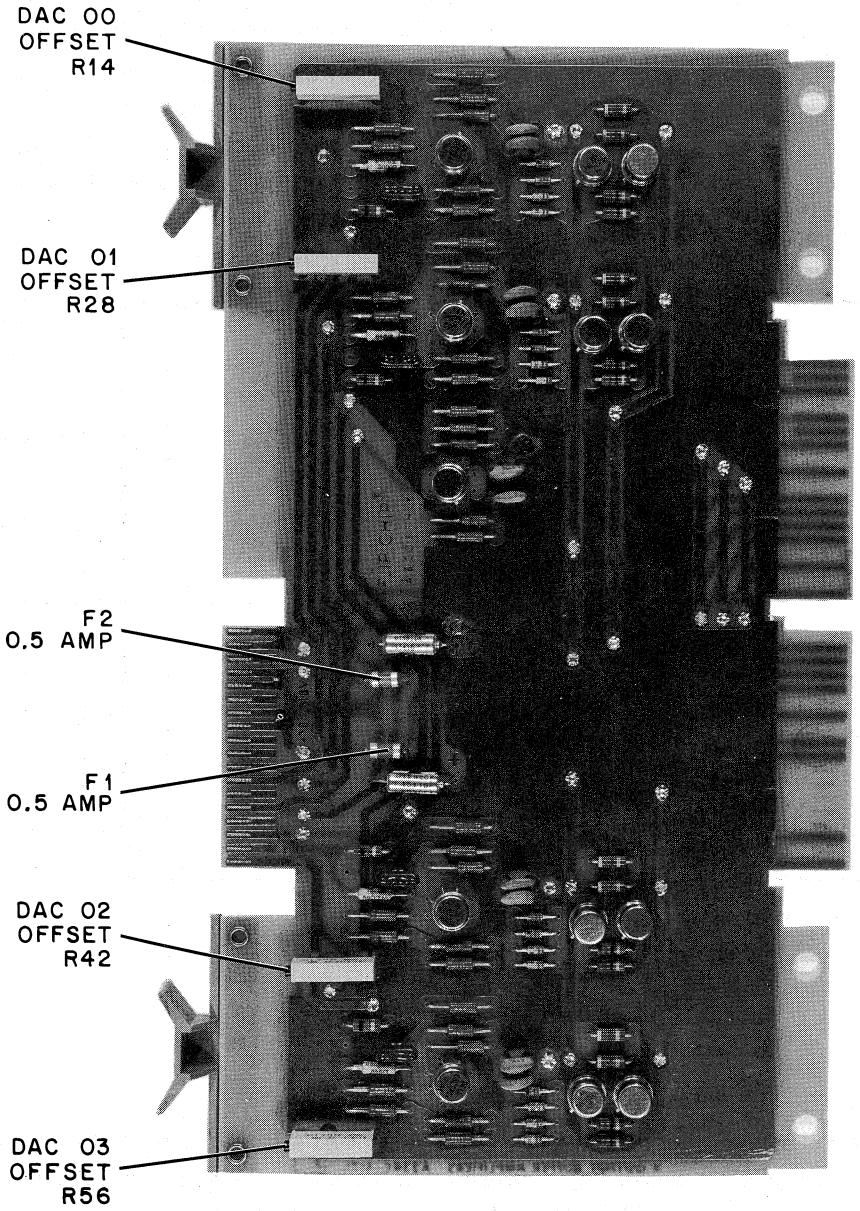


Figure 4-58 Location of Adjustments and Fuses (A234)

A235
BUFFERED CURRENT SIGNAL-CONDITIONING MODULE

FUNCTIONAL SPECIFICATIONS

Analog output:	+4 mA to +20 mA into 750Ω maximum (see below)
Zero input offset:	Adjustable to give +4 mA out.
Settling time:	35 μs maximum to within 0.05% of final value with 150 pF capacitor across the load. 50 μs with DAC A633.
Linearity:	⩾99.95%
Power:	+18V ± 0.05V 126 mA maximum -18V ± 0.05V 46 mA maximum Power is supplied from an external H738A supply and applied through the screw terminals (BC40C Cable Assembly).

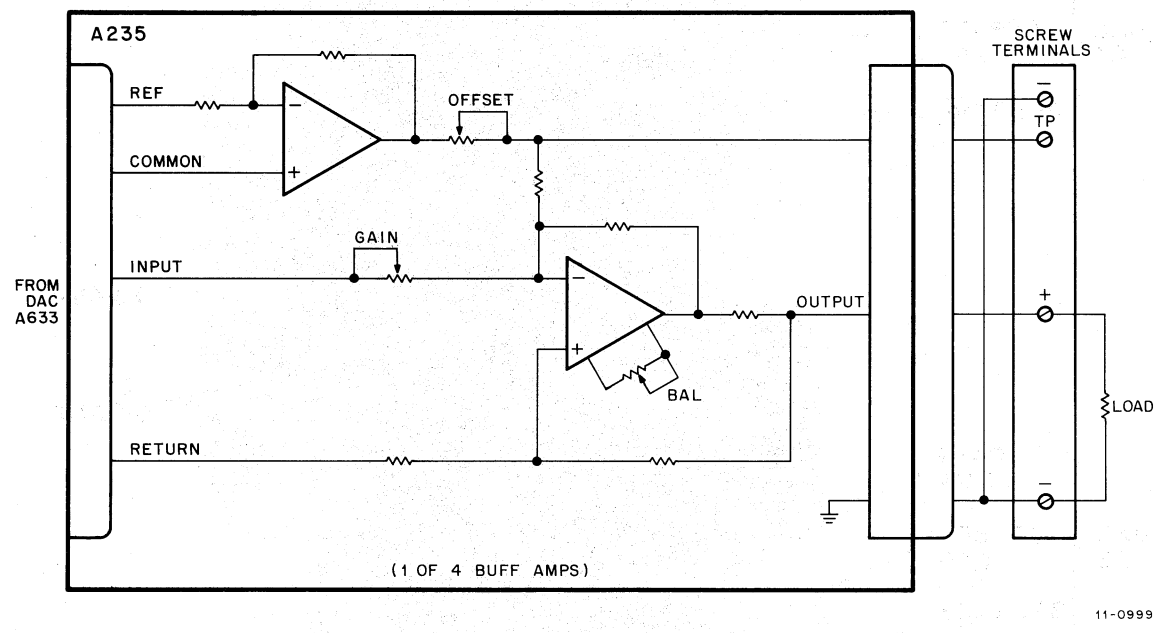


Figure 4-59 Simplified Schematic Diagram (A235)

DESCRIPTION

The A235 Buffered Current Signal-Conditioning Module (Figures 4-59 and 4-60) contains four current source circuits. The module is used as a signal-conditioning module for the A633 DAC Module. The output current is directly proportional to the voltage from the A633 DAC, but is offset by +4 mA. The maximum load that will not cause saturation is 750Ω.

A twisted-pair cable is recommended to connect the output from the screw terminals to the load. This cable should be of sufficient wire size to prevent excessive losses along the cable. The resistance of the cable must be included as part of the load.

DATA FORMAT (Channel 00)

Digital Input to A633	DAC Voltage from A633	Current Output at Screw Terminals
000000	0.000V	+ 4.000 mA
020000	-5.000V	+12.000 mA
037760	-9.990V	+19.984 mA

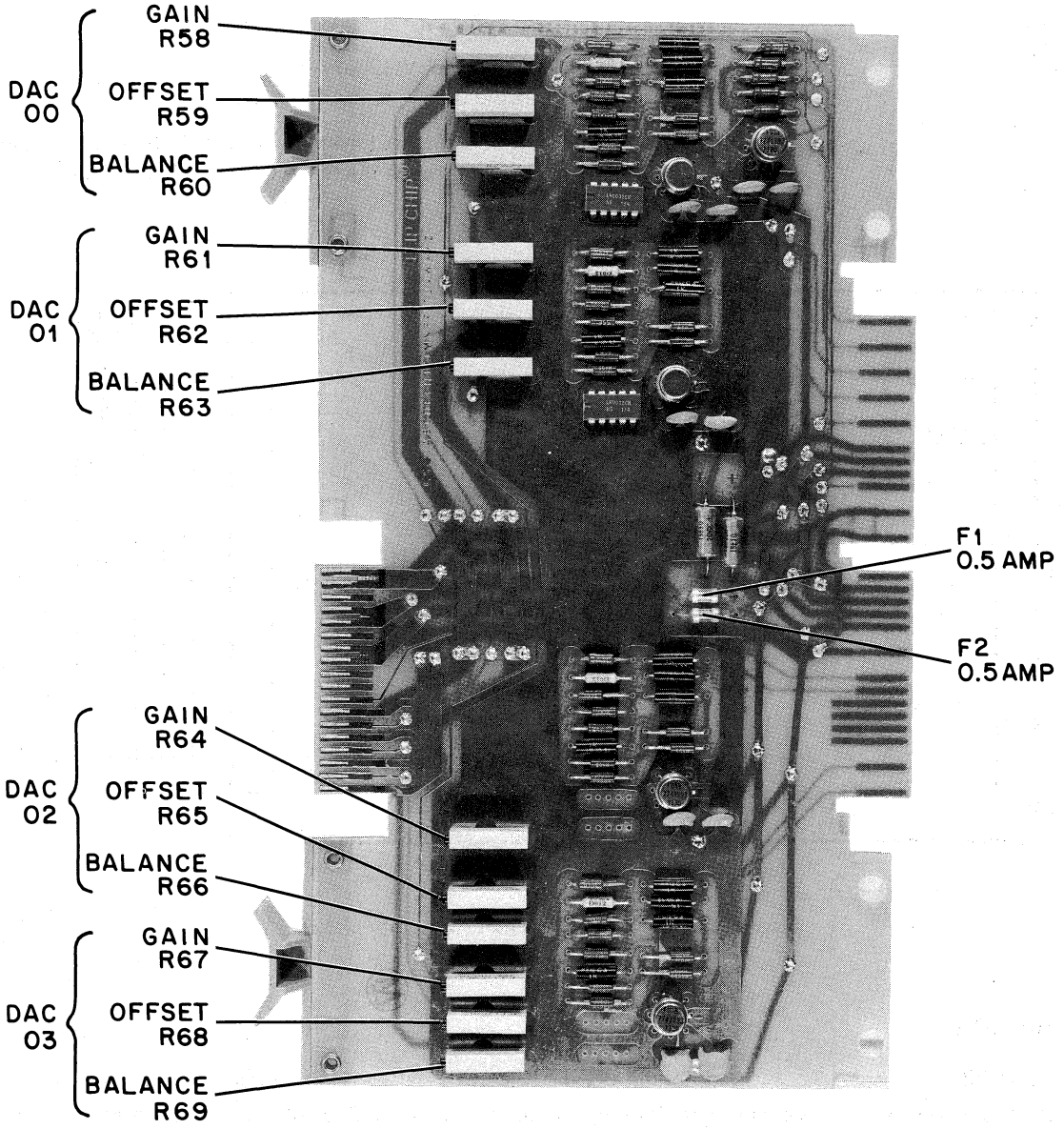


Figure 4-60 Location of Adjustments and Fuses (A235)

A236
BUFFERED CURRENT SIGNAL-CONDITIONING MODULE

FUNCTIONAL SPECIFICATIONS

Analog output:	+10 mA to +50 mA into 300Ω maximum (see below)
Zero input offset:	Adjustable to give +10 mA out.
Settling time:	35 μs maximum to within 0.05% of final value with 150 pF capacitor across the load. 50 μs with DAC A633
Linearity:	⩾99.95%
Power:	+18V ± 0.05V 246 mA -18V ± 0.05V 46 mA Power is supplied from an external H738A supply and applied through the screw terminals (BC40C Cable Assembly).

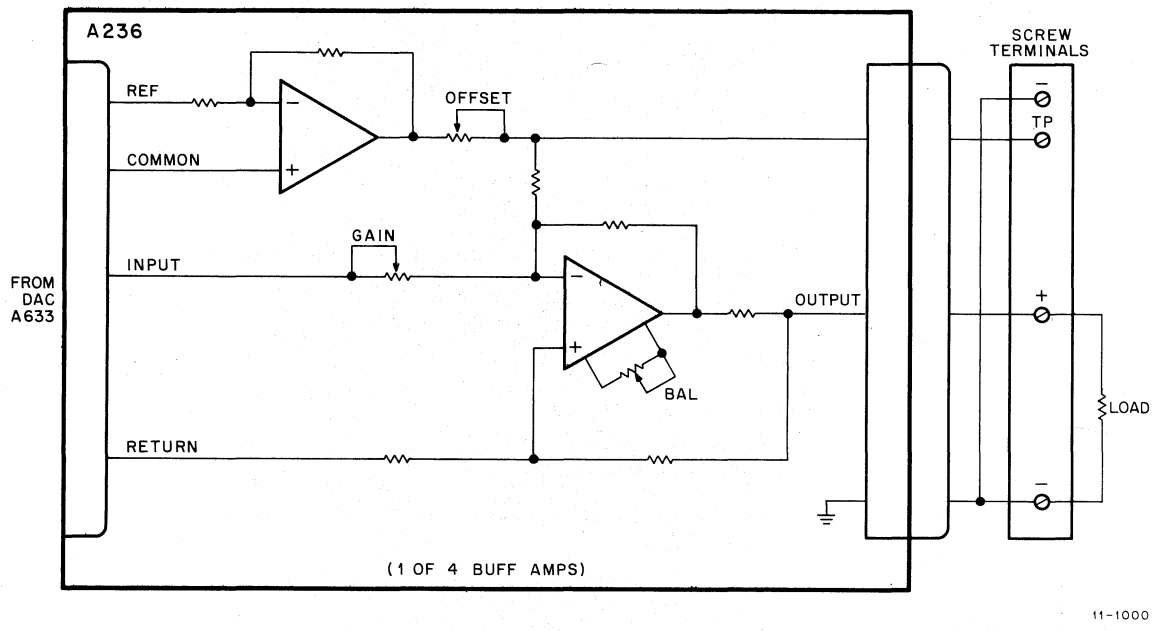


Figure 4-61 Simplified Schematic Diagram (A236)

DESCRIPTION

The A236 Buffered Current Signal-Conditioning Module (Figures 4-61 and 4-62) contains four current source circuits. The module is used as a signal-conditioning module for the A633 DAC Module. The output current is directly proportional to the voltage from the A633 DAC, but is offset by +10 mA. The maximum load that will not cause saturation is 300Ω.

A twisted-pair cable is recommended to connect the output from the screw terminals to the load. This cable should be of sufficient wire size to prevent excessive losses along the cable. The resistance of the cable must be included as part of the load.

DATA FORMAT (Channel 00)

Digital Input to A633	DAC Voltage from A633	Current Output at Screw Terminals
000000	0.000V	+10.000 mA
020000	-5.000V	+30.000 mA
037760	-9.990V	+49.961 mA

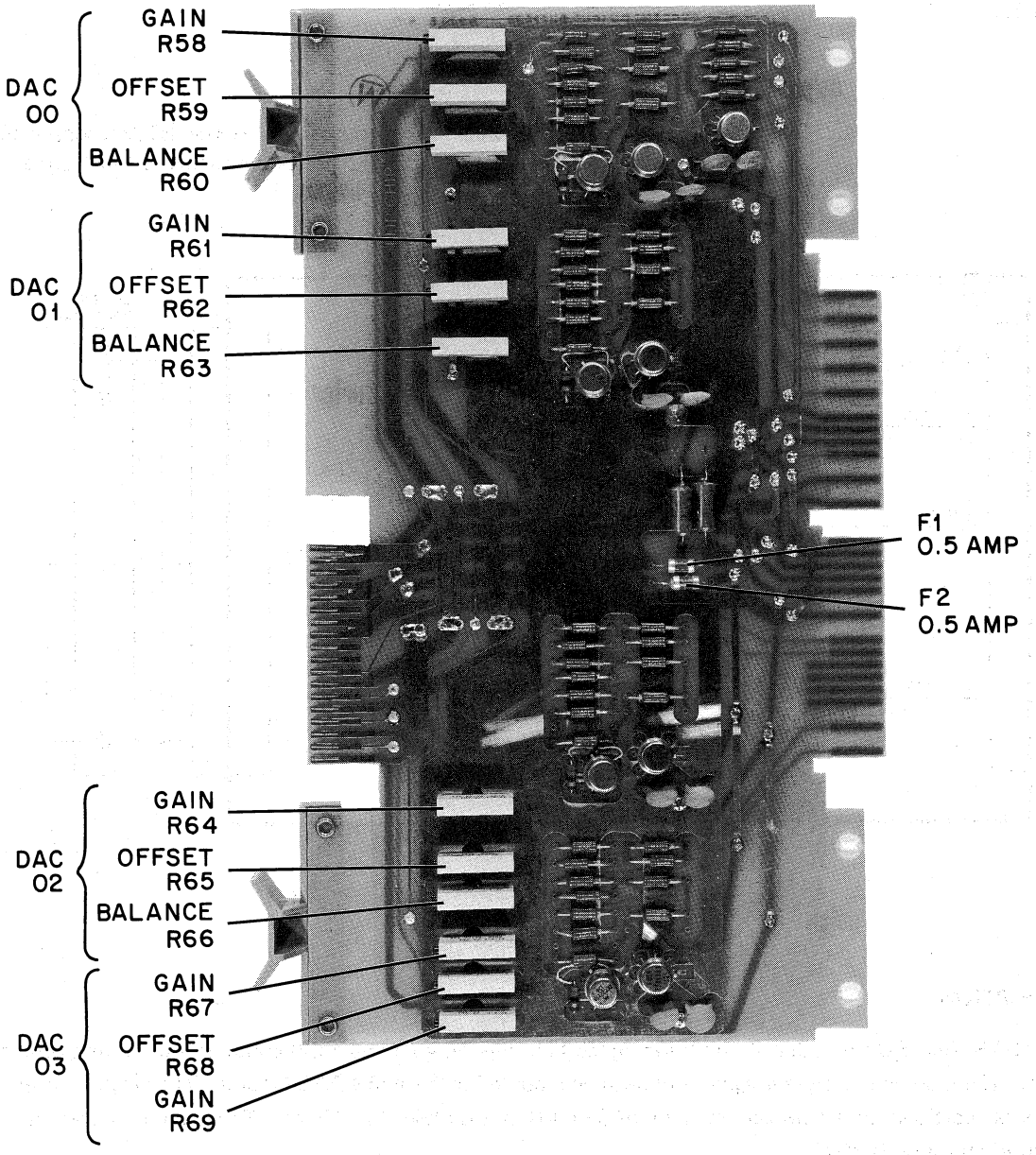


Figure 4-62 Location of Adjustments and Fuses (A236)

4.7 FIELD WIRING

There are certain wiring procedures and practices that are recommended for the proper installation of all lead-in wires connecting remote analog and digital devices with the computer. Deviations from this procedure may introduce unpredictable system errors or inaccuracies because of variables that are unknown and/or uncontrollable. All basic computer accuracies are thus given at the connection cabinet terminals and any inaccuracies caused by lead-in wires must be considered separately.

The field input and output interface circuits have been inherently designed to cope with the majority of adverse industrial plant environments. The design features include such things as:

a. Current rather than voltage sensitive digital inputs for greater immunity to induced voltages.

b. DC isolation between the UDC bus and the individual inputs and outputs.

Although these features allow the user more freedom in his lead-in cable installation, certain special precautions for the various types of inputs and outputs are still necessary for optimum operation.

4.7.1 Wire Specifications

All signal wiring should be individual twisted pairs containing about 6 to 12 twists per foot. Cables should be composed of concentric twisted pairs with all lays and pairs twisted in the same direction for greater flexibility.

Recommended wire sizes, contingent upon compliance with specifications for maximum line impedance and voltage drop, are:

a. No. 16 AWG (4.0Ω per 1000 ft) or equivalent.
b. No. 18 AWG (6.4Ω per 1000 ft) or equivalent.
c. No. 20 AWG (10.1Ω per 1000 ft) or equivalent.

Stranded wire should be used for flexibility. Tinned copper wire is recommended for oxidation resistance. The insulation resistance between conductor and from either conductor to ground should not be less than 500 MΩ per 1000 ft (PVC).

The dielectric strength of the cable and conductor insulation should not be less than 600V. The multi-paired cable should be jacketed in polyvinyl, polyethylene, or teflon at least 0.034 in. thick for mechanical protection. Teflon should be specified for areas where the ambient temperature is expected to be between 105°C (221°F) and 200°C (424°F).

4.7.1.1 Analog Output Wiring – Analog output signals are normally current or high-level voltage signals so that most of the precautions necessary for low level analog signals can be relaxed. Analog output signal wires should be run as twisted pairs and may be run in multi-pair cable if their destinations are common.

4.7.1.2 Digital Input Wiring – Digital input signal wires may be run as twisted pairs and may be run in multi-paired cables. Digital input signals may also utilize 16 input signal wires and one common as long as they are closely associated or twisted together in the same cable. Digital input cable should not be run near ac power cables. Digital input wires may be mixed with digital output wires in the same cable tray. Digital input wires should not be mixed with high-level digital output wires in the same cable.

Pulse type (counter) input wires and edge sensing interrupt-type (alarm) input wires should be run as twisted pairs in a multi-paired digital input cable.

4.7.1.3 Digital Output Wiring – Digital output signal wires should be run as twisted pairs in multi-paired cables containing no analog wires.

Contact closure type (relay) output wires should be run separate from other input and output signal wires in electrostatically shielded multi-twisted pair cables because of the noise producing characteristics of the devices (lamps and relays) that are frequently powered from these outputs. Contact closure type signals are usually made and broken quite suddenly, which can cause high voltage inductive spikes to appear on these lines and any others in close proximity if the driven inductive devices do not have proper suppression.

It is strongly recommended that all ac devices and dc inductive devices incorporate arc suppression circuits to limit noise spikes to less than 2V above the signal level being switched.

Stepping motor driver output wires may be run as twisted pairs or as four wires and a common as long as they are in close proximity or twisted together in the same cable.

4.7.1.4 Grounding – Ideally all grounds should be separated into categories such as power grounds, logic grounds, digital grounds, analog grounds, and relay grounds and each category of grounds run directly to the ground electrode and tied to it at one point only. Practically this is not very feasible so that divisions can be made only as to analog grounds and non-analog grounds.

4.7.2 Installation

Field wiring can be brought into the UDC systems cabinets either from the top or bottom. If the field wiring is brought in through conduit, a space should be provided so that the conduit does not touch the IDACS cabinet.

4.7.2.1 Top Entry – A clamping plate is provided on the top entry version of the cabinet so the leads may be securely clamped to the cabinets. Clamps are not provided by DEC. The plate must be drilled and the clamp secured by a nut, bolt, and lock washer.

The H964MA allows the screw terminals to be set back to accommodate larger and larger bundles of lead. The mounting screws are set on 2 in. centers. It is recommended that the screw terminals be set back 2 in. for each complete file implemented.

4.7.2.2 Bottom Entry – No provision is made for clamping bottom entry cables. As in the top entry, the H964MA must be set back 2 in. per file.

4.7.2.3 Cable Routing Lengths – From a distance 2 in. above the cabinet to the first bend is 12 in. The cable must run 15 in. toward the back of the cabinet to the second bend. It then runs vertically down 6 in. to the bottom of the first screw terminal assembly. A minimum of 16 in. should be allowed to run and dress the longest lead. The screw terminals are mounted on 1-3/8 in. centers, so incremental increases of 1-3/8 in. must be planned for running additional leads.

4.7.2.4 Breakouts – A 2 in. stand-off is provided at each terminal assembly of the mounting screws. These posts provide a means for anchoring the cable and tying off the lead breakouts to the screw terminal assemblies.

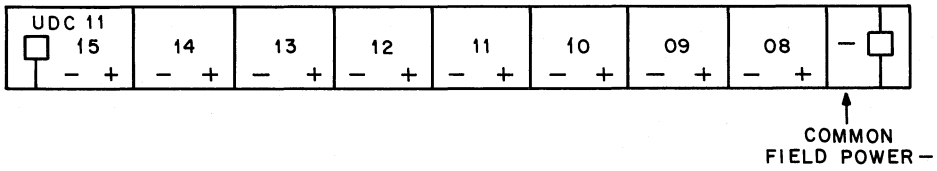
4.7.2.5 Rear Terminal Assemblies – An additional 10 in. is added to the run following the first bend to get to the back of the cabinet. Then a 40 in. vertical run is made to the first breakout. Note where cables of large diameter are formed, it is necessary to add several inches extra for the radius of each bend.

4.7.3 Screw Terminal Markers

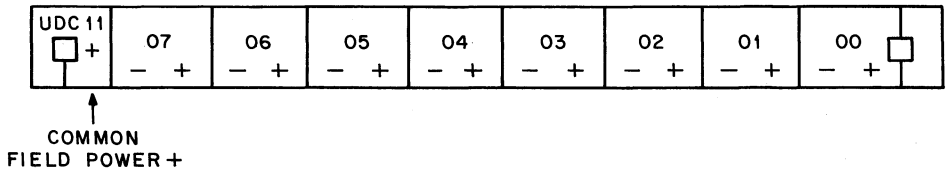
Each screw terminal assembly has 17 pairs of screw terminals. Marker strips are supplied with each UDC system to identify each screw terminal pair. Up to three types of marker strips (in two pieces) may be supplied, one type for each class of I/O modules being utilized. The classes are:

a. Digital I/O
b. DAC
c. Counter

The digital I/O class contains the following modules: W731, W733, W741, W743, M685, M687, M803, M805, and M807. The marker strips to be used for these modules are shown below.



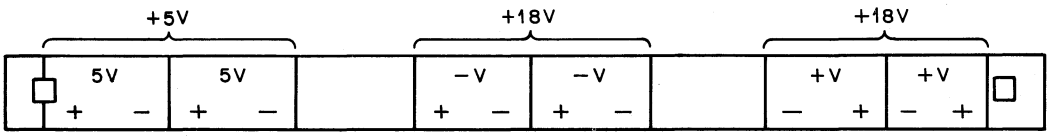
Left Side



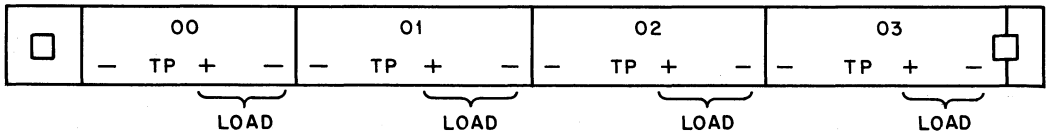
Right Side

The + and – terminal markings for each bit refer to the input polarity of the W731, W733, W741 and W743 Modules. For mercury-wetted relay contact output modules (M800 series), the marked polarity must also be observed if an arc suppression circuit is installed.

The marker strips for DAC module A633 are shown below.

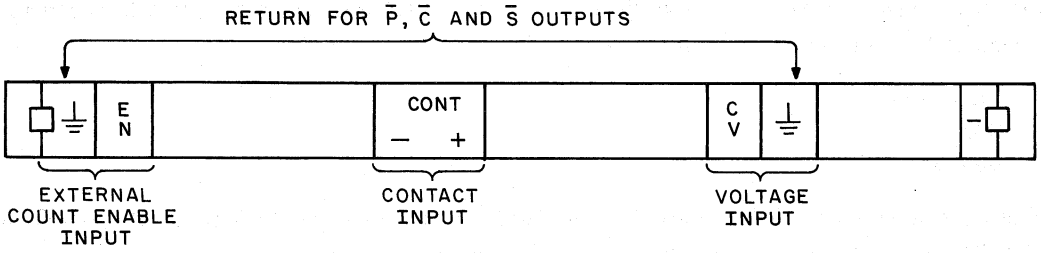


Left Side

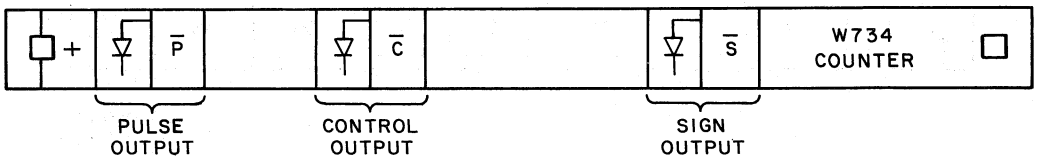


Right Side

The marker strips for counter module W734 are shown below:



Left Side



Right Side

CHAPTER 5
MAINTANENCE

5.1 GENERAL

The maintenance procedures presented in this chapter are limited to those required for maintaining and testing the UDC11 equipment bays. Procedures for maintaining and testing the PDP-11/20 computer system are contained in the *PDP-11 Maintenance Manual.* The maintenance philosophy to be followed for the UDC11 should be preventive in nature; that is, an optimum amount of preventive procedures performed at a routine schedule will eliminate many costly equipment breakdowns and forecast impending failures long before they occur. When a failure does occur, the modular design of the UDC11 minimizes repair and downtime. To locate a specific module or file unit, refer to the channel/system unit identification chart on the rear of the logic cabinet.

5.2 PREVENTIVE MAINTENANCE

Since the UDC11 peripheral contains no special mechanical devices, only standard computer system maintenance procedures are required to ensure reliable operation of the equipment. Failures encountered in the UDC11 should be recorded in the established system maintenance log for future reference. Regular entries in the maintenance log of maintenance performed, troubles encountered, and corrective measures taken, can serve as a powerful tool in maintaining system reliability. A mechanical inspection, diagnostics referenced in Paragraph 1.6, and voltage checks should be performed at regular intervals to verify proper operation of the UDC11. Since each equipment bay has its own H740D Power Supply, the voltage checks should be performed for each bay. Cooling air filters at the top of the logic cabinet should be checked and cleaned as necessary.

5.3 CORRECTIVE MAINTENANCE

5.3.1 General

The simplicity of the universal digital controller and the logic description provided in this manual, along with the results of the diagnostic tests, normally permit the use of standard troubleshooting techniques for isolating a malfunction quickly and efficiently.

A special UDC Field Tester has been developed to aid the DEC Field Service Engineer in isolating and correcting UDC problems. The tester is used in conjunction with the UDC Function Exerciser and consists of lamps and switches used to test UDC outputs and simulate field inputs. It also includes cables that bypass the screw terminals and plug directly into the signal-conditioning modules.

CAUTION

In all cases, when troubleshooting the UDC, disconnect screw terminal wiring from signal conditioning modules, to eliminate hazardous field voltages.

For economical maintenance under most conditions, replace the inoperative module with a spare module, and return the defective module to DEC for repair or replacement.

NOTE

Be sure that the jumpers in the replacement module are set up to reflect those in the defective module.

Recommended spare modules are listed in Table 5-1, and recommended component spares are listed in Table 5-2.

Table 5-1
Recommended Module Spares
(For Module Level Maintenance)

Modules	Module Type	Quantity
0—10V DAC Output*	A233	1
+1 to +5 DAC Output*	A234	1
+4 mA to 20 mA DAC Output*	A235	1
+10 mA to +50 mA DAC Output*	A236	1
DAC*	A633	1
Power Connector	G772	1
Jumper Card	G736	1
Address Selector	M105	1
Inverter	M111	1
Ten 2-Input NAND Gate	M113	1
Eight 3-Input NAND Gate	M115	1
AND/NOR Gates	M121	1
Six Flip-Flops	M216	1
Dual Delay Multivibrator	M302	1
One-Shot Delay	M304	1
Delay Line	M310	1
Variable Clock	M401	1
Pulse Amplifier	M602	1
4-Input Power NAND Gate	M617	1
Bus Driver	M623	1
16-Bit Flip-Flop Relay Driver*	M685	1
16-Bit Single-Shot Relay Driver*	M687	1
Interrupt Control	M782	1
Unibus Drivers	M783	1
Unibus Receivers	M784	1
Unibus Transceiver	M785	1
16-Bit Latching Relay*	M803	1
16-Bit Flip-Flop Relay*	M805	1
Bus Receiver and 8-Bit Address Decoder	M851	1
Bus Connector	M935	1
Bus Terminator	M942	1
Isolated Power Cable Board*	W400	1
Common Power Cable Board*	W402	1
Relay Driver Power Cable Board	W403	1
16-Bit Contact Sense*	W731	1
16-Bit Contact Interrupt*	W733	1
I/O Counter*	W734	1

*If more than ten of any one of these modules are utilized in the system, then one additional spare should be stocked.

Table 5-2
Recommended Component Spares

Components	DEC No.	Quantity
Relay, Quad Form B (used on W731)	12-10116-0	2
Relay, Quad Form C (used on W733)	12-10172-0	2
Mercury-Wetted Latching Form C Relay (used on M803)	12-09672-1	2
Mercury-Wetted Form C (used on M805)	12-09575-1	2
Pig-Tail Fuses, 4A 3AG	90-07219-2	5
Optically Coupled Isolator	19-10845	2
DEC 3568 Transistor (M685 and M687)	15-02937	2

5.3.2 Test Equipment Required

Maintenance activities for the UDC11 require standard test equipment and special materials as listed in Table 5-3, and standard hand tools, test cables, and probes.

Table 5-3
Test Equipment Required

Equipment	Manufacturer	Designation
Multimeter	Triplett or Simpson	Model 630-NA or 260
Oscilloscope	Tektronix	Type 543 or equivalent
Probe (2)	Tektronix	P6010
X10 Probe (2)	Tektronix	P6008
Module Extender*	DEC	Type W982
Test Set	DEC	Optional
Service Kit*	DEC	For single-shot timing adjustments

*Provided with each system.

5.3.3 H740D Power Supply Adjustment

The +5V source should be adjusted for 5 ± 0.250V under full-load conditions. Use the jumper connections on the rear of any G729 Module for access points. Figure 5-1 shows the location of the +5V control.

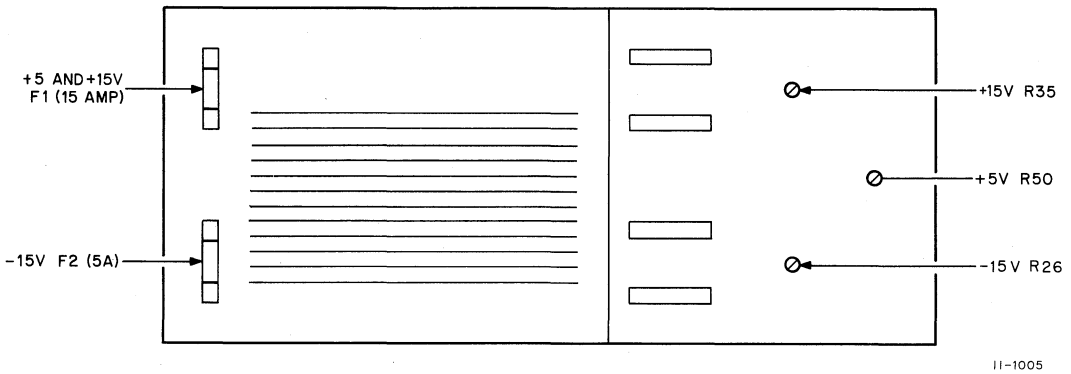


Figure 5-1 H740 Power Supply Fuses and Adjustment Controls

5.3.4 Scanner Clock Adjustment

Scanner clock in slot D01 (Module M401) should be adjusted to a period of 1.0 μs (1.0 MHz) by adjusting the trimpot on the module while viewing the waveform at pins D01D2 or D01E2 (Figure 5-2).

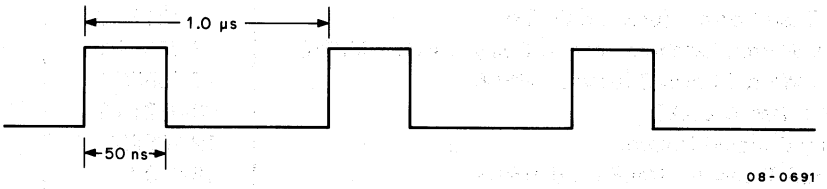


Figure 5-2 Scanner Clock Waveform

5.3.5 UDC Bus Clock Signal Adjustments

System clock CLK00 in slot F07 (Module M401) can be adjusted over the range of 175 Hz to 1.75 kHz by adjusting its trimpot while viewing the waveform at pin C06K1. Clock CLK01 in slot F08 (Module M401) can be adjusted over the range of 1.75 kHz to 17.5 kHz while viewing the waveform at pin C06N1. For testing W734 type modules, these clocks must be set to 1.0 kHz and 16 kHz, respectively, for correct operation of the W734 Module. After the test, these clocks should reset to their original setting.

CHAPTER 6
ENGINEERING DRAWINGS

6.1 GENERAL

This chapter lists DEC block schematics and cabling diagrams of the UDC11 (Table 6-1). These drawings are contained in Volume II of this manual, and provide detailed information about the logic and wiring of the UDC11 peripheral.

Table 6-1
UDC11 Engineering Drawings

Drawing Number	Title
A-ML-IDAC-0	Industrial Data Acquisition and Control
A-PL-IDAC-0-1	Parts List
D-AR-IDAC-0-0	IDAC Arrangements
A-ML-DD01-0	UDC-11 Interface & Control
A-PL-DD01-D-0	UDC-11 Interface & Control
D-BS-DD01-D-02	Device Decoding Integrating Address Scan
D-BS-DD01-D-03	UDC Bus Drivers and Receivers
D-BS-DD01-D-04	Bus Receiver and Address Decoder
K-WL-DD01-D-0-06	Wire List (DD01-D)
A-ML-DD02-0	Expansion System Unit
A-PL-DD02-0-0	Expansion System Unit
D-BS-DD02-0-04	Bus Receiver and Address Decoder
K-WL-DD02-0-03	Wire List (DD02)
E-CS-A233-0-1	0–10V DAC Output
E,D-CS-A234-0-1	+1 to +5V DAC Output
E,D-CS-A235-0-1	+4 mA to 20 mA DAC Output
E,D-CS-A236-0-1	+10 mA to +50 mA DAC Output
E-CS-A633-0-1	DAC
B-CS-G729-0-1	X–Y Addr. Jumper Module
B-CS-G736-0-1	X–Y Jumper Card
B-CS-G772-0-1	Power Connector Module
D-CS-H738A-0-1	DAC Option Power Supply
C-CS-M105-0-1	Address Selector
B-CS-M111-0-1	Inverter
B-CS-M113-0-1	10 2-Input NAND Gates
B-CS-M115-0-1	8 3-Input NAND Gates
B-CS-M121-0-1	AND/NOR Gates
B-CS-M216-0-1	Six Flip-Flops

(continued on next page)

Table 6-1 (Cont)
UDC11 Engineering Drawings

Drawing Number	Title
B-CS-M302-0-1	One Shot Delay Multivibrator
C-CS-M304-0-1	One Shot Delay Multivibrator – Quad
B-CS-M310-0-1	Delay Line
B-CS-M401-0-1	Variable Clock
B-CS-M602-0-1	Pulse Generator
C-CS-M617-0-1	6 4-Input NOR Buffer
C-CS-M623-0-1	Bus Driver
D-CS-M685-0-1	6-Bit F.F. Relay Driver
E-CS-M687-0-1	16-Bit Single Shot Relay Driver
D-CS-M782-0-1	Interrupt Control
B-CS-M783-0-1	Unibus Drivers
B-CS-M784-0-1	Unibus Receivers
B-CS-M785-0-1	Unibus Transceivers
E-CS-M803-0-1	Latching Relay Output
D-CS-M805-0-1	16 Flip-Flop Relay Output
D-CS-M851-0-1	Bus Receiver Addr Decoder
C-CS-M942-0-1	Bus Terminator
D-CS-M7820-0-1	Interrupt Control
D-CS-M7821-0-1	Interrupt Control
E-CS-W731-0-1	Quad Contact
D-CS-W733-0-1	16-Bit Contact Interrupt
E & D-CS-W734-0-1	General Purpose Counter
D-CS-W741-0-1	Contact Sense (Solid State)
D-CS-W743-0-1	Solid State Contact Interrupt
B-CS-849A-0-1	Power Control
D-CS-5409728-0-1	Regulator Board for H740

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