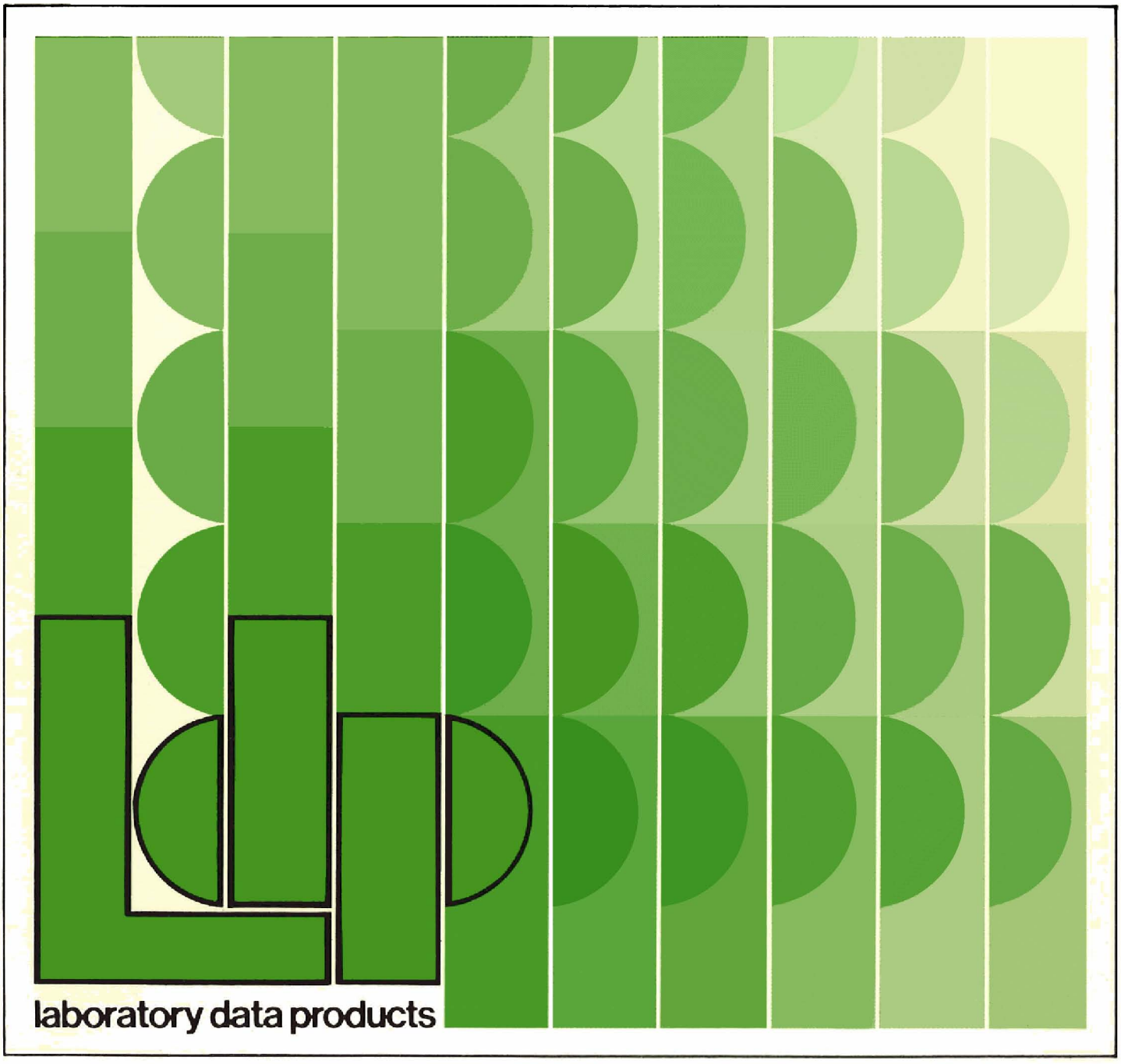
Digital Equipment Corporation
Maynard, Massachusetts

digital

LV8/LV12/LV11 printer/plotter user's guide



DEC-12-HLVAA-A-D

LV8/LV12/LV11 printer/plotter user's guide

digital equipment corporation · maynard, massachusetts

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CONTENTS

CONTENTS (Cont)

ILLUSTRATIONS

ILLUSTRATIONS (Cont)

TABLES

CHAPTER 1
INTRODUCTION

1.1 SCOPE

This guide contains operating, installation, programming, and technical reference data on the LV8/LV12/LV11 Printer/Plotter System. The printer/plotter system consists of two components: an LV01 Line Printer/Plotter (manufactured by Versatec, Inc.) and a Digital Equipment Corporation (DEC) computer interface unit. The interface unit designations for use with each DEC computer are listed below.

Interface	Used with DEC Computer
LV8	PDP-8/E, PDP-8/M
LV12	PDP-12, PDP-8/I, PDP-8/L (positive bus only)
LV11	PDP-11

For example, the LV11 system consists of an LV01 Printer/Plotter and an LV11 Interface Controller for use with a PDP-11 computer.

This guide and the Versatec maintenance manual must be used together for a complete understanding of the printer/plotter system. The prime subject of this guide is the LV8, LV12, and LV11 Controller. The prime subject of the Versatec maintenance manual is the printer/plotter itself; the manual presents a detailed discussion of the print and plot mechanisms, including installation, operation, maintenance, troubleshooting, and engineering drawings.

Paragraph 1.5 lists all reference documents related to the printer/plotter system.

1.2 GENERAL DESCRIPTION

The LV01 Printer/Plotter is a hard copy device manufactured by Versatec, Inc., Cupertino, California, to an exacting set of DEC specifications. Its speed, compact size, and quietness of operation make it ideal for use in hospitals, research laboratories, and offices. The line printer has 132 columns, a 96 ASCII character set, and prints at a speed of up to 500 lines per minute (full line). The plotter speed is 120 lines per second maximum, with a data transfer rate of 500K bytes per second maximum.

Printing is accomplished by depositing an electrostatic charge on a dielectric surface and blackening the charged areas with fine particles deposited from a liquid toner. The paper is then dried by directing air flow over the paper.

The LV01 is available in two models. The 115V model, designated LV01-BA, handles 104–132 Vac at 50 or 60 Hz. The 240V model, designated LV01-BB, handles 208–264 Vac at 50 or 60 Hz.

Interfaces between the LV01 and most DEC computers are available. The interface between the LV01 and a PDP-8/E or PDP-8/M is designated LV8; the interface between the LV01 and a PDP-12 is designated LV12; the interface between the LV01 and a PDP-11 is designated LV11. The LV8 and LV11 interfaces are described in this manual; LV12 operation is identical to the LV8 interface operation.

1.3 FUNCTIONAL DESCRIPTION (Figure 1-1)

1.3.1 Print Mode

In the print mode of operation, the LV01 accepts, in parallel, 7-bit ASCII input code from the LV8, LV12, or LV11 Controller. Each character received is stored in a 132-character memory (buffer). These 132 characters represent one full line of data on 11-inch wide paper. Once the 132-character memory is full, the LV01 automatically prints the 132 characters on a line and then performs an automatic carriage return. If less than a full line is received, certain format control codes (described in Table 3-3) must be transmitted to the LV01 to initiate printing of that line.

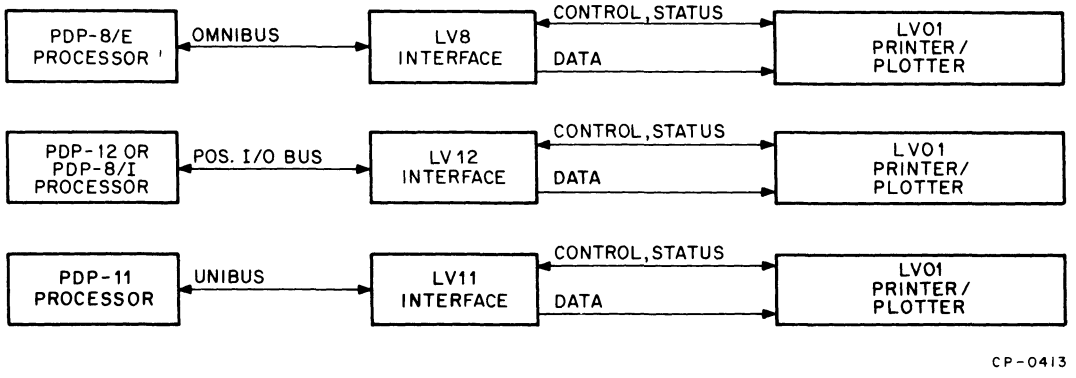


Figure 1-1 LV01 Functional Block Diagram

When printing is to occur, each ASCII character must be decoded and translated in the form of horizontal and vertical dots that can produce a recognizable image on the paper surface. Each character is composed of dots within a 7 X 9 matrix; a total of 63 bits of binary information are associated with each character. Read-only memories (ROMs) are used to store this information until needed by the printer. These bits are sequentially applied to the writing points to produce the desired pattern. When a black dot is required, a charge is placed on the paper; when no dot is required, no charge is applied to the paper. This process, which is also known as the raster scan method of writing, is similar to the writing technique used in television and on television-like terminals.

1.3.2 Plot Mode

When the plot mode of operation is selected, the LV01 accepts, in parallel, 8-bit data bytes. This binary information is stored in a 1024-bit buffer which represents a full scan line on 11-inch paper. The line is automatically printed when the last byte (128th) is received. The character generator used in the print mode is disabled and the unweighted binary information is transferred directly to the writing surface. Input bit 08 prints as the left-most writing point in the current byte when viewing the resultant printout. As an example, input bit 08 would print as the first dot on a scan line if set in the first byte of data transmitted.

Because of the electrostatic method of writing, data must be presented to the plotter in the form of a bit map of the desired graphical information. This can be accomplished with a basic software package which translates simple commands into the required binary data. Unlike pen plotters, speed is not dependent on the complexity of the image to be produced. For example, the LV01 could produce an 8-1/2 inch long X 11 inch wide graph or chart in 10 seconds, regardless of complexity. This opens a new dimension in the use of plotting with computers, since pen plotters have always had a severe limitation on speed due to the necessity of writing every line with a single writing pen.

The ability to produce shading or complex minute patterns in a plot is a feature of the LV01. The writing points are spaced at 0.010 inch intervals and allow the accurate reproduction of minute details.

Plotting applications that can be accommodated on fanfold paper are easier to store, handle, and preserve for future reference. For this reason, the ASCII functions of Form Feed (FF) and End-of-Transmission (EOT) are made available to the user. They are accomplished by pulsing the remote control line associated with that function. These two functions allow formatting of the graphics so printing can begin at the top of a page and the finished graph can be ejected into the viewing area for examination and/or removal.

1.3.3 LV8 Interface

The LV8 Interface Controller transfers data from the PDP-8/E AC (via the DATA lines on the OMNIBUS) to the LV01 under program control. In the plot mode, data is transferred in 8-bit bytes using AC bits 04 through 11. The most significant digit is bit AC 04, which prints at the left-most writing point of the data byte when viewing the copy. For the print mode, data is transferred in 7-bit characters using AC bits 05 through 11. AC bit 11 is bit 01 of the ASCII character.

In addition, the LV8 monitors all line printer error conditions and initiates interrupt requests to the PDP-8. All of the LV8 logic is contained on one module designated M8302. This interface module is discussed in detail in Chapter 4 of this guide.

NOTE

The interface controller for the PDP-12 and PDP-8/I (positive I/O bus only) is designated LV12 and operates similarly to the LV8.

1.3.4 LV11 Interface

The LV11 Interface Controller provides interface logic between the LV01 and a PDP-11 processor. The PDP-11 transfers data utilizing byte instructions to the low order byte of a PDP-11 word (bits 07 through 00). For the print mode, 7-bit ASCII characters (the eighth bit, bit 07, is ignored) are transferred to the LV11 via the Unibus. The plot mode utilizes all eight bits of the low order PDP-11 word. The LV11, in turn, transfers the characters to the line printer/plotter while maintaining program status information and generating program interrupts.

All logic for the LV11 is implemented on one M7258 quad integrated circuit module. This interface module is discussed in detail in Chapter 4 of this guide.

1.4 LV01 SPECIFICATIONS

Physical

Width	19 in. (0.48m)
Height	38 in. (0.96m)
Depth	18 in. (0.46m)
Weight	160 lb. (72 kg)

Electrical

LV01-BA	104–132 Vac, 47–63 Hz, single-phase
LV01-BB	208–264 Vac, 47–63 Hz, single-phase
Power/Heat Dissipation	600W/2000 Btu/hr

Environmental

Operating Temperature	50° to 110°F (10° to 45°C)
Relative Humidity	20% to 80% (non-condensing)

Operational

Paper Drive	Incremental
Paper Drive Increment	0.010 in.
Paper Advance Speed	1.20 in./second
Writing Spot Size	0.0075 in. diameter
Paper Width	11 in.

Plotter

Plotting Area	10.24 in.
Total Writing Points	1024
Writing Point Spacing	0.010 in. center to center
Input	8-bit bytes/parallel
Data Transfer Rate	500K bytes/second maximum
Plotting Speed	120 lines/second maximum
Memory	One line buffer (1024 bits)

Printer

Columns	132
Character Spacing	12.5 in.
Line Spacing	7.6 in.
Character Font	7 X 9 dot matrix
Character Generator	Read-only memory (ROM)
Speed	500 lines/minute printing 132 columns/line
Input Code	7-bit ASCII, USASX3.4-1968, parallel no parity
Character Set	96 (95 printing characters and a space)
Memory	One line buffer (132 characters)

1.5 REFERENCE DOCUMENTS

The following documents supplement the information contained in this guide:

PDP-8/E and PDP-8/M Small Computer Handbook, DEC., 1972

PDP-8/I Maintenance Manual, Volume 1, DEC-8I-HR1A-D

PDP-8/E, PDP-8/F and PDP-8/M Maintenance Manual, Volume 1, DEC-8E-HR1B-D

PDP-11 Peripherals and Interfacing Handbook

PDP-11/20, PDP-11/40, PDP-11/45 Handbooks

PDP-12 Maintenance Manual, Volume 1, DEC-12-HR1B-D

Versatec, Inc. Maintenance Manual for 1100A DEC Printer/Plotter, document number M-1100A-DEC-01

CHAPTER 2
INSTALLATION

2.1 UNPACKING INSTRUCTIONS

2.1.1 Removing LV01 Unit from Shipping Container

The LV01 is shipped in a shock-resistant wooden box. Lift the entire top portion of the box off of the base (after the restraining straps have been removed). Next unstrap the LV01 unit and lift it off the base.

2.1.2 Inspecting LV01 Unit for Shipping Damage

A complete inspection should be made for any shipping damage. A typical sign of a damaged machine could appear as cabinet distortion. The top casting (Figure 2-1) should be opened and closed carefully to ensure that it has not been damaged, distorted, or misaligned during shipment. Check the casters and observe that the unit rolls about freely.

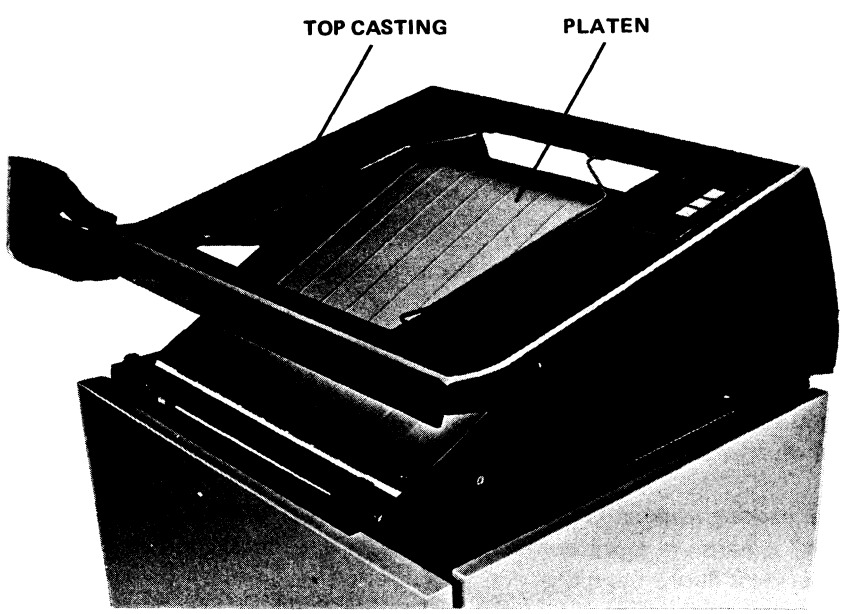


Figure 2-1 Damage Inspection

The front panel is hinged on the left side and held in place by a magnetic catch on the right side. Pull at the upper right corner to open this panel. The side panels are held in place by two snaps at the top. To remove the panel, pull out on the top of the panel, then lower the panel to remove it. The back panel is taken off by loosening (1/2 turn to the left) the two fasteners at the top. After the rear panel is removed, a visual inspection should be made to determine if any of the electrical components have become loose during shipment (Figure 2-2).

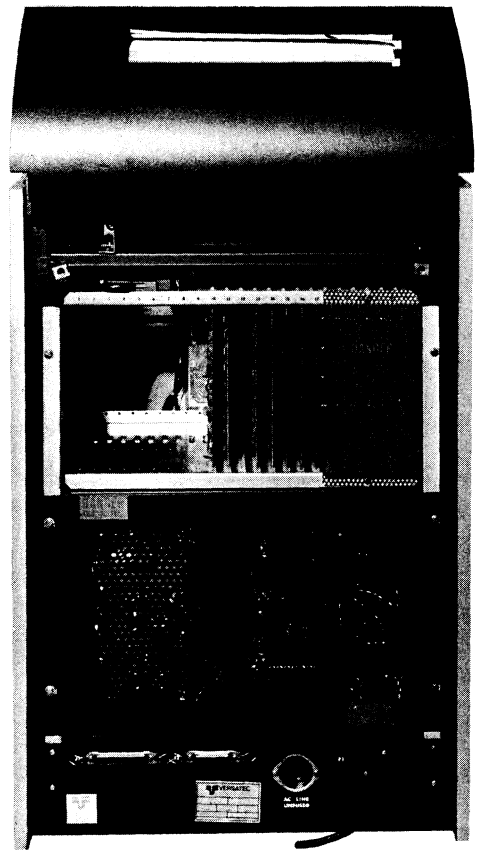


Figure 2-2 Back Panel Removed

2.1.3 Opening the Mechanical Module

Open the top casting as far as it will go. In the raised position, it is held open by its own weight. Raise the black handle (Figure 2-3) which releases the platen module. Raise the platen until it is held open by its own weight.

Remove the protective packing material that has been placed over the writing head and toner channel (Figure 2-4). The metal "spool-cross" is normally taped in place in the "L" shaped brackets. This can be freed by removing any tape that was used to secure it during shipping.

Inspect for possible damage to the back-up electrodes (double segmented bar) and paper drive roller located at the top of the module. The writing head is located between the paper supply compartment and the toner applicator channel.

A light attempt to move the writing head should determine if it has loosened during shipment. If it has loosened, re-alignment of the writing head is necessary. This procedure is described in the preventive maintenance chapter of the Versatec maintenance manual.

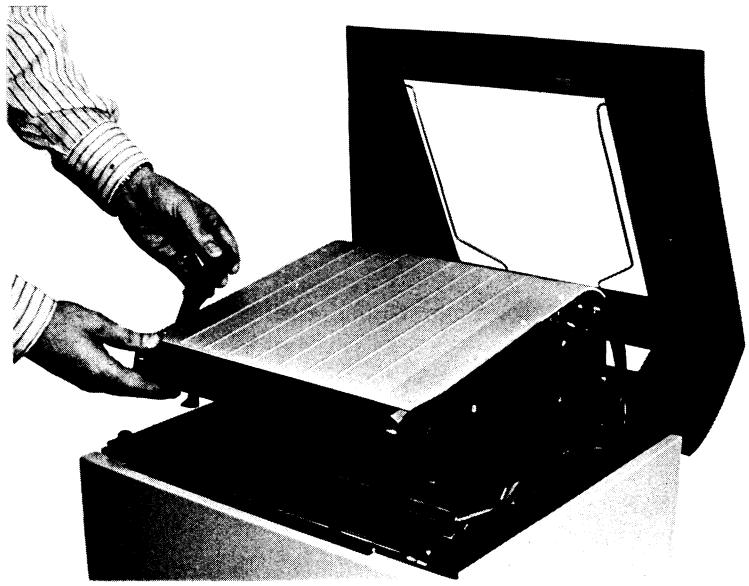


Figure 2-3 Platen Raised View

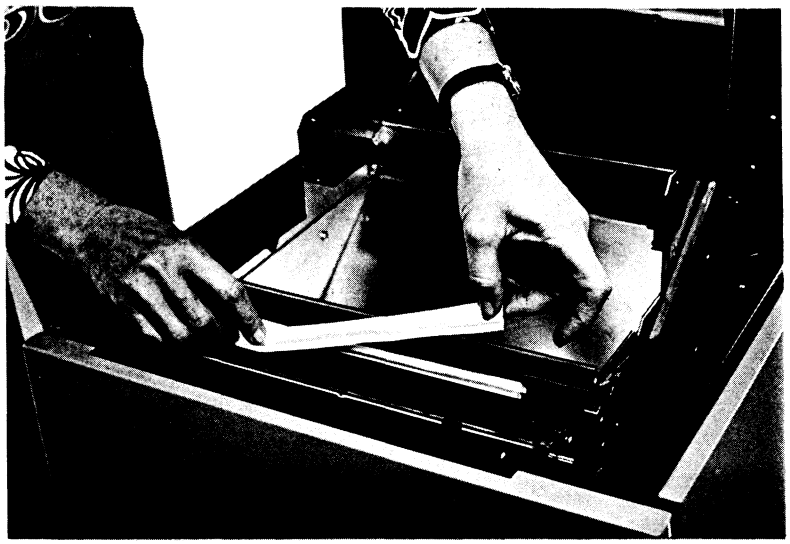


Figure 2-4 Removing Packing Material

2.1.4 Operating Supplies

The following items are included with each LV01 unit:

One (1) LV8/LV12/LV11 User's Guide (DEC no. DEC-12-HLVAA-A-D)

One (1) two-gallon bottle of Toner Pre-Mix (DEC no. 49-01099)

One (1) eight-ounce bottle of Toner Concentrate (DEC no. 49-01100)

One (1) bottle of clear dispersant for cleaning purposes (DEC no. 49-01101)

One (1) carton of 1000 feet continuous form fanfold paper (DEC no. 36-11227-01)

Since print quality depends on the type and characteristics of paper and toner used, supplies furnished by DEC are recommended for proper operation. Performance may be degraded if other supplies are used and machine performance cannot be guaranteed.

2.2 CABLING REQUIREMENTS

2.2.1 Power Cable

A 7.5-foot power cord is permanently attached to the LV01 at the rear of the machine adjacent to the fuse holder. The cord for 60 Hz systems terminates in a standard 3-wire, male, wall-type plug (NEMA 5-15P). The cord for 50 Hz systems has a 15A, 250V male plug (NEMA 6-15P).

CAUTION

LV01 power requirements are 104–132 Vac, 3A, 47–63 Hz or 208–264 Vac, 47–63 Hz, 600W maximum. *Prolonged operation above or below rated voltages may cause equipment failure and void the warranty.* A 3-wire (hot, neutral, ground) receptacle must be available for proper power application. If a proper 3-wire receptacle is not available, a separate wire must be connected from the LV01 chassis to "earth ground".

WARNING

Do not work on the LV01 unit without disconnecting main power to the machine. Make sure that the safety screen over the power supply section at the rear of machine is *always* installed. Dangerous voltages of approximately 1000V are present in this section during operation.

2.2.2 LV01 to Interface Controller

The interface cable between the LV01 and the respective LV11 or LV8 interface is shown on DEC drawing D-IA-7009133-0-0. The LV01 connects to a Cannon DCC-37P located at the lower left corner on the rear of the LV01. The cable terminates at the interface in a Berg connector (DEC no. 12-09941).

2.2.3 LV11, LV8 Interface Controller Module Mounting

The M7258 module (LV11) is mounted in either a DD11-A mounting unit or one of the slots of the processor mounting box. Refer to the *PDP-11 Peripherals and Interfacing Handbook* for detailed information on mounting and Unibus connections.

The M8302 module (LV8) should be mounted in accordance with the recommended order of PDP-8/E module installation as listed in Table 2-3 of the *PDP-8/E, PDP-8/F and PDP-8/M Maintenance Manual,* Volume 1.

2.2.4 Jumper Configurations

2.2.4.1 LV11 (M7258) Jumpers – Table 2-1 lists the required M7258 jumpers and their function.

Table 2-1
M7258 Jumpers

Jumper	Purpose	Function
A4, A5, A7	Address Selection	Jumpers A3 through A12 are used to select the bus address to which the M7258 module will respond. The assigned address, 77751x, is selected by removing all "A" jumpers except A4, A5, and A7.
J14	Address Selection	Jumpers J12, J13, and J14 are used to further define the bus address for the LV11. The LV11 is normally configured with J14 installed. This causes the address logic to assert BUS SSYN L when either address 777514 or 777516 is decoded.
V7	Vector Address	The LV11 uses the vector block at address 200. Removing all "V" jumpers except V7 will produce this interrupt vector address.
N1	NPR Latency	This jumper is normally installed to improve bus latency on NPR devices. New systems on the PDP-11/15 and PDP-11/20 are shipped with a KH11 option which allows use of the N1 jumper. If the LV11 is an add-on option to a PDP-11/15/20, verification that the KH11 has been installed must be made or the system may malfunction. If the KH11 has not been installed, removal of the N1 jumper will disable this circuitry on the M7258.

The M7258 module was designed as a multipurpose interface/controller. Jumpers J1 through J11 are used to accommodate differing signal polarities and control features of these various devices. A general discussion of the jumpers as they apply to the LV11 follows.

J1	Miscellaneous	Jumpers J1 and J2 provide conversion of lower case ASCII codes to the corresponding upper case character before loading the LVDB. With J1 installed, ASCII bit 6 is passed unaltered from the bus receivers to the data register.
J3, J5		These jumpers allow connection of the P DATA 8 H signal to ASCII bit 6, thus allowing the P DATA 8 H signal to be used as a control line. Jumpers J3 and J5 are installed on the LV11 and pass the data unaltered from the LVDB to the LV01.

Table 2-1 (Cont)
M7258 Jumpers

Jumper	Purpose	Function
J7		Jumpers J6 and J7 select the proper clock polarity for the clock input to the Done flip-flop. J7 is installed for the LV11 since the Ready line from the LV01 is low (ground) when true. Thus, the high-to-low transition of the Ready line is inverted and applied to the clock input as a positive transition clocking the Done flip-flop.
J9		Jumpers J8 and J9 select the correct Strobe polarity for the LV01. The LV01 requires a positive pulse for a strobe signal so jumper J9 is installed for LV11 operation.
J10		Jumper J10 is normally installed to allow the remote functions of BUF CLR, REM EOT, REM FF, LINE TERM, and MODE. These remote functions facilitate formatting and data output when the LV11 is used in the plot mode. Jumper J11 installed will disable these functions.

2.2.4.2 **LV8 (M8302) Jumpers** – The only jumpers required on the LV8 M8302 module are the address decoders that allow the 6657 instruction to be utilized. The following jumpers are required on the M8302 for LV8 operation: W1, W3, W5, W7, W11, W12, and W14.

2.3 PACKING LV01 FOR SHIPMENT

Never ship the LV01 unit with toner and concentrate installed; ensure that critical items are secured before packing, otherwise damage may result.

1. Open front door and unscrew toner hose cap from the bottle. Remove concentrate bottle hose after allowing the hose to drain in toner bottle.
2. Wrap paper towels around all of the tubes and cap and tape securely to prevent leakage.
3. Discard unused portion of toner and concentrate. Do not attempt to reseal bottles since leakage and damage may occur during shipment.
4. Raise machine top cover and mechanical module top.
5. Remove roll type paper and tape empty "spool-cross" to its holder.
6. If fanfold paper is being used, remove paper guide and paper stacking insert from the machine. Remove paper tray on rear of machine. Package these parts separately.
7. Fold paper towels to fit in toner applicator channel and insert with light pressure. There are three sections, and each will hold at least one paper towel.
8. Using clear dispersant, wipe any dirt and toner from mechanical module, side, back panels, and door.
9. Close mechanical module top and lock.
10. Wrap AC input cord and place inside the machine. Strap machine in original container for shipment.

CHAPTER 3
OPERATION AND PROGRAMMING

This chapter describes the loading procedures for both roll and fanfold paper and the toner, the LV01 operating controls, the ASCII character set, the format control codes, and presents PDP-11 and PDP-8 programming information relative to the LV01.

3.1 OPERATING INSTRUCTIONS

This section describes the procedures for loading paper and toner and preparing the machine for operation.

3.1.1 Loading Roll-Type Electrographic Paper

To load roll paper, follow the instructions listed below.

1. Remove paper roll from moisture resistant bag (Figure 3-1).

2. Insert "spool-cross" into paper core (Figure 3-2).

3. Position spool-cross in the spool holder which consists of the two "L"-shaped brackets on each side of the paper supply compartment (Figure 3-3).

NOTE
The spring-loaded edge guide (a button on the right side) must be held "in" by the paper when properly loaded. The spool-cross should sit squarely in the holder.

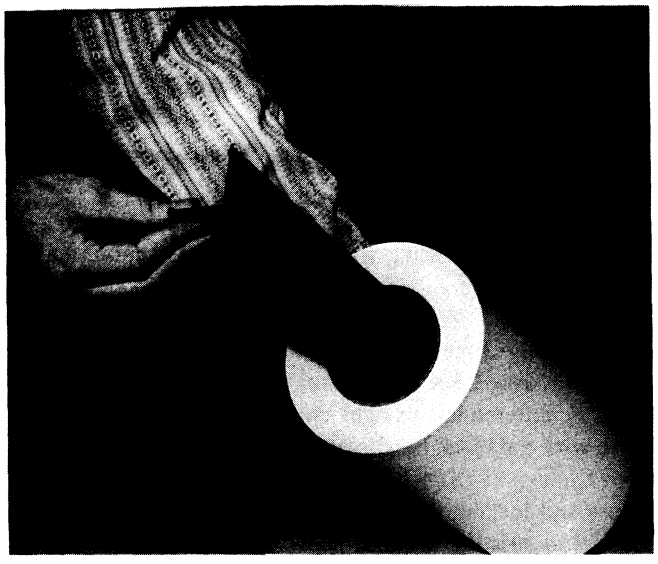
4. Paper should come off the *top* of the roll (Figure 3-4). Since the paper has a dielectric coating on one side only, it must be mounted correctly, as shown. No writing will occur if paper is mounted up-side down (coming off the bottom of the roll).

5. Pull the paper forward off of the roll approximately 2 feet. It should pull easily if the spool-cross has been installed correctly. With the platen module about 3/4 closed, run the paper back over the paper drive roller onto the platen (ensure that paper is centered left to right on the roller) then close the platen (Figure 3-5). Lock the platen module in place with the black handle on the left side.

6. After the platen has been lowered into place and locked, lift the paper and pull up. At this point the paper is resting against the paper tear bar. With a twisting motion, paper can be torn off evenly against this tear bar.

7. Check the position of the ROLL/FAN FOLD switch. It should be in the ROLL position. This switch is located on the right side of the frame after opening the front panel (Figure 3-6).

Figure 3-1 Paper Removal



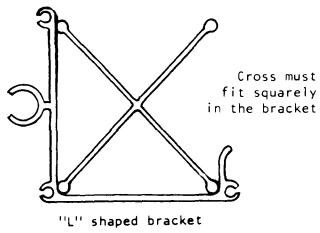


Figure 3-2 Inserting Cross in Roll Paper

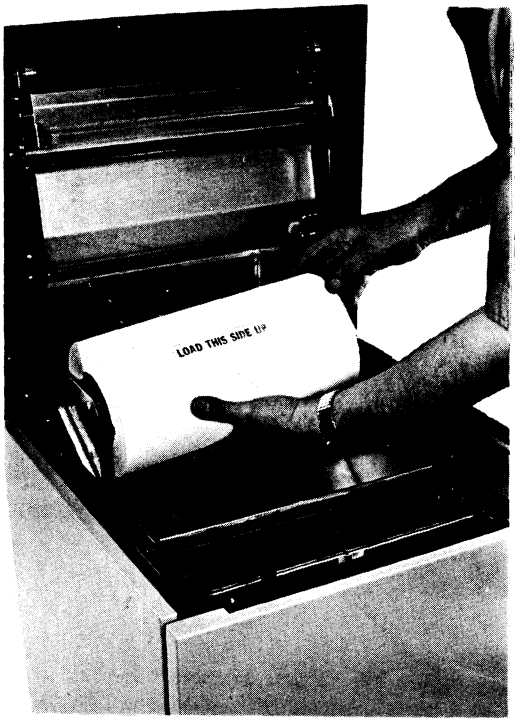


Figure 3-3 Inserting Roll Paper

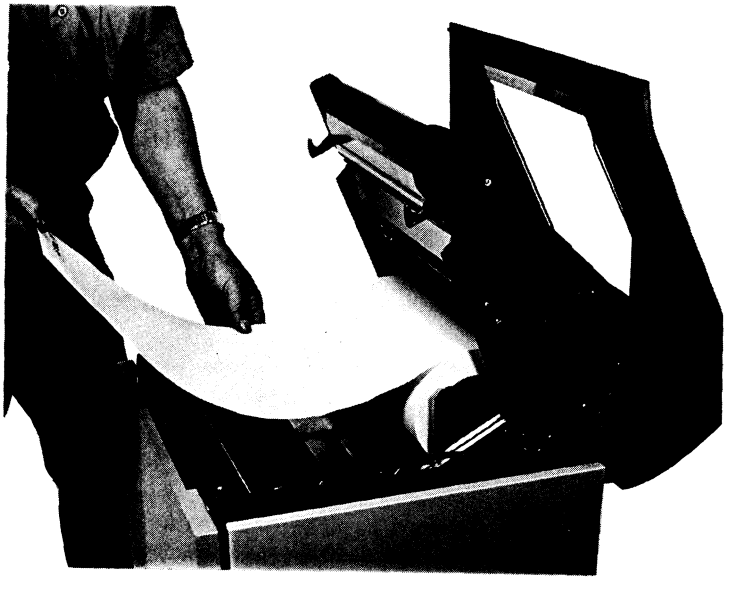


Figure 3-4 Paper Pulled Out

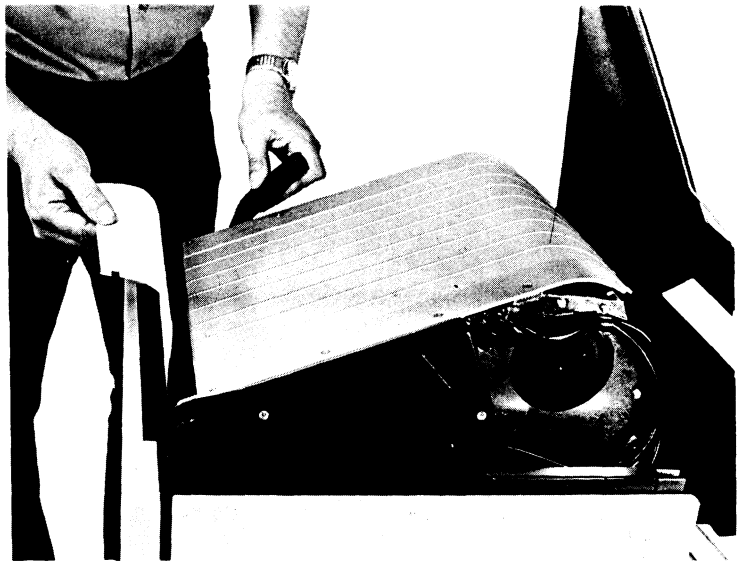


Figure 3-5 Paper Transport Module

Figure 3-6 Control Panel

3.1.2 Loading Fanfold Type Electrographic Paper

The pages of the fanfold paper are perforated at the top and bottom for ease of folding, handling, and separating.

The fanfold paper guide and paper stacking insert are shown in Figures 3-7 and 3-8. These two parts are used for fanfold paper operation only. They are packaged separately for shipment.

To load fanfold paper, follow the instructions listed below:*

1. Remove the spool-cross from the L-shaped paper support brackets. (One L-shaped bracket is located at each side of the paper supply compartment.) The spool-cross is used with roll paper only. Figure 3-9 shows the paper supply compartment with the spool-cross removed.

2. Position the paper stacking insert (Figure 3-8) in the bottom of the paper supply compartment. For positioning, see "D" in Figure 3-11. Notice that the hinges on the paper stacking insert are located toward the front of the machine when the insert is positioned properly.

* Refer to Figures 3-11 and 3-12. These two figures are also found on the inside of the front panel.

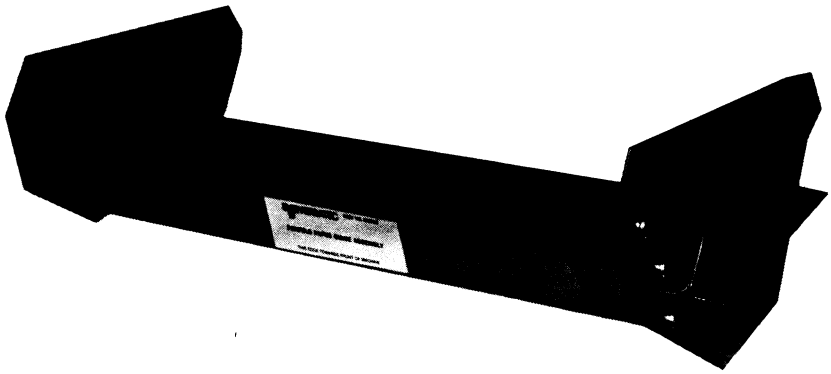


Figure 3-7 Fanfold Paper Guide

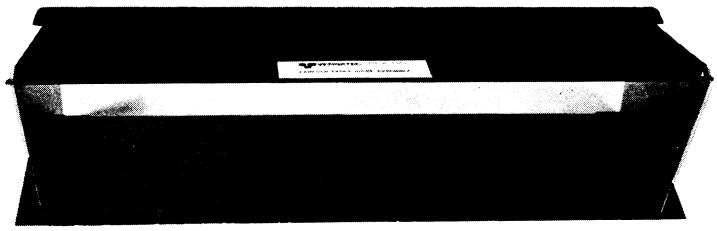


Figure 3-8 Paper Stacking Insert

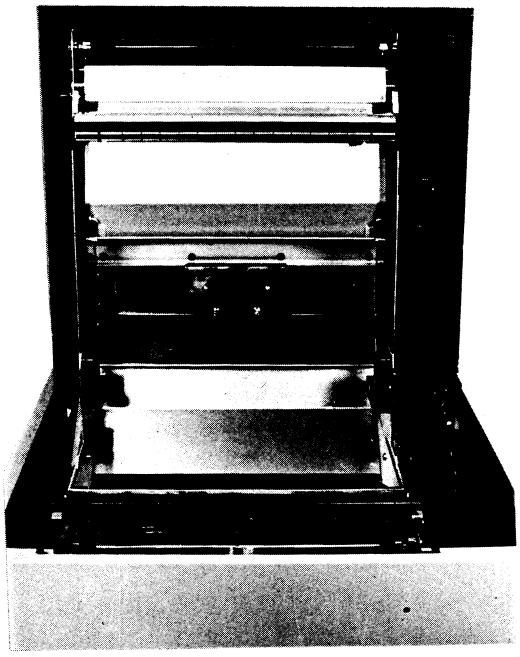


Figure 3-9 Paper Supply Compartment

3. Remove a pack of fanfold paper from its carton. "Break" and "fan" the paper from both ends to loosen the stack before installing in the machine (Figure 3-10).

4. For accurate positioning the paper should sit in the paper stacking insert. The rear of the stack of paper should be higher than the front edge of the paper. The front edge of the stack should be under the hinge of the paper stacking insert flap.

   Load the paper stack with the leading edge of the first sheet toward the front of the machine. The rectangular black mark should be at the front right-hand edge of the stack (see "E", Figure 3-11). Printing occurs on the side of the paper opposite to that on which the black mark is located. The black mark is sensed by the optical mark sensor located on the right side in the top of the mechanical module directly below the back-up electrode (Figure 3-9).

5. Install the fanfold paper guide assembly into the L-shaped paper support brackets (Figure 3-16). The brace welded to each end of the fanfold paper guide should form the hypotenuse (hypotenuse being the line of the triangle opposite the right angle) of a right triangle. The right angle of this same triangle is formed by the L-shaped paper support brackets.

6. Pull the first fanfold sheet back under, then forward over the top of the Teflon coated tension roller, as shown in Figure 3-12. The paper DOES NOT GO BETWEEN the horizontal aluminum spacer bar and the tension roller. The paper DOES GO AROUND both the spacer bar and the tension roller.

7. Place the U-shaped retainer, attached to a small chain on the right side of the installed assembly, between the flange on the spring-loaded roll paper guide and the L-shaped paper support bracket (see "H", Figure 3-12). This keeps the roll paper guide depressed, which prevents interference to the paper travel during fanfold operation.

8. Pull out about 3 feet of paper as shown in Figure 3-13. Lower the platen module and ensure that the paper is centered right and left on the paper roller, then fold the paper back onto the platen. Close the platen module and lock it in place by pushing the black handle on the left side of the module all the way down.

9. Close the top casting as shown in Figure 3-14. Notice that the black mark is not visible.

10. Mount the paper receiver basket on the rear of the machine as shown in Figure 3-15. Metal hangers are provided for the paper basket on the back of each machine.

11. Check the position of the ROLL/FAN FOLD switch. This switch is located on the front of the frame (Figure 3-6) and can be seen after opening the front panel. At this time it should be in the FAN FOLD position. Normal operation with fanfold paper can now proceed. Turn LV01 unit on. Press the FORM FEED pushbutton and observe that the paper advances a page at a time. When actual operation begins, check to see that the paper begins folding correctly in the receiver basket.

12. If fanfold paper operation does not proceed properly, the paper may be misaligned with respect to the sensor. Check paper and fanfold paper guide assembly for correct installation (Figure 3-7).

    If the sensor becomes dirty or clogged with foreign material or paper debris, it will not function properly. Ensure that the sensor is kept clean at all times.

If the black mark is not sensed for any reason (e.g., dirty sensor, missing black mark on paper, or sensor lamp failure) the sensor logic is disabled and the LV01 unit treats an EOT or FF the same as a line feed (LF).

In the event that the sensor logic is disabled, turn power "off", determine the cause of the malfunction and correct it.

After the malfunction is corrected and power is turned "on" again, the sensor logic is automatically reset.

When the ROLL/FAN FOLD switch is in the ROLL position, or when the LV01 unit is in the plot mode of operation, the top-of-form detection circuit is disabled. In the ROLL position, the FF, and EOT control signals advance the paper 2.5 and 8 inches, respectively.

One L-shaped bracket is mounted at each end of the paper supply compartment. This assembly just sits in the L-shaped brackets. It is not attached to the LV01 unit in any way.

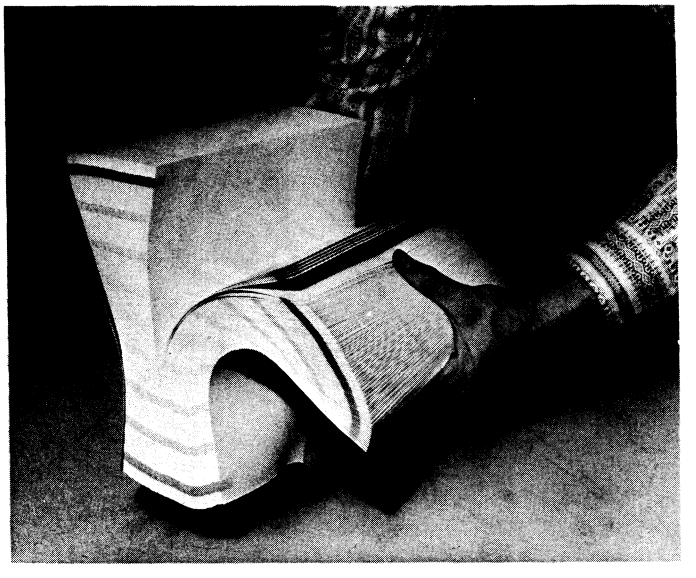


Figure 3-10 'Fan' the Paper to Loosen the Sheets

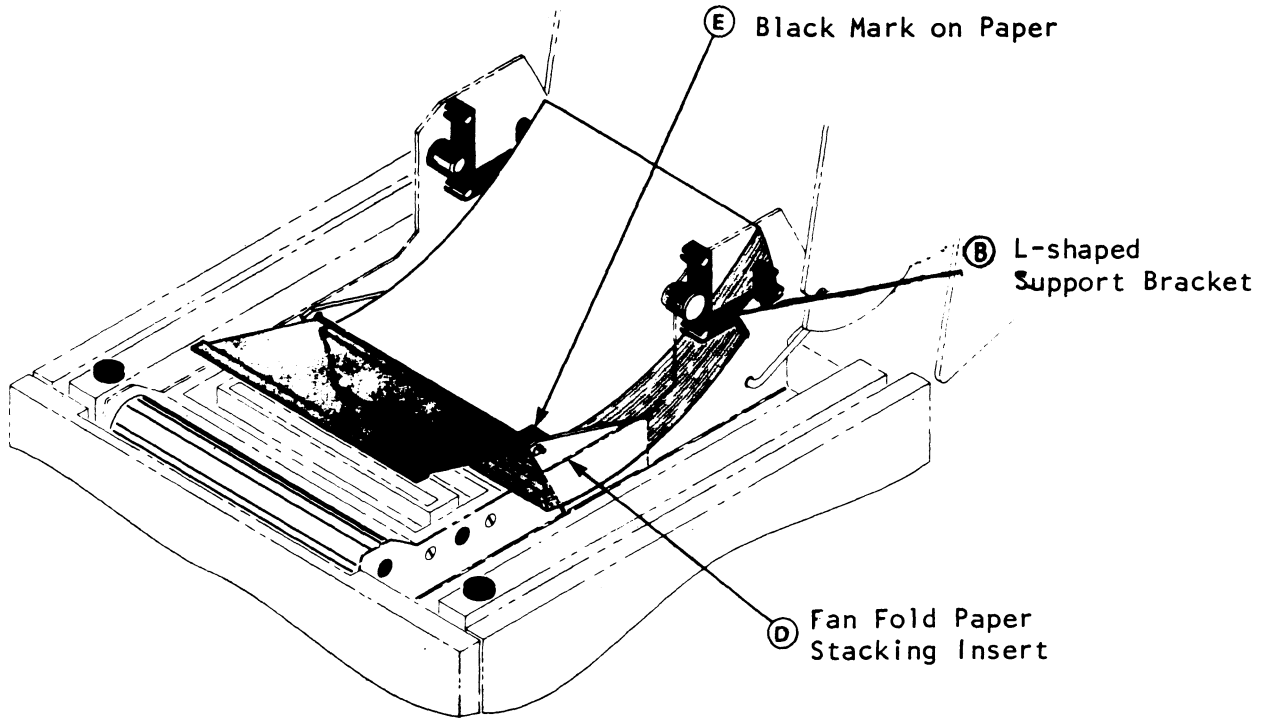


Figure 3-11 Position of Stack for Fanfold Operation

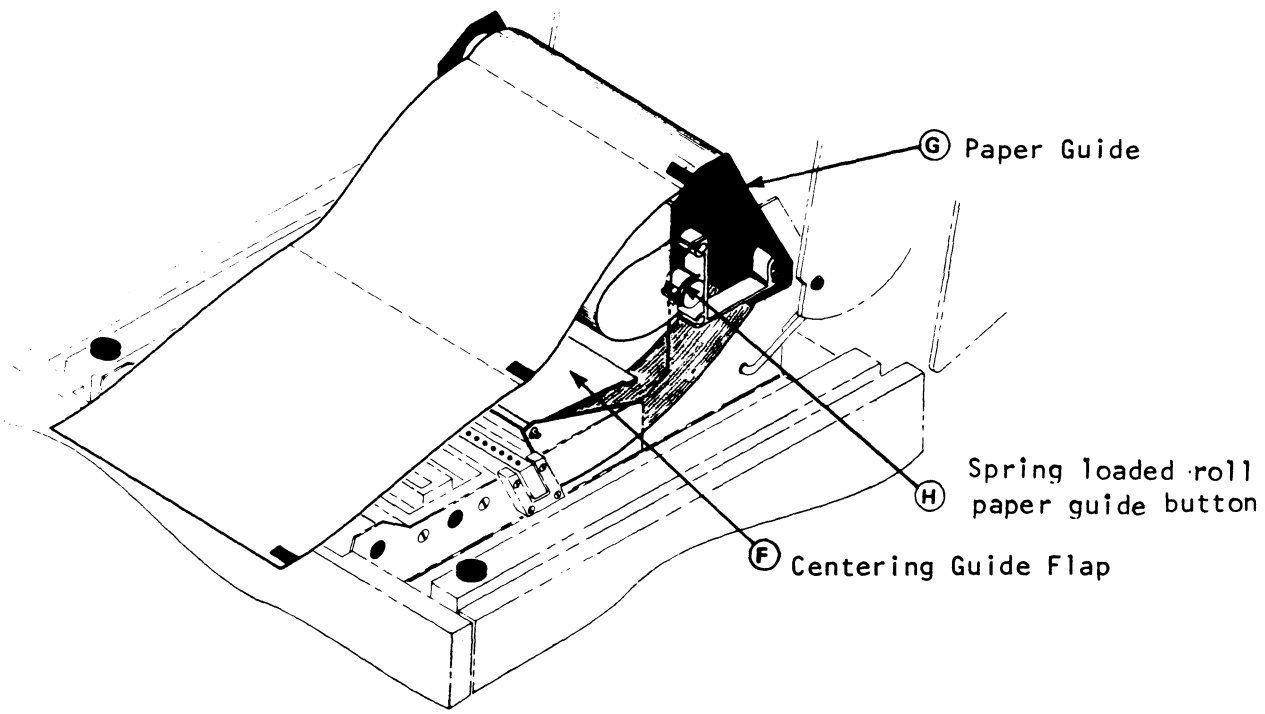


Figure 3-12 Loading Paper over the Paper Guide Assembly

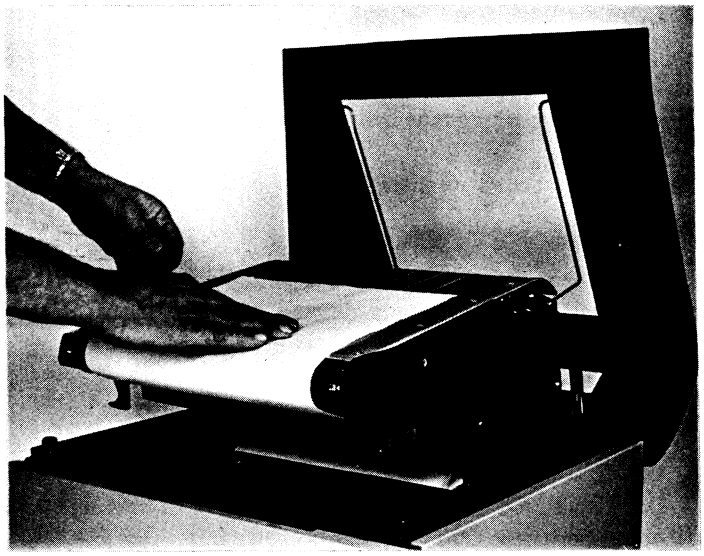


Figure 3-13 Positioning the Paper Left-to-Right on the Paper Roller

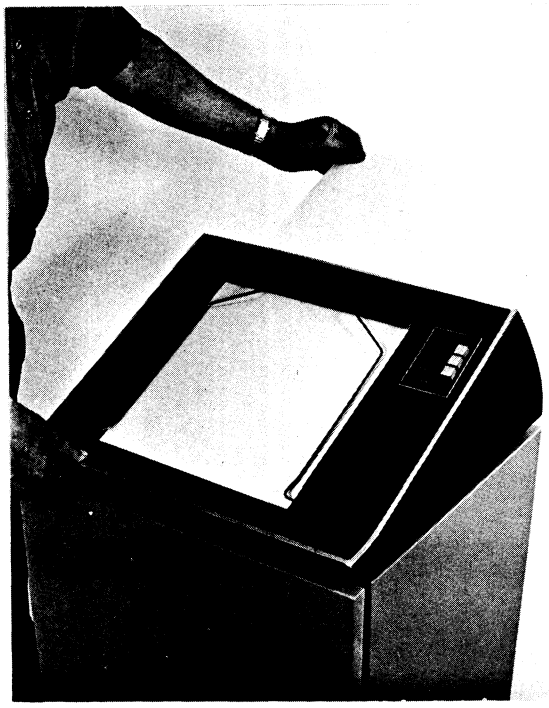


Figure 3-14 Paper Loaded and Top Casting Closed

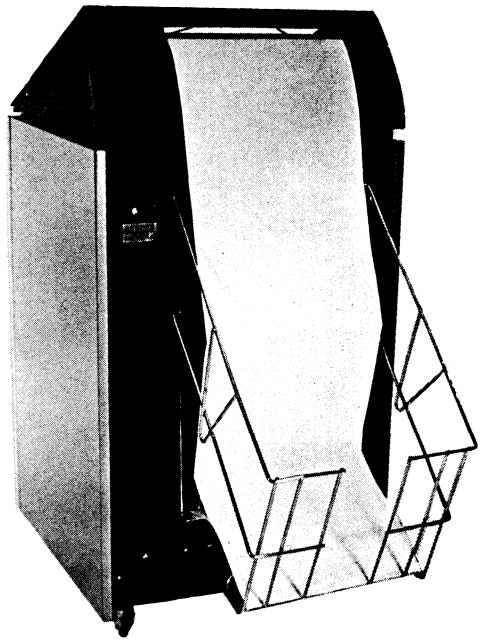


Figure 3-15 Location of Paper Receiver Basket

3.1.3 Loading with Toner

1. Open front door and remove packing tape from toner hoses and tubes.

2. Remove cap and aluminum seal from large bottle of toner pre-mix. Insert tubes into toner bottle and screw cap on securely (Figure 3-16).

3. Inspect all hoses to be sure that they are held securely in place. Hose clamps hold the top of the hoses to the toner channel. Visual inspection should determine if any of the hoses have vibrated loose during shipment. After the toner pump is turned on inspect the system for leaks.

4. Install small toner concentrate bottle in its holder as shown in Figure 3-17. Connect the small hose from the injector spout to the top of the large bottle.

DO NOT ADD CONCENTRATE UNTIL NEEDED. The normal mixture of the toner pre-mix, as shipped, is usually sufficient for four to six rolls of paper usage. The print may become light after this amount of usage (depending on the amount of print-out or "black" being put on the paper). When concentrate is needed, it should be added a little at a time (three injections maximum). It may take several minutes of operation to note a darkening in the print. The decrease in contrast or fading of the printed message is a gradual one; therefore, an optimum toner mix can be obtained by experimenting.

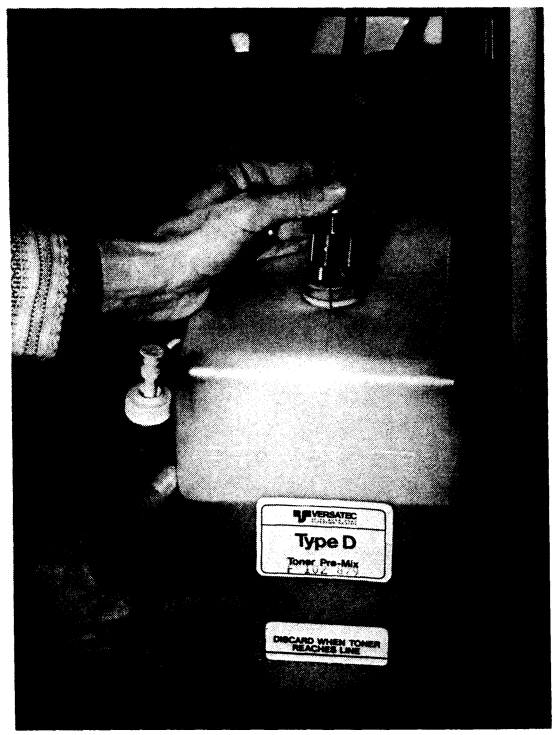


Figure 3-16 Inserting Tubes in Toner Bottle

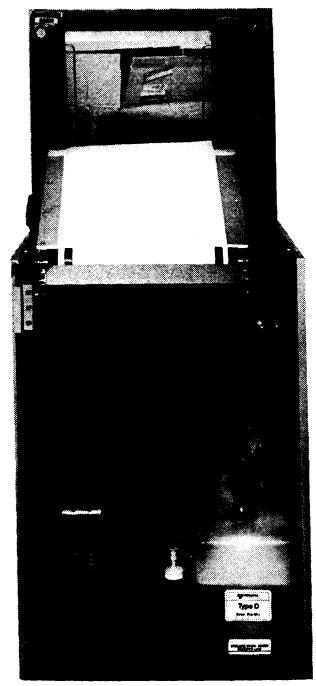


Figure 3-17 Toner and Concentrate Bottles Installed

DO NOT ADD EXCESSIVE CONCENTRATE. If this is done, a dark background will appear, and the quality of the record will be poor. In this event, the toner pre-mix will have to be diluted with clear dispersant.

Under normal operating conditions, the two-gallon toner pre-mix and eight-ounce toner concentrate is sufficient for five to ten thousand feet of paper. Replace these bottles when the low level mark, identified on the toner pre-mix bottle, is reached. NEVER ADD OLD TONER TO A NEW BOTTLE. The replacement reservoir (toner bottle) is a positive design feature of the toning system, since any residue collected in the bottle should be discarded periodically.

3.2 OPERATOR CONTROLS AND INDICATORS

Table 3-1 lists the functions of the LV01 controls and indicators.

Table 3-1
LV01 Controls and Indicators

Nomenclature	Function
ON/OFF	Applies ac power to the LV01. When power is applied, the switch is illuminated and remains depressed. Depressing the switch a second time removes power from the unit.
PAPER ADVANCE	Depressing this switch causes paper to advance provided no data remains in the LV01 data buffer. The switch remains inoperative until the data is printed. Printing may be accomplished under computer control or by depressing the FORM FEED switch located just below the PAPER ADVANCE switch. Paper movement will continue until the switch is released.
FORM FEED	This switch causes the printer to enter a print cycle and print any data remaining in the data buffer. Upon completion of printing of the line, the paper is advanced to the top of the next page when using fanfold paper and the ROLL/FAN FOLD switch is in the FAN FOLD position, or for a distance of 2-1/2 inches when this switch is in the ROLL position.
LOW PAPER	This indicator is red in color and, when illuminated, indicates an out-of-paper condition in the printer. The LV01 will not accept data when this condition exists. An additional supply of paper should be loaded.
CONTRAST ADJUSTMENT	The contrast adjustment is located inside the front panel of the LV01 and is labeled DARK. Its purpose is to allow the operator to compensate for variations in contrast due to humidity changes in the atmosphere. It should be turned as far clockwise as necessary to permit high contrast writing without excessive background writing.

Table 3-1 (Cont)
LV01 Controls and Indicators

Nomenclature	Function
ROLL/FAN FOLD	This switch is located on the frame behind the front door. When this switch is in the ROLL position, the top-of-form detection circuit is disabled. The paper is advanced 2-1/2 inches for a FF and 8 inches for an EOT. When in the FAN FOLD position, the commands are executed as described in Paragraph 3.3. Should this switch be placed in the FAN FOLD position when using roll paper, the top-of-form circuitry will be disabled following the first FF or EOT command. These commands will then be treated as a LF command when in print mode, or as a Line Terminate in the plot mode.

CAUTION
Should any of the manual controls be depressed while the LV01 is in operation, printing will be interrupted to perform the manual function indicated.

3.3 LV01 PRINTER ASCII CHARACTER SET

Table 3-2 lists the ASCII codes recognized by the LV01 line printer. The complete 96-character set (95 characters and a space) is available for use.

Table 3-2
LV01 ASCII Codes

Bit No. 4	3	2	1	7 6 5	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
0	0	0	0				SP	0	@	P	`	p
0	0	0	1				!	1	A	Q	a	q
0	0	1	0				"	2	B	R	b	r
0	0	1	1				#	3	C	S	c	s
0	1	0	0		EOT		$	4	D	T	d	t
0	1	0	1				%	5	E	U	e	u
0	1	1	0				&	6	F	V	f	v
0	1	1	1				'	7	G	W	g	w
1	0	0	0				(	8	H	X	h	x
1	0	0	1				)	9	I	Y	i	y
1	0	1	0		LF		*	:	J	Z	j	z
1	0	1	1				+	;	K	[	k	{
1	1	0	0		FF		,	<	L	\	l	¦
1	1	0	1		CR		-	=	M	]	m	}
1	1	1	0				.	>	N	^	n	~
1	1	1	1				/	?	O	–	o	■

3.4 FORMAT CONTROL CODES

The format control characters used in the print mode of operation are LF (Line Feed), FF (Form Feed), CR (Carriage Return), and EOT (End-of-Transmission). Table 3-3 lists each control character and defines the action taken by the printer upon receipt of that code. The explanation assumes fanfold paper is being used and the ROLL/FAN FOLD switch is in the FAN FOLD position. If the switch is in the ROLL position, the action taken is as described in Table 3-1.

Table 3-3
Format Control Codes

Mnemonic	Octal Code	Function
LF	012	Paper is advanced one line and printing occurs except under the following conditions: (1) LF is the first character received following printing on a full buffer; (2) LF is received as the first character following a CR which caused printing and paper advance of one line; (3) LF is received as the first character following a CR which was immediately preceded by printing on a full buffer. The Demand (or Ready) line will go false upon receipt of the LF code and remain false until the printing operation has been completed. The column control will be returned to the left margin and the line buffer will be cleared.
CR	015	Paper is advanced one line only if a minimum of one character is loaded into the buffer. The column control will be returned to the left margin and the line buffer will be cleared. If this command is received following the printing on a full buffer, it is ignored and no action is taken by the printer. Subsequent CR commands will be ignored by the printer and cause no paper advance or printing unless a minimum of one character has been loaded into the buffer. The Demand (or Ready) line will go false upon receipt of the CR code and remain false until the printing operation is completed.
EOT	004	Data contained in the data buffer will be printed. The paper will be advanced 8 inches, the toner pump will be disabled, and the paper will continue to advance to the next top-of-form sensor. The column control will be returned to the left margin and the line buffer will be cleared. The Demand (or Ready) line will go false until the EOT operation is completed.
FF	014	Data contained in the data buffer will be printed. The paper will be advanced to the next top-or-form sensor. If this distance is greater than 8 inches, the toner pump will shut down and paper movement to the top-of-form sensor will continue. The Demand (or Ready) line will go false until the FF operation is completed.

The LV01 operation, when used as a printer, is very similar to a conventional impact printer in terms of data transfer, programming, and format control. An exception to this is in the handling of the CR function. In a line printer, the CR function prints the line but does not advance the paper. This is not possible with the LV01. Printing can only occur as the paper is being advanced in the electrostatic printer. In most cases, this should not present a problem. However, the user should be aware that this difference exists. The control codes are handled in a manner that prevents multiple line spacing when using standard printer output routines. The following examples show the variety of line terminating sequences available that will not produce multiple line spacing.

Sequence	Results
1. Transmit X number of characters	Characters loaded into the buffer.
2. Transmit CR code	The line is printed and paper is advanced by one line.
1. Transmit X number of characters	Characters loaded into the buffer.
2. Transmit CR code	The line is printed and paper is advanced by one line.
3. Transmit LF code	LF code is ignored.
1. Transmit X number of characters	Characters loaded into the buffer.
2. Transmit LF code	The line is printed and paper is advanced by one line.
3. Transmit CR code	CR code is ignored.

Although the LF and CR codes produce the same results when data is to be printed, it is recommended that "driver' routines for the LV01 use the conventional line terminating sequence of CR followed by an LF code. This enables the same routine to be shared with other printer devices requiring both codes. Specialized software, usable on only one device, is thus avoided.

3.5 PROGRAMMING CONSIDERATIONS

Points to consider for desirable programming techniques include efficiency, speed, and print quality. Programming can only affect one of the factors related to print quality. It can vary the time from application of the charge to application of the toning liquid by controlling the data transfer rate. The important consideration is to maintain a relatively constant data transfer rate so that toning time for each line remains constant. This will eliminate contrast variations in the printed information. It is worth noting that data which is not toned within several minutes after transmission may be lost.

To obtain maximum efficiency and printing speed, data should be transmitted as quickly as possible to the LV01. It can accept one byte of information per microsecond when loading the data buffer. In many cases, this is faster than the processor can transfer. When printing is to occur, it can take 120 ms for a line of text or 8.3 ms for a plot line. This is quite long and the processor should not be held in a loop waiting for completion of the print operation. An interrupt driven handler should be set up and the processor allowed to continue its normal program tasks. If no printing has occurred within the last 1.5 seconds, an additional 1.5 second delay will be encountered when the first line is to be printed. This allows the toner sufficient time to rise in the toning channel before paper movement begins. Again, an interrupt routine would save valuable processor time.

3.6 PDP-11 PROGRAMMING

All software control of the LV11 Controller is performed by means of two device registers (control/status and data). These device registers have been assigned Unibus addresses and can be read or loaded by any PDP-11 instruction that refers to their address.

3.6.1 Control and Status Register (LVCS)

Address: 777514

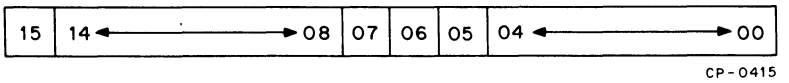


Figure 3-18 Control and Status Register Bit Assignments

Figure 3-18 shows the bit assignments for the LVCS. Loading "read only" bits has no affect on the bit position. Loading unused bits results in data being lost in the corresponding bit position. "Write only" bits will be read as logic 0s. INIT refers to the initialization signal generated by the processor when powering up, when powering down, for a RESET instruction, or by depressing START on the processor console.

Bit	Name	Meaning and Operation
15	ERROR	Asserted (1) whenever an error condition exists in the printer. Error conditions are: 1. No paper 2. Power off 3. No printer connected to LV11 This bit is reset only by manual correction of the error condition. Read only.
14–08	Unused	
07	READY	Asserted (1) whenever the printer is ready to receive the next data transfer. Indicates that the previous function is either complete or has been started and continued to a point where the printer can accept the next data. This bit is set only by the LV01. Read only.
06	INTERRUPT ENABLE	Set or cleared under program control. Cleared by INIT signal from Unibus. When set, an interrupt is requested when READY or ERROR becomes a 1.
05	Unused	
04	BUFFER CLEAR	Set under program control. Clears the buffer indicated by the Mode Control bit. Write only.
03	REMOTE END OF TRANSMISSION	Set under program control. Forces the LV01 to perform an ASCII EOT when in plot mode. Write only.

Bit	Name	Meaning and Operation
02	REMOTE FORM FEED	Set under program control. Forces the LV01 to perform an ASCII FF when in the plot mode. Write only.
01	LINE TERMINATE	Set under program control. Forces the LV01 to print the graphics line prior to receipt of a complete scan line. Write only.
00	MODE CONTROL	May be set or cleared under program control. Cleared by INIT from the Unibus. When cleared the LV01 interprets data as 7-bit ASCII (1968). The complete 96-character set will be printed. It will respond to the control characters in the manner listed in Table 3-3. When asserted (1), the LV01 interprets data as a bit map of computer graphics. A complete scan or assertion of the Line Terminate status bit is required to print the line.

3.6.2 Data Buffer Register (LVDB) (Figure 3-19)

Address: 777516

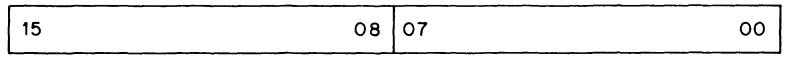


Figure 3-19 Data Buffer Register

Bit	Name	Meaning and Operation
15–08	Unused	The data is lost in these bits if they are loaded.
07–00	DATA	Eight-bit data buffer. Bits 06–00 contain the ASCII characters. Bit 07 is used only in the plot mode.

3.6.3 Interrupts

A program interrupt sequence is initiated whenever the Error or Ready bit is set in the LVCS and the Interrupt Enable bit is set. An interrupt request is generated when the interrupt is granted. It uses the vector block at location 200. The normal priority level is BR4; however, this level may be changed by using a different priority plug in the LV11 controller module. Detailed descriptions of PDP-11 Unibus interrupt sequences are contained in the *Peripherals and Interfacing Handbook.*

3.7 PDP-8/PDP-12 PROGRAMMING

3.7.1 IOT Instructions

The IOT programming instructions and commands that command the LV01 are presented in Table 3-4.

Table 3-4
IOT Programming Instructions

Octal Code	Mnemonic	Function
6657	LPB	Load the contents of AC bits 06 through 11 into the status register.
6661	LSF	Skip on LV01 Done flag. The state of the Done flag is sensed. If it is a 1, the content of the PC is incremented by one so that the next sequential instruction is skipped.
6662	LCF	Clear Character flag. The LV01 flag is cleared to a logic 0.
6663	LSR	Skip on error. The state of the Ready line is sensed and, if it is a 0, indicating an error exists, the content of the PC is incremented by one so that the next sequential instruction is skipped. Errors detected with this instruction are Paper Out, Power Off, or the printer is physically disconnected from the LV8.
6664	LLC	Load printer buffer. Data is transferred to the LV01 buffer from the contents of AC bits 04 through 11. All eight bits are used during a plot operation while only seven are used in the print mode.
6665	LSP	Enable program interrupt. Sets the Interrupt Enable flip-flop.
6666	LPC	Clear the printer Done flag and load printer buffer. Micro-instruction combination of LCF and LLC.
6667	LCP	Disable program interrupt. Clears the Program Interrupt Enable flip-flop.

3.7.2 Status Register

The status register bit assignments are described in Table 3-5.

Table 3-5
Status Register Bit Assignments

Bit	Name	Description
11	MODE CONTROL	Setting this bit forces the LV01 to enter the plot mode of operation. Clearing it indicates a print mode. Initialized to the print mode.
10	MODE ENABLE	Setting this bit enables the LPB IOT to load status bit 11 from the content of AC bit 11. A 0 prevents the changing of bit 11.
09	REMOTE FORM FEED	Setting this bit forces the LV01 to perform an ASCII FF when in the plot mode.

Table 3-5 (Cont)
Status Register Bit Assignments

Bit	Name	Description
08	REMOTE END OF TRANSMISSION	Setting this bit forces the LV01 to perform an ASCII EOT function when in the plot mode.
07	BUFFER CLEAR	Setting this bit forces the LV01 to clear all data contained in the buffer regardless of the status of the Mode Control bit. Printing returns to the left margin and no paper movement will occur.
06	LINE TERMINATE	This bit is used only in the plot mode. If the Mode Control bit is a 0, this function will be disabled. It will also be disabled during the instruction which writes a 1 into the Mode Control bit.

3.7.3 Programming Considerations

Programming of the LV8 is similar to the LP08 with the one exception of the LPB (6657) IOT instruction. The addition of this instruction adds the graphic features of the electrostatic printer. The user is allowed access to ASCII, FF and EOT functions for convenience in formatting graphical information on fanfold paper. In addition, the graphic scan line can be terminated at any time without the necessity of transmitting unnecessary data to the printer.

When used in the print mode, the LV01 will respond to the control codes listed in Table 3-3. With the exception of the CR and EOT codes, the response is identical to the LP08 line printer. When data is in the buffer, the CR code will also force an LF (Line Feed) function in the LV01. This is due to the electrostatic method of writing. It is impossible to write the line of characters without moving the paper.

The EOT code is different because it is not available for use on the LP08. Its function is to ensure that the last information printed will reach the viewing area so the operator can examine and/or remove the printed copy. In exact terms, it will advance the paper 8 inches and then to the next top of form indicator.

Double spacing between lines of characters will not occur due to the manner in which the format control codes are handled by the LV01. The first CR, LF, or CR/LF combination received following the printing due to a full buffer condition is ignored by the printer.

The LV8 interface contains a Done flag which aids the program transfer of data to the printer. When raised, the Done flag indicates that the printer is ready to receive another byte of data. This flag is raised in less than 1 μs after a load data command for all data except the last transfer of the line, a CR, LF, FF, or EOT code. At these discrete times, printing will occur and the time necessary for the flag to return will vary with the function transmitted.

If no printing has occurred within the last 1.5 seconds, the flag is delayed an additional 1.5 seconds. This additional time is necessary to ensure that the toner pump starts up and that the toner has sufficient time to reach the paper.

No restrictions exist when changing between plot and print modes. Once the print cycle has been initiated under either mode, it will continue under that mode even though the Mode Control line is changed. It is not necessary, therefore, to sense the Ready line prior to initiating the mode change.

CHAPTER 4
PRINCIPLES OF OPERATION

This chapter presents a general operating discussion of the LV01 Printer/Plotter and detailed descriptions of the LV8 and LV11 Interface Controllers. (The LV12 operates identically to the LV8.) Complete detailed technical data for the LV01 is contained in the Versatec, Inc. maintenance manual supplied with each unit.

Voltage levels in the LV01 and respective interface are TTL compatible. A 0 state is defined as 0V to +0.8V. A 1 state is defined as +3.0V to +5.0V. A high is also defined as a logic 1, while a low is defined as a logic 0.

4.1 LV01 PRINTER/PLOTTER

4.1.1 General Operation

Figure 4-1 shows all of the interface signals between the LV01 and the interface controller. The print mode of operation is entered whenever the Mode Control line is asserted to a logic high or 1. Conversely, the LV01 operates in the plot mode when the Mode Control line is 0. Following system turn-on and initialization, the interface receives the low condition of the Ready line, which indicates that the LV01 is capable of receiving data. The processor eventually responds with data that is then loaded into the LV01, via lines DATA 1–8, by means of the Data Strobe pulse. As determined by the state of the Mode Control line, the data is either interpreted as printing characters or plot information.

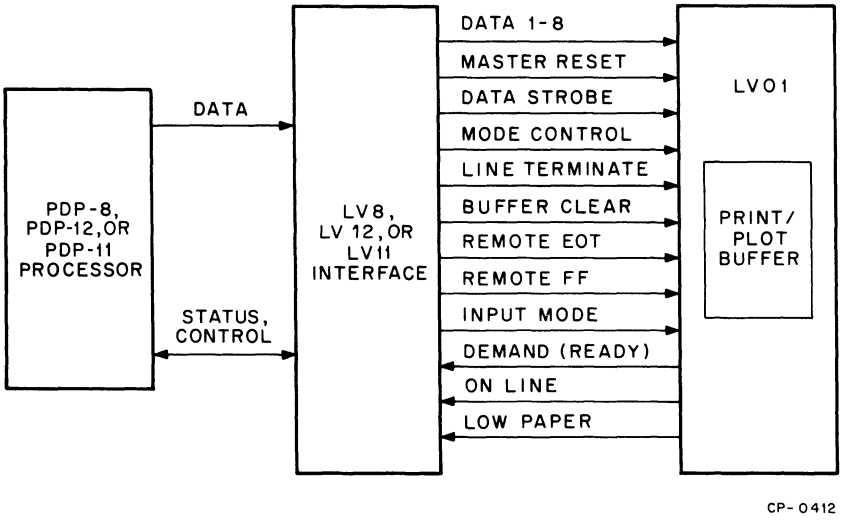


Figure 4-1 LV01 Interface Signals

The Ready line then goes false (high) following the leading edge of the Strobe pulse and returns true (low) when the LV01 is ready for more data. This procedure is repeated until the LV01 buffer is full, at which time its contents are printed. An unfilled buffer, however, may be printed upon the receipt of one of the format control codes listed in Chapter 3.

4.1.2 Electrostatic Writing Technique

In the electrostatic writing process, the paper passes in front of a writing head, which is a laminated assembly consisting of conducting wires in a linear array permanently affixed in a rugged fiberglass structure. The surface of the paper is coated with a nonconducting dielectric material that holds electrical charges received when voltages are applied to the individual writing points. This potential varies between two levels, writing and nonwriting, and can be related directly to the binary data output of the computer.

The writing potential deposits a minute electrical charge on the insulating surface of the paper. A negligible electric current is involved so there is no problem of arcing or burning. Since the electrical signals are placed directly on the paper, the LV01 uses a truely electrostatic writing technique. There is no intermediate step or mechanism, such as mechanical parts or light sources, as is the case in most office copying devices. There are no moving parts associated with the writing process, only a paper transporting mechanism is used.

In order to write in this manner, since the writing points do not move, they must be made to write in a predetermined manner. The nonmoving writing point is only capable of writing a small dot on the paper; many hundreds of these are used to write across a standard size sheet of paper. Controlled information, therefore, must be provided in order to create a recognizable image.

In the electrostatic method, images on the paper, formed from the small dot charges, become visible when the paper surface passes over a toner applicator channel and is exposed to a liquid toner. This toner contains suspended particles of a colored material which contrast to the paper. The particles are of opposite charge to the charge dot on the paper, and are attracted and fixed permanently to the charged areas, making them visible. The trailing edge of the toner channel wipes the excess liquid from the paper and air is directed over the paper's surface for drying. No further fixing or special handling is necessary and the record is available for immediate use. The finished copy exhibits excellent archival qualities and is reproducible on office copying machines.

4.2 LV11 DETAILED DESCRIPTION

The following paragraphs provide a logic level description of the M7258 Interface Module functional units (Figure 4-2): Address Selector, Interrupt Control, Data Register, and Printer Control. The LV11 logic is shown on engineering drawing D-CS-M7258-0-1 (Printer Interface), sheets 1 through 3. These sheets are, respectively, the Data Register (sheet P-2), the Printer Control (sheet P-3), and the Address Selection and Interrupt Control (sheet P-4).

4.2.1 Address Selection Logic

The address selection logic (sheet P-4) decodes the address information from the Unibus and provides three gating signals (only two are used) and four select line signals (two are used) to control the LV11 controller registers. Jumpers are arranged so that the module responds only to standard device register addresses 777514 through 777517 (jumpers in A4, A5, A7, J14). Although these addresses have been selected by DEC as the standard address assignments for the LV11 Controller, the customer can change the jumpers to any address desired. However, any MAINDEC program that references the LV11 Controller standard address assignments must be modified to reflect the new assignments.

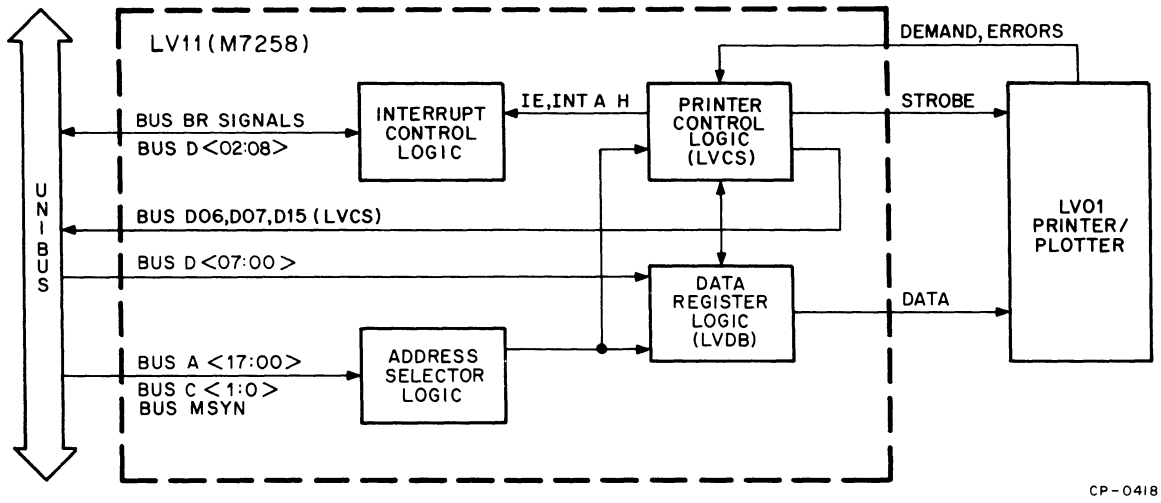


Figure 4-2 LV11 Functional Block Diagram

The first five octal digits of the address (77751x) indicate that the LV11 has been selected as the device to be used. The final octal digit, consisting of A02, A01, and A00, determines which register has been selected and whether a word or byte operation is to be performed. The two mode control lines, C00 and C01, determine whether the selected register is to perform an input or output function. The three jumpers, J12, J13, and J14, determine the responses to the last octal digit of the address as follows:

J12 – a response only from 0 and 2 and no response (no SSYN) from 4 and 6.

J14 – a response only from 4 and 6 and no response (no SSYN) from 0 and 2 (standard).

J13 – a response from 0, 2, 4, and 6.

4.2.1.1 Address Inputs – A simplified block diagram of the address selection logic is shown in Figure 4-3. Note that IN and OUT are always used with respect to the master (controlling) device. Thus, when the line printer controller is used, an OUT transfer is a transfer of data out of the master (the processor) and into the device. Likewise, an IN transfer is the operation of the controller furnishing data to the processor.

The address selection logic input signals consist of 18 address lines, A (17:00); 2 bus control lines, C (1:0); and a master synchronization, MSYN, line. The address selection logic decodes the incoming address as described below. This address format is shown in Figure 4-4. Note that all input gates are standard bus receivers.

a. Line A00 is used for byte control.

b. Lines A01 and A02 are decoded to select one of the two control registers (status or data buffer).

c. Decoding of lines A (12:03) is determined by jumpers. When a given line contains a jumper, the address logic searches for a 0 on that line. If there is no jumper, the logic searches for a 1.

d. Address lines A (17:13) must be all 1s. This specifies an address within the top 8K byte address bounds for device registers.

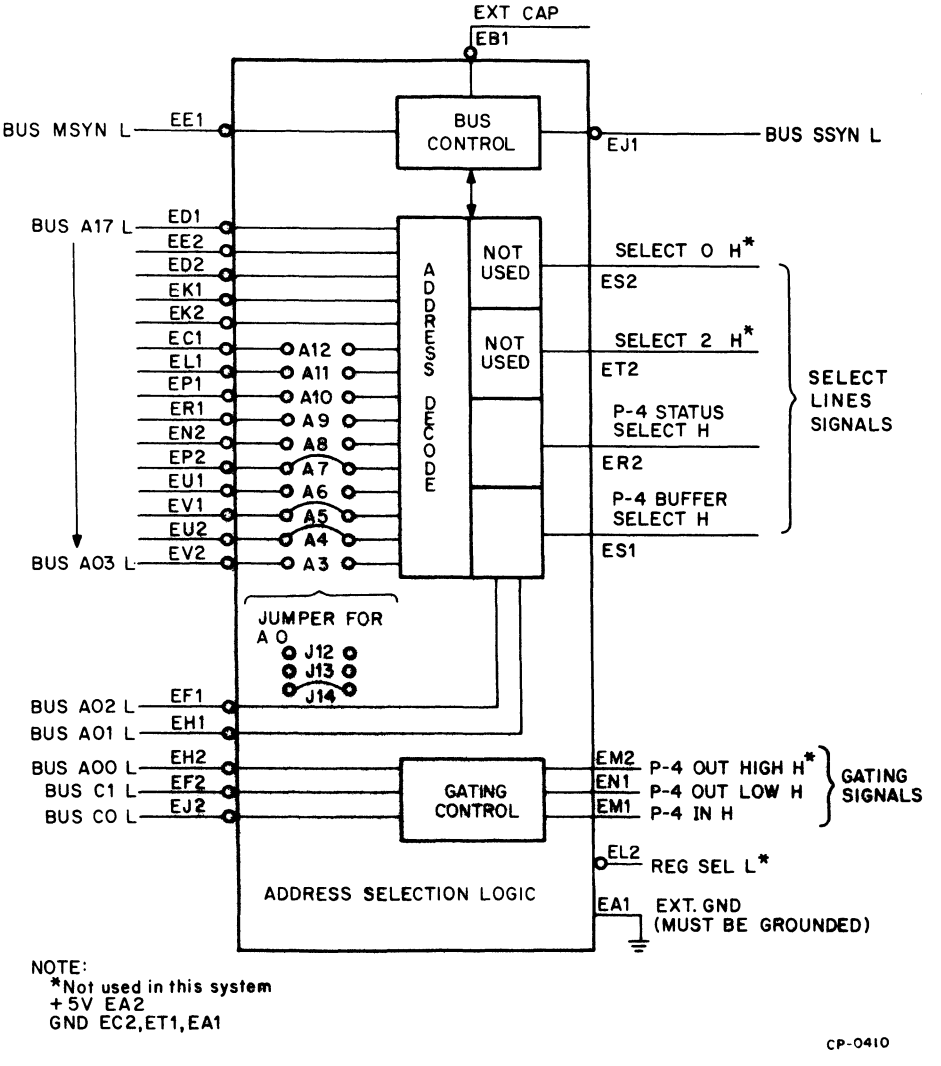


Figure 4-3 Address Selection Logic, Simplified Diagram

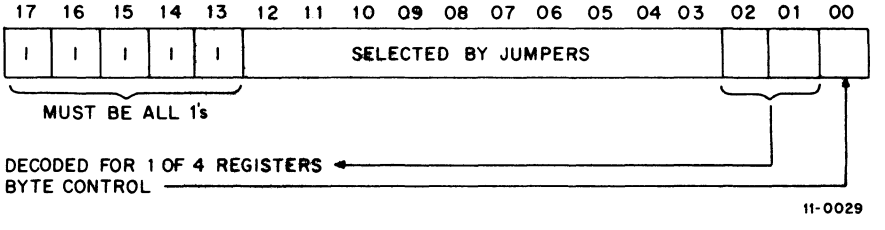


Figure 4-4 Controller Select Address Format

4.2.1.2 Outputs – The address selection logic output signals permit selection of two 16-bit registers and provide three signals that are used for gating information into and out of the master device. All of the output signals are listed in Table 4-2. Note, however, that only two gating signals are listed (IN and OUT). Actually, there are two OUT signals, OUT LOW and OUT HIGH, but OUT HIGH is not used by the LV11 Controller. The logic diagram (drawing P-4) shows two additional select line signals, SELECT 0 and SELECT 2. Neither of these signals is used by the controller.

Tables 4-1 and 4-2 indicate the input signals that select the control output line states.

Table 4-1
Select Lines

Input Lines A (02:01)	Select Lines True (+3V)
00	0 } not used
01	2 } in LP11
10	4 (Status)
11	6 (Data)

NOTES
1. **Lines A (17:13) must be all 1s (0V on Unibus).**
2. **Lines A (12:03) are selected by jumpers.**

Table 4-2
Gating Control Signals

Mode Control C (1:0)	Byte Control A00	Gating Control Signals True (+3V)	Bus Sequence
00	0	IN	DATI
00	1	IN	DATI
01	0	IN	DATIP
01	1	IN	DATIP
10	0	OUT LOW OUT HIGH	DATO
10	1	OUT LOW OUT HIGH	DATO
11	0	OUT LOW	DATOB
11	1	OUT HIGH	DATOB

NOTES
1. **Gating control signals may become true although select lines are not.**
2. **OUT HIGH not used in LV11 Controller.**

When EXT CAP is grounded, it inhibits the acknowledgment signal (SSYN) normally generated by the address selection logic.

4.2.2 Interrupt Control

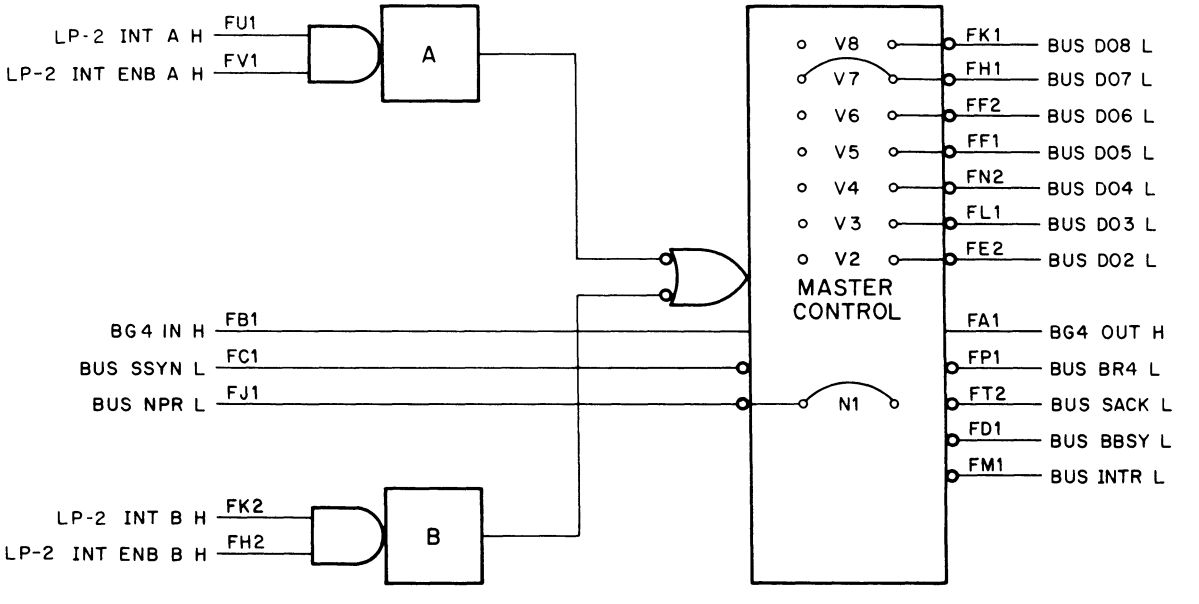
The interrupt control logic (drawing P-4) permits the LV11 Controller to gain control of the bus (become bus master) and perform an interrupt operation. The jumpers on this logic are arranged so that the logic has a normal vector address of 200 (jumper in bit position 7). Although this is the recommended vector address, the user may change the jumpers to correspond to any address desired, but MAINDEC programs and other software referencing the standard vector address assignment of 200 *must* be changed to reflect the new assignments.

The interrupt control logic consists of a dual-input request and grant acknowledge circuit for establishing bus control. The interrupt occurs at vector address 200. The B input portion of the logic is disabled because neither an INT B or INT ENB B can be generated by the LV11 Controller (these two input lines are grounded as shown on drawing P-3).

Before the interrupt control logic can generate an interrupt request, two input signals must be high: INT A and INT ENB A. The logic that generates these two signals is shown on drawing P-3. When a 1 is loaded into bit 06 of the status register, it sets the INT ENB flip-flop in the E14 IC to produce INT ENB A H. The data input to this flip-flop is the 1 from BUS D06 and the clock input is the load signal P-4 (SEL 4 H and P-4 OUT LOW H).

The second signal that must be present to generate an interrupt is INT A H. The INT A H signal is produced by an OR gate and an inverter that is qualified when either a DONE or an ERROR condition exists. The DONE and ERROR conditions are described in Paragraphs 4.2.3 and 4.2.4.

The master control section of the interrupt logic (Figure 4-5) is used to gain control of the bus. When both the INT A and INT ENB A requesting inputs are asserted, a bus request is made on the BR level corresponding to the level of the priority plug. The standard level for the LV11 Controller is BR4, but this may be changed by the priority plug, if desired. When the priority arbitration logic in the processor recognizes the request and issues a bus grant signal, the master control circuit acknowledges with a SACK signal. When the controller has fulfilled all requirements to become bus master (BBSY false, SSYN false, BG false), the master control section asserts BBSY.



NOTES:
1. Input B not used (INT B and INT ENB B are grounded) in LV11 controller.
2. Bus request made on level 4.
3. Interrupt vector is 200.
4. Jumpers are: jumpers for a 1.

CP-0411

Figure 4-5 Interrupt Control Logic, Simplified Block Diagram

Once the controller has gained bus control by means of a BR request, an interrupt is generated. The interrupt vector address is selected by jumpers on the logic as shown on Figure 4-5. Because the vector is a 2-word (4-byte) block, it is not necessary to assert the state of bits 00 and 01. The seven selectable lines determine the vector address.

The BG IN signal is allowed to pass through the logic to BUS BG OUT when the controller is not issuing a request. To request bus use, the AND condition of INT A and INT ENB A must be satisfied. These levels must be true until the interrupt service routine clears INT or INT ENB. Once bus control has been attained, it is released when the processor responds with BUS SSYN after it has strobed in the interrupt vector. After releasing bus control, the logic inhibits further bus requests even if INT A and INT ENB A remain asserted. In order to make another bus request, INT A or INT ENB A must be dropped and then reasserted to cause the logic to reassert the request line. This prevents multiple interrupts when the master control is used to generate interrupts.

4.2.3 Data Register Logic

The data register logic (sheet P-2) consists of an 8-bit data buffer, the decoding circuitry necessary to detect the LF and FF commands when in the print mode, and the line drivers for the eight data lines and the prime signal. The eight bits of data from BUS D00 L through BUS D07 L are applied to the data inputs of the two 74175 D-type flip-flop ICs and clocked into the register by the LD BUF H signal. The LD BUF H signal is asserted when both P-4 BUFFER SELECT H and P-4 OUT LOW H are true. The P-4 BUFFER SELECT H signal indicates that the LV11 data register address has been decoded by the address decoding logic. The P-4 OUT LOW H signal indicates that a DATO or DATOB bus operation is in progress. Thus, the data register is loaded by addressing the LVDB and initiating a DATO or DATOB transfer.

The output of the data buffer is monitored by the LF and FF decoding circuits. If either code (012_8 or 014_8) is detected, P-2 LF/FF L is asserted when P-3 GATE H is generated by the printer control logic.

The outputs of the data buffer are also applied to the 7437 line drivers that drive the cable lines going to the LV01. The 1K resistors help terminate the interface cable to minimize reflections and noise.

The BUS INIT L signal is bufferred and inverted by E20. It is then applied as a high signal to the 7437 driver where it undergoes a second inversion and is transmitted to the LV01 as a low true signal called P PRIME L.

The data register logic also contains the interrupt priority plug (E26). The LV11 is normally configured with a BR4 interrupt level priority plug.

4.2.4 Printer Control Logic

The printer control logic (sheet P-3) monitors line printer control lines, provides the interrupt control logic with interrupt request information, contains the LV11 Control and Status Register (LVCS), and provides a strobe signal to load data from the LVDB into the LV01 buffer. In addition, the printer control logic contains circuitry to force the transmission of a CR code to the LV01 when the P-2 LF/FF signal is asserted.

During data transfers, other than LF and FF, the trailing edge of P-2 LD BUF H (asserted by the data register logic) fires a 74123 monostable multivibrator (one-shot) which generates a 500 ns pulse. This time interval is used to allow the data lines to settle before strobing the information into the LV01. The trailing edge of this pulse (pin 13 of E25) fires a second one-shot whose output is applied to a line driver through jumper J9. The output of the 7437 driver is used as the strobe signal for the LV01. Strobe is a positive TTL level pulse with a duration of approximately 500 ns. Refer to Figure 4-6 for character transfer timing.

P-2 LD BUF H also clears the Done flip-flop (Done is initially set by BUS INIT L) and fires another 74123 one-shot (E23) producing P-3 GATE H (pin 13 of E23). P-3 GATE H is an input to the data register logic and generates P-2 LF/FF L, if an LF or FF code is contained in the LVDB. With P-2 LF/FF L unasserted, the Hold flip-flop remains clear and P DEMAND will set the DONE bit when the character has been accepted by the LV01. The DONE bit may then be read under program control and a new DATO transfer to the LVDB initiated. If the interrupt enable (IE) bit in the LVCS is set, an interrupt request is generated. The PDP-11 can then service the Done interrupt by sending another character to the LVDB.

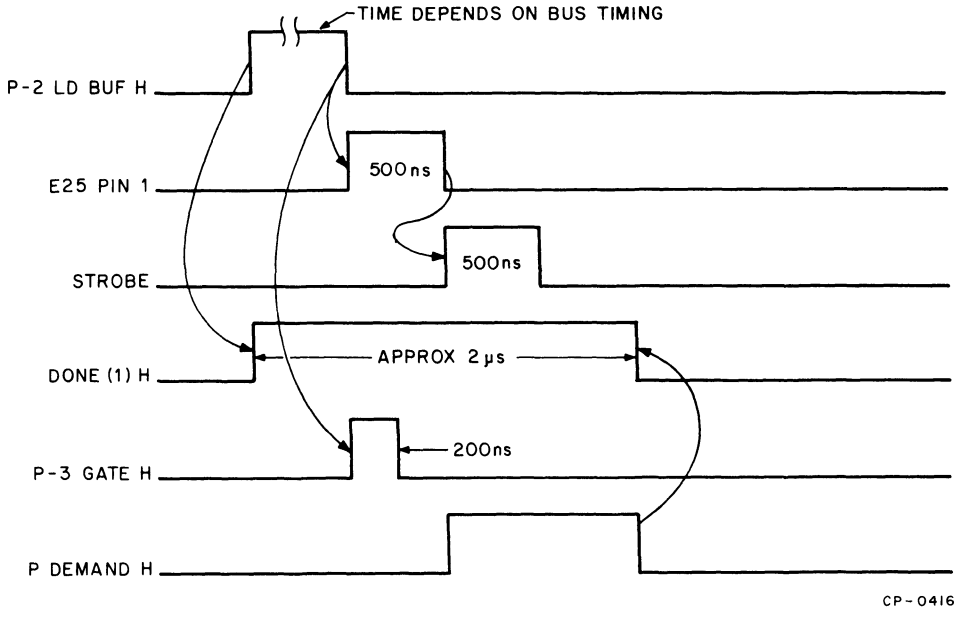


Figure 4-6 LV11 Character Transfer, Timing Diagram

If, when P-3 GATE H is asserted, P-2 LF/FF is generated by the data register logic indicating that an LF or FF is to be output to the LV01, the Hold flip-flop is direct set (Figure 4-7). This forces the lower three data bits (P DATA 1 through P DATA 3) to an octal 05, converting the LF (012) or FF (014) code to a CR (015) command at the LV11 output lines. The reset side of the Hold flip-flop is connected to the data input of the Done flip-flop. Therefore, when the converted CR is loaded into the LV01 by Strobe, P DEMAND does not set Done, but clears the Hold flip-flop. The clearing of the Hold flip-flop fires a 200 ns one-shot (pin 13 of E25). The sequence then proceeds the same as in a normal character transfer. The 74123 one-shot (pin 4 of E24) is fired to generate Strobe which loads the LF or FF character, still in the LVDB, into the LV01 buffer. With Hold now clear, P DEMAND will set the Done flip-flop when the LF or FF operation has been completed.

The printer control logic also generates P-3 INT A H when an error condition exists in the LV01. If P HDWR H or P PAPER H is asserted from the LV01, ERROR H is generated for at least 400 ms by a 74123 one-shot (E23). (Signals P FAULT L and P SELECT L are not used by the LV01.) ERROR H produces P-3 INT A H and inhibits Done from being read by the program. Therefore, ERROR H or DONE (1) H generates P-3 INT A H which initiates an interrupt request to the interrupt control logic, if the IE bit is set in the LVCS. Signals P-4 IN H and P-4 STATUS SELECT H drive bits 06 (IE), 07 (Done), and 15 (Error) onto the respective Unibus D lines during a DATI operation to the LVCS.

The functions of BUF CLR, REM EOT, REM FF, and LINE TERM are produced by the 74174 IC (E14) and the 74123 one-shot (E25). These signals are initiated under program control and are controlled by the Unibus D lines when the LVCS register is addressed. This discussion is for BUF CLR; the other functions are generated in a similar manner. When a DATO to the LVCS register is performed, P-4 OUT LOW H and P-4 STATUS SELECT 4 H are generated by the address selection logic. These two signals are ANDed to form the clock signal for the 74174 control register (E14). The leading edge of this clock pulse loads P-2 BD04 H (buffer clear) into the register. The trailing edge of the clock pulse fires the 74123 one-shot (E25) producing a 500 ns pulse at its output. This pulse is gated by the output of the control register (pin 12 of E14) and a 500 ns negative pulse is transmitted to the BUF CLR line. The leading edge of the pulse also clears the Done flag, prohibiting further data transfers until the BUF CLR operation has been completed.

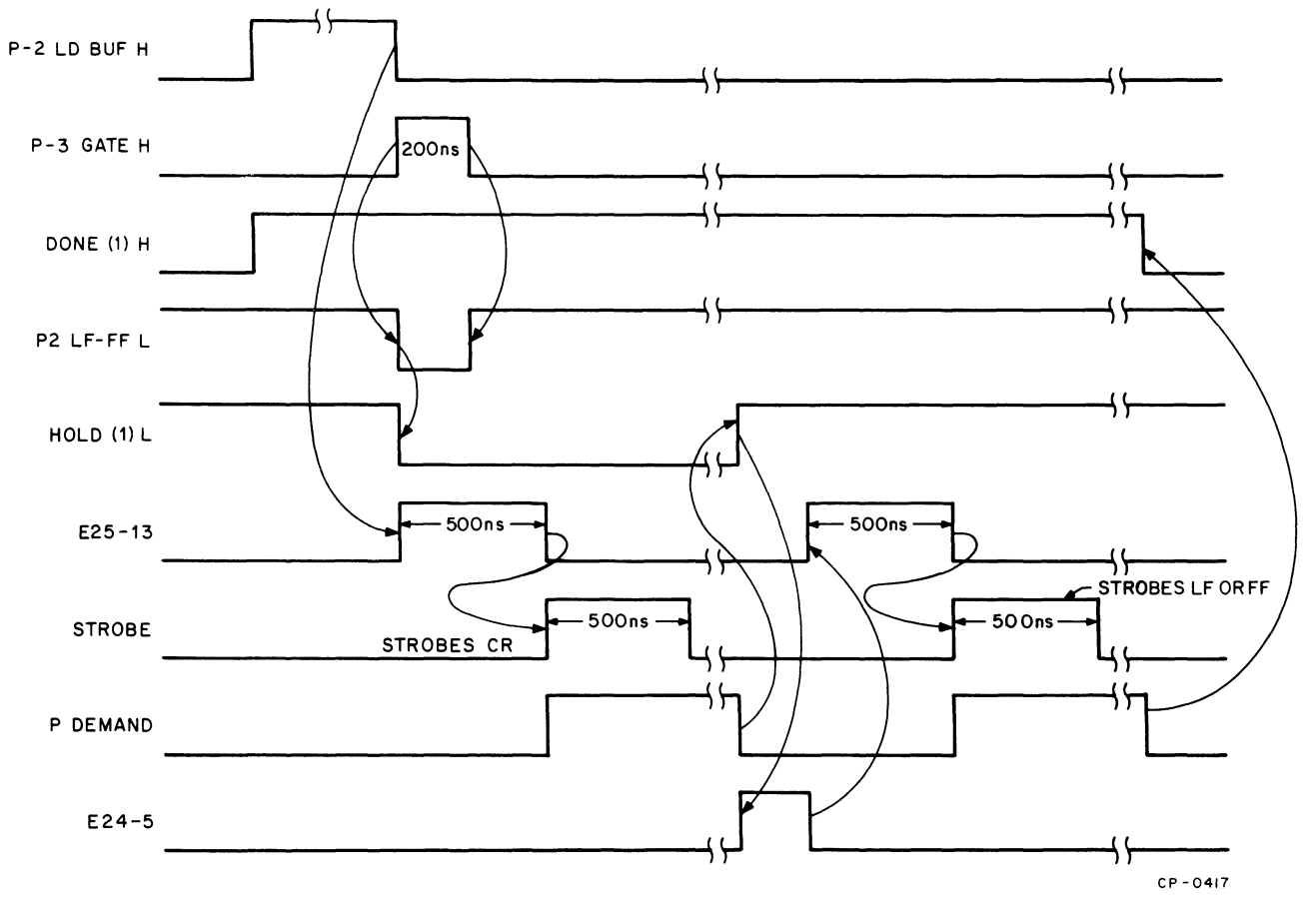


Figure 4-7 FF and LF Timing Diagrams

The remaining bit in the control register is the Mode bit. The state of this bit determines whether the LV01 will interpret the data presented to it as ASCII characters or as graphical information. The Mode bit is cleared by BUS INIT L and places the LV01 in the print mode following the application of power or a program initialize. Setting this bit will force the LV01 to enter the plot mode of operation and accept the data presented to it as unweighted binary data in the form of a bit map of the desired graphical information. The Ready flag is not cleared when the mode of operation is changed.

The LV01 timing associated with REM EOT, REM FF, BUF CLR, and P PRIME L is shown in Figure 4-8. The timing for LINE TERM is shown in Figure 4-9.

4.3 LV8 DETAILED DESCRIPTION

The LV8 Printer/Plotter System is contained on a quad 8E card whose pins are defined by the 8E OMNIBUS. The interface is designated the M8302 and the logic is shown on drawing D-CS-M8302-0-1, sheets 1 and 2. The logic is divided into four functional units (Figure 4-10): IOT Decode, Interrupt and Skip Control, Printer Control, and Data Register. The following paragraphs provide a logic level explanation of these functional units. The level of discussion assumes that the reader is familiar with the principles of operation covered in the PDP-8 reference manuals listed in Paragraph 1.5.

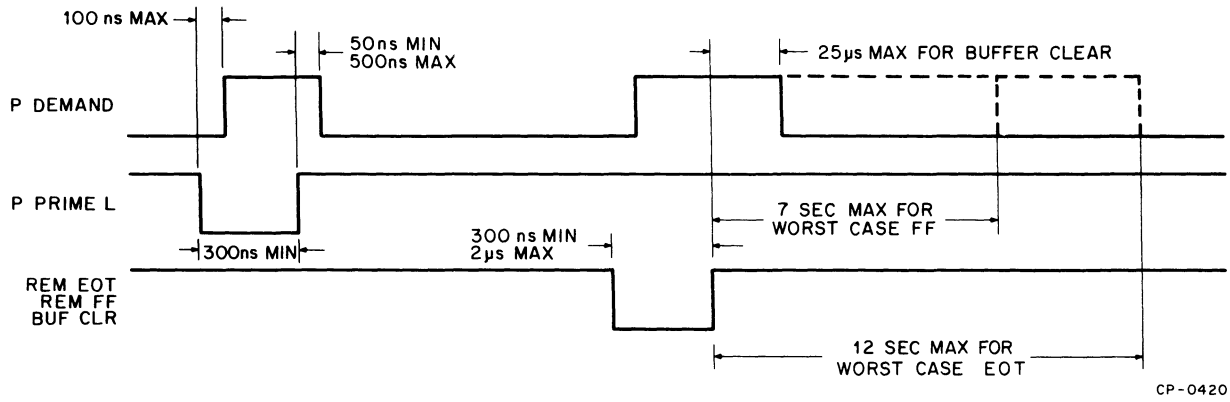


Figure 4-8 Remote Control Timing Diagram

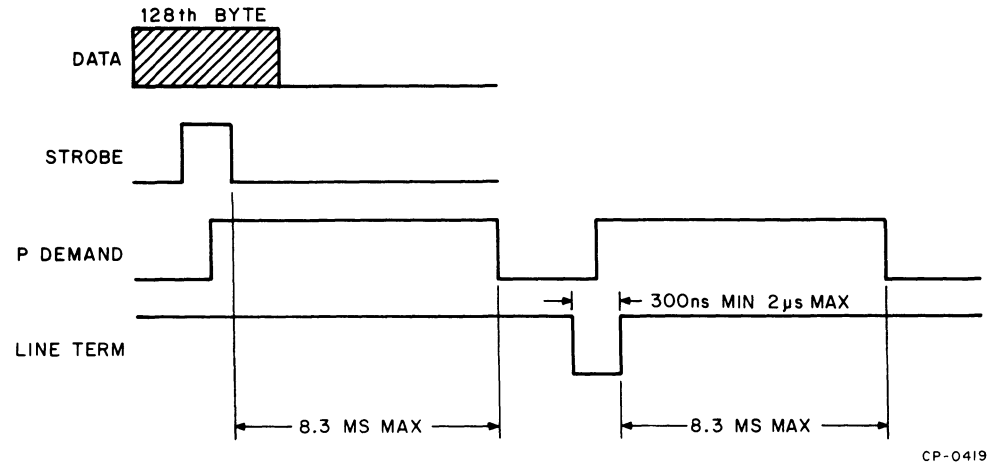


Figure 4-9 Plot Mode Timing Diagram

4.3.1 IOT Decoding

Control of the LV8 system is accomplished by using programmed input/output transfer instructions (IOTs). Seven IOT codes are used in the LV8 and an operational description of each can be found in Paragraph 3.7.

IOT codes 6650 through 6667 are decoded in the IOT decoding logic.

IOT's 6660 through 6667 are fixed by design and their function is exactly the same as the standard LP08 or LE8 line printers. No modifications to present software is necessary to output to the LV8 as a line printer.

An additional IOT has been added to implement the graphic features of the LV01 and to provide the functions of LINE TERM, REM FF, and REM EOT in the graphic or plot mode of operation. The IOT used for this function is selectable using jumpers, but the M8302 is supplied with IOT 6657 as the standard code. Any software supplied by DEC will use this code as the LPB instruction.

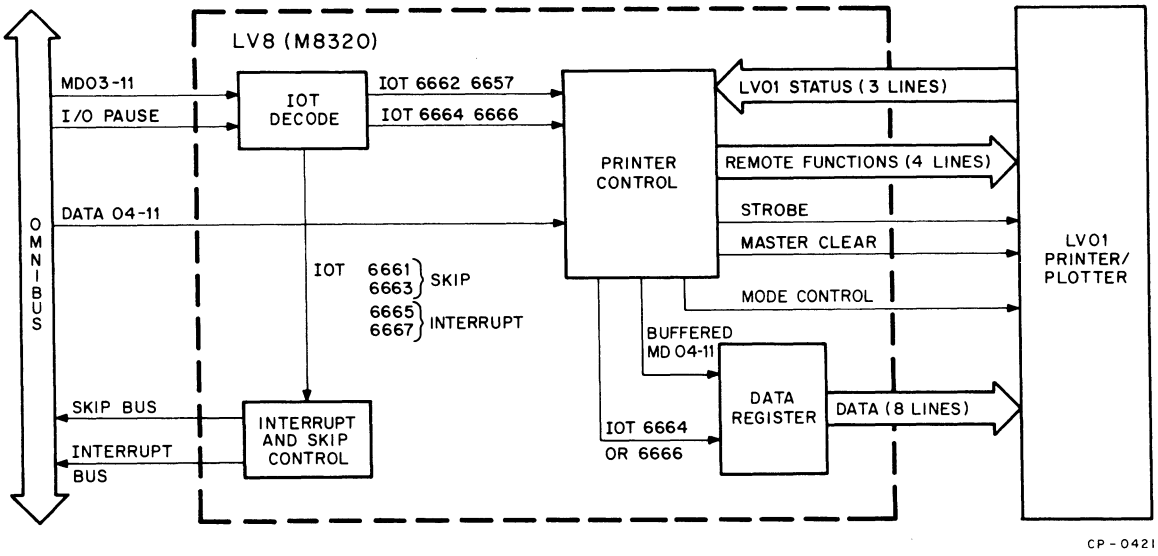


Figure 4-10 LV8 Functional Block Diagram

Decoding of these codes is accomplished by examining the state of MD03 through MD11 and I/O PAUSE. I/O PAUSE, when true, indicates that an IOT has been decoded by the CPU (octal code 6XXX). I/O PAUSE is used as an enable input to the Device Selection logic (E9 and E17). Pin 3 of E9 will be high during an IOT for Device code 66. This signal is inverted by E5 and used as an enable to the IOT generator (E6). The other inputs to E6 (MD09, MD10, and MD11) define the specific IOT to be performed. The signal at pin 3 of E9 is also inverted by E18 and provides the INTERNAL I/O signal to the OMNIBUS.

Pin 3 of E17 will be high during an IOT instruction for device code 65 (standard). The IOT decoding proceeds in a manner similar to that outlined for the 66 device code.

4.3.2 Printer Control

The function of the printer control is to (a) initiate the transfer of data between the LV8 Data Register and the LV01 by generating the STROBE signal, (b) provide operating mode information to determine print or plot modes of operation, (c) initiate remote functions under program control, and (d) process the LV01 status signals for use by the interrupt and skip control.

Data can be transmitted to the LV01 by loading the Accumulator Register (AC) in the CPU and performing a 6664 or 6666 IOT instruction. The decoded 6664 (pin 9 of E6) and 6666 (pin 4 of E6) are ORed by E5 and NANDed with TP3 by E5 providing a negative 100 ns pulse at pin 8 of E5. This pulse is inverted by E15 and clocks the data register. The pulse also fires a 74123 monostable multivibrator (one-shot) which produces a positive 500 ns pulse at its output (pin 5 of E3). This time period is used to allow the data lines to settle before strobing the data into the LV01. The trailing edge of this pulse fires a second one-shot whose output is used as the strobe signel to the LV01.

AC bit 11, called the mode bit, is used as the data input to the Print/Plot flip-flop. The clock input is controlled by AC bit 10 and the LDB instruction. Therefore, AC bit 10 is used as an enable to the Print/Plot flip-flop. Whenever AC 10 is true, AC 11 will be loaded into the Print/Plot control. The Print/Plot flip-flop is cleared by the INIT signal on the OMNIBUS placing the LV8 in the print mode of operation. Setting it places the system in the plot mode of operation.

During the LDB instruction (6657), the state of AC bits 07, 08, and 09 is sensed to determine if a BUF CLR, REM EOT, or REM FF is to be performed. The LOAD STATUS L signal (pin 12 of E23) is gated by the Data Bus signals and, if the Data line is true (low), fires a 74123 one-shot producing a 500 ns negative pulse on the corresponding remote function line.

The RLTER function is performed in a similar manner. However, the RLTER function is disabled during the instruction which changes the Print/Plot flip-flop to plot mode (sets it). The RC time constant associated with R8 and C41 holds E7 reset until the leading edge of the LDB instruction has passed. This disables the RLTER one-shot and prevents it from firing.

The set side of the Print/Plot flip-flop also gates the remote functions to the LV01 and prevents their use during printing operations. LV01 timing associated with REM FF, REM EOT, BUF CLR, and P PRIME L is shown in Figure 4-8. The timing for LINE TERM is shown in Figure 4-9.

The printer control also monitors the status signals from the LV01 to the LV8 interface. The ON LINE L and PAPER OUT L signals are inverted and ORed by E26 to form the error signal to the Interrupt and Flag control. The READY L signal enters on pin X of the 40 pin Berg connector and is terminated by a resistor network that matches the characteristic impedance of the interconnecting cable. It is inverted by E23 to provide a positive edge to set the Flag flip-flop. The FLAG signal is then fed to the Interrupt and Skip control as a high signal.

The Flag flip-flop can be cleared under program control by the LCF (6662) or LPC (6666) instruction. It is also cleared during an REM FF, REM EOT, BUF CLR, LINE TERM, or P PRIME L operation. The false-to-true transition of the Ready line sets the flag when the function is complete.

4.3.3 Data Register

The data register consists of eight 7474 D-type flip-flops. The data inputs to the data register are the bufferred data lines from the CPU. During an IOT instruction, these lines reflect the contents of the CPU (AC). The clock for the data register is generated by TP3 during an LLC or LPC IOT instruction. Therefore, the contents of the AC are transferred to the data register during the LLC or LPC instruction.

4.3.4 Interrupt and Skip Control

Two methods of data transfer, program transfer and program interrupt, may be used when programming the LV8.

Use of the first method, program transfer, involves the skip control section of the LV8 interface. The state of the flag is sensed during execution of the LSF instruction producing a skip (PC+1→MA) if the flag is set. Another instruction, LSR, is used to sense the state of the error signal produced in the printer control. Should an error exist, a low level is placed on the skip bus producing a program skip in the CPU.

Use of the second method, program interrupt, involves the interrupt control section of the LV8 interface. The interrupt control consists of the Interrupt Enable flip-flop and two 8881 bus drivers. The LSP (6665) instruction sets Interrupt Enable and an interrupt request is generated whenever an error condition exists or the Done flag is set. It is the responsibility of the interrupt service routine to determine the cause of the interrupt and service it accordingly. The LCP (6667) instruction disables the program interrupt control by clearing the Interrupt Enable flip-flop. Interrupt Enable is also cleared by INIT on the OMNIBUS.

CHAPTER 5
MAINTENANCE

LV01 Printer/Plotter maintenance is discussed in detail in the Versatec, Inc. maintenance manual supplied with each unit. The only maintenance tasks concerning the LV11 and LV8 interface controllers are inspection and diagnostic procedures.

5.1 INSPECTION

Inspection of the LV11 and LV8 is a visual check to ensure that the module is configured properly and not damaged.

1. Check that the LV11 module (M7258) or LV8 module (M8302) is plugged into the correct slots.

2. Check the LV01 cable for proper connection to the M7258 or M8302 module.

3. Remove and check the M7258 or M8302 for broken connections or damaged components. Look for discoloration on all surfaces and loose solder joints.

4. Check that jumpers are installed correctly as outlined in Paragraph 2.2.4.

5.2 DIAGNOSTICS

The LV11 and LV8/LV12 logic is completely checked by running MAINDEC-11-DALVA-A and MAINDEC-08-DALVA-A, respectively, for ten passes. These programs, including a program listing, are supplied with each LV11, LV12, or LV8 shipped. The program listing contains a program description and explanation, along with instructions for running the diagnostic.

READER'S COMMENTS

LV8/LV12/LV11
PRINTER/PLOTTER USER'S GUIDE
DEC-12-HLVAA-A-D

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