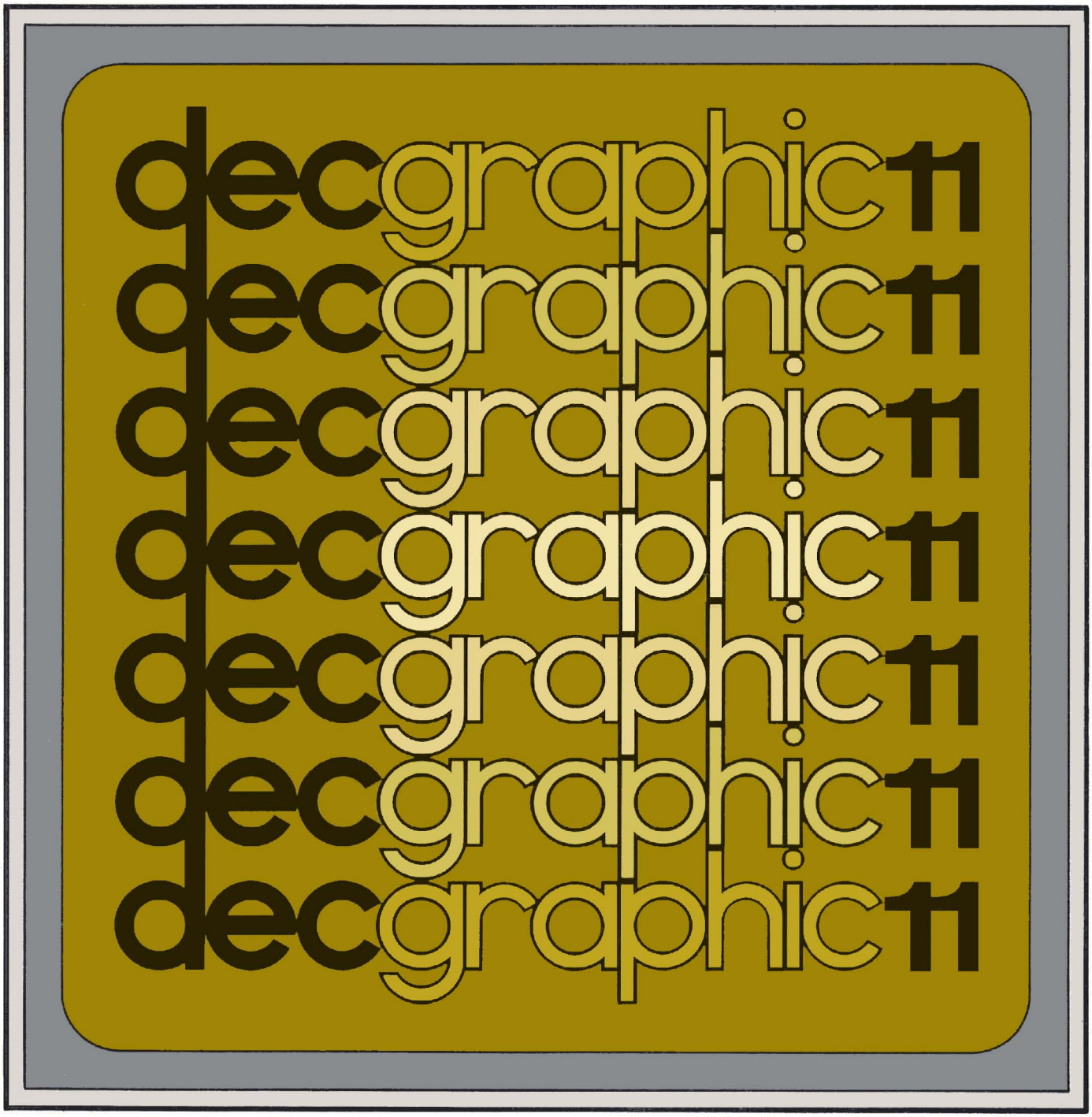
VR14/VR17 CRT display monitor user's manual



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WARNING

Maintenance procedures should be performed by qualified service personnel only.

High voltages are present within the unit and, under certain conditions, are potentially dangerous. All electrical safety precautions must be observed.

Inherent implosion protection is employed in the CRT design; however, the tube may be damaged if it is subjected to rough treatment or dropped while being removed from or installed in the display. Exercise caution during these operations.

CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

The VR14 and VR17 are completely self-contained CRT display monitors that require only analog X- and Y-position information and an intensity input, to generate sharp, bright displays. The VR14 and VR17 are electrically identical. The VR17, however, has a larger display screen (17 inches diagonal) than the VR14 (12 inches diagonal). This necessitates a correspondingly larger enclosure, and a CRT support bracket for the VR17. Except for the CRT itself, both VR14 and VR17 are composed of fully solid state circuits, utilizing high-speed magnetic deflection to enhance brightness and resolution. The inputs for the X- and Y- deflection may be balanced or single ended, bipolar or offset, and positive- or negative-going without any modification to the VR14/VR17.

The VR14 and VR17 come in several configurations, listed in Table 1-1.

Table 1-1
VR14 and VR17 Configurations

Designation	Mounting	Power	Light Pen Option
VR14-0	Rack	115 V	No
VR14-A	Rack	230 V	No
VR14-B	Rack	100 V	No
VR14-C	Table	115 V	No
VR14-D	Table	230 V	No
VR14-E	Table	100 V	No
VR14-LC	Table	115 V	Yes
VR14-LD	Table	230 V	Yes
VR17-LC	Table	115 V	Yes
VR17-LD	Table	230 V	Yes

The VR14 versions without the light pen option contain a W682 Intensity Control Circuit Board and a G838 Fault Protection Circuit Board, as well as a front panel CHANNEL switch which operates with the W682 board. In this variation, intensity pulses may be time multiplexed or gated by a separate input to allow the screen to be timeshared by two inputs.

The VR14/VR17 versions with the light pen option (VR14-LC, VR14-LD, VR17-LC, VR17-LD) do not have this timesharing capability nor channel selectivity. They contain a W684 Intensity Control Circuit Board in place of the W682, and a G840 Light Pen Amplifier in place of the G838. The G840 circuit board, however, contains the fault protection circuitry of the G838 board.

1.2 SPECIFICATIONS

VR14/VR17 specifications are as follows:

Physical:

	VR14	VR17
Height	10-1/2 in. (267 mm)	15 in. (381 mm)
Width	19 in. (483 mm)	21-1/2 in. (546 mm)
Depth	17 in. (432 mm)	27 in. (686 mm)
Weight	75 lb (34 kg)	85 lb (39 kg)
Viewable Area	6-3/4 in. X 9 in. (171.45 X 228.6 mm)	8-1/4 in. X 11 in. (210 X 280 mm)

VR14 and VR17

Spot Size:

≤ 20 mils inside the usable screen area at a brightness of 30 fL

Jitter:

≤ ±1/2 spot diameter

Repeatability:

≤ ±1 spot diameter

(Repeatability is the deviation from the nominal location of any given spot)

Gain Change:
From a fixed point on the screen, less than ±0.3% gain change for each ±1% line voltage variation

Temperature Range:
0° to 50° C (operating)

Relative Humidity:
10% to 90% (noncondensing)

Brightness:
≥ 30 fL for VR14, ≥ 25 fL for VR17; measured using a shrinking raster technique

Linearity:
Maximum deviation of any straight line is ≤ 1% of the line length, measured perpendicular to a best-fit straight line.

Deflection Method:
Magnetic (70° diagonal deflection angle)

Focus Method:
Electrostatic

High Voltage:
10.5 kV dc nominal (voltage proportional to input line voltage). Supply is self-contained and equipped with a bleeder resistor.

Shielding:
CRT is fully enclosed in a magnetic shield.

Overload Protection:
Unit is protected against fan failure or air blockage by thermal cutouts. Power supply and amplifiers are current limited. Phosphor protection is provided against fault conditions.

Deflection Amplifier

a. Deflection amplifiers are dc coupled and are capable of sustaining a full screen ac or dc deflection at environmental extremes.

b. Input Specifications:

1. Inputs are differential.

2. Differential input impedance, 5 kΩ minimum.

3. Input sensitivity, 500 mV/inch maximum (200 mV/inch with resistor change)

4. Common mode rejection ratio, 40 dB

5. Maximum operating input, ±6 V. (Maximum operating input is the sum of the common mode input and the differential input.)

6. Input offset not to exceed ±1/2 peak-to-peak input signal.

7. Maximum nonoperating input, ±50 V

c. Full screen deflection and settling time to within ±1 spot diameter, ≤ 18 μs.

d. Small signal settling time to within 1/2 spot diameter, ≤1 μs for a 0.1 inch deflection

e. Small signal linear slew rate, ≥ 0.4 inch/1 μs

f. Velocity error coefficient, 500 ns maximum (average ramp delay between input and output)

Z-Axis (on VR14 without Light Pen Option)

a. Z-Input – A negative transition from ≥ +2.4 V, but not exceeding +8 V, to ≤ +0.8 V, but not more negative than −4 V, in ≥ 20 ns, causes an unblanking pulse at the CRT cathode from approximately +62 V to ground with a duration of ≥ 200 ns at the 50 percent points. Delay between the 50 percent point of the negative input transition to the 50 percent point of the output pulse is less than 100 ns. Driver must sink 4 mA.

b. Z-Direct – A positive-going pulse not exceeding 65 V, but at least 45 V in height and not exceeding 10 μs, but at least 1 μs in duration, unblanks the CRT to a viewable intensity. This signal is ac coupled to the CRT grid.

c. Channel Select – With the Channel Select Switch in the Channel 1 position, a positive level of greater than +2.4 V, but not exceeding +8 V, enables the Z-input circuit. A level of less than +0.8 V, but not more negative than −4 V, disables the circuit. With the switch in the Channel 2 position, a positive level disables the Z-circuit; a negative level enables it. Placing the switch in the Channel 1 & 2 position disables this input.

Z-Axis [on VR14/VR17 with Light Pen Option (VR14L and VR17L)]

a. Z-Input – This is a TTL logic signal. When a TTL low, it unblanks the CRT by causing the cathode voltage to change from approximately +62 V to ground. The CRT will remain unblanked as long as the Z-input is at a logic low.

b. Intensity 0, 1, 2 – These three signals, together with the brightness control, generate a voltage of from -80 V to 0 V on the CRT grid 1, to determine image brightness. The combination of the three intensity signals asserts one of eight possible analog voltages, which in turn is ANDed with the output of the brightness control to generate a grid voltage in the 0 to -80 V range. Thus, there are eight intensity levels at each of the infinite positions of the brightness control.

Power

a. All power supplies necessary for operation of the unit are self-contained.

b. Input Requirements

Voltage: (Selectable by tap changes)
100 V ± 10%
115 V ± 10%
230 V ± 10%
Frequency – 50–60 Hz
Power – ⩽ 500 W
Current – ⩽ 5 A
Type – Single Phase

1.3 BLOCK DIAGRAM DESCRIPTION

Figure 1-1 is the functional block diagram of the VR14 without the light pen option. The X- and Y- position signals are connected to their respective A225 Deflection Amplifier Circuit Boards. The A225s boost the input signal to a level sufficient to drive the power transistors, while also providing gain and position controls. In turn, the power transistors drive the deflection yoke that positions the electron beam on the screen. The yoke currents are then passed through a 0.5 Ω resistor that converts the yoke currents back into voltages that are used as feedback for each A225 deflection amplifier. This feedback allows the A225 to produce an exact current replica in the yoke of the input signals.

The intensity input is applied to the W682 circuit board that converts this input to a 60 V pulse which drives the cathode. The cathode pulse is negative going; this pulse turns on the electron beam, creating a spot on the screen. The W682 accepts a gating input that allows the intensity pulse to be time-multiplexed between two input sources. The G838 Fault Protection Board disables the intensity circuit in the event of a ±22 V failure. This prevents the phosphor screen from burning, as there would be no deflection under these conditions.

Line power is passed through a fuse, an on-off switch, and then through one normally closed thermal cutout switch. The switch is located on the +22 V regulator heat sink, and in the event of a fan failure or excessive temperature on the heat sink, VR14/VR17 input power will be shut off until it cools down. The line power is then connected to the power transformer, the high voltage power supply, and the fans. The high voltage supply converts the input line voltage to 10.5 kV that is connected to the CRT anode. The power transformer has three basic secondaries: a 6.3 V for filament, a 70/150 for CRT electrodes, and a 72 V center tapped for deflection. The 72 Vac is rectified and filtered to provide ±43 Vdc unregulated. This ±43 Vdc is regulated with circuits on the G836 board, along with four power transistors on the regulator heat sink assembly. The regulated output is ±22 Vdc and is distributed to the deflection amplifiers. The 70/150 ac is rectified and filtered on the G836 to generate ±80 Vdc and +400 Vdc. The -80 Vdc is used for the brightness potentiometer which is tied to the grid. One side of the brightness control is connected to another potentiometer on the G836 which can adjust the maximum brightness range of the brightness potentiometer. The +400 Vdc is supplied directly to grid 2 and also to one side of the focus potentiometer on the G836 board. The wiper of the focus potentiometer goes directly to the focus electrode on the CRT.

Figure 1-2 is a block diagram of the VR14L and VR17L, i.e., VR14/VR17 with the light pen option. Note that the G840 Light Pen Amplifier replaces the G838 Fault Protection Circuit Board. The G840 contains the G838 circuitry as well as an amplifier to detect and shape pulse outputs from the light pen. The output of the light pen amplifier is brought out of the VR14L/VR17L through pin 19 of the 24-contact amphenol connector (J17) at the rear of the display monitor.

Note that in the VR14L and VR17L, the W684 intensity control replaces the W682. The W684 allows an intensity pulse to the cathode whose duration is equal to that of the Z intensify signal. The W684 circuitry also modifies the grid 1 bias voltage, thereby allowing eight intensity levels for a particular setting of the front panel brightness control.

All other circuits represented in Figure 1-2 are identical to those represented in Figure 1-1.

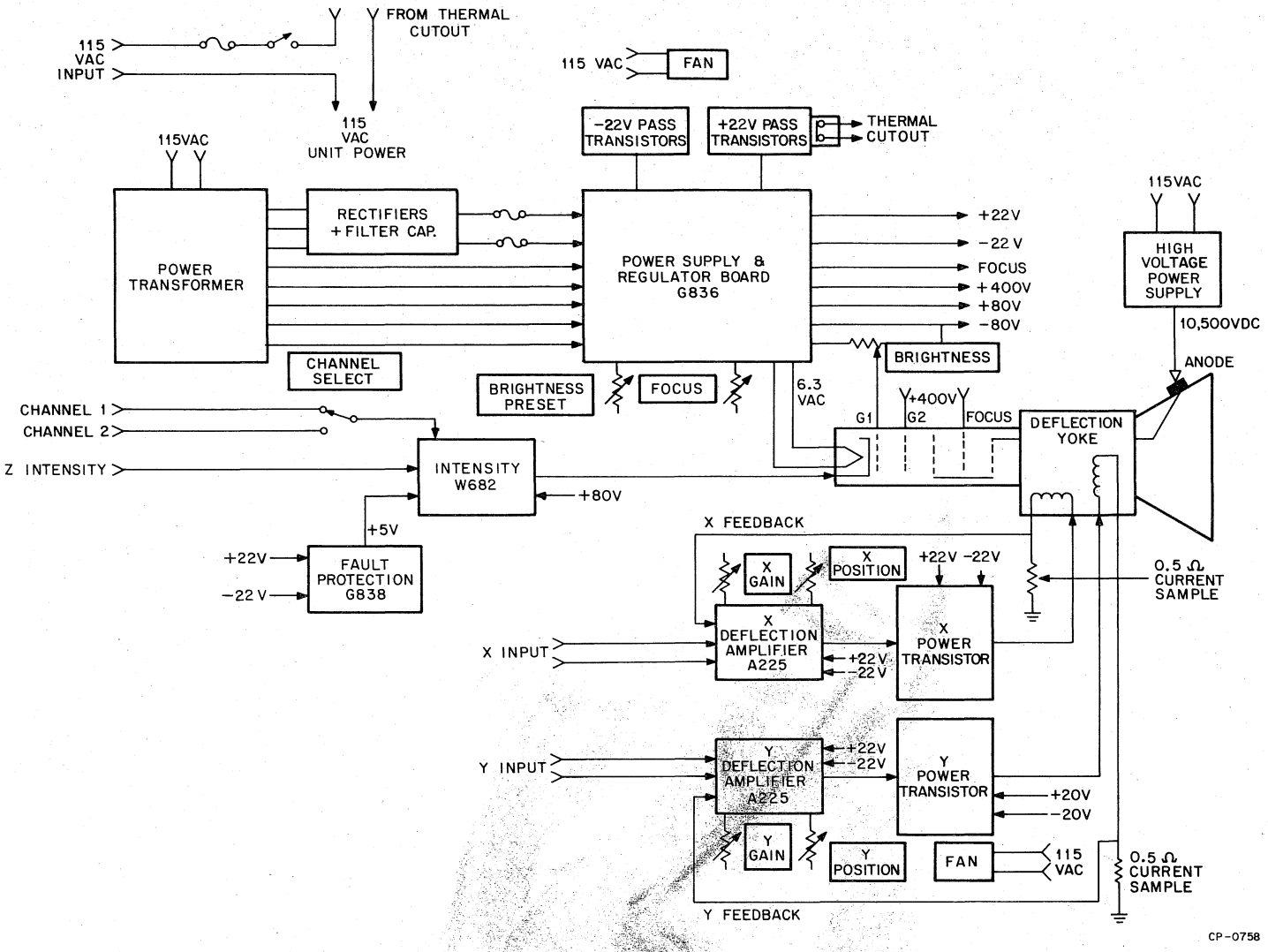


Figure 1-1 Block Diagram of VR14 Without Light Pen Option

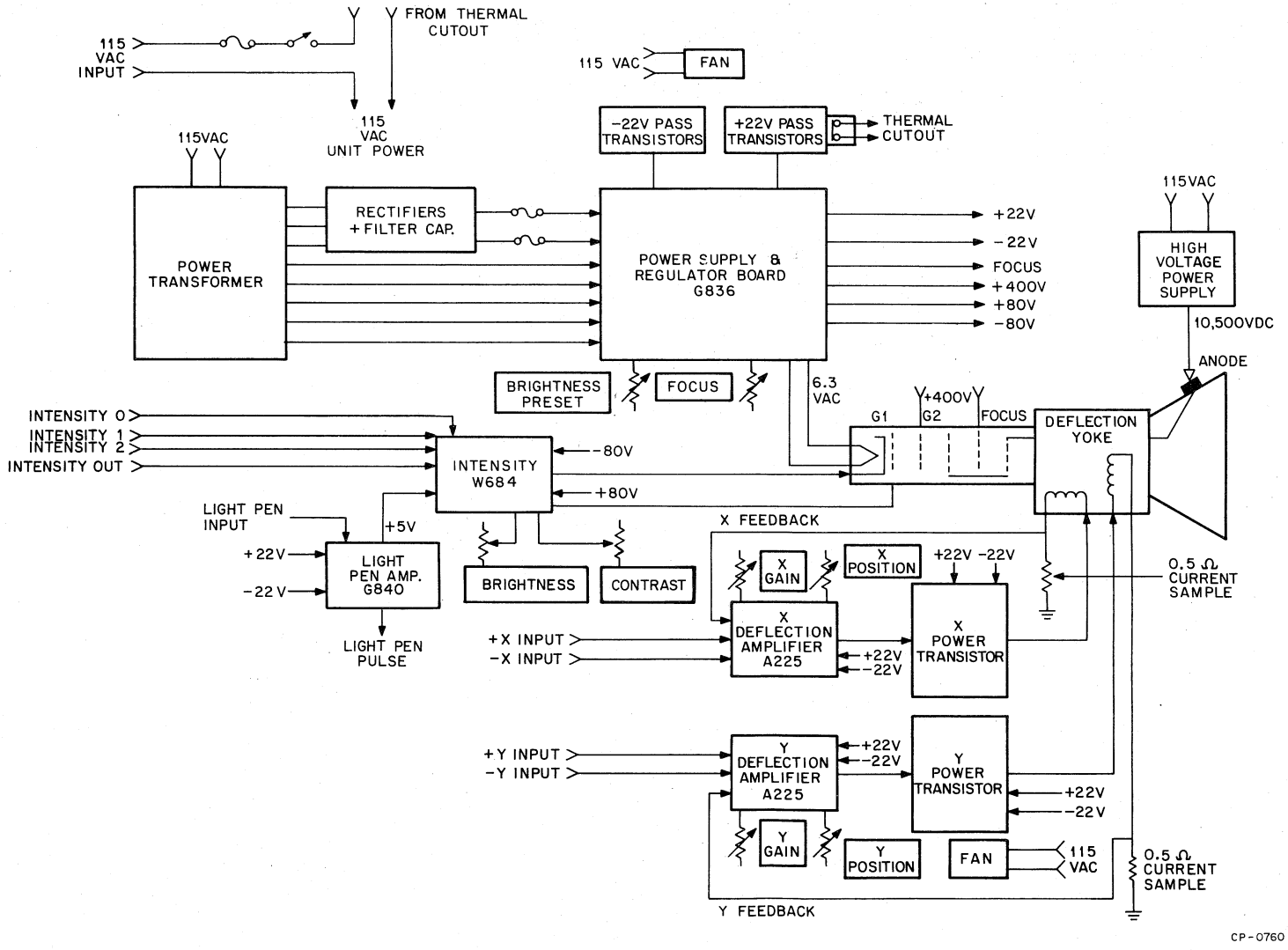


Figure 1-2 VR14L/VR17L Block Diagram

CHAPTER 2
OPERATION

2.1 INSTALLATION

The VR14 is shipped either as a standard RETMA 19 inch by 10-1/2 inch (10-7/16 inch) rack-mounted unit or as a table-top model (without chassis slides) with its own decorator cover. The VR17 comes only in a table-top model. The VR14/VR17 can operate from a power line frequency between 47 and 63 Hz. The input line voltage, however, is specified by a letter designation after the VR14/VR17 (0,C is 115 V; A,D is 230 V; and B,E is 100 V). The VR14/VR17 can operate with any of the three input line voltages simply by changing the jumpers and interconnections on TB1 and TB2 (Figure 2-1 and drawing D-CS-7007084-0-1).

Equipment cooling is the most important VR14/VR17 installation requirement. Fans draw air from the bottom of the unit; therefore, at least 1 inch of free air space must be provided below the bottom chassis. The table-top model keeps the bottom 1 inch above the table surface. In the rack-mounted unit, if equipment is mounted immediately below the VR14, as long as there is open area under the VR14 fans (a screen is acceptable; a solid plate closer than 1 inch is not), proper cooling can occur. The same requirements apply, on the rack-mounted unit, to the area immediately above the unit. The table-top model has a solid top cover. The cooling air exits from the rear of the unit. Therefore, at least 2 inches of free space must be provided immediately behind the unit. (Do not push the VR14/VR17 flush against a wall or solid vertical surface that would cut off air circulation.)

NOTE

Before applying power to the VR14/VR17, ensure that the position potentiometers are set for the particular input signals being used. Because of the universal nature of allowable input signals, the deflection amplifiers may be driven into saturation far off screen by position settings. Leaving the deflection amplifiers saturated way off screen continuously may cause damage. See Paragraph 2.5 and Table 2-2 for proper settings.

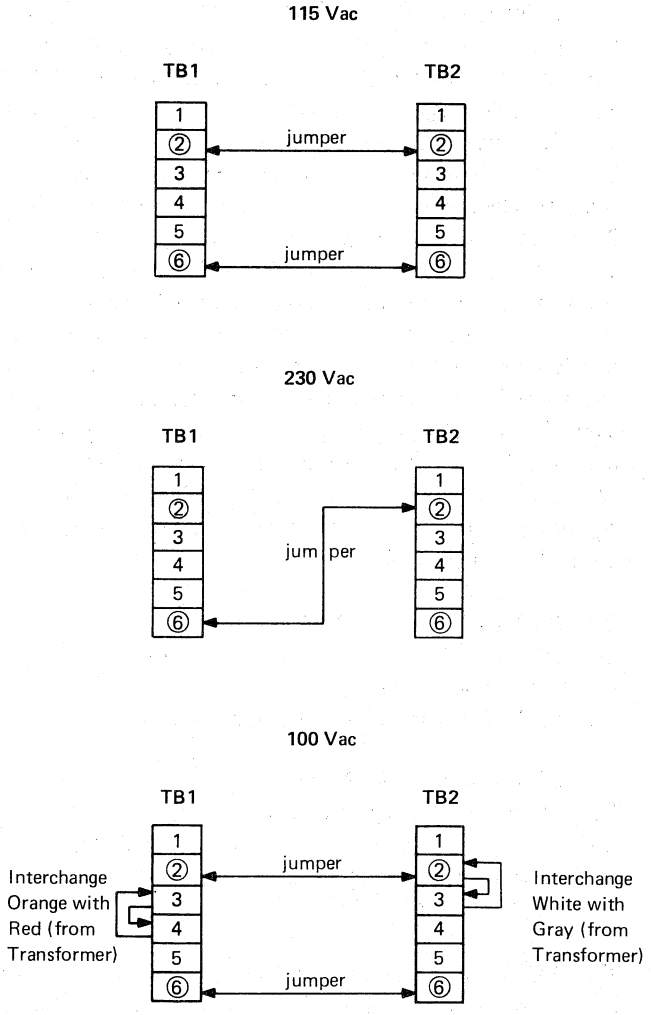


Figure 2-1 Input Power Jumper

2.2 FRONT PANEL CONTROLS

The on/off, brightness control, and the channel select control (not applicable to VR14L/VR17L) are located on the front panel. The on/off switch turns on input power to the VR14/VR17 when the knob is rotated clockwise from the maximum counterclockwise off position. Turning the knob clockwise also increases the brightness of the dis-

played information. A delay of about 30 seconds occurs before information appears on the screen while the CRT filament warms up. In an operating system, it is recommended that power be left on the display even when it is not in continuous use so that the filament warmup delays do not occur.

The channel select switch on VR14s without the light pen option works in conjunction with the channel select signal applied at the rear connector. When not using the dual-channel feature, the select switch should be in the 1 & 2 position. When using the dual-channel system, points on the screen will be intensified from Z-intensity inputs only when the channel select signal at the rear connector is high and the channel select switch is in the Channel 1 position. If the channel select input signal goes low while the select switch is at 1, intensification ceases. On the other hand, the Channel 2 position works in the opposite manner. If the channel select input signal is low and the select switch is at 2, Z-intensification signals will intensify on the screen. Thus, if a group of information points is to be separated from another group, separation can be achieved by having group 1 intensification pulses occur only when the Z-select line is high, and group 2 intensification pulses occur only when the Z-select line is low. Channel select position 1 & 2 overrides the select input signal and displays every intensification pulse of both channels at once. To observe only Channel 1 information, select Channel 1 and all Channel 2 signals are locked out. By selecting Channel 2, only Channel 2 signals are displayed.

2.3 REAR PANEL CONNECTORS

The rear panel has an Amphenol 14-contact connector (J18) and an Amphenol 24-contact connector (J17). Tables 2-1 and 2-2 list rear connector pin assignments.

2.4 INTERNAL CONTROLS

The VR14/VR17 internal adjustments include six potentiometers: X position, X gain, Y position, Y gain, focus, and brightness preset. Access to the adjustments is gained by removing the case cover (Figure 2-2).

The gain and position adjustments are located on the top, left central portion of the VR14/VR17 (as viewed from the front). The two forward potentiometers on the deflection circuits are the horizontal gain on the left, and vertical gain on the right. The two rear potentiometers are the horizontal position on the left, and the vertical position on the right.

The gain adjustments allow the VR14/VR17 to accommodate a range of input signal amplitudes and expand or contract the horizontal and vertical deflection to suit full screen requirements. The position controls accommodate a variety of input signals and allow offset inputs to be centered on the CRT screen. Once initially adjusted for the particular input signals used, the gain and position controls rarely have to be adjusted. Gross positioning off screen or excessive gain deflecting off the extremities of the screen should be avoided, since the deflection amplifiers will go into current limiting and may overheat if allowed to stay in this condition any length of time. Turning the X and Y gain controls clockwise, increases the gain or displayed image size. Turning the X and Y positions clockeise moves the displayed information right and up, respectively.

The focus and brightness preset adjustments are located at the top, right central portion of the unit. They are on the power supply regulator circuit (G836) that is somewhat recessed from the top of the unit. The brightness preset is the rear-most of the two. This potentiometer allows the range of the front panel brightness control to be limited to any maximum brightness desired. Turning the brightness preset counterclockwise increases the maximum brightness range of the front panel control. Generally, this control is set so that at maximum brightness setting on the front panel knob, the displayed information does not "bloom" causing a degradation in resolution. The focus potentiometer is in front of the brightness preset. The adjustment is quite insensitive and requires several turns to go through focus.

The VR14L and VR17L also contain a contrast adjusting potentiometer (R29), located on the W684 module. It is accessible from the top of the VR14/VR17. This control is used to extend or contract the brightness range of the CRT display. It does not normally have to be changed after an initial adjustment is made to compensate for component variations.

2.5 INPUT SIGNAL REQUIREMENTS

NOTE

The deflection amplifiers must not be driven so that the CRT beam is off screen for any length of time or permanent damage may occur. Ensure that input deflection signals fail to a safe, on-screen value.

The VR14/VR17 requires analog voltage inputs for X- and Y-deflection, and a logic level change or pulse for intensify. The X- and Y-inputs are identical. However, because the CRT is a 3 X 4 rectangle, only 3/4 of the horizontal deflection is required for full vertical deflection. The deflection inputs are differential but may be driven from single-ended sources. When using single-ended sources, the differential input is helpful in eliminating annoying ground loops and hum. By carrying the "local" common or ground

Table 2-1
J17 Rear Connector Pin Assignments

J17 24-Pin Connector	Destination	VR14		VR14L/VR17L	
		Signal Name	Function	Signal Name	Function
Pin 1	A4 L	Z-Select	High input enables Z-intensify to occur if channel select switch on 1. A low input enables Z-intensify to occur if channel select switch on 2.	Intensity 2	Determines intensity level
Pin 2	A4 B		Not Used	Intensity 0	Determines intensity level
Pin 3	A4 K		Not Used	Intensity 1	Determines intensity level
Pin 4	A4 J	Z-Input	When this input goes from high to low, an intensify pulse is generated.	Z-Input	When this input is low, an intensify signal is applied to the CRT.
Pin 5	GND				
Pin 6	GND				
Pin 7	A2 B	-X Input	One side of X-input signal line	-X Input	One side of X-input signal line
Pin 8	A2 E	+X Input	Other side of X input signal line (ground for single ended input)	+X Input	Other side of X-input signal line (ground for single ended input)
Pin 9	A2 H	X-Signal GND	X signal reference ground	X-Signal GND	X signal reference ground
Pin 10	A3 B	-Y Input	One side of Y-input signal line	-Y Input	One side of Y-input signal line
Pin 11	A3 E	+Y Input	Other side of Y input signal line (ground for single ended input)	+Y Input	Other side of Y input signal line (ground for single ended input)
Pin 12	A3 H	Y-Signal GND	Y signal reference ground	Y-Signal GND	Y signal reference ground
Pin 13	A4 D	Z-Direct	Input signal that directly modulates CRT grid (ac coupled)		Not Used
Pin 14	N/C				

Table 2-1 (Cont)
J17 Rear Connector Pin Assignments

J17 24-Pin Connector	Destination	VR14		VR14L/VR17L	
		Signal Name	Function	Signal Name	Function
Pin 15	J18–Pin 4		Not Used	Bell (Speaker)	Used in LK40 option
Pin 16	N/C				
Pin 17	J18–Pin 5		Not Used	+KB Signal	Used in LK40 option
Pin 18	J18–Pin 6		Not Used	-KB Signal	Used in LK40 option
Pin 19	A1 H		Not Used	Light Pen Out	Amplified light pen pulses
Pin 20	J18–Pin 12		Not Used	+5 V IN	Used in LK40 option
Pin 21	N/C				
Pin 22	J18–Pin 8	+22 V	+22 V is available if J18–Pin 8 is jumpered to J18 pin 1.	+22 V	+22 V is available if J18–Pin 8 is jumpered to J18 pin 1.
Pin 23	J18–Pin 10	-22 V	-22 V is available if J18 pin 10 is jumpered to J18 pin 3.		-22 V is available if J18 pin 10 is jumpered to J18 pin 3.
Pin 24	J18–Pin 9	GND	J18 pin 9 must be jumpered to J18 pin 2.	GND	J18 pin 9 must be jumpered to J18 pin 2.

Table 2-2
J18 Rear Connector Pin Assignments

J18 14-Pin Connector	Destination	Signal Name	Function
Pin 1	+22 V Regulated	+22 V	For VR14/VR17 options
Pin 2	GND	GND	For VR14/VR17 options
Pin 3	-22 V Regulated	-22 V	For VR14/VR17 options
Pin 4	J17 Pin 15	Bell (Speaker)	Used with LK40 option
Pin 5	J17 Pin 17	+KB Signal	Used with LK40 option
Pin 6	J17 Pin 18	-KB Signal	Used with LK40 option
Pin 7	N/C	Not Used	
Pin 8	J17 Pin 22	+22 V	Jumpered from J18 pin 1 to J18 pin 8 by P18
Pin 9	J17 Pin 23	GND	Jumpered from J18 pin 2 to J18 pin 9 by P18
Pin 10	J17 Pin 24	-22 V	Jumpered from J18 pin 3 to J18 pin 10 by P18
Pin 11	N/C		
Pin 12	J17 Pin 20	+5 V	Provides +5 V to LK40 option
Pin 13	GND	GND	Provides GND to LK40 option
Pin 14	-22 V	-22 V	Provides -22 V to LK40 option

along with the deflection signal from where it is generated, a quasi-differential signal is generated. Instead of terminating this ground at the VR14/VR17 chassis, use the ground as if it were one side of a differential signal (the other side being the deflection signal itself). The VR14/VR17 uses the deflection signal with respect to its own ground and not the VR14/VR17 ground, which, most likely, is different and could cause picture ripple and hum. If a separate ground is not available, the single deflection signal is applied to one side of the differential input. The remaining differential input is terminated with the source impedance of the driving signal or, if this is low, the input is simply grounded (signal ground not chassis ground). (Signal ground is pin 9 and pin 12, X- and Y-signal ground, respectively.) Never use chassis ground for X- and Y-input reference – always use signal ground. When using balanced or differential inputs, tie each side of the twisted-pair shielded cable to the two inputs and the shield to the signal ground. The importance of using signal ground cannot be overstated; most noise and washing displays are a result of indiscriminate grounding.

The minimum voltage signal for full X-deflection is 2 V peak-to-peak and 1.7 V for Y when R1 and R2 on the A225 are 3.3 kΩ (Figure 3-1). For larger input signals, R1 and R2 are normally 10 kΩ. With 10 kΩ, the maximum input sensitivity is 0.5 V/inch. The input impedance is 5 kΩ minimum for maximum sensitivity (R1 and R2: 3.3 kΩ)

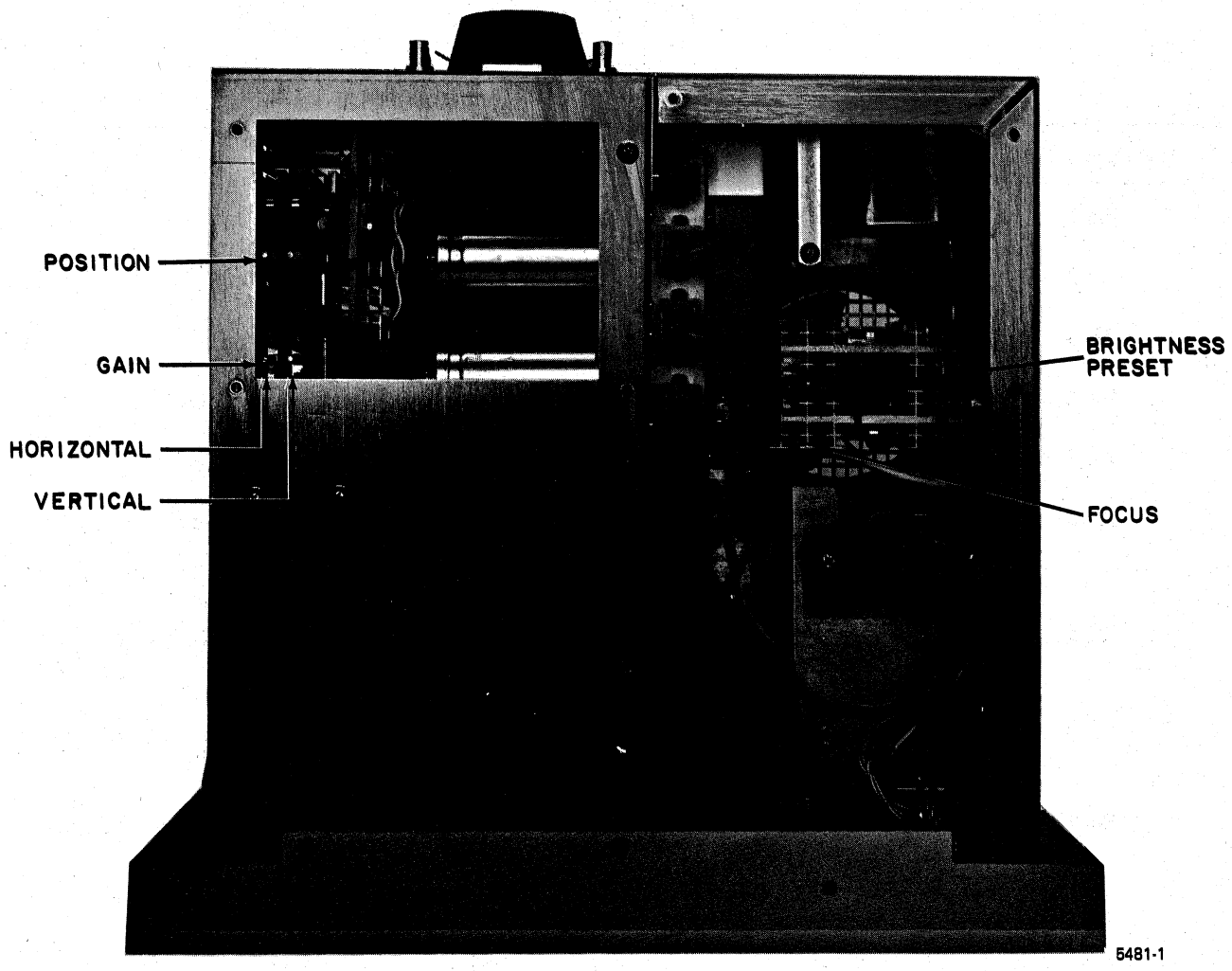


Figure 2-2 Locations of Internal Controls

and 20 kΩ minimum for R1 and R2 = 10 kΩ. When driving long cables (more than 30 feet), high-speed deflection may not be possible unless the cables are terminated in a low impedance (less than 100 Ω) since the VR14/VR17 input impedance is too high for this application.

Input signals larger than 2 V may be used by attenuating with the gain controls and R1 and R2 on the X- and Y-deflection circuit boards. However, the potentiometers become much too sensitive for input signals greater than 10 V peak-to-peak and R1 and R2 should be increased to provide pre-attenuation for these larger input signals. The input signals may be bipolar such as ±5 V or unipolar such as 0 V to +5 V or 0 V to -5 V. The position potentiometer allows the deflection to be offset plus or minus half a screen; thus, a unipolar signal may be completely centered on the screen. Offsets more than half of the full-scale inputs cannot be handled. In other words, if the full-scale deflection is offset from 0 V by more than half its full scale value, centering on the screen cannot be accomplished. A 3 V peak-to-peak deflection signal, for example, may not be offset from 0 by more than ±1.5 V. So ±1.5 V, 0 V to -3 V or 0 V to +3 V are all acceptable, but a deflection input that goes from +1 V to +4 V cannot be used until it is shifted down a minimum of 1 V. Table 2-3 summarizes the control settings for various inputs.

Table 2-3
Control Settings

Input Deflection	Position Setting
±2 V to 5 V 0,0 = center +2 V to +5 V is up and to right	With no inputs, set X- and Y-position potentiometers to get 0 V at A02-A (for X) and A03-A (for Y).
0 V to +2 V to +5 V 0,0 = upper right screen	With no inputs, set −2.2 V @ A02-A, A03-A with X- and Y-position potentiometers.
0 V to −2 V to −5 V 0,0 = lower left	With no inputs, set +2.2 V @ A02-A, A03-A with X- and Y-position potentiometers.

The Z-intensify input requirement is simply a TTL transition from high to low. In VR14s using a W682 Intensity Control, this triggers the intensity circuit to generate a 300 ns intensify pulse. In VR14Ls and VR17Ls, which use the W684 Intensity Control, the intensify circuit is triggered, and remains active, until Z-intensify goes high.

NOTE

The intensify signal must be delayed from the X- and Y-position signal for an appropriate length of time to allow the deflection coil to settle the electron beam to its required position. Failure to do so displays smeared dots that are located incorrectly on the screen. Also, at least a 500 ns waiting period must be allowed to intensify a dot before commanding the electron beam to move to its next location. Not giving enough time to intensify a dot after the deflection is settled will also smear the dot, since the deflection amplifier will start "dragging" the dot to the new position. The amount of delay required from the time new X- and Y-position information is presented to the VR14/VR17 and the intensify pulse is requested depends upon how large a position change is requested and how perfectly settled the dot has to be to its final ideal position. Full-scale deflection changes, such as far left to far right or corner to corner, require a 20 μs waiting period for the dot to settle to within 0.01 inch of its final value. If larger errors can be tolerated, 18 μs may be used. Small deflection changes require much less time. A 0.1 inch change can be settled in less than 1 μs. If there is no way for the circuits driving the VR14/VR17 to distinguish small position changes from large ones, each change must be assumed to be large and thus requires the worst-case delay. Also, if the D/A converters driving the display have "gliches" (error spikes generated while changing values), proportionately longer delays are required since the deflection amplifiers have to recover from the "gliches."

The Z-direct input (applicable only to VR14s without light pen option) allows direct modulation of the brightness. Positive-going signals increase brightness. This input is not direct coupled; therefore, dc brightness information cannot be used. The RC time constant is approximately 30 ms. The Z-direct may be used with or without the Z-intensify input. If Z-direct is used with Z-intensify, it can alter the brightness of the normal intensify pulse by adding or subtracting at the CRT grid. This is accomplished by pulsing the Z-direct with a pulse of equal duration with the Z-intensify. By varying the amplitude and polarity of the Z-direct pulse, the dot will be of a different brightness. When using Z-direct without the Z-intensify (such as for vector intensity control or any other non-point plotting application) the signal must be large enough to overcome the CRT cutoff. A typical direct signal will have 5 V to 10 V of actual brightness information riding on top of a 40 V pedestal; the 40 V pedestal ensures that the CRT will reside below cutoff.

The Z-select input (applicable only to VR14s without light pen option) works in conjunction with the front panel channel select switch. The Z-select allows the Z-intensify pulse to be gated or time multiplexed. When the channel select switch is on the 1 & 2 position, Z-select inputs have no effect on the VR14. When the channel select switch is in the 1 position, Z-intensification occurs only when Z-select input is a TTL high. When the channel select switch is at 2, Z-intensification occurs only when Z-select is held at a TTL low. Thus, if two separate pieces of information are to be displayed, by placing Z-select at a high only during Channel 1 intensification times, and low only during Channel 2 intensification times, both curves will be displayed when the channel select switch is at 1 & 2, and only Channel 1 when Channel 1 is selected, and Channel 2 when Channel 2 is selected.

In the VR14L and VR17L, brightness level is a function of three input signals [Intensity (2:0)], as well as the front panel brightness control. These input signals combine in the W684 module to generate a voltage which is applied to grid 1 of the CRT, establishing a particular brightness level.

CHAPTER 3
THEORY OF OPERATION

3.1 X- AND Y-DEFLECTION CIRCUITS

The X- and Y-deflection circuits are identical; therefore, only one axis will be described. The deflection circuit consists of the A225 circuit board, two power transistors, and a deflection yoke (Figure 3-1). The input signal is applied to pins E and B on the A225 circuit board. The input signal is handled as a differential or balanced signal, even if the input is driven from a single-ended source (the single-ended source being a special case of a balanced input where one side is grounded). R1 and R2 establish the minimum input impedance and form an attenuator with R3, the gain potentiometer. The voltage developed across R3 is amplified and converted from balanced to single-ended by amplifier E1. E1 is an inverting amplifier whose gain is established by the resistor ratios of R7 to R4 and R6 to R5. The bandwidth of the amplifier is tailored by C5 and C6, which act internally on the integrated circuit, and C13 and C14, which act at high frequency to roll off the low frequency gain established by the R7 to R4 and R6 to R5 ratios. A ±6 V is generated for both E1 and E2 from the ±22 V. This is done by dropping resistors R18 and R19 and Zener diodes D5 and D6.

C1 and C3, and C2 and C4 are local high frequency bypass filters for the ±6 V to reduce any high frequency signal noise at each operational amplifier, thus avoiding the possibility of parasitic oscillation. The single-ended output of E1 is conducted to R11, which is the input to the actual deflection amplifier; E1 serves more as a signal conditioner-preamplifier.

The amplifier is essentially an inverting voltage-to-current amplifier, i.e., an input voltage is converted to an output current 180° out of phase or inverted with respect to this input. Because the input is a voltage, however, the output current must be converted back into a voltage in order that the feedback compare volts with volts. Current is converted to voltage with a 0.5 Ω resistor in series with the yoke. The voltage across this resistor is an exact replica of the current flowing in the yoke; thus, the amplifier compares the input voltage with the yoke current to ensure that the yoke current is an exact replica of the input position signal. E2 compares the input voltage at R11 with the feedback voltage at R31, R10.

Because the amplifier has voltage gain, only a small voltage is needed between pins 10 and 9 of E2 to cause large changes in the output. Pin 9 of E2 is referenced to ground through R13, which is strictly an impedance balancing resistor that minimizes offsets in E2 due to temperature changes. Therefore, pin 9 is essentially grounded. If any voltage appears at pin 10 of E2, the output will immediately respond in a manner that tends to reduce the voltage at pin 10 to zero; thus, a null is always achieved at pin 10 of E2. If a variable voltage is present at the input of R11, the output (or yoke current) will vary in such a manner that a continuous null is achieved at pin 10. The only way this can occur is if instantaneously the yoke current undergoes exact equal and opposite changes to those occurring at the input to R11. Therefore, the yoke current will be an exact but opposite polarity replica of the input voltage.

In absolute numbers, the actual yoke current versus input voltage can be determined by comparing resistor ratios. For example, if +1 V is applied to the input of R11, 1 mA will flow through R11. This occurs because the amplifier forces pin 10 of E2 to 0 V; thus, one side of R11 is 0 V, the other is 1 V, so 1 mA flows. This current does not flow into pin 10 of E2 because, if it did, pin 10 would rise in voltage because the input of E2 looks like a high impedance. The current must flow through R10 and R31. This occurs only if the feedback voltage is a negative value, because R10/R31 is tied to pin 10 which is 0 V; so pin A must be negative. In fact, if 1 mA flows through R10 and R31, the feedback voltage must be 3.2 V and negative. The -3.2 V originates from the 0.5 Ω resistor in series with the yoke; therefore, -3.2 V divided by 0.5 Ω current is flowing through the yoke. This, of course, is -6.4 A which is an excessive amount of voltage, and current limit circuits (explained later) would probably be called into action to limit the output transistors.

The remaining transistors on the A225 boost the current from E2 to a sufficient drive level to operate the power transistors on the large heat sink. The output of E2 drives Q1 through its base resistor R14. Q1 serves two purposes: a stage of inversion and a level shifter. Inversion is necessary to get the final output in the proper polarity for negative feedback. Level shifting is required to drive Q2 at its base voltage; E2 cannot do this alone. The Q1 stage has no voltage gain but has current gain. Q2, however, has voltage and current gain and is where the true output voltage is first generated. Q2 is a "grounded" emitter amplifier where, in this case, the emitter, although tied to +22 V, can be considered "grounded" and the collector resistor R23 is not tied to -22 V but, for analysis, tied to -44 V. Q2 has the capability of swinging its collector almost a full ±22 V. This large swing is necessary for the yoke, which must swing as close as possible to the ±22 V. The reason for this will be explained later.

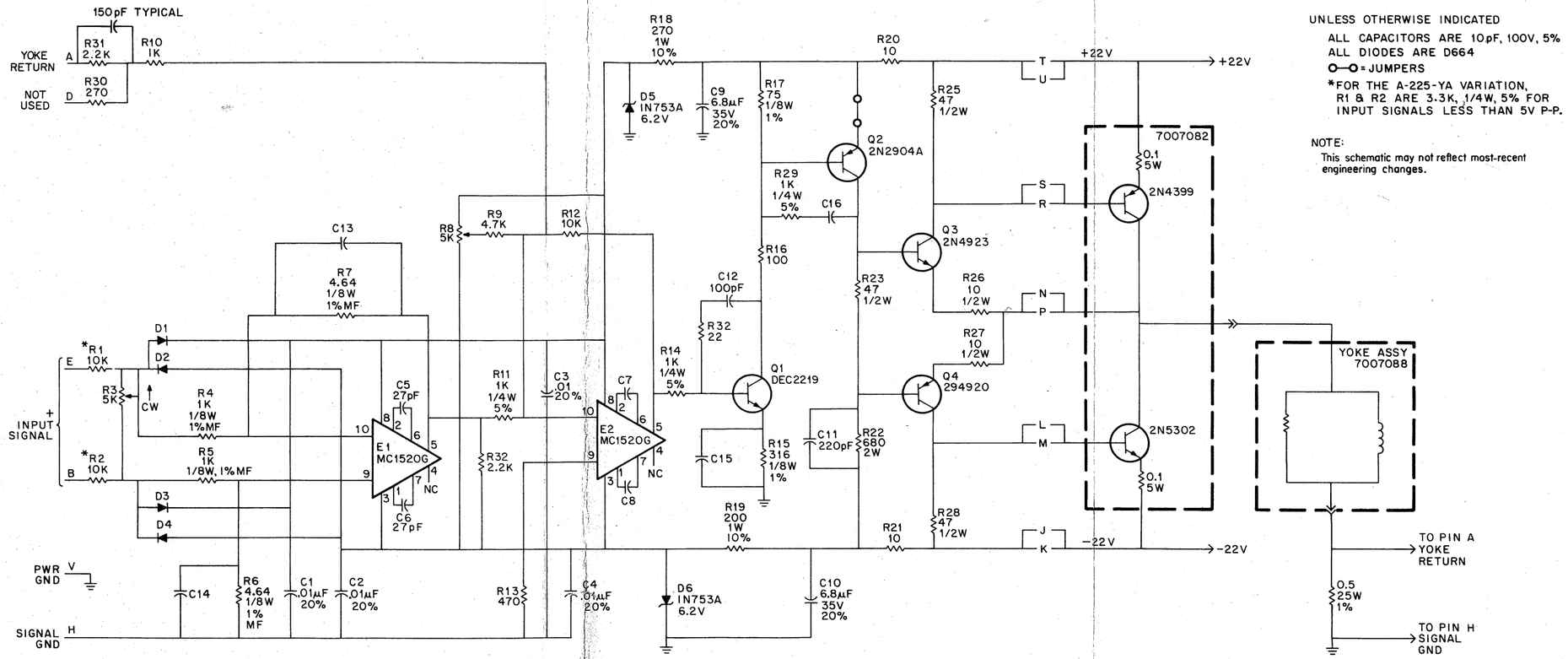
The collector of Q2 drives Q3 and Q4 which are emitter followers for the positive and negative outputs. Since a low output impedance is necessary, emitter followers are used; however, Q3 and Q4 are not capable of handling the output power necessary since each can only drive 0.5 A. A bootstrap power stage is used to raise the emitter follower current capability to the ±4 A required. This is accomplished with two power transistors on an external forced-air cooled heat sink.

These external transistors are essentially "slaved" to the Q3 and Q4 emitter followers. Because the positive swing and negative swing work in the same way, only the positive is described. When the amplifier is required to deliver positive current in the yoke, the circuit responds by turning Q2 on, thus placing a positive voltage on the base of Q3. Q3's emitter responds in a similar manner; however, it cannot supply the necessary yoke current. Still, Q3 attempts to deliver the necessary current. Unlike a normal emitter follower, Q3's collector is not tied to +20 V, but instead to the base of the 2N4399 Power Transistor, Thus, when Q3 tries to deliver the output current from its emitter, this very current must flow into Q3's collector from the base of the 2N4399 which will now turn on. Because the 2N4399's collector is also tied to the output (the yoke) it also supports the output current and, in fact, becomes the primary source of output current. Depending on Q3's demands, the 2N4399 is completely slaved to Q3. If Q3 turns on harder, so does the 2N4399. If Q3 shuts off, so does the 2N4399. Therefore, the output looks like it is an emitter follower (Q3) but the 2N4399 delivers all the current and handles the necessary power dissipation requirement.

To minimize power consumption, the output would like to operate in Class B; i.e., while positive current is required, no negative current transistors should be turned on and vice versa. However, this approach creates problems at the point where the transition between positive and negative current takes place. The reason is that one set of transistors does not shut off exactly where the other set takes over, but instead shut off prematurely. This creates a dead zone or "no man's land" where neither the positive nor the negative transistors are on and controllable. The appearance on the CRT screen of such a phenomenon is a bunching or nonlinear compression of displayed information where it occurs (usually near the center of the screen). This problem can be solved by not allowing the positive transistors to shut off at zero, but rather conduct somewhat into the opposite side's region. In so doing, the positive transistors would not shut off, for example, until the negative transistors were well turned on. Thus, the amplifier would have control to cancel any nonlinearities that might occur. This task is accomplished with R23, R26, R27. The major influence is R23 because it places voltage between Q3 and Q4 bases which allow one to be on a little into the conduction region of the other. If R23 were 0, the dead zone would be very abrupt, causing maximum distortion. On the other hand, as R23 is increased, the transistor conducts further and further into the opposite side's operating region. This creates two major problems. The power dissipation causes excessive heating of the output stage and the extra current required overloads the power supply. The value of R23 is chosen, therefore, to minimize dissipation but also to minimize the cross-over distortion.

The output at the yoke has the capability of swinging a full ±22 V. This is necessary because even though the yoke is less than 0.1 Ω at dc, it has inductance; thus, to force current through at high speeds requires a lot of voltage ($V = L \frac{\Delta i}{\Delta t}$). To change 2 A through 20 μH in 2 μs requires 20 V. That is why the A225 not only has to boost the input signal to a large current but also has to have good voltage capability to force the yoke current to change quickly.

Position control in the A225 is accomplished by adding another input to E2 exactly the way the signal comes in. This is accomplished with R9. The position "signal" is nothing more than an adjustable dc level (from R8) which, through R9, adds or subtracts voltage from the actual input signal. This allows the displayed information to move up/down, left/right on the screen or, in the case of offset input signals, allows the information to be centered on the screen.



UNLESS OTHERWISE INDICATED

ALL CAPACITORS ARE 10pF, 100V, 5%
ALL DIODES ARE D664
O—O = JUMPERS
*FOR THE A-225-YA VARIATION, R1 & R2 ARE 3.3K, 1/4W, 5% FOR INPUT SIGNALS LESS THAN 5V P-P.

NOTE:
This schematic may not reflect most-recent engineering changes.

Figure 3-1 X and Y Deflection Circuit

The remaining component on the A225 is frequency compensation which allows the amplifier to operate over its required bandwidth without oscillation. Because the amplifier must operate from dc to beyond 1 MHz, the voltage gain must be reduced continuously at higher and higher frequencies. If this were not done, excessive phase shift between input and output (from feedback) could cause the output to be in phase with the input and thus oscillate. R12, R3, R32, C16, C15, and C11 perform the required gain reduction functions. R12 reduces the open-loop gain of E2 at all frequencies. C11 reduces the gain of Q2 at high frequencies and is of major significance to the overall bandwidth. The yoke itself represents a major roll off for the amplifier, and its high frequency characteristics dominate the stability of the amplifier. An RC network across the yoke enhances the high frequency settling characteristics of the yoke.

The power output stage (2N5302 and 2N4399) is current limited by the +22 V and -22 V power supply regulators. If the deflection amplifiers are driven way off screen, the power supply limits the maximum current to 11 A. If this condition is allowed to exist, eventually either the +22 V fuse or the -22 V fuse will blow, rendering the circuit safe from such overloads.

3.2 PLUS AND MINUS LOW VOLTAGE REGULATED SUPPLY

The input line voltage is stepped down in the power transformer to approximately 36 Vrms. There are two identical secondary windings to deliver these 36 V. Both windings are connected in series, making a 72 V center-tapped winding. Using full wave bridge rectification, the ac becomes approximately 86 Vdc. By grounding the center tap, the 86 Vdc split evenly with respect to ground; thus, a +43 V and a -43 V are available with respect to ground. A filter capacitor on each ±43 V line smooths the ripple and finishes the task of generating the raw, unregulated dc for the ±22 V regulators. The regulators are contained on the G836 circuit board (Figure 3-2) and the heat sink adjacent to the G836. Since the ±22 V regulators are symmetrical, only the negative regulator is described. The ±43 V is dropped by R33 and R34 and preregulated with D5 and D6 to +12 Vdc and D7 and D8 to -12 Vdc. The ±12 Vdc are the voltages necessary to operate E1 and E2; they are also used to generate the reference voltages with which the output voltage will be compared. The reference for the -22 V regulator is made with the +12 Vdc passing through R1 and establishing +6.2 V across D1. C1 across D1 reduces the dynamic resistance of the reference by removing high frequency fluctuations. The reference voltage is delivered to R2, which ties to the summing point (pin 2) of operational amplifier E1.

The feedback from the output regulated voltage through R3 is also applied to the summing point of E1. The nature of the circuit is that a null will be maintained at pin 2 of E1. Therefore, because the voltage on R2 (reference) is stable, the only variable is the output. Whenever the output changes for any reason, the null is disturbed at pin 2 of E1; E1 then forces the output to change in a manner that returns the null. For example, if the input line voltage increases, causing the -43 V to increase, the -22 V regulated output starts to climb. The null would then be disturbed and E1 would shut the output down somewhat so that the null could be maintained. On the other hand, if a heavy load occurred on the -22 V regulator causing the -43 V to drop, the null would again be disturbed and E1 would act in a way that would turn on the output hard enough to return to its proper level, the level that maintains the null.

This regulating action takes place in a matter of microseconds. The actual output voltage at which the null will be maintained is determined by the ratio of R3 to R2 times the reference voltage. The mechanics of how E1 controls the output can be traced stage by stage. E1 drives an emitter follower, Q1, to give the output of E1 sufficient drive capability to fully turn on Q2, if required. Q2, through R12, controls the base current of the series pass transistors that are external to the G836 board. The pass transistors maintain a constant output, since they are supplied power from the raw dc source. Because of the high open-loop voltage gain, high frequency networks are used to roll off the gain of the regulator to ensure stable nonoscillatory operation. C2, R5, and C5 serve this purpose.

The output power transistors are current limited by D13 and D14. These diodes conduct whenever excessive collector current is demanded. In so doing, the diodes limit the base drive, thereby limiting the maximum fault current that may flow.

3.3 CRT ELECTRODE VOLTAGES

The CRT requires the following electrode voltages: filament, cathode, grid 1, grid 2, focus, and anode.

The filament voltage is derived from the ±3.5 Vac windings of the power transformer. The ±3.5 Vac windings are connected in series yielding 7 Vac. Due to resistance losses, approximately 6.3 Vac is provided across the CRT filament.

The 70 Vrms winding is used to provide cathode and grid 1 bias voltages. The 70 Vrms winding terminates on the G836 (Figure 3-2). Through D11, C17, R36, and C16, this winding generates a -80 Vdc by half wave rectification. The same winding, in like manner, generates +80 Vdc from D12, C18, R37, and C19. The -80 V is applied to one side of the front panel brightness potentiometer. The other side of the potentiometer returns to the brightness preset potentiometer (G836–R38). R38 setting determines the maximum voltage that can be made available to grid 1, and thereby acts as a limiter of the maximum intensity. The wiper of the brightness potentiometer is connected to pin E of the W682/W684 circuit board. In VR14 versions where the W682 Intensity Control (Figure 3-3) is used, pin E connects by way of R9 to grid 1 of the CRT.

The W684 Intensity Control is used in the VR14L and VR17L. In the W684 (Figure 3-4 and drawing D-CS-W684-0-1), the voltage at pin E is "modulated" by the three intensity signals [Intensity (2:0)], before it is sent to grid 1. (Operation of W682/W684 circuitry is explained in Paragraph 3.5.) The bias voltage applied to grid 1 of the CRT may vary from -80 Vdc to 0 V, the upper limit being determined by the setting of R38 on G836.

Intensity on the screen is generated by cathode pulses from the W682/W684 card. When not intensifying, the cathode is held at +62 V. The +62 V is derived from the +80 Vdc at the W682/W684. When the beam is to be turned on, the +62 V on the cathode is grounded, or made 0 V. However, this alone does not determine brightness, since intensity is related to grid-to-cathode voltage. Thus, the cathode is constantly going between +62 V and 0 V but, depending on where the grid voltage (brightness potentiometer) is set, the beam may never be on, dim, or very bright.

Grid 2 of the CRT is operated at approximately +400 Vdc. The 400 V is generated from the 150 Vac tap of the power transformer by a voltage doubler on the G836 board. The ac passes through C14 and is prevented from going negative by D9. This causes the entire peak-to-peak voltage to become positive. D10 rectifies this voltage and C15 filters it; the resultant output is +400 Vdc. The 400 Vdc goes directly to grid 2. If grid 2 is not substantially positively biased, the CRT beam can never be turned on, regardless of how much grid-to-cathode drive occurs. The 400 Vdc also goes to one side of the focus potentiometer R35 on the G836 board. The other side of the potentiometer goes to -80 Vdc. The wiper goes to the focus electrode on the CRT. Because of CRT manufacturing tolerances, proper focus may occur from unit to unit anywhere between -80 Vdc and +400 Vdc.

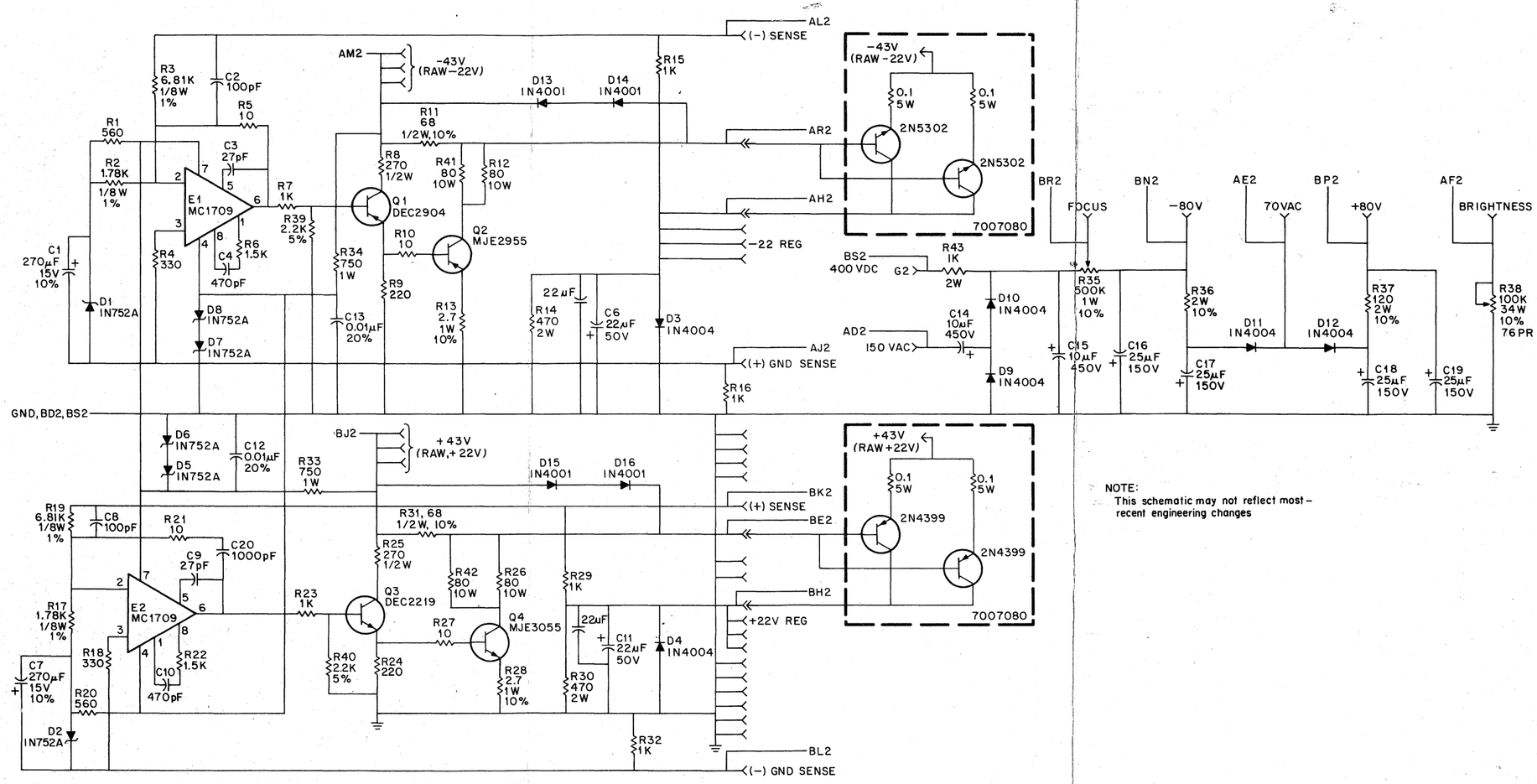
The anode is supplied 10.5 kV from the high voltage supply.

3.4 HIGH VOLTAGE POWER SUPPLY

The high voltage supply is a self-contained high voltage source that requires only line voltage input. The input is actually the split primary of its own internal step-up transformer. For 115 V operation, the primary windings are operated in parallel; for 230 V operation, they are operated in series. The step-up transformer delivers high voltage ac to a voltage doubler and filter. The ultimate dc voltage is 10.5 kV and unregulated. Thus, the high voltage is slaved to the line voltage, and varies linearity with it.

Because the electron beam is accelerated by the high voltage, the ability to deflect the beam will change as the high voltage changes. If a constant deflection current flows through the yoke, the amount of deflection is reduced if the anode high voltage is increased (smaller displayed picture); the deflection grows if the anode high voltage decreases (larger displayed picture). The actual deflection factor change is proportional to the square root of the ratio of the old anode voltage to the new anode voltage, i.e., deflection factor = $\sqrt{V_1/V_2}$. For example, if the high voltage is halved, the deflection would grow 1.414 ($\sqrt{2/1}$). In terms of line voltage, the deflection factor is approximately 0.4 of the change, i.e., a 5 percent line change causes a 2 percent deflection change.

The VR14/VR17 incorporates circuitry which protects the unit from possible damage due to arcing. Arcing is due to transient conditions within the CRT, which cause a spark to jump between the anode and other CRT elements. The protection circuitry consists of two voltage transient suppressors (DEC part no. 11 11562), R30 and D13 on W684, R43 on G836, R9 on W682, and a 1K resistor mounted on the CRT socket. The resistors act as current limiters; diode D13 prevents grid 1 from becoming more positive than 0 V; the voltage transient suppressors, mounted on the CRT socket, prevent grid 2 and the focus electrode from exceeding +600 V.



NOTE:
This schematic may not reflect most-recent engineering changes

CP-0763

Figure 3-2 G836 Circuit Board,
Part of the 7007165 Power Regulator Assembly

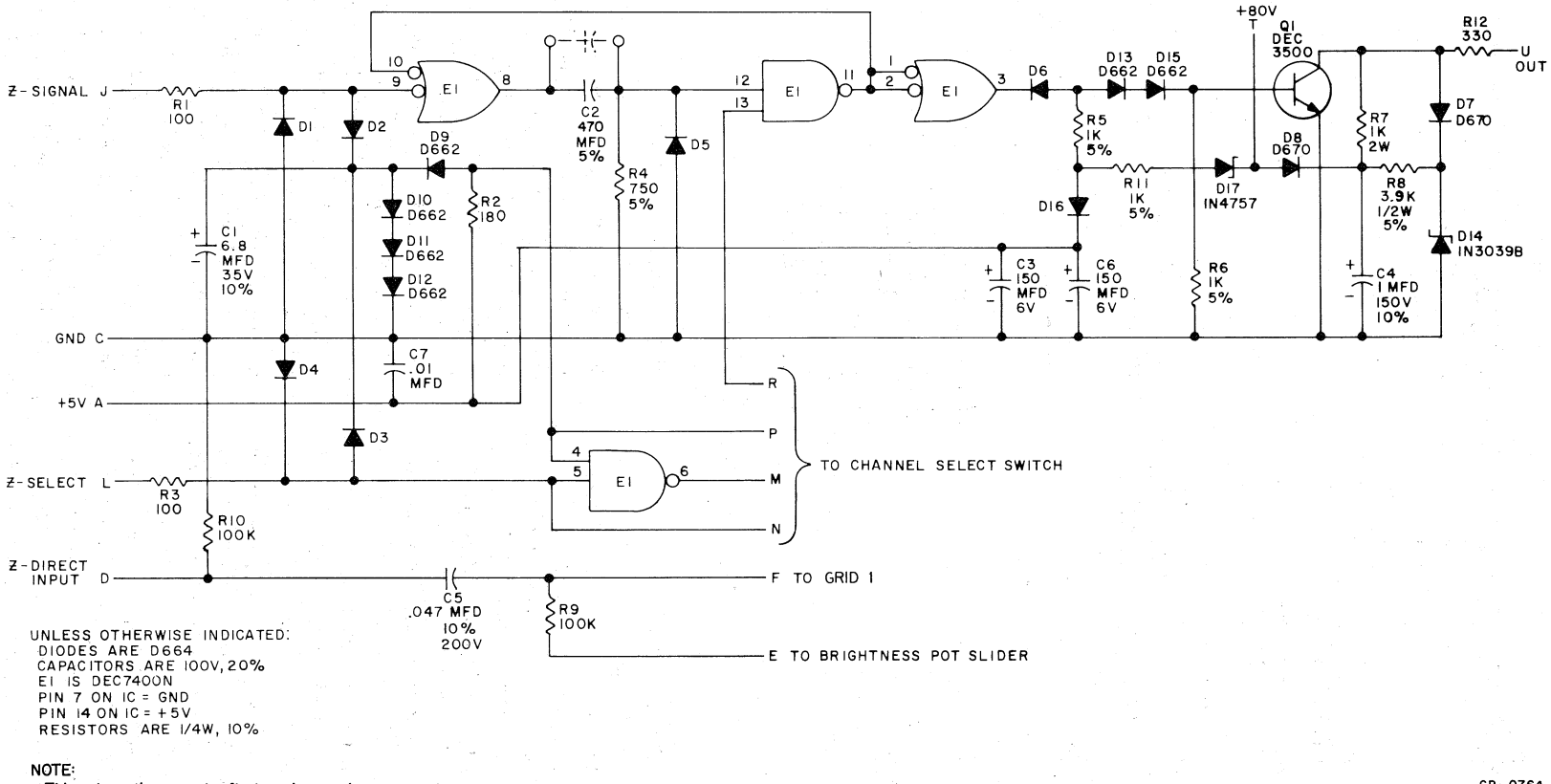


Figure 3-3 Intensity Amplifier W682, Circuit Schematic

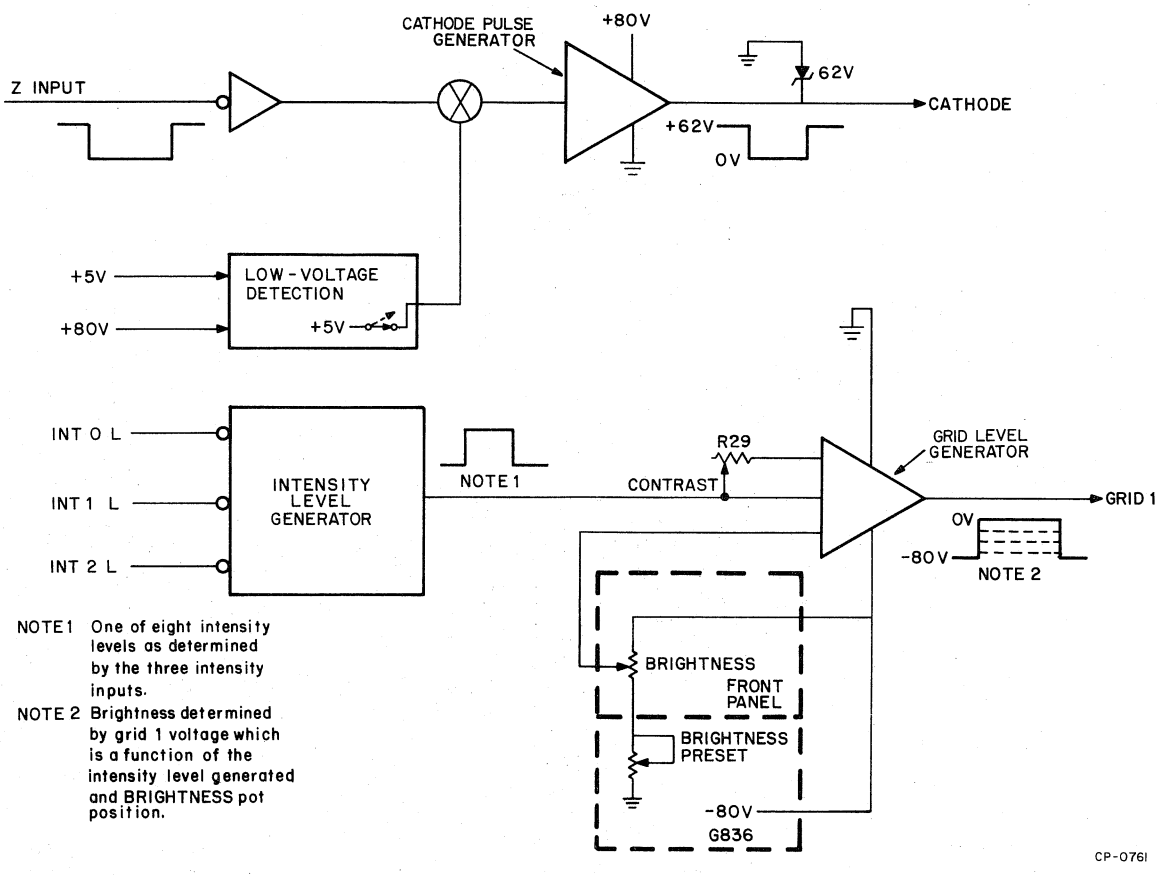


Figure 3-4 W684 Intensity Control

3.5 W682 AND W684 INTENSITY CIRCUITS

In the VR14 without the light pen option the intensification of points on the screen is controlled by the W682 circuit board. The intensity signal is routed to pin J. This signal is a transition from a high to a low. While the Z-signal is at a high (above +2.4 V), the output from gate A (pins 8, 9, 10) is low. When the Z-input is low momentarily, the output of A goes high. This positive-going transition is ac coupled through C2 and becomes a positive spike that exponentially decays to 0. The time constant of this decay is determined by C2 and R4. This positive-going spike is the input to gate B (pins 11, 12, and 13). Also, as input to B, is the channel select information which comes from pin R. This information either enables gate B to respond to the intensification spike or not. Assuming B is enabled from pin R, the positive spike causes the output of B to go to a low. This low remains as long as the input spike to B is above its 1 or high threshold level. As soon as the spike decays below the threshold, B's output immediately reverts to the high state. B's output is fed back to A's input (pin 10) to allow A's output to latch high, thus not requiring A's input (pin 9) to remain low, but rather be a momentary drop from a high. Of course, when the spike decays at B's input, the latching input is removed from A (pin 9) thus enabling A to respond to the next negative-going transition on the Z-intensify input. D5 clamps the input from going negative during the negative-going transition that occurs when A resets. Gate C (pins 1, 2, and 3) simply inverts the intensify pulse to drive the output pulse amplifier Q1. Gate C normally is low until a pulse comes along. This low "grounds" out the base drive for Q1; therefore, it will be off. D13 and D15 guarantee that Q1 will be off, even though there is a residual voltage drop across D6 and the output of gate C. Q1's collector is tied through R7 and D8 to +80 Vdc. With Q1 off, the collector tries to ride up to +80 Vdc, but D7 begins to conduct at +62 V clamping the collector at +62 V. The +62 V is generated by dropping the +80 V across R8 and Zener diode D14. Q1's collector is tied through R12 to the CRT cathode. Therefore, in the absence of an intensify input, the cathode resides at +62 V. This, along with the negative bias on the grid, keeps the CRT beam shut off. When an intensify signal occurs, gate C's output goes high, allowing Q1 to receive base current from the +80 Vdc via D17, R11, R5, D13, and D15. This base drive turns on Q1, causing its collector (and the cathode of the CRT) to go from +62 V to 0 V. This turns

the CRT beam on. The duration of this intensify pulse is determined by the time constant of C2, R4 and is normally 300 ns. D16 prevents the voltage supplied to R5 from exceeding 5 V; this is necessary to prevent damage to gate C.

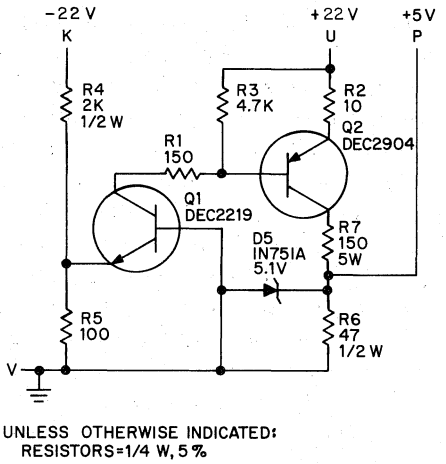
When power is removed from the VR14, the CRT must be prevented from blooming and possibly burning the phosphor. Blooming can occur because the necessary voltages (±80 Vdc) that keep the CRT shut off, drain to 0 V faster than the high voltage supply. When the grid-to-cathode voltage becomes more positive than cutoff, the CRT turns on very hard. D8 and C14 prevent this from happening. When power is turned off, the +80 V goes to 0 V but, in so doing, C4 hangs on to its voltage and thus back biases D8 which does not allow C4 to discharge. C4 momentarily acts like Q1's power source, allowing the collector (and CRT cathode) to hold at +62 V which is the safe or off condition. Eventually C4 discharges; however, by that time the high voltage has also discharged, rendering the CRT safe.

Five volts are supplied at pin A for E1 and also as a clamp for D16. A +3 V logical 1 level is generated across D9, 10, 11, and 12 through R2. D2 and D3 protect gate A and gate D inputs from exceeding +5 V. D1 and D4 prevent the same inputs from becoming negative.

The two remaining inputs on the W682 are the Z-select and Z-direct. The Z-select is a bit that allows the intensity pulse to be multiplexed or time enabled. As mentioned before, whether or not the intensity pulse is allowed to pass to the output through gate B depends on whether or not a high input is available at pin 13 of gate B. This high is continuously available, independently of the Z-select input, when the channel select switch is in the 1 & 2 position. When the channel select switch is in the 1 position, intensification occurs only when a high is presented at Z-select and an intensify input is presented. When the channel select switch is in the 2 position, gate B is enabled only when the Z-select input is a low.

The Z-direct is an input directly to the grid through C5. Video or other time varying brightness information may be coupled to the grid at pin D.

In the event of a failure of either the ±22 V supplies, deflection ceases and a bright spot could occur on the CRT, causing a burn. To prevent this, G838 (Figure 3-5) contains a circuit that supplies +5 V to the W682. If either the +22 V or -22 V goes to 0 (in the case of a short circuit or blown secondary fuse), the circuit supplying the +5 V shuts down. Because the G838 has a low value resistor across the 5 V (47 Ω), the 5 V line (pin A) on the W682 is grounded. This causes the base drive to Q1 to be shunted to ground through D16 and renders Q1 off; this shuts off the CRT.



G840

Figure 3-5 ~~G838~~ Circuit Diagram

In the VR14L and VR17L, the intensification of points on the screen is controlled by the W684 module. The Z-input intensity signal enters the W684 at pin J (drawing D-CS-W684-0-1). Before the Z-input is asserted, pin J is a TTL high. The output of E2 pin 3 is low, disabling the two AND gates, E2 pin 6 and E2 pin 11. This causes Q7 to be cut off and Q6 to conduct. Consequently, Q2 is cut off because its base is low at this time. With Q2 cut off, the cathode voltage at pin U will be positive, approximately +62 V, and no beam is generated. The cathode voltage is produced by the Zener action of D4 from +80 V input from the G836.

When the Z-input is asserted, E2 pin 3 is disabled and E2 pin 6 and E2 pin 11 are enabled. Now the situation is reversed: Q6 is cut off and Q7 conducts. With Q7 conducting, +5 REG is coupled to the base of Q2 causing it to conduct. The cathode voltage goes from +62 to 0 V and a beam can be produced, provided one other condition is satisfied – grid 1 must be sufficiently positive before the grid-to-cathode voltage results in a beam strong enough to cause screen fluorescence.

Grid voltage can be varied from approximately -80 to almost 0 V; brightness increases as the voltage becomes more positive. Q3 controls the grid voltage with the screen brightest when Q3 is cut off. When Q3 conduction increases, the image becomes dimmer. Conduction of Q3 is determined, along with the contrast control setting, by the voltages present at the base of Q4 and the emitter of Q5.

The voltage at the base of Q4 is established by the front panel brightness control. Turning this control clockwise causes Q4 to conduct less; the emitter voltage becomes more positive. As a result, the base of Q3 becomes more positive. Coincident with this, the emitter voltage of Q5 is determined by the state of the three intensity level signals [Intensity (2:0) L]. These signals forward bias three diodes (D8, D9, and D10) that control the conduction of +5 REG through a voltage divider consisting of R21, R22, and R23. Table 3-1 shows the relationship between the three intensity levels and the resultant brightness level. As the number of levels asserted increases from 0 through 3, the brightness level increases from 0 through 7. The higher the brightness level, the more positive the emitter of Q5 and therefore the harder Q5 conducts. As Q5 conducts harder, more voltage is dropped over the Q4, R18, R19, and R29 network, causing the base of Q3 to become more positive. This, in turn, decreases Q3 conduction and the emitter (grid 1) voltage approaches 0 V.

Figure 3-6 illustrates the relationship between the eight brightness levels, that are program controlled, and the brightness control, which can be changed by the operator. Reference A shows the relative brightness at a particular brightness control setting, for each of the brightness levels. As the control is turned clockwise, there is a linear increase in brightness at each level (reference B).

The contrast control, R19, is positioned between Q4 and Q5. As the control is turned clockwise, dropping more voltage, the brightness range between brightness level 0 and brightness level 7 is increased; i.e., the image contrast is increased. This is indicated in Figure 3-6 as the change from reference A to reference C; the original brightness spread (x) is increased (y). Actually, level 0 becomes dimmer and level 7 becomes brighter. Therefore, the brightness control must also be adjusted at the same time to compensate for the decreased lower intensity levels. Reference D shows the result of this final adjustment.

Note that grid 1 voltage is the consequence of the three intensity levels generating a brightness level (one of eight) that is then combined with the particular brightness control setting. At the same time, the contrast control setting determines the difference in brightness between the brightness levels.

Table 3-1
Brightness Control

Intensity Level			Brightness Level	Front Panel Brightness Control
2L	1L	0L		
H	H	H	0	
H	H	L	1	
H	L	H	2	
H	L	L	3	
L	H	H	4	
L	H	L	5	
L	L	H	6	
L	L	L	7	

In case of a decrease in the +5 or +80 V input to the W684, the cathode and grid circuits described above are disabled. If these circuits were not shut off when this low voltage condition occurred, the phosphor would be burned and the screen damaged. This is because X and Y deflection circuits are disabled by the same power failure and the electron beam would be continually directed to the same spot on the screen. If the +5 V input from the G840 at pin A drops to about +4 V, Q9 loses forward bias and ceases to conduct.

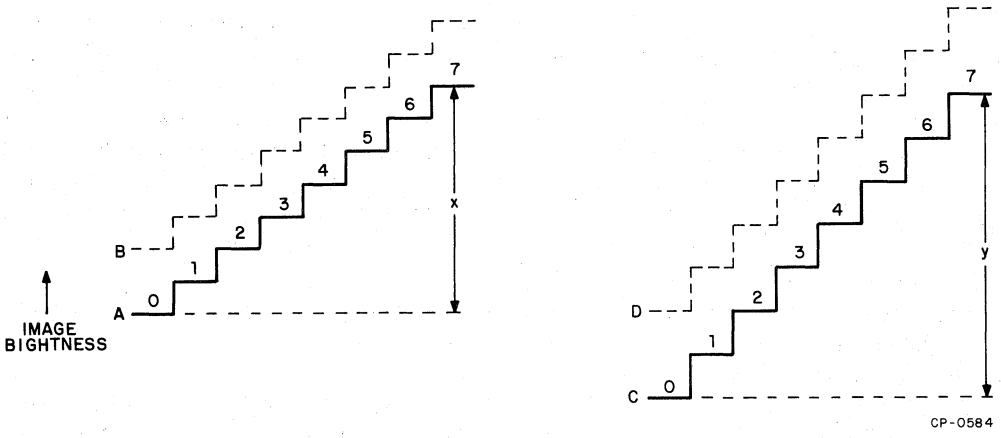


Figure 3-6 VR14L/VR17L Brightness and Contrast Control

Effectively, this opens the +5 V input to the emitter of Q7 (cathode circuit) and to the R21, R22, and R23 voltage divider (grid 1 circuit). The same result occurs if the +80 V input to the cathode circuit fails. In this instance, the base of Q9 becomes more positive; Q9 is cut off and the +5 V input opens.

When power is removed from the VR14L/VR17L, the CRT must be prevented from blooming and possibly burning the phosphor. Blooming can occur because the necessary voltages (±80 V), that keep the CRT shut off, drain to 0 V faster than the high voltage supply. When the grid-to-cathode voltage becomes more positive than cut-off, the CRT turns on very hard. D2 and C1 prevent this from happening. When power is turned off, the +80 V goes to 0 V but, in so doing, C1 hangs on to its voltage (+60 V) and thus back biases D2, which does not allow C1 to discharge. C1 momentarily acts like Q1's power source, allowing the emitter (and CRT cathode) to hold at +62 V, which is the safe or off condition. Eventually C1 discharges; however, by that time the high voltage has also discharged, rendering the CRT safe.

3.6 LIGHT PEN AMPLIFICATION

The input from the 375 Light Pen that results from detection of beam intensification is not usable in its analog form; it must first be converted to a TTL compatible signal. This is the prime function of the G840 Light Pen Amplifier module (drawing D-CS-G840-0-1 and Figure 3-7).

In relation to the G840, the light pen phototransistor acts as a variable resistor that presents a low-going signal at the input (J1, pin 3) to the module when screen intensification occurs within the light pen's angle of acceptance. This negative-going analog signal is inverted by Q1, and peaked by the circuit at the collector of Q1. The signal, now positive-going with a greatly decreased rise time (about 1 μs), is differentiated before being input to the LM 306 Comparator.

The LM 306 is a high-speed voltage comparator designed to produce a sharp-edged, TTL compatible output when the input attains a predetermined threshold voltage. In this application, the (+) input to the LM 306 (pin 2) is held at about 400 mV. When the differentiated input at the (-)

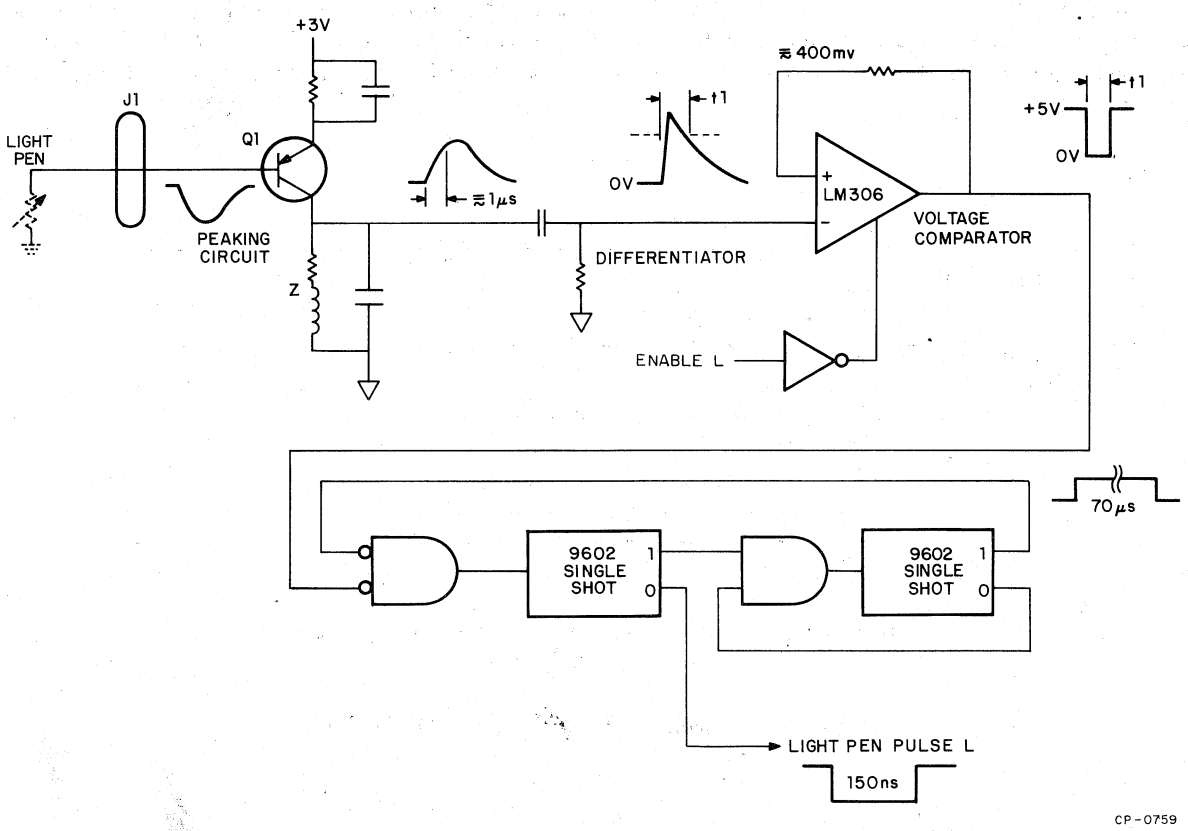


Figure 3-7 Light Pen Amplifier

input reaches this threshold, a negative-going output signal is produced at pin 7, provided an ENABLE signal is present at E3 pin 13. This qualifying signal ensures that all light pen hits (LIGHT PEN PULSE L) from the G840 are valid, inhibiting those hits that might be generated by spurious noise from the light pen. The LM 306 output occurs about 30 ns after the two input voltages compare (fall time is approximately 20 ns) and remains low as long as the (-) input stays above the 400 mV threshold. This assertion time is indicated in Figure 3-7 as t1. Positive feedback is provided from the output to the (+) input to assist the input signal comparison.

The negative-going output from the LM 306 triggers one stage of a 9602 Monostable Multivibrator, which, in this application, functions as a single-shot to produce a 150 ns output signal, LIGHT PEN PULSE L. Coincident with this signal from the 0 output, the 1 output from the first stage of the 9602 triggers the second stage, also configured as a single-shot. The 1 output of the second stage, high for 70 μs, inhibits a second light pen hit immediately following the first one.

Timing for this operation is shown in Figure 3-8. The comparator output assertion time is unimportant because only the negative-going transition is needed to initiate LIGHT PEN PULSE L.

In the event of a failure of either 22 V supply, deflection ceases and a bright spot occurs on the CRT, resulting in a burn. To prevent this, the circuit on the G840 module that produces +5 V for the W684 intensity module will be disabled if either the +22 V or -22 V goes to 0 (in the case of a short circuit or blown secondary fuse). Referring to drawing D-CS-G840-0-1, if +22 V fails, Q3 loses forward bias (at the emitter) and turns off, shutting down the +5 V. If the -22 V goes to 0, Q2 loses emitter voltage and the base of Q3 goes high. This causes Q3 to turn off and +5 V drops. This circuitry (aside from some component values) is identical to the fault protection circuitry on the G838 (Figure 3-5). Note that this failure detection circuit is in addition to the W684 low +5 V voltage protection circuit previously described (Paragraph 3.5).

3.6.1 375 Light Pen

The 375 Light Pen is simply constructed. A phototransistor is recess-mounted (drawings C-UA-375-0-0 and D-CS-5410268-0-0) in a polished cylinder approximately 0.45 X 5.0 inches. The output signal connection is via a cable that plugs into the VR14L/VR17L front panel. When an intensified beam strikes the CRT phosphor where the light pen is being aimed, the phototransistor (Q1) conducts and negative-going alternation is output to the G840 Light Pen Amplifier module (Figure 3-7). In the G840, the light pen output is shaped to become the TTL compatible signal LIGHT PEN PULSE L.

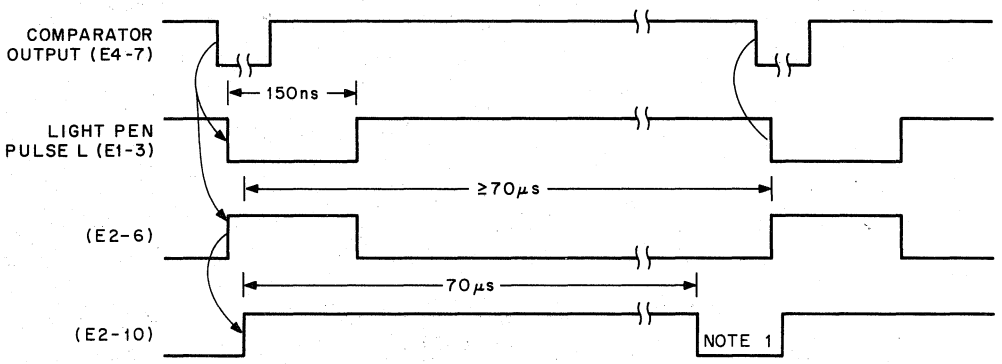


Figure 3-8 Light Pen Pulse Timing, G840 Module

CHAPTER 4
MAINTENANCE

This chapter deals with the prevention, diagnosis, and repair of fault conditions. Successful troubleshooting of the VR14/VR17 can be performed using a volt-ohm-milliampere meter; however, an oscilloscope facilitates and expedites isolation and repair of faults.

4.1 PREVENTIVE MAINTENANCE

VR14/VR17 preventive maintenance consists of ensuring that the equipment is getting and maintaining proper air flow for cooling and a periodic, cursory inspection for abnormal hardware conditions. Because of the power dissipation on the deflection and regulator heat sinks, good air flow must be maintained. A periodic check is required to see that fans are operating properly and are not obstructed by dirt, dust accumulation, or inadvertently blocked by external equipment or surfaces.

Prolonged off-screen deflection of the CRT beam can damage the VR14/VR17. Ensure that the X and Y driving signals into the VR14/VR17 never drive the CRT beam off screen because of intermittent incorrect signals.

4.2 TROUBLESHOOTING

VR14/VR17 voltage checks (Table 4-1) and most tests can be done with a volt-ohm-milliampere meter; however, an oscilloscope will be needed if waveform analysis is required.

NOTE

When making voltage measurements on a malfunction VR14/VR17, set the voltmeter (or oscilloscope) to the proper range, connect the leads to the test points, then turn the power on and off very quickly so that the anticipated reading may be taken. Power is only on for a very brief moment. In this way, fault conditions may be discovered without causing further damage. Never leave power on to a malfunctioning or repaired VR14/VR17 until all necessary checkpoints are measured and proved nominal.

The circuit card connector block, as viewed from the wiring side, is labeled A01 and A04 left to right on the top section, and B01 to B04 on the bottom section. Figure 4-1 shows pin and connector locations for P1, P2, P3 and P4.

4.2.1 No Picture

Probably the most common failure mode with this type of equipment is "no picture." Unfortunately, this condition can be caused by almost any malfunction such as a loss of input intensity pulse, incorrect input deflection signals driving the beam off the screen, a power supply fuse, or fan failure (thermal cutout). The following sequence of events leads to the isolation of the fault(s):

1. Check fuses. If they are in good condition, continue. If not, replace any that are blown and then continue. (If a blown fuse is replaced, leave power on only long enough to complete each check in this procedure.)

2. Remove all input signals at the rear of the unit and all modules except W682/W684 and G836.

3. With a voltmeter (or oscilloscope), measure the +22 Vdc (20 Vdc to 22 Vdc is acceptable). This can be measured between A01-U (red wire) and A02-V which is ground. Momentarily apply and shut down power. If the +22 V is above +22 V, the regulator has a fault; refer to Appendix A. If 0 V or below +20 Vdc occurs, the +22 V is overloaded; continue to the next step.

4. Set up to measure -22 V. This can be found between A01-K (blue wire) and A02-V which is ground. Momentarily apply and shut down power. If the -22 V is more negative than -22 Vdc, the -22 V regulator has a fault; refer to Appendix A. If 20 V or more positive, the -22 V is overloaded; continue to next step.

Table 4-1
VR14/VR17 Voltage Check Points

Circuit Block Pin	Voltage	Signal/Control
A02A	*2.2V nominal	X Current Sample
A03A	*2.2V nominal	Y Current Sample
A02E, B	*	X Input Signal
A03E, B	*	Y Input Signal
A01U	+22 Vdc (Red)	+ Regulated dc
A01K	-22 Vdc (Blue)	- Regulated dc
A01P	+5 Vdc	For W682/W684
Deflection Heat Sink Pin X-Axis / Y-Axis	**Voltage**	**Component**
P5 - 2 / P5 - 14	+21 Vdc	PNP Base (2N4399)
P5 - 1 / P5 - 15	+22 Vdc	PNP Emitter (2N4399)
P5 - 3 / P5 - 13	*< 1V	All Collectors
P5 - 4 / P5 - 12	-21 Vdc	NPN Base (2N5302)
P5 - 5 / P5 - 11	-22 Vdc	NPN Emitter (2N5302)
Regulator Heat Sink Pin	**Voltage**	**Component**
P3 - 1	+43 Vdc Orange	Emitters of 2N4399
P3 - 2	+42 Vdc Gray/Yellow	Bases of 2N4399
P3 - 3	+22 Vdc Red	Collectors of 2N4399
P3 - 12	-43 Vdc Green	Emitters of 2N5302
P3 - 11	-42 Vdc Gray/Blue	Bases of 2N5302
P3 - 10	-22 Vdc Blue	Collectors of 2N5302
7007165 (G836) Regulator Circuit Connectors P1, P2, P4	**Voltage**	**Signal/Control**
P1 - 1	+43 Vdc ORANGE	Raw + dc
P1 - 3, 6	Ground BLK	
P1 - 4	-43 Vdc GREEN	Raw - dc
P2 - 1	3.5 Vrms YELLOW	1/2 Filament
P2 - 2, 4, 7, 9	Ground BLK	
P2 - 3	3.5 Vrms YELLOW	1/2 Filament
P2 - 5	70 Vrms (200 P-P) BLK/WHITE	±80V tap
P2 - 6	150 Vrms (400 P-P) BLK/YELLOW	+400V tap
P4 - 1	+22 Vdc Red	+ Regulated
P4 - 2, 14	Ground Black	
P4 - 3	+22 Vdc Red	Hot + Sense
P4 - 4	0 Vdc Black	Cold ± Sense
P4 - 5	-80 to +400 Vdc Gray/Red	Focus
P4 - 6	+400 Vdc Orange	Grid 2

*Indicates voltage depends upon input signal.

Table 4-1 (Cont)
VR14/VR17 Voltage Check Points

7007165 (G836) Regulator Circuit Connectors P1, P2, P4	Voltage	Signal/Control
P4 - 7	3.5 Vrms Brown	Filament
P4 - 8	3.5 Vrms Brown	Filament
P4 - 9	-80 Vdc Gray/Green	To Brightness Potentiometer
P4 - 10	0 to -40 Vdc Gray/Violet	Brightness Preset
P4 - 11	+80 Vdc Gray/Orange	For W682/W684
P4 - 12	-22 Vdc Blue	Hot - Sense
P4 - 13	0 Vdc Black	Cold - Sense
P4 - 15	-22 Vdc Blue	- Regulated

Note: All voltages measured with respect to ground (chassis or A02V).

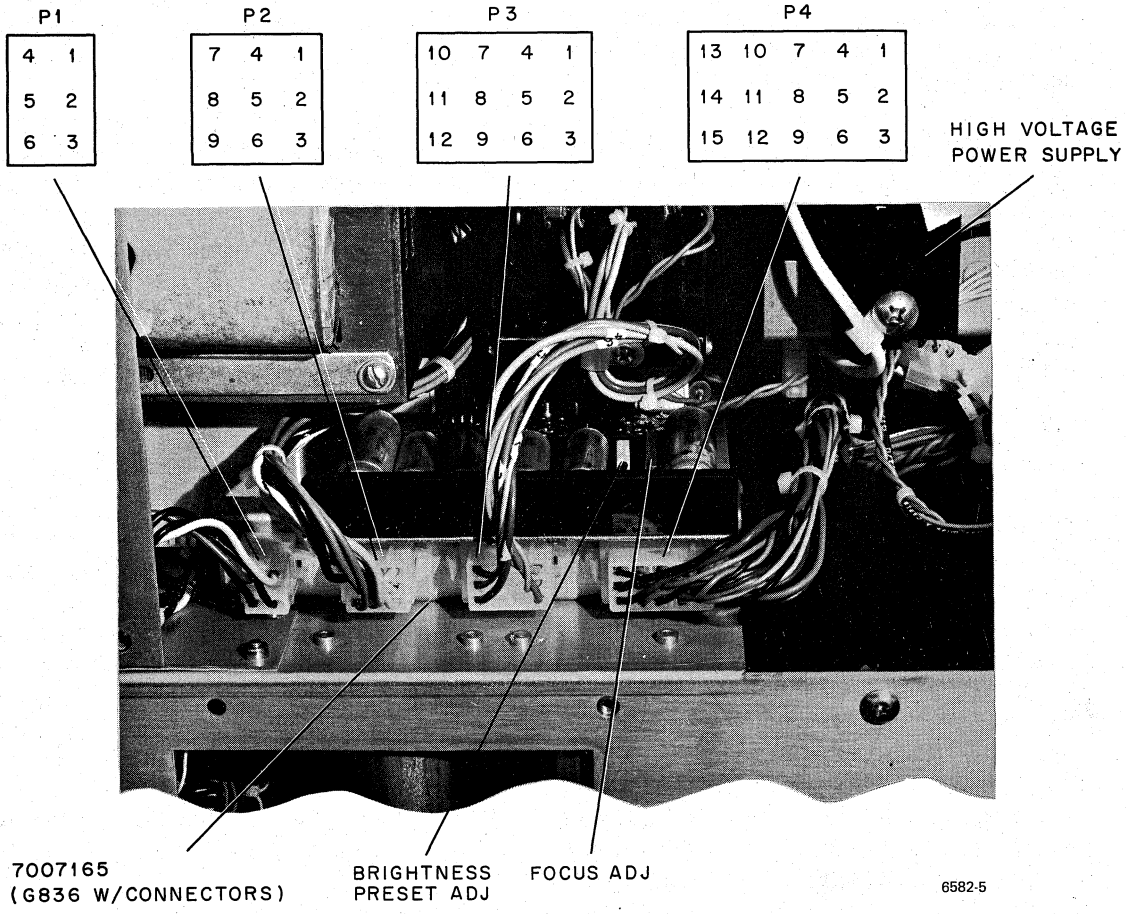


Figure 4-1 VR14/VR17 Interior View

5. With an oscilloscope or meter, measure ±2.2 V maximum at A02-A with respect to ground (A02-V). This point (A02-A) is the X-axis deflection coil current sample. Because coil current flows through a 0.5 Ω resistor, voltage measured at A02-A multiplied by two equals the current flowing. With the A225 circuit cards removed, no coil current should flow. Momentarily turn on power to the VR14/VR17. If A02-A has any voltage plus or minus (refer to Appendix B), a deflection power transistor probably is shorted.

6. Measure the same as in step 5 for the Y-axis deflection coil current at A03-A with respect to ground (A02-V). Momentarily turn VR14/VR17 power on and off. No voltage should be read; this indicates no Y-deflection coil current is flowing. If any voltage is observed, refer to Appendix B, since a Y-axis deflection transistor is probably shorted.

7. Replace the G838/G840 circuit into A01 and the A225 circuit into A02. (Still leave the Y-axis, A03 board out.) Measure less than ±2.2 V at pin A02-A with respect to ground (A02-V). Momentarily apply power. If the voltage is within safe limits (within ±2.2 V), leave power on and adjust the position potentiometer on the A225 circuit. Doing this should change the voltage reading on A02-A, providing the A225 indeed is controlling the coil current. Return the position potentiometer to its original position. If the voltage at A02-A is beyond ±2.2 V, shut down immediately. Because the position potentiometer on the A225 can drive more current than the ±2.2 V limit signifies (4.4 A), it is possible that it (the position potentiometer) has been adjusted to one extreme or the other. To prove whether this is the case or if the A225 circuit board is faulty, turn the position potentiometer as follows: clockwise if the voltage at A02-A was very negative; counterclockwise if the voltage at A02-A was very positive. If no change is noted at A02-A after adjusting the position potentiometer, the A225 board is faulty and should be replaced or repaired (refer to Appendix C).

8. Repeat the same tests as in step 7 for the Y-axis deflection circuit A225 plugged into A03. Monitor A03-A. Refer to Appendix C for A225 repair.

9. If the fault has not been isolated, the intensity circuit W682/W684, the electrode voltages, and the high voltage supply are suspect. The output of the W682/W684 drives the cathode. At rest, it should be +62 V and, when triggered, go to approximately 0 V.

   To check the W682, apply a proper Z-input (+3 V to 0 V transition) at J17 pin 4 and check to see that the signal reaches A04-J. If so, check A04-R with the channel select in the 1 & 2 position to see that a high is present there. If so, see that +5 V is being supplied to A04-A. If A04-A is less than +4 V replace or repair the G838 module as this is where the +5 V is developed. If the three preceding measurements are good and the W682 output (measured at A04-U) is not going from +60 V to 0 V for at least 300 ns, repair or replace the W682 module.

   To check the W684, apply 0 V (ground) to the Z-input at J17 pin 4 and check to see that it reaches A04-J. If so, see that +5 V is being supplied to A04-A. If A04-A is less than +4 V, replace or repair the G840 module, as this is where the +5 V is developed. If the two preceding measurements are good, and the W684 output (measured at A04-U) is not at approximately 0 V, repair or replace the W684 module.

10. Measure 6.3 Vac between P4-7 and P4-8 and observe the glowing filament on the CRT. No 6.3 Vac can be traced back to the power transformer by way of P2 pins 1 and 2.

11. Measure the grid 1 voltage at A04-F. It should vary from -80 Vdc to between -30 V and 0 V when the front panel brightness control is varied. The -80 Vdc comes from the G836 board. Trace back to the G836.

12. Measure grid 2 at P4-6. It should be at least +300 V. Trace back to the G836.

13. The last item operating improperly for "no picture" is the high voltage supply itself. Generally, all other measurements should be made before considering the high voltage, since the majority of "no picture" conditions will not be caused by the high voltage supply. Measuring the high voltage directly is extremely

dangerous and not recommended. Instead, a quick method is to take a long screwdriver and ground the blade with two separate clip leads for safety. Turn the VR14/VR17 on for 5 seconds and then SHUT IT OFF. After it is off, ground out the anode cap on the CRT with the GROUNDED screwdriver. If done within 5 to 10 seconds after power is turned off, an arc should occur to the screwdriver indicating that the CRT was charged with high voltage. If no arc occurs, replace the high voltage supply.

4.2.2 Faulty Picture

a. No Focus – Check the range of the focus potentiometer on the G838 by monitoring the focus voltage at P4-5 while adjusting the focus potentiometer through its range. Minimum range is +350 Vdc to -60 Vdc. See G836 for repair.

b. Half or Quarter of the Picture Missing – Generally, this condition indicates that one of the two deflection transistors is not working; thus, only half deflection is available. The transistor in question can be identified by observing which side of the screen is not working. The left and bottom portions of the screen are controlled by the PNP (2N4399) power transistors on the deflection heat sink. These are the lower two transistors; the left side of the screen is controlled by the left lower power transistor (if the deflection heat sink is viewed from the front of the VR14/VR17), the lower part of the screen is controlled by the right lower power transistor. Of course, the upper and right are controlled by the NPN (2N5302), the right side of the heat sink controlling the upper screen, the left side of the heat sink controlling the right screen.

c. The remaining possible faulty picture patterns, such as picture swim (60 Hz), oscillations, distortion, etc., will be restricted generally to improper input signals (especially grounding techniques) or faults on the A225 circuit board. If input signals are not suspect, a faulty A225 may be isolated by swapping X and Y A225s with one another to see if the problem changes axis.

d. If a weak picture that is deflected off the screen on all sides is encountered, with excessive jitter and ripple, the high voltage supply should be replaced.

4.3 ASSEMBLY REPLACEMENT INSTRUCTIONS

Other than the G838/G840, A225s, and W682/W684 circuit modules, most repair and replacement will involve the G836 regulator subassembly; the regulator heat sink assembly; and the deflection heat sink assembly; and, in rare cases, the high voltage assembly, yoke, and CRT. It cannot be stressed too strongly that the VR14/VR17 line cord be removed from the line before doing any maintenance. Turning power off or removing fuses does not render the unit safe from shock hazards, since the power switch and fuse interrupt only one side of the ac input line voltage, the other side is permanently connected as long as the line cord is plugged in. Do not take chances, UNPLUG the line cord.

NOTE

Photographs in this section are of a VR14 prototype, but generally apply to all VR14 and VR17 configurations.

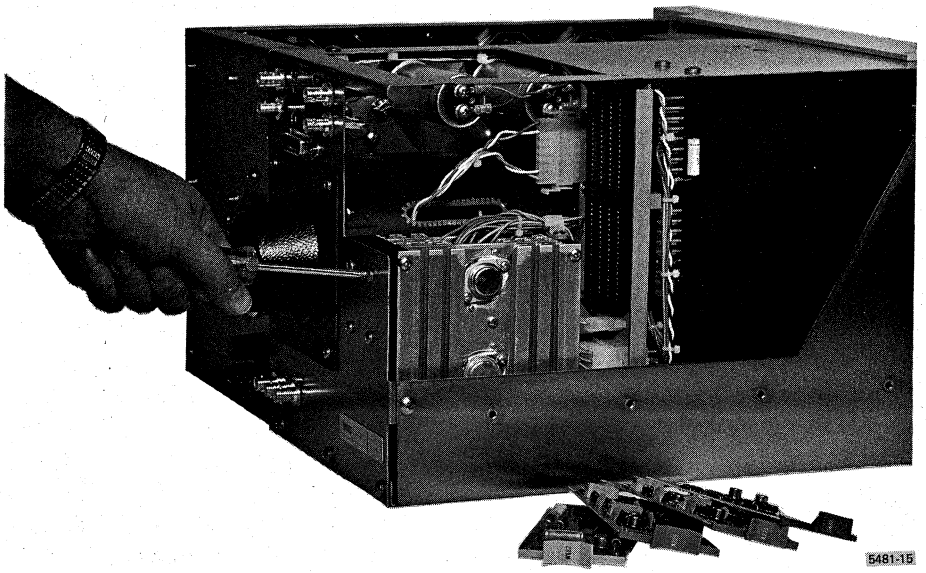
4.3.1 Deflection Heat Sink Removal

To remove the deflection heat sink (Figure 4-2) proceed as follows:

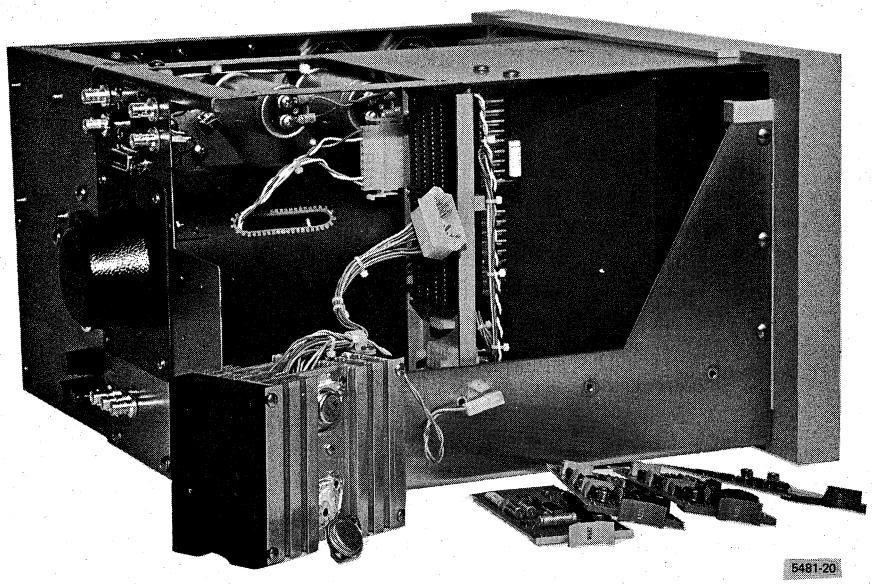
1. Remove the line cord and all circuit modules above the deflection heat sink assembly (G838/G840, A225s, W682/W684).

2. Remove the four 6-32 screws that hold the heat sink assembly to the rear chassis plate.

3. Lift the assembly out to make room for removing the assembly cable connector. The 15-pin connector is removed by squeezing the retaining tabs on each side of the connector so that when the connector is pulled, the tabs pass through the square holes that they were butted against. Do not pull the connector by its wires, only by its plastic body.



a. Remove circuit boards and the four 6-32 screws holding the deflection sink to the rear panel.



b. Remove heat sink assembly (and its connectors if necessary) and remove faulty power transistor.

Later models do not have the four BNC connectors at the top rear of the unit.

Figure 4-2 Deflection Heat Sink Removal

4. To remove a faulty transistor, unscrew the two 6-32 screws that hold the transistor down. Then pull the transistor straight out from the socket. Apply an even coat (approximately 1/32 inch thick) of thermal compound to all mating surfaces of the new transistor. Replace the new transistor, making sure that the base and emitter pins are oriented properly; otherwise, the transistor case will not align with the two screw holes. Also, ensure that the insulating washer is between the transistor and the heat sink and each mounting screw has a star washer.

4.3.2 7007165 Power Regulator Assembly Removal

The 7007165 Power Regulator Assembly comprises a G836 regulator printed circuit board with a mounting frame for J1, J2, J3, and J4. To remove the 7007165 Power Regulator Assembly proceed as follows:

1. Remove the line cord and all circuit modules (G838/G840, A225, W682/W684).

2. Remove all four cable connectors (Figure 4-3) coming into the connector bracket on the 7007165 by squeezing the two locking tabs on the sides of each connector, while pulling the connector straight up, allowing the locking tabs to pass through the square holes they were butted against. Do not pull the connector by its wires; only by its plastic body.

3. Remove the two mounting screws for the 7007165 from the opposite side of the 7007165 chassis wall.

4. The 7007165 is now free and may be pulled straight out.

WARNING

The 7007165 has +80 Vdc, -80 Vdc, and +400 Vdc available on it. These voltages do not disappear immediately when power is shut off. Use extreme caution when troubleshooting the board.

5. For troubleshooting, the 7007165 may be operated outside its normal mounting position by laying the board flat and reconnecting the four cable connectors. Ensure that the etch side of the module does not touch the chassis, causing short circuits, by insulating the board with a book or piece of cardboard as shown in Figure 4-4b.

NOTE

When placing the 7007165 back into the unit, ensure that the bottom of the circuit board rests in the slotted groove insulator block provided on the bottom chassis.

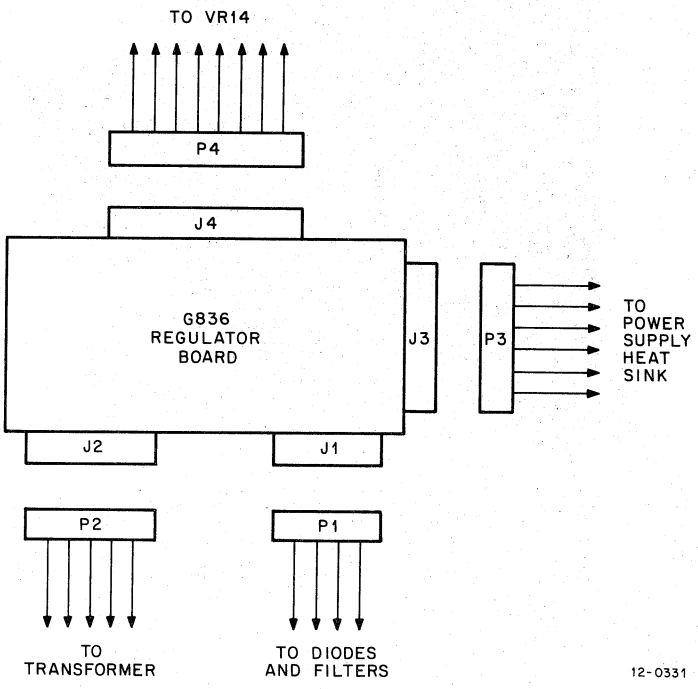
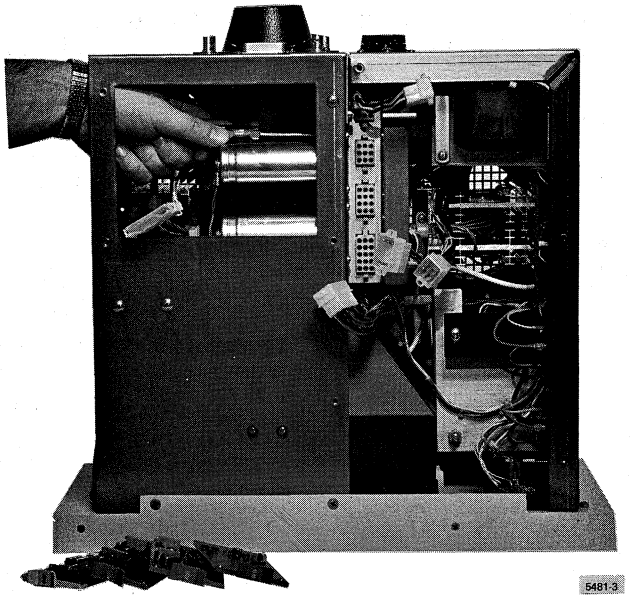
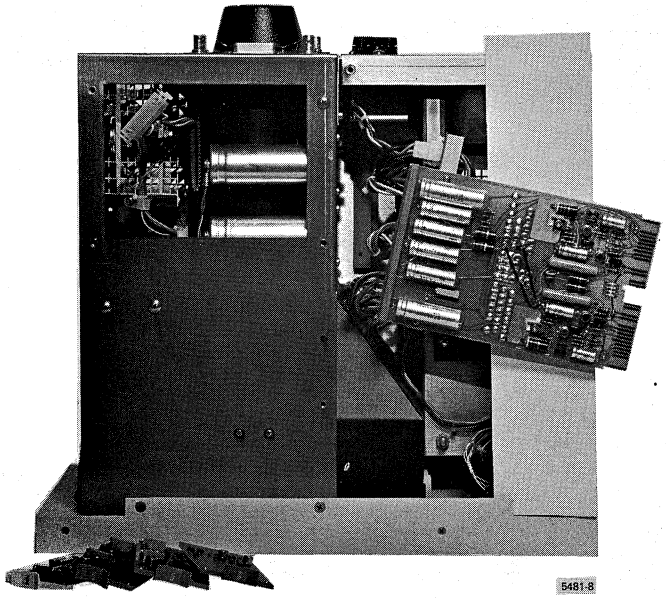


Figure 4-3 7007165 Power Regulator Assembly



a. Remove power cord and all connectors to the 7007165. Unscrew mounting screws from the opposite side of the vertical chassis wall.



b. Reconnect connectors and place a cardboard under the 7007165 to prevent shorting out the circuit against the chassis when troubleshooting the board outside the unit.

Figure 4-4 7007165 Removal

4.3.3 Regulator Heat Sink Removal

To remove the regulator heat sink (Figure 4-5) proceed as follows:

1. Remove the 7007165. See Paragraph 4.3.2 for instructions.

2. Remove the four heat sink mounting screws on the right chassis wall (when viewed from front).

3. Lift the heat sink assembly straight out.

4. To remove a faulty transistor(s), unscrew the two 6-32 screws holding the transistor(s) down; then pull the transistor(s) straight out from the socket. Apply an even coat (approximately 1/32 inch thick) of thermal compound to all mating surfaces of the new transistor. Replace the new transistor, ensuring that the base and emitter pins are oriented properly; otherwise, the transistor case will not align with the two screw holes. Also, ensure that the insulating washer is between the transistor and the heat sink and that each mounting screw has a star washer.

4.3.4 Yoke and CRT Removal

To remove the yoke proceed as follows:

1. Remove the line cord and all the circuit modules (G838/G840, A225, W682/W684) along with the plastic CRT socket cover.

2. Carefully remove the yoke cable connector from its mating connector on the inner side of the circuit board mounting bracket.

3. Using a screwdriver, loosen the screw that holds the yoke neck clamp by inserting the nut driver through the access slot provided in the CRT shield. Loosen sufficiently for the yoke clamp to be slipped off the yoke.

4. Carefully remove the CRT socket connector and slide the yoke clamp off the CRT neck.

5. Slip the yoke connector through the access slot in the CRT shield and pass it, along with the entire yoke assembly, off the CRT neck and out the rear. Sometimes the yoke gets stuck at the socket end of the CRT because the yoke plastic mounting piece hugs the CRT neck tightly and must be spread to pass over the CRT socket.

To remove the CRT proceed as follows:

1. Remove the yoke first, as described above, and double check that the line cord is removed.

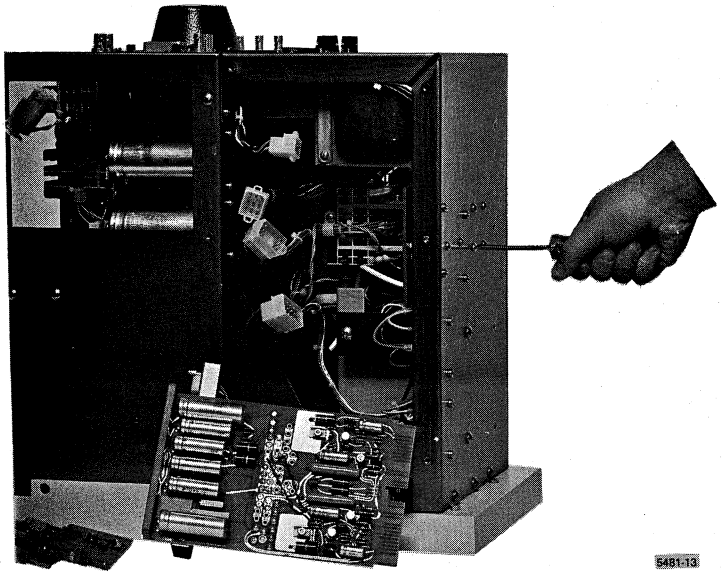
2. With a long-bladed screwdriver that is grounded to the chassis (a clip lead between the screwdriver blade and chassis plus a second clip lead for safety is adequate), slide the blade under the rubber cup on the high voltage connection at the CRT and touch the anode connection to discharge any remaining high voltage. At the same time, remove the high voltage connection. The connection is made by two stiff wires that each have a bend or hook on the end. The connection at the CRT is made by squeezing these two wires together so they can fit in the CRT metallic hole. Then those two wires are let go so they can expand and grab the inner lip of the CRT with the hooked ends. The connection is removed by squeezing the "hook wires" together and, at the same time, pulling them out so that the wires can clear the anode hole.

3. Remove the CRT plastic mask by removing the top and bottom screws from the front bezel casting.

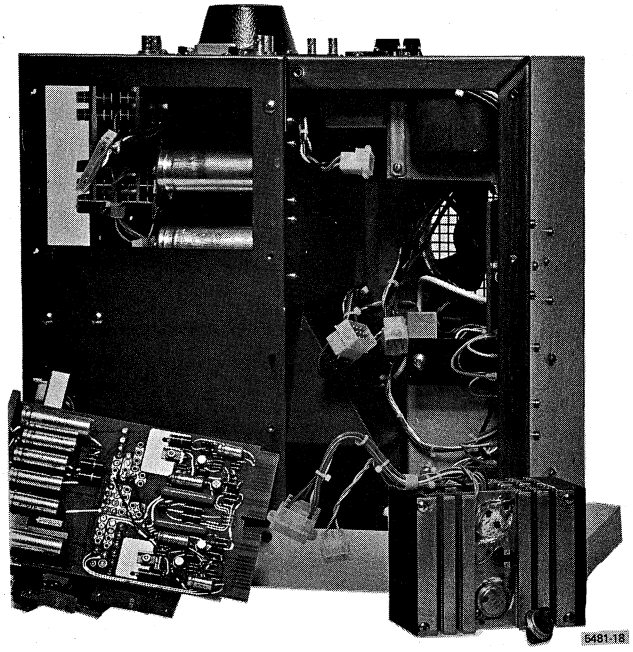
4. The CRT is held by four screws, one at each corner of the screen. As each screw is removed, support the weight of the CRT.

CAUTION

The CRT is under high vacuum and is potentially in danger of implosion if subjected to sharp blows or very rough handling. Also, to avoid dropping the CRT accidentally, never place your hand over the anode high voltage button while picking up or carrying the CRT, in case the CRT has residual charge. The shock is not, in itself, dangerous but the surprise may cause the user to drop the CRT. Never hold the CRT by the neck (the thin cylindrical portion) alone since it will break off.



a. Remove the 7007165 as shown in Figure 4-4 and unscrew the four 6-32 heat sink mounting screws from the side chassis. Remove two pin connector from the high voltage bracket.



b. Lift heat sink straight out and repair faulty transistor.

NOTE

Thermal cutouts have line voltage on them – be sure line cord is removed

Figure 4-5 Regulator Heat Sink Removal

The VR14 CRT has a shell bond frame by which it is directly fastened. The VR17 CRT is fastened to its support bracket by four clamp tubes (DEC part no. 7411301) mounted to the CRT by a worm gear clamp (DEC part no. 9009555). The clamp tubes and worm gear clamp are reused when replacing the VR17 CRT. When installing a new CRT on the VR17, mount the 4 clamp tubes to the CRT using the worm gear clamp. Do not tighten fully, but leave sufficient slack so that the clamp tubes may be aligned with the support bracket screw holes. Once the clamp tubes are aligned, and the CRT fastened to the support bracket, tighten the worm gear clamp.

4.3.5 High Voltage Supply Removal

To remove the high voltage supply proceed as follows:

1. Remove the yoke and CRT as outlined in Paragraph 4.3.4. Ensure that the line cord is unplugged.

2. Disconnect the two red and two white wires from the high voltage supply from TB1 and TB2 of the right side chassis.

3. Remove the cast bezel by removing the three right and left retaining screws.

4. Remove the two side and two bottom high voltage assembly mounting bracket screws and remove the high voltage assembly out toward the front of the unit.

CHAPTER 5
ENGINEERING DRAWINGS

Each VR14/VR17 is shipped with a current set of engineering drawings. If any discrepancies exist between the schematics in this manual, and those delivered with the unit, the set of drawings shipped with the unit should be considered the most accurate. Tables 5-1 and 5-2 list the drawings shipped with the VR14 and VR17, respectively.

Table 5-1
VR14 Engineering Drawings

Title	Drawing No.
Drawing Directory	B-DD-VR14-0
Engineering Specification	A-SP-VR14-0-4
Block Schematic	D-IC-VR14-0-1
Module Utilization	C-MU-VR14-0-3
Module Utilization	A-PL-VR14-0-3
Circuit Schematic (G836)	D-CS-G836-0-1
Circuit Schematic (G840)	D-CS-G840-0-1
Circuit Schematic (G838)	B-CS-G838-0-1
Circuit Schematic (PL)	A-PL-G838-0-0
Circuit Schematic (A225)	D-CS-A225-0-1
Circuit Schematic (W684)	D-CS-W684-0-1
Circuit Schematic (W682)	B-CS-W682-0-1
Circuit Schematic (PL)	A-PL-W682-0-0
Cable Keybd. Interlock	C-IA-7009248-0-0
Circuit Schematic (Heat Sink)	C-CS-7007080-0-1
Circuit Schematic (Deflection)	C-CS-7007082-0-1
Circuit Schematic (Power Supply)	D-CS-7007084-0-1
VR14 Display Assy	D-UA-VR14-0-0
VR14 Display Assy (PL)	A-PL-VR14-0-0
Wired Assy	D-AD-7007078-0-0
Wired Assy (PL)	A-PL-7007078-0-0
Top Mtg Assy	D-AD-7007077-0-0
Top Mtg Assy (PL)	A-PL-7007077-0-0
CRT Yoke Assy	D-IA-7007088-0-0
Light Pen Assy	C-UA-375-0-0
VR14 Accessory List	A-AL-VR14-0-7

Table 5-2
VR17 Engineering Drawings

Title	Drawing No.
Drawing Directory	B-DD-VR17-0
Engineering Specification	A-SP-VR17-0-4
Block Schematic	D-IC-VR14-0-1
Module Utilization	C-MU-VR14-0-3
Module Utilization	A-PL-VR14-0-3
Circuit Schematic (G836)	D-CS-G836-0-1
Circuit Schematic (G840)	D-CS-G840-0-1
Circuit Schematic (A225)	D-CS-A225-0-1
Circuit Schematic (W684)	D-CS-W684-0-1
Cable Keybd. Interlock	C-IA-7009248-0-0
Circuit Schematic (Heat Sink)	C-CS-7007080-0-1
Circuit Schematic (Deflection)	C-CS-7007082-0-1
Circuit Schematic (Power Supply)	D-CS-7007084-0-1
VR17 Display Assy	D-UA-VR17-0-0
VR17 Display Assy (PL)	A-PL-VR17-0-0
Wired Assy	D-AD-7007078-0-0
Wired Assy (PL)	A-PL-7007078-0-0
Top Mtg Assy	D-AD-7007077-0-0
Top Mtg Assy (PL)	A-PL-7007077-0-0
CRT Yoke Assy	D-IA-7007088-0-0
Light Pen Assy	C-UA-375-0-0
VR17 Accessory List	A-AL-VR17-0-6

APPENDIX A
POWER SUPPLY TROUBLESHOOTING

NOTE

The power regulator heat sink contains a thermal cutout connected to the input line voltage. Always remove the line cord before handling the heat sink.

Generally, if the ±22 V reads above ±25 V, one or both of the regulator transistors has shorted. The +22 V is controlled by the PNPs (2N4399) that are the front set of transistors on the regulator heat sink (as viewed from the front of the VR14/VR17). The -22 V is controlled by the NPNs (2N5302) on the rear section of the regulator heat sink. If, after replacing the power transistors, the problem is not corrected, the G836 board itself is suspect. If the regulator circuits are not working, the output could be beyond its nominal value. The MC1709 is the most likely suspect, followed by the drive transistors, Q3 for +22 V and Q1 for -22 V.

If, on the other hand, the ±22 V read zero, the same power transistors are still suspect (they may be open). Also, in this case, if the two 1N4001 diodes used as current limiting for the power transistors are shorted, the power transistors cannot receive base current and thus will not turn on, rendering their output 0 V. To check for this condition, turn off the power and measure resistance with a VOM set at RX1 across D15 and D16 if the +22 V was 0, and D13 and D14 if the -22 V was 0. The resistance with the VOM lead connected either way should always be above 5 Ω.

APPENDIX B
DEFLECTION AMPLIFIER TROUBLESHOOTING

When the deflection circuit cards (A225) are removed, their respective power transistors receive no drive and, therefore, are off. When monitoring A02-A (X-yoke current sample) and A03-A (Y-yoke current sample) no reading should be observed. Any voltage at these points indicates a power transistor is on by itself. Generally this transistor is shorted. To determine which transistor is faulty, observe which pin, A02-A or A03-A, has voltage. The A02-A (X-axis) transistors are on the right side of the heat sink assembly when viewed from the front of the VR14/VR17; A03-A (Y-axis) transistors are on the left side. In both cases, a plus voltage at A02-A or A03-A means the PNPs (2N4399) are at fault. These are the lower transistors on both sides. If the voltage at A02-A or A03-A is minus, the NPNs (2N5302) are faulty. These are the upper transistors on both sides.

If no readings are observed at A02-A or A03-A when the A225 boards are removed, then the deflection fault is on the boards themselves (assuming, of course, proper input signals are applied and all power supply voltages are nominal). If the yoke current goes full negative only when the A225 card is plugged into that axis, the most likely suspect is the 2N2904A, Q2. If one axis is faulty, a quick check can be made by swapping the X- and Y-deflection boards (A225) to see if the faulty axis follows the circuit board in question.

APPENDIX C
A225 REPAIR

After the power supply and deflection power transistors have been proven sound, incorrect deflection coil current readings may be isolated to the A225 circuit board itself. If, when the A225 is plugged in, the deflection current goes full negative (about −4 V as measured at A02-A for X, A03-A for Y) and not controllable, Q2 has probably opened and should be replaced. If only half deflection is working (no positive current or no negative current capability) and the power transistors are operating properly, Q3 should be replaced for no positive current and Q4 for no negative current. Also, check R26 and R27 for burns. These resistors overheat if the deflection amplifier is operated in the fault current limit condition for any length of time. Finally, if C9 or C10 become shorted, R9 or R10, respectively, will burn out. Check C9 or C10 with an ohmmeter to verify this type of failure.

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