DMC11 IPL microprocessor maintenance manual

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EK-DMCMP-MM-001

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DMC11 IPL microprocessor maintenance manual

PRELIMINARY

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CONTENTS

CONTENTS (Cont)

CONTENTS (Cont)

CHAPTER 1

INTRODUCTION

1.1 MICROPROCESSOR GENERAL DESCRIPTION

This manual provides the information necessary to install, operate, and maintain the DMC11 Microprocessor. Specifically, it covers the DMC11-AD Microprocessor which has its ROMs configured to operate under the discipline of the DDCMP protocol. It is organized into five chapters and two appendices as follows.

Chapter 1 - Introduction

Chapter 2 - Installation

Chapter 3 - Device Registers and Programming Information

Chapter 4 - Detailed Description

Chapter 5 - Maintence

Appendix A - PDP-11 Memory Organization and Addressing Conventions

Appendix B - Integrated Circuit Descriptions

In this manual, the term DMC11 denotes the DMC11 Network Link which consists of a microprocessor module and a line unit module. Explicit references to these modules may or may not be prefixed by the term DMC11.

The DMC11-AD Microprocessor module is designated M8200.

Where the computers are located remotely and connected via common carrier facilities, DMC11s can be configured to interface to synchronous modems such as Bell models 208 and 209.

The DMC11 ensures reliable data transmission by implementing the DDCMP line protocol in firmware using a high speed microprocessor. The DDCMP protocol detects errors on the channel interconnecting the systems by using a 16-bit Cyclic Redundancy Check (CRC-16). Errors are corrected, when necessary, by automatic retransmissions. Sequence numbers in message headers ensure that messages are delivered in proper order with no omissions or duplications.

A number of advantates are offered by the DMC11 over conventional interfaces which require a combination of hardware and software to implement a protocol. Programming is greatly simplified. Extensive communications expertise is no longer required when programming the DMC11. PDP-11 memory and processor time are not wasted with instructions implementing the protocol. As a direct result throughput is enhanced because the DMC11 operates at high speeds and is not delayed when the processor has to perform high priority tasks.

There are two versions of the line unit. The M8202 high speed line unit is intended for local network applications using coaxial cables. The M8202 contains an integral modem that operates at 1M bps or 56K bps.

The M8201 low speed line unit has no integral modem but contains level conversion logic to interface with EIA/CCITT V24 or CCITT V35 compatible modems at speeds up to 19.2K bps and 56K bps, respectively.

The M8201 and M8202 line units can operate with DDCMP and Bit Stuff protocols.

The line unit is not a stand alone device. It must be used with a DMC11 Microprocessor.

A separate manual (EK-DMCLU-MM-001) covers the M8201 and M8202 line units.

The Microprocessor is a general purpose control unit providing a full duplex parallel data interface between any PDP-11 family central processor and a given DMC11 Line Unit. With the microprocessor/line unit combination, computers can be configured in many different network applications. Where the computers are located at the same facility, DMC11s can be configured for high speed operation (56,000 or 1,000,000 bits-per-second) over inexpensive coaxial cable. The necessary modems are built-in.

Other DMC11 (M8200) features include:

- Down-line loading of satellite computer systems.
- Ability to initialize an incorrectly functioning satellite computer system by command over the link (Remote Load Detect).
- Same PDP-11 software supporting local or remote, full or half duplex configurations.
- Recovery from power failures at either or both ends of a link without losss of data.
- 16-bit NPR (DMA) transfers.

A typical configuration is illustrated in Figure 1-1. Shown is the DMC11-DA (M8201) line unit used for synchronous data communications. The M8201 interface converts data from the DMC11 to a binary serial format compatible with the Electronic Industries Association RS-232C interface specification, used by nearly all low speed modem manufacturers as a standard.

The other line unit is the M8202 with an integral modem. The overall system function is identical to that of the M8201. In this case however, because of the built-in modem, the M8202 interfaces directly to a local coaxial cable.

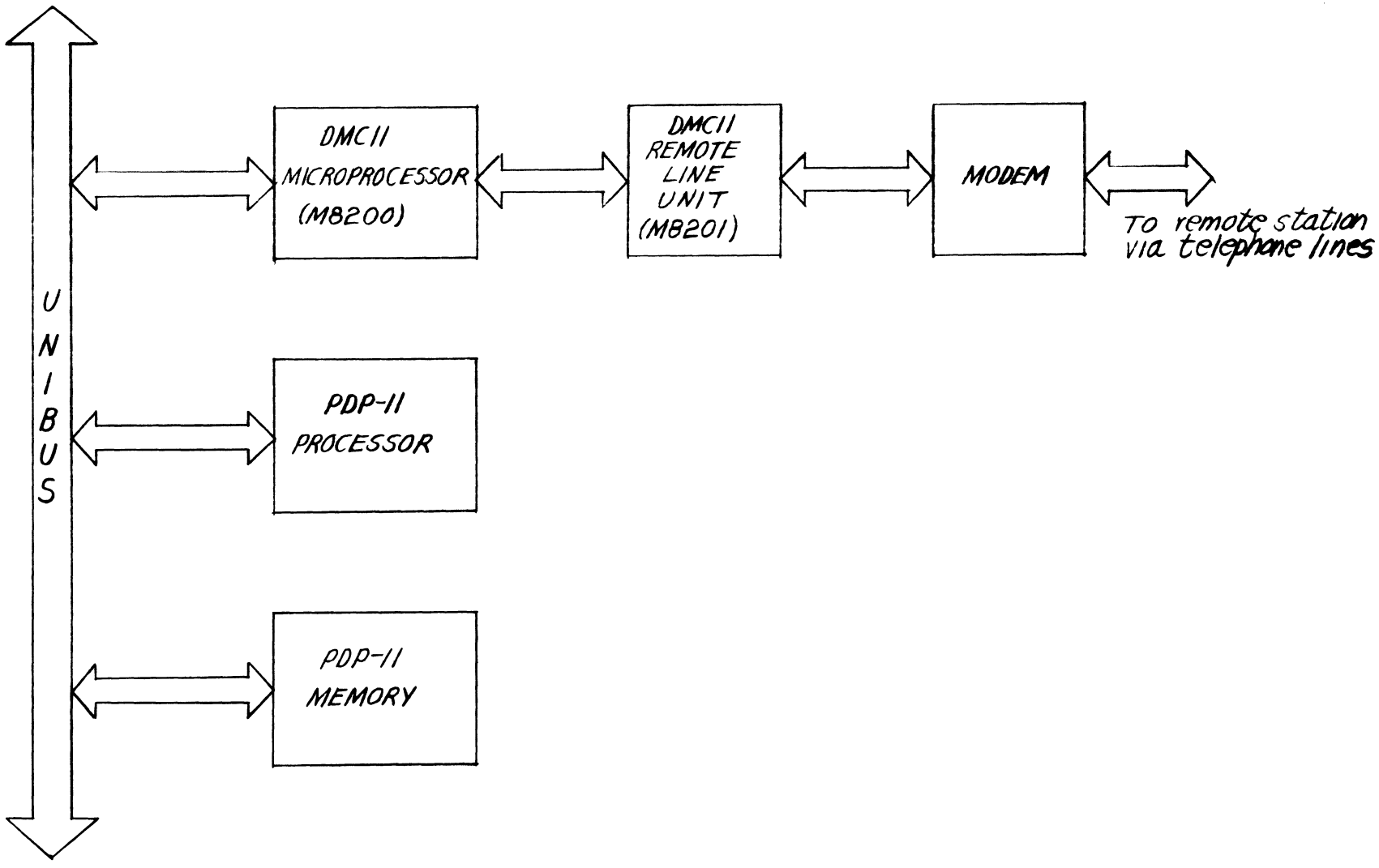


Figure 1-1 DMC11 Remote Line Unit Interface

This configuration uses a single coaxial cable for half duplex operation or two coaxial cables for full duplex operation. (Figure 1-2).

Figure 1-2 defines in greater detail the general interface between the microprocessor and any line unit. First, there are two eight bit parallel data buses; one is an input bus and the other is an output bus. Two separate buses are used to sustain full duplex operation. In the line unit, the data source is addressed by the microprocessor using the INPUT/OUTPUT register address bus.

The line unit contains eight registers. During a read operation, which uses the INPUT bus, the microprocessor uses four addressing bits. The most significant bit is held low to show that a line unit register is being read. The other three bits select the line unit register to be read. During a write operation, which uses the OUTPUT register, the microprocessor uses four different addressing bits. The most significant bit is an enabling bit and the other three bits select the line unit register to be written into. Simultaneous addressing on the INPUT and OUTPUT buses is possible.

The remaining bus, the control signal interface, delivers timing and control information to the line unit such as clock sync and data strobe signals.

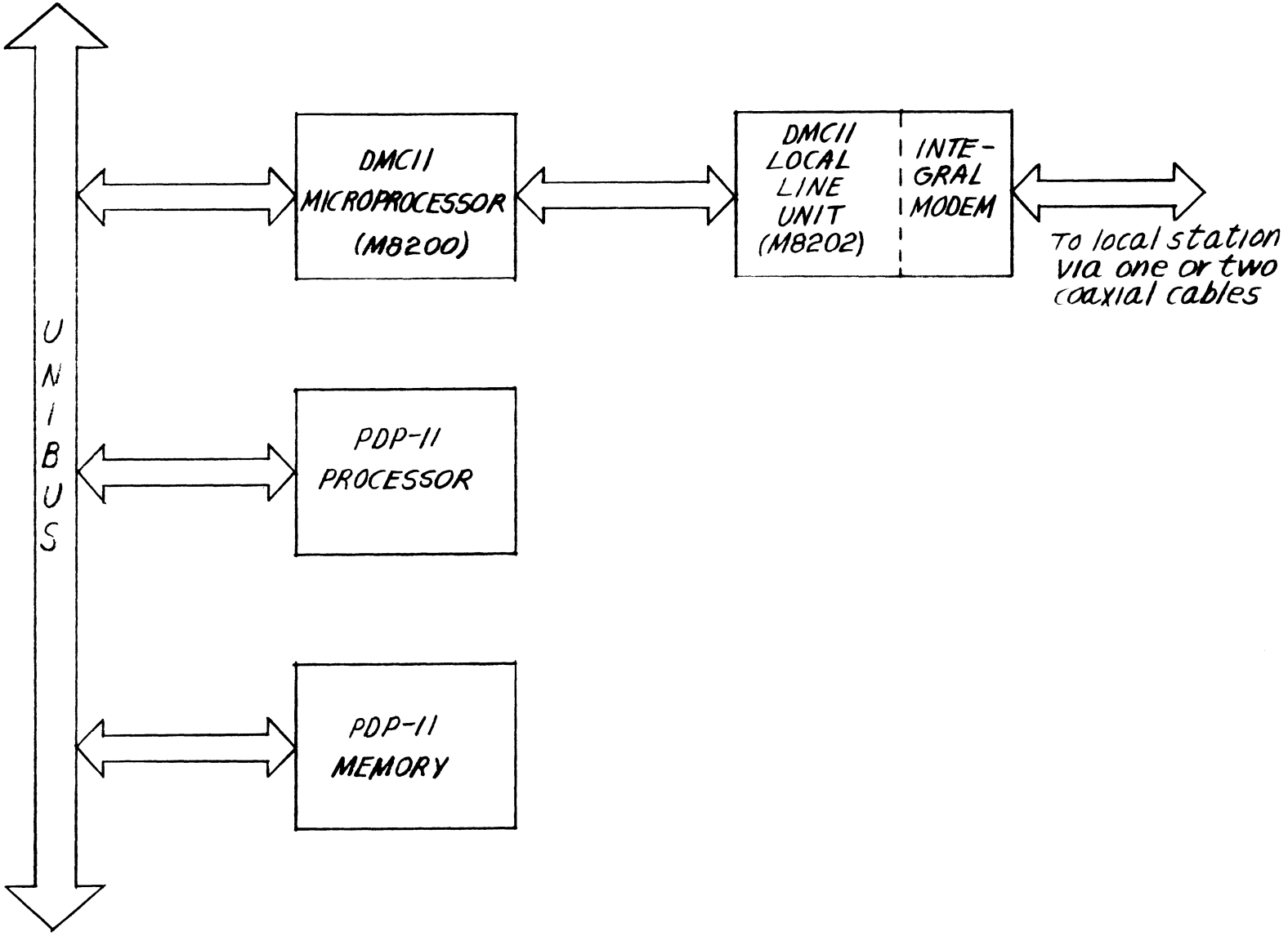


Figure 1-2 DMC11 Local Line Unit Interface

Data transfers between the DMC11 and the PDP-11 processor are in the form of the three common bus transactions. They are the NPR bus cycle, the interrupt sequence, and the reading (DATI) and writing (DATO) of DMC11 Control and Status Registers (CSR's).

The UNIBUS CSR's are composed of eight bytes of device addresses and are accessed by addresses 76XXX0 through 76XXX7. These device addresses are henceforth referred to as Byte Select (BSEL) 0-7 for indicating individual bytes, and SEL 0, 2, 4, 6 for indicating word transfers (SEL0 consists of BSEL0 and BSEL1, SEL2 consists of BSEL2 and BSEL3, etc...). BSEL0 and BSEL2 are handshaking CSR's which interlock transfers through a common data port. This data port is accessed through BSEL4-7 (SEL 4,6).

When the PDP-11 program wishes to transfer data to the DMC11, the program (through BSEL0) sets up a REQUEST IN (RQI) and a function describing the data to be passed. The DMC11 responds by setting READY IN. BSEL4-7 is then loaded by the PDP-11 program, and clears RQI. The DMC11 takes the data and drops RDYI which completes the exchange.

Similarly, the DMC11 transfers data to the PDP-11 program by setting READY OUT (RDYO) with a function after having loaded BSEL 4-7. The PDP-11 program, after reading the required registers, should then clear RDYO, releasing the port for further use.

The DMC11-AD (M8200) is referenced as a microprocessor throughout this manual as well as in other related documentation.

This is due to the fact that ROMs are used as controlling elements. The ROMs act as compact logic arrays that replace a large amount of distributive logic. For example, a 2048 bit ROM is organized as 512 words of 4-bits each. Combining four of these ROMs produces 512 words of 16-bits each. Each word in the ROM is pre-programmed and in unalterable. When addressed, a specific word always produces the same output.

The information stored in the ROMs at the word level can be called microsteps. Executing an appropriate series of microsteps is called a microroutine. It can represent a particular instruction or function. The combination of microroutines is called a microprogram.

As the microroutine is being executed, the ROM output signals are sent to the appropriate circuits in the microprocessor to perform the instruction or function that is represented by the microroutine.

As illustrated in Figure 1-3, the DMC11 essentially connects the UNIBUS to the line unit interface through internal registers. This allows the data to be processed by the microprocessor as it passes between the two buses. The processing is dependent on the microprogram residing in the microprocessor. Currently, a microprogram is available to accommodate the DDCMP line protocol.

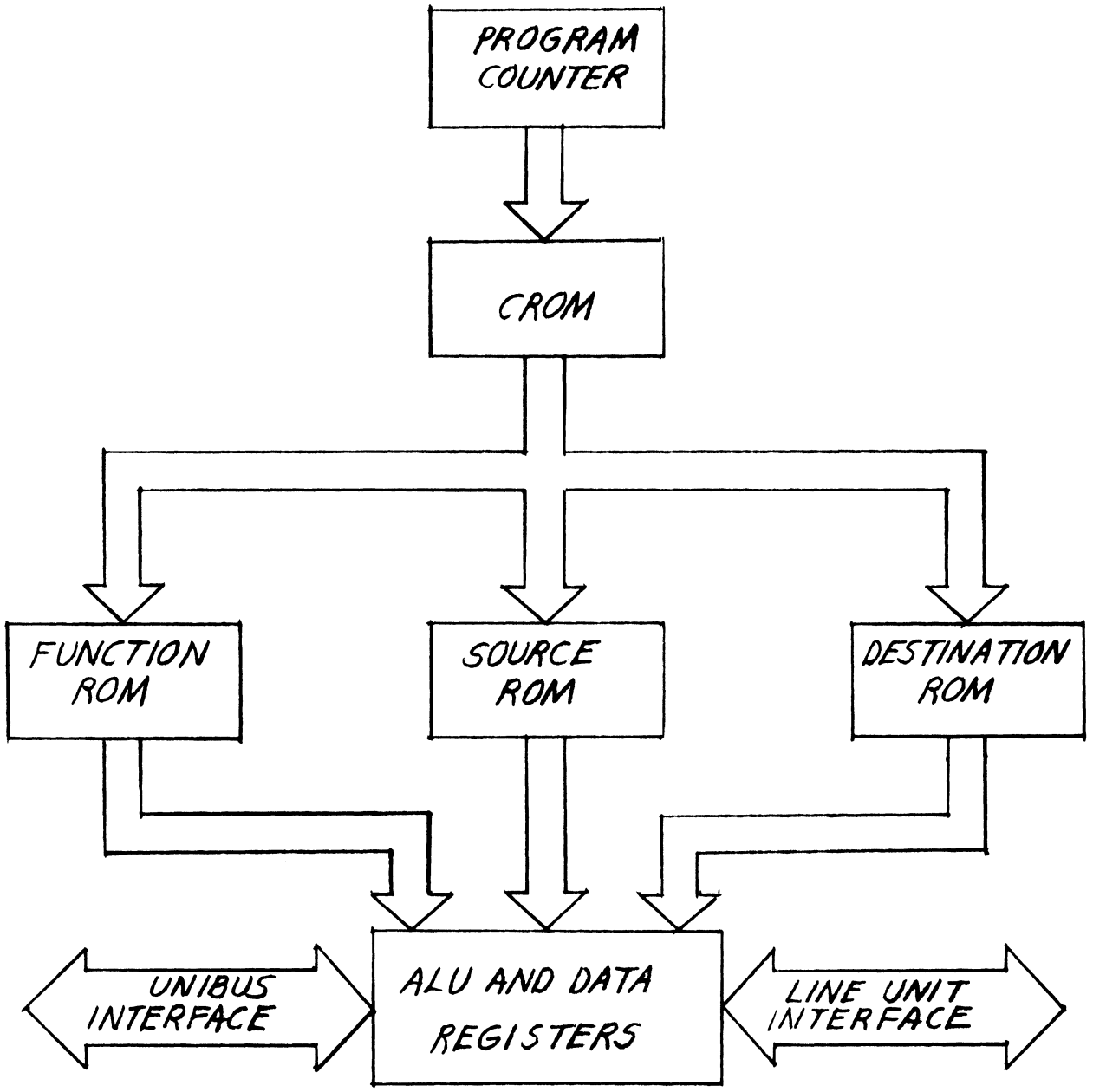


Figure 1-3 Microprocessor Simplified Block Diagram

The block diagram in Figure 1-3 very much resembles a processor, hence the term microprocessor. It has a program counter (PC) addressing the microprogram residing in 1K of ROM. Each microinstruction is a sixteen bit word. Certain bits of the microinstruction then serve as address bits for three additional ROM's which control data flow and determine what operation to perform on the operands. Chapter 4 covers these internal registers in more detail.

The DMC11 and line unit consist of two separate modules interconnected by a one foot cable. Each is ordered separately. One microprocessor version and four synchronous line unit versions are available: local operation at 1M bps, local operation at 56K bps, remote operation with EIA/CCITT V24 compatible modems up to 19.2K bps, and remote operation with CCITT V35 compatible modems up to 56K bps.

The DMC11-AD microprocessor module (hex SPC) includes a 300 nsec bipolar microprocessor, a ROM implementing the DDCMP protocol, local scratch pad memory, and a UNIBUS interface.

The DMC11-MA line unit module (notched hex) includes a built-in modem for local operation at 1M bps over coaxial cable up to 6,000 feet in length.

The DMC11-MD line unit module (notched hex) includes a built-in modem for local operation at 56K bps over coaxial cable up to 18,000 feet in length.

Coaxial cables are not included with either line unit. Optional BC03N-A0 coaxial cable is available in 100 ft lengths only. One is required for half-duplex operation and two are required for full-duplex operation.

The two versions of the remote line unit, DMC11-DA and DMC11-FA, use the same module (M8201). Both versions contain level conversion logic that accommodates the EIA/CCITT V24 interface and the CCITT V35 interface. The only difference is the modem cable that is supplied to match the specified interface.

The DMC11-DA is shipped with a 25 foot BC05C cable for the EIA/CCITT V24 interface to accommodate Bell 208 or 209 synchronous modems or their equivalent.

The DMC11-FA is shipped with a 25 foot BC05Z cable for the CCITT V35 interface. This synchronous interface is used in certain European networks and in the domestic Digital Data Service (DDS).

CHAPTER 2

INSTALLATION

2.1 SCOPE

This chapter provides all necessary information for a successful installation and subsequent checkout of the DMC11 micro-processor subsystem.

2.2 UNPACKING AND INSPECTION

The microprocessor/line unit system combination arrives at the customer site in one of two ways, either as a part of a complete computer system or as an add-on option. When it arrives as an add-on option, the microprocessor module, line unit module, and associated mounting hardware and cables arrive packaged in a single carton. Inspect the carton visually for any signs of physical damage. Included in the contents of the carton are the following.

1. M8200-YA Microprocessor Module
2. M8201 or M8202 Line Unit Module
3. BC08S-1 Cable (Interconnects microprocessor and line unit)
4. BC05C-25 Cable (M8201 EIA/CCITT V24 interface only)
5. BC05Z-25 Cable (M8201 CCITT V35 interface only)
6. H325 Test Connector (M8201 only)
7. 12-12528 Coaxial Cable Test Connector (M8202 only)
8. MAINDEC-11 DZDMC Microprocessor Basic W/R and Up Test

9. MAINDEC-11 DZDME Line Unit DDCMP Test

10. MAINDEC-11 DZDMF Line Unit Bit Stuff Test

11. MAINDEC-11 DZDMG Jump and Free Running Test

12. ---- DEC/XII System Test

13. ---- ITEP One Line Test

14. EK-DMCUP-MM-001 Microprocessor Manual

15. EK-DMCLU-MM-001 Line Unit Manual

2.3 OPTION DESIGNATIONS

There is only one microprocessor available. It is designated DMC11-AD and its ROMs are configured to implement the DDCMP protocol only.

The various line units and cables are listed in Table 2-1 and 2-2, respectively.

2.4 MECHANICAL PACKAGING

The DMC11 consists of a microprocessor module (hex) and a line unit module (notched hex). These modules plug into any DD11-B Rev E or later, DD11-C, DD11-D or equivalent SPC system unit. The microprocessor module must always plug into either slot 2 or 3 in the DD11-B or DD11-C. The line unit module may be installed into any of the remaining slots. Should two DMC11's be installed in a single DD11-B, then the line unit module plugs into slot 1 or 4.

Table 2-1

Line Unit Option Designations

Option	Description
DMC11-DA	M8201 Line Unit Module with cable for EIA/CCITT V24 interface
DMC11-FA	M8201 Line Unit Module with cable for CCITT V35 interface
DMC11-MA	M8202-YA Line Unit Module with 1 Mbps integral modem and no cable
DMC11-MD	M8202-YD Line Unit Module with 56 Kbps integral modem and no cable

Table 2-2

Line Unit Cables

Option	Description
BC03N-A0	100 ft. coaxial cable with connectors. Used with M8202 Line Unit Module.
BC05C-25	25 ft. EIA/CCITT V24 cable for use with DMC11-DA Line Unit.
BC05Z-25	25 ft. CCITT V35 cable for use with DMC11-FA Line Unit.

The line unit does not interface with the Unibus so module edge connectors A and B are not required. As a result, the corner of the module in the vicinity of the A and B connectors has been removed. This allows the M8201 and M8202 to be installed in the end slots of the DD11-B, C, and D System Interfacing Units. The module plugs into connectors C, D, E,and F and fits over the Unibus cable connector and short length (approximately 2-1/2 in.) Unibus terminator that are installed in end slot connectors A and and B.

The two modules are interconnected by a BERG 40-pin connector and a one-foot BC08S-1 cable.

2.5 PRE-INSTALLATION PROCEDURES

2.5.1 General Information

Installation of the microprocessor/line unit combination should be done in three phases. First the microprocessor is physically installed then checked and verified with MAINDEC-11 DZDMC. In this manner the microprocessor is checked as a stand-alone module apart from the line unit. Next, the line unit module is installed and operationally verified with MAINDEC-11 DZDME and MAINDEC-11 DZDMR which also provides an additional confidence factor for the microprocessor. The third and final installation phase involves the execution of MAINDEC-11 DZDMG which verifies the operational status of both the microprocessor and the line unit as a free

running test. Additionally, this test checks the contents of the ROMs (microcode) and the BRANCH instructions.

A minimum of 8K of memory is necessary for execution of the MAINDEC diagnostics.

Check the power supply to insure against overloading. The microprocessor/line unit total current requirements for the +5 volt supply is approximately 8 Amperes. Additionally, the line unit requires ±15V for the silos and the level conversion logic and the integral modem.

Installation requires two adjacent Hex SPC slots, one of which can be either the UNIBUS input or terminator slot if the modules are 2-1/2 in. or less. The DMC11 microprocessor requires a full hex slot while the line unit fits into any slot in the DD11 backplane. The microprocessor can be installed in the DD11-B Rev E or higher, DD11-C, DD11-D or equivalent backplanes. Such an equivalent backplane is that used in the PDP-11/04 or PDP-11/34 Computers.

2.5.2 Preinstallation Checkout Procedures

Before installing the microprocessor module, the following functions must be performed.

1. Verify that jumper W1 is installed. This jumper should not be removed in the field. It is removed only at the factory during automated module testing to inhibit the oscillator in the microprocessor clock logic.

2. The microprocessor device address must be selected in accordance with paragraph 2.7.

3. The microprocessor vector address must be selected in accordance with paragraph 2.8.

4. Verify that a BR5 priority card is installed in position E75.

5. Verify that switch numbers 7 and 9 in the DIP switch package located in position E76 are both OFF. In this package, switches 1-6 are used for the vector address and switches 8 and 10 are not used.

Switch 7 is the Run Inhibit (RI) switch which is connected between ground and the CLEAR input of the RUN flip-flop. Normally, it is OFF and the RUN flip-flop cannot be directly cleared. Under normal conditions, initialization of the microprocessor directly sets the RUN flip-flop which allows the microcode to be executed immediately. Because of an internal malfunction or execution of malicious microcode during power up, it is possible for the

microprocessor to hang the Unibus. Now, it is not possible to load the diagnostics to determine the fault. Placing the Run Inhibit Switch in the ON position clears the RUN flip-flop and allows the diagnostics to be loaded.

Switch 9 is the Byte Sel 1 Lockout (BS1) switch. It is related to the "computer in a closet" application where all programs are down line loaded. When set, the BS1 switch prevents a runaway program in the PDP-11 Processor from preventing a boot or down line loading operation via the DMC11 link. This switch inhibits all maintenance functions.

NOTE

Before installing the microprocessor (M8200), remove the NPR Grant wire that runs between pins CA1 and CB1 on the backplane for the slot that is going to accept the M8200. Do not remove the wire for the slot that is going to accept the line unit (M8201 or M8202).

The M8200 Microprocessor presents one load to the Unibus and the M8201 and M8202 Line Units present no load to the Unibus except for power requirements.

The local DMC11 configuration (DMC11-AD Microprocessor and DMC11-MA or DMC11-MD Line Unit) requires bus placement nearest to the

PDP-11 Processor. This is due to the high rate of NPR transactions that are required. For example, the DMC41-MA Line Unit (1 Mbps) requires an average of one NPR every 8μs.

2.6 INSTALLATION

After completing the pre-installation checkout procedures in paragraph 2.5.2, proceed with the installation as follows.

1. Insert the microprocessor module in the proper backplane slot.

2. Run MAINDEC-11 DZDMC to verify correct operation of the microprocessor.

DIAGNOSTIC NOTE

If the installation is in a system using a PDP-11/04 or other PDP-11 Processor that does not have a switch register, a software switch register is used to allow the user the same switch options. If a switch register is available but contains all 1s (177777), the software switch register is used. Refer to the appropriate diagnostic document for further details.

3. Check all appropriate switch settings and jumpers on the line unit module in accordance with the recommendations in Chapter 2 INSTALLATION of the line unit manual (EK-DMC11LU-MM-001).

4. Insert the line unit module in the proper backplane slot.

5. Interconnect the line unit and microprocessor using cable BC08S-1 which is a one-foot long 40 conductor flat mylar cable with H856 female connectors on each end. The mating connector on the microprocessor and line unit is an H854 male connector. On the microprocessor, this connector is designated J1. On the M8201 Line Unit, it is designated J2 and on the M8202 Line Unit it is J1.

6. On the M8201, install the BC05C-25 cable to connector J1. On the other end of this cable, connect the H325 test connector.

   On the M8202, install the 12-12528 coaxial test connector which ties the two coaxial pigtails together. These two 3-foot cables are soldered to the M8202.

7. On the M8202, check that the integral modem clock is within specifications. Refer to the line unit manual.

8. On the backplane, check that the supply voltages are within the following tolerances.

Voltage			Backplane
Min	Nominal	Max	Pin
+4.75	+5.0	+5.25	C1A2
-14.25	-15.0	-15.75	C1B2
+14.25	+15.0	+15.75	C1U1

9. Run MAINDEC-11 DZDME and DZDMF to verify correct line unit operation.

10. Run MAINDEC-11 DZDMG to verify correct line unit/ microprocessor operation. This diagnostic also tests the microcode and BRANCH instructions.

11. Remove the test connector.

For the M8201, connect the BC05C-25 or BC05Z-25 cable to the customer supplied modem.

CAUTION

The maximum allowable length for the BC05C and BC05Z cables is 50 feet.

For the M8202, connect the pigtails to the customer coaxial cables or the optional 100 foot BC03N-A0 cable.

2.7 DEVICE ADDRESSES

2.7.1 Introduction

Starting with the DJ11, new communications devices are to be assigned floating addresses. The addresses for current production devices are to be retained.

The word floating means that addresses are not assigned absolutely for the maximum number of each communications device that can be used in a system.

2.7.2 Floating Device Address Assignments

Floating device addresses are assigned as follows:

1. The floating address space starts at location 760010 and extends to location 764000 (octal designations).

2. The devices are assigned in order by type: DJ11, DH11, DQ11, DU11, DUP11, DMC11, and then the next device introduced into production. Multiple devices of the same type must be assigned contiguous addresses.

3. The first address of a new type device must start on a modulo 10_8 boundary, if it contains one to four bus-addressable registers. The starting address of the DH11 must be on a modulo 20_8 boundary because the DH11 has eight registers.

4. A gap of 10_8, starting on a modulo 10_8 boundary, must be left between the last address of one type device and the first address of the next type device. A gap must be left for any device on the list that is not used, if the device following it is used. The equivalent of a gap should be left after the last device assigned to indicate that nothing follows.

5. No new type devices can be inserted ahead of a device on the list.

6. If additional devices on the list are to be added to a system, they must be assigned contiguously after the original devices of the same type. Reassignment of other type devices already in the system may be required to make room for the additions.

The following examples show typical floating device assignments for communications devices in a system.

Example 1: No DJ11s, 2 DH11s, 2 DQ11s, 1 DUP11, and 1DMC1

760010 DJ11 gap

760020 DH11 #0 first address

760040 DH11 #1 first address

760060 DH11 gap

760070 DQ11 #0 first address

760100 DQ11 #1 first address

760110 DQ11 gap

760120 DU11 gap

760130 DUP11 #0 first address

760140 DUP11 gap

760150 DMC11 #0 first address

760160 Indicates no more DMC11s and no other devices follow.

Example 2: 1 DJ11, 1 DH11, 2 DQ11s, 2 DUP11s, and 2 DMC11s

760010 DJ11 #0 first address

760020 DJ11 gap

760040 DH11 #0 first address

760060 DH11 gap

760070 DQ11 #0 first address

760100 DQ11 #1 first address

760110 DQ11 gap

760120 DU11 gap

760130 DUP11 #0 first address

Example 2 (Cont.)

760140 DUP11 #1 first address

760150 DUP11 gap

760160 DMC11 #0 first address

760170 DMC11 #1 first address

760200 Indicates no more DMC11s and no other devices following.

2.7.3 Device Address Selection

In the floating address space (760010-764000), bits 13-17 are always 1s (function of PDP-11 processor). Appendix A shows the PDP-11 memory organization and addressing conventions. Bits 3-12 are selected by switches in the address decoding logic (Table 2-3). With the switch on (closed), the decoder looks for a 0 on the associated Unibus address line. Bits 0, 1 and 2 are decoded to select 1 of 8 registers.

The device address selection switches are contained in one DIP switch package located in position E113. All 10 switches in the package are used. The correlation between switch numbers and address bit numbers is shown in Table 2-3. The ON and OFF positions and the switch numbers are marked on the package. The switches are rocker type and are pushed to the desired position (Figure 2-1).

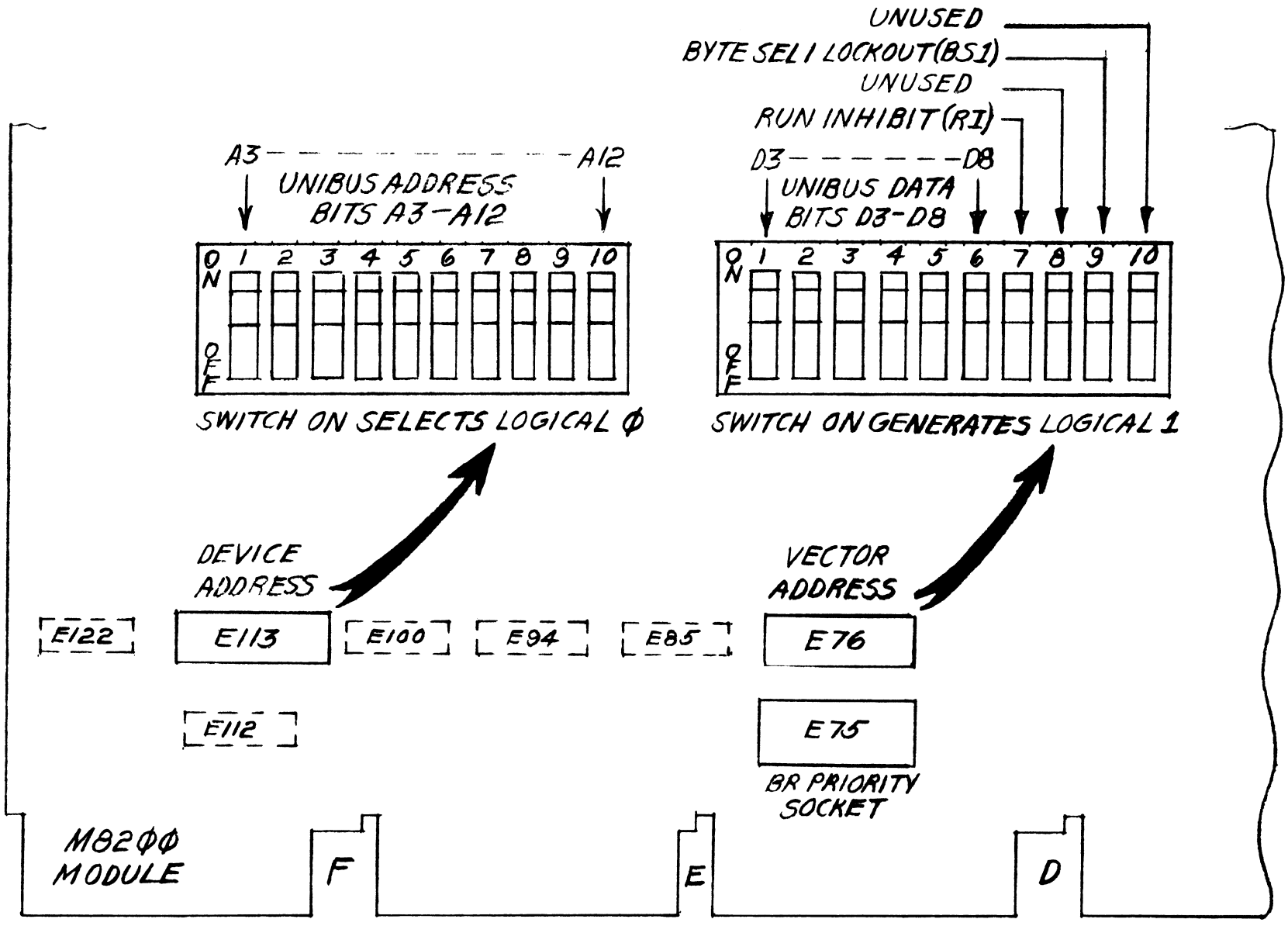


Figure 2-1 Microprocessor Device
and Vector Address Switches

Table 2-3

Guide for Setting Switches to

Select Device Address

Switch No.	10	9	8	7	6	5	4	3	2	1	Device
Bit No.	12	11	10	9	8	7	6	5	4	3	Address
										X	760010
									X		760020
									X	X	760030
								X			760040
								X		X	760050
								X	X		760060
								X	X	X	760070
							X				760100
						X					760200
						X	X				760300
					X						760400
					X		X				760500
					X	X					760600
					X	X	X				760700
				X							761000
			X								762000
			X	X							763000
		X									764000

NOTES:

1. X means switch off (open) to respond to logical 1 on the Unibus.
2. Switch numbers are physical positions in switch package 1.

2.8 VECTOR ADDRESSES

2.8.1 Introduction

Communications devices are assigned floating vector addresses. This eliminates the necessity of assigning address absolutely for the maximum number of each device that can be used in the system.

2.8.2 Floating Vector Address Assignment

Floating vector addresses are assigned as follows:

1. The floating address space starts at location 300 and proceeds upward to 777. Addresses 500-534 are reserved.

2. The devices are assigned in order by type: DC11; KL11/DL11-A, B; DP11; DM11-A; DN11; DM11-BB; DR11-A; DR11-C; PA611 Reader; PA611 Punch; DT11; DX11; DL11-C, D, E; DJ11; DH11; GT40; LPS11; VT20; DQ11; KW11-W; DU11; DUP11; DV11; DMC11.

3. If any type device is not used in a system, address assignments move up to fill the vacancies.

4. If additional devices are to be added to the system, they must be assigned contiguously after the original devices of the same type. Reassignment of other type devices already in the system may be required.

2.8.3 Vector Address Selection

Each drive interrupt vector requires four address locations (two words) which implies only even-numbered addresses. A further constraint is that all vector addresses must end in a 0 or 4. The vector address is specified as a three digit, binary-coded, octal number using Unibus data bits 0-8. Because the vector must end in 0 or 4, bits 1 and 0 are not specified (they are always 0) and bit 2 determines the least significant octal digit of the vector address (0 or 4). The interrupt control logic send only seven bits (2-8) to the PDP-11 processor to represent the vector address.

The DMC11 is shipped with a BR5 priority selection card installed in the interrupt control logic. This logic generates two vector addresses: RDY I interrupts generate vector addresses of the form XX0, and RDY O interrupts generate vector addresses of the form XX4. For this method of operation, the state of bit 2 is selected by the logic not by a switch. The two most significant octal digits of the vector address are determined by switches in lines 3-8 (Table 2-4). With the switch OFF (open), a 0 is generated on the associated Unibus data line; with the switch ON (closed), a 1 is generated on the associated Unibus data line.

The vector address selection switches are contained in one DIP package located in position E76 (Figure 2-1). Only 6 of the 10 switches in the package are used for the vector address. The

correlation between switch numbers and bit numbers is shown in Table 2-4. The ON and OFF positions and the switch numbers are marked on the package. The switches are rocker type and are pushed to the desired position.

2.9 INSTALLATION CHECKLIST

The following items represent a concise checklist of the important features of the DMC11 installation.

1. Power Requirements

   M8200 +5V @ 4.0 A

   M8201 +5V @ 3.0 A
   +15V @ 0.03 A
   -15V @ 0.31 A

   M8202 +5V @ 3.0 A
   +15V @ 0.18 A
   -15V @ 0.46 A

2. Unibus Loading

   The M8200 presents one Unibus load. The M8301 and M8202 present no Unibus loads.

3. Special Installation Requirements

   a. M8200 Microprocessor

      Before installing, remove the NPR Grant continuity wire that runs between pins CA1 and CB1 on the backplane

Table 2-4

Guide for Setting Switches to Select Vector Address

Switch Switch No.	6	5	4	3	2	1	Vector
Bit No.	8	7	6	5	4	3	Address
	X			X	X	X	300
	X			X	X		310
	X			X		X	320
	X			X			330
	X				X	X	340
	X				X		350
	X					X	360
	X						370
		X	X	X	X	X	400

		X		X	X	X	500

			X	X	X	X	600

				X	X	X	700

Notes:

1. X means switch off (open) to produce a logical 0 on the Unibus.
2. Switch numbers are physical positions in switch package 2.

for the slot that is going to accept the M8200. If a system change requires removal of the M8200, the wire must be replaced.

b. M8200 Microprocessor with Local Line Units (DMC11-MA or DMC11-MD)

This configuration must be placed on the Unibus closest to the PDP-11 Processor because of the high rate of NPR transactions that are required. It must also be placed before a DB11-A Bus Repeater if one is used.

4. M8200 Microprocessor Switch Settings

a. Address Selection (E113)

Switch No.	Address Bit
1	3
2	4
3	5
4	6
5	7
6	8
7	9
8	10
9	11
10	12

Switch OFF (open) to respond to logical 1 on Unibus.

Switch ON (closed) to respond to logical 0 on Unibus.

b. Vector Selection (E76)

Switch No.	Vector Bit
1	3
2	4
3	5
4	6
5	7
6	8

Switch OFF (open) to produce a logical 0 on the Unibus.

Switch ON (closed) to produce a logical 1 on the Unibus.

c. Remaining Switches in E76

Switch 7 is RUN INHIBIT (RI) and should be OFF.

Switch 9 is BYTE SEL 1 LOCKOUT (BS1) and should be OFF.

Switches 8 and 10 are not used and should be OFF.

5. Line Unit Switch Settings and Jumper Configuration as Shipped

a. Switch Settings

(1) Switch Pack No. 2 (E87 on M8201 and E90 on M8202) - All switches should be OFF.

(2) Switch Pack No. 3 (E88 on M8201 and E91 on M8202) - All switches should be OFF.

(3) Switch Pack No. 1 (E26 on M8201 and E29 on M8202) - The switches should be positioned as shown in Figure 2-2.

b. The jumpers should be configured as shown in Figure 2-2.

*	DMC11-DA	DMC11-FA	DMC11-MA/MD
Switch No.	M8201	M8201	M8202
1	OFF	OFF	OFF
2	OFF	OFF	OFF
3	OFF	OFF	OFF
4	OFF	ON	OFF
5	OFF	OFF	OFF
6	OFF	OFF	OFF
7	ON	ON	OFF
8	ON	ON	OFF
Jumper No.			
1	IN	IN	IN
2	IN	IN	OUT
3	OUT	OUT	OUT
4	IN	IN	OUT
5	OUT	OUT	OUT
6	Not Present	Not Present	OUT (FD) IN (HD)

NOTES:

* Switch pack no. 1 located at E26 on M8201 and E29 on M8202.

FD = Full Duplex

HD = Half Duplex

Figure 2-2 Configuration of Jumpers and Switch Pack No. 1 on Line Unit

CHAPTER 3

PROGRAMMING INFORMATION

3.1 INTRODUCTION

This chapter contains general information necessary for PDP-11 programming of the DMC11 Microprocessor. In general, the information is presented by operational categories such as input transfers, output transfers, etc. Also included are descriptions of the Unibus control and status registers, microprocessor control and status registers, and line unit control and status registers.

The information in this chapter is arranged as follows.

3.2 INTERRUPT VECTORS

The DMC11 generates two vector addresses: input (PDP-11 to microprocessor) interrupts generate vector addresses of the form XX0; and output (microprocessor to PDP-11) interrupts generate vector addresses of the form XX4. The conditions that initiate the interrupts are:

XX0 - An interrupt at address XX0 occurs when the PDP-11 requests the port (SEL4 or SEL6) and the microprocessor responds by asserting Ready In (RDYI) and Interrupt Enable In. (IEI).

XX4 - An interrupt at address XX4 occurs when, after charging the port with data, the microprocessor asserts Ready Out (RDYO) and Interrupt Enable Out (IEO).

3.3 PRIORITY SELECTION

The priority for the interrupts is selectable on the microprocessor via a plug-in priority selection card. It is shipped with a card that establishes BR5 as the priority level.

3.4 PDP-11 PROGRAMMING INFORMATION

3.4.1 Introduction

Programming the DMC11 is described at two levels. The first level describes how a PDP-11 program uses the DMC11 control and status registers together with the interrupt system for transfer of control and status information between the PDP-11 program and the DMC11 microprogram. The second level describes details of these transactions, including formats, details of device and protocol initialization, data transfer and unusual cases.

In order to successfully program the DMC11, it is not necessary to be familiar with the details of DDCMP protocol operation. These are handled by the DMC11 microprogram. However, some familiarity with the protocol operation is useful in interpreting the significance of the various error counters provided to assess the quality of the circuit connecting the two computers. If a DMC11 is to communicate with a different interface, which uses a software implementation of DDCMP, the person programming the software implementation should consult the DDCMP protocol standard document.

3.4.2 Unibus Control and Status Registers

Communication of control and status information between the PDP-11 and the DMC11 uses eight bytes of control and status registers (CSR's). These are addressed as 76XXX0, 76XXX1, 76XXX2, 76XXX3, 76XXX4, 76XXX5, 76XXX6, and 76XXX7. These device addresses are

subsequently referred to as Byte Select 0 to 7 (BSEL0 - BSEL7) for indicating individual bytes and as SEL0, SEL2, SEL4, and SEL6 for indicating words.

NOTE

The Control and Status Registers are implemented with Random Access Memory (RAM). Thus, at power on, the CSR's come up in random states. As part of the microprocessor initialization, the CSR's (SEL0-6) are cleared with the exception of bit 15 of SEL0 (RUN) which is set. The lower order 8 bits of SEL0 (BSEL0) are cleared first, Due to the high speed of the microprocessor, the registers are cleared before access by the PDP-11 is possible.

BSEL4-7 comprise a 32 bit data port that is used to pass information between the microprocessor and the PDP-11. The transfer of information from the PDP-11 to the microprocessor is called an Input Transfer, often abbreviated IN or I. The transfer of information from the microprocessor to the PDP-11 is called an Output Transfer, often abbreviated OUT OR O. These terms are not to be confused with sending and receiving data on the serial line which are called sending or transmission, and receiving or reception.

BSEL0 controls input transfers and BSEL2 controls output transfers. BSEL1 contains bits used for maintenance purposes which are of no concern to the programmer. It also contains the MASTER CLEAR bit which can be used to initialize the DMC11 microprocessor. BSEL2 is not used. A switch on the microprocessor module prevents the PDP-11 program from clearing RUN or performing other maintenance functions in BSEL1 which would disable the microprocessor's ability to initialize an unattended PDP-11 computer system.

As reference for the programmer, the bit assignments for the Unibus CSRs are shown in Figure 3-1. A detailed description of each register is shown in tabular form.

3.4.2.1 BSEL0 - Input Register

This register comprises the low byte of address 76XXX0 (Figure 3-1).

Bit	Name	Description
0, 1	TYPE INPUT (TYPE I)	These bits define the type of input transfer as follows.

Bit 1	Bit 0	Buffer Address/
0	0	Character Count In (BA/CC I)
0	1	Control In (CNTL I)
1	0	Reserved
1	1	Base In (BASE I)

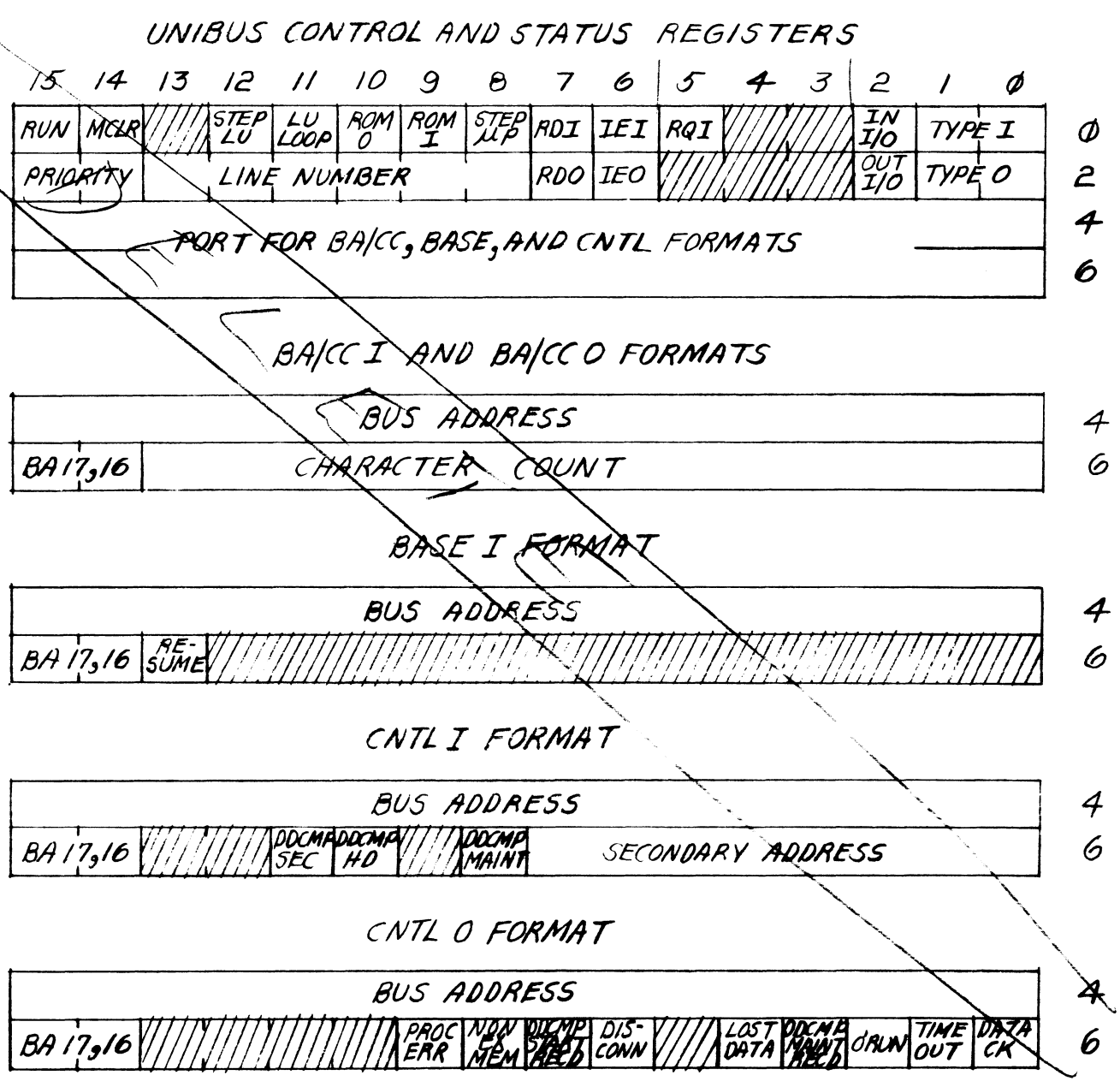


Figure 3-1 Unibus Control and Status Registers

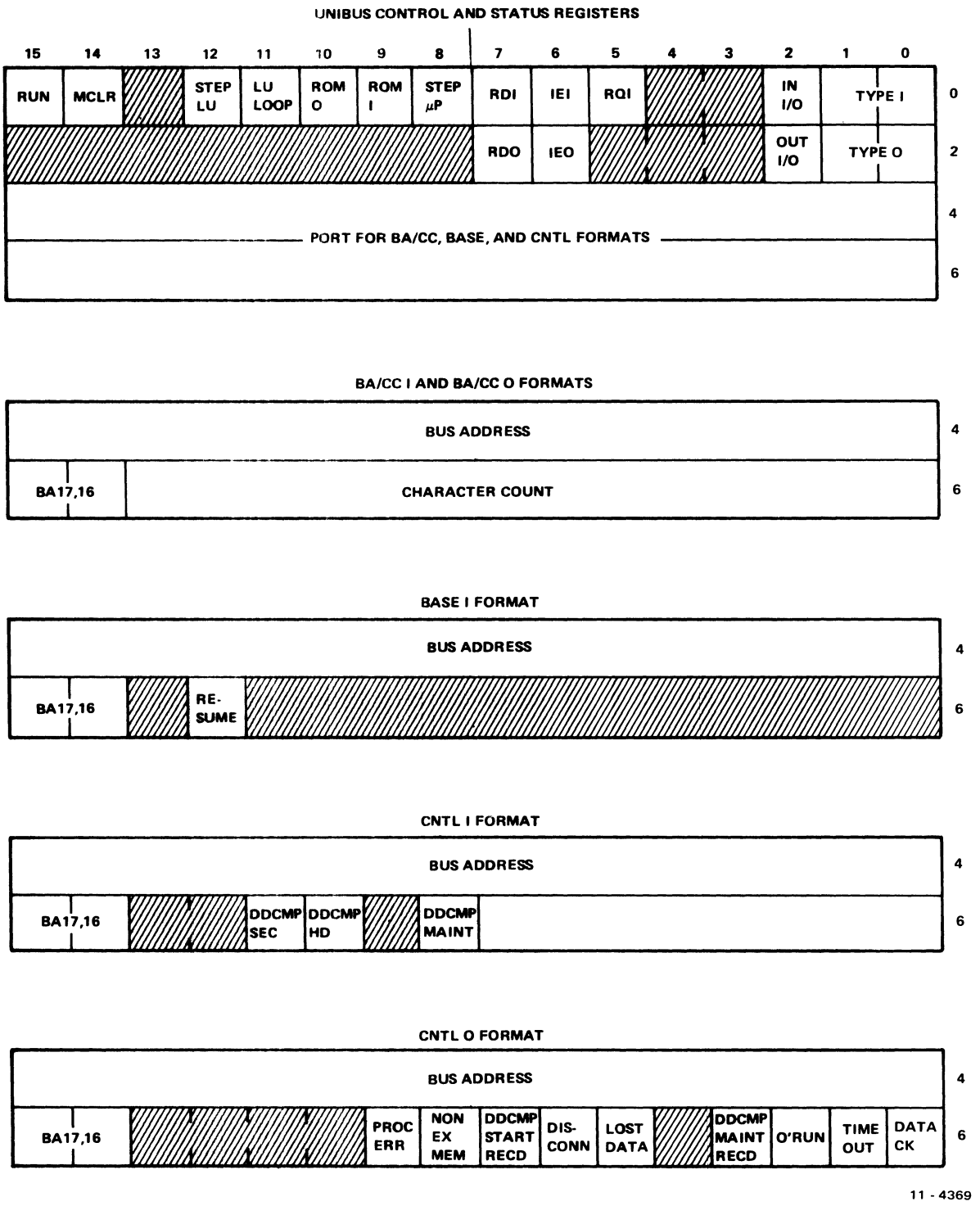


Figure 3-1 Unibus Control and Status Registers

3.4.2.4 BSEL3 - Reserved

3.4.2.5 Data Port Message Formats - The data port is represented by addresses 76XXX4 and 76XXX6. The first half of the port is 76XXX4, which includes BSEL4 and BSEL5. The second half of the port is 76XXX6, which includes BSEL6 and BSEL7.

The port is loaded by the PDP-11 on input transfers and by the microporcessor on output transfers.

The format and contents of the data port depend on the transfer type (TYPE I or TYPE O).

In discussing the data port message formats, it is sometimes more convenient to use word designations (SEL4 and SEL6) than byte designations (BSEL4-7).

There are four formats:

1. Buffer Address/Character Count Input and Output (BA/CC I and BA/CC O) Format

   The formats for BA/CC I and BA/CC O are the same (Figure 3-1). SEL4 contains the least significant 16 bits (0-15) of the 18-bit buffer address. The two most significant bits (16 and 17) of this address are contained in bits 14 and 15 of SEL6. The remaining 14 bits (0-13) of SEL6 contain the character count in positive notation, not 2's complement notation.

Bit	Name	Description
0, 1 (Cont.)	TYPE INPUT (TYPE I) (Cont.)	Each of these transfers is explained in detail. 00 = Buffer Address/Character Count In Utilized with REQUEST IN (RQI). This is a request to the microprocessor by the PDP11 to use the data port (BSEL 4-7) for purposes of transferring an 18-bit bus address and a 14-bit character count to the microprocessor. The character count must be expressed as a positive binary number. 01 = Control In - When used with RQI, requests the use of the data port (BSEL 4-7) from the microprocessor for the purpose of transferring protocol and/or process control information. 10 Reserved 11 Base I - Base In provides a base address which, when used with RQI, requests from the microprocessor the the use of data port (BSEL 4-7) for the purpose of transferring up to an 18-Bit Base Address and RESUME (power fail) bit.

Bit	Name	Description
02	IN I/O	Defines the Flags (BA/CC etc.) for Input (receive) or Output (transmit). For example, if BSEL 4-7 contained a new BA/CC, the microprocessor would need knowledge of whether this was a block to be transferred out, or a buffer for a message to be received.
3, 4	RESERVED	
5	REQUEST IN (RQI)	Set by the PDP-11 to request an input transfer. Cleared by the PDP-11 when the data has been loaded. This bit serves as an interlock bit which is used to request the use of the data port (BSEL 4-7) in order to transfer up to 40 bits of data from the PDP11 program. The RQI bit is accompanied by type of transfer as defined by bits 2:0.
6	INTERRUPT ENABLE INPUT (IEI)	When set, allows the microprocessor to vector interrupts to XX0 having set RDY I.

Bit	Name	Description
7	READY IN (RDY I)	This is a microprocessor response to RQI. When asserted, it indicates to the PDP11 program to proceed with loading the data port (BSEL 4-7). This bit is cleared by the microprocessor at the end of an input transfer.

3.4.2.2 BSEL 1 Maintenance Register

This CSR contains all maintenance functions other than MASTER CLEAR and is not intended for normal user communications between the PDP-11 program and the microprocessor. These functions override all other control functions. All bits are read/write; however, only MASTER CLEAR is functional if BSEL 1 LOCK OUT is set. This register comprises the high byte of address 76XXX0 (Figure 3-1).

Bit	Name	Description
8	STEP MICRO-PROCESSOR (STEP MP)	This bit when set steps the micro-processor through one instruction cycle, composed of five 60 nsec clock pulses. The RUN flip-flop should be cleared before executing this control function.

Bit	Name	Description
9	ROM INPUT (ROM I)	When set, directs the contents of BSEL 6-7 as the next microinstruction to be executed by the microprocessor when STEP MP is asserted.
10	ROM OUTPUT (ROM 0)	When Set, modifies the source paths for BSEL 4-7 to be the contents of the addressed CROM ~~or~~ i.e. the next microinstruction executed when STEP MP is asserted.
11	LINE UNIT LOOP (LU LOOP)	This control function when asserted connects the line units serial line out back to its serial line in. This is done at the TTL level, before level conversion. When the LINE UNIT LOOP bit is set and RUN is cleared, the STEP LU clock is the only clock available for shifting data out or in. When LU LOOP is set and RUN is set data is clocked at a 10 Kbps rate. If the H325 loop back connector is installed at the end of the EIA cable with RUN set and not in LU LOOP mode, data is shifted by a free running clock of approximately 10 Kbps.

Bit	Name	Description
11 (Cont.)	LINE UNIT LOOP (LU LOOP) (Cont.)	The 1 Mbps and 56 Kbps line units require a 12-12528 coaxial adapter installed at the line unit pig-tail cables to provide the loop back. The line unit operates at the clock rate of the integral modem in this case.
12	STEP LINE UNIT (STEP LU)	This control function is used in conjunction with LU LOOP. When asserted, the tranmistter shifts, and when negated, the receiver shifts.
13	RESERVED	
14	MASTER CLEAR	When set, MASTER CLEAR initializes both the microprocessor and the line unit. This bit is self cleaning. The microprocessor clock is enabled and the RUN flip-flop is asserted. The CROM's PC is also temporarily cleared by MASTER CLEAR allowing the microcode to enter the idle state.
15	RUN	RUN controls the microprocessor clock. This bit is set by BUS initialization

Bit	Name	Description
15 (Cont.) (Cont.)	RUN (Cont.)	or MASTER CLEAR which enables the microprocessor clock. RUN can be cleared for maintenance states. A switch (BS1) is provided which prevents RUN from being cleared by a runaway microcode program when the microprocessor malfunctions. Refer to Chapter 2 INSTALLATION for more information concerning the BS1 switch.

3.4.2.3 BSEL 2 Output Register

This register contains control information relative to output transfers from the microprocessor to the PDP11 program. This register comprises the low byte of address 76XXX2 (Figure 3-1).

Bit	Name	Description
0, 1	TYPE OUTPUT (TYPE O)	These bits are encoded for the type of data transfer from the microprocessor to the PDP11 program. 00 = Bus Address and Character Count Out 01 = Control Output 10 = Reserved 11 = Reserved

Bit	Name	Description
2	OUT I/O	OUT I/O defines the Flags (BA/CC etc.) for Input (receive) or Output (transmit). For example, if BSEL4-7 contained a BA/CC, the PDP111program would want to know whether this was a block completed on output or a message received. An Input is indicated when this bit is set and an output is indicated when this bit is cleared.
3-5	RESERVED	
6	INTERRUPT ENABLE OUTPUT (IEO)	When set, the microprocessor, upon asserting RDYO, vectors an interrupt to XX4.
7	READY OUTPUT (RDYO)	This bit, when asserted, indicates that BSEL4-7 contain data as defined by bits 0-2. This bit must be cleared by the PDP11 program after the port data has been sampled.

3.4.2.4 BSEL3 Line Number/Priority Register

If the DMC11 is used as a multiple line controller, this register is used to designate line numbers and to assign priority for block data transfers.

This register comprises the high byte of address 76XXX2 (Figure 3-1).

Bit	Name	Description
8-13	LINE NUMBER	These bits are designated for line numbers during format transfers. The line number bits are required when the DMC11 microprocessor is used as a multiple line controller.
14, 15	PRIORITY	These bits assign priority to blocks of data for transfer via the DMC11 microprocessor when it is used as a multiple line controller. This is especially useful when lines of different speed are used.

3.4.2.5 Data Port Message Formats

The data port is represented by addresses 76XXX4 and 76XXX6. The first half of the port is 76XXX4 which includes BSEL4 and BSEL5. The second half of the port is 76XXX6 which includes BSEL6 and BSEL7.

3.4.2.4 BSEL3 - Reserved

3.4.2.5 Data Port Message Formats - The data port is represented by addresses 76XXX4 and 76XXX6. The first half of the port is 76XXX4, which includes BSEL4 and BSEL5. The second half of the port is 76XXX6, which includes BSEL6 and BSEL7.

The port is loaded by the PDP-11 on input transfers and by the microporcessor on output transfers.

The format and contents of the data port depend on the transfer type (TYPE I or TYPE O).

In discussing the data port message formats, it is sometimes more convenient to use word designations (SEL4 and SEL6) than byte designations (BSEL4-7).

There are four formats:

1. Buffer Address/Character Count Input and Output (BA/CC I and BA/CC O) Format

   The formats for BA/CC I and BA/CC O are the same (Figure 3-1). SEL4 contains the least significant 16 bits (0-15) of the 18-bit buffer address. The two most significant bits (16 and 17) of this address are contained in bits 14 and 15 of SEL6. The remaining 14 bits (0-13) of SEL6 contain the character count in positive notation, not 2's complement notation.

The microprocessor can stack a maximum of seven BA/CCs each for input and output. This number is based on the size of the core tables (BASE) in the PDP-11 memory, which is limited to 256 bytes.

For input operations, BA/CC I supplies new message buffers to the microprocessor.

For output operations, BA/CC O returns the buffers to the PDP-11 that were successfully transferred to the microprocessor.

2. Base Input (BASE I) Format

SEL4 and bits 14 and 15 of SEL6 provide the first address of a reserved block of addresses in the PDP-11 memory (Figure 3-1). The block size is 256 bytes. Upon assigning the BASE address to the microprocessor, the PDP-11 program must not modify any locations within the assigned block.

Bit 12 of SEL6 is called RESUME. If this bit is cleared, the microprocessor initializes the base table and protocol. If set, the microprocessor resumes operation as specified by the contents of the base table.

3. Control Input (CNTL I) Format

The CNTL I format provides a means of implementing certain control functions (Figure 3-1). The control bits are located in SEL6 as shown below.

it	Name	Description
∅-7	Reserved	

8	DDCMP Maintenance (DDCMP MAINT)	With this bit set, the microprocessor enters the DDCMP maintenance mode where it remains until it is subsequently initialized.
9	Reserved	
10	DDCMP Half Duplex (DDCMP HD)	With this bit set, DDCMP half duplex operation is selected. With this bit cleared, DDCMP full duplex operation is selected. This bit must be used with bit 11.
11	DDCMP Secondary (DDCMP SEC)	With this bit set, DDCMP half duplex secondary station operation is selected. With this bit cleared, DDCMP half duplex primary station operation is selected. Not used for full duplex.
12, 13	Reserved	

4. Control Output (CNTL O) Format

The CNTL O format provides a means of informing the PDP-11 program of error conditions involving the DMC11 hardware, PDP-11 program, communications channel, or the remote station.

SEL4 and bits 14 and 15 of SEL6 contain the address of this format. The control bits are located in SEL6 as shown below (Figure 3-1).

Bit	Name	Description
Ø	Data Check (DATA CK)	When set, this bit indicates that a retransmission threshold has been exceeded.
1	Time Out	When set, this bit indicates that the microprocessor has received no response from the remote end of the link for 24 seconds.
2	Overrun (ORUN)	When set, this bit indicates that a message was received but no buffer is available to receive it.
3	DDCMP Maintenance Received (DDCMP MAINT RECD)	When set, this bit indicates that a message in the DDCMP maintenance format has been received and that the device must be reinitialized to enter the maintenance state. The message that caused this bit to be set is lost.
4	Lost Data	When set, this bit indicates that the received message is longer than the supplied buffer. This is a fatal error and the device must be reinitialized.
5	Reserved	

6	Disconnect	When set, this bit indicates that an on-to-off transition of the modem Data Set Ready lead has been detected after the data link has been started.
7	DDCMP Start Received (DDCMP START RECD)	When set, this bit indicates that a DDCMP Start message was received when the protocol was in the running state. This is a fatal error and the device must be initialized following its occurence.
8	Nonexistent Memory (NON EX MEM)	When set, this bit indicates that a Unibus address timeout has occurred. This is a fatal error and the device must be initialized following its occurence.
9	PROCEDURE ERROR (PROC ERR)	When set, this bit indicates that the PDP-11 program has performed a procedural error. This is a fatal error and the device must be initialized following its occurence.

3.4.3 Input Transfers

Whenever the data port is not in use, it is subject to being seized by the microprocessor for use in an output transfer. Therefore, the PDP-11 program must request the microprocessor to assign it the port before proceeding with an input transfer. It must also

specify the type of input transfer (a transmit buffer, a receive buffer, control information, etc.) so the microprocessor can make appropriate preparations.

The PDP-11 program should set bits Ø-2 of BSELØ to indicate the type of transfer and then set bit 5, Request In (RQI), to request the port. These bits may be set by a single instruction. The microprocessor responds by setting bit 7, Ready In (RDYI), when the port has been assigned to the PDP-11 program. When RDYI has been set, the PDP-11 program should load the desired data into the data port (BSEL4-7); then it should clear RQI. The microprocessor takes the data and clears RDYI, which completes the transfer.

Bit 6 of BSELØ, Interrupt Enable Input (IEI), controls whether the PDP-11 program receives an interrupt (to Vector XXØ) when the microprocessor has set RDYI. It is most efficient for the PDP-11 program to have interrupts disabled and simply scan RDYI one or more times until the microprocessor has set it. While the PDP-11 program is waiting, it must be prepared to accept an output transfer because the microprocessor may have seized the port in the meanwhile.

The microprocessor cannot service certain types of input transfers immediately. In these cases, it is convenient to use interrupts. If the PDP-11 program finds RDYI clear after several scans, it can enable interrupts by setting IEI with a BIS or MOV instruction. The PDP-11 should ensure that IEI was successfully set following the setting of IEI while waiting for RDYI. If the PDP-11 was unsuccessful, it should try again. The DMC11 interrupts the PDP-11

(to Vector XXØ) when the microprocessor has set RDYI. The PDP-11 program gets the interrupt in all cases, even if the microprocessor had already set RDYI at the time the program sets IEI. The program can bypass any scanning if IEI is set when the program sets RQI. The PDP-11 program may clear IEI at any time other than when awaiting RDYI.

NOTE

The PDP-11 program should not begin a new input transfer until the previous transfer has been completed, as indicated by the microprocessor clearing RDYI. If the PDP-11 program wishes to begin a new transfer immediately, it should check that RDYI has been cleared before setting RQI. This can be done by scanning RDYI until it has been cleared.

The PDP-11 program must not attempt to queue more than seven buffers for transmission or reception, as data integrity may be lost.

3.4.4 Output Transfers

The microprocessor initiates an output transfer when it has status or error information to transfer to the PDP-11 program or it wishes to return a full buffer on reception or an empty buffer on transmission. The microprocessor can initiate an output

transfer any time the data port is free; that is, not assigned to the PEP-11 program for an input transfer and not in use for a previous out-t transfer. However, if the PDP-11 has initialized the DMC11 by setting MASTER CLEAR or generating the INIT signal on the Unibus, the microprocessor does not generate any output transfer until it has been initialized by the PDP-11 program.

The microprocessor loads status or error information into the data port (BSEL4-7) and sets bits Ø-2 of BSEL2 to indicate the format and significance of the data. It then sets bit 7 of BSEL2, Ready Out (RDYO), to indicate to the PDP-11 programs that data is available. In response to RDYO setting, ıe PDP-11 program should note the type of output transfer as specified in bits Ø-2 of BSEL2 and read the data in the data port. When the PDP-11 program has sampled all the data, it must complete the output transfer by clearing RDYO. This frees the data port for a subsequent transaction.

the PDP-11 program wishes, it can enable interrupts on output transfers by setting bit 6 of BSEL2, Interrupt Enable Output (IEO). If IEO is set, the DMC11 interrupts the PDP-11 (to Vector XX4) after the microprocessor has set RDYO. Since the PDP-11 program usually does not know when an output transfer will occur (for example, when a message will be received), ın efficient PDP-11 program ordinarily enables interrupts on output transfers

NOTE

The PDP-11 program must respond to RDYO being set by reading the data and clearing RDYO. Failure to do this prevents the data port from being freed. If the PDP-11

program has requested an input transfer by setting RQI, it must be prepared to respond to an output transfer prior to being given RDYI. If the PDP-11 program fails to respond to RDYO, it never gets RDYI. The PDP-11 program should not spin on RDYI in a loop that does not also test RDYO unless interrupts on output transfers are enabled, and the loop executes at a lower priority level than the DMC11 interrupt level.

3.4.5 Initialization

The powerup sequence and Unibus INIT signal initialize the DMC11. The PDP-11 program can achieve the same effect by setting MASTER CLEAR in BSEL1. Each of these procecures restarts the microprocessor to the beginning of its microprogram. In this state, the microprocessor does not send or receive messages on the serial line or generate output transfers.

The PDP-11 program should not access the CSRs for 2 us following MASTER CLEAR.

When the PDP-11 program wishes the DMC11 to function, it must perform an input transfer that specifies the base address of a 128-word table in PDP-11 memory, which is called the base table. The PDP-11 program requests the BASEI transfer by setting TYPEI to 11. In response to RDYI, the program loads the low-order 16

bits of the address into SEL4 and the high-order 2 bits of the address into bits 15 and 14 of SEL6. If the DDCMP protocol operation is to be initialized, the RESUME bit (bit 12 of SEL6) must be clear.

Once the PDP-11 has specified a base address, the 128-word base table belongs to the microprocessor until the DMC11 is master cleared by INIT or MASTER CLEAR. The PDP-11 program may examine the contents of the base table (for example, error counters relating to protocol operation) but must not alter its contents.

By supplying a base address with the RESUME bit clear, the microprocessor is conditioned to enter the DDCMP start-up state.

The PDP-11 program must perform an input transfer, using the Control In format by setting the Half Duplex bit (HD) in SEL6 (bit 10) if the channel is half duplex or by leaving this bit clear if the channel is full duplex. In addition, the program must specify whether the DMC11 is to operate as a half duplex secondary station (long timer) or a half duplex primary station (short timer) by setting or clearing the Secondary bit (SEC) in SEL6 (bit 11). A half duplex link should have one primary station and one secondary station. The only difference between the two is in the length of time spent before retransmitting start sequences. Half duplex operation may be specified at any time by a Control In transfer to accommodate switching to a half duplex backup communications channel. The DMC11 options containing the integral modem must be

specifically strapped for half duplex when using single cable operation in addition to requiring the Control In transfer.

3.4.6 DDCMP Start-Up

Before data messages may be transmitted or received, the DDCMP start-up sequence must be completed to make certain both ends of the link are correctly initialized and to place the protocol in the running state. The start-up procedure will be initiated within one timer interval following the assignment of the BASE.

The PDP-11 program may ignore the details of the start sequence. However, one property of the sequence is significant. Once the local DMC11 has entered the running state, it detects and flags as an error the fact that the other end has initiated the start sequence. As a result, the PDP-11 program receives a Control Out transfer with SEL6 bit 7 (DDCMP START RECD) set. If this happens, the PDP-11 program knows that the other end of the link has restarted. The PDP-11 program should initialize the DMC11 and begin again.

3.4.7 Data Transmission

When the PDP-11 program wishes to transmit a buffer of data, it clears bits 1 and Ø of BSELØ to indicate a Buffer Address/Character Count In transfer and clears bit 2 of BSELØ (IN I/O) to specify that this is a full buffer to be transmitted. It then requests an input transfer by setting RQI. In response to RDYI, it loads SEL4 with the low-order 16 bits of the buffer address, bits 15 and 14 of SEL6 with the high-order bits of the address,

and bits 13-0 of SEL6 with the 14-bit character count. Buffers from 1 to 16,383 bytes long may be used for local operation. For remote operation, buffers should be limited to a practical maximum of about 512 bytes, depending on the error rate of the communications facilites. Each buffer corresponds to a single DDCMP data message.

When the message has been successfully transmitted and an acknowledgement received, the microprocessor initiates an output transfer with bits 1 and Ø of BSEL2 clear to indicate the Buffer Address/Character Count Out (BA/CC O) format. Bit 2 (OUT I/O) is clear to indicate that a successfully transmitted buffer has been returned to the program.

The PDP-11 program may queue up to seven buffers for transmission by supplying buffers to the microprocessor faster than it returns them.

NOTE

The PDP-11 program must not request an input transfer that supplies a transmit buffer if seven are already outstanding, as data integrity may be lost.

3.4.8 Data Reception

When the PDP-11 program has an empty buffer it wishes to fill with received data, it clears bits 1 and Ø of BSELØ to indicate a BA/CC I transfer and sets bit 2 of BSELØ (IN I/O) to specify that an empty buffer has been made available for reception. It

then requests an input transfer by setting RQI. In response to RDYI, it loads SEL4 and SEL6 with the buffer address and character count in the same format as for transmission. The character count must be large enough to accommodate the longest message expected.

When a message has been successfully received and stored in the buffer, the microprocessor initiates an output transfer with bits 1 and Ø of BSEL2 clear to indicate the BA/CC 0 format. Bit 2 (OUT I/O) is set to indicate that a buffer has been received. SEL4 and SEL6 contain the address of the buffer and the actual number of characters received.

If a message is received when no receive buffer is available, the microprocessor informs the PDP-11 by means of a Control Out transfer with bit 2 of SEL6 (ORUN) set. The other end of the link is informed of the error and automatically retransmits the message. The PDP-11 program should supply a buffer as soon as possible.

The PDP-11 may queue up to seven empty buffers for reception by supplying them to the microprocessor faster than it returns buffers.

NOTE

The PDP-11 program must not request an input transfer that supplies a buffer for reception if seven are already outstanding, or data integrity may be lost.

3.4.9 Control Out Transfers

The microprocessor informs the PDP-11 program of unusual or error conditions involving the communications channel, remote end of the link, DMC11 hardware, or PDP-11 program by means of an output transfer with bit 1 of BSEL2 clear and bit Ø set, indicating a Control Out (CNTL O) transfer. SEL6 contains bits that indicate the error condition. Some errors are advisory in nature and normal operation may continue. Others are fatal and require the PDP-11 program to initialize the DMC11.

Bit Ø (DATA CK) indicates that a retransmission threshold has been exceeded (more than eight consecutive retransmissions have occurred for transmission or reception). This indicates a defective communications channel or that the other end of the link has failed to supply a buffer for reception. The PDP-11 can examine error counters in the base table for more details of the error. This is a non-fatal error. When the cause of the error is corrected, normal operation continues with no messages lost in either direction. This error may appear repeatedly until the condition is corrected or until the DMC11 is initialized. Transient errors corrected before eight retransmissions are not reported to the PDP-11 program but are counted in the base table.

Bit 1 (TIME OUT) indicates that the microprocessor has received no response from the remote end of the link for a specified period (24 seconds). This indicates a broken communications channel or a failure at the other end of the link (possibly a power failure). Like DATA CK, this is a non-fatal error which can occur repeatedly.

Bit 2 (ORUN) indicates that a message was received but no buffer was available. This is a non-fatal error. The PDP-11 program can prevent this error from recurring repeatedly by supplying a buffer.

Bit 3 (DDCMP MAINT RECD) indicates that a message in the DDCMP maintenance format was received. The message causing the contition was lost, and the PDP-11 must reinitialize the DMC11 to enter the maintenance state. This is a fatal error.

Bit 4 (LOST DATA) indicates that a message was received that is longer than the buffer supplied by the PDP-11 program. This is a fatal error.

Bit 6 (DISCONNECT) indicates that an on-to-off transition of the modem Data Set Ready lead has been detected (remote operation only). This is a non-fatal error. For dial-up operation, the PDP-11 program must consider the possibility that a new caller has connected to the DMC11, if this is required by security considerations.

Bit 7 (DDCMP START RECD) indicates that a DDCMP Start message was received when the protocol was in the running state. This indicates that the remote computer has initialized its end of the link. This is a fatal error. The PDP-11 program should initialize the DMC11 if it wishes to start over and complete the start-up sequence.

Bit 8 (NON EX MEM) indicates that a Unibus address timeout has occurred. This could have been caused by the PDP-11 program

specifying an invalid base address, buffer address, or count that was stored illegally in the base table or that by a defective PDP-11 memory. This is a fatal error.

Bit 9 (PROC ERR) indicates a procedure error on the part of the PDP-11 program. The requested input transfer cannot be honored due to a programming error. This error can be caused by requesting a BA/CC before supplying a base address, requesting a base address a second time, or specifying an invalid code in BSELØ bits 1 and Ø. This is a fatal error. The PDP-11 program may create this condition as a means of shutting down the DMC11 in an orderly manner (see Paragraph 3.4.13). Data Terminal Ready will be cleared as a result of this error condition.

3.4.10 Maintenance Messages

A special DDCMP message format, the maintenance message, is used for down-line loading, restarting, or otherwise maintaining satellite computer systems. Messages in this format are subject to error checking but are unsequenced, unacknowledged, and not retransmitted automatically by the DMC11. Transmission is always half duplex.

Maintenance messages can only be sent and received while the microprocessor is in the DDCMP maintenance state. The PDP-11 program may cause the microprocessor to enter this state by a CNTL I transfer with bit 8 of SEL6 (DDCMP MAINT) set.

If a maintenance message is received while in the running state, the microprocessor performs a CNTL O transfer with DDCMP MAINT RECD set in

SEL6. The PDP-11 program must then initialize the device to the maintenance state to transfer messages in maintenance format.

Once in DDCMP maintenance mode, maintenance messages can be sent and received similarly to data messages. On transmission, the data portion of the message is taken from the buffer with the DMC11 generating the header and CRCs. On reception only, the data portion is placed in the buffer. Messages not in DDCMP maintenance format or having incorrect CRCs are simply discarded.

The data portion of the maintenance message may contain any data that is desired, but ordinarily it conforms to the Digital Maintenance Operation Protocol (MOP) formats. When operating in conformance with MOP, the DMC11 must be operated in a single buffered manner, causing a line turn-around after each message transmitted. When a host computer wishes to restart a satellite computer system, it must send the appropriate MOP messages as described below.

In order to leave maintenance mode, the PDP-11 program must initialize the DMC11 and supply a base address with the RESUME bit clear.

3.4.11 Remote Load Detect

Whenever the microprocessor is running, it is constantly scanning the serial line for a DDCMP maintenance message containing an ENTER MOP MODE data field. What happens when this particular message is received depends on the setting of two switch packs on the DMC11 line unit. Depending on the setting of these switches, the DMC11 will either trigger the PDP-11 to begin executing a program in a read-

only memory (ROM) bootstrap (DM873, M93Ø1, etc.) or simply pass the data to the PDP-11 as an ordinary maintenance message. In case a ROM bootstrap is triggered, switches on the line unit specify an 8-bit word offset to the bootstrap address space.

The data portion of the ENTER MOP MODE message is 5 bytes long. The first byte contains the decimal number 6. The remaining 4 bytes contain the same 8-bit value. This value is specified by a switch pack on the DMC11 line unit and serves as a password to protect against inadvertent recognition of the ENTER MOP MODE message. ENTER MOP MODE messages with an invalid password are discarded if the switch settings specify remote load defect.

3.4.12 Power Fail Recovery

The DMC11 keeps all data necessary to attempt recovery from a power failure in its base table. When the PDP-11 program detects a power failure, it should cease requesting input transfers and create a procedure error by specifying an invalid code in BSELØ bits 1 and Ø. At this point, the DMC11 will cease to send and receive messages already sent and acknowledged or received, until the procedure error code appears in a CNTL O transfer. When power has been restored, the PDP-11 power recovery program can tell the DMC11 microprocessor to recover from the error by performing a BASE I transfer with the RESUME bit set. The original base address must be specified and the contents of the base table must be the same as they were when power was lost; otherwise, the program must start over (RESUME bit clear). If the base table is within MOS or bipolar memory (without battery

backup), recovery will not be successful since the base table will have been lost. If the PDP-11 processor is a PDP-11/35, 11/4Ø, 11/45, 11/5Ø, 11/55, or 11/7Ø, DMC11 power fail recovery may be accompanied by data loss, and the software should be designed to reinitialize the DMC11 using software-maintained information about transmit and receive messages pending.

3.4.13 Shutdown of the DMC11

The PDP-11 program may shut down the DMC11 by creating a procedure error by specifying an invalid code in BSELØ bits 1 and Ø. The PDP-11 program should process output transfers for messages already sent and acknowledged or received until the procedure error code appears in a CNTL O transfer.

3.4.14 Data Set Control

The microprocessor maintains Data Terminal Ready continuously, dropping it following an on-to-off transition of Data Set Ready, or as a result of a procedure error (PROC ERR). Data Terminal Ready will be reasserted when the device is master cleared. An on-to-off transition of Data Set Ready provides a CNTL O transfer as described above, if the DMC11 has been given a base address.

3.4.15 Cumulative Error Counts

In order to help localize component failures in the communications channel, the DMC11 provides a record of each recoverable communications error it encounters. Eight bit counters for these errors are provided within the base table. The base table is updated periodically to provide these counters. The format of these counters is detailed in Table 3-1.

3.4.16 Optimizing Performance of the DMC11

The DMC11 implements the DDCMP protocol, which imposes a fixed overhead of ten characters on each data message and requires a synchronization sequence whenever the line has gone idle. Optimal performance will be approached when the message sizes approach the maximum that may be transmitted without error, the DMC11 is provided with maximal numbers of buffers, and message transfer is bidirectional. Applications using very small messages yield poor link efficiency. Applications using very large messages may yield poor link efficiency as a result of line error rates.

Table 3-1 Cumulative Error Counters

Location	Condition
BASE+3	NAKS Recd -- No Buffer Available
BASE+4	NAKS Recd -- Bad Header BCC
BASE+5	NAKS Recd -- Bad Data BCC
BASE+6	NAKS Sent -- No Buffer Available
BASE+7	NAKS Sent -- Bad Header BCC
BASE+10	NAKS Sent -- Bad Data BCC
BASE+11	REPS Sent
BASE+12	REPS Recd

Once this message has been successfully received, the DMC11 starts the PDP-11 program at the specified transfer address. The DMC11 must be initialized before it does anything else except recognize a subsequent ENTER MOP MODE maintenance message.

3.4.12 Power Fail Recovery

The DMC11 keeps all data necessary to recover from a power failure in its base table. When the PDP-11 program detects a power failure, it should cease requesting input transfers and not respond to output transfers. When power has been restored, the PDP-11 power recovery program can tell the DMC11 microprocessor to recover from the error by performing a BASE I transfer with the RESUME bit set. The original base address must be specified and the contents of the base table must be the same as they were when power was lost; otherwise, the program must start over. (RESUME bit clear). As part of the power recovery, the PDP-11 program must repeat an uncompleted input transfer. It must set IEI and IEO as desired. The microprocessor repeats an uncompleted output transfer.

3.4.13 Data Set Control

If the switches on the DMC11 line unit specify bootstrap ROM triggering or down-line loading, the microprocessor maintains Data Terminal Ready continuously, dropping it for a one second period following an on to off transition of Data Set Ready. Otherwise, the DMC11 does not turn Data Terminal Ready on until it has received a base address. It drops Data Terminal Ready

when initialized by INIT or MASTER CLEAR and it drops it for one second following an on to off transition of Data Set Ready. An on to off transition of Data Set Ready provides a CNTL O transfer as described above, if the DMC11 has been given a base address.

3.5 MICROPROCESSOR CONTROL AND STATUS REGISTERS

3.5.1 Introduction

The Unibus Control and Status REgisters described in paragraph 3.4.2 are physically located in the multiport RAM. The RAM capacity is 128 bits arranged as 16 8-bit bytes, which is equivalent to 8 16-bit words. The RAM can be accessed simultaneously from two sources. One source is the Unibus and the other is the microprocessor. Therefore, when these Unibus CSRS (BSEL1-BSEL7) are viewed from the microprocessor, they are called Microprocessor Control and Status Registers. Specifically, they are identified as OUTBUS*/INBUS* registers 0-7 (octal).

The remaining multiport RAM capacity, which is 8 8-bit bytes, contains the NPR Data and BA registers. These registers are also called Microprocessor CSRs and are specified as OUT BUS/IN BUS registers 0-7 (octal).

There are two additional byte sized hardware registers that are listed in the OUT BUS*/IN BUS* category. They are the NPR Control Register (10_8) and the Microprocessor Miscellaneous Register (11_8).

The microprocessor has the capability of addressing 32 byte sized registers. As a convention, it has been decided to show 16 assigned addresses under each category; that is, OUT BUS*/IN BUS* and OUT BUS/IN BUS. As a result, six undefined registers 12-17 (octal) are listed under OUT BUS*/IN BUS*. These registers do not exist physically. The line unit device registers, 10_8-17_8 have been added to the OUT BUS/IN BUS category. These registers are physically located in the line unit. Address 10_8 is listed twice because two line unit register use the same address. The In Data Silo is read only and the Out Data Silo is write only. Therefore, there are nine registers in the line unit.

The arrangement of the Microprocessor CSRs is shown in Figure 3-2.

The detailed discussion of the Line Unit CSRs is contained in paragraph 3.6.

3.5.2 OUT BUS*/IN BUS* Registers 0-7

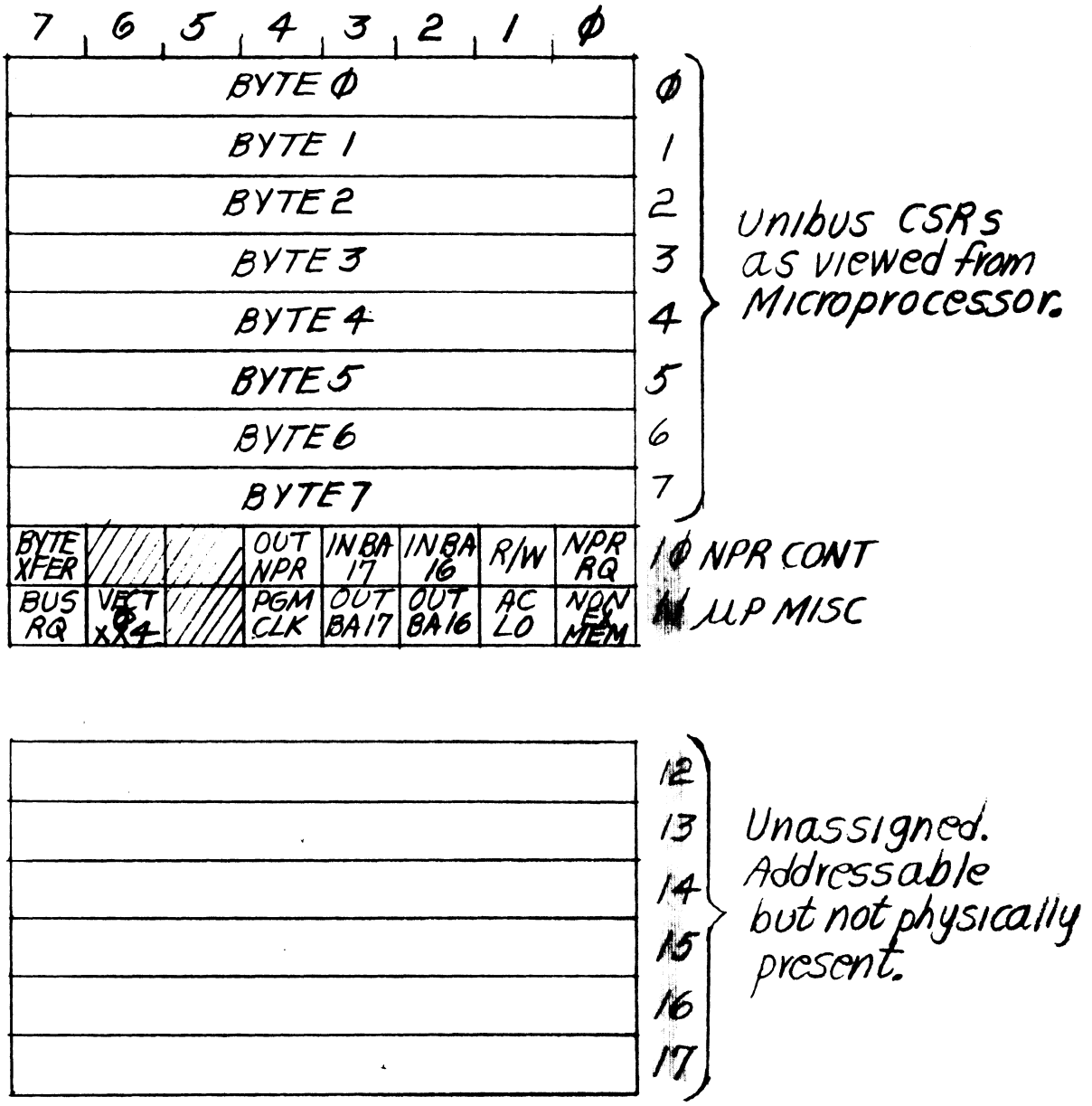
These eight registers are identical to those described in paragraphs 3.4.2.1 through 3.4.2.5.

3.5.3 NPR Control Register (OUT BUS*/IN BUS* 10)

Bit	Name	Description
0	NPR REQUEST (NPR RQ)	This bit can be set only. It is automatically cleared by the hardware

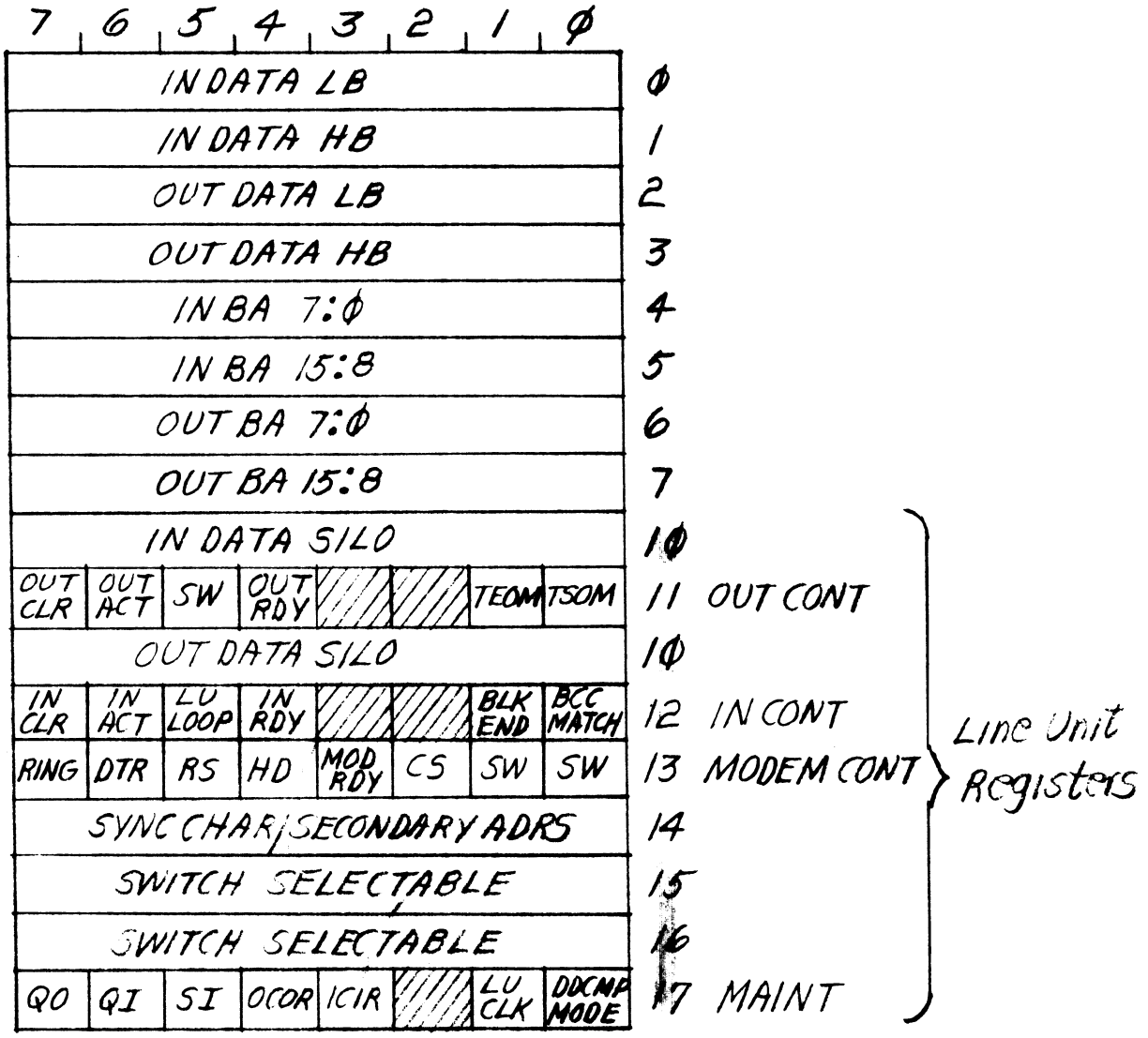
MULTIPORT RAM

INTERNAL DMC11 REGISTERS ONLY



16 Registers Assigned to OUTBUS*/INBUS* Category

Figure 3-2 Microprocessor Registers



16 Registers Assigned to OUTBUS/INBUS Category

Figure 3-2 Microprocessor Registers

Bit	Name	Description
0 (Cont.)	NPR REQUEST (Cont.)	when the NPR has been completed. When set, this bit requests an NPR via the Unibus to the PDP-11 memory. If OUT NPR (bit 4) is cleared, data is transferred from the PDP-11 memory. If OUT NPR is set, data is transferred to the PDP-11 memory. Bit 7 (BYTE XFER) controls word/byte selection. For an IN NPR, the PDP-11 memory address is in OUT BUS/IN BUS registers 4 and 5. For an OUT NPR, the address is in OUT BUS/IN BUS registers 6 and 7. The data that is associated with the transaction comes from OUT BUS/IN BUS registers 2 and 3 for OUT DATA and from OUT BUS/IN BUS registers 0 and 1 for OUT NPR (bit 4) is Unibus Control line C1 and BYTE XFER (bit 7) is Unibus Control line C0. When BYTE XFER is set, the state of the BA least significant bit (0) is used to select the byte. The truth table for the type of

Bit	Name	Description
0 (Cont.)	NPR REQUEST (NPR RQ) (Cont.)	transaction, as selected by these bits, is shown below.

OUT NPR (C1)	BYTE XFER (C0)	BA0	UNIBUS TRANSACTION
0	0	0	DATI
0	0	1	DATI
0	1	0	Illegal
0	1	1	Illegal
1	0	0	DATO
1	0	1	DATO
1	1	0	DATOB (Low Byte)
1	1	1	DATOB (High Byte)

1	READ/WRITE (R/W)	This read/write bit provides no function and may be treated in the microcode as a flag or state indicator.
2, 3	IN BA 16 and IN BA 17	These are the PDP-11 memory extension bits used during an IN NPR (C1 = 0) transaction.

Bit	Name	Description
4	OUT NPR	This bit is used in association with NPR RQ (bit 0). The details of the inter-relationship between these bits are covered in the description of NPR RQ (bit 0).
5, 6	RESERVED	
7	BYTE XFER	This bit is used in association with OUT NPR to indicate a byte transfer to the PDP-11 memory. When this bit is set, the PDP-11 uses address bit A0 for byte selection. If A0 is a 0, OUT DATA 7-0 is stored in the low byte of the PDP-11 memory. If A0 is a 1, OUT DATA 7-0 is stored in the high byte of the PDP-11 memory. If BYTE is cleared during an OUT NPR operation, OUT DATA 15-0 is transferred to the PDP-11 memory as a word.

3.5.4 Microprocessor Miscellaneous Register (OUT BUS*/IN BUS* 11)

Bit	Name	Description
0	NON-EXISTENT MEMORY (NON-EX MEM)	During an NPR, this bit is set approximately 20μs after a non-existent memory location is addressed by the microprocessor. At this time, the NPR logic releases the Unibus.
1	AC LOW	This bit is a set only bit. When set, it triggers a 1-shot with a pulse duration of 0.5s. This pulse goes to the Unibus and initiates a power fail recovery procedure in the PDP-11 Processor.
2, 3	OUT BA 16 and OUT BA 17	These are the PDP-11 memory extension bits used during an OUT NPR transfer.
4	PROGRAM CLOCK (PGM CLK)	This bit acts as a timer for the microprocessor. It can be read to determine lapse time for time out, flag testing, etc.
		This bit is the 0 output of a re-triggerable 1-shot with a 1s pulse

Bit	Name	Description
4 (Cont.)	PROGRAM CLOCK (PGM CLK) (Cont.)	duration. As long as the triggering pulses come along at less than 1 second intervals, the 1-shot remains asserted and this bit is read as a 0. If the 1-shot times out, this bit is read as a 1.
5	RESERVED	
6	VECTOR AT XX4	If this bit is set when BR RQ (bit 7) is set, vector address XX4 is generated. If it is cleared when BR RQ is set, vector address XX0 is generated. Address XX0 is associated with RDYI and address XX4 is associated with RDYØ.
7	BR REQUEST (BR RQ)	When set, this bit initiates a Bus Request via the Unibus at BR level 4, 5, 6, or 7. The microprocessor is shipped with a BR5 priority card installed. This bit can be set only and is cleared by the hardware after the BR has been completed.

3.5.5 NPR Bus Address and Data Registers (OUT BUS/IN BUS 0-7)

Register	Name	Description
0, 1	IN DATA	Low byte (register 0) and high byte (register 1) of data to be transferred from the PDP-11 memory.
2, 3	OUT DATA	Low byte (register 2) and high byte (register 3) of data to be transferred to the PDP-11 memory.
4, 5	IN BA	Contains BUS Address (BA) bits 0-16 during an NPR transfer from the PDP-11 memory. Bit 0 of register 4 is BA bit 0 and bit 7 of register 5 is BA bit 16.
6, 7	OUT BA	Contains Bus Address (BA) bits 0-16 during an NPR transfer to the PDP-11 memory. Bit 0 of register 6 is BA bit 0 and bit 7 of register 7 is BA bit 16.

3.6 LINE UNIT REGISTERS

3.6.1 In/Out Data Silo Registers (10)

The In Data Silo is loaded with 8 bits of received data from the Receiver Data Register. When the microprocessor performs a read operation on this register, the data is presented to the IBUS.

Physically, the In Data Silo is in the form of a 64 word by 12 bit silo. The other four bits considered to be part of the In Control Register.

When the microprocessor performs a write operation on the In Data Silo, nothing happens to this register. However, the 8 bits of data to be transmitted is taken from the OBUS and is presented to the input of the Out Data Silo, which is a 64 word by 12 bit silo. The other four bits are considered to be part of the Out Control Register.

3.6.2 Out Control Register (11)

Bit	Name	Description
0	TSOM (Transmit Start of Message)	This bit is used to initiate the start of a new message. DDCMP Mode: The Sync character must be loaded into the Out Data Silo along with TSOM bit. This character is transmitted as the Sync character until

Bit	Name	Description
0 (Cont.)	TSOM (Transmit Start of Message) (Cont.)	TSOM is cleared. Until it is cleared, the characters are not included in the CRC accumulation. When TSOM is cleared, the present Sync character is transmitted and is followed by data. All data is included in the CRC accumulation, if CRC is enabled. Once TSOM has been set, the CRC accumulation cannot be inhibited unless the line unit is initialized. Bit Stuff Mode: When TSOM is set, a flag character is automatically transmitted. The character that is loaded with the TSOM bit is lost. Flag characters are automatically transmitted as long as TSOM is set. When data is to be transmitted, TSOM is cleared and data is loaded into the Out Data Silo. At the completion of the current flag character, the actual transmission of data begins. All information to be transmitted is included in the CRC accumulation, if the CRC function is enabled.

Bit	Name	Description
0 (Cont.)	TSOM (Transmit Start of Message) (Cont.)	This bit is program write only. It is cleared by the initialization logic and by the fact that data was loaded into the Out Data Silo. It is loaded into the Silo and passed to the transmitter through the Silo.
1	TEOM (Transmit End of Message)	This bit is used to terminate the message in progress and control the transmission of the CRC character, if the CRC function is enabled. DDCMP Mode: When TEOM is set, the CRC character is transmitted. If no more messages are pending (TSOM cleared), the transmitter is shut down. Bit Stuff Mode: When TEOM is set, the character loaded with it is lost. The CRC character is transmitted. If no more messages are pending, the transmitter is shut down by having a second TEOM in the silo. This generates a single closing or intermessage flag.

Bit	Name	Description
1 (cont.)	TEOM (Transmit End of Message) (Cont.)	This bit is program write only. It is cleared by the initialization logic and by the TSIP flip-flop which is set whenever data is loaded into the Out Data Silo.
2 and 3	Reserved	These bits are program write only. They are cleared by the initialization logic and by the TSIP flip-flop which is set whenever data is loaded into the Out Data Silo. These bits and bits 0 and 1 are passed to the transmitter through the silo everytime register 10 is written into; therefore, if the CONTROL IN format is to be sent, these bits must be written before register 10 is written into.
4	OUT RDY (Out Ready)	When asserted, this bit informs the microprocessor that the transmitter is ready to accept data. It indicates that space is available in the Out Data Silo. The microprocessor loads the Out Data Silo and then reads OUT RDY. The speed of the microprocessor allows OUT RDY to be read and interpreted as true

Bit	Name	Description
4 (Cont.)	OUT RDY (Cont.) (Out Ready)	before the silo has loaded the data. Therefore, one cycle must elapse between loading the silo and reading OUT RDY. This bit is read only.
5	Reserved	Read only. Physically, this bit is a switch.
6	OUT ACTIVE	OUT ACTIVE informs the microprocessor of the status of the transmitter. When it is set, the transmitter is active. This bit is read only. It is set by the hardware and cleared by the initialization logic.
7	OCLRP (OUT CLEAR)	This bit is used to clear all the transmitted functions. OCLRP is program write only.

3.6.3 In Control Register (12)

Bit	Name	Description
0	BBC MATCH (Block Check Character Match)	BBC MATCH is the output of the receiver CRC error logic that monitors the contents of the CRC register. With

Bit	Name	Description
0 (Cont.)	BBC MATCH (Cont.) (Block Check Character Match)	the CRC function enabled, BBC MATCH is asserted at the end of an errorless message. In the DDCMP protocol, the contents of the Receiver CRC Register equals zero when an errorless message has been received. In the SDLC protocol, the contents of the Receiver CRC Register equal 016417. This bit is read only and is updated everytime register 10 is read.
1	BLOCK END	BLOCK END is used to inform the microprocessor, in SDLC mode, that a terminating flag has been received. This flag may be the leading flag for the next message. The BLOCK END bit is loaded with the high byte of the CRC character; therefore, the BLOCK END bit along with the BCC MATCH bit should be used to indicate reception of a good message. This bit is read only and is not used in the DDCMP mode. It is updated every-time register 10 is read.

Bit	Name	Description
2 and 3	Reserved	When asserted, this bit informs the microprocessor that received data is ready for processing. It indicates that data is available at the output of the In Data Silo. This bit is read only.
5	ALT LU LOOP (Alternate Line Unit Loop)	During maintenance, this bit is set to loop the receiver on the transmitter with no connection to the modem control lines. This bit is program read/write.
6	IN ACTIVE	When asserted, this bit informs the microprocessor that the receiver is in the data reception mode; that is, it is receiving data or CRC characters. DDCMP Mode: IN ACTIVE is asserted upon receipt of the first non-sync character. SDLC Mode: IN ACTIVE is asserted upon receipt of the first data character.

Bit	Name	Description
7	ICLRP (In Clear)	This bit is used to clear all the receiver functions. ICLRP is program write only.

3.6.4 Modem Control Register (13)

Bit	Name	Description
0	SECURE	The function of this bit is reserved for future use. This read only bit is selected by a switch. SECURE is asserted when the switch is OFF (open).
1	SW	The function of this bit is reserved for future use. This read only bit is selected by a switch. SW is asserted when the switch if OFF (open).
2	CS (Clear to Send)	The CS bit informs the microprocessor of the state of the modem Clear to Send line. This bit and MODEM RDY (bit 3) must be asserted simulteneously to generate SEND which is the transmitter enabling signal. This bit is read only.

Bit	Name	Description
3	MODEM RDY (Modem Ready)	The MODEM RDY bit informs the microprocessor of the state of the Modem Ready line. On the M8201 Line Unit, this signal can be held asserted permanently through the use of a jumper. On the M8202 Line Unit, this signal is asserted when power is turned on. This bit is read only.
4	HDX (Half Duplex)	The HDX bit is used to put the line unit in the half-duplex mode. When this bit and the Request to Send bit are asserted, the receiver clock is inhibited which blinds the receiver during operation in the half-duplex mode. This bit is program read/write and can be directly cleared by the clear signal from the microprocessor.
5	RS (Request to Send)	The RS bit informs the microprocessor of the state of the modem Request to Send line. This bit is controlled by the line unit logic and not by the

Bit	Name	Description
5 (Cont.)	RS (Cont.) (Request to Send)	microprocessor. It is cleared by absence of data or by the initialization logic. This bit is read only.
6	DTR (Data Terminal Ready)	The DTR bit enables the modem via the Data Terminal Ready line. This bit is program read/write. It is directly set by the initialization logic but it can be cleared only by writing a 0 into it.
7	RING	The RING bit informs the microprocessor of the state of the modem Ring line. RING is inhibited on the M8202 Line Unit. This bit is read only.

3.6.5 Sync Register (14)

The Sync Register is an 8-bit program read/write register.

DDCMP Mode: The register is loaded with a program selectable sync character.

Bit Stuff: In the secondary mode, this register is loaded with secondary station address. This 8 bit character follows the initial flag in the SDLC message format.

3.6.6 Switch Selectable Registers (15 and 16)

Both of these registers are DIPs containing eight switches each. The program determines the function of both registers.

3.6.7 Maintenance Register (17)

Bit	Name	Description
0	MODE	The MODE bit selects the protocol (DDCMP or Bit Stuff families). When set DDCMP is selected; when cleared, Bit Stuff is selected. During initialization, the CLEAR signal from the microprocessor sets this bit to select DDCMP. This bit can be cleared (SDLC selected) only by writing a 0 into it. This bit is read/write.
1	ECS (Internal Clock)	ECS is the output of the internal RC clock (approximately 10 KHz). This bit is read only.

Bit	Name	Description
2	Reserved	Read only.
3	ICIR (In Composite Input Ready)	When asserted, this bit indicates that the In Data Silo is ready to accept data. This bit is read only.
4	OCOR (Out Composite Output Ready)	When asserted, this bit indicates that data is ready at the output of the Out Data Silo. This bit is read only.
5	SI (Serial Input)	SI is the serial input data from the modem. This bit is read only.
6	QI (Quotient In)	QI is the least significant bit of the Receiver CRC Register. This bit is read only.
7	QO (Quotient Out)	QO is the least significant bit of the CRC Register. This bit is read only.

CHAPTER 4

DETAILED DESCRIPTION

4.1 SCOPE

This chapter provides a detailed description of the DMC11 logic. Included in a general description of the DMC11 microinstruction word formats.

4.2 MICROPROCESSOR DESCRIPTION

4.2.1 Introduction

The following discussion includes a detailed description of each register and associated logic in the DMC11 microprocessor. Figure 4-1 illustrates a general block diagram showing registers and all internal data paths. Throughout the chapter, reference this diagram in all discussion relevant to data flow.

At times, it becomes important to know the contents of registers relative to other registers as well as machine timing. Figure 4-2 shows this relationship with respect to the master clock.

4.2.2 Microinstruction Word Formats

Two different microinstructions can be executed by the DMC11 microprocessor. They are the MOVE and BRANCH microinstructions. These microinstructions reside as permanent microcode in a Read-Only-Memory defined as the Control ROM (CROM). The CROM has enough storage capacity to store a microprogram of 1024 words. Each microinstruction word is sixteen bits long.

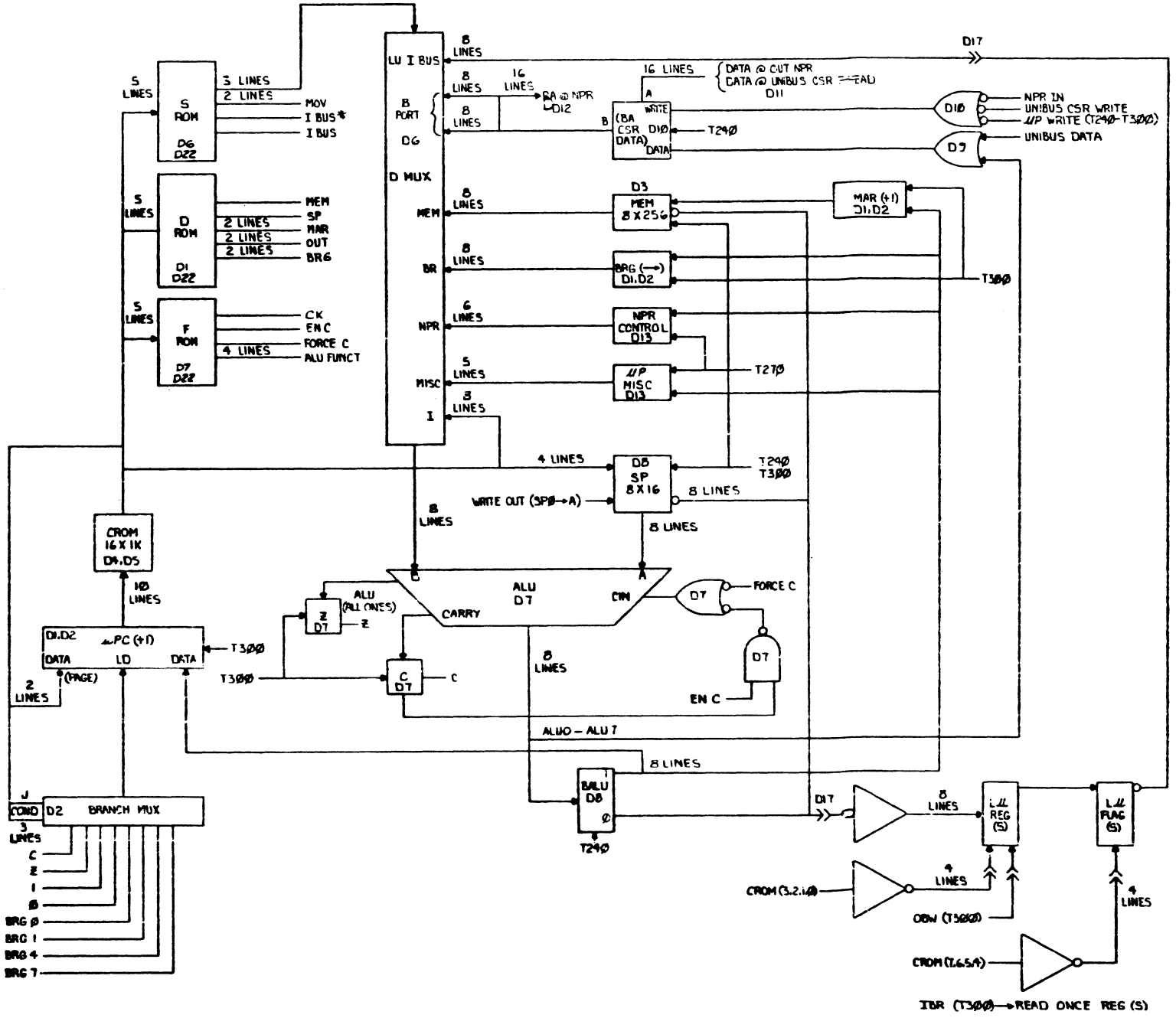


Figure 4-1 Microprocessor Block Diagram

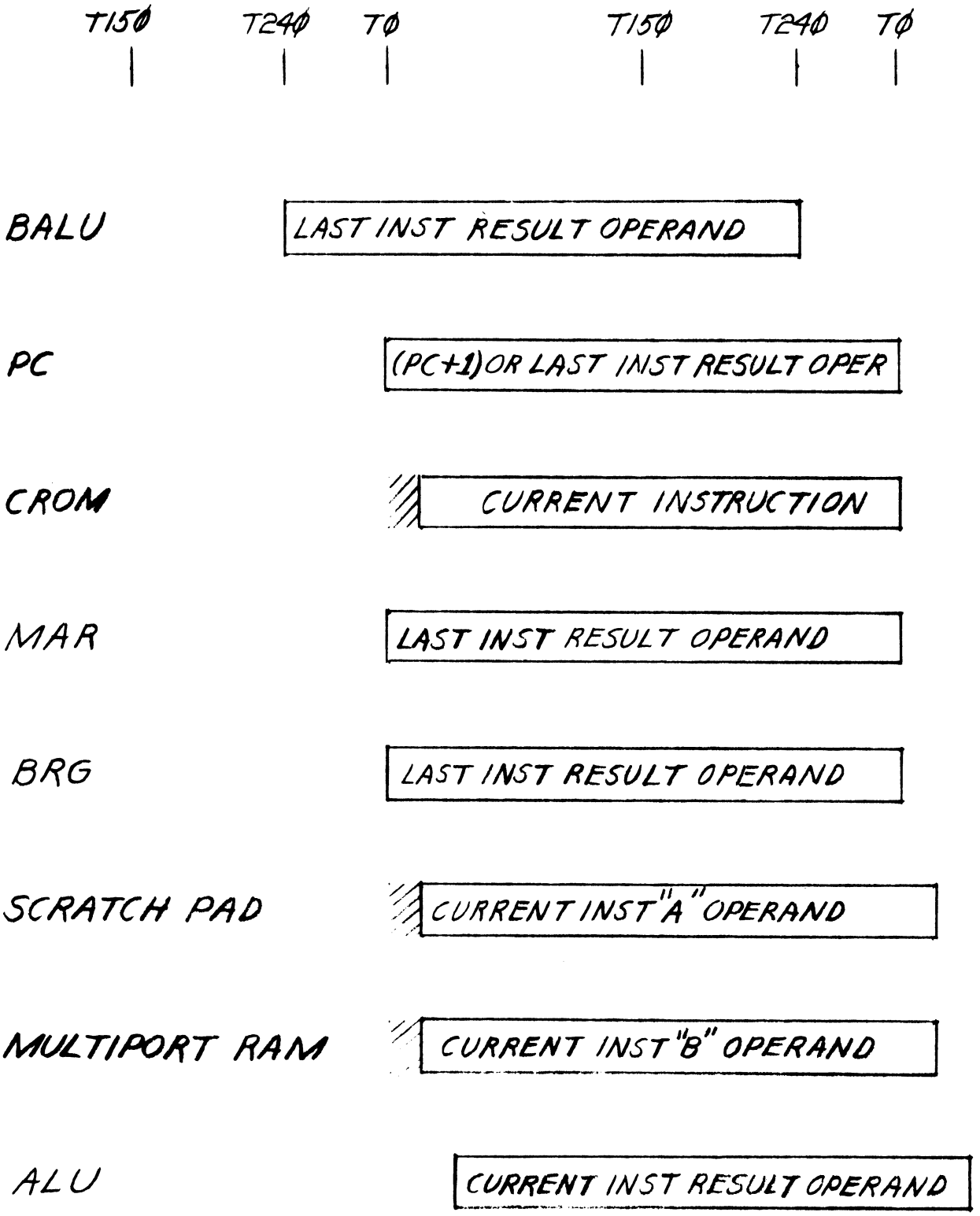


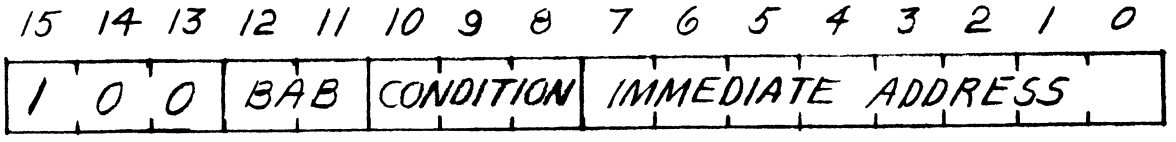
Figure 4-2 Microprocessor Register Timing

Figure 4-3 illustrates the word format of the BRANCH microinstruction. Bits 13-15 are the operation code defining the microinstruction as a branch. The operation code defines further the source operand from which the partial branch address is developed. The branch address being the address of the next microinstruction, should the branch condition be satisfied.

The condition under which the branch is to occur is defined by bits 8-10. The resultant branch address is partially defined by bits 0-7 of the microinstruction. These eight bits are combined with microinstruction bits 11 and 12 to form the complete ten bit branch address capable of addressing any of the 1024 locations within the CROM.

Three BRANCH microinstructions exist, each defining a different source operand from which to develop the low eight bits of the branch address.

4.2.2.1 0_8 - Branch Immediate (I)



The microprogram branches if the condition specified by microinstruction bits 8-10 is met. The ten bit branch address

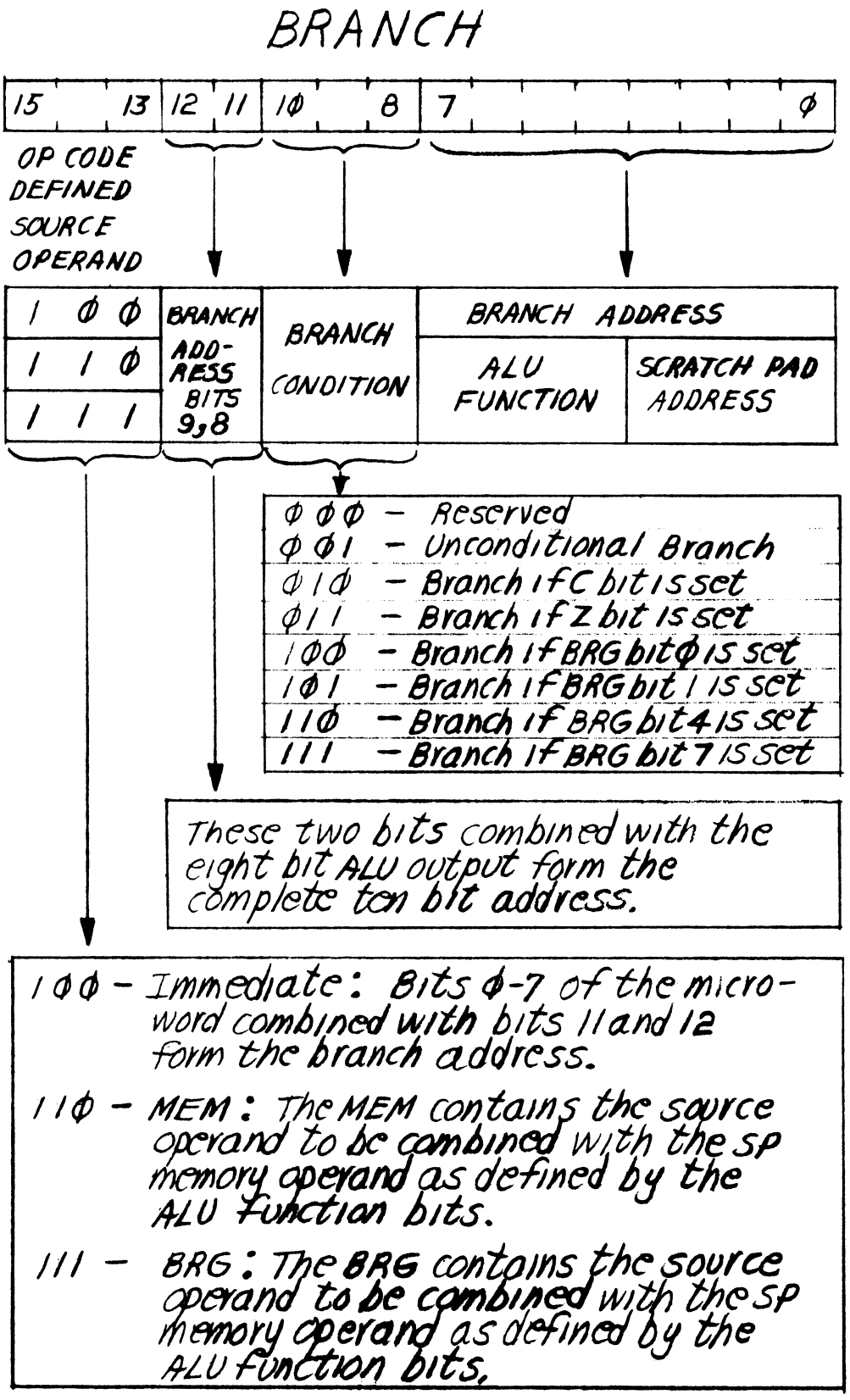


Figure 4-3 Branch Microninstruction Word Format

Figure 4-3 (Cont.)

ALU Function		Code
SUB	(A-B)	1110
2's COMP SUB	(A-B-1)	1111
ADD	(A,B)	0000
ADD W/C	(A,B,C)	0001
SUB W/C	(A-B-C)	0010
INC A	(A+1)	0011
A PLUS C	(A,C)	0100
2A	(A,A)	0101
2A W/C	(A,A,C)	0110
DEC A	(A-1)	0111
SEL A	(A)	1000
SEL B	(B)	1001
A or $\overline{B}$	(A+$\overline{B}$)	1010
A and B	(AB)	1011
A or B	(A+B)	1100
A X or B	(A $\oplus$ B)	1101

Notes:

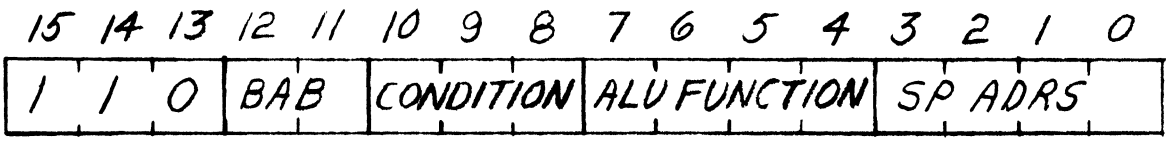
C = Carry

W/C = With Carry

C and Z are set/cleared with MOVE instructions.

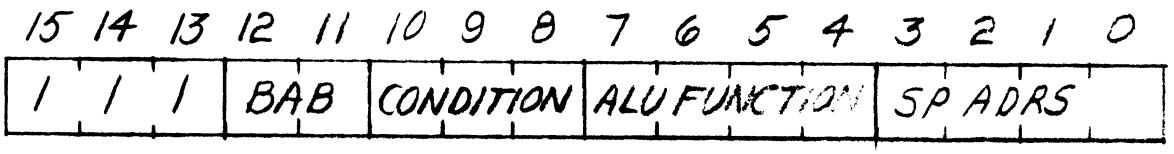
address is the result of combining microinstruction bits 0-7 with the Branch Address Bits (BAB) (bits 11 and 12).

4.2.2.2 6_8 - BRANCH Memory (MEM)



This microinstruction combines two operands in the Arithmetic Logic Unit (ALU) under control of the ALU FUNCTION bits (bits 4-7). The result operand when combined with microinstruction bits 11 and 12, produces a ten bit branch address. One operand is from a MEM storage location and the other is from the Scratch Pad (SP). Microinstruction bits 0-3 address the operand in the Scratch Pad, while the MEM operand is from the location addressed by the current contents of the Memory Address Register (MAR). The desired address would have been loaded into the MAR by a previous instruction other than the BRANCH under execution. The condition for the branch is defined by the CONDITION CODE, bits 8-10. Figure 4-3 defines the ALU FUNCTION CODES possible with this microinstruction.

4.2.2.3 7_8 - BRANCH Register (BRG)



With this microinstruction, the contents of the BRG and a Scratch Pad memory location are operated on to generate the partial branch address. Bits 0-3 specify the Scratch Pad memory location and bits 4-7 define the ALU FUNCTION to perform on the two operands.

The other microinstruction, the MOVE, like the BRANCH is a highly versatile microinstruction. When combined with the BRANCH in a microprogram, the combination produces a DMC-11 microprocessor of high versatility and power. In all, five variations of the MOVE microinstruction exist, each specifying a different source for the operand. The source is defined by the operation code. Figure 4-4 illustrates the MOVE microinstruction word format.

The operation code is defined by bits 13-15. Bits 11 and 12 specify the function to perform on the MAR. According to bits 11 and 12, the MAR can remain unmodified, incremented, or loaded from the Buffered ALU (BALU). The destination of the result operand is defined by microinstruction bits 8-10. The low byte of the microinstruction is operation code dependent further defining input addresses, ALU function, and output addresses.

The ALU Function Field (Figure 4-4), microinstruction bits 4-7, define the operation to be performed on the two operands. These four bits plus operation code bit 14 serve as the address input to the Function ROM (FROM). The FROM microword controls the ALU inputs.

MOVE

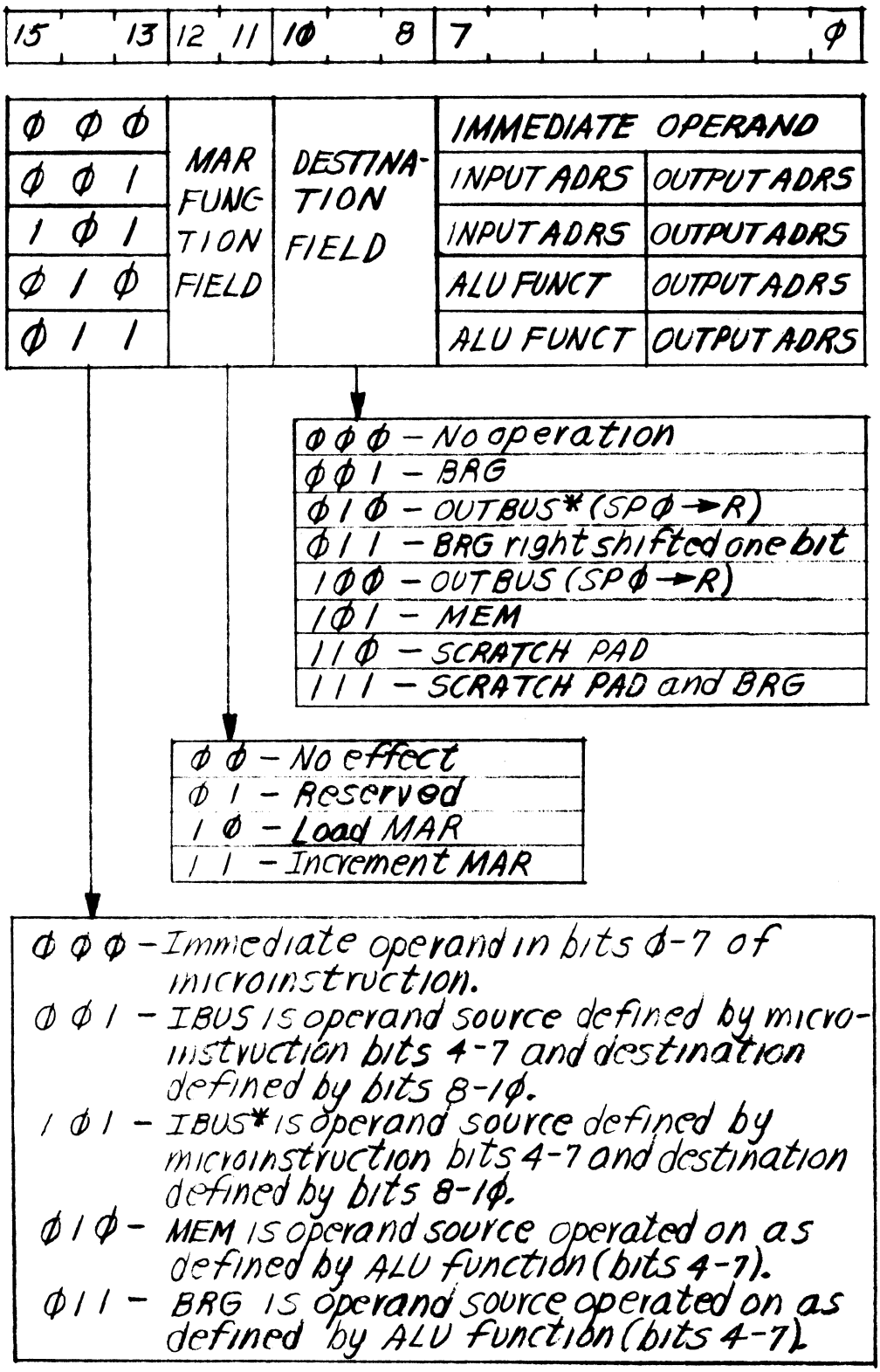


Figure 4-4 Move Microinstruction Word Format

Figure 4-4 (Cont.)

MOV ALU Functions

ALU Function		Code		
SUB	(A-B)	1110		
2's COMP SUB	(A-B-1)	1111		
ADD	(A,B)	0000	MOV	
ADD W/C	(A,B,C)	0001	INST	
SUB W/C	(A-B-C)	0010	CLOCK	
INC A	(A+1)	0011	C	MOV
A PLUS C	(A,C)	0100	(Note 1)	INST
2A	(A,A)	0101		CLOCK
2A W/C	(A,A,C)	0100		Z
DEC A	(A-1)	0111		(Note 2)
SEL A	(A)	1000		
SEL B	(B)	1001		
A or $\overline{B}$	(A+$\overline{B}$)	1010		
A and B	(AB)	1011		
A or B	(A+B)	1100		
A X or B	(A $\oplus$ B)	1101		

NOTES:

1. If ADD function, C is set to indicate carry or overflow.
2. If SUB function, C is cleared to indicate borrow or sign change.
2. Z is set when ALU out is all 1s.
3. C = Carry

   W/C = with Carry

   A = Arithmetic or scratch pad (SP) side of ALU.

   B = Logic or DMUX side of ALU.

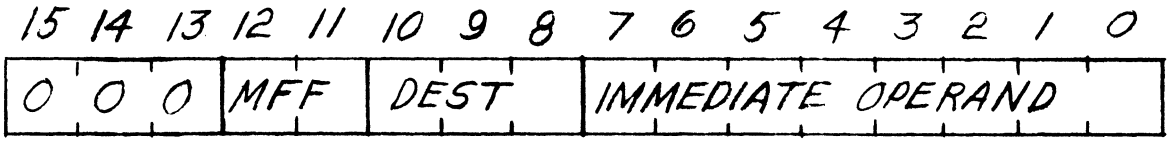
Common to all five MOVE microinstructions are the MAR FUNCTION FIELD and the DESTINATION FIELD. The MAR can be modified as per the previous paragraph. The MAR increment and load function sets up the MEM operand for the next microinstruction where necessary. The DESTINATION FIELD, as the name implies, specifies the destination of the result operand. Three of the eight possible destination references are microprocessor discrete registers, i.e., BRG, MEM, and BRG shifted and consequently need no further address definition. The specific location in MEM was predefined with a previous microinstruction. Four destination references require still further address definition. These include OUT BUS, OUT* BUS, SCRATCH PAD, and SCRATCH PAD/BRG. The low order four bits (bits 0-3) of the microinstruction provide a specific destination address within OUT BUS, OUT* BUS or the Scratch Pad memory when any of these are referenced as a destination.

When destinations OUT BUS and OUT BUS* are microprogrammed, SP address 0 is presented to ALU input A. Thus, if MOVE instruction MEM or BRG is used, all 16 ALU functions are available to operate on the two source operands (SP0 and MEM or BRG).

The BRG right shift destination performs a right shift on bits 7 to 0. Bit 0 is passed through the ALU B side before returning to BRG bit 7 during a MOVE type BRG instruction. This allows all 16 ALU functions with the SP to be used for the possible alteration of the data bit returned to BRG bit 7.

Instruction types MOV I, MOV IBUS, MOV IBUS* and MOV MEM may also be used with a BRG right shift. However, in these cases ALU bit 0 is a function of sources I, IBUS and IBUS* while MOV MEM, which is similar to MOV BRG, is a function of MEM and SP as selected by the 16 ALU functions.

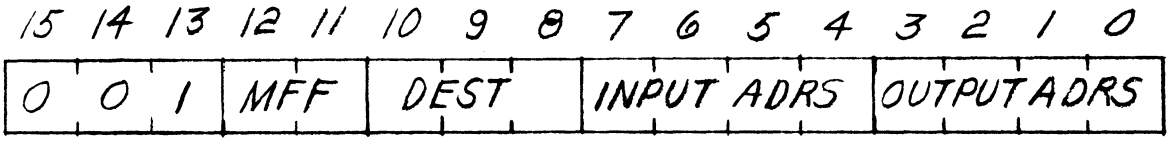
4.2.2.4 0_8 - MOVE Immediate (I)



The operand, microinstruction bits 0-7, is moved to the destination as specified by microinstruction bits 8-10.

With the MOVE IMMEDIATE, the destination reference is normally limited to the BRG, MEM, and the MAR. The other possible destination references are useable, however, they require special consideration since the same data is used both as an operand and destination address.

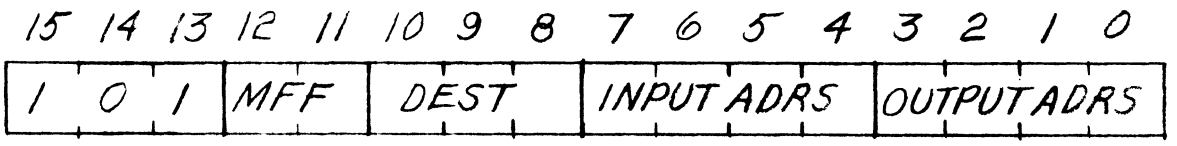
4.2.2.5 1_8 - MOVE IN BUS (I BUS)



The operation code specifies the I BUS as the source operand. However, because the IBUS is a block of sixteen 8-bit words additional address information must be provided by the INPUT

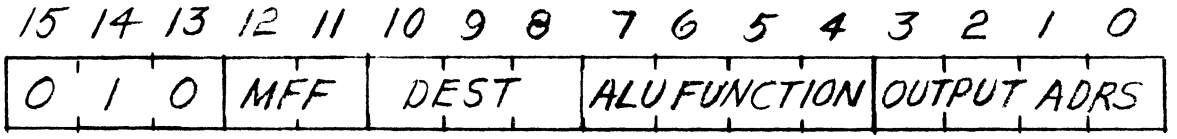
ADDRESS portion of the microinstruction (bits 4-7). In cases where the DESTINATION FIELD specifies data blocks, i.e., OUT BUS, OUT* BUS or the Scratch Pad memory, microinstruction bits 0-3 specify the byte position within the block as the destination. In addition the operand can also be clocked into the MAR when so indicated by the MAR FUNCTION FIELD, microinstruction word bits 11 and 12.

4.2.2.6 5_8 - MOVE IN BUS* (I BUS*)



This microinstruction is similar to the MOVE I BUS microinstruction with the exception that the MOVE I BUS* addresses the * I BUS block of words.

4.2.2.7 2_8 - MOVE Memory (MEM)



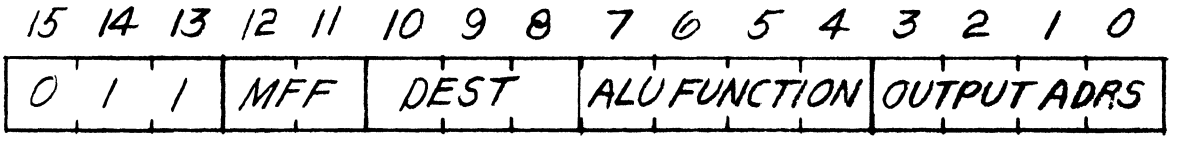
The MOVE MEM microinstruction performs either an arithmetic or logical operation on two designated operands and deposits the result operand into the specified destination address. One of the two operands is from MEM while the second is from the Scratch Pad memory. The specific location within the SCRATCH PAD memory

is defined by the microinstruction OUTPUT ADDRESS field (bits 0-3).

The result operand is moved to the destination as specified by the DESTINATION field, microinstruction bits 8-10.

When the Scratch Pad memory or MEM is designated as the destination, then the respective source operand is destroyed by delivery of the result operand.

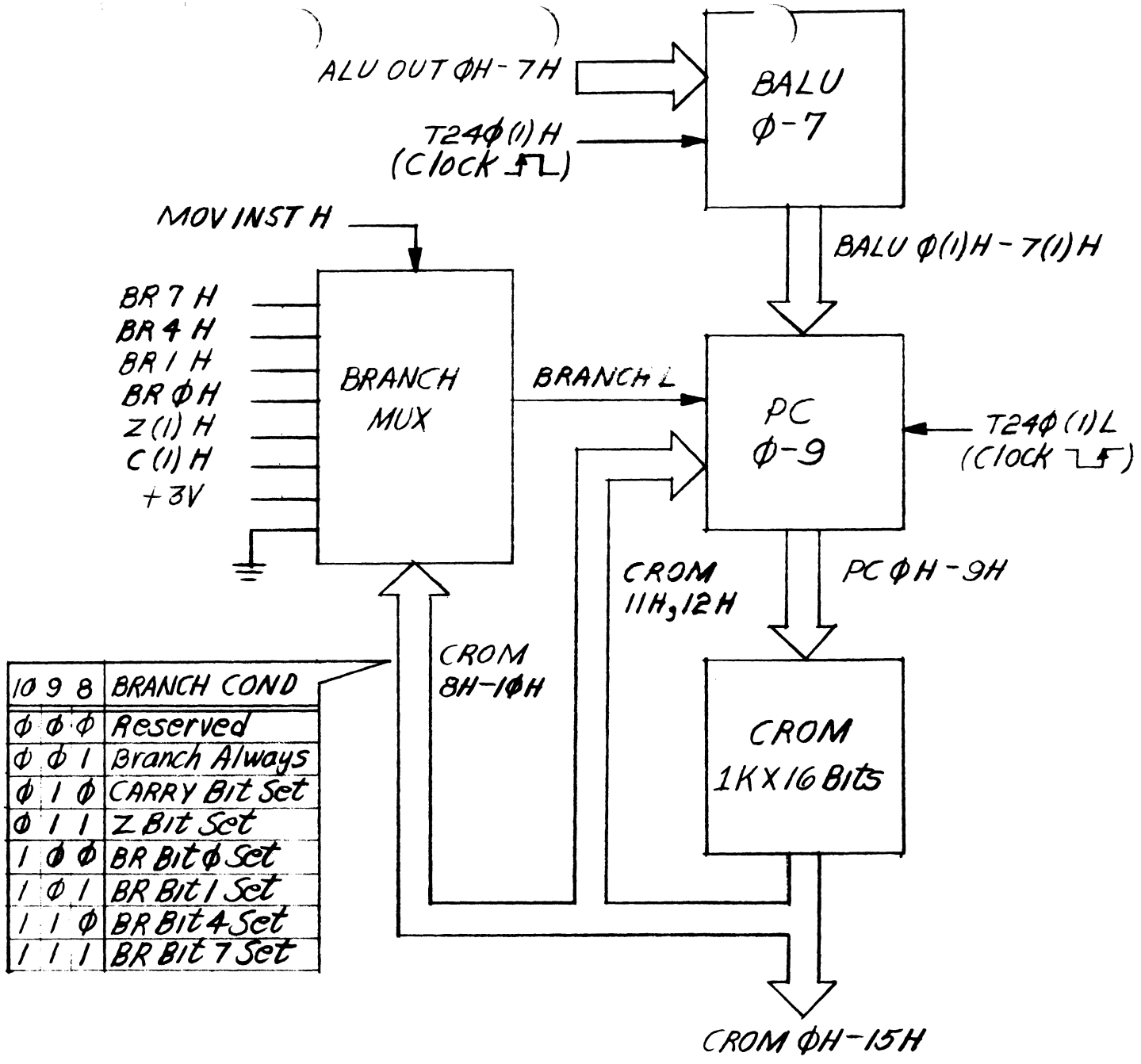
4.2.2.8 3_8 - MOVE BRANCH REGISTER (BRG)



The operation of the MOVE BRG microinstruction is similar to the MOVE MEM with one exception. The two operands of this microinstruction are the contents of the BRG and the Scratch Pad memory. If the microinstruction specifies either the Scratch Pad memory or the BRG as the destination, then the respective source operand is destroyed by the delivery of the resultant operand.

4.2.3 CROM, MAR, BR, PC and BRANCH MUX

The basic microprogram stored in the CROM is addressed by a ten bit Program Counter (PC). See Figure 4-5. The PC operates in



10 9 8	BRANCH COND
Ø Ø Ø	Reserved
Ø Ø 1	Branch Always
Ø 1 Ø	CARRY Bit Set
Ø 1 1	Z Bit Set
1 Ø Ø	BR Bit Ø Set
1 Ø 1	BR Bit 1 Set
1 1 Ø	BR Bit 4 Set
1 1 1	BR Bit 7 Set

Figure 4-5 Block Diagram of Program Counter Control Logic

two modes. It can be either incremented or parallel loaded from the BALU. The BRANCH MUX output determines which function occurs. A low condition on the BRANCH MUX output causes the PC to load i.e., branch. The PC is always altered on the trailing edge of T240. Eight bits of the branch address come from the BALU while the high order two bits come directly from the microinstruction word (bits 12 and 11).

CROM bits 8-10 determine which one of eight inputs is selected by the BRANCH MUX. The truth table in Figure 4-5 lists the selection codes controlling the MUX. Note in Figure 4-5 the BRANCH MUX is disabled when executing any MOVE microinstruction. Conversely it would be enabled for all BRANCH microinstructions.

Using the BRG, the microprocessor has the ability to shift a byte of data one bit position to the right, each time the appropriate microinstruction is executed. Data is rotated to the right with BALU 0 in the loop. BALU 0 gates to BRG7 while BRG0 passes through the ALU and is subsequently clocked into BALU0.

Control of the BRG is determined by the two inputs SO and SI. With these two control signals, the BRG can load data, shift data, or recirculate data.

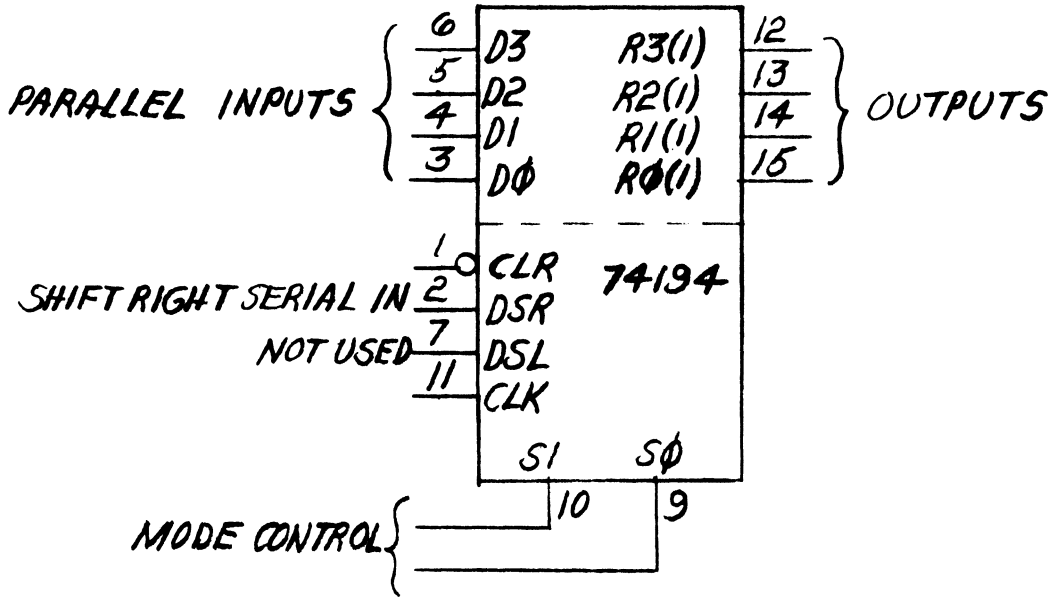
See the truth table in Figure 4-6. While SO and SI determine what function to perform, the clock signal, CLOCK MAR, BR L, determines when to do it. This BRG clock always occurs on the trailing edge of T240 when executing a MOV microinstruction.

Main memory (MEM) with 256 locations is addressed by the eight bit Memory Address Register (MAR). Like the PC, the MAR can be parallel loaded from the BALU outputs or incremented on the trailing edge of the clock signal CLOCK MAR, BRG L. Clocking always occurs on the trailing edge of T240 during execution of a MOVE microinstruction. Two bits of the DESTINATION ROM (DROM) microword determine the function to perform on the MAR (MAR LD L and MAR INC EN L).

As previously discussed, the DROM microword controls the MAR and the BRG. It also has four additional bits to control writing into MEM, Scratch Pad memory, Scratch Pad memory address register, and the *OUT BUS. Microinstruction bits 8-12 form the DROM address which in the MOVE microinstruction represents the DESTINATION field and MAR FUNCTION FIELD. The DROM is shown in Figure 4-7 and the DROM map is shown in sheet D20 of the print set.

4.2.4 Main Memory (MEM)

Eight integrated circuit chips comprise the 256 location main memory. Each chip stores one bit of an eight-bit byte. Stored in the memory are items such as message headers and commonly used protocol messages.

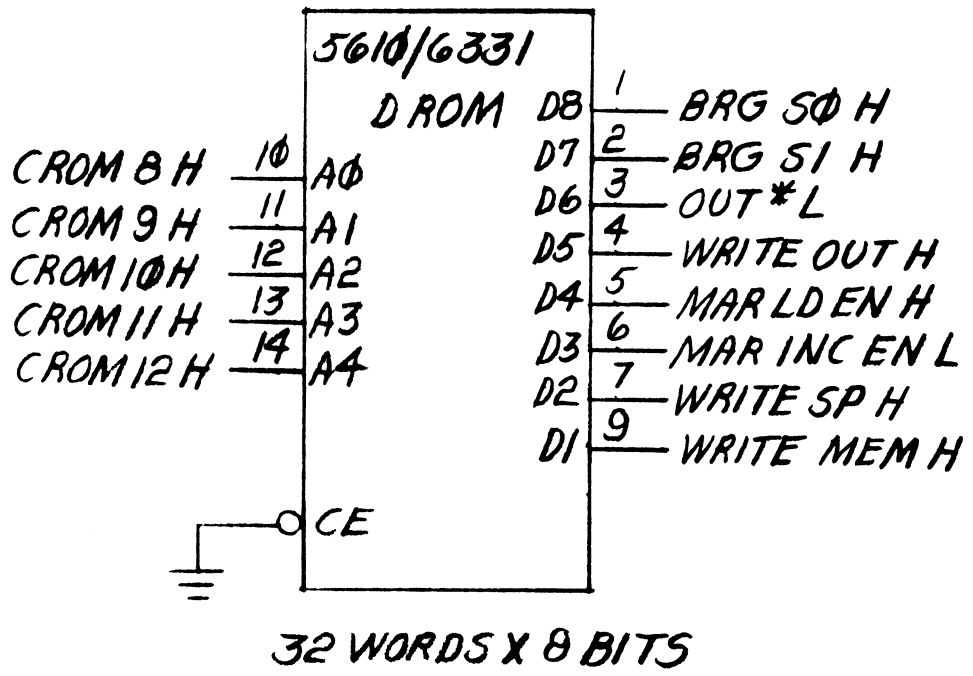


74194 TRUTH TABLE

S1	SØ	FUNCTION
1	1	Parallel Load
Ø	1	Shift Right
1	Ø	Not Used
Ø	Ø	Hold (Inhibit Clock)

The BRG is composed of two 74194 4-Bit Bidirectional Universal Shift Registers.

Figure 4-6 Configuration of the B Register



See print set sheet D20 for DROM Map.

Figure 4-7 Configuration of DROM

Memory addressing is accomplished using the MAR, while write data is gated directly from the BALU outputs. Write timing is controlled through the function WRITE MEM L, originating at the DROM. The memory contents can be sourced with the MOVE microinstructions and two of the three BRANCH microinstructions. Operation code 6_8 can only read MEM contents.

The MEM output feeds the DMUX input and is selected with a code of 2_8 for a MOVE or 6_8 for a BRANCH. The DMUX selects the MEM output during execution of the MOVE MEM or BRANCH MEM microinstruction.

4.2.5 CROM and the Maintenance REG

The CROM is the heart of the microprocessor system through which complete system control is exercised. Stored within the CROM is the unique microprogram necessary for execution of the DDCMP protocol. This stored microprogram utilizes the two powerful microinstructions discussed at the beginning of this chapter. A total of 1024 memory storage locations are available for the microprogram, through the use of eight integrated circuit chips. Each chip stores four bits of the microinstruction in 512 storage locations. Addressing is with the ten bit Program Counter.

Microinstructions read from the CROM become the address for a second level microword contained within three additional ROMs.

In addition, certain microinstruction bits directly control gating and timing operations throughout the microprocessor.

Each ROM chip has a chip enable input (pin 13) which must be asserted low in order to enable the chip. Because these chips are tri-state devices, a disabled chip presents a high impedance (Z) output allowing the wiring of outputs, thus expanding total memory capacity. In the microprocessor, two memory chips (each storing 512 four bit words) have their outputs wired together forming a memory of 1024 locations. The appropriate chip is selected with PC9.

A maintenance feature of the microprocessor allows the PDP-11 software to simulate the CROM outputs through the use of the Maintenance Register. The output of the Maintenance Register is wire ORed with the CROM output. With the CROM disabled and the Maintenance Register enabled, the contents of the register become the system microinstruction. The register is loaded from the UNIBUS data receivers when Select 6 (SEL 6) of the CSRs is loaded from the PDP-11. However, the maintenance register is not gated on unless ROM I in BSEL 1 is asserted. ROM I also deselects the CROM (high Z outputs).

4.2.6 DMUX and SROM

The DMUX is an eight bit wide, eight to one multiplexer, whose output feeds the B input of the Arithmetic Logic Unit (ALU).

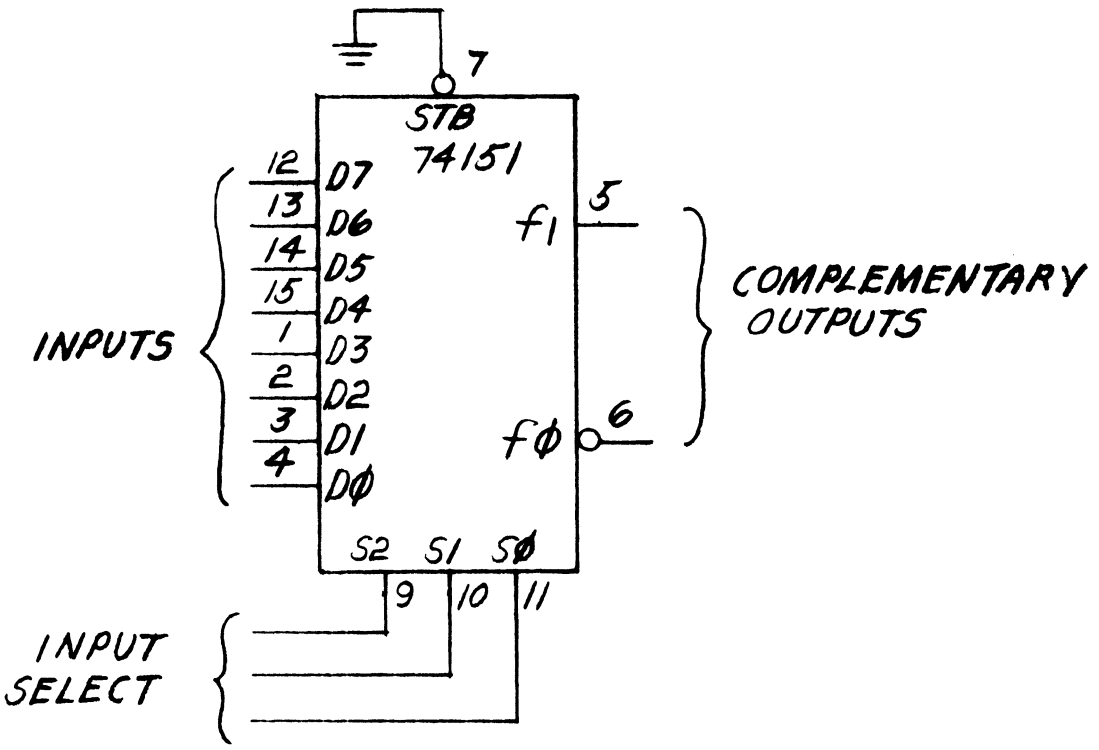
Input selection is controlled by three bits originating at the SOURCE ROM (SROM). The DMUX and associated truth table are shown in Figure 4-8.

The SROM is a thirty-two location ROM containing an eight bit microword. The SROM is shown in Figure 4-9 and the SROM map is shown in sheet D20 of the print set. The SROM is addressed directly by the CROM (bits 13-15, 4 and 7). Note three of these bits are the microinstruction operation code.

4.2.7 ALU and Associated Logic

With the Arithmetic Logic Unit (ALU), the microprocessor can execute ten arithmetic and six logical operations on any data presented to its A and B inputs. See Figure 4-10.

The ALU is built around two 74S181 integrated circuit chips each accommodating four bits or one-half byte. Four functional inputs feed the ALU while three others output from it. Two of the inputs are eight bit operands. A third input, carry in, is a carry function which can be inserted under control of the microprocessor. The fourth and final input is a five bit function bus defining the type of operation to perform on the two operands and carry in. This operation is defined by the FUNCTION ROM (FROM) microword. The FROM is shown in Figure 4-11 and the FROM map is shown in sheet D20 of the print set.

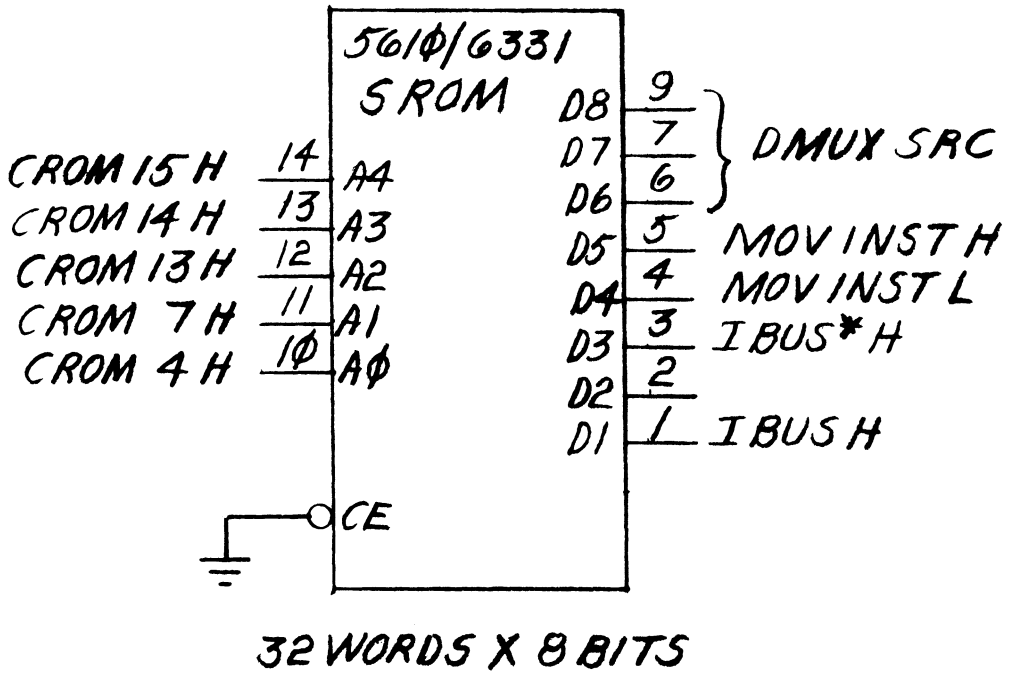


74151 TRUTH TABLE

SELECT			INPUT
S2	S1	SØ	
H	H	H	D7-µP MISC REG
H	H	L	D6-NPR CNTL REG
H	L	H	D5-BPORT ODD BYTE
H	L	L	D4-BPORT EVEN BYTE
L	H	H	D3-BRG
L	H	L	D2-MEM
L	L	H	D1-LU IBUS
L	L	L	DØ-CROM 9-7

The DMUX is composed of eight 74151 multiplexers.

Figure 4-8 Configuration of DMUX



See print set sheet D20 for SROM Map.

Figure 4-9 Configuration of SROM

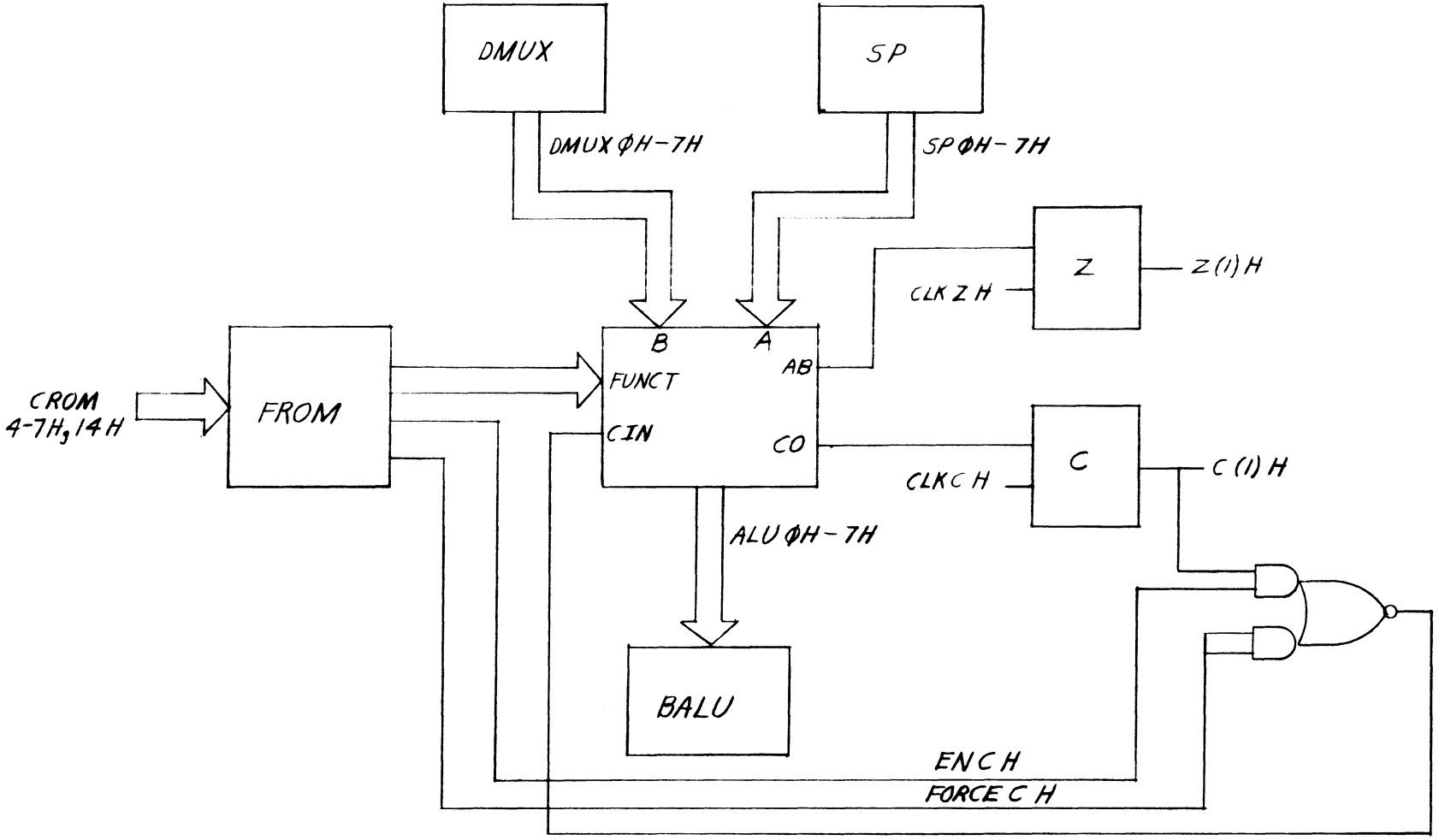
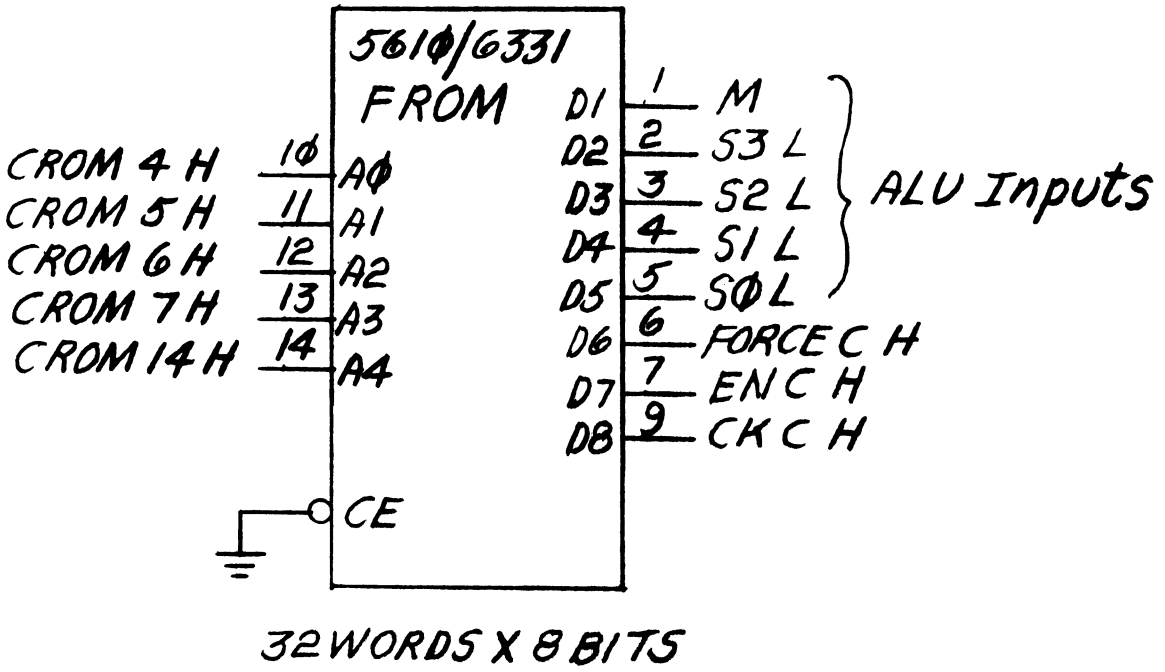


Figure 4-10 ALU and Associated Logic



See print set sheet D20 for FROM Map.

Figure 4-11 Configuration of FROM

The result of any logical or arithmetic operation appears asynchronously at the ALU's output data bus and on the leading edge of T240 is clocked into the BUFFERED ALU REGISTER (BALU). Another output Z becomes asserted when the ALU output is all 1s. The third and final output is the carry bit. Both the carry bit and the A = B output are clocked into storage flops, under control of the FROM microword.

Insertion of a carry occurs under one of two conditions defined by the FROM. A carry insert can be forced with FORCE C H or inserted as a function of the C flip-flop with ENABLE C H.

4.2.8 Scratch Pad Memory

The only way to present an operand to the ALU A input is through the Scratch Pad memory. The Scratch Pad memory contains sixteen locations, all addressable by CROM bits 0-3. Two type 3101 integrated circuits chips, each storing one-half byte, comprise the complete memory.

Addressing is controlled by a 74157 multiplexer, supplying one of two possible inputs as a four bit address to the S PAD memory. Selection is by DI WRITE OUT H, which when asserted selects a hardwired input address of all zeroes. The default input is CROM bits 0-3. This signal is a bit in the DROM microword.

The DROM also controls writing into the SCRATCH PAD memory. Data is written from the BALU output.

4.2.9 Multiport RAM

The MULTIPORT RAM is an eight word random access memory having the capability of being simultaneously accessed from two sources. Each word is sixteen bits in length. A total of four chips comprise the multiport ram with each chip containing eight four bit wide storage locations. A functional description of the chips follows. Refer to Figure 4-12.

Two independent read outputs are available, one referenced as the A PORT (pins 8, 9, 10, and 11) and another as the B PORT (pins 13, 14, 15, and 16). Note each read bus is four data bits wide.

Associated with each read port is an address input. Valid data appears at the A port output for the location addressed by the A port address input (pins 6, 5, and 4). A unique feature of this memory is that simultaneously another location can be addressed by presenting this second address to the B port address input (pins 18, 19, and 20). The contents appear at the B port output. The read enable input (pin 7 for A and pin 17 for B), must be asserted low in order to read data from either port.

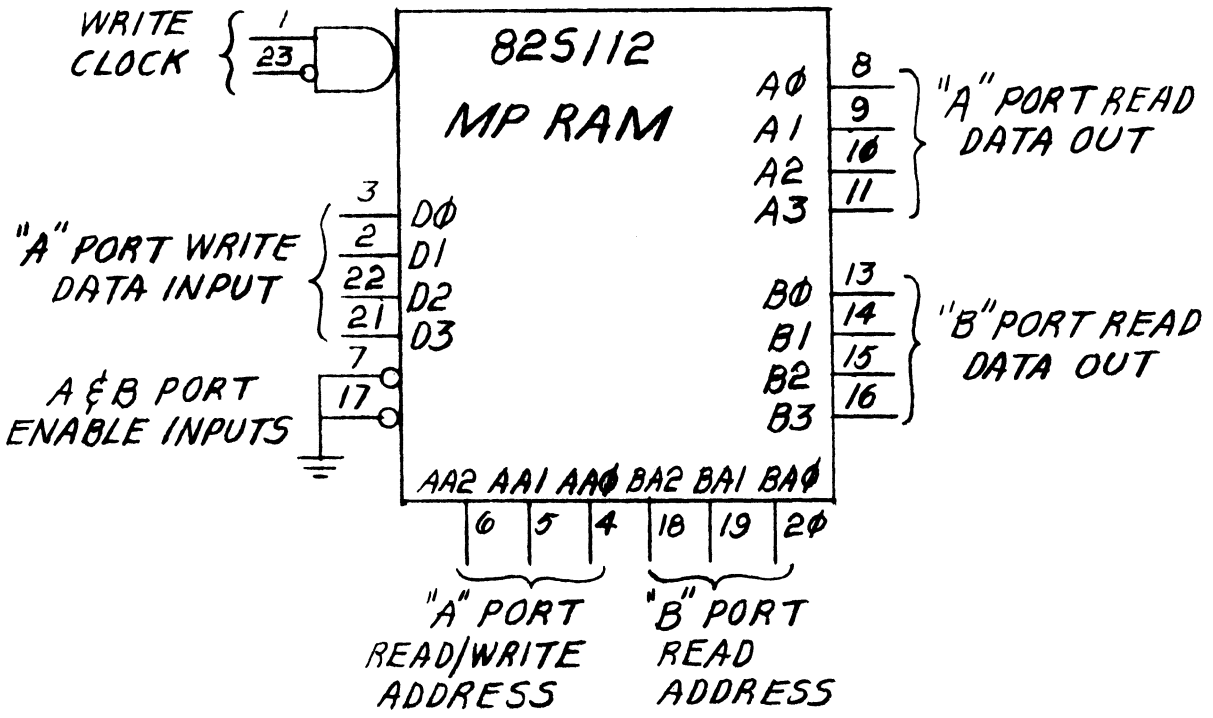


Figure 4-12 Multiport RAM

Although data can be read from both ports, it can be written only through one port, the A PORT. This is done by presenting the desired address to the A PORT ADDRESS INPUT while simultaneously presenting data to the A PORT WRITE DATA INPUT (pins 3, 2, 22, and 21). The necessary timing is supplied through pins 1 and 23.

The MULTIPORT RAM address assignments are shown in Figure 4-13. Note the memory is divided into two blocks, one block of four words associated with the OUT/IBUS and the other with OUT*/IBUS. Stored in the memory as OUT/IBUS addresses are both data and addresses of the data for NPR transfers with the PDP-11 memory. These MULTIPORT RAM memory locations are applicable during NPR cycles. Additionally, the OUT*/IBUS* addresses shown are the Unibus CSRs as addressed from either the microprocessor or the Unibus.

The block diagram in Figure 4-14 illustrates the relative position of the MULTIPORT RAM within the microprocessor architecture. Shown are the three output loads, the two data input sources and the addressing schemes.

The B PORT output data bus feeds both the UNIBUS address bus drivers and the DMUX. However, because the DMUX is only eight bits wide and the RAM output is sixteen bits, the RAM output is fed to the DMUX on two separate inputs.

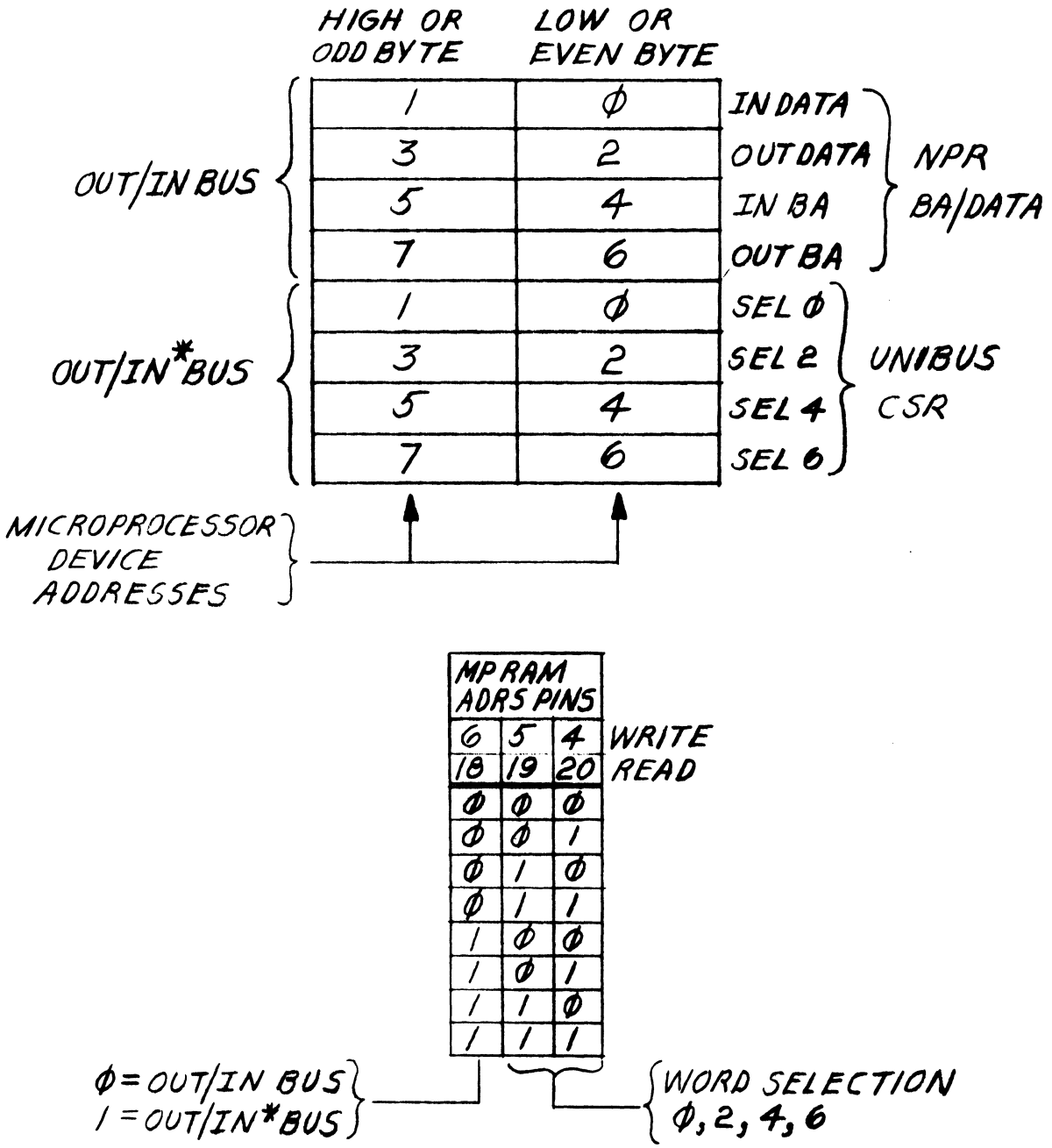


Figure 4-13 Multiport RAM Addresses

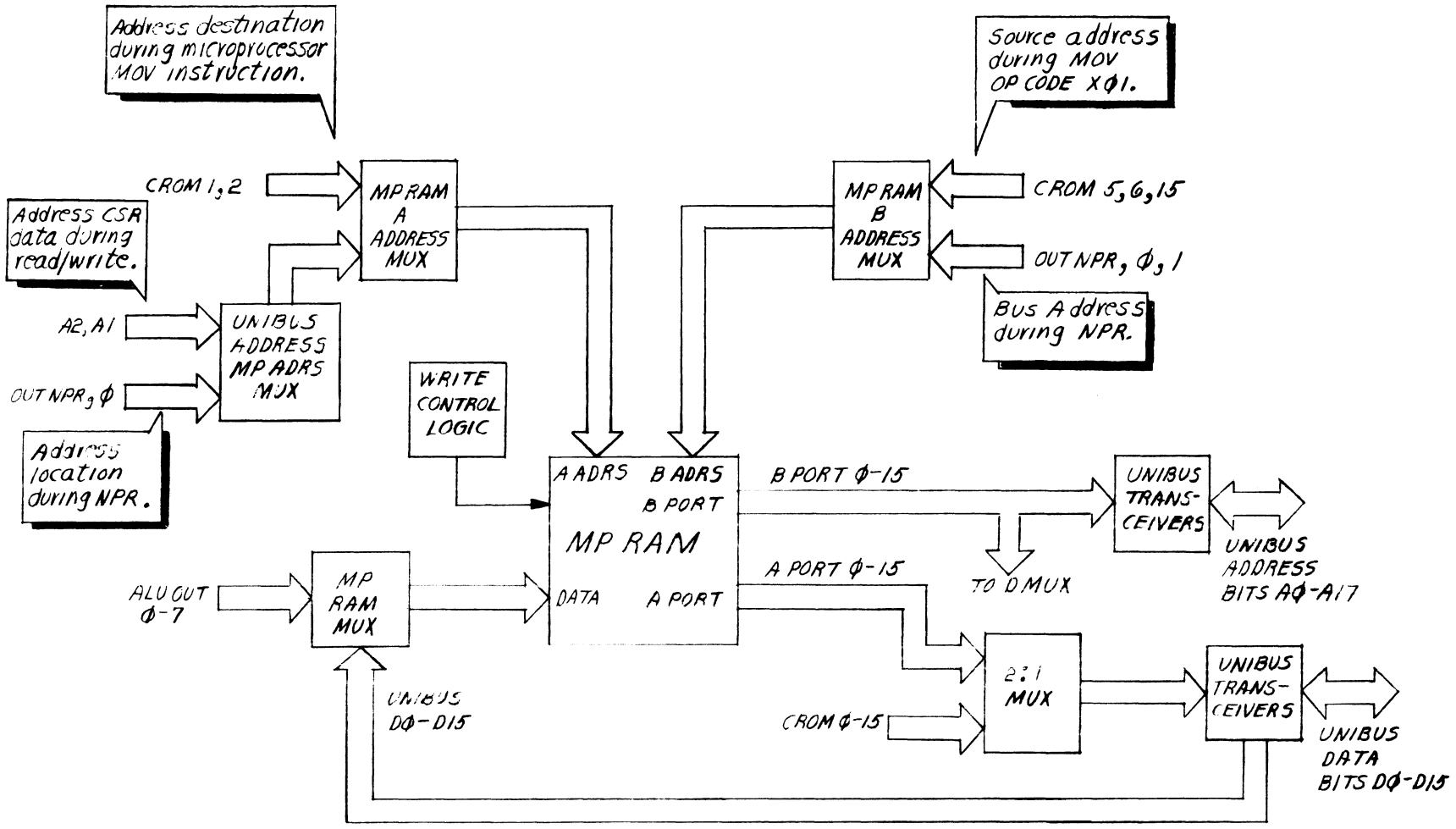


Figure 4-14 Block Diagram of Multiport RAM and Associated Logic

When the microprocessor executes NPR cycles, the bus address will be fetched from the RAM through the B PORT and clocked into the bus drivers by NPR MASTER. The two RAM locations where the bus address is stored is defined by the B PORT address multiplexer with MP READ CYCLE low. This results in addressing either location two or three, as determined by OUT NPR.

The remaining input to the B port address multiplexer becomes active during a particular MOVE microinstruction (X01) and in turn gates the addressed data either to the high byte or to the low byte input on the DMUX. Bits 5, 6, and 15 determine the RAM address. Bit 15 determines which group is to be addressed, the IBUS or *IBUS. The location within the selected group is addressed by bits 5 and 6. The appropriate byte is selected by the DMUX.

With the A PORT, both reading and writing must be considered. The A PORT output bus feeds a 2:1 multiplexer which feeds the UNIBUS data bus drivers. Data is written into the RAM through another 2:1 multiplexer which selects either the UNIBUS data receivers or the ALU output as the data to be written.

There are three conditions under which data is written into the MULTIPORT RAM: (1) an output NPR cycle, (2) loading a CSR by the PDP-11, and (3) writing by the microprocessor. MP WRITE CYCLE is asserted when the microprocessor executes a write cycle. This condition then selects the ALU output to be written into the

RAM as illustrated in Figure 4-14. On the other hand the UNIBUS data receivers are selected as the RAM input data for both NPR cycles and CSR loading.

A full word or one byte at a time can be written into the MULTIPORT RAM. This is controlled by HBWL and LBWL. When writing the ALU output, the eight bit byte can be written into either the high or low byte position. Bit zero of the microinstruction (CROM0) determines the byte position. During NPR cycles full words are always written into the RAM. When writing into a CSR, the PDP-11 instruction determines the write control condition with C0 and A0.

The A PORT addressing is determined through two levels of multiplexing as shown in Figure 4-14. CROM bits 1 and 2 determine addressing with the first multiplexer when the microprocessor writes into the RAM. The second input to this multiplexer is an output of another multiplexer under control of NPR MASTER. During the execution of NPR cycles, one of two fixed locations (location 0 or 1) is always addressed. Which location is addressed is a function of desired data transfer direction. CSR addressing is determined by the UNIBUS address bits A01 and A02, and always reference the high four RAM addresses.

4.2.10 Maintenance CSR (BSEL 1)

A number of maintenance features are available for the DMC-11

through the use of the MAINTENANCE CSR. The MAINTENANCE CSR address is 76xxx1 and can be referenced via a word or byte transfer. With this feature, the PDP-11 diagnostic program can read the contents of the CROM, write into the MAINTENANCE INSTRUCTION REGISTER thereby substituting the CROM microword, step either or both the microprocessor and the line unit, and loop transmitted data through the line unit back to the microprocessor for verification.

The MAINTENANCE CSR byte format is illustrated above with the logic shown on drawing D17. Five of the bits are stored in the microprocessor each time the MAINTENANCE CSR instruction is executed. D09-D12 are stored in a 74174 while D15 is stored in a 74S74 on the leading edge of LD BSEL 01L provided the BYTE SEL 01 LOCK OUT switch is off. This switch must be off to enable all diagnostic features. Another switch, RUN INHIBIT, when on prevents the RUN flop from setting. Obviously, this switch must be off to enable the microprocessor to enter RUN mode. The two remaining bits D14 and D08 pulse the microprocessor at instruction execution.

4.2.10.1 Step LU H

This signal, a function of bit 12, feeds directly to the line unit interface controlling the stepping of the line unit. When set, it clocks the line unit transmitter and when it is cleared it clocks the line unit receiver.

4.2.10.2 LU Loop H

This signal, a function of bit 11, feeds directly to the line unit enabling the loopback feature. With this feature, the diagnostic program can transmit known data which the line unit then sends back to the microprocessor as received data. The program then performs a comparison on transmitted data and received data to determine if any errors had occurred.

4.2.10.3 CROM OUT H

Under control of bit 10, the diagnostic program can read the contents of the CROM in order to determine the validity of machine cycling. The functions CROM OUT H and A2H select the CROM microword through a multiplexer then drive the UNIBUS data lines.

What this means is that a second instruction, a DATI with an address of $xxxxx4_8$ must be executed following the MAINTENANCE CSR instruction which set CROM OUT H. This enables the multiplexer on print D11 to select the CROM microword and feed it to the UNIBUS data lines.

4.2.11 Microprocessor Clock

The basic clock consists of six JK flip-flops interconnected as a shift register generating six discrete time intervals. Each time interval is asserted for a period of 60 nsec. However, due to unique clocking, four time intervals overlap resulting in an overall clock period of 300 nsec instead of the expected 360 nsec. Figure 4-15 illustrates the clock sequencing. Note the overlap of T90 with T60 and T240 with T210. These clock signals are distributed throughout the microprocessor to clock registers and provide system timing.

A 33.33 Mhz oscillator generates the timing used to clock the shift register. However, before being applied to the clock inputs of the shift register, the oscillator output (CK) first passes through a control flop (WAIT SYNC) and a divide-by-two flop (SYSTEM CLOCK). See drawing D14 in the print set. The control flop WAIT SYNC stops the clock when the multiport RAM is being accessed and allows the clock to continue only when the multiport RAM becomes available. This clock hold state is in effect with WAIT SYNC in the reset state. But with WAIT SYNC set, SYSTEM CLOCK toggles with each Hi to Low transition on its clock input. Both outputs of SYSTEM CLOCK (Q and $\overline{Q}$) are used as shift register clocks.

Refer to drawing D14 for the following logic analysis. Note the flip-flops T0 through T240 are wired as a right shifting shift

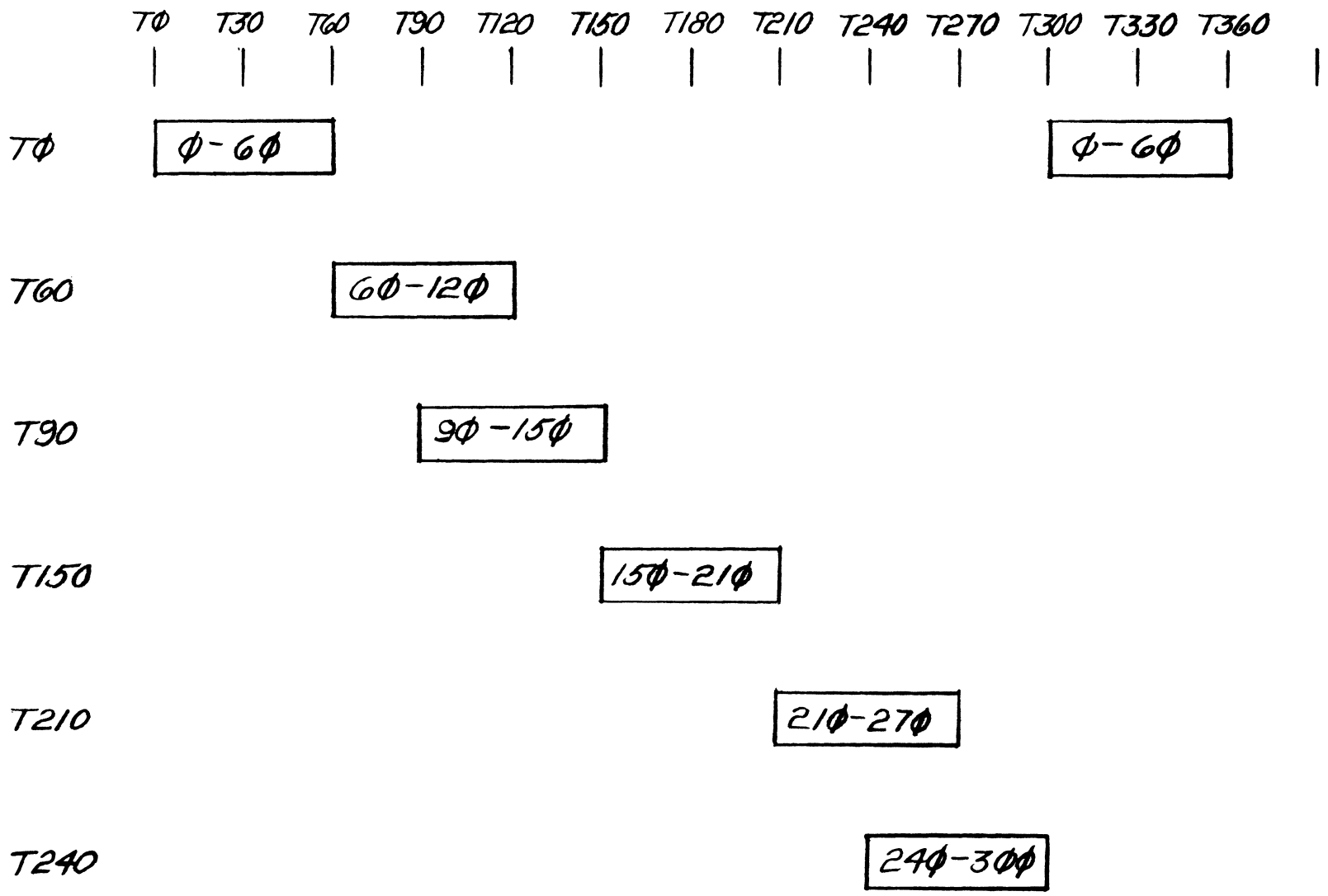


Figure 4-15 Clock Sequence

register with T240's output dropping off into the bit bucket. T0's JK inputs are wired to toggle T0 when the four flip-flops T60, T90, T150, and T210 are all reset and RUN SYNC is set. Note the shift register does not use the same clock source for all positions. T90, T150, and T210 are clocked by the "Q" output of SYSTEM CLOCK, while T0, T60, and T240 are clocked by SYSTEM CLOCK's Q output. The aforementioned overlap of time intervals is generated by using these two clocks 180° out of phase.

Given the initial conditions of RUN SYNC and WAIT SYNC both set, and the shift register all zeroes, results in a Hi condition on both the J and K inputs to T0 placing T0 in the toggle mode. The next time SYSTEM CLOCK sets, T0 will set. This point in time is referenced as "time 0". See Figure 4-16. With T0 set, the set input to T60 is qualified while simultaneously the toggle input to T0 remains asserted. Therefore, on the next SYSTEM CLOCK occurring 60 nsec later, T60 sets and T0 resets. From this point, the clock functions as a shift register. When the bit reaches T240, a new bit is regenerated at the inputs to T0.

The microprocessor cycling can be halted by stopping the SYSTEM CLOCK. This is done by resetting the RUN flop. When the RUN flop is reset, RUN SYNC allows the clock shift register to complete the current clock cycle and stop with the shift register cleared.

In STEP MODE, each STEP MC L pulse sets RUN SYNC allowing one complete clock cycle (T0 - T240) to occur.

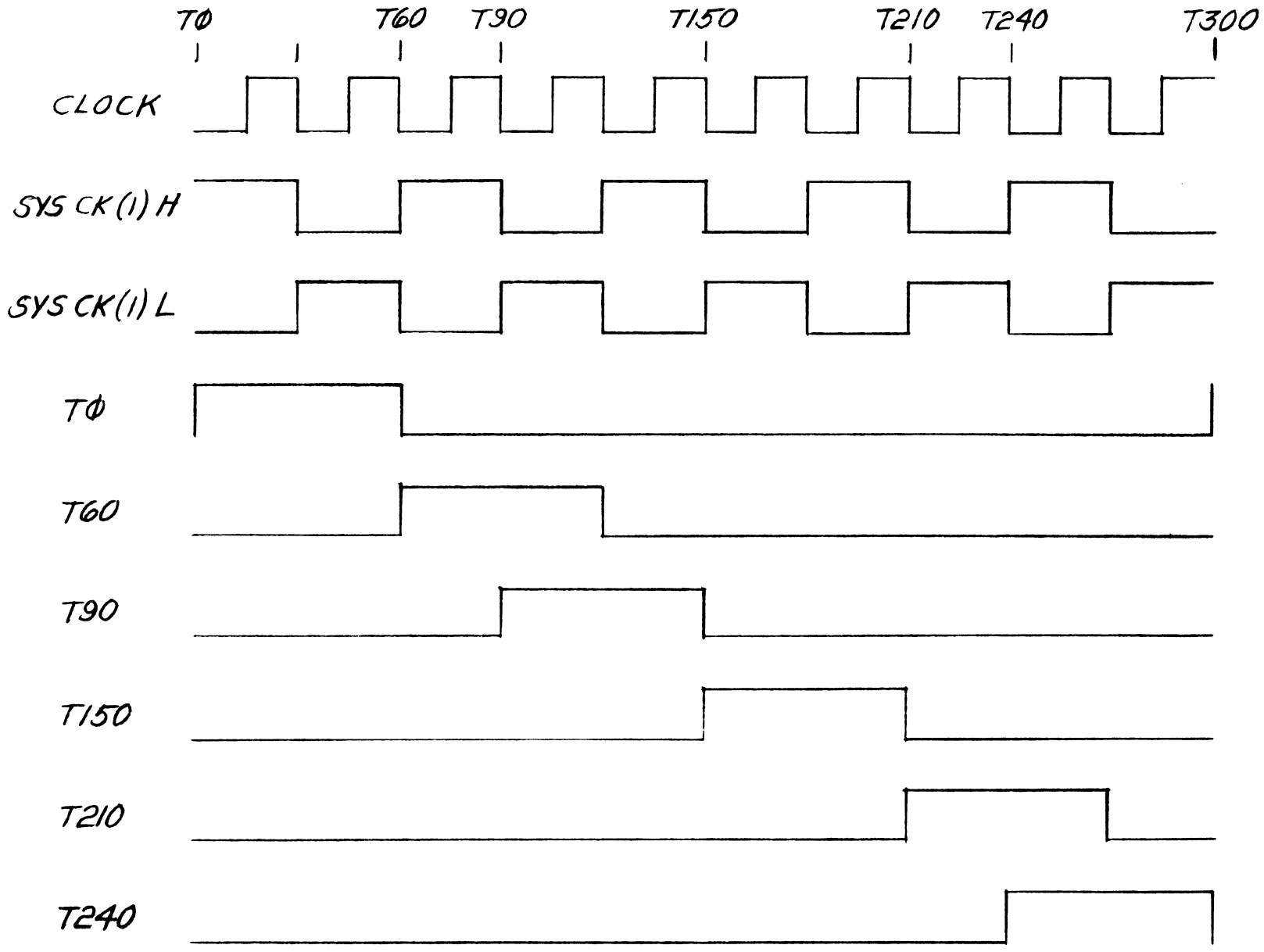


Figure 4-16 System Clock Timing Diagram

4.2.12 Address Selection Logic

Drawing D16 illustrates the logic used to recognize a DMC-11 microprocessor address. The JK flop OSSYN sets upon address recognition. The assigned address is configured with ten switches, each switch associated with a unique address bit. Address bits A3 through A12 are available for configuration, allowing an addressing range of four words within the DMC-11 microprocessor.

The logic compares the switch code with the respective address bits using two comparator chips whose outputs are wire "OR" connected. When the inputs are equal bit for bit, the comparator outputs go high. The remaining hi-order address bits, A13-A17, all of which must be true are ANDed with MSYN to produce a set condition on the inputs to OSSYN. On the next clock (CK) OSSYN sets. BOSSYN is asserted 130 nsec later, acknowledging bus master.

4.2.13 NPR Control Logic

Initiation of an NPR cycle is under complete control of the microprogram. To initiate an NPR cycle, a MOVE microinstruction referencing the OUT*BUS is executed specifying a unique output address of 10_8. This microinstruction along with BALU0(1) sets NPR RQ. Once NPR RQ sets, the logic then executes the NPR cycle asynchronously with respect to the microprogram.

Figure 4-17 illustrates the timing sequence for an output NPR cycle. The requirements for execution are: (1) a UNIBUS address, (2) data gated to the UNIBUS, (3) a DATO defined via C0 and C1, and (4) assertion of master sync (MSYNC). Drawing D15 contains the relevant logic. The addressed unit (slave) then recognizes its address and interprets the control lines. After gating the data from the data bus, the slave acknowledges receipt of the data by asserting slave sync (SSYN).

Refer to Figure 4-17 and drawing D15 for the following discussion. First, the standard handshake for bus control takes place. The timing begins with the assertion of NPR RQ(1) which in turn generates the bus signal DATA BUS NPR L. The central processor then responds with DATA BUS NPG IN H, provided no other device was already queued up for bus mastership. In such a situation, the microprocessor simply stalls until its priority is the highest of all requesters. When BUS NPG IN H does arrive at the microprocessor, it resets BUS NPR L following a delay of 70 ns. In addition, further propagation of the grant signal to other devices is prevented by the microprocessor. The grant signal also sets selection acknowledge (SACK), acknowledging to the central processor the reception of the grant signal. At this point, the microprocessor becomes the next bus master as soon as the current master relinquishes control. The microprocessor monitors busy to determine when to take control.

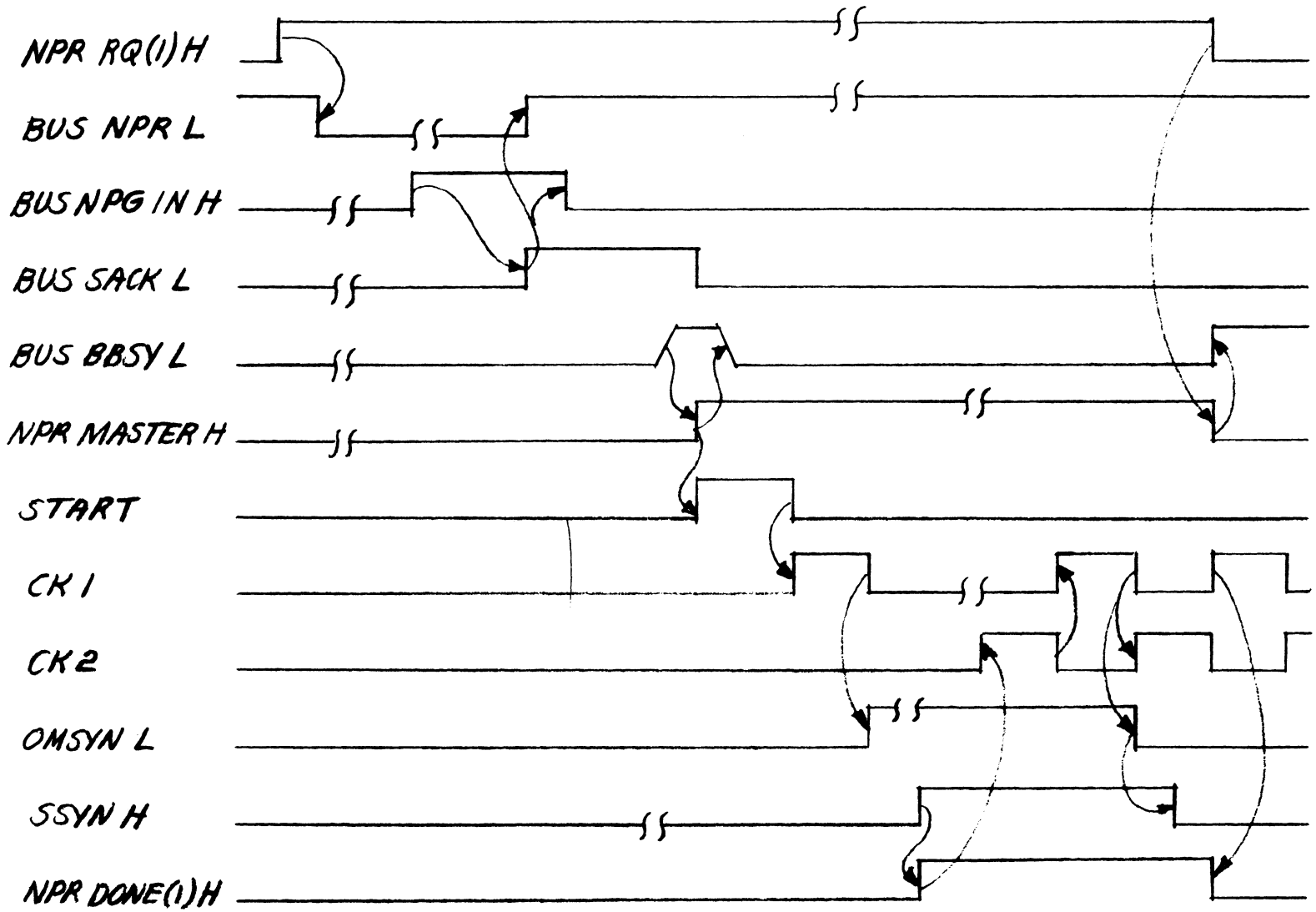


Figure 4-17 NPR Output Timing Diagram

The actual NPR cycle or data transfer takes place during the time the microprocessor is bus master. Once the previous bus master relinquishes the bus and provided the microprocessor is queued up to be next [SACK(1) H], the microprocessor then takes control by asserting BUS BBSY L. Simultaneously, SACK is reset and NPR MASTER is set. The NPR cycle now begins.

The address is gated to the UNIBUS with NPR MASTER as well as C0 and C1. Data, on the other hand, is gated to the data bus under control of DATA → BUS L. These three conditions occur simultaneously during an OUTPUT NPR cycle. On the leading edge of NPR MASTER, a 250 nsec delay is triggered, at the conclusion of which BUS MSYN is asserted.

INPUT NPR cycle timing is illustrated in Figure 4-18 and for the most part is similar to the OUTPUT NPR cycle. In this case the microprocessor waits for the addressed slave to respond with data and BUS SSYN. The microprocessor then loads the data into the multiport RAM and acknowledges receipt by dropping BUS MSYN terminating the NPR cycle.

4.2.14 Interrupt Control Logic

The execution of an interrupt cycle is accomplished through a two-phase operation. First, bus mastership must be gained and then the actual INTERRUPT cycle execution.

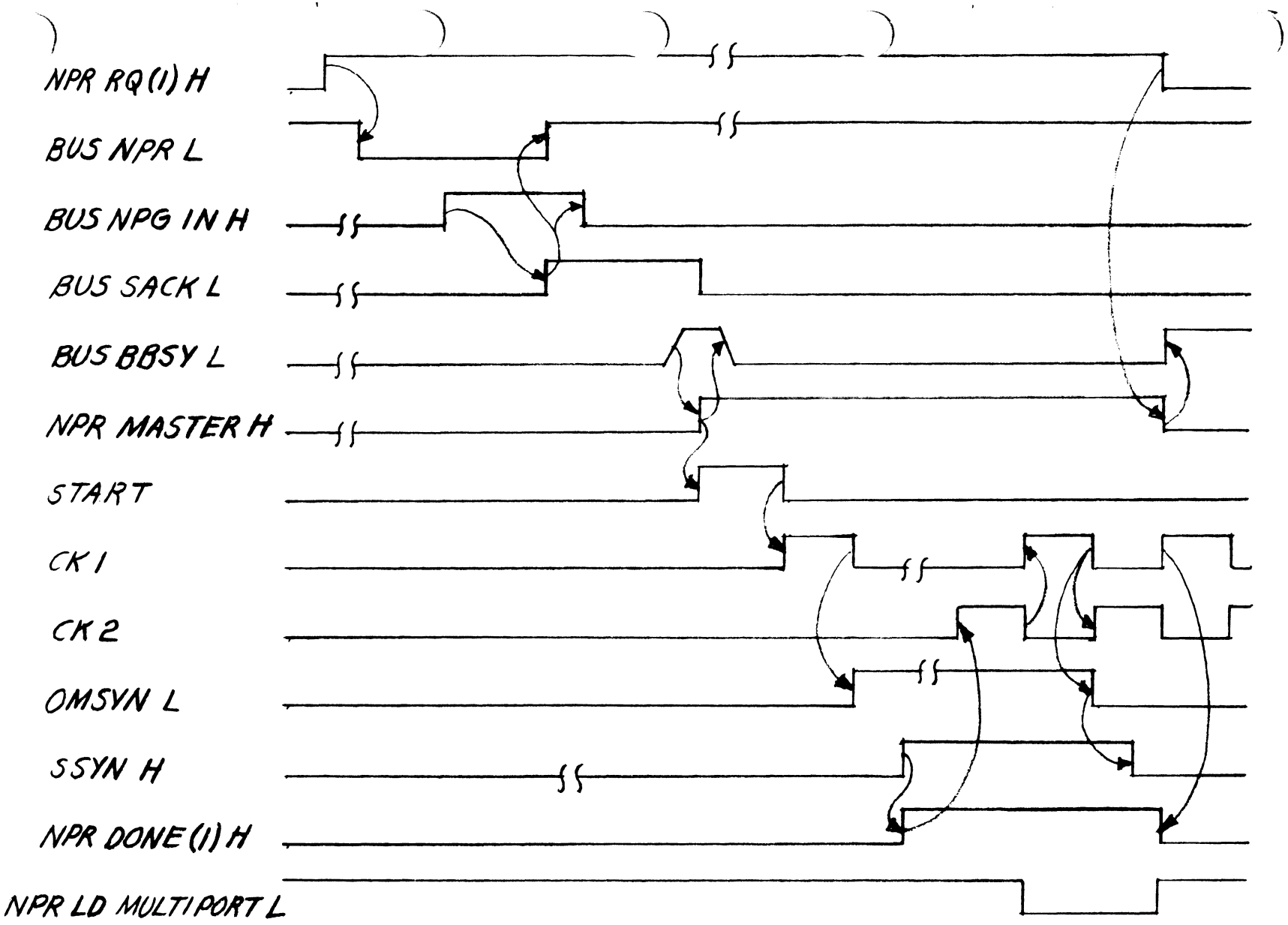


Figure 4-18 NPR Input Timing Diagram

Figure 4-19 illustrates the timing sequence for execution of an INTERRUPT cycle. The entire process is initiated with the assertion of BR RQ. A MOVE microinstruction having an output address of 05_8, with bit seven of the operand equal to a one, sets BR RQ.

With both BR MASTER and SACK still reset, the condition is satisfied to generate BUS BR L. BUS BR L feeds the Priority Card which in turn generates the appropriate bus request signal to the central processor. The interrupt logic then stalls, awaiting the bus grant signal from the PDP-11 Processor. When bus grant arrives (BUS B BG IN), it sets SACK and resets BUS BR L. At this point, the microprocessor becomes the next bus master and again stalls until the current bus master relinquishes bus control. When this happens, BR MASTER (1) H sets which begins the INTERRUPT cycle. BUS INTR L is asserted while simultaneously the microprocessor logic places the interrupt vector address onto the data bus. The operation is concluded when the central processor acknowledges receipt of the interrupt with BUS SSYN.

4.2.15 Line Unit Interface

Interconnection between the microprocessor and the line unit is done via the LINE UNIT interface. The interface cable carries 33 signal lines between the two units, of which eight originate in the LINE UNIT and the remaining 25 in the microprocessor.

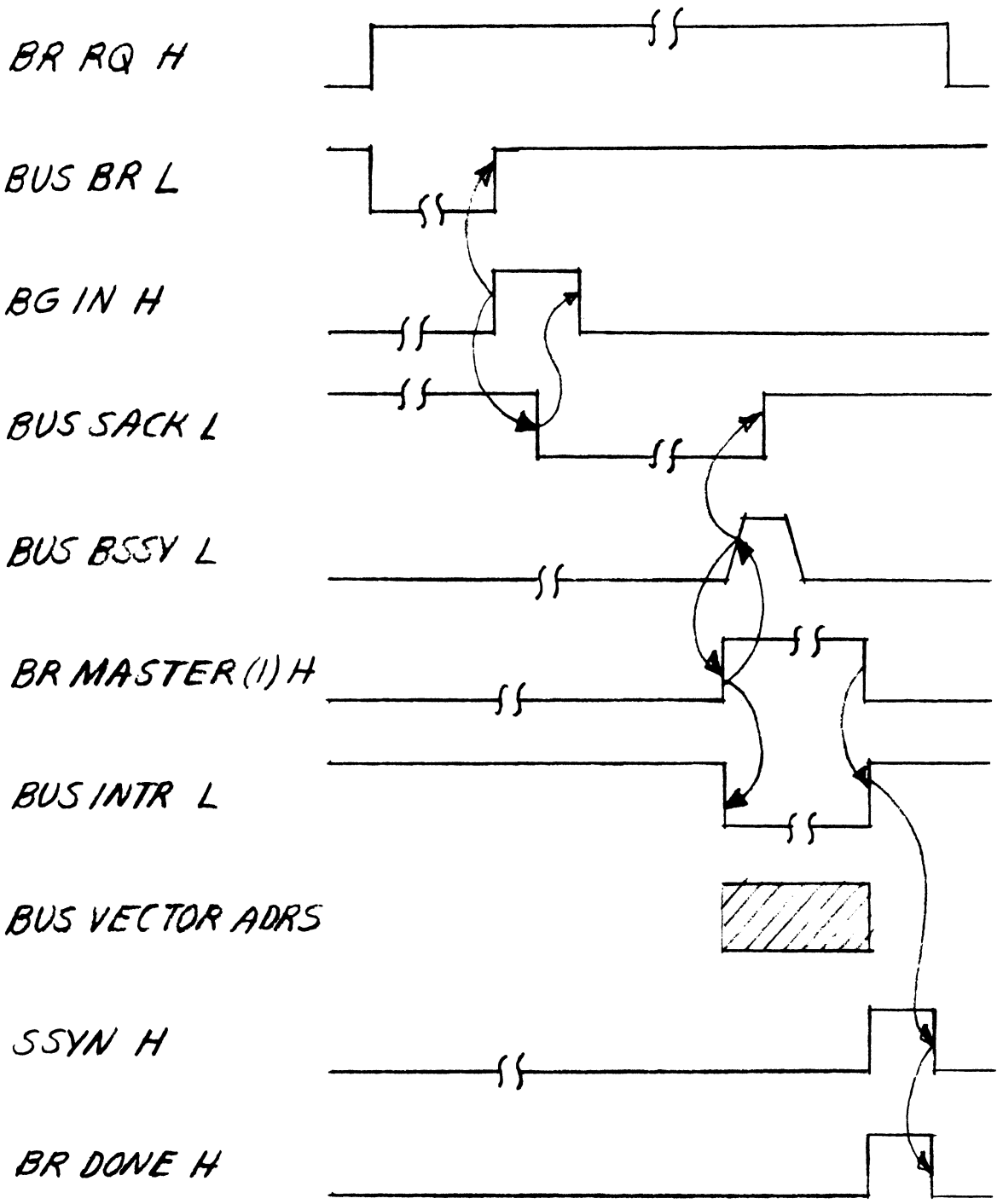


Figure 4-19 Interrupt Timing Diagram

4.2.15.1 LU IBUS 0 H - LU IBUS 7 H

These eight lines are the Line unit input bus. This bus originates in the line unit and delivers data to the microprocessor from the register addressed by the microword (CROM 0 - CROM 2).

4.2.15.2 BALU0L - BALU7L

These eight lines are the microprocessor output bus. The data goes to the buffered ALU register then to the interface on to the line unit.

4.2.15.3 IBR L/IBR*H

This signal acknowledges to the line unit receipt of data, and is asserted during T240.

4.2.15.4 BT240

BT240 is used to synchronize the line unit with the microprocessor.

4.2.15.4 OBW L

This signal is the output data strobe. The line unit uses this signal to clock or strobe the output data into an internal register.

4.2.15.5 OUT * L

This signal when asserted low indicates to the line unit to direct the output data to the *OUT BUS instead of the OUT BUS.

4.2.15.6 CROM 0 L - CROM 7 L

These CROM bits are the input/output address used by the line unit to address internal registers. The output registers are addressed by CROM 0-3 and the input registers with bits CROM 4-7.

4.2.15.7 Clear

This signal initializes the line unit placing it in a reset state.

4.2.15.8 LU Loop

With this diagnostic function, the line unit loops data from its transmitter to its receiver.

4.2.15.9 Step LU

This signal commands the line unit to advance one cycle.

4.2.16 Typical System Timing

Typical system timing is illustrated in Figures 4-20 and 4-21. Figure 4-20 shows applicable signals used in an output cycle along with typical line unit logic. Note that the address is valid from T90 through T300 while the data for the cycle in question is valid from approximately T270 through the next T240. The data is strobed into an internal register with the low to high transition of OBW L.

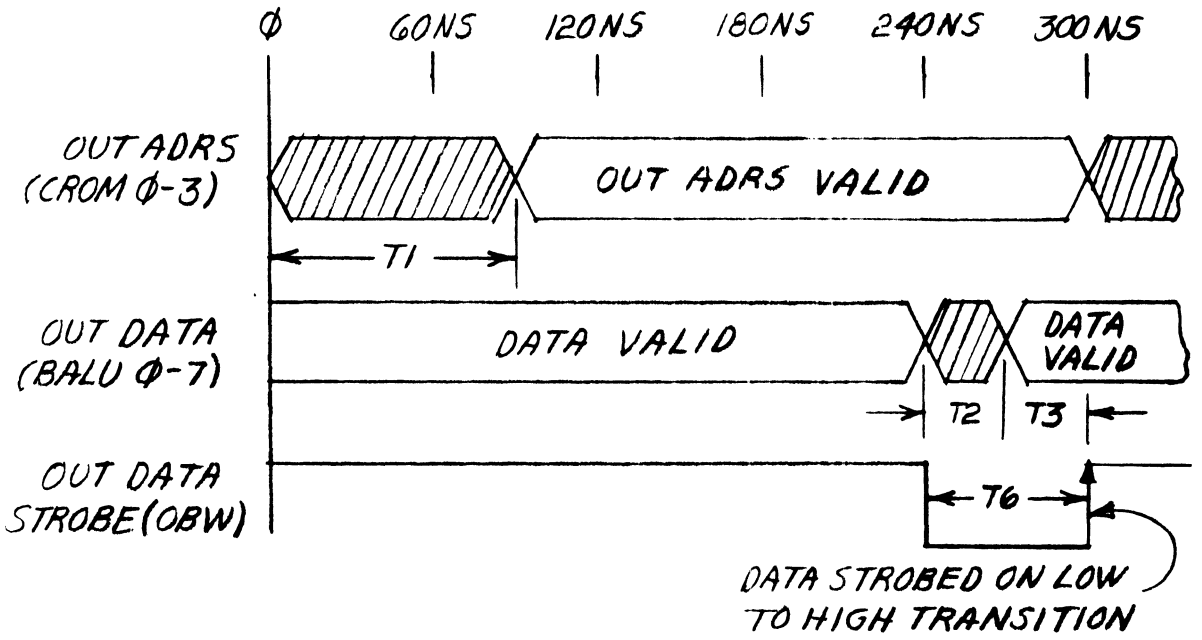


Figure 4-20 Typical Output Bus Timing

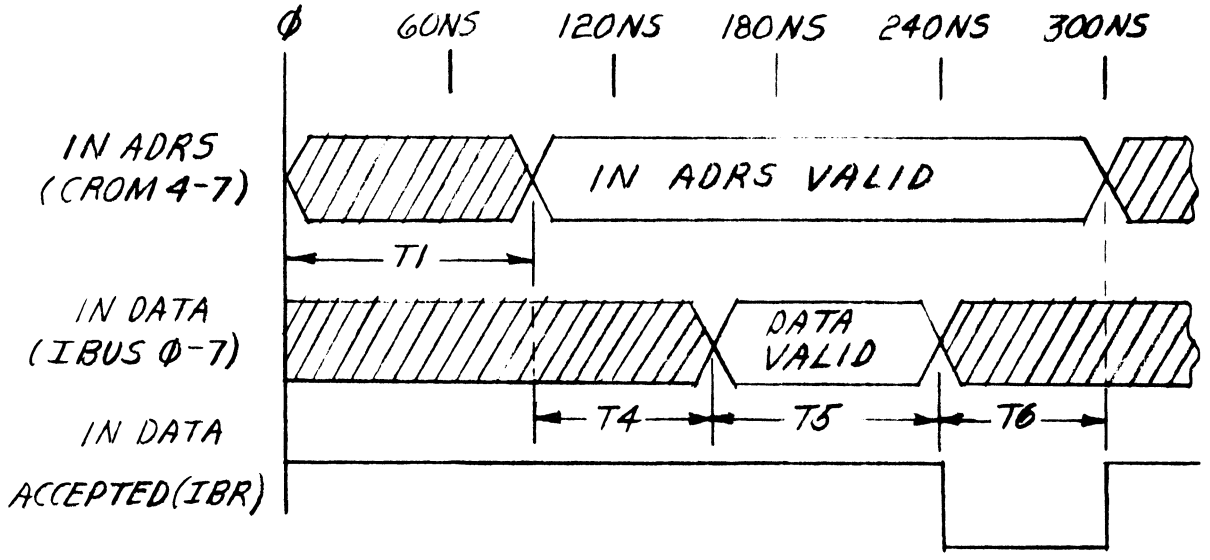


Figure 4-21 Typical Input Bus Timing

Input bus timing is illustrated in Figure 4-21. Again, the address is valid for the same period as in the output cycle (T90 - T300). The line unit then places data on to the input bus during its T5 time, which approximately coincides with T160 - T240 in the microprocessor.

CHAPTER 5

MAINTENANCE

5.1 SCOPE

This chapter lists required test equipment and provides a complete description of DMC11 microprocessor preventive and corrective maintenance procedures.

5.2 Maintenance Philosophy

Basically, DMC11 microprocessor maintenance consists of preventive and corrective maintenance procedures, diagnostic programs, and a maintenance log. The preventive maintenance procedures are performed regularly in an attempt to detect any deterioration due to aging and any damage caused by extremes in environmental conditions or improper handling of the module and the interconnect cable. The corrective maintenance procedures are performed to isolate the failure to the microprocessor module and correct the failure primarily through module replacement. Only under unusual circumstances should component level isolation and component replacement be considered as a corrective maintenance procedure. The maintenance log is used to record all maintenance activities for future reference and analysis.

5.3 Preventive Maintenance

Preventive maintenance consists of tasks performed at periodic intervals to ensure proper equipment operation and minimum

unscheduled down-time. These tasks consist of visual inspection, operational checks and running diagnostics.

The preventive maintenance schedule depends on the environmental and operating conditions that exist at the installation site. Under normal conditions preventive maintenance should be performed every 3 months. However, relatively extreme conditions of temperature humidity and mechanical shock may demand more frequent maintenance.

5.4 Test Equipment Required

Maintenance procedures for the DMC11 microprocessor require the standard test equipment and diagnostic programs listed in Table 5-1.

5.5 Corrective Maintenance

The corrective maintenance procedures are designed to aid the service technician in determining that the failure is in the DMC11 microprocessor module and correcting the failure through module replacement. Essentially this involves running the microprocessor diagnostics and observing any error messages. For those situations where component level repair is required, the basic microprocessor test MAINDEC-11-DZDMC has been divided into 140_8 subtest to sequentially test each section of logic.

The free-running test MAINDEC-11-DZDMG should be used after corrective maintenance to ensure that the microprocessor functions correctly using its control ROM (CROM), at full speed.

5.5.1 Diagnostic Modes

The DMC11 microprocessor can be tested using two basic modes during servicing. These are:

1. Maintenance Mode
2. System Test (free running)

5.5.1.1 Maintenance Mode

Maintenance mode can be invoked using selected bits in the upper byte of the first CSR. These can be used to halt the microprocessor (clear bit 15), step the microprocessor (set bit 8), examine the current CROM location (assert bit 10 and examine CSR 6), override the current CROM instruction with a different instruction and execute that instruction (assert bits 8 and 9 and load CSR 6 with the new instruction).

NOTE

Be sure that B SEL1 LOCK OUT (switch 9, E76) is OFF to allow access to the maintenance bits in the CSR.

With this switch ON, however, it is still possible to clear the microprocessor by setting bit 14 in the first CSR.

5.5.1.2 System Test

This mode tests the functionality of the microprocessor running at full speed and utilizing the control ROM.

NOTE

Be sure the RUN INHIBIT switch (switch 7 E76) is OFF to utilize this mode and for normal operating conditions.

Table 5-1

Test Equipment Required

Equipment	Manufacturer	Designation
Multimeter	Triplett or Simpson	Model 630-NA or 260
Oscilloscope	Tektronix	Type 453
X10 Probes (2)	Tektronix	P6008
Module Extenders	DEC	W984 (Double) W987 (Quad) NOTE For a hex board us a double and a quad.
Diagnostic Tapes	DEC	DZDMC, DZDMG

APPENDIX A

PDP-11 MEMORY ORGANIZATION AND ADDRESSING CONVENTIONS

The PDP-11 memory is organized in 16-bit words consisting of two 8-bit bytes. Each byte is addressable and has its own address location; low bytes are even numbered and high bytes are odd numbered. Words are addressed at even numbered locations only and the high (odd) byte of the word is automatically included to provide a 16-bit word. Consecutive words are therefore found in even numbered addresses. A byte operation addresses an odd or even location to select an 8-bit byte.

The Unibus address word contains 18 bits identified as A(17:00). Eighteen bits provide the capability of addressing 256K memory locations each of which is an 8-bit byte. This also represents 128K 16-bit words. In this discussion, the multipler K equals 1024 so that 256K represents 262,144 locations and 238K represents 131,072 locations. The maximum memory size can be used only by a PDP-11 processor with a memory management unit that utilizes all 18 address bits. Without this unit, the processor provides 16 address bits which limits the maximum memory size to 64K (65,536) bytes or 32K (32,768) words.

Figure A-1 shows the organization for the maximum memory size of 256K bytes. In the binary system, 18 bits can specify 2^{18} or 262,144 (256K) locations. The octal numbering system is used to

designate the address. This provides convenience in converting the address to the binary system that the processor uses as shown below.

The highest 8K address locations (760000-77777) are reserved for internal general registers and peripheral devices. There is no physical memory for these addresses; only the numbers are reserved. As a result, programmable memory locations cannot be assigned in this area; therefore, the user has 248 bytes or 124K words to program.

A PDP-11 processor without the memory management unit provides 16 address bits that specify 2^{16} or 65,536 (64K) locations (Figure A-2). The maximum memory size is 65,536 (64K) bytes or 32,768 (32K) words. Logic in the processor forces address bits A(17:16) to 1s if bits A(15:13) are all 1s when the processor is master to allow generation of addresses in the reserved area with only 16-bit control.

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	ADDRESS BIT
0	0	1	0	0	1	1	1	1	1	1	0	0	0	0	0	1	0	BINARY
	1		1		7		6		0		1							OCTAL

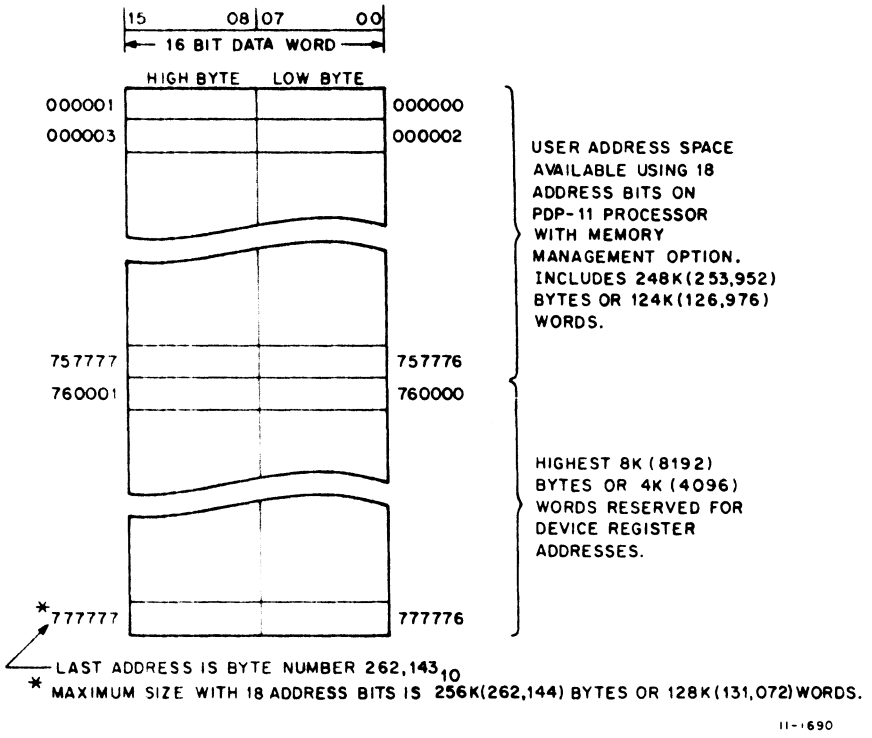


Figure A-1 Memory Organization for Maximum Size Using 18 Address Bits

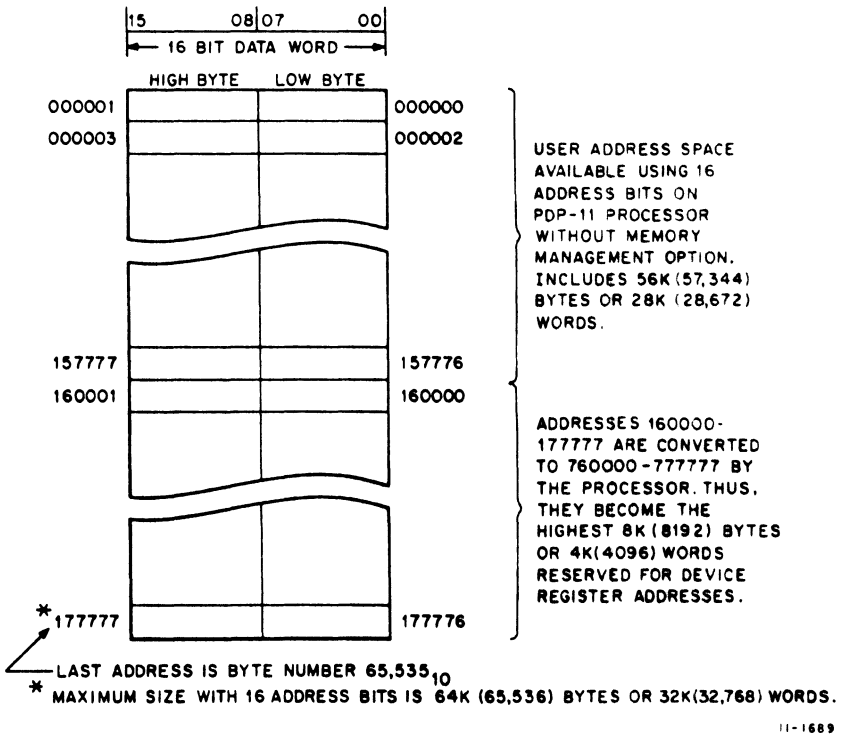


Figure A-2 Memory Organization for Maximum Size Using 16 Address Bits

Bit 13 becomes a 1 first at octal 160000 which is decimal 57,344 (56K). This is the beginning of the last 8K bytes of the 64K byte memory. The processor converts locations 160000-177777 to 760000-777777 which relocates these last 8K bytes (4K words) to the highest locations accessible by the bus. These are the locations that are reserved for internal general register and peripheral device addresses; therefore, the user has 57,344 (56K) bytes or 28,672 (28K) words to program.

Memory capacities of 56K bytes (28K words) or under do not have the problem of interference with the reserved area, because designations less than 160000 do not have a binary 1 in bit A13. No addresses are converted and there is no possibility of physical memory locations interfering with the reserved space.

PDP-11 core memories are available in 4K or 8K increments. The highest location of various size core memories are shown below.

Memory Size		Highest Location
K-Words	K-Bytes	(Octal)
4	8	017777
8	16	037777
12	24	057777
16	32	077777
20	40	117777
24	48	137777
28	56	157777

ADDENDUM TO

DMC11 IPL MICROPROCESSOR MAINTENANCE MANUAL

(EK-DMCMP-MM-001)

October 1976

Changing the Option Designations

This manual refers to the DMC11-AD Microprocessor (M8200-YA module) that is used with all versions of the local and remote DMC11 line units.

The DMC11-AD option has been replaced by two options. One is DMC11-AR (M8200-YA module), which is used only with the remote line unit. The other is DMC11-AL (M8200-YB), which is used only with the local line unit. The line unit option designations have not been changed.

The following table describes the mircoprocessor and line unit options.

Option	Module	Description	Prerequisite
DMC11-AR	M8200-YA	Microprocessor with DDCMP microcode for remote applications (M8201 Line Unit)	PDP-11
DMC11-AL	M8200-YB	Microprocessor with DDCMP microcode for local applications (M8202 Line Unit)	PDP-11
DMC11-DA	M8201	Line unit with cable for for EIA interface	DMC11-AR

DMC 11-FA	M8201	Line unit with cable for V35/DDS interface	DMC11-AR
DMC11-MA	M8202-YA	Line unit with 1M bps integral modem	DMC11-AL
DMC11-MD	M8202-YO	Line unit with 56K bps integral modem	DMC11-AL

Programming Sections

Sections 3.4.2.1 through 3.4.2.15 have been substantially revised and the corrected version is attached:

Replace page 3-6

Retain pages 3-7 through 3-13

Replace pages 3-14 through 3-37

Retain the rest of the chapter.

The port is loaded by the PDP-11 on input transfers and by the microprocessor on output transfers.

The format and contents of the data port depend on the transfer type (TYPE I or TYPE O).

In discussing the data port message formats, it is sometimes more convenient to use word designations (SEL4 and SEL6) rather than byte designations (BSEL4-7).

There are four formats.

1. Buffer address/character count input and output (BA/CC I and BA/CC O).
2. Base input (BASE I)
3. Control input (CNTL I)
4. Control output (CONL O)

1. BA/CC I and BA/CC O Format

   The formats for BA/CC I and BA/CC O are the same (Figure 3-1). SEL4 contains the least significant 16 bits (0-15) of the 18 bit buffer address. The two most significant bits (16 and 17) of this address are contained in bits 14 and 15 of SEL6. The remaining 14 bits (0-13) of SEL6 contain the character count in positive notation not 2's complement notation.

The microprocessor can stack a maximum of seven BA/CCs each for input and output. This number is based on the size of the core tables (BASE) in the PDP-11 memory which is limited to 256 bytes.

For input operations, BA/CC I supplies new message buffers to the microprocessor.

For output operations, BA/CC O returns the buffers to the PDP-11 that were successfully transferred to the microprocessor.

2. BASE I Format

SEL4 and bits 14 and 15 of SEL6 provide the first address of a reserved block of addresses in the PDP-11 memory (Figure 3-1). The block size is 256 bytes. Upon assigning the BASE address to the microprocessor, the PDP-11 program must not modify any locations within the assigned block.

Bit 13 of SEL6 is called RESUME. If this bit is cleared, the microprocessor initializes the base table and protocol. If set, the microprocessor resumes operation as specified by the contents of the base table.

MESSAGE

ENQ	ΦΦ5
STRT	ΦΦ6
FLAGS	3ΦΦ
FILL	ΦΦΦ
FILL	ΦΦΦ
ADDRESS	ΦΦ1
BCC (16 bit)	? 75
	? 95

11 000 000

C C

---

should receive a STACK

same as stack except byte 1 is

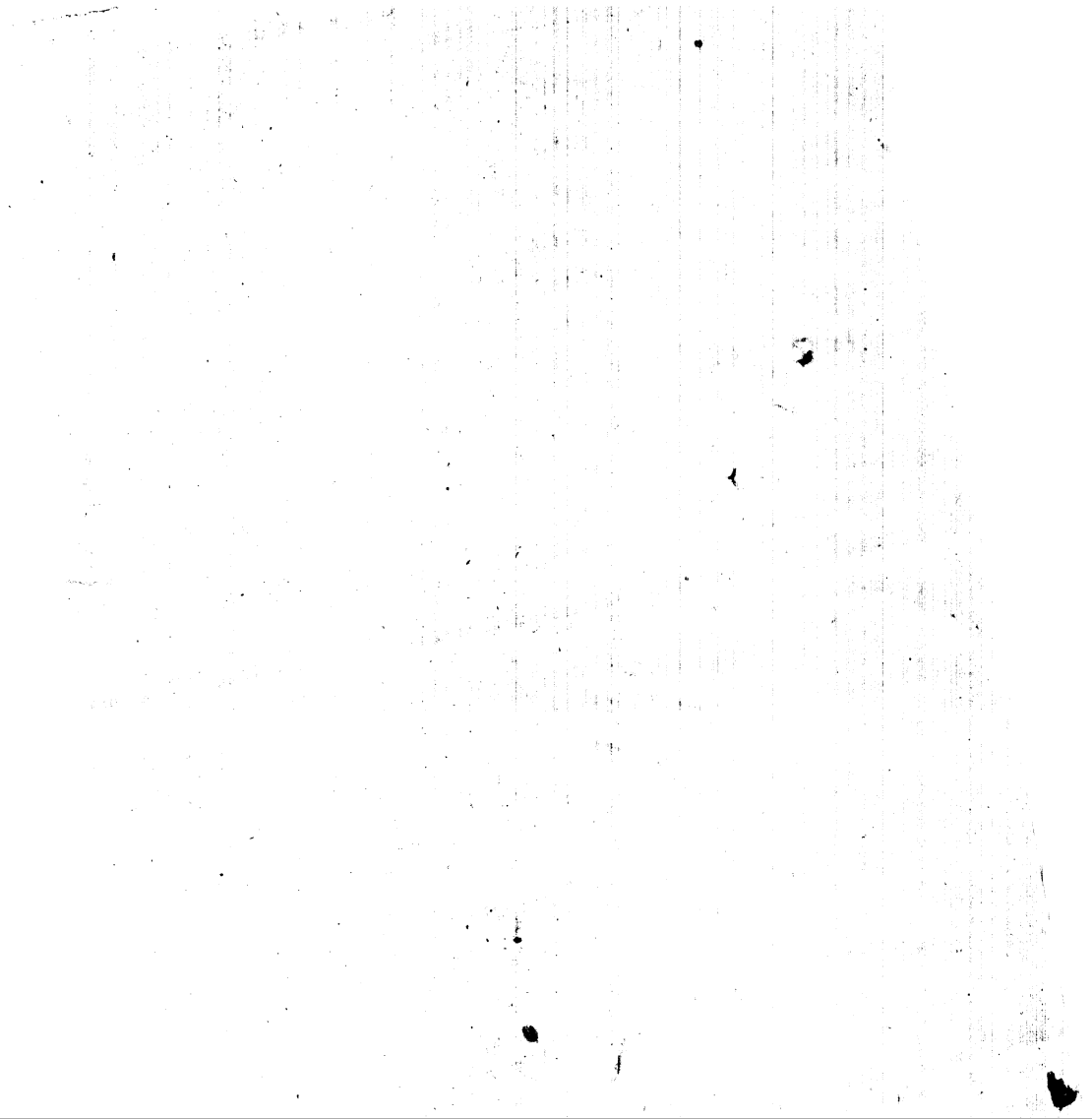
→ instead of 6

CD	8
RTS	4
CTS	5
DTR	20
DST	6

4 → 8 → 5

6 → 14 → 22

24 → 15



3. CNTL I Format

The CNTL I format provides a means of implementing certain control functions (Figure 3-1).

SEL4 and bits 14 and 15 of SEL6 contain the address for this format. The control bits are located in SEL6 as shown below.

Bit	Name	Description
0-7	SECONDARY ADDRESS (SEC ADRS)	These bits define the address of a station in the secondary mode under the discipline of DDCMP.
8	DDCMP MAINTENANCE (DDCMP MAINT)	With this bit set, the microprocessor enters the DDCMP maintenance mode where it remains until it is subsequently initialized.
9	RESERVED	
10	DDCMP HALF DUPLEX (DDCMP HD)	With this bit set, DDCMP half duplex operation is selected. With this bit cleared, DDCMP full duplex operation is selected. This bit must be used with bit 11.

Bit	Name	Description
11	DDCMP (SECONDARY DDCMP SEC)	With this bit set, DDCMP half duplex secondary station operation is selected. With this bit cleared, DDCMP half duplex primary station operation is selected. Not used for full duplex.
12, 13	RESERVED	

4. CNTL O Format

The CNTL O format provides a means of informing the PDP-11 program of error conditions involving the DMC11 hardware, PDP-11 program, communications channel, or the remote station.

SEL4 and bits 14 and 15 of SEL6 contain the address of this format. The control bits are located in SEL6 as shown below (Figure 3-1).

Bit	Name	Description
0	DATA CHECK (DATA CK)	When set, this bit indicates that a retransmission threshold has been exceeded.
1	TIME OUT	When set, this bit indicates that the microprocessor has received no

Bit	Name	Description
1 (Cont.)	TIME OUT (Cont.)	response from the remote end of the link for 21 seconds.
2	OVERRUN (ORUN)	When set, this bit indicates that a message was received but no buffer is available to receive it.
3	DDCMP MAINTENANCE RECEIVED (DDCMP MAINT RECD)	When set, this bit indicates that a message in the DDCMP maintenance format has been received and that the protocol operation has entered the maintenance state.
4	LOST DATA	When set, this bit indicates that the received message is longer than the supplied buffer.
5	RESERVED	
6	DISOONNECT	When set, this bit indicates that an off to on transition of the modem Data Set Ready lead has been detected.
7	DDCMP START RECEIVED (DDCMP START RECD)	When set, this bit indicates that a DDCMP Start message was received when the protocol was in the Running or Maintenance state.

Bit	Name	Description
8	NON EXISTANT MEMORY (NON EX MEM)	When set, this bit indicates that a Unibus address time out has occurred.
9	PROCESSOR ERROR (PROC ERR)	When set, this bit indicates that the PDP-11 program has performed a procedural error.

3.4.3 Input Transfers

Whenever the data port is not in use, it is subject to being seized by the microprocessor for use in an output transfer. Therefore, the PDP-11 program must request the microprocessor to assign it the port before proceeding with an input transfer. It must also specify the type of input transfer (a transmit buffer, a receive buffer, control information, etc.) so the microprocessor can make appropriate preparations.

The PDP-11 program should set bits 0-2 of BSELO to indicate the type of transfer and then set bit 5 Request In (RQI) to request the port. These bits may be set by a single instruction. The microprocessor responds by setting bit 7, Ready In (RDYI) when the port has been assigned to the PDP-11 program. When RDY1 has been set, the PDP-11 program should load the desired data into the data port (BSEL4-7). Then, it should clear RQI. The microprocessor takes the data and clears RDYI which completes the transfer.

Bit 6 of BSELO, Interrupt Enable Input (IEI), controls whether the PDP-11 program receives an interrupt (to Vector XX0) when the microprocessor has set RDYI. The microprocessor responds to RQI immediately (within 10 microseconds) when operating at speeds below 1 megabit or at 1 megabit when either the transmitter or receiver is idle. It is most efficient for the PDP-11 program to have interrupts disabled and simply scan RDYI one or more times until the microprocessor has set it. While the PDP-11 program is waiting it must be prepared to accept an output transfer because the microprocessor may have seized the port in the meanwhile.

The microprocessor cannot service certain types of input transfers immediately. For example, the PDP-11 program may attempt to queue more than 7 buffers for transmission. In these cases, it is convenient to use interrupts. If the PDP-11 program finds RDYI clear after several scans, it can enable interrupts by setting IEI with a BIS or MOV instruction. The DMC11 interrupts the PDP-11 (to Vector XX0) when the microprocessor has set RDYI. The PDP-11 program gets the interrupt in all cases, even if the microprocessor had already set RDYI at the time the program sets IEI. The program can bypass any scanning if IEI is set when the program sets RQI.

NOTE

The PDP-11 program should not begin a new input transfer until the previous transfer

until the previous transfer has been completed, as indicated by the microprocessor clearing RDYI. The microprocessor does this within 10 microseconds after the program has cleared RQI. If the PDP-11 program wishes to begin a new transfer immediately, it should check that RDYI has been cleared before setting RQI. This can be done by scanning RDYI until it has been cleared.

3.4.4 Output Transfers

The microprocessor initiates an output transfer when it has status or error information to transfer to the PDP-11 program or it wishes to return a full buffer on reception or an empty buffer on transmission. The microprocessor can initiate an output transfer at any time the data port is free; that is, not assigned to the PDP-11 program for an input transfer and not in use for a previous output transfer. However, if the PDP-11 has initialized the DMC11 by setting MASTER CLEAR or generating the INIT signal on the UNIBUS, the microprocessor does not generate any output transfer until it has been initialized by the PDP-11 program.

The microprocessor loads status or error information into the data port (BSEL4-7) and sets bits 0-2 of BSEL2 to indicate the format and significance of the data. It then sets bit 7 of BSEL2,

Ready Out (RDYO) to indicate to the PDP-11 programs that data is available. In response to RDYO setting, the PDP-11 program should note the type of output transfer as specified in bits 0-2 of BSEL2 and read the data in the data port. When the PDP-11 program has sampled all the data, it must complete the output transfer by clearing RDYO. This frees the data port for a subsequent transaction.

If the PDP-11 program wishes, it can enable interrupts on output transfers by setting bit 6 of BSEL2, Interrupt Enable Output (IEO). If IEO is set, the DMC11 interrupts the PDP-11 (to Vector XX4) after the microprocessor has set RDYO. Since the PDP-11 program usually does not know when an output transfer will occur (for example, when a message will be received) an efficient PDP-11 program ordinarily enables interrupts on output transfers.

NOTE

The PDP-11 program must respond to RDYO being set by reading the data and clearing RDYO. Failure to do this prevents the data port from being freed. If the PDP-11 program has requested an input transfer by setting RQI, it must be prepared to respond to an output transfer prior to being given RDYI. If the PDP-11 program fails to respond to RDYO, it never gets RDYI. The PDP-11 program should

not spin on RDYI in a loop that doesn't also test RDYO unless interrupts on output transfers are enabled, and the loop executes at a lower priority level than the DMC-11 interrupts level.

3.4.5 Initialization

The power up sequence and UNIBUS INIT signal initialize the DMC11. The PDP-11 program can accomplish the same effect by setting MASTER CLEAR in BSEL1. Each of these procedures restart the microprocessor to the beginning of its microprogram. In this state, the microprocessor does not send or receive messages on the serial line or generate output transfers.

When the PDP-11 program whiches the DMC11 to function, it must perform an input transfer that specifies the base address of a 128 word table in PDP-11 memory, which is called the Base Table. The PDP-11 program requests the BASEI transfer by setting TYPEI to 11. In response to RDYI, the program loads the low order 16 bits of the address into SEL4 and the high order 2 bits of the address into bits 15 and 14 of SEL6. If the DDCMP protocol operation is to be initialized, the RESUME bit (bit 13 of SEL6) must be clear.

Once the PDP-11 has specified a base address, the 128 word base table belongs to the microprocessor until the DMC11 is master cleared by INIT or MASTER CLEAR. The PDP-11 program may examine

the contents of the base table (for example, error counters relating to protocol operation) but must not alter its contents.

By supplying a base address with the RESUME bit clear, the microprocessor is conditioned to respond to the DDCMP start-up sequence received from the remote system. However, the microproce microprocessor does not initiate the start-up sequence on its own accord unless the PDP-11 program supplies a buffer of data to be transmitted.

If the DMC11 is connected to a half-duplex channel, the PDP-11 program must now perform an input transfer using the Control In format and set the Half Duplex bit (HD) in SEL6 (bit 10). In addition, the program must specify whether the DMC11 is to operate as a half duplex secondary station (3 second timer) or a half duplex primary station (1 second timer) by setting or clearing the Secondary bit (SEC) in SEL6 (bit 11). A half duplex link must have one primary station and one secondary station. The only difference between the two is in the length of time spent before retransmitting in case of errors. Half duplex operation may be specified at any time by a Control In transfer to accomodate switching to a half duplex back up communications channel. The DMC-11 options containing the integral modem must be specifically strapped for half duplex operation in addition to requiring the Control In transfer.

3.4.6 DDCMP Start Up

Before data messages may be transmitted or received, the DDCMP start-up sequence must be completed to make certain both ends of the link are correctly initialized and to place the protocol in the running state. Either end may initiate the start sequence or both ends may do so simultaneously. If the PDP-11 program supplies a buffer of data to be transmitted, the local DMC11 initiates the start sequence.

The PDP-11 program may ignore the details of the start sequence. However, one important property of the sequence is significant. Once the local DMC11 has entered the running state, it detects and flags as an error the fact that the other end has initiated the start sequence. As a result, the PDP-11 program receives a Control Out transfer with SEL6 bit 7 (DDCMP START REC'D) set. If this happens, the PDP-11 program knows that the other end of the link has restarted. The PDP-11 program should initialize the DMC11 and begin again.

3.4.7 Data Transmission

When the PDP-11 program wishes to transmit a buffer of data, it clears bits 1 and 0 of BSELO to indicate a Buffer Address/ Character Count In transfer and clears bit 2 of BSELO (INI/O) to specify that this is a full buffer to be transmitted. It then requests an input transfer by setting RQI. In response to RDYI,

it loads SEL4 with the low order 16 bits of the buffer address, bits 15 and 14 of SEL6 with the high order bits of the address, and bits 13 to 0 of SEL6 with the 14 bit character count. Buffers from 1 to 16,383 bytes long may be used for local operation. For remote operation buffers should be limited to a practical maximum of about 512 bytes, depending on the error rate of the communications facilities. Each buffer corresponds to a single DDCMP data message.

When the message has been successfully transmitted and an acknowledgement received, the microprocessor initiates an output transfer with bits 1 and 0 of BSEL2 clear to indicate the Buffer Address/Character Count Out (BA/CC O) format. Bit 2 (OUT I/O) is clear to indicate that a successfully transmitted buffer has been returned to the program.

The PDP-11 program may queue up to seven buffers for transmission by supplying buffers to the microprocessor faster than it returns them. An attempt to queue more than seven buffers forces the microprocessor to delay granting the request for the input transfer until a buffer has been returned.

NOTE

The PDP-11 program should not request an input transfer that supplies a transmit buffer if 7 are already outstanding, unless it is certain

that the other end of the link can supply enough buffers for reception. In particular, if two PDP-11's connected by DMC11's attempt to queue up 8 buffers, while no receive buffers are queued, they become deadlocked and must initialize their DMC11's.

3.4.8 Data Reception

When the PDP-11 program has an empty buffer it wishes to fill with received data, it clears bits 1 and 0 of BSELO to indicate a BA/CC I transfer and sets bit 2 of BSELO (IN I/O) to specify that an empty buffer has been made available for reception. It then requests an input transfer by setting RQI. In response to RDYI, it loads SEL4 and SEL6 with the buffer address and character count in the same format as for transmission. The character count must be large enough to accommodate the longest message expected.

When a message has been successfully received and stored in the buffer, the microprocessor initiates an output transfer with bits 1 and 0 of BSEL2 clear to indicate the BA/CC O format. Bit 2 (OUT I/O) is set to indicate a full buffer has been received. SEL4 and SEL6 contains the address of the buffer and the actual number of characters received.

If a message is received when no receive buffer is available, the microprocessor informs the PDP-11 by means of a Control Out transfer

with bit 2 of SEL6 (O'RUN ERR) set. The other end of the link is informed of the error and automatically retransmits the message. The PDP-11 program should supply a buffer as soon as possible.

The PDP-11 may queue up to seven empty buffers for reception by supplying them to the microprocessor faster than it returns buffers. An attempt to queue more than seven buffers forces the microprocessor to delay granting the request for input transfer until a full buffer has been returned.

NOTE

The PDP-11 program should not request an input transfer than supplies a buffer for reception if 7 are already outstanding, unless it is certain that the other end of the link is supplying buffers for transmission.

3.4.9 Control Out Transfers

The microprocessor informs the PDP-11 program of unusual or error conditions involving the communications channel, remote end of the link, DMC11 hardware or PDP-11 program by means of an output transfer with bit 1 of BSEL2 clear and bit 0 set indicating a Control Out (CNTL)) transfer. SEL6 contains bits that indicate the error condition. Some errors are advisory in nature and normal operation may continue. Others are fatal and require the PDP-11 program to initialize the DMC11.

Bit 0 (DATA CK) indicates that a retransmission threshold has been exceeded. (More than 7 consecutive retransmissions have occurred for transmission or reception.) This indicates a defective communications channel or that the other end of the link has failed to supply a buffer for reception. The PDP-11 can examine error counters in the base table for more details of the error. This is a non-fatal error. Should the cause of the error be corrected, normal operation continues with no messages lost in either direction. This error may appear repeatedly until the condition is corrected or until the DMC11 is initialized. Transient errors corrected before 7 retransmissions are not reported to the PDP-11 program but are counted in the base table.

Bit 1 (TIME OUT) indicates that the microprocessor has received no response from the remote end of the link for a specified period (21 seconds). This indicates a broken communications channel or a failure at the other end of the link (possibly a power failure). Like DATA CK, this is a non-fatal error which can occur repeatedly.

Bit 2 (O'RUN) indicates that a message was received but no buffer was available. This is a non-fatal error. The PDP-11 program can prevent this error from recurring repeatedly by supplying a buffer.

Bit 3 (DDCMP MAINT REC'D) indicates that a message in the DDCMP Maintenance format was received and that the protocol operation has entered the Maintenance state.

Bit 4 (LOST DATA) indicates that a message was received that is longer than the buffer supplied by the PDP-11 program. This is a fatal error.

Bit 6 (DISCONNECT) indicates that an on to off transition of the modem Data Set Ready lead has been detected (remote operation only). This is a non-fatal error. For dial-up operation, the PDP-11 program must consider the possibility that a new caller has connected to the DMC11, if this is required by security considerations.

Bit 7 (DDCMP START REC'D) indicates that a DDCMP Start message was received when the protocol was in the Running or Maintenance states. This indicates that the remote computer has initialized its end of the link. This is a fatal error. The PDP-11 program may initialize the DMC11 if it wishes to start over and complete the start-up sequence.

Bit 8 (NON EX MEM) indicates that a UNIBUS address time out has occurred. This could have been caused by the PDP-11 program specifying an invalid base address, buffer address, or count, that was stored illegally in the base table or the PDP-11 memory is defective. This is a fatal error.

Bit 9 (PROC ERR) indicates a procedure error on the part of the PDP-11 program. The requested input transfer can not be honored due to a programming error. This error can be caused by requesting

a BA/CC before supplying a base address, requesting a base address a second time, or specifying an invalid code in BSEL0 bits 1 and 0. This is a fatal error.

3.4.10 Maintenance Messages

A special DDCMP message format, the Maintenance message, is used for down line loading, restarting, or otherwise maintaining satellite computer systems. Messages in this format are subject to error checking but are unsequenced, unacknowledged, and not retransmitted automatically by the DMC11. Transmission is always half duplex.

Maintenance messages can only be sent and received while the microprocessor is in the DDCMP maintenance state. The PDP-11 program may cause the microprocessor to enter this state by a CNTL I transfer with bit 8 of SEL6 (DDCMP MAINT) set. The microprocessor enters the Maintenance state if a maintenance message is received. In this case, the microprocessor performs a CNTL O transfer with DDCMP MAINT REC'D set in SEL6 to indicate the state change and availability of a maintenance message.

Once in DDCMP maintenance mode, maintenance messages can be sent and received similarly to data messages. On transmission, the data portion of the message is taken from the buffer with the DMC11 generating the header and CRC's. On reception only, the data portion is placed in the buffer. Messages not in DDCMP

maintenance format or having incorrect CRC's are simply discarded.

The data portion of the maintenance message may contain any data that is desired, but ordinarily it conforms to the Digital Maintenance Operation Protocol (MOP) formats. When a host computer wishes to restart a satellite computer system, it must send the appropriate MOP messages as described below.

In order to leave Maintenance mode, the PDP-11 program must initialize the DMC11 and supply a base address with the RESUME bit clear.

3.4.11 Remote Load Detect and Down Line Load

Whenever the microprocessor is running, it is constantly scanning the serial line for a DDCMP maintenance message containing an ENTER MOP MODE data field. What happens when this particular message is received depends on the setting of two switch packs on the DMC11 line unit. Depending on the setting of these switches, the DMC11 will either commence down line loading in MOP mode, trigger the PDP-11 to begin executing a program in a read only memory (ROM) bootstrap (BM873, M9301, etc.) or simply pass the data to the PDP-11 as an ordinary maintenance message. In case a ROM bootstrap is triggered, switches on the line unit specify an 8 bit word offset to the bootstrap address space.

The data portion of the ENTER MOP MODE message is 5 bytes long. The first byte contains the decimal number 6. The remaining 4 bytes contain the same 8 bit value. This value is specified by a switch pack on the DMC11 line unit and serves as a password to protect against inadvertant recognition of the ENTER MOP MODE message.

If an ENTER MOP MODE message is recognized and the switches specify to commence down line loading, the DMC11 microprocessor takes over the PDP-11 computer system. All peripherals on the system are initialized by an INIT sequence and the processor is placed into a tight loop where it remains until control is transferred to a program loaded down the line.

In response to the ENTER MOP MODE message, the DMC11 sends a REQUEST MOP SECONDARY MODE message in DDCMP maintenance format containing a data field three bytes long that contains the decimal numbers 8.12,1. This informs the remote end that the ENTER MOP MODE message was received.

The remote end should now send a MEMORY LOAD WITH TRANSFER ADDRESS message in DDCMP maintenance format. The first two bytes are zero, the next 4 bytes are an 18 bit memory address right justified, followed by a memory image to be loaded and four bytes of transfer address.

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