pdp11

KMC11 general purpose microprocessor user's manual

digital

KMC11 general purpose
microprocessor
user's manual

PRELIMINARY

This document was set on DIGITAL's DECset-8000 computerized typesetting system.

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CHAPTER 1

INTRODUCTION

1.1   SCOPE

This manual provides the information necessary to install and

operate the KMC11-A General Purpose Microprocessor. It is organized

into five chapters and one appendix as follows:

    Chapter 1 - Introduction.

    Chapter 2 - Installation.

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1.2   GENERAL DESCRIPTION OF KMC11-A MICROPROCESSOR

The KMC11-A (Module M8204) is a Unibus compatible general purpose

microprocessor with writeable control storage. It is used primarily

to reduce the input/output load on the CPU in a PDP-11 system;

hence, the KMC11 functions more like a data handler than a data

processor.

The functions performed by the KMC11 are determined by the

microprogram contained in its instruction memory. The architecture

of the KMC11 does not allow it to modify its own instruction area.

The KMC11 is a stand alone device and can be programmed by the

user to perform an appropriate task. The KMC11 can also be used with
a DMC11 Synchronous Line Unit. The KMC11 can be microprogrammed to
control the line unit for character type protocols such as DEC's
Digital Data Communications Message Protocol (DDCMP) or bit stuff
protocols. There are two basic versions of the line unit. One is the
local unit (M8202) which interconnects PDP-11 computers by coaxial
cables in local network applications. The other is the remote unit
(M8201) which interconnects remote PDP-11 computers via modems and
common carrier facilities. There are two variations of each line
unit; however, the 1 M bps version is not recommended for non-Digital
programming. These four options are listed in Table 1-1.

Table 1-1 DMC11 Line Unit Options

Line Unit	Interface	Speed	Modem
DMC11-MA Local	Coaxial Cable (6000 ft. max)	1 Mbps*	Integral
DMC11-MD Local	Coaxial Cable (18,000 ft. max)	56 Kbps	Integral
DMC11-DA Remote	RS-232-C or CC1TT V.24	Up to 19.2 Kbps	Bell 208,209, or equivalent

Table 1-1 DMC11 Line Unit Options (Cont)

Line Unit	Interface	Speed	Modem
DMC11-FA Remote	CC1TT V.35	Up to 250 Kbps	GTE/Lenkurt L500A-5, WEC0 (Bell) 500A L1/5, or equivalent modem used on the Digital Data service

*Not recommended for non-DEC programming

The KMC11 is an enchanced version of the DMC11 with writeable
control storage in place of ROMs. The KMC11 has increased main
memory and provisions for performing consecutive NPRs without
relinquishing Unibus mastership. Comparative KMC11/DMC11 specifications
are shown in Table 1-2.

Table 1-2 KMC11/DMC11 Comparative Specifications

Function	DMC11 (M8200)	KMC11-A (M8204)
Cycle time for complete instruction	300ns or 330ns if multiport access	300ns or 330ns if multiport access
Main Memory	256 bytes	1K bytes

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Table 1-2 KMC11/DMC11 Comparative Specifications (Cont)

Scratch Pad	16 bytes	16 bytes
Instruction length	16 bits	16 bits
Control ROM	1K words	N/A
Control RAM	N/A	1K words
Data paths	8 bits	8 bits
NPR address	18 bits	18 bits
Interrupt Vectors	2	2
CSR (RAM) microcode defined	7 bytes	7 bytes
ALU functions	16	16
NPR data transfers	byte or word	byte or word
CSR transfers	byte or word	byte or word
Program timer	1.0 second	50 µs
Multiple NPRs	no	yes (use NPR Control Register bit 1)

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Table 1-2 KMC11/DMC11 Comparative Specifications (Cont)

MAR load high	no	yes
CSR Sel 0 bit 13 (WRITE CRAM) functional)	no	yes
Assert AC L0	yes	yes
I/0 DMC11 Line Unit compatible	yes	yes
MAR 8 and 10 status bits	no	yes
Module size	hex	hex
Voltage/current	+5V at 5A	+5V at 5A

Figure 1-1 shows a typical KMC11/peripheral device configuration. The KMC11 is microcoded to service a normally interrupt-driven device in the flag mode; that is, interrupts turned off. A buffer pointer and character count field are transfered from the PDP11 program to the KMC11. The data is then moved to/from the peripheral device via NPRs initiated by the KMC11. In effect, a character-by-character device is converted to a high throughput block transfer device by combining it with a microcoded KMC11.
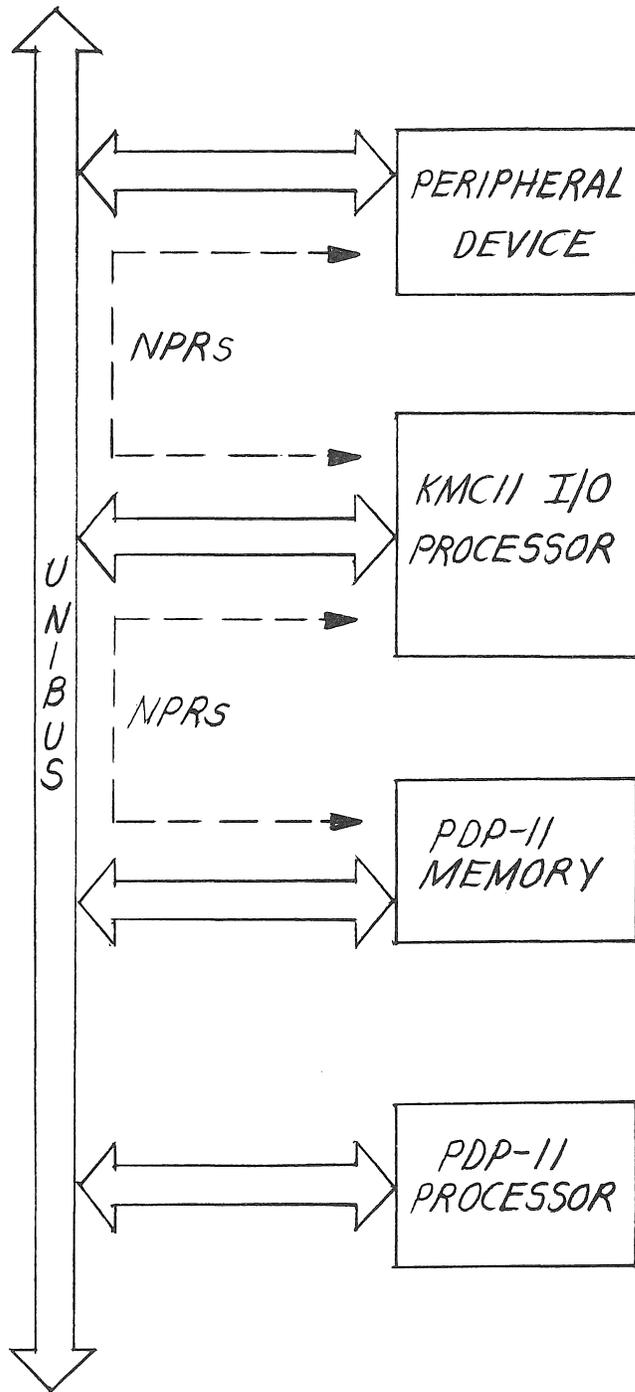
Figure 1-1   KMC11-A I/O Microprocessor

Figure 1-2 shows a typical KMC11/DMC11 Local Line Unit application.
Local stations are interconnected by a single coaxial cable for
half-duplex operation or two cables for full-duplex operation.

Figure 1-3 shows a typical KMC11/DMC11 Remote Line Unit application.
Remote stations are interconnected via modems that use common
carrier facilities.

Figure 1-4 is a simplified block diagram of the KMC11 Microprocessor.
It shows the basic controlling elements of the KMC11 and how it is
located functionally between the Unibus and its I/0 port. The KMC11
I/0 port interfaces with the device (line unit, etc) through a one
foot cable. The KMC11 interfaces with the Unibus and, because of its
self-contained micro-program and fast operating speed, the input/output
load on the PDP-11 Processor is reduced significantly.

The KMC11 performs direct memory access (DMA) operations using non
processor request (NPR) transactions. It also performs interrupt
transactions. Communications between the PDP-11 Processor and the
microprocessor's Unibus Control and Status Registers (CSRs) is done
through data in (DATI) transactions for reading and data out (DATO)
or data out byte (DATOB) transactions for writing.

The major functional areas of the KMC11 Microprocessor are:
1. Main Memory (MEM) and Memory Address Register (MAR) - The
    main memory is a 1024 word-by-8 bit random access memory
    that is the KMC11 data storage area. This area cannot be
    used for instruction storage nor can the stored data be
    executed as an instruction.
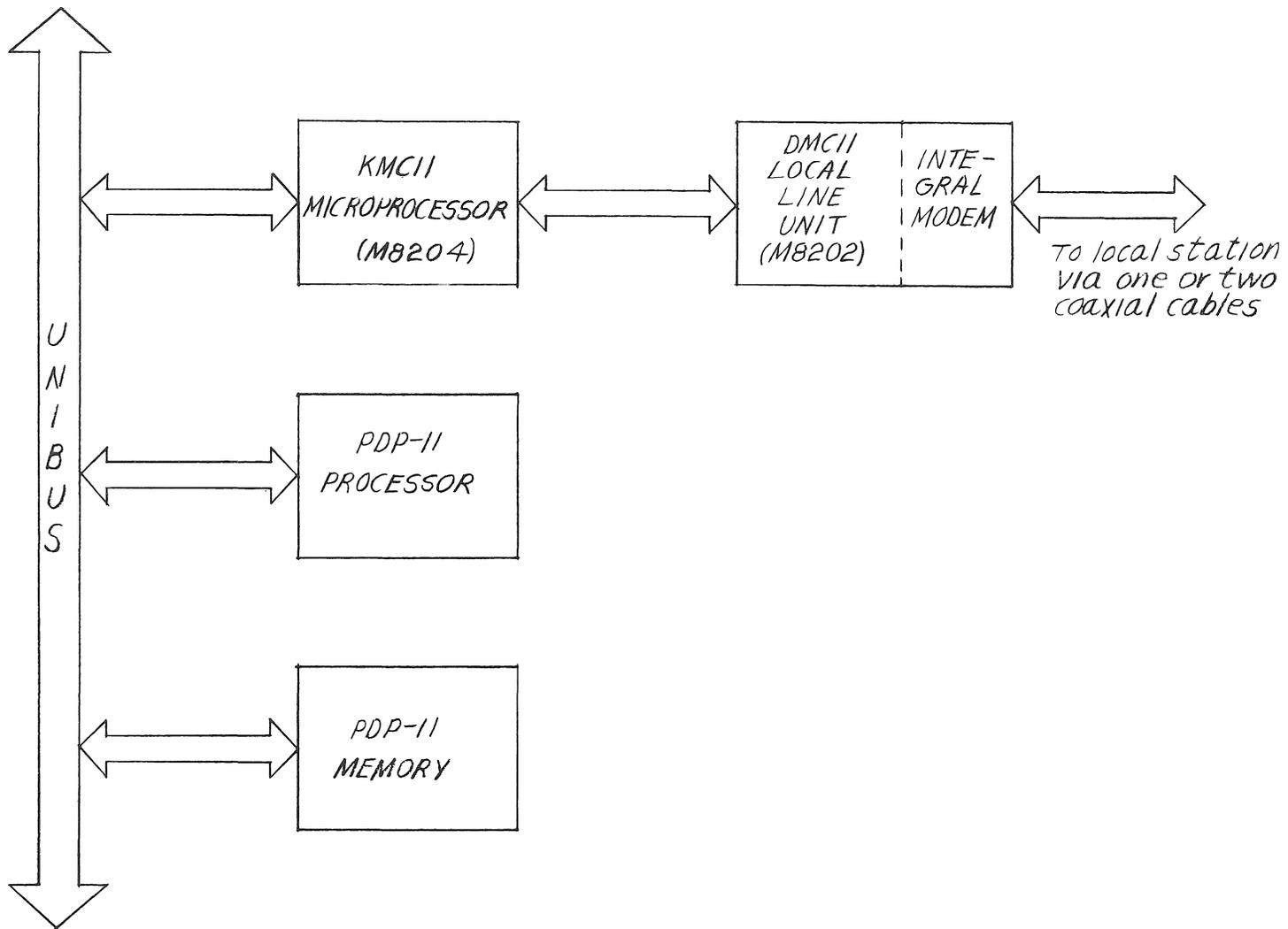
Figure 1-2   KMC11 Local Line Unit Interface
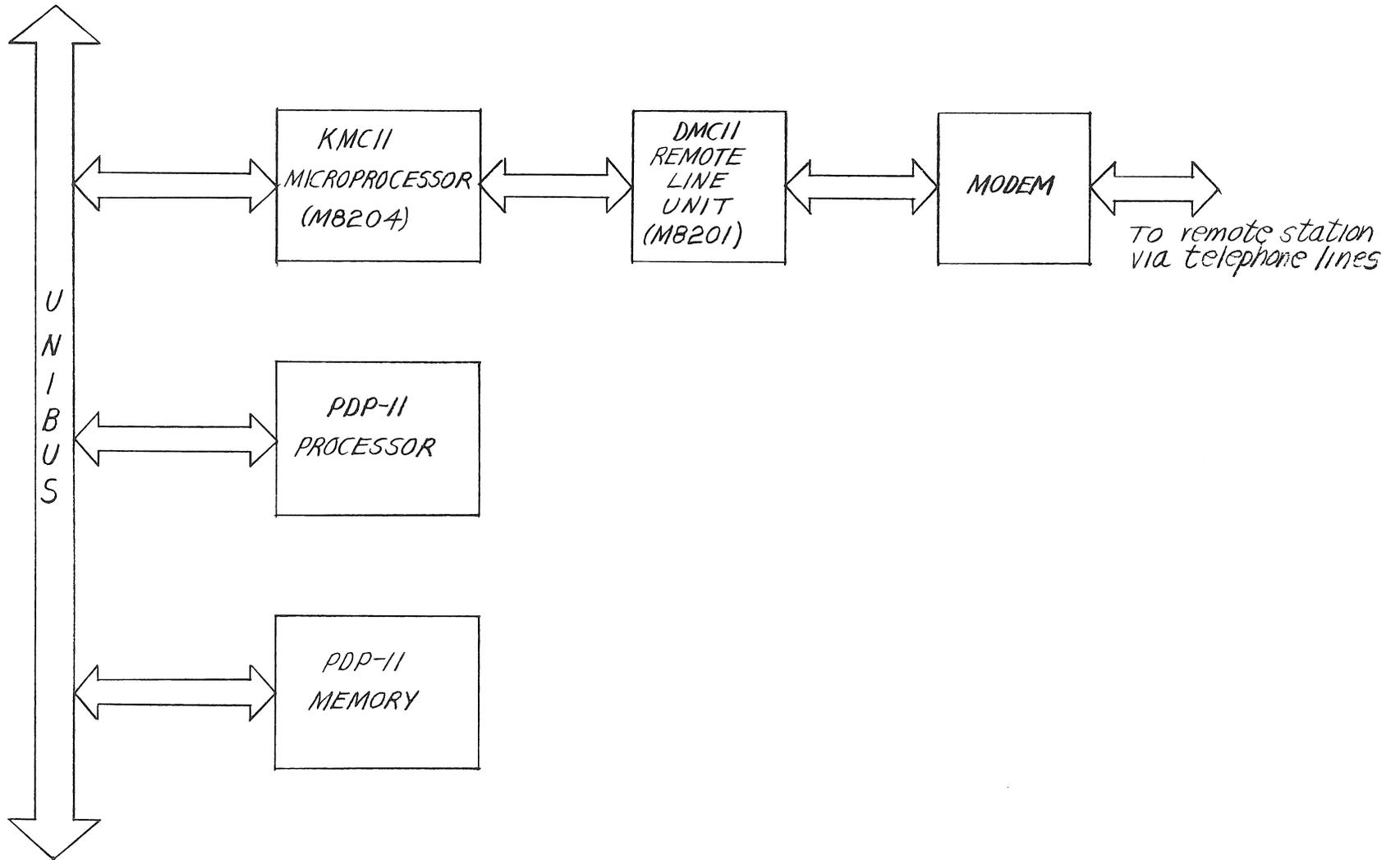
Figure 1-3   KMC11 Remote Line Unit Interface
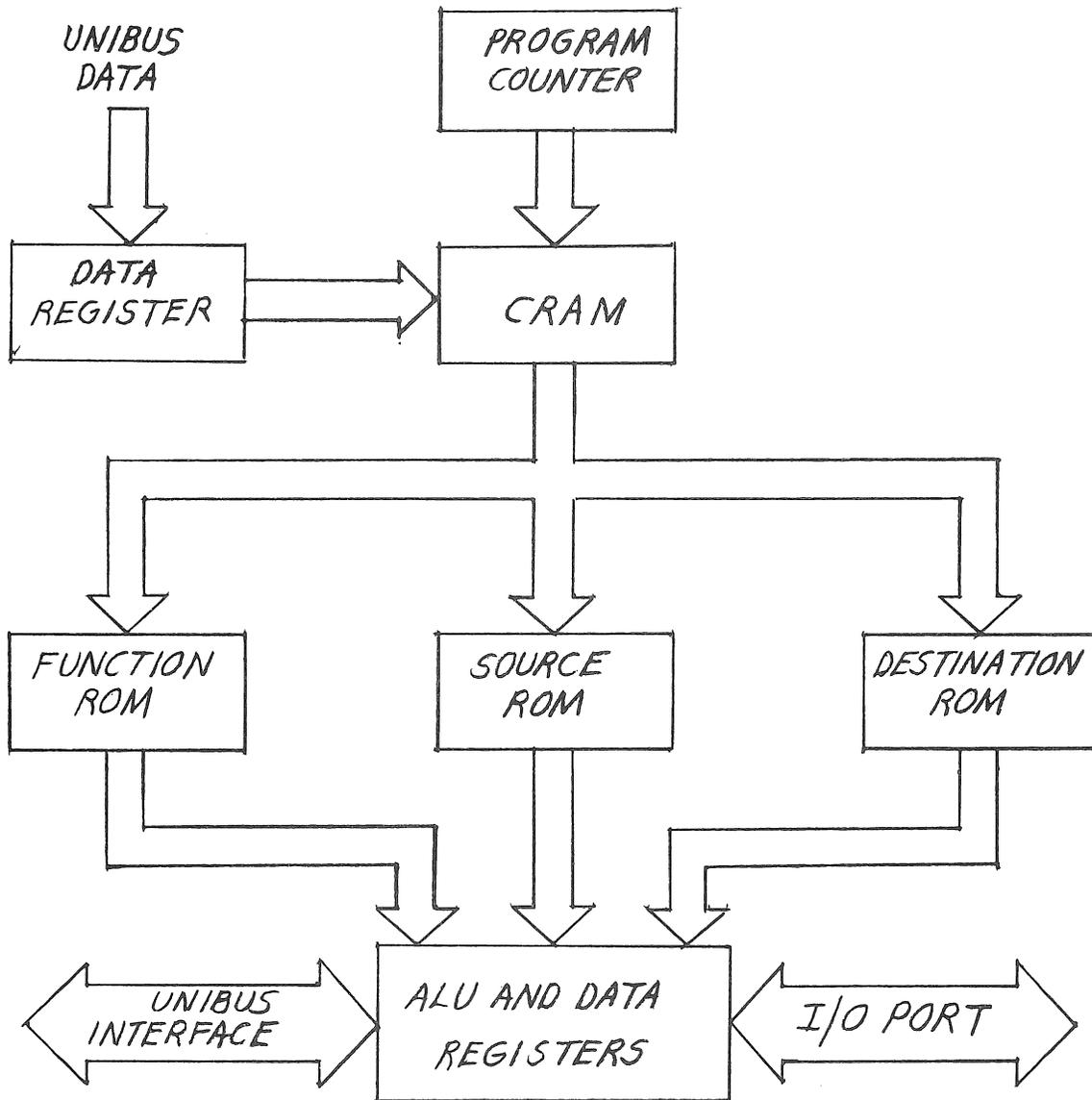
Figure 1-4   Microprocessor Simplified Block Diagram

This memory is addressed by the outputs of the
Memory Address Register.

2. Branch Register (BRG) - This 8-bit register is used
    as a temporary data register for branch determination
    and for a rotate right operation. It.has three modes
    of operation: load, shift right, and hold. Input data
    comes from the buffered ALU except during shifting when
    only the BRG's most significant bit is sourced from
    the ALU.

    Output data goes to the B input of the ALU via the
    data multiplexer.

3. Program Counter, Maintenance Address Register and
    PC Address Multiplexer - The program counter outputs
    are used to address the control random access memory
    (CRAM). The program counter can be parallel loaded,
    in case of a BRANCH, or incremented. The outputs of the
    program counter go to the PC address multiplexer before
    going to the CRAM. During normal operation, the mux
    selects the PC outputs. During micro-program loading or
    CRAM verifying, the mux selects Unibus data, via the
    maintenance address register, as the source for the
    CRAM addresses.

4. Control RAM, RAM Data Register, and Maintenance
    Instruction Register - The control RAM is a 1024

by -16 bit random access memory that is the micro-program storage area. The RAM data register is used to load the CRAM from the Unibus. The maintenance instruction register is loaded from the Unibus. Its outputs are wire-ORed with the CRAM outputs so that the maintenance instruction register contents can be substituted for the CRAM during servicing of the KMC11.

5. Data Multiplexer and Source Read Only Memory (SROM) - The data multiplexer (DMUX) is an 8-bit wide 8 line-to-1 line multiplexer. Its 8-bit output goes to the B input of the Arithmetic Logic Unit (ALU). Input selection for the DMUX is controlled by the SROM which is a 32-by-8 bit read only memory. The SROM also determines if a move instruction is to be executed.

6. Scratchpad Memory and Addressing Multiplexer - The scratchpad memory (SP) is a 16-by-8 bit read/write memory that is used for temporary storage of data. An operand can be presented to the A input of the ALU only through the scratchpad memory. SP addressing is done through a multiplexer. During normal operation, the addressing is controlled by the CRAM. During an output transfer, SP address 0000 is automatically presented to the A input of the ALU.

7. Arithmetic Logic Unit and Function Read Only Memory (FROM) - The arithmetic logic unit (ALU) allows the microprocessor to perform arithmetic and logic operations

on its A and B inputs. The FROM, which is a 32-by-8 bit
read only memory, controls up to 16 functions to be
performed by the ALU. The carry output (C Bit) of the
ALU is connected to a flip-flop to store the carry
indication if it occurs during a move or if it is forced
by the FROM.

The AB output (Z Bit) of the ALU is connected to a
flip-flop to store the indication of equality of the
A and B inputs of the ALU if it occurs during a MOVE
instruction.

8.   Multiport RAM and Associated Logic - The multiport
     RAM is a random access memory that contains all the
     KMC11 status registers except two. They are the NPR
     Control Register and the Miscellaneous Register. The
     multiport RAM has two ports (A and B) that can be
     accessed simultaneously for a read operation; however
     only the A port can be written into. The associated logic
     consists of read/write control and addressing
     multiplexers which allow access to the multiport RAM by
     the microprocessor and the PDP-11 Processor. The
     multiport RAM contains the control and status registers
     that are accessible by both the KMC11 and the PDP11
     program. It also contains the NPR buffer pointers and
     data buffers that are accessible only by the KMC11.

9.   System Clock - The clock provides clock pulses for the
     microprocessor. It generates a series of five non

overlapping 60 ns pulses during a time interval of 300 ns.
It is started by the PDP11 program when bit 15 of CSR
SEL0 is set. Its operation is suspended when the multiport
RAM is being accessed by the KMC11 for a write operation
while the PDP11 has a write operation in progress. Suspension
of operation also occurs if an NPR is in progress and the
KMC11 tries to read or write the multiport RAM.

10. NPR Request and Control Logic - This logic allows the
micro-processor to initiate an NPR under microprogram
control and assume Unibus mastership so it can transfer
data to or from the PDP-11 memory.

11. Interrupt Control Logic - This logic allows the
microprocessor to interrupt the PDP-11 Processor and
cause vectoring to either of two programmable locations
in the floating vector address space. The vector
address is switch selectable.

The KMC11 interrupt priority can be level 4, 5, 6 or 7;
however, it is shipped as a level 5 device.

12. Address Selection Logic - This logic consists of switches
to specify the microprocessor device address plus logic
to decode this address. This logic also decodes the
selected register and type of Unibus transaction requested.
Using these factors, the logic generates the appropriate
control signals to implement a read or write operation as
directed by the Unibus control lines.

CHAPTER 2

INSTALLATION

2.1   SCOPE

This chapter provides the information necessary to install and
check out the KMC11 Microprocessor as a stand alone device or
in combination with the DMC11 Synchronous Line Unit.

2.2   UNPACKING AND INSPECTION

The microprocessor or microprocessor/line unit combination
arrives at the customer site in one of two ways; either as
part of a complete computer system or as an add-on option.
When it arrives as an add-on option, the microprocessor module,
line unit module (if ordered), and associated mounting hardware
and cables arrive packaged in a single carton. Inspect the
carton visually for any signs of physical damage. Included in
the contents of the carton are the following:

    1.   M8204 KMC11 Microprocessor Module.

   *2.   M8201 or M8202 DMC11 Line Unit Module.

   *3.   BC08S-1 Cable to interconnect microprocessor
          and line unit.

   *4.   BC05C-25 Cable for DMC11-DA (M8201) Line Unit
          only. This option has an EIA/CC1TT V.24 interface.

*5. BC05Z-25 Cable for DMC11-FA (M8201) Line Unit

       only. This option has a CC1TT V.35 interface.

*6. H325 Test Connector for DMC11-DA (M8201) only.

*7. H3250 Test Connector for DMC11-FA (M8201) only.

*8. 12-12528 Coaxial Cable Test Connector (M8202 only).

 9. MAINDEC-11 DZKCC KMC11 Microprocessor Basic W/R

       and Data Paths Static Tests.

10. MAINDEC-11 DZKCA KMC11 Free Run Micro Diagnostics.

*11. MAINDEC-11 DZKCE DMC11 Line Unit Static Character

        Protocol Tests.

*12. MAINDEC-11 DZKCF DMC11 Line Unit Static Bit Stuff

        Protocol Tests.

*13. MAINDEC-11 DZKCG Line Unit Free Running Tests Under

        DDCMP Mode.

14. MAINDEC-11 KMAA DEC/X11 KMC11 System Test.

*15. MAINDEC-11 DZKCB ITEP Module for KMC11 with live unit.

16. EK-KMCMP-OP-001 Microprocessor User's Manual.

*17.   EK-DMCLU-OP-001 Line Unit User's Manual.

18.   MAINDEC-11-DZKCD Microprocessor CRAM and Branch

Static Tests

*Used only with KMC11 Microprocessor/DMC11 Line Unit combination.

2.3   OPTION DESIGNATIONS

The microprocessor is designated KMC11-A. Table 2-1 lists the

microprocessor and line unit options. Table 2-2 lists the line unit

cables.

2.4   MECHANICAL PACKAGING

The KMC11 Microprocessor consists of a single hex module. The

DMC11 Line Unit consists of a single notched hex module. These

modules plug into any DD11-C, DD11-D SPC system unit or equivalent

backplane. The microprocessor module must always plug into either

slot 2 or 3 in the DD11-C. The line unit module may be installed

in any of the remaining slots. Should two microprocessor/line

unit combinations be installed in a single DD11-C, then the line

unit modules plug into slots 1 and 4.

Table 2-1

Microprocessor and Line Unit

Option Designations

Option	Module	Description	Prerequisite
KMC11-A	M8204	Microprocessor	PDP-11 with DD11-C, D or equivalent
DMC11-DA	M8201	Line unit with cable for EIA interface	KMC11-A
DMC11-FA	M8201	Line unit with cable for V35/DDS interface	KMC11-A
DMC11-MA	M8202-YA	Line unit with 1M bps integral modem	KMC11-A
DMC11-MD	M8202-YD	Line unit with 56K bps integral modem	KMC11-A

Table 2-2

Line Unit Cables

Option	Description
BC03N-A0	100 ft. coaxial cable with connectors. Used with M8202 Line Unit Module.
BC05C-25	25 ft. EIA/CCITT V.24 cable for use with DMC11-DA Line Unit.
BC05Z-25	25 ft. CCITT V.35 cable for use with DMC11-FA Line Unit.

The line unit does not interface with the Unibus so module edge
connectors A and B are not used. As a result, the corner of the
module in the vicinity of the A and B connectors has been removed.
This allows the M8201 and M8202 to be installed in the end slots
of the DD11-C and D System Interfacing Units. This module
plugs into connectors C, D, E, and F and fits over the Unibus
cable connector and short length (approximately 2-1/2 in.) Unibus
terminator that are installed in end slot connectors A and B.

The microprocessor and line unit modules are interconnected by
a one-foot BC08S-1 cable that connects to a BERG 40 pin connector on
each module.

2.5   PRE-INSTALLATION PROCEDURES

2.5.1   General Information
After installing the KMC11 microprocessor as a stand-alone
device, it should be checked for proper operation by running
diagnostics DZKCC, DZKCD, and DZKCA. Its interaction with the other
devices on the Unibus can be checked by running KMAA which is
the DEC/X11 System Test for the KMC11.
Installation of the microprocessor/line unit combination should
be done in three phases. First the microprocessor is physically
installed then checked and verified with diagnostics DZKCC,
DZKCD, DZKCA, and KMAA. In this manner, the microprocessor is
checked as a stand-alone module apart from the line unit. Next,

the line unit module is installed and operationally verified with
diagnostics DZKCE and DZKCF which also provides an additional
confidence factor for the microprocessor. The third phase involves
the execution of diagnostic DZKCG which verifies the operational
status of both the microprocessor and the line unit as a free
running test. If both ends of a station consist of identical KMC11/line
unit pairs, they may be tested by using diagnostic DZKCB (ITEP).

A minimum of 8K of memory is necessary for execution of the
MAINDEC diagnostics.

Check the power supply to insure against overloading. The
microprocessor/line unit total current requirements for the
+5 volt supply is approximately 8 Amperes. Additionally, the line
unit requires $\pm$15V for the silos and the level conversion logic and
the integral modem. Refer to paragraph 2.9 for details.

Installation requires two adjacent slots, one of which can be
either the UNIBUS input or terminator slot, if the modules are
2-1/2 in. or less. The KMC11 microprocessor requires a full hex
slot while the line unit fits into any slot in the DD11 backplane.
The microprocessor can be installed in the DD11-C, DD11-D or
equivalent backplanes. Such an equivalent backplane is that used in
the PDP-11/04 or PDP-11/34 Computers.

2.5.2   Preinstallation Checkout Procedures

Before installing the microprocessor module, the following functions
must be performed.

1. Verify that M8204 jumper W1 is installed. This jumper should not be removed in the field. It is removed only at the factory during automated module testing to inhibit the oscillator in the microprocessor clock logic.

2. The microprocessor device address must be selected in accordance with paragraph 2.7.

3. The microprocessor vector address must be selected in accordance with paragraph 2.8.

4. Verify that a BR5 priority card is installed in position E74.

NOTE

Before installing the microprocessor (M8204), remove the NPR Grant wire that runs between pins CA1 and CB1 on the backplane for the slot that is going to accept the M8204. Do not remove the wire for the slot that is going to accept the line unit (M8201 or M8202). If a system change requires removal of the M8204, the NPR Grant wire must be replaced.

The M8204 Microprocessor presents one load to the Unibus and the M8201 and M8202 Line Units present no load to the Unibus except for power requirements.

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The local configuration (KMC11-A Microprocessor and DMC11-MA or DMC11-MD Line Unit) requires bus placement nearest to the PDP-11 Processor. This is due to the high rate of NPR transactions that are required. For example, the DMC11-MA Line Unit (1 Mbps) operating in full duplex requires an average of one NPR every 8μs.

2.6 INSTALLATION

After completing the pre-installation checkout procedures in paragraph 2.5.2, proceed with the installation as follows:

1. On the backplane, check that the supply voltages are within the following tolerances.

	Voltage		Backplane
Min	Nominal	Max	Pin
+4.75	+5.0	+5.25	C1A2
-14.25	-15.0	-15.75	C1B2
+14.25	+15.0	+15.75	C1U1

2. Insert the microprocessor module in the proper backplane slot.

3. Run diagnostics DZKC, DZKCD, DZKCA and KMAA in the order listed to verify correct operation of the microprocessor.

DIAGNOSTIC NOTE

If the installation is in a system using

a PDP-11/04 or other PDP-11 Processor that

does not have a switch register, a software

switch register is used to allow the user

the same switch options. If a switch register

is available but contains all 1s (177777),

the software switch register is used. Refer

to the appropriate diagnostic document for

further details.

4. Check all appropriate switch settings and jumpers on

    the line unit module in accordance with the recommendations

    in Chapter 2 INSTALLATION of the line unit manual

    (EK-DMC11LU-OP-001).

5. Insert the line unit module in the proper backplane slot.

6. Interconnect the line unit and microprocessor using cable

    BC08S-1 which is a one-foot long 40 conductor flat mylar

    cable with H856 female connectors on each end. The mating

    connector on the microprocessor and line unit is an H854

    male connector. On the microprocessor, this connector is

    designated J1. On the M8201 Line Unit, it is designated

    J2 and on the M8202 Line Unit it is J1.

7. On the DMC11-DA(M8201) Line Unit, install the BC05C-25
   cable to connector J1. On the other end of this cable,
   connect the H325 test connector.

   On the DMC11-FA(M8201) Line Unit, install the BC05Z-25
   cable to connector J1. On the other end of this cable,
   connect the H3250 test connector.

   On the M8202, install the 12-12528 coaxial test connector
   which ties the two coaxial pigtails together. These two
   3-foot cables are soldered to the M8202.

8. On the M8202, check that the integral modem clock is
   within specifications. Refer to the line unit manual.

9. Run diagnostics DZKCE and DZKCF to verify correct
   line unit operation.

10. Run diagnostic DZKCG to verify correct line unit/microprocessor
    operation.

11. Remove the test connector.

    For the M8201, connect the BC05C-25 or BC05Z-25 cable
    to the customer supplied modem.

CAUTION

The maximum allowable length for the

BC05C and BC05Z cables is 50 feet.

For the M8202, connect the pigtails to the customer

coaxial cables or the optional 100 foot BC03N-A0

cable.

12.   Diagnostic DZKCB(ITEP) can be run to check operation

between stations interconnected by KMC11

Microprocessor/DMC11 Line Unit combinations.

2.7   DEVICE ADDRESSES

2.7.1   Introduction

Starting with the DJ11, new communications devices are to be

assigned floating addresses. The addresses for current production

devices are to be retained.

The word floating means that addresses are not assigned absolutely

for the maximum number of each communications device that can be

used in a system.

2.7.2   Floating Device Address Assignments

Floating device addresses are assigned as follows:

1.   The floating address space starts at location 760010

and extends to location 764000 (octal designations).

2. The devices are assigned in order by type: DJ11, DH11, DQ11, DU11, DUP11, LK11-A, DMC11, DZ11, KMC11 and then the next device introduced into production. Multiple devices of the same type must be assigned contiguous addresses.

3. The first address of a new type device must start on a modulo 10_8 boundary, if it contains one to four bus-addressable registers. The starting address of the DH11 must be on a modulo 20_8 boundary because the DH11 has eight registers.

4. A gap of 10_8, starting on a modulo 10_8 boundary, must be left between the last address of one type device and the first address of the next type device. A gap must be left for any device on the list that is not used, if the device following it is used. The equivalent of a gap should be left after the last device assigned to indicate that nothing follows.

5. No new type devices can be inserted ahead of a device on the list.

6. If additional devices on the list are to be added to a system, they must be assigned contiguously after the

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original devices of the same type. Reassignment of
other type devices already in the system may be
required to make room for the additions.

The following example show typical floating device
assignments for communications devices in a system.

Example: 2 DH11s, 2 DQ11s, 1 DUP11, and 1 KMC11

    760010   DJ11 gap

    760020   DH11 #0 first address

    760040   DH11 #1 first address

    760060   DH11 gap

    760070   DQ11 #0 first address

    760100   DQ11 #1 first address

    760110   DQ gap

    760120   DU gap

    760130   DUP11 #0 first address

    760140   DUP11 gap

    760150   LK11- A gap

    760160   DMC11 gap

    760170   DZ11 gap

    760200   KMC11 #0 first address

    760210   Indicates no more KMC11s and no
                                  other devices follow.

2.7.3   Device Address Selection

In the floating address space (760010-764000), bits 13-17 are always 1s (function of PDP-11 processor). Appendix A shows the PDP-11 memory organization and addressing conventions. Bits 3-12 are selected by switches in the address decoding logic (Table 2-3). With the switch on (closed), the decoder looks for a 0 on the associated Unibus address line. Bits 0, 1 and 2 are decoded to select 1 of 8 registers.

The device address selection switches are contained in one DIP switch package located in position E116. All 10 switches in the package are used. The correlation between switch numbers and address bit numbers is shown in Table 2-3. The ON and OFF positions and the switch numbers are marked on the package. The switches are rocker type and are pushed to the desired position (Figure 2-1).

To Be Supplied

(Shows switch pack locations
and switch designations)

Figure 2-1   Microprocessor Device
and Vector Address Switches

Table 2-3

Guide for Setting Switches to

Select Device Address

Switch No.	10	9	8	7	6	5	4	3	2	1	Device
Bit No.	12	11	10	9	8	7	6	5	4	3	Address
										X	760010
									X		760020
									X	X	760030
								X			760040
								X		X	760050
								X	X		760060
								X	X	X	760070
							X				760100
						X					760200
						X	X				760300
					X						760400
					X		X				760500
					X	X					760600
					X	X	X				760700
				X							761000
			X								762000
			X	X							763000
		X									764000

NOTES:

1. X means switch off (open) to respond to logical 1 on the Unibus.
2. Switch numbers are physical positions in switch package 1.

2.8   VECTOR ADDRESSES

2.8.1   Introduction

Communications devices are assigned floating vector addresses. This eliminates the necessity of assigning address absolutely for the maximum number of each device that can be used in the system.

2.8.2   Floating Vector Address Assignment

Floating vector addresses are assigned as follows:

1.   The floating address space starts at location 300 and proceeds upward to 777. Addresses 500-534 are reserved.

2.   The devices are assigned in order by type: DC11; KL11/DL11-A, B; DP11; DM11-A; DN11; DM11-BB; DR11-A; DR11-C; PA611 Reader; PA611 Punch; DT11; DX11; DL11-C, D, E; DJ11; DH11; GT40; LPS11; VT20; DQ11; KW11-W; DU11; DUP11; DV11, LK11-A; DMC11; DZ11; DWR70, VTV01; KMC11.

3.   If any type device is not used in a system, address assignments move up to fill the vacancies.

4.   If additional devices are to be added to the system,
they must be assigned contiguously after the original
devices of the same type. Reassignment of other type
devices already in the system may be required.

2.8.3   Vector Address Selection

Each device interrupt vector requires four address locations
(two words) which implies only even-numbered addresses. A
further constraint is that all vector addresses must end in a
0 or 4. The vector address is specified as a three digit,
binary-coded, octal number using Unibus data bits 0-8. Because
the vector must end in 0 or 4, bits 1 and 0 are not specified
(they are always 0) and bit 2 determines the least significant
octal digit of the vector address (0 or 4). The interrupt
control logic send only seven bits (2-8) to the PDP-11 processor
to represent the vector address.

The KMC11 is shipped with a BR5 priority selection card installed
in the interrupt control logic. This logic generates two vector
addresses: input interrupts generate vector addresses of the form
XX0, and output interrupts generate vector addresses of the form
XX4. For this method of operation, the state of bit 2 is selected
by the logic not by a switch. The two most significant octal digits
of the vector address are determined by switches in lines 3-8
(Table 2-4). With the switch OFF (open), a 0 is generated on the
associated Unibus data line; with the switch ON (closed), a 1 is
generated on the associated Unibus data line.

The vector address selection switches are contained in one
DIP package located in position E65 (Figure 2-1). Only 6 of
the 8 switches in the package are used for the vector address.
The correlation between switch numbers and bit numbers is shown
in Table 2-4. The ON and OFF positions and the switch numbers
are marked on the package. The switches are rocker type and are
pushed to the desired position.

2.9   INSTALLATION CHECKLIST

The following items represent a concise checklist of the important
features of the KMC11 and KMC11/DMC11 Line Unit installations.

1.   Power Requirements

   M8204   +5V @ 5.0A

   M8201   +5V @ 3.0 A
               +15V @ 0.03 A
               -15V @ 0.31 A

   M8202   +5V @ 3.0 A
               +15V @ 0.18 A
               -15V @ 0.46 A

2.   Unibus Loading

   The M8204 presents one Unibus load. The M8201 and M8202
   present no Unibus loads.

Table 2-4

Guide for Setting Switches to Select Vector Address

Switch Switch No.	6	5	4	3	2	1	Vector
Bit No.	8	7	6	5	4	3	Address
	X			X	X	X	300
	X			X	X		310
	X			X		X	320
	X			X			330
	X				X	X	340
	X				X		350
	X					X	360
	X						370
		X	X	X	X	X	400

		X		X	X	X	500

			X	X	X	X	600

				X	X	X	700

Notes:

1. X means switch off (open) to produce a logical 0 on the Unibus.

2. Switch numbers are physical positions in switch package E65.

3.   Special Installation Requirements

    a.   M8204 Microprocessor

        Before installing, remove the NPR Grant

        continuity wire that runs between pins CA1

        and CB1 on the backplane for the slot that

        is going to accept the M8204. If a system

        change requires removal of the M8204, the

        wire must be replaced.

    b.   M8204 Microprocessor with Local Line Units

        (DMC11-MA or DMC11-MD)

        This configuration must be placed on the

        Unibus closest to the PDP-11 Processor

        because of the high rate of NPR transactions

        that are required. It must also be placed

        before a DB11-A Bus Repeater if one is used.

4. M8204 Microprocessor Switch Settings

    a.   Address Selection (E116)

Switch No.	Address Bit
1	3
2	4
3	5
4	6
5	7
6	8
7	9
8	10
9	11
10	12

    Switch OFF (open) to respond to logical 1 on Unibus.

    Switch ON (closed) to respond to logical 0 on Unibus.

    b.   Vector Selection (E65)

Switch No.	Vector Bit
1	3
2	4
3	5
4	6
5	7
6	8

    Switch OFF (open) to produce a logical 0 on the Unibus.

    Switch ON (closed) to produce a logical 1 on the Unibus.

    c. Remaining Switches in E65 are unused.

5. Line Unit Switch Settings and Jumper Configuration

    as Shipped

    a. Switch Settings

        (1) Switch Pack No. 2 (E87 on M8201 and E90

             on M8202) - All switches should be OFF.

        (2) Switch Pack No. 3 (E88 on M8201 and E91

             on M8202) - All switches should be OFF.

        (3) Switch Pack No. 1 (E26 on M8201 and E29

             on M8202) - The switches should be positioned

             as shown in Figure 2-2.

    b. The jumpers should be configured as shown in

        Figure 2-2.

*	DMC11-DA	DMC11-FA	DMC11-MA/MD
Switch No.	M8201	M8201	M8202
1	OFF	OFF	OFF
2	OFF	OFF	OFF
3	OFF	OFF	OFF
4	OFF	ON	OFF
5	OFF	OFF	OFF
6	OFF	OFF	OFF
7	ON	ON	OFF
8	ON	ON	OFF

Jumper No.			
1	IN	IN	IN
2	IN	IN	OUT
3	OUT	OUT	OUT
4	IN	IN	OUT
5	OUT	OUT	OUT
6	Not Present	Not Present	OUT (FD) / IN (HD)

NOTES:

* Switch pack no. 1 located at E26 on M8201 and E29 on
  M8202.

FD = Full Duplex

HD = Half Duplex

Figure 2-2   Configuration of Jumpers and
Switch Pack No. 1 on Line Unit

2-25

CHAPTER 3

UNIBUS CONTROL AND STATUS REGISTERS

3.1   INTRODUCTION

Eight byte sized Control and Status Registers (CSRs) are used for
the exchange of control and status information between the
PDP-11 program and the KMC11-A Microprocessor. They are address
as 76XXX0 - 76XXX7 and are referred to as Byte Select 0-7
(BSEL0-BSEL7). Words are indicated as SEL 0, SEL 2, and SEL 4.

The KMC11 is the reference point for all transfers of
information between the PDP-11 program and the KMC11. An OUT
transfer denotes information from the KMC11 to the PDP-11
program. An IN transfer denotes information from the PDP-11
program to the KMC11.

The KMC11 is a general purpose microprocessor. Seven of the eight
byte-sized CSRs are undefined and can be programmed by the user
to satisfy his particular application. The one exception is
BSEL 1 which is the Maintenance Register.

Figure 3-1 shows the Unibus CSRs including the bit assignments
for BSEL 1.

3.2   BSEL 1 MAINTENANCE REGISTER

This register contains only maintenance functions, with the
exception of MASTER CLEAR (bit 14). It is intended for servicing
the KMC11 and should not be used for normal communications

3-1

			*	*												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
RUN	MCLR	CRAM WRITE	STEP LU	LU LOOP	ROM O	ROM I	STEP μP									0
																2
																4
																6

* Applicable only when M8201 or M8202 Line Unit is used.

	CRAM ADDRESS	4 } ROM I/O
ROM O =1 → READ CRAM @ ADRS OR MAINT INST (IF ROM I =1) ROM I =1 → BITS 15:00 IS NEXT MP INST		6

	CRAM ADDRESS (ROM O=1)	4 } CRAM WRITE
CRAM DATA @ CRAM WRITE		6

Figure 3-1   Unibus Control and Status Registers

between the PDP-11 program and the KMC11. This register is contained
in the Multiport RAM but it is imaged by hardware to interact with
the KMC11 logic to implement the specified maintenance functions.

The bit assignments for the Maintenance Register are listed below.
All bits are read/write. See NOTE at the end of the bit descriptions.

Bit	Name	Description
8	STEP MICROPROCESSOR (STEP MP)	This bit, when set, steps the microprocessor through one instruction cycle, composed of five 60-ns clock pulses. The RUN flip-flop should be cleared before executing this control function.
9	ROM INPUT (ROM I)	When set, directs the contents of BSEL 6-7 as the next microinstruction to be executed by the microprocessor when STEP MP is asserted.
10	ROM OUTPUT (ROM O)	When set, modifies the source paths for SEL 4 to be the CRAM PC, enabling read and/or write via SEL 6 of the specified locations. A write is accomplished by loading the new CRAM data into SEL 6 and asserting bit 13 of BSEL 1. CRAM read is accomplished by reading SEL 6.
11	LINE UNIT LOOP (LU LOOP)	This bit is the output of a flip-flop and is accessible at pin A of the Berg

Bit	Name	Description (Cont)

connector on the KMC11 for assignment
by the user. However, if an M8201 or
M8202 Line Unit is being used, this bit
has a specific function and is called
LINE UNIT LOOP (LU LOOP).

When this bit is set, with a M8201 or M8202
connected, the line units serial output line
is connected to its serial input line
internally. This is done at the TTL logic
level, before the level conversion logic.
When LU LOOP is set and RUN is cleared, the
STEP LU bit is used, under diagnostic control,
to single step data in or out. When LU LOOP
is set and RUN is set, data is clocked at
a 10K bps rate.

For the M8201 Line Unit, if the loop back
connector is installed at the end of the
modem cable with RUN set and LU LOOP cleared,
data is clocked at a 10K bps rate and the
level conversion logic and cable are
exercised also.

For the M8202 line Unit, the coaxial adapter
is used to interconnect the pigtail cables
to provide the loop back. In this case, data
is clocked at the operating speed of the
integral modem.

3-4

Bit	Name	Description (Cont)
12	STEP LINE UNIT (STEP LU)	This bit is the output of a flip-flop and is accessible at pin B of the Berg connector on the KMC11 for assignment by the user. However, if an M8201 or M8202 Line Unit is being used, this bit has a specific function and is called STEP LINE UNIT (STEP LU).
		This bit is used in conjunction with LU LOOP. When STEP LU is asserted, the line unit transmitter is single stepped. When it is cleared, the line unit receiver is single stepped.
13	CRAM WRITE	When set, this bit allows the contents of SEL 6 to be loaded into the CRAM at the address specified in SEL 4. Bit 10 (ROM O) must also be set to accomplish the loading procedure.
14	MASTER CLEAR	When set, MASTER CLEAR initializes both the microprocessor and the line unit, if installed. This bit is not self clearing and must be cleared by the PDP11 program. The microprocessor clock is halted and the RUN flip-flop is cleared. The CRAM's PC is also cleared by MASTER CLEAR. If other bits set in BSEL 1, use a MOVE instruction that

Bit	Name	Description (Cont)

sets MASTER CLEAR and clears all other bits.

MASTER CLEAR should not be asserted without raising the PDP11 processor status to level 7 if the KMC11-A is programmed to perform BUS Requests (XX0 or XX4). The use of an incorrect procedure may hang the Unibus if a Bus Request transaction is in progress when the MASTER CLEAR is issued.

15   RUN

RUN controls the microprocessor clock. This bit is cleared by BUS initialization or MASTER CLEAR, which stops the microprocessor clock. RUN can be set or cleared as required by the PDP11 program.

NOTE

The PDP11 program writes into the Multiport RAM and the BSEL 1 hardware but it reads only the Multiport RAM. The KMC11 reads and writes only the Multiport RAM. It cannot write into the actual BSEL 1 hardware.

CHAPTER 4

MICROPROCESSOR CONTROL AND STATUS REGISTERS

4.1   INTRODUCTION

The Unibus CSRs described in Chapter 3 are physically located
in the multiport RAM. The RAM capacity is 128 bits arranged as
16 8-bit bytes, which is equivalent to eight 16-bit words. The
RAM can be accessed simultaneously from two sources. One source
is the Unibus and the other is the microprocessor. Therefore,
when these Unibus CSRs (BSEL1-BSEL7) are viewed from the
microprocessor, they are called Microprocessor CSRs. Specifically,
they are identified as OUTBUS*/INBUS* registers 0-7 (octal).

The remaining multiport RAM capacity, which is 8 8-bit bytes,
contains the NPR Data and BA registers. These registers are also
called Microprocessor CSRs and are specified as OUT BUS/IN BUS
registers 0-7 (octal).

There are two additional byte sized hardware registers that are
listed in the OUT BUS*/IN BUS* category. They are the NPR Control
register (10_8) and the Microprocessor Miscellaneous register (11_8).

The microprocessor has the capability of addressing 32 byte
sized registers. As a convention, it has been decided to show 16
assigned addresses under each category; that is, OUT BUS*/IN BUS*
and OUT BUS/IN BUS. As a result, six undefined registers 12-17

(octal) are listed under OUT BUS*/IN BUS*. These registers do not

exist physically. The M8201/M8202 Line Unit device registers,

10_8-10_8 have been added to the OUT BUS/IN BUS category. These

registers are physically located in the line unit. Address 10_8 is

listed twice because two line unit registers use the same address.

The In Data Silo is read only and the Out Data Silo is write only.

Therefore, there are nine registers in the line unit.

The arrangement of the Microprocessor CSRs is shown in Figure 4-1.

4.2   OUT BUS*/IN BUS* REGISTERS 0-7

These eight registers are the Unibus CSRs as viewed from the

microprocessor. They are identical to those described in Chapter 3.

Note that the KMC11 may write into BSEL 1 (MAINT REG), however, only

the Multiport RAM changes state. The flip-flops and gates that

image BSEL 1 and actually control the hardware (RUN, MASTER CLR, etc)

are not affected.

4.3   NPR CONTROL REGISTER (OUT BUS*/IN BUS* 10)

The bit assignments for the NPR Control Register are described

below.

Bit	Name	Description
0	NPR REQUEST (NPR RQ)	This bit can be set only. It is automatically cleared by the hardware when the NPR has been completed. When set, this bit requests an NPR via the Unibus to the PDP-11 memory. If OUT NPR (bit 4) is cleared, data is transferred from the PDP-11 memory. If OUT NPR (bit 4) is cleared, data is transferred from the PDP-11 memory. If OUT

Figure 4-1   Microprocessor Registers

Bit positions: 7 6 5 4 3 2 1 0

Register	Contents	
0	BYTE 0	
1	BYTE 1	
2	BYTE 2	
3	BYTE 3	Unibus CSRs as viewed from Microprocessor.
4	BYTE 4	
5	BYTE 5	
6	BYTE 6	
7	BYTE 7	

	7	6	5	4	3	2	1	0	
10 NPR CONT	BYTE XFER	MAR 10	MAR 8	OUT NPR	IN BA 17	IN BA 16	NOT LAST XFER	NPR RQ	
11 μP MISC	BUS RQ	VECT x4	///	PGM CLK	OUT BA17	OUT BA16	AC LO	NON EX MEM	

Register	
12	
13	
14	Undefined
15	
16	
17	

16 Registers Assigned to OUTBUS*/INBUS* Category

4-3

7	6	5	4	3	2	1	0		
IN DATA LB								0	
IN DATA HB								1	
OUT DATA LB								2	
OUT DATA HB								3	
IN BA 7:0								4	
IN BA 15:8								5	
OUT BA 7:0								6	
OUT BA 15:8								7	
IN DATA SILO								10	
OUT CLR	OUT ACT	SW	OUT RDY	///	///	TEOM	TSOM	11	OUT CONT
OUT DATA SILO								10	
IN CLR	IN ACT	LU LOOP	IN RDY	///	///	BLK END	BCC MATCH	12	IN CONT
RING	DTR	RS	HD	MOD RDY	CS	SW	SW	13	MODEM CONT
SYNC CHAR/SECONDARY ADRS								14	
SWITCH SELECTABLE								15	
SWITCH SELECTABLE								16	
QO	QI	SI	OCOR	ICIR	///	LU CLK	DDCMP MODE	17	MAINT

Line Unit Registers (Used only if Sync Line Unit M8201 or M8202 is installed.) — (brace grouping registers 10 through 17)

16 Registers Assigned to OUTBUS/INBUS Category

Figure 4-1 Microprocessor Registers (Cont)

4-4

Bit	Name	Description (Cont)

NPR is set, data is transferred to the PDP-11 memory. Bit 7 (BYTE XFER) controls word/byte selection.

For an IN NPR, the PDP-11 memory address is in OUT BUS/IN BUS registers 4 and 5. For an OUT NPR, the address is in OUT BUS/IN BUS registers 6 and 7. The data that is associated with the transaction comes from OUT BUS/IN BUS registers 2 and 3 for OUT DATA and from OUT BUS/IN BUS registers 0 and 1 for IN DATA. OUT NPR (bit 4) is Unibus Control line C1 and BYTE XFER (bit 7) is Unibus Control line C0. When BYTE XFER is set, the state of the BA least significant bit (0) is used to select the byte. The truth table for the type of transaction, as selected by these bits, is shown below.

OUT NPR (C1)	BYTE XFER (C0)	BA0	KMC11-A Transaction*
0	0	0	IN NPR
0	0	1	Illegal
0	1	0	Illegal
0	1	1	Illegal
1	0	0	OUT NPR

Bit	Name	Description

OUT NPR	BYTE XFER		KMC11-A
(C1)	(C0)	BA0	Transaction
1	0	1	ILLEGAL
**1	1	0	OUT NPR (Destination is low byte)
**1	1	1	OUT NPR (Destination is high byte)

*Reference is from KMC11-A

**Source is OUT BUS/IN BUS Register 2

Bit	Name	Description
1	NOT LAST TRANSFER (NOT LAST XFR)	This bit is used to permit the KMC11 to maintain Unibus mastership following the execution of an NPR in order to perform multiple NPRs. Setting NOT LAST XFR with NPR RQ allows multiple NPRs to be performed by maintaining Unibus mastership following completion of each NPR.

In the case of multiple NPRs, the last required NPR is performed by asserting NPR RQ followed by the clearing of NOT LAST XFR in the next KMC11 instruction. When NPR RQ is cleared again, Unibus mastership is relinquished by the KMC11. |
| 2, 3 | IN BA 16 and IN BA 17 | These are the PDP-11 memory extension bits used during an IN NPR (C1 = 0) transaction. |

Bit	Name	Description
4	OUT NPR	This bit is used in association with NPR RQ (bit 0). The details of the inter-relationship between these bits are covered in the description of NPR RQ (bit 0).
5	MAR 8	This read only bit is used to monitor bit 8 of the Memory Address Register (MAR)
6	MAR 10	This read only bit is brought out as a flag for use in debugging the KMC11. During debugging, it is valuable to know the contents (MEM address) of the MAR at a specific time. Only MAR bits 8 and 10 can be read.

MAR bits 0-9 are loaded as either 1s or 0s but MAR bit 10 is always loaded as a 0. By incrementing the MAR from some unknown location to the 1024th MEM address, output bits 0-9 are all 1s. On the next clock pulse, output bit 10 goes to a 1. By counting the number of clock pulses required to drive bit 10 to a 1, the starting point of the MAR can be determined.

4-7

Bit	Name	Description
7	BYTE XFER	This bit is used in association with OUT NPR to indicate a byte transfer to the PDP-11 memory. When this bit is set, the PDP-11 uses address bit A0 for byte selection. If A0 is a 0, OUT DATA 7-0 is stored in the low byte of the PDP-11 memory. If A0 is a 1, OUT DATA 7-0 is stored in the high byte of the PDP-11 memory.

If BYTE is cleared during an OUT NPR operation, OUT DATA 15-0 is transferred to the PDP-11 memory as a word.

4.4 MICROPROCESSOR MISCELLANEOUS REGISTER(OUTBUS*/IN BUS* 11)

Bit	Name	Description
0	NON-EXISTENT MEMORY (NON-EX MEM)	During an NPR, this bit is set approximately 20 us after a non-existent memory location is addressed by the microprocessor. At this time, the NPR logic releases the Unibus.
1	AC LOW	This bit is a set only bit. When set, it triggers a 1-shot with a pulse duration of 0.5 second. This pulse goes to the Unibus and initiates a power fail recovery procedure in the PDP-11 processor. The AC LOW bit is not recommended for non DEC use.

Bit	Name	Description
2, 3	OUT BA 16 and OUT BA 17	These are the PDP-11 memory extension bits used during an OUT NPR transfer.
4	PROGRAM CLOCK (PGM CLK)	This bit acts as a timer for the microprocessor. It can be read to determine elapsed time for time-out, flag testing, etc.
		This bit is the 0 output of a retriggerable 1-shot with a 50us pulse duration. When this bit is set by the KMC11 microprogram, the 1-shot is triggered. As long as the triggering pulses come along at less than 50us intervals, the 1-shot remains asserted and this bit is read as a 0. If the 1-shot times out, this bit is read as a 1.
5	RESERVED	
6	VECTOR AT XX4	If this bit is set when BR RQ (bit 7) is set, vector address XX4 is generated. If it is cleared when BR RQ is set, vector address XX0 is generated.

Bit	Name	Description
7	BR REQUEST (BR RQ)	When set, this bit initiates a Bus Request via the Unibus at BR level 4, 5, 6, or 7. The microprocessor is shipped with a BR5 priority card installed. This bit can be set only and is cleared by the hardware after the BR has been completed.

4.5 NPR BUS ADDRESS AND DATA REGISTERS (OUT BUS/IN BUS 0-7)

Register	Name	Description
0, 1	IN DATA	Low byte (register 0) and high byte (register 1) of data to be transferred from the PDP-11 memory.
2, 3	OUT DATA	Low byte (register 2) and high byte (register 3) of data to be transferred to the PDP-11 memory.
4, 5	IN BA	Contains Bus Address (BA) bits 0-15 during an NPR transfer from the PDP-11 memory. Bit 0 of register 4 is BA bit 0 and bit 7 of register 5 is BA bit 15.

Register	Name	Description
6, 7	OUT BA	Contains Bus Address (BA) bits 0-15 during an NPR transfer to the PDP-11 memory. Bit 0 of register 6 is BA bit 0 and bit 7 of register 7 is BA bit 15.

CHAPTER 5

MICROINSTRUCTION FORMATS AND

PROGRAMMING INFORMATION

5.1   SCOPE

This chapter provides a detailed description of the KMC11 micro-

instruction word formats and general programming information.

The word formats are presented along with a simplified block

diagram and a simplified timing diagram of the microprocessor.

5.2   MICROINSTRUCTION WORD FORMATS

The KMC11 Microprocessor executes two types of microinstructions:

BRANCH and MOVE. It uses three variations of the BRANCH micro-

instruction and five versions of the MOVE microinstruction as

shown below.

BRANCH	MOVE
Immediate (I)	Immediate (I)
Memory (MEM)	In Bus (IBUS)
Register (BRG)	IN BUS* (IBUS*)
	Memory (MEM)
	Register (BRG)

The microinstructions are stored in the control RAM (CRAM) which is

a 1024-by-16 bit random access memory.

To assist the reader in visualizing microprocessor data flow and

timing, a microprocessor simplified block diagram (Figure 5-1) and

timing diagram (Figure 5-2) are included in this section.

5-1
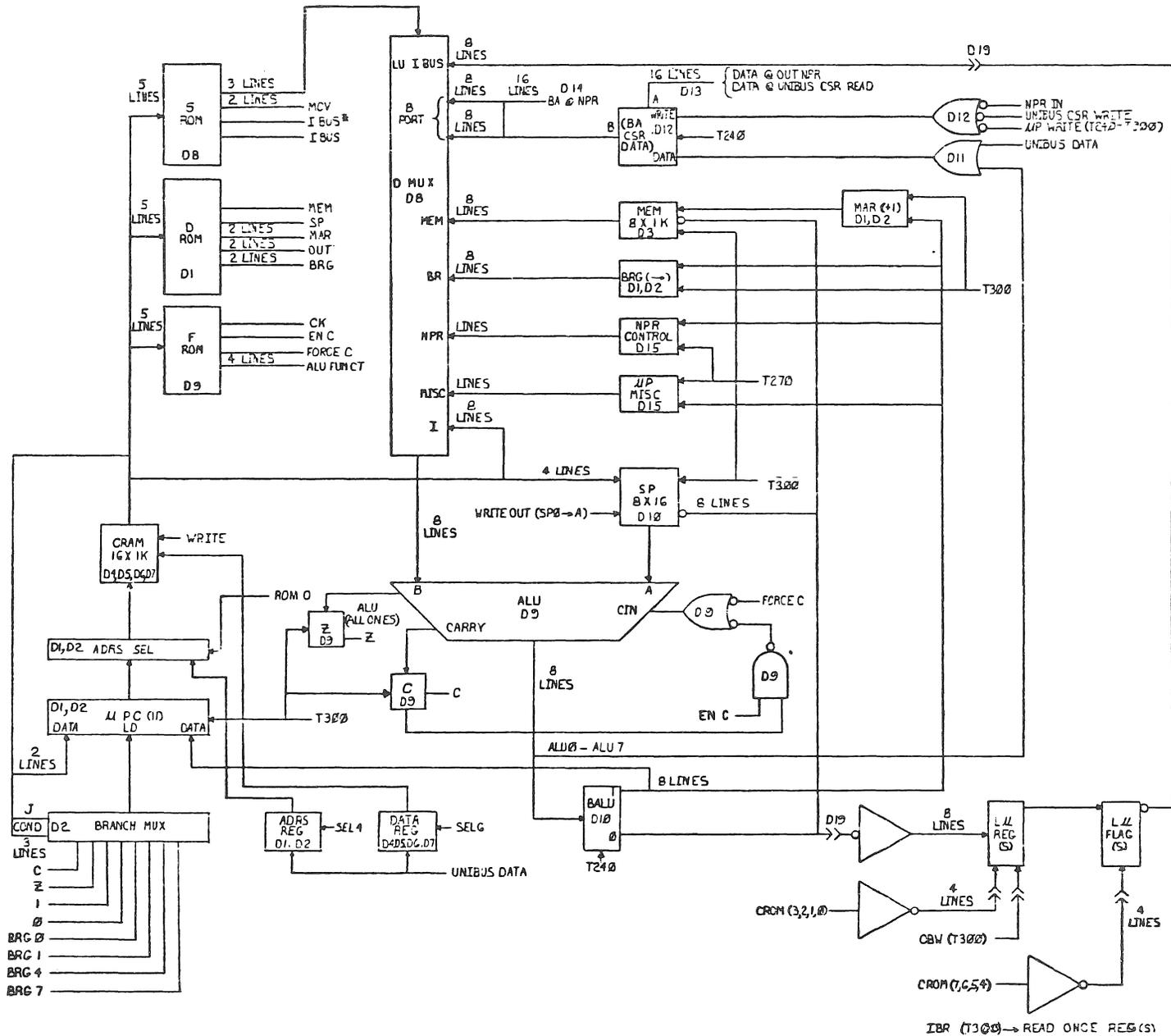
Figure 5-1   Microprocessor Block Diagram

```
      T12ϕ       T24ϕ     Tϕ              T12ϕ      T24ϕ    Tϕ
```

BALU | LAST INST RESULT OPERAND |

PC | (PC+1) OR LAST INST RESULT OPER |

CRAM | CURRENT INSTRUCTION |

MAR | LAST INST RESULT OPERAND |

BRG | LAST INST RESULT OPERAND |

SCRATCH PAD | CURRENT INST "A" OPERAND |

MULTIPORT RAM | CURRENT INST "B" OPERAND |

ALU | CURRENT INST RESULT OPERAND |
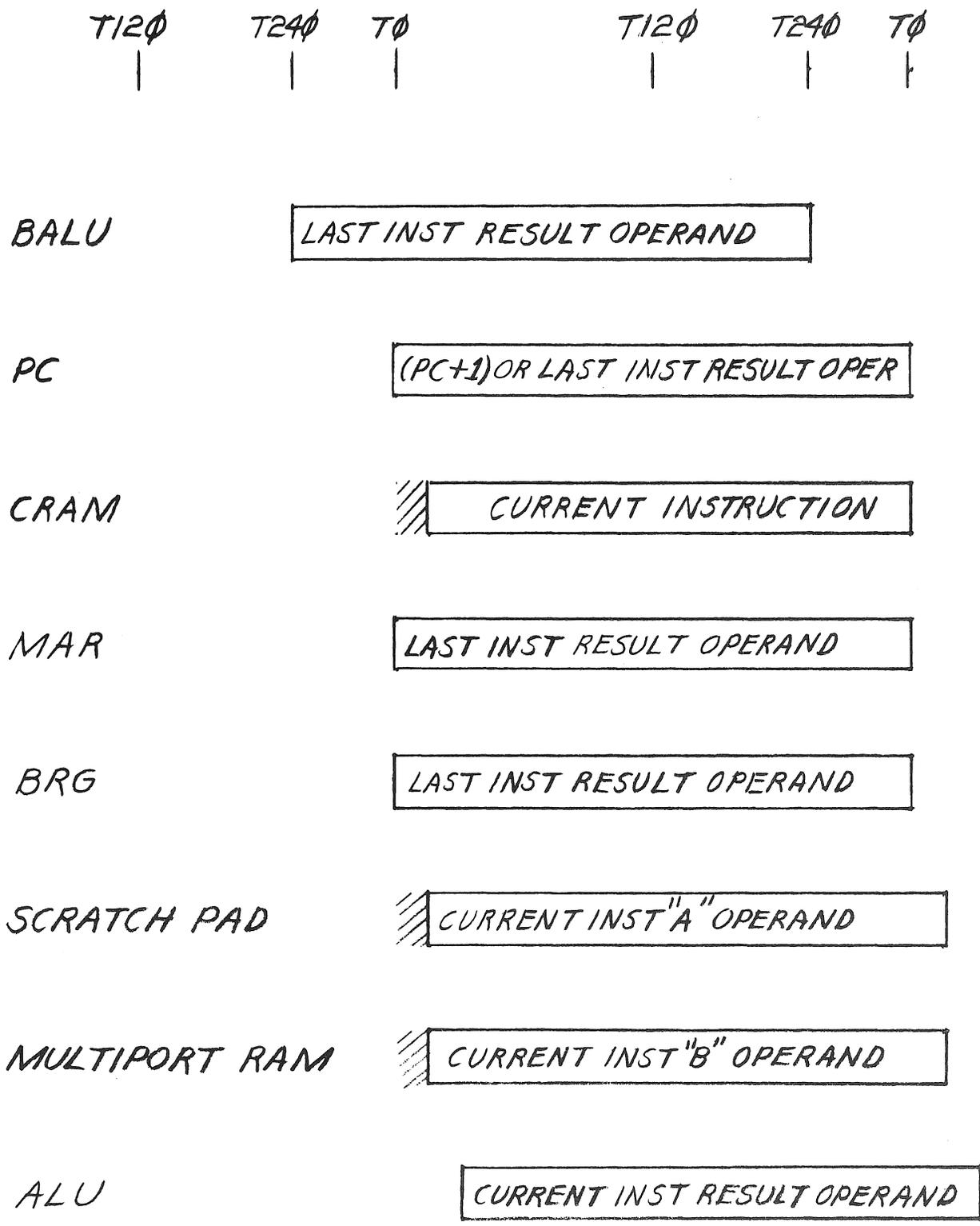
Figure 5-2   Microprocessor Register Timing

5.2.1   BRANCH Microinstruction

Figure 5-3 illustrates the word format of the BRANCH microinstruction. Bits 13-15 are the operation code defining the microinstruction as a branch. The operation code defines further the source operand from which the partial branch address is developed. The branch address being the address of the next microinstruction, should the branch condition be satisfied.

The condition under which the branch is to occur is defined by bits 8-10. The resultant branch address is partially defined by bits 0-7 of the microinstruction. These eight bits are combined with microinstruction bits 11 and 12 to form the complete ten bit branch address capable of addressing any of the 1024 locations within the CRAM.

Three BRANCH microinstructions exist, each defining a different source operand from which to develop the low eight bits of the branch address.

5.2.1.1 0_8 - BRANCH Immediate (I)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	BAB		CONDITION			IMMEDIATE ADDRESS							
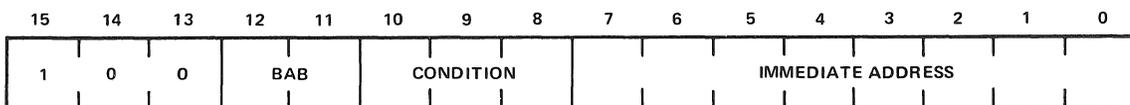
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The microprogram branches if the condition specified by microinstruction bits 8-10 is met. The ten bit branch address is the result of combining microinstruction bits 0-7 with the Branch Address Bits (BAB) 11 and 12.

BRANCH

```
| 15        13 | 12   11 | 10        8 | 7                                   0 |
```

OP CODE
DEFINED

SOURCE
OPERAND

1 0 0	BRANCH ADD- RESS BITS 9, 8	BRANCH CONDITION	BRANCH ADDRESS	
1 1 0			ALU FUNCTION	SCRATCH PAD ADDRESS
1 1 1				

```
000  —  Reserved
001  —  Unconditional Branch
010  —  Branch if C bit is set
011  —  Branch if Z bit is set
100  —  Branch if BRG bit 0 is set
101  —  Branch if BRG bit 1 is set
110  —  Branch if BRG bit 4 is set
111  —  Branch if BRG bit 7 is set
```

These two bits combined with the
eight bit ALU output form the
complete ten bit address.

ALU Function		Code
SUB	(A–B)	1110
2's COMP SUB	(A–B–1)	1111
ADD	(A,B)	0000
ADD W/C	(A,B,C)	0001
SUB W/C	(A–B–C)	0010
INC A	(A,1)	0011
A PLUS C	(A,C)	0100
2A	(A,A)	0101
2A W/C	(A,A,C)	0110
DEC A	(A–1)	0111
SEL A	(A)	1000
SEL B	(B)	1001
A or $\overline{B}$	(A+$\overline{B}$)	1010
A and B	(AB)	1011
A or B	(A+B)	1100
A X or B	(A⊕B)	1101

100 — Immediate: Bits 0–7 of the microword
combined with bits 11 and 12 form
the branch address.

110 — MEM: The MEM contains the source
operand to be combined with the SP
memory operand as defined by the
ALU function bits.

111 — BRG: The BRG contains the source
operand to be combined with the SP
memory operand as defined by the
ALU function bits.

Notes:

C = Carry
W/C = With Carry
C and Z are set/cleared with MOVE Instructions.
A = Arithmetic or scratch pad (SP) side of ALU.
B = Logic or DMUX side of ALU.

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Figure 5-3   Branch Microinstruction Word Format

5.2.1.2 6_8 - BRANCH Memory (MEM)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	BAB		CONDITION			ALU FUNCTION				SP ADRS			
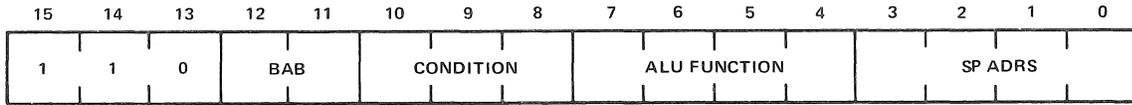
11 - 4394

This microinstruction combines two operands in the Arithmetic
Logic Unit (ALU) under control of the ALU FUNCTION bits (bits
4-7). The resultant operand, when combined with microinstruction
bits 11 and 12, produces a ten bit branch address. One operand
is from a MEM storage location and the other is from the Scratch
Pad (SP). Microinstruction bits 0-3 address the operand in the
Scratch Pad, while the MEM operand is from the location addressed
by the current contents of the Memory Address Register (MAR). The
desired address would have been loaded into the MAR by a previous
instruction other than the BRANCH under execution. The condition
for the branch is defined by the CONDITION CODE, bits 8-10. Figure
5-3 defines the ALU FUNCTION CODES possible with this microinstruction.

5.2.1.3 7_8 - BRANCH Register (BRG)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	BAB		CONDITION			ALU FUNCTION				SP ADRS			
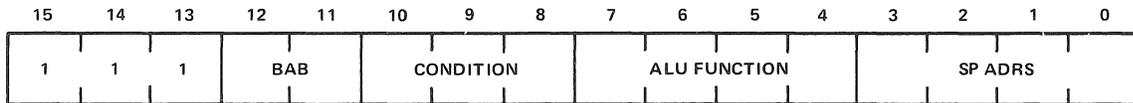
11 - 4395

With this microinstruction, the contents of the BRG and a Scratch
Pad memory location are operated on to generate the partial branch
address. Bits 0-3 specify the Scratch Pad memory location and bits
4-7 define the ALU FUNCTION to be performed on the two operands.

5.2.2 MOVE Microinstruction

The MOVE microinstruction is also highly versatile. When combined with the BRANCH in a microprogram, the combination produces versatility and power. In all, five variations of the MOVE microinstruction exist, each specifying a different source for the operand. The source is defined by the operation code. Figure 5-4 illustrates the MOVE microinstruction word format.

The operation code is defined by bits 13-15. Bits 11 and 12 specify the function to be performed on the MAR. According to bits 11 and 12, the MAR can remain unmodified, be incremented, or be loaded(HI/LO) from the Buffered ALU (BALU). The destination of the resultant operand is defined by microinstruction bits 8-10. The low byte of the microinstruction is operation code dependent and further defines input addresses, ALU function, and output addresses.

The ALU Function Field, microinstruction bits 4-7, defines the operation to be performed on the two operands. These four bits plus operation code bit 14 are the Function ROM (FROM) address inputs. The FROM microword controls the ALU inputs.

Common to all five MOVE microinstructions are the MAR FUNCTION FIELD and the DESTINATION FIELD. The MAR increment and load function sets up the address of the MEM operand for the next microinstruction where necessary.

MOVE

| 15 | | 13 | 12 | 11 | 10 | | 8 | 7 | | | | | | | 0 |

0 0 0			IMMEDIATE OPERAND	
0 0 1	MAR FUNC- TION FIELD	DESTINATION FIELD	INPUT ADRS	OUTPUT ADRS
1 0 1			INPUT ADRS	OUTPUT ADRS
0 1 0			ALU FUNCT	OUTPUT ADRS OR SCRATCH PAD ADRS
0 1 1			ALU FUNCT	
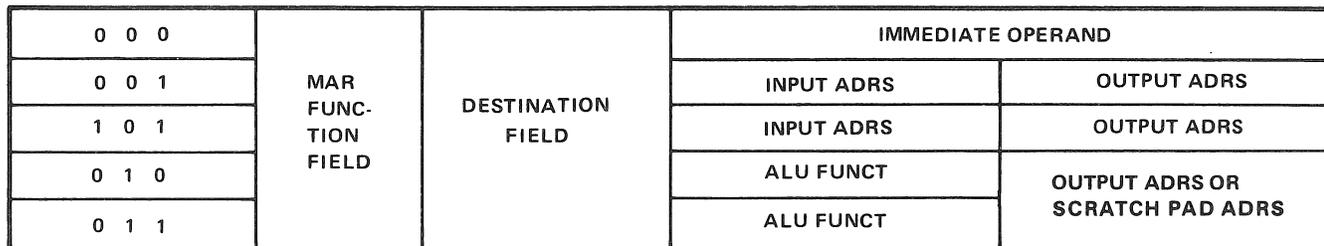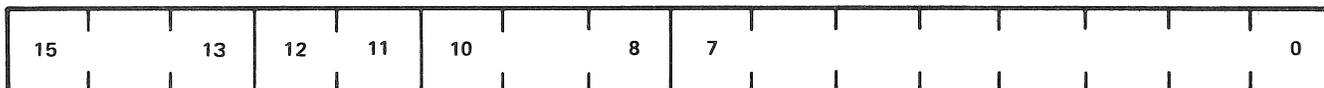
```
0 0 0  —  No operation
0 0 1  —  BRG
0 1 0  —  OUTBUS* (SP0 → A)
0 1 1  —  BRG right shifted one bit
1 0 0  —  OUTBUS (SP0 → A)
1 0 1  —  MEM
1 1 0  —  SCRATCH PAD
1 1 1  —  SCRATCH PAD and BRG
```

```
0 0  —  No effect
0 1  —  Load MAR Hi
1 0  —  Load MAR Low
1 1  —  Increment MAR
```

```
0 0 0  —  Immediate operand in bits 0—7 of
           microinstruction.

0 0 1  —  IBUS is operand source defined by
           microinstruction bits 4—7 and
           destination defined by bits 8—10.

1 0 1  —  IBUS* is operand source defined by
           microinstruction bits 4—7 and destination
           defined by bits 8—10.

0 1 0  —  MEM is operand source operated on as
           defined by ALU function (bits 4—7).

0 1 1  —  BRG is operand source operated on as
           defined by ALU function (bits 4—7).
```

ALU Function		Code		
SUB	(A–B)	1110		
2's COMP SUB	(A–B–1)	1111		
ADD	(A,B)	0000	MOV	
ADD W/C	(A,B,C)	0001	INST	
SUB W/C	(A–B–C)	0010	CLOCK	
INC A	(A,1)	0011	C	MOV
A PLUS C	(A,C)	0100	(Note 1)	INST
2A	(A,A)	0101		CLOCK
2A W/C	(A,A,C)	0110		Z
DEC A	(A–1)	0111		(Note 2)
SEL A	(A)	1000		
SEL B	(B)	1001		
A or $\overline{B}$	(A+$\overline{B}$)	1010		
A and B	(AB)	1011		
A or B	(A+B)	1100		
A X or B	(A⊕B)	1101		

Notes:

1. If ADD function, C is set to indicate carry or overflow.

   If SUB function, C is cleared to indicate borrow or sign change.

2. Z is set when ALU out is all 1s.

3. C = Carry
   W/C = with Carry
   A = Arithmetic or scratch pad (SP) side of ALU.
   B = Logic or DMUX side of ALU.

11 - 4375

Figure 5-4   Move Microinstruction Word Format

The DESTINATION FIELD, as the name implies, specifies the destination of the resultant operand. Three of the eight possible destination references are microprocessor discrete registers, i.e., BRG, MEM, and BRG shifted and consequently need no further address definition. The specific location in MEM was predefined with a previous microinstruction. Four destination references require still further address definition. These include OUT BUS, OUT* BUS, SCRATCH PAD, and SCRATCH PAD/BRG. The low order four bits (bits 0-3) of the microinstruction provide a specific destination address within OUT BUS, OUT* BUS or the Scratch Pad memory when any of these are referenced as a destination.

When destinations OUT BUS and OUT BUS* are microprogrammed, SP address 0 is presented to ALU input A. Thus, if MOVE instruction MEM or BRG source is used, all 16 ALU functions are available to operate on the two source operands (SP0 and MEM or BRG).

The BRG right shift destination performs a hardware right shift on bits 7 to 0. Unshifted BRG bits 7-0 are passed through the ALU B side with bit 0 returning to BRG bit 7 during a MOVE type BRG instruction. This allows all 16 ALU functions with the SP to be used for the possible alteration of the data bit returned to BRG bit 7. Additionally, the unshifted BRG is available for a MAR load.

Instruction types MOV I, MOV IBUS, MOV IBUS* and MOV MEM may also be used with a BRG right shift. However, in these cases ALU bit 0 is a function of source I, IBUS and IBUS* while MOVE MEM, which is similar to MOV BRG, is a function of MEM and SP as selected by the 16 ALU functions.

5.2.2.1 0_8 - MOVE Immediate (I)

| 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	MFF		DEST			IMMEDIATE OPERAND							
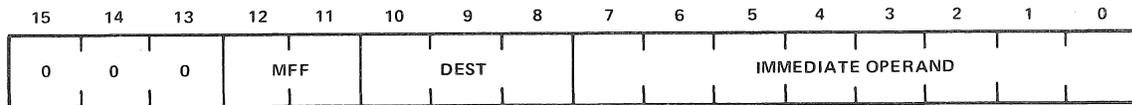
<div align="right">11 - 4396</div>

The operand, microinstruction bits 0-7, is moved to the destination as specified by microinstruction bits 8-10.

With the MOVE IMMEDIATE, the destination reference is normally limited to the BRG, MEM, and the MAR. The other possible destination references are usable; however, they require special consideration since the same data is used both as an operand and destination address.

5.2.2.2 1_8 - MOVE IN BUS (IBUS)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	MFF		DEST			INPUT ADRS				OUTPUT ADRS			
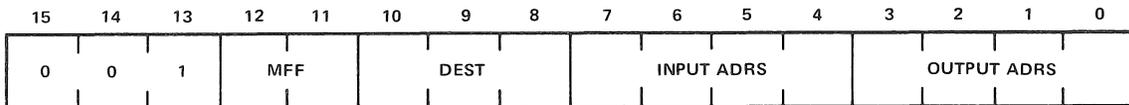
<div align="right">11 - 4397</div>

The operation code specifies the IBUS as the source operand. However, because the IBUS is a block of sixteen 8-bit words additional address information must be provided by the INPUT ADDRESS portion of the microinstruction (bits 4-7). In cases where the DESTINATION FIELD specifies data blocks, i.e., OUT BUS, OUT* BUS or the Scratch Pad memory, microinstruction bits 0-3 specify the byte position within the block as the destination. In addition, the operand can also be clocked into the MAR when so indicated by the MAR FUNCTION FIELD, microinstruction word bits 11 and 12.

<div align="center">5-10</div>

5.2.2.3 5_8 — MOVE IN BUS* (IBUS*)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	MFF		DEST			INPUT ADRS				OUTPUT ADRS			
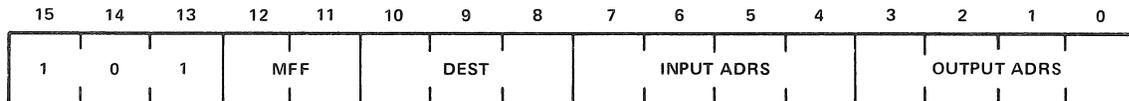
11 - 4398

This microinstruction is similar to the MOVE IBUS microinstruction with the exception that the MOVE IBUS* addresses the IBUS* block of words.

5.2.2.4 2_8 — MOVE Memory (MEM)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	MMF		DEST			ALU FUNCTION				OUTPUT ADRS			
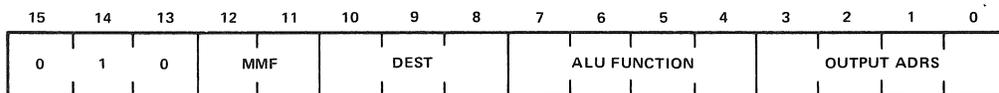
11 - 4399

The MOVE MEM microinstruction performs either an arithmetic or logical operation on two designated operands and deposits the resultant operand into the specified destination address. One of the two operands is from MEM while the second is from the Scratch Pad memory.

The Scratch Pad address is 0000 if the destination is OUT, OUT*, or if bits 0-3 are 0000 when one of the other six destinations are defined.

The selection of an arithmetic or logical operation on the operand is determined by ALU function field bits 7 through 4.

The resultant operand is moved to the destination as specified by the DESTINATION field, microinstruction bits 8-10 and/or bits 11 and 12 if the MAR is loaded.

When the Scratch Pad memory or MEM is designated as the destination, then the respective source operand is destroyed by delivery of the resultant operand.

5.2.2.5 3_8 - MOVE BRANCH REGISTER (BRG)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	MFF		DEST			ALU FUNCTION				OUTPUT ADRS			
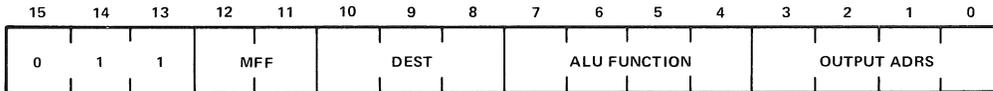
11 - 4400

The operation of the MOVE BRG microinstruction is similar to the MOVE MEM with one exception. The two operands of this microinstruction are the contents of the BRG and the Scratch Pad memory. If the microinstruction specifies either the Scratch Pad memory or the BRG as the destination, then the respective source operand is destroyed by the delivery of the resultant operand.

5.3   KMC11-A SAMPLE PROGRAMMING

5.3.1   Programming Samples for Accessing the CSRs

Example 1: MOV #20 to CRAM at KMC11 program counter location
32 and verify. The functions and procedures to be
performed are:

Write Functions

        a.   Clear BSEL1 if desired.

        b.   Load PC #32 into SEL 4.

        c.   Load CRAM data (20) into SEL 6.

        d.   Set bit 10 in SEL 0 to address CRAM.

        e.   Set bit 13 in SEL 0 to write data.into CRAM
              at specified location.

        f.   Clear BSEL 1.

Programming Write Functions

MOV #32, SEL 4   ;set CRAM address

MOV #20, SEL 6   ;set data to load

MOV #4, BSEL 1   ;select CRAM at PC 32

BISB #40, BSEL 1   ;write CRAM

CLRB BSEL 1   ;reset select and write CRAM

Read Functions

        h.   Repeat steps b, c, and d.

        i.   Read SEL 6 and verify.

        j.   Clear BSEL 1.

Programming Read Functions

MOV #32, SEL 4   ;set CRAM address to read.

MOV #4, BSEL 1   ;select CRAM at PC 32

5-13

```
        CMP #20, SEL 6              ;compare the contents of CRAM address
                                        with the original data.

        BNE ERROR                  ;if not equal, then branch.

        CLRB BSEL 1                ;reset select CRAM PC.


        Example 2:  Master clear the KMC11-A and then set RUN to
                    execute code in CRAM from program counter
                    location 0.


        Program Procedure

        MOVB #100, BSEL 1          ;set master clear.

        MOVB #200, BSEL 1          ;reset master clear and set RUN.


5.3.2   Microcode Programming Samples

        Example 1:  Write to BSEL 4 using SP0 as an operand.

        OUT         SELA, OPORT 1       ;write SP0 to OUT *4


        Example 2:  Increment the output BA (18 bits).

        SP          IBUS, IOBA1, SP0  ;read low byte

        OUT         INCA, OBA1        ;write it out

        SP          IBUS, IOBA2, SP0  ;read low byte

        OUT         APLUSC, OBA2      ;add carry from low byte

        C           10 $             ;branch carry from high byte


                            Always Exit

10$:    SP          IBUS, UBBR, SP0   ;read extended BA

        BWRTE       IMM, 4            ;

        SP          BR, ADD, SP0      ;increment them

        BWRTE       IMM, 115          ;mask to save state of XX4
                                         and NXM
```

5-14

Always Exit (Cont)

```
OUT           BR, AANDB, OBR        ;write extended BA bits back
              Always Exit
```


Example 3: Perform an NPR OUT to a BA of 20,000

```
BRWRTE            IMM, 0                  ;

OUT               BR, SELB, OBA1          ;

BRWRTE            IMM, 40                 ;

OUT               BR, SELB, OBA2          ;

SP                IBUS, UBBR, SP0         ;

BRWRTE            IMM, 101                ;

OUT               BR, AANDB, OBR          ;clear extended
                                           memory bits

BRWRTE            IMM, DATAL              ;data to write to
                                           20000

OUT               BR, SELB, OUTDA1        ;

BRWRTE            IMM, DATAH              ;high byte

OUT               BR, SELB, OUTDA2        ;

BRWRTE            IMM, 21                 ;

OUT               BL, SELB, ONPR          ;start the NPR
```


Example 4: Perform Unibus BR at XX4

```
SP                IBUS, UBBR, SP0         ;read the Miscellaneous
                                           Register

BRWRTE            IMM, 15                 ;save state of extended
                                           memory bits and NXM bit

SP                BR, AANDB, SP0          ;

BRWRTE            IMM, 300                ;BR request and XX4

OUT               BR, AORB, OBR           ;
```

Example 5:   Branch on BRG bit 5 (requires shift) and use
             MEM as source for next PC bits 07:00.

       BRWRTE   MEMX, SELB   ;

       BRSHFT

       BR4   XXX

Example 6:   Send characters from MEM to the Line Unit.

       OUT   MEMI, SELB, TMTDAT   ;increment memory
                                                        address

5$:   BRWRTE   IBUS, TMTCON   ;read xmit status

       BR?   10$;ready

       ALWAYS   5$;not ready wait

10$:   OUT   MEMI, SELB, TMTDAT   ;

15$:   BWRTE   IBUS, TMTCON   ;

       BR?   20$;

       ALWAYS   15$;

5.4 KMC11-A PROGRAMMING NOTES

The following information represents some practical aspects of programming the KMC11-A that will be of value to the user.

1. The KMC11 Control and Status Registers (CSR) are implemented with a multiport random access memory (RAM). These CSRs allow the arbitrary selection of bits, bytes, and words for control and/or data transfer. The only requirement is that the PDP11 program and the KMC11 microprogram agree on the bit functions. BSEL 1 is the only portion of the CSRs that the user cannot define. This byte is the Maintenance Register and is defined by the hardware.

2. Since the CSRs are RAM, a power up sequence leaves all bits in random states. As a minimum requirement, the PDP11 program should clear BSEL 1 before any control transfers are attempted.

3. Following power up, the Control Random Access Memory (CRAM) contains random data. Therefore, following power up, RUN (BSEL 1 bit 15) should not be asserted until known microcode resides in the CRAM.

4. A procedure for loading the CRAM and verifying its contents is outlined below.

   Loading Procedure

   a. Write all 0s into BSEL 1.

   b. Load PC (right justified) into SEL 4.

   c. Load CRAM data into SEL 6.

   d. Set ROM O (BSEL 1 bit 10).

e.   Set ROM O (BSEL 1 bit 10) and CRAM WRITE (BSEL 1
     bit 13).

f.   Clear ROM O and CRAM WRITE bits.

g.   Repeat steps b through f as required.

Reading Procedure

a.   Write all 0s into BSEL 1.

b.   Load PC (right justified) into SEL 4.

c.   Set ROM O (BSEL 1 bit 0).

d.   Read SEL 6 which contains CRAM data.

e.   Clear ROM O bit.

f.   Repeat steps b through e as required.

5.   Control transfer between the PDP11 code and the KMC11
     code could be filled with destructive race conditions.
     These control transfers should be interlocked sequential
     procedures. The sequence for a control transfer should
     not allow the possibility of both the PDP11 and the
     KMC11 wanting to write into the same byte at the same
     time. The occurrence of a race condition would cause lost
     data.

     A race-free control transfer initiated by the PDP11 could
     be as follows.

     a.   The PDP11 program asserts the Request bit and encoded
          transfer type.

     b.   The KMC11 responds with an acknowledgement to proceed.

     c.   The PDP-11 program loads data into predefined bytes and
          clears the Request bit.

5-18

d. Observing the clearing of the Request bit, the KMC11 accepts the data and clears the acknowledge bit which completes the transaction.

6. Single bit control functions asserted from either side of the CSRs are guaranteed to be race free. However, a race condition could exist if the request used in item 5, includes one or more bits to define a type of transfer along with the request.

When the request is detected and a service subroutine is entered, the Transfer Type bits should be read again to insure that no bits have been lost.

This procedure is required because the KMC11 may be reading the CSR at the same time that the PDP11 program is writing into it. All bits cannot be written simultaneously so the request may be detected by the KMC11 but the additional function bits may not be detected.

7. The KMC11 is able to do NPRs to any 18 bit address, hang the Unibus, and cause power fail traps as a function of hardware failure. As a precaution, a KMC11 microcode package should include some diagnostic capability; at least as a start up function before it interacts in any way with the PDP11 program.

8. Most common system troubles occur because the Not Last Transfer bit (NPR Control Register bit 1) is used incorrectly or the BA extended bits (16, 17) are not maintained.

9. No bits (except the Not Last Transfer bit) should be
    changed in the KMC11's NPR Control Register, if the NPR
    Request Bit is asserted, because a race condition will be
    introduced. Refer to item 13 for an explanation of the Not
    Last Transfer bit.

10. No bits should be changed in the KMC11's Miscellaneous
    Register if the BR Request bit as asserted because a race
    condition will be introduced.

11. The ACLO bit in the KMC11's Miscellaneous Register is not
    recommended except by DEC.

12. NPR Control Register bits BYTE XFER (C0) and OUT NPR (C1)
    are used as follows:

C0	C1	Function
0	0	NPR from Unibus at IN BA address.
0	1	NPR to Unibus at OUT BA address.
1	0	Do not use.
*1	1	Byte NPR to Unibus at OUT BA address.

    *The LSB of the BA transfer address must always be 0 unless
    code 11 is used. Also, the byte transfer is always sourced
    from the OUT DATA LB register. If the BA LSB is 0, then the
    contents of OUT DATA LB are transfered to the destinations'
    low byte position and the high byte remains undisturbed.
    If the BA LSB is a 1, then the contents of OUT DATA LB is

transferred to the destinations' high byte and the low
byte remains undisturbed.

13. The KMC11-A is capable of maintaining Unibus mastership
     following execution of an NPR transaction. This feature is
     intended to allow the KMC11 to perform multiple NPRs for
     moving data in the minimum time or to enable Read-Modify-Write
     operations on the Unibus. However, the user is cautioned that
     if the Not Last Transfer (NOT LAST XFER) is left asserted
     it locks up the Unibus..

     The following procedure should be used for multiple NPRs.
     It is assumed that the proper BA and NPR data registers
     are maintained.

     a. Assert NOT LAST XFER and NPR RQ (NPR Control Register
         Bits 1 and 0, respectively). The NPR RQ bit self-clears
         at the completion of the NPR and may be reasserted for
         each NPR. The KMC11 retains Unibus mastership during
         this period. That is, no other Unibus transactions are
         possible other than NPRs controlled by the KMC11.

     b. The last required NPR is performed by asserting NPR RQ
         followed by the clearing of NOT LAST XFER in the next
         KMC11 instruction. Clearing NOT LAST XFER drops BUS
         SACK and allows Unibus arbitration for the next master
         while the last NPR is in progress.

When NPR RQ is cleared again, Unibus mastership is
relinquished.

NOT LAST XFER may also be cleared if NPR RQ is already
cleared and the KMC11 is Unibus master. In this case,
the immediate clearing of BUS SACK and relinquishing
of Unibus mastership occurs. However, this sequence
is in violation of the Unibus Specifications.

5.5   DMC11 LINE UNIT PROGRAMMING NOTES

1.   Transmit Start of Message (TSOM) and Transmit End of Message
(TEOM) are bits 0 and 1 of the Out Control Register. TSOM
and TEOM are loaded into this register by the microprocessor.
These bits are sent from the Out Control Register to the
Transmitter Buffer when the microprocessor loads a character
(sync, data, etc.) into the Out Data Silo Register. If set,
the control bit (TSOM or TEOM) goes along with the character.
However, the load signal for the Out Data Silo also clocks
the TSIP flip-flop which clears the TSOM and TEOM bits in
the Out Control Register.

Therefore, always load the TSOM or TEOM bit into the Out
Control Register before loading the Out Data Silo. The
control information is cleared from this register automatically
as the Out Data Silo accepts the data.

In the Bit Stuff mode, the data written into the Out Data
Silo with either TSOM or TEOM is lost. This is an internal
function that is performed automatically by the transmitter

control logic. Physically, this is accomplished by inhibiting the loading of the Transmitter Data Shift Register.

In place of the shift register output, the transmitter control logic transmits a flag character when TSOM is set and it sends the transmitter CRC check character when TEOM is set. If both TEOM and TSOM are set, 16 zeroes are sent.

3. BCC MATCH and BLOCK END are bits 0 and 1 of the In Control Register. Physically, they are part of the 3341 FIFOs that constitute the In Data Silo. When the 8 data bits of the In Data Silo are read by the microprocessor, BCC MATCH and BLOCK END are lost. These bits are read as part of the In Control Register.

    Therefore, always read the In Control Register before reading the In Data Silo.

4. In the DDCMP mode, the BCC MATCH flag is presented with the CRC check character that produced the match information.

    In the Bit Stuff mode, the BLOCK END bit is asserted when the terminating flag has been received. This bit is loaded with the high byte of the CRC Check Character. Therefore, the BCC MATCH bit along with the BLOCK END bit should be used to indicate reception of an errorless message.

5. The Request to Send (RS) function is read only to the
    microcode. The line unit control logic asserts RS when
    data is available in the Out Data Silo. The delay between
    assertion of RS and assertion of Clear to Send (CS)
    determines the time that the microcode has to provide silo
    depth before serial transmission of data starts.

    For the DMC11-DA and FA Line Units, the CS delay is a
    function of the modem used. The DMC11-MD CS delay is about
    90 us and the DMC11-MA CS delay is about 100us.

6. A transmitter underrun condition occurs if data is not
    present at the bottom of the Out Data Silo when the
    transmit logic is ready for a character. This condition
    is not flagged by the hardware and it can occur if an
    EOM is not used to terminate a message.

    The transmitter automatically sends all 1s for a
    minimum of one character time before dropping RS. For the
    DMC11-DA and FA Line Units, the all 1s data stream length
    is determined by the modem/DSU used. For the DMC11-MA and
    MD Line Units, the all 1s data stream occurs for at least
    15 bits.

    In bit stuff mode, the all 1s sequence is recognized as
    an ABORT sequence because no 0s are stuffed.

    In character oriented mode, only those protocols with

proper error detection methods can recover easily from this
condition. Such a protocl is DDCMP.

7. The In Data Silo does not have an overrun indicator. It
   is assumed that the high speed of the KMC11 microprocessor
   precludes the requirement for an overrun indicator.

   Protocols with proper error detection methods, such as
   DDCMP, detect this condition as a CRC error. Protocols
   that rely on a specific bit sequence to terminate a
   message or protocols with indeterminate size messages
   may loose data and be unable to detect the overrun.

8. For bit stuff protocols, two Transmit Start of Message
   (TSOM) control transfers are always required to start
   transmission of a new block of information. This causes
   two flag characters to be transmitted on the serial
   output line.

APPENDIX A

PDP-11 MEMORY ORGANIZATION

AND ADDRESSING CONVENTIONS

The PDP-11 memory is organized in 16-bit words consisting of two
8-bit bytes. Each byte is addressable and has its own address
location; low bytes are even numbered and high bytes are odd
numbered. Words are addressed at even numbered locations only
and the high (odd) byte of the word is automatically included to
provide a 16-bit word. Consecutive words are therefore found in
even numbered addresses. A byte operation addresses an odd or
even location to select an 8-bit byte.

The Unibus address word contains 18 bits identified as A(17:00).
Eighteen bits provide the capability of addressing 256K memory
locations each of which is an 8-bit byte. This also represents
128K 16-bit words. In this discussion, the multipler K equals
1024 so that 256K represents 262,144 locations and 238K represents
131,072 locations. The maximum memory size can be used only by a
PDP-11 processor with a memory management unit that utilizes all
18 address bits. Without this unit, the processor provides 16
address bits which limits the maximum memory size to 64K (65,536)
bytes or 32K (32,768) words.

Figure A-1 shows the organization for the maximum memory size of
256K bytes. In the binary system, 18 bits can specify 2^{18} or
262,144 (256K) locations. The octal numbering system is used to

designate the address. This provides convenience in converting
the address to the binary system that the processor uses as
shown below.

The highest 8K address locations (760000-77777) are reserved for
internal general registers and peripheral devices. There is no
physical memory for these addresses; only the numbers are
reserved. As a result, programmable memory locations cannot be
assigned in this area; therefore, the user has 248 bytes or 124K
words to program.

A PDP-11 processor without the memory management unit provides
16 address bits that specify 2^{16} or 65,536 (64K) locations
(Figure A-2). The maximum memory size is 65,536 (64K) bytes or
32,768 (32K) words. Logic in the processor forces address bits
A(17:16) to 1s if bits A(15:13) are all 1s when the processor
is master to allow generation of addresses in the reserved area
with only 16-bit control.

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	ADDRESS BIT
0	0	1	0	0	1	1	1	1	1	1	0	0	0	0	0	1	0	BINARY
1			1			7			6			0			1			OCTAL

```
         |15        08|07        00|
         |←—  16 BIT DATA WORD —→|

           HIGH BYTE   LOW BYTE
 000001   ┌──────────┬──────────┐  000000       USER ADDRESS SPACE
 000003   ├──────────┼──────────┤  000002       AVAILABLE USING 18
          │          │          │               ADDRESS BITS ON
          │          │          │               PDP-11 PROCESSOR
          └──────────┴──────────┘            ⎫  WITH MEMORY
                                             ⎬  MANAGEMENT OPTION.
          ┌──────────┬──────────┐               INCLUDES 248K(253,952)
          │          │          │               BYTES OR 124K(126,976)
          │          │          │               WORDS.
 757777   ├──────────┼──────────┤  757776
 760001   ├──────────┼──────────┤  760000
          │          │          │
          └──────────┴──────────┘               HIGHEST 8K (8192)
                                                BYTES OR 4K (4096)
          ┌──────────┬──────────┐            ⎬  WORDS RESERVED FOR
          │          │          │               DEVICE REGISTER
          │          │          │               ADDRESSES.
 *777777  └──────────┴──────────┘  777776
```

LAST ADDRESS IS BYTE NUMBER $262,143_{10}$

* MAXIMUM SIZE WITH 18 ADDRESS BITS IS 256K(262,144) BYTES OR 128K(131,072)WORDS.

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Figure A-1   Memory Organization for Maximum Size Using

18 Address Bits
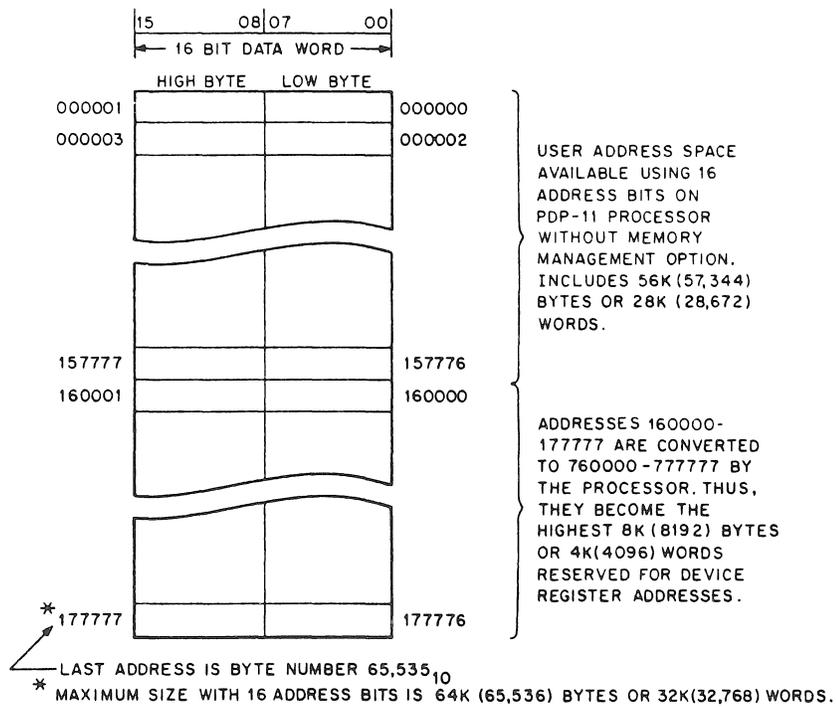
Figure A-2 Memory Organization for Maximum Size Using

16 Address Bits

Bit 13 becomes a 1 first at octal 160000 which is decimal 57,344
(56K). This is the beginning of the last 8K bytes of the 64K
byte memory. The processor converts locations 160000-177777 to
760000-777777 which relocates these last 8K bytes (4K words) to
the highest locations accessible by the bus. These are the
locations that are reserved for internal general register and
peripheral device addresses; therefore, the user has 57,344 (56K)
bytes or 28,672 (28K) words to program.

Memory capacities of 56K bytes (28K words) or under do not have
the problem of interference with the reserved area, because
designations less than 160000 do not have a binary 1 in bit A13.
No addresses are converted and there is no possibility of physical
memory locations interfering with the reserved space.

PDP-11 core memories are available in 4K or 8K increments. The
highest location of various size core memories are shown below.

| Memory Size | | Highest Location |
K-Words	K-Bytes	(Octal)
4	8	017777
8	16	037777
12	24	057777
16	32	077777
20	40	117777
24	48	137777
28	56	157777

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