digital

VT100

SERIES
VIDEO TERMINAL
TECHNICAL MANUAL

EK-VT100-TM-003

VT100 SERIES VIDEO TERMINAL TECHNICAL MANUAL

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of
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CHAPTER 1
INTRODUCTION AND SPECIFICATIONS

This is the technical manual for the VT100 series video terminals. It contains information a service technician or engineer needs to operate, test, and repair the VT100 series to a component level.

Chapter 1	Contains VT100 specifications and documentation ordering information.
Chapter 2	Contains basic operator information, including use of the keyboard, use of SET-UP modes for setting terminal characteristics, and simple trouble checking.
Chapter 3	Contains installation procedures and interface information.
Chapter 4	Contains a technical description of the basic VT100 video terminal. This chapter assumes that the reader has the Field Engineering Print Set, MP00633.
Chapter 5	Contains servicing information for the VT100 series video terminals.
Chapter 6	Contains SET-UP information for the various VT100 series options, installation information, a technical description, and service information for the Advanced Video option, Current Loop option, VT105 Graphics Processor, VT1XX-AC Printer option, and VT125 Graphics Processor.
Chapter 7	Contains a technical description and interfacing information for the standard terminal port (STP).
Chapter 8	Contains interfacing information for the graphics connector.
Appendix A	Contains programming information for the VT100 series, including interface timing considerations and descriptions of control functions the VT100 responds to, both in ANSI mode and in DEC VT52-compatible mode. Also contains copy of VT125 Programming Reference Card, EK-VT125-RC-001.
Appendix B	Contains a recommended spares list (RSL).
Appendix C	Contains a glossary of terms and abbreviations used in this manual.
Appendix D	Contains a description of the ANSI code extension techniques.

VT100 SPECIFICATIONS

DIMENSIONS

Monitor

Height	36.83 cm (14.5 inch)
Width	45.72 cm (18 inch)
Depth	36.20 cm (14.25 inch)

Keyboard

Height	8.89 cm (3.5 inch)
Width	45.72 cm (18 inch)
Depth	20.32 cm (8 inch)
Minimum table depth	51.4 cm (20.25 inch)

Weight

Monitor	13.6 kg (30 lb)
Keyboard	2.0 kg (4.5 lb)
Shipping weight	18.6 kg (41 lb)

ENVIRONMENTAL

Operating

Temperature	10° to 40° C (50° to 104° F)
Relative humidity	10% to 90%
Maximum wet bulb	28° C (82° F)
Minimum dew point	2° C (36° F)
Altitude	2.4 km (8,000 ft)

Nonoperating

Temperature	−40° to 66° C (−40° to 151° F)
Relative humidity	0 to 95%
Altitude	9.1 km (30,000 ft)

Power

Line voltage	90–128 V rms single phase, 2 wire 180–256 V rms single phase, 2 wire (switch-selectable)
Line frequency	47–63 Hz
Current	3.0 A rms maximum at 115 V rms 1.5 A rms maximum at 230 V rms
Input power	250 VA apparent 150 W max.
Current limiting	3 A normal blow fuse
Power cord	Detachable, 3 prong, 1.9 m (6 ft)

Display	
CRT	30 cm (12 inch) diagonal measure, P4 phosphor
Format	24 lines × 80 characters or 14 lines × 132 characters (selectable)
Character	7 × 9 dot matrix with descenders
Character size	
80 column mode	3.35 mm × 2.0 mm (0.132 inch × 0.078 inch)
132 column mode	3.35 mm × 1.3 mm (0.132 inch × 0.051 inch)
Active display size	203 mm × 127 mm (8 inch × 5 inch)
Character set	96-character displayable ASCII subset (upper- and lowercase, numeric, and punctuation)
Cursor type	Keyboard-selectable, blinking block character or blinking underline
Keyboard	
General	83-key detachable unit with 1.9 m (6 ft) coiled cord attached
Key layout	65-key arrangement and sculpturing similar to standard typewriter, with 18-key numeric keypad.
Numeric keypad	18-key with period, comma, minus, enter, and four general purpose function keys.
Visual indicators	7 LEDs; 3 dedicated to ON LINE, LOCAL, and KBD LOCKED; 4 are user-programmable.
Audible signals	
Keyclick	Sound simulates typewriter.
Bell	1) sounds upon receipt of BEL code; 2) sounds 8 characters from right margin (keyboard-selectable).
Multiple bell	Sounds upon detection of error in SET-UP save or recall operation.
Communication	
Type	EIA
Speeds	Full duplex: 50, 75, 110 (two stop bits), 134.5, 150, 200, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 9600, 19,200
Code	ASCII
Character format	Asynchronous
Character size	7 or 8 bits; keyboard-selectable. (Note: if 8-bit character is selected, 8th bit is always space.)
Parity	Even, odd, or none (keyboard-selectable)
Synchronization	Keyboard-selectable via automatic generation of XON and XOFF control codes.

ORDERING DOCUMENTATION

You can purchase the following VT100 series video terminal documents from DIGITAL's Accessories and Supplies Group.

Title	Part Number
VT100 User Guide	EK-VT100-UG
VT100 Series Pocket Service Guide	EK-VT100-J1
VT100 Illustrated Parts Breakdown (IPB)	EK-VT100-IP
VT100 Print Set (contains VT1XX-AC)	MP-00633
VT105 Technical Manual	EK-VT105-TM
VT105 Illustrated Parts Breakdown (IPB)	EK-VT105-IP
VT105 Print Set	MP-00642
VT125 User Guide	EK-VT125-UG
VT125 Print Set	MP-01053
VT1XX-CB, -CL Print Set	MP-01052
VT125 Illustrated Parts Breakdown (IPB)	EK-VT125-IP
VT132 User Guide	EK-VT132-UG
VT132 Print Set (contains VT1XX-AC)	MP-00748
VT132 Illustrated Parts Breakdown (IPB)	EK-VT125-IP
VT1XX-AC User Guide	EK-VT1AC-UG
VT1XX-AC Print Set	MP-00901

You can order accessories and supplies (including documentation) by mail or phone.

Continental USA

Call 800-258-1710 or mail order to:

Digital Equipment Corporation
P.O. Box CS2008
Nashua, NH 03061

New Hampshire

Call 602-884-6660 or mail order to:

Digital Equipment Corporation
P.O. Box CS2008
Nashua, NH 03061

Alaska or Hawaii

Call 408-734-4915 or mail order to:

Digital Equipment Corporation
632 Caribbean Drive
Sunnyvale, CA 94086

Canada

Call 800-267-6146 or mail order to:
Digital Equipment Corporation
P.O. Box 13000
Kanata, Ontario Canada K2K 2A6
Att: A&SG Business Manager
Telex: 610-562-8732

Related Documentation

Intel 8080 Microcomputer Systems User's Manual
From: Intel Corporation
3065 Bowers Avenue
Santa Clara, California 95051

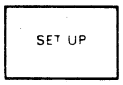
EIA Specifications RS-232-C and RS-170
From: Electronic Industry Association
EIA Engineering Department
2001 Eye Street, N.W.
Washington, DC 20006

ANSI Standards X3.41-1974, X3.64-1977, 3.4-1977
From: Sales Department
American National Standards Institute
1430 Broadway
New York, NY 10018

CHAPTER 2
OPERATOR INFORMATION

PART 1 KEYBOARD CONTROLS AND INDICATORS

The VT100 terminal normally performs a two-part function. It is an input device to a computer – information entered through the keyboard is sent to the computer. It is simultaneously an output device for the computer – that is, data coming in from the computer is displayed on the video screen. The following controls and indicators on the VT100 keyboard are illustrated in Figure 2-1.



SET-UP Key

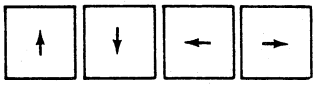
Used in conjunction with other keys to perform specific functions such as setting tabs, scrolling, and altering terminal characteristics.

ON LINE Indicator
Lights to show that the VT100 is on-line and ready to transmit or receive messages.

LOCAL Indicator
Lights to show that the terminal is off-line and cannot communicate with the host device. In local mode the keyboard remains active and all characters typed are placed on the screen.

KBD LOCKED Indicator
Lights to show the keyboard has been turned off. The VT100 is still able to receive data from the host. This condition can be cleared by entering and exiting SET-UP mode.

L1–L4 Indicators
These indicators are turned on and off by the host. Consult your local operating procedures for the meaning of each indicator. L1–L4 also show self-test errors.



Keys

Each of these keys causes the VT100 to transmit a code that has a special meaning to your system. Consult your local operating procedures for the meaning of these keys. In SET-UP mode the ↑ and ↓ keys increase or decrease display brightness. The ← and → keys move the cursor left and right.

BACKSPACE Key

Transmits a backspace code.

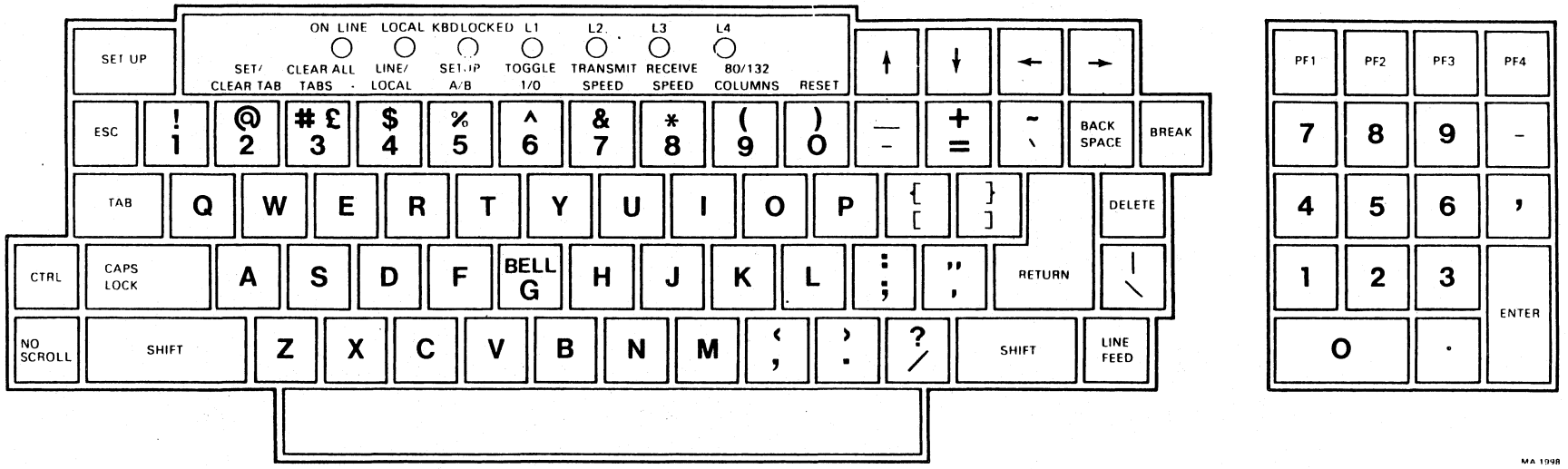
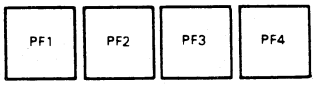


Figure 2-1 VT100 Keyboard

BREAK Key

Transmits a break signal.



PF1–F4 Keys

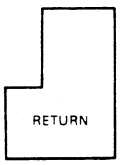
Each of these keys causes the VT100 to transmit a code that has a special meaning to your system. Consult your local operating procedures for the meanings of these keys.

Numeric Keypad

The numeric keypad enables numbers to be entered in calculator fashion. Each key in the numeric keypad generates the same character as the corresponding numeric key on the main keyboard. The **ENTER** key corresponds to the **RETURN** key. These keys may also be interpreted by the host computer as special function keys. Consult your local operating procedures for the meanings of these keys.

DELETE Key

Causes the VT100 to transmit a delete character code to the host system. The deleted character may or may not be erased from the screen.

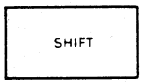


RETURN Key

Transmits either a carriage return (CR) code or a carriage return and line feed (LF) code. This is a SET-UP selectable feature.

LINEFEED Key

This key transmits a line feed code.



SHIFT Key

When pressed, this key enables the uppercase function of all keys. If a key does not have an uppercase function the SHIFT key is disregarded.

RESET Key

In SET-UP mode this key starts the reset sequence. This has the same result as turning the terminal power off and then on.

(9

80/132 COLUMNS Key

In SET-UP A mode this key switches the display line size from 80 to 132 characters per line or from 132 to 80 characters per line.

* 8

RECEIVE SPEED Key

In SET-UP B mode this key steps the terminal through the receive baud rate settings in ascending order.

& 7

TRANSMIT SPEED Key

In SET-UP B mode this key steps the terminal through the transmit baud rate settings in ascending order.

^ 6

TOGGLE 1/0 Key

In SET-UP B mode this key turns the selected operational feature on or off.

BELL G

BELL Key

When pressed in combination with the **CTRL** key this key causes a bell code to be sent to the host.

% 5

SET-UP A/B Key

In SET-UP mode this key switches the terminal from SET-UP A to SET-UP B or from SET-UP B to SET-UP A.

$ 4

LINE/LOCAL Key

In SET-UP mode this key switches the VT100 to communicate with your system (ON LINE) or stops the VT100 from communicating with your system (LOCAL).

£ 3

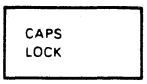
CLEAR ALL TABS Key

In SET-UP A this key clears all horizontal tabs set in the VT100.

@ 2

SET/CLEAR TAB Key

In SET-UP A this key sets or clears individual horizontal tabs.



CAPS LOCK Key

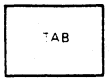
This key enables the transmission of uppercase alphabetic characters only. All numeric and special symbol keys remain in lowercase.

NO SCROLL Key

When first pressed, this key stops the transmission of data from the computer to the VT100. When pressed a second time, transmission resumes from where it was stopped. Check your local operating procedures to ensure that your system recognizes this key.

CTRL Key

When pressed in combination with another key, **CTRL** causes the VT100 to transmit a code that has a special meaning to your system.



TAB Key

This key transmits a tab code.

ESC Key

This key transmits a code that normally has a special meaning to your system. In many applications, it tells your system to treat the next keys pressed as a command.

MONITOR CONTROL

The VT100 monitor contains only one control, the power switch, shown in Figure 2-2.

AUDIBLE INDICATORS (TONES)

There are three audible indicators associated with the VT100: a short tone (click), a long tone (beep), and a series of long tones.

Short Tone (click)

The short tone sounds whenever a key is pressed, with the following exceptions:

- **SHIFT** or **CTRL** keys do not generate any keyclick because these keys do not transmit any codes but only modify the codes transmitted by other keys.
- When the KBD LOCKED indicator is turned on; in which case, the characters typed are lost.
- The keyclick feature has been turned off in SET-UP mode.

Long Tone (beep)
The long tone sounds to indicate one of the following conditions:

- A bell code was received from the computer.
- The cursor is eight characters away from the right margin and the margin bell feature is enabled.

Series of Long Tones
The terminal sounds the long tone several times in rapid succession to indicate that the nonvolatile memory (NVR) had difficulty reading or writing SET-UP features. (When this occurs, check the SET-UP features and then perform the recall or save operation again.)

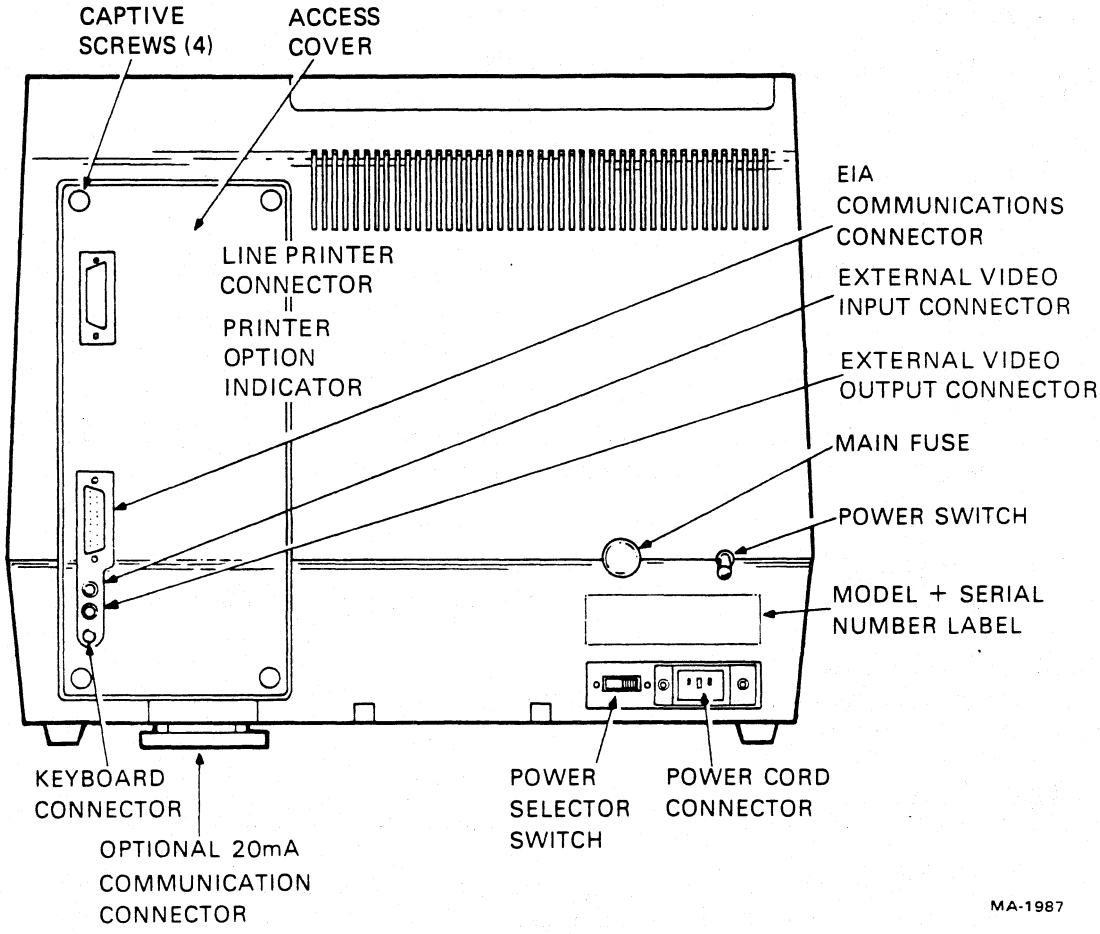


Figure 2-2 VT100 Terminal (Rear View)

PART 2 SET-UP MODE

Unlike most terminals, the VT100 does not use switches or jumpers to individually turn the built-in terminal features on or off. Instead, the VT100 uses a nonvolatile memory (NVR) that always remembers what features have been selected, as if a switch had been set.

Selection and storage of built-in terminal features is performed in a special mode of operation called SET-UP mode. When you enter SET-UP mode, the status of features stored in temporary memory shows on the screen. You can then change the features and store any new feature selections either temporarily, by leaving SET-UP mode; or on a fixed basis, by performing a Save operation. In either case, terminal operation reflects the new feature selection. If a recall operation is performed, or the terminal is reset, or terminal power is turned off, all temporary feature settings are replaced by features that have been stored on a fixed basis.

SET-UP Features

SET-UP mode provides two brief summaries of the current feature status. The first presentation – SET-UP A – displays the location of tab stops set and a visual ruler that numbers each character position on the line. The second presentation – SET-UP B – summarizes the status of the other terminal features.

SET-UP A – To enter SET-UP A, press the **SET-UP** key. The display has a presentation similar to Figure 2-3. The bottom line of the display consists of a "ruler" that numbers each character position available on a line. Each tab stop is shown by a "T" above the ruler. If the tab stop(s) set are those desired, you may exit **SET-UP** mode by pressing the SET-UP key again or you may now change the tabs to meet your requirements.

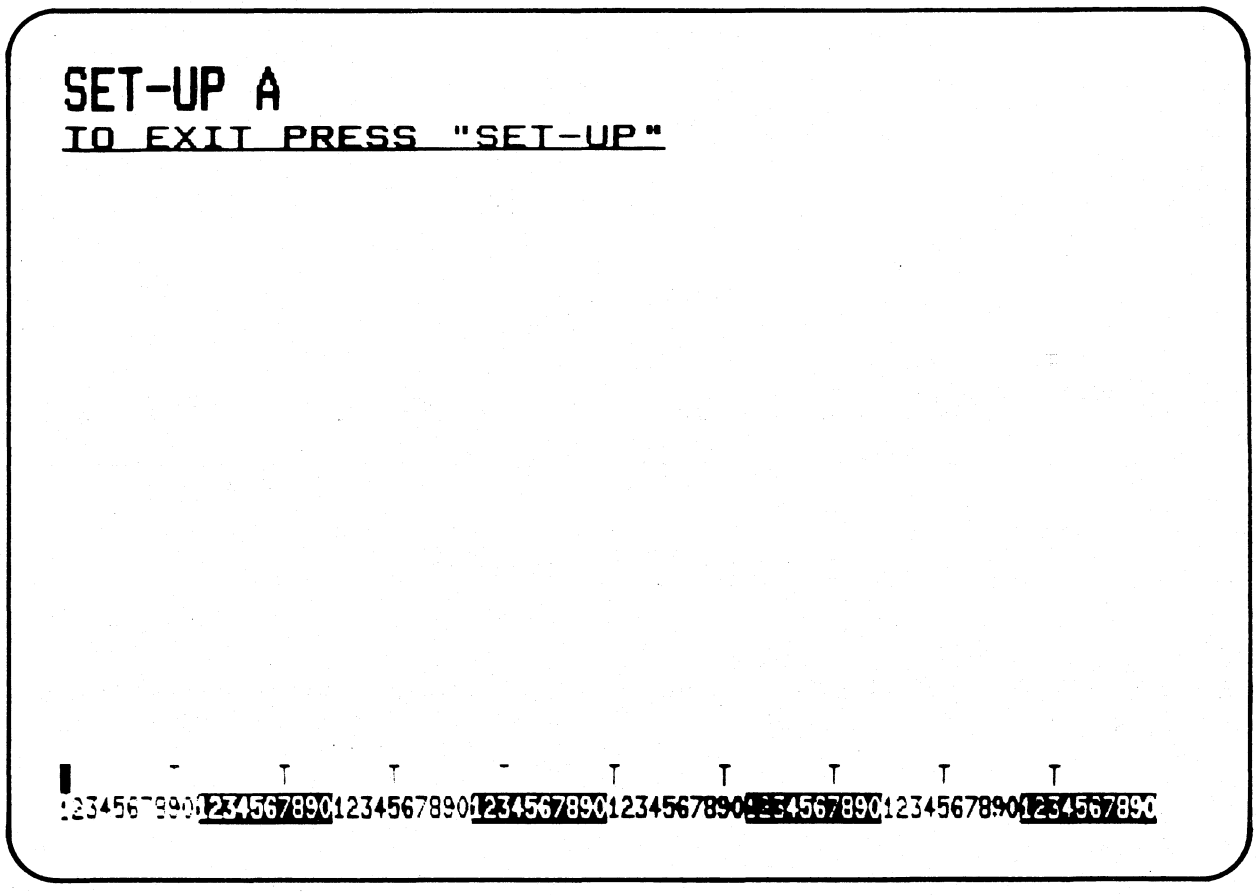


Figure 2-3 SET-UP A Mode Presentation

SET-UP B – SET-UP B mode may only be entered from SET-UP A mode. To enter SET-UP B from SET-UP A press the **5** key on the main keyboard. The display looks like Figure 2-4. Figure 2-5 summarizes the SET-UP B presentation. This summary allows you to quickly determine what features are enabled. For additional information on a feature refer to in Part 3, SET-UP Feature Definitions.

To exit SET-UP B press the **SET-UP** key.

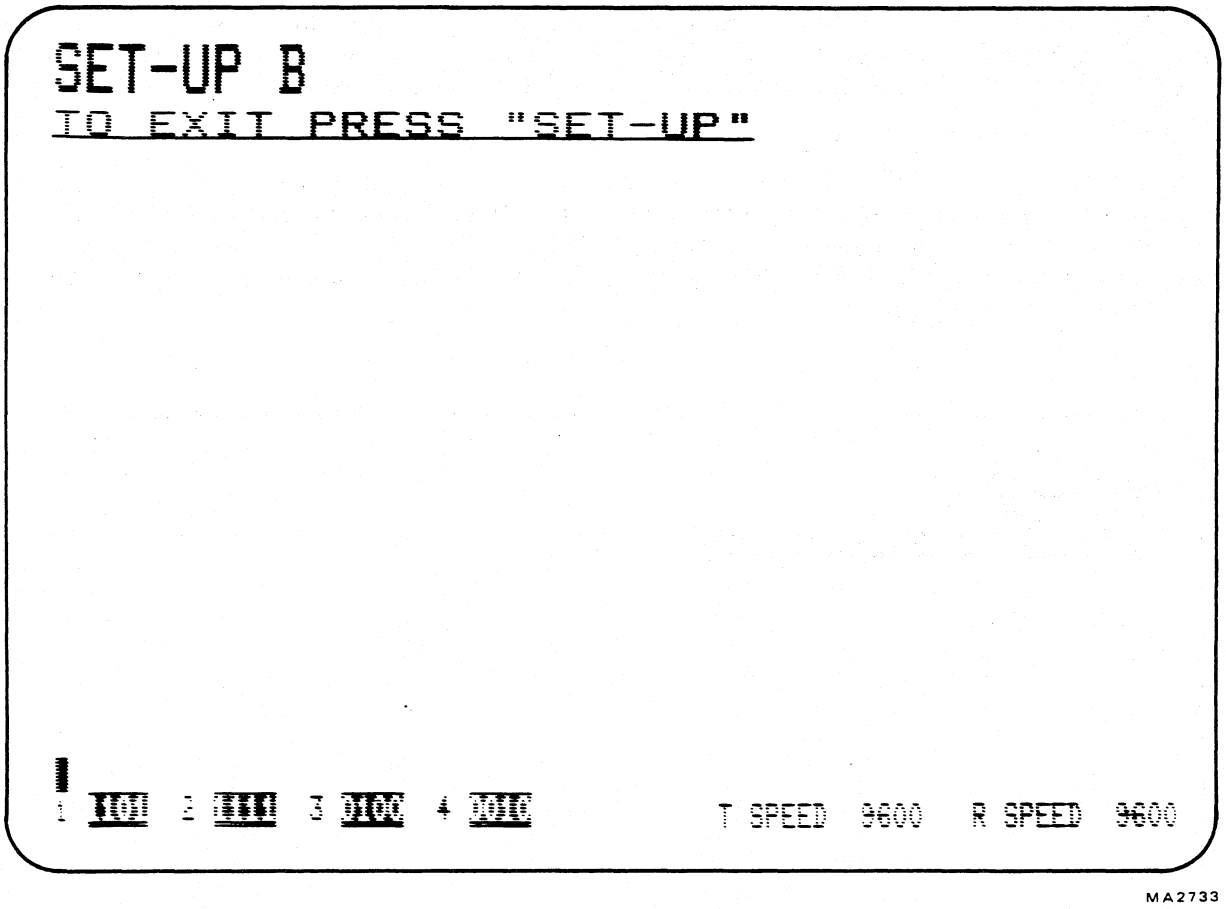


Figure 2-4 SET-UP B Mode Presentation

Determining What a SET-UP Feature Does
SET-UP features are basically a series of options in the VT100 that allow the terminal to be tailored to its operating environment. Table 2-1 lists each feature and shows one of the following general categories.

Installation
Computer compatability
Operator comfort

The installation category includes the initial installation of the terminal and any special options that may be attached to the terminal. If any options are added or removed, or the physical location of the terminal is changed, verify the settings of these SET-UP features.

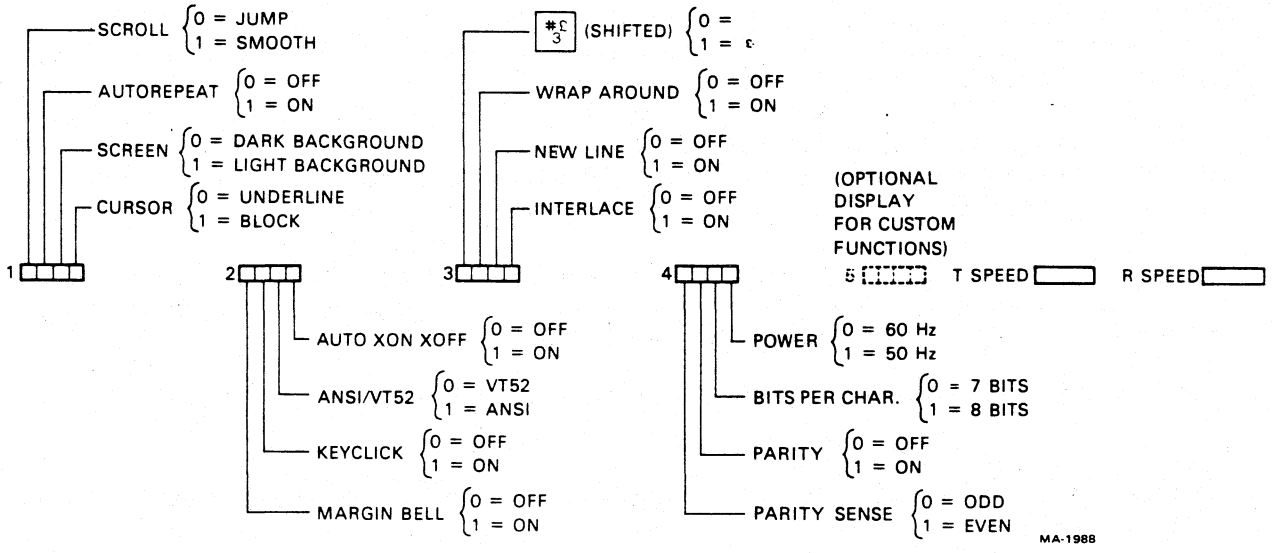


Figure 2-5 SET-UP B Mode Summary

Table 2-1 Categories of SET-UP Features

Feature	Installation	Computer Compatibility	Operator Comfort
Ansi/VT52 mode		X	
Answerback message		X	
Auto Repeat			X
Auto XON/XOFF		X	
Bits per Character		X	
Characters per Line		X	
Cursor			X
Interlace	X		
Keyclick			X
Line/Local		X	
Margin Bell			X
New Line		X	
Parity		X	
Parity Sense		X	
Power	X		
Receive Speed		X	
Screen Background			X
Screen Brightness			X
Scroll		X	X
Tabs		X	
Transmit Speed		X	
Wraparound		X	
# £ 3 (shifted)		X	

Computer compatibility contains the features that must be set correctly so that the VT100 can communicate with the host computer. An error in these settings may cause incorrect data to be sent to or received from the computer; or an error may prevent the VT100 from communicating with the computer. The settings for these features must be obtained from the host computer programmer, operator, or system manager since there are many combinations of settings designed to work with particular computers and special software. These feature settings normally change only when you need to communicate with a different computer or a unique software package.

The operator comfort category contains SET-UP features designed exclusively for the operator. These features allow the operator to tailor the VT100 to fit individual preference. These features do not affect any operations that occur between the terminal and the computer.

Part 3, SET-UP Feature Definitions, describes the specific function of each feature.

How to Change a SET-UP Feature
Changing any or all SET-UP features is a simple operation and is generally performed by following the same basic steps.

1. Enter SET-UP mode by pressing the **SET-UP** key.

2. Select the appropriate SET-UP mode by pressing the **5** key on the main keyboard each time you want to switch from SET-UP A to SET-UP B or from SET-UP B to SET-UP A.

3. Position the cursor above the feature switch or tab stop to be changed. To position the cursor, the **SPACE** bar, ←, →, **TAB**, and **RETURN** keys may be used. Some features do not use this step since a specific key is dedicated to changing the feature.

4. Change the feature setting by pressing either the **6** key on the main keyboard or the appropriate dedicated key. Each time the key is pressed the feature changes, generally to the opposite state.

Table 2-2 briefly summarizes SET-UP features, the SET-UP mode you must be in to change a feature, and the key used to change the feature setting.

Table 2-2 SET-UP Feature Change Summary

Feature	Changed In SET-UP Mode	Key to Change Feature
Answerback message	B	*
ANSI/VT52 mode	B	^ 6
Auto Repeat	B	^ 6
Auto XON/XOFF	B	^ 6
Bits per Character	B	^ 6
Brightness	A	↑ ↓

* A special sequence is required for this feature. See the detailed features description.

Table 2-2 SET-UP Feature Change Summary (Cont)

Feature	Changed In SET-UP Mode	Key to Change Feature
Characters per Line	A	(9
Cursor	B	^ 6
Interlace	B	^ 6
Keyclick	B	^ 6
Line/Local	A	$ 4
Margin Bell	B	^ 6
New Line	B	^ 6
Parity	B	^ 6
Parity Sense	B	^ 6
Power	B	^ 6
Receive Speed	B	* 8
Screen	B	^ 6
Scroll	B	^ 6
Tabs	A	@ 2 and # £ 3
Transmit Speed	B	& 7
Wraparound	B	^ 6
# £ 3 (shifted)	B	^ 6

Setting the Answerback Message

Setting the answerback message differs from setting any other terminal feature. An answerback message can be typed into the VT100, using the following steps.

1. Place the terminal in SET-UP B mode.
2. Press the **SHIFT** and **A** keys at the same time. The terminal responds by placing A = on the screen. (The **SHIFT** key is required. The **CAPS LOCK** key does not work here.)

3. Type the message delimiter character which may be any character not used in the actual answerback message. The message delimiter character is not part of the answerback message. If a mistake is made when typing the answerback message, type the message delimiter character again and go back to step 2. This is the *only* way to correct errors in the answerback message.

4. Type the answerback message. The message may be up to 20 characters, including space and control characters. Control characters are displayed as a character to indicate their presence in the message.

5. Type the message delimiter character. Once the message delimiter character is typed the answerback message disappears from the screen.

Once the above steps have been completed the answerback message is temporarily stored in the VT100 and can be saved with the save operation.

Saving SET-UP Features

SET-UP features may be changed and stored on either a temporary or a fixed basis. To temporarily store a feature, exit SET-UP mode after changing the feature; the terminal now reacts according to the new setting. If a recall operation is performed, or the terminal is reset, or terminal power is turned off, all temporary feature settings are replaced by the features that have been stored on a fixed basis.

To store SET-UP feature settings on a fixed basis, perform a save operation. This is a simple operation that is accomplished by performing the following steps.

1. Place the terminal in SET-UP mode.

2. Press the **SHIFT** and **S** keys at the same time. The screen clears and the message "Wait" is displayed in the upper-left corner. After a brief wait, the terminal returns to SET-UP A mode.

NOTE

The save operation must be performed at the terminal keyboard. The computer cannot perform this operation, although it can temporarily modify the setting of VT100 features.

Once these steps have been performed, SET-UP features which had been temporarily stored are now stored on a fixed basis.

Recalling SET-UP Features

Temporarily stored SET-UP feature settings may differ from settings that are stored on a fixed basis. To return to the fixed settings, perform the recall operation as follows.

1. Place the terminal in SET-UP mode.

2. Press the **SHIFT** and **R** keys at the same time. The screen clears and the message "Wait" appears in the upper-left corner. After a brief wait the terminal returns to SET-UP A mode.

NOTE

When a recall operation is performed the contents of the screen are destroyed.

Resetting the Terminal
The VT100 may be reset from the keyboard. When the terminal is reset, the terminal memory is cleared and the self-test program runs as if the terminal power switch was turned off and then back on. To reset the terminal:

1. Place the terminal in SET-UP mode.

2. Press the **O** key on the main keyboard. The VT100 is reset, the power on self-test runs, and the terminal reacts according to the fixed SET-UP features.

NOTE
When a reset operation is performed the contents of the screen are destroyed.

PART 3 DEFINITIONS SET-UP FEATURE

This section describes each SET-UP feature in detail (in alphabetical order) and states how each feature affects the terminal.

NOTE
Unless otherwise stated, entering SET-UP mode and changing features does not result in the loss of data displayed on the screen.

ANSI/VT52 Mode
The VT100 terminal follows two programming standards - American National Standards Institute (ANSI) and VT52. In ANSI mode, the VT100 generates and responds to coded sequences per ANSI standards X3.41-1974 and X3.64-1977. In VT52 mode, the VT100 terminal is compatible with previous DIGITAL software using the VT52 video terminal. Both ANSI and VT52 modes are outlined in Appendix A of this manual.

Answerback Message
Answerback is a question and answer sequence where the host computer asks the terminal to identify itself. This feature allows the terminal to identify itself by sending a message to the host. The entire answerback sequence takes place automatically without affecting the screen or requiring operator action. The answerback message may also be transmitted by pressing the **CTRL** and **BREAK** Keys at the same time.

Auto Repeat
Auto repeat allows a key to be automatically repeated at the rate of about 30 characters per second when the key is held down for more than one-half second. The auto repeat feature affects all keyboard keys except the following:

SET-UP
ESC
NO SCROLL
TAB
RETURN
CTRL and any key

Auto XON/XOFF
The VT100 can automatically generate synchronizing codes XON (DC1) and XOFF (DC3). XOFF stops data transmission from the computer to the terminal; XON resumes transmission. With the feature enabled, the VT100 generates the XOFF code when one of the following occurs:

1. the internal buffer is nearly full
2. the **NO SCROLL** key is pressed
3. the terminal is placed in SET-UP mode
4. **CTRL-S** is pressed.

When the buffer empties, the **NO SCROLL** key is pressed again, the terminal is taken out of SET-UP mode, or **CTRL-Q** is pressed, the VT100 transmits the XON code to resume transmission from computer to terminal.

If the host computer software does not support the XON/XOFF codes, data sent during buffer full conditions, or when the terminal is in SET-UP mode, may be lost.

NOTE
The VT100 always stops transmission when an XOFF (DC3) code is received and resumes transmission when an XON (DC1) code is received regardless of the Auto XON/XOFF feature setting.

Bits per Character
This feature allows the terminal to transmit and receive either 7- or 8-bit characters. When set for 8-bit operation, bit 8 is set to a space (or 0) for characters transmitted and is ignored for all characters received.

Characters per Line
The VT100 can display either 80 or 132 characters per line. In 80 character per line mode, the screen is 80 characters wide by 24 lines high. In 132 character per line mode, the screen is 132 characters wide by 14 lines high (24 lines if the VT100 is equipped with the Advanced Video Option). In 132 character per line mode, the displayed lines are physically the same width as 80 character per line mode but the characters are more compact.

NOTE
When changing from 80 to 132 character per line mode or vice versa, the current contents of the screen are lost.

Cursor
The VT100 has two cursor displays to indicate the "active positions" or where the next character will be placed on the screen. The cursor may be displayed as either a blinking underline (—) or a blinking block (■). The cursor selection may perform an additional function; see the SGR escape sequence definition in Appendix A.

Interlace
This feature is used for high resolution options. The interlace feature should be turned off if such an option is not installed.

Keyclick Tone
The keyclick is a tone that sounds every time a key is pressed. The keyclick may be turned on or off to suit the operator's needs. However, research and experience has shown that an operator is more accurate when there is audible feedback from the keyboard. Like the bell tone, the keyclick volume *is not adjustable*.

LINE/LOCAL
The LINE/LOCAL feature allows the operator to easily place the terminal in either an ON-LINE or a LOCAL (off-line) condition. When the terminal is on-line (ON-LINE indicator is lit) all characters typed on the keyboard are sent directly to the computer and messages from the computer are displayed on the screen. In the LOCAL condition (LOCAL indicator is lit), the terminal is electrically disconnected from the computer; messages are not sent to or received from the computer; and characters typed on the keyboard are echoed on the screen directly.

Margin Bell
The margin bell feature is much the same as the bell in a typewriter. If the cursor is eight characters from the end of the current line while typing, the VT100 sounds a tone to alert the operator.

New Line
The new line feature enables the **RETURN** key on the terminal to function like the return key on an electric typewriter. When the new line feature is enabled, pressing the **RETURN** key generates the carriage return (CR) and line feed (LF) codes. When a line feed code is received, the code is interpreted as a carriage return and line feed.

When the new line feature is disabled, the **RETURN** key generates only the CR code; an LF code causes the terminal to perform a line feed only.

NOTE

If double line feeds occur consistently, turn this feature off since the computer is already performing this function.

Parity
When enabled, parity checks for correct data transmission. If a transmission error occurs, the VT100 detects it and indicates its presence by placing a checkerboard character (▒) on the screen in place of the character with the error. The parity sense feature determines if the parity is even or odd. When parity is disabled, no parity bit is transmitted or received.

Parity Sense
The parity sense feature defines which of the two methods of parity checking, odd or even, is being used by the VT100. If the parity feature is on, the terminal's parity sense must be matched to the parity the computer is sending. If the parity sense features do not match, most characters sent to the computer are rejected even though the character was received correctly by the VT100. If a parity incompatibility occurs, the checkerboard character appears on the screen in place of the received character.

NOTE

If the parity feature is turned off, the parity sense selection is disregarded.

Power
During initial installation, the terminal display must be set to the power line frequency. In the U.S. this is 60 hertz.

Receive Speed
Receive speed must be set to match computer transmit speed. The VT100 is capable of receiving at any one of the following preselected speeds: 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 9600, and 19,200 baud.

Receive speed is independent of transmit speed; the terminal may receive data at one speed and transmit data at a different speed.

Screen Background
This feature allows the operator to select the background of the screen display. In the normal screen mode, the display contains light characters on a dark background; in reverse screen mode, the display contains dark characters on a light background.

Screen Brightness
Unlike most video terminals, the VT100 does not contain switches or knobs to adjust screen brightness. Instead, the VT100 electronically controls screen brightness. This feature eliminates the high failure rate of mechanical controls and still allows the operator to select the desired level of brightness for maximum comfort under varied lighting conditions. This setting may be saved like any other feature in the terminal.

Scroll
Scrolling is the upward or downward movement of existing lines on the screen to make room for new lines at the bottom or top of the screen. It can be performed in two ways: jump scroll or smooth scroll. In jump scroll mode, new lines appear on the screen as fast as the computer sends them to the terminal. At the higher baud rates, the data is very difficult to read due to the rapid upward movement of the lines. In smooth scroll mode, a limit is placed on the speed at which new lines of data may be sent to the terminal. Upward movement of lines occurs at a smooth steady rate allowing data to be read as it appears on the screen.

NOTE

Smooth scroll mode allows a maximum of six lines of data per second to be added to the screen. The auto XON/XOFF feature must be enabled and supported by the host computer to ensure that data is not lost when smooth scroll mode is enabled.

Tabs
The VT100 can jump or tab to preselected points on a line just like a typewriter. The tab stops may be individually changed or totally cleared and then reset.

Transmit Speed
Transmit speed must be set to match the computer receive speed. The VT100 can transmit at any one of the following preselected transmit speeds: 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 9600, and 19,200 baud.

Transmit speed is independent of receive speed; the terminal may transmit data at one speed and receive data at a different speed.

Wraparound
When this feature is enabled, the 81st or 133rd character (depending on line size selected) inserted on a line is automatically placed in the first character position of the next line. If the wraparound feature is not enabled, the 81st or 133rd character and all following characters are overwritten into the last character position of the current line.

(shifted)

The VT100 contains character sets for the U.S. and the United Kingdom. The difference between the two sets is one character, the # or ↑ symbol. When the standard U.S. character set is selected, the uppercase **3** key on the main keyboard displays the # character. The ↑ character is displayed when the U.K. character set is selected.

PART 4 SELF-TESTING THE VT100

A self-test mode in the VT100 automatically, or on command, tests the condition of the terminal if a fault is suspected. The self-test program checks the following items.

Internal memory
Advanced video memory (if option is installed)
Nonvolatile memory (NVR)
Keyboard

This test is performed automatically whenever the terminal is turned on.

Self-Test Error Codes
There are two broad categories of errors: fatal and nonfatal. Fatal errors cause the terminal to immediately stop all operations. No intelligible information is displayed on the screen, but the screen most likely contains a random pattern of characters. The only error indication (in addition to random characters) is a possible error code displayed on programmable keyboard LEDs L1–L4. However, no terminal function, including the lighting of LEDs, is guaranteed if a fatal error is found. See Table 2-3.

Nonfatal errors do not halt the terminal processor. Instead, the terminal is forced to LOCAL mode and an error code character is displayed in the upper-left corner of the screen. There are five types of nonfatal errors:

1. Advanced Video Option data RAM (AVO)
2. Nonvolatile data RAM checksum error (NVR)
3. Keyboard missing or malfunction (KBD)
4. Data loopback error (Data)
5. EIA modem control lines loopback error (EIA).

NOTE
Loopback tests are not performed on power-up; they must be invoked separately with the proper escape sequence. See Appendix A for further information on this test.

Table 2-4 shows the possible nonfatal error characters that may appear on the screen and the failure represented by each character.

If the terminal passes all these tests, a final check of its operation is possible in SET-UP mode. Examine the display and compare it with the printed examples. Double height, double width, bold, blinking, reverse, etc., are all represented in SET-UP mode.

Table 2-3 Fatal Displayed Error Codes

Keyboard LEDs L1	L2	L3	L4	Error	Replace FRU
OFF	OFF	OFF	ON	ROM 1	Terminal controller
OFF	OFF	ON	OFF	ROM 2	Terminal controller
OFF	OFF	ON	ON	ROM 3	Terminal controller
OFF	ON	OFF	OFF	ROM 4	Terminal controller
OFF	ON	OFF	ON	Main Data RAM	Terminal controller

Table 2-4 Nonfatal Displayed Error Codes

Char	Faulty Module AVO	NVR	KBD	Data	EIA
1	X				
2		X			
3	X	X			
4			X		
5	X		X		
6		X	X		
7	X	X	X		
8				X	
9	X			X	
:		X		X	
;	X	X		X	
<			X	X	
=	X		X	X	
>		X	X	X	
?	X	X	X	X	
@				X	
A	X				X
B		X			X
C	X	X			X
D			X		X
E	X		X		X
F		X	X		X
G	X	X	X		X
H				X	X
I	X			X	X
J		X		X	X
K	X	X		X	X
L			X	X	X
M	X		X	X	X
N		X	X	X	X
O	X	X	X	X	X

PART 5 WHAT TO DO IN THE EVENT OF A PROBLEM

If it appears that there is a problem in the terminal, you should initiate the self-test procedure. This test will help to determine if the problem lies in your terminal or in some other part of the computer system. If the terminal appears to be faulty, refer to Table 2-5. This table describes the items an operator can check prior to making a service call.

Table 2-5 Problem Checklist

Symptom	Possible Cause and Corrective Action
VT100 will not turn on when power switch is set to ON.	AC power cord not plugged into wall outlet; plug in cord.
	AC power cord not plugged into terminal; plug in cord.
	Power not coming from wall outlet; check outlet with known working electrical device (a lamp). If no power, call your electrician.
	AC line fuse blown. Turn terminal OFF and have the fuse replaced. (See Figure 1-2 for location.)
No keyboard response	Keyboard cable not plugged into monitor; plug in keyboard cable.
	KBD LOCKED indicator on; computer has turned keyboard off. If condition persists, check with the host computer software people for a possible operating error.
	Perform the self-test operation.
Garbled characters	Transmit and/or receive speeds, parity sense, or parity enable may be wrong; check settings.
	Perform the self-test operation.

CHAPTER 3
INSTALLATION AND INTERFACE INFORMATION

SITE CONSIDERATIONS

The design of the VT100 (Figure 3-1) normally poses few constraints on selecting a place in which to install the terminal. In most cases, any environment suitable to the operator is a satisfactory environment in which to operate the terminal. Extremes of temperature and humidity should be avoided. A summary of VT100 guaranteed operating conditions may be found in Chapter 1.

UNPACKING AND INSTALLATION

The VT100 shipping carton contains the following items:

VT100 monitor
VT100 detached keyboard
VT100 power cord
VT100 SET-UP label
VT100 User Guide.

To install the VT100 perform the following steps:

1. Remove the VT100 from the shipping carton and place it in the desired work area.

2. Place the keyboard in front of the terminal and plug the keyboard coiled cord into the keyboard receptacle at the rear of the terminal (Figure 3-2).

3. Verify that the power selector switch shows the correct wall outlet voltage (115 V is standard in the U.S.) and the power switch is off.

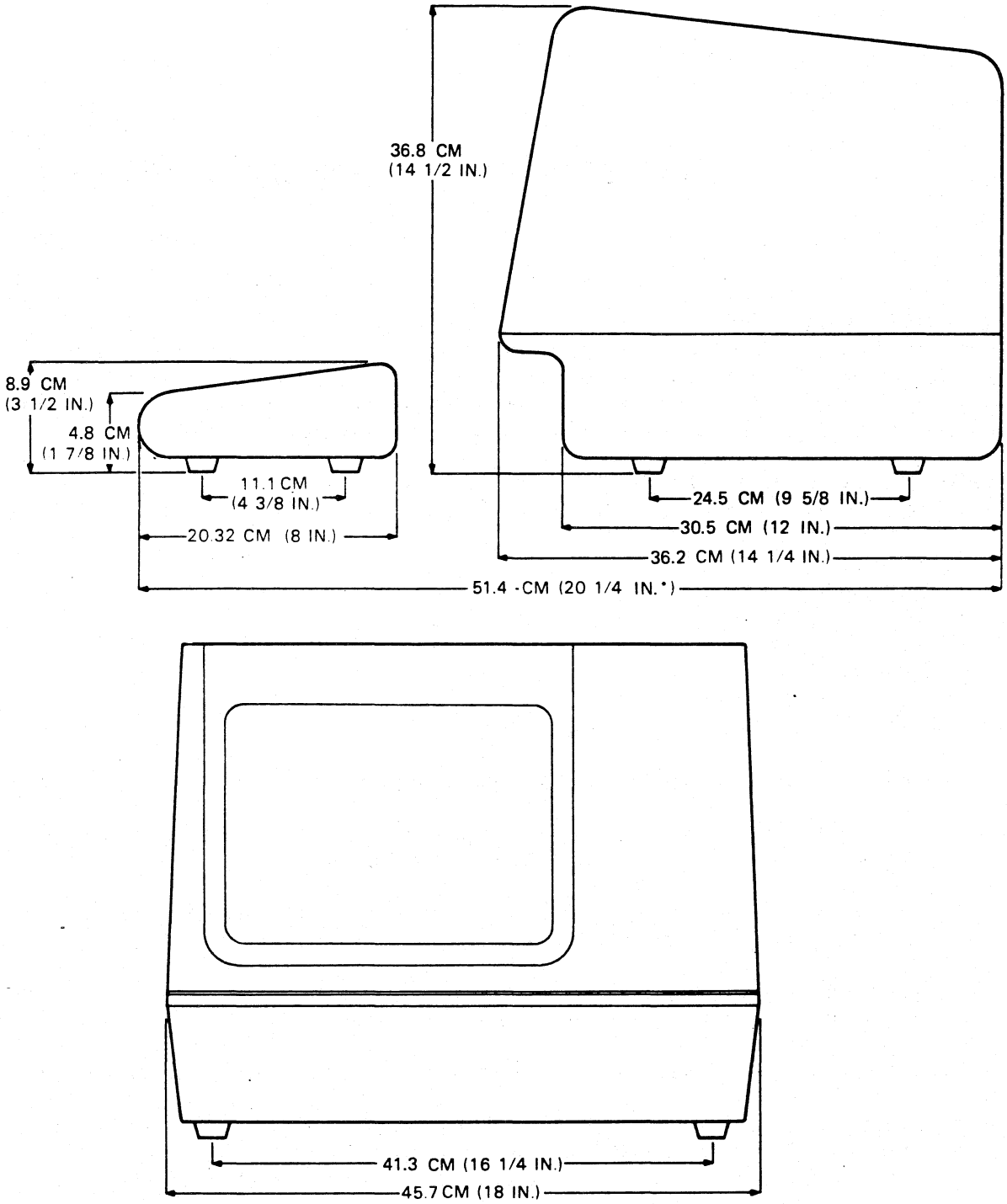
4. Connect the power cord to the power cord receptacle at the rear of the terminal and plug the other end of the power cord into a nearby wall outlet.

5. Connect the communications cable to the appropriate communications receptacle.

6. Turn the power switch on. The terminal automatically performs the power-up self test and either the ON LINE or LOCAL indicator on the keyboard will light. After approximately one minute the cursor will be visible in the upper-left corner of the screen.

7. Set the desired SET-UP features outlined in the operator section of this manual.

8. Once the installation procedure is complete, record the SET-UP features selected on the VT100 SET-UP label and attach the label to the underside of the keyboard.



*MEASUREMENT TAKEN WITH THE KEYBOARD PLACED FLUSH TO FRONT OF TERMINAL UNDER UNDERCUT.

MA-1991

Figure 3-1 VT100 Terminal Dimensions

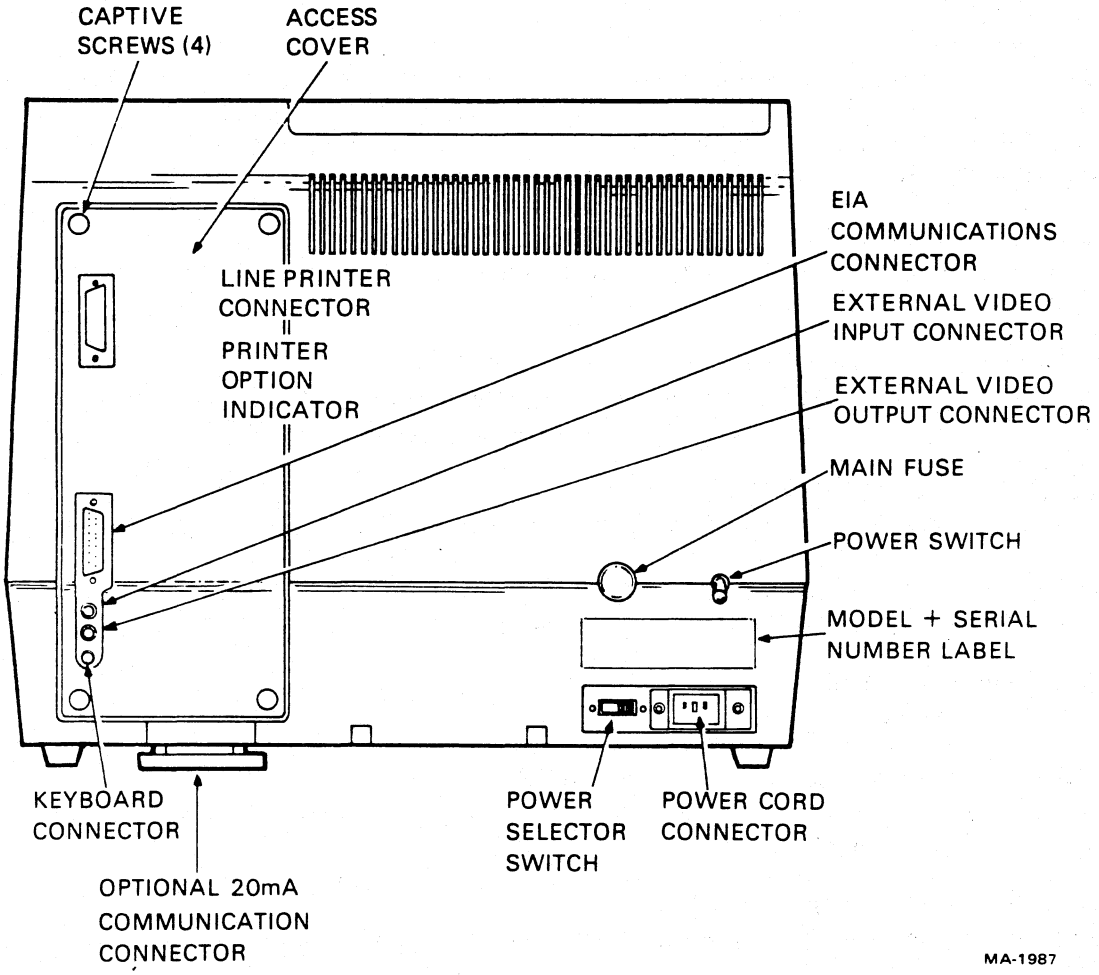


Figure 3-2 VT100 Rear View

USER MAINTENANCE

The keyboard keys are the only moving parts of the terminal and require no preventive maintenance by the owner. The VT100 surfaces may be cleaned with soap and water or any mild detergent. Cleaners with solvents should not be used.

The VT100 packaging is not meant to be weatherproof; there are several openings in the case through which liquids, coins, paper clips, and other objects can fall. Such objects would disturb the electronic operation of the terminal if they came into contact with the circuitry. For this reason, avoid putting drinks and metal objects on the top of the terminal, or using excessive water to clean the terminal. Rubbing the keys with a dry or barely moist cloth should clean them. Do not remove the keycaps to clean them more thoroughly; damage may result to the switch contacts if they are replaced incorrectly.

Keep the ventilation slots clear. Blocking these slots by placing objects on top of or under the VT100 may cause the terminal to overheat.

INTERFACE INFORMATION

EIA Interface

The basic VT100 operates on full duplex, asynchronous communication lines. The terminal interfaces to the line with a 25-pin connector mounted on the back of the terminal which meets the requirements of EIA specification RS-232-C. Table 3-1 summarizes the EIA connector signals. The following paragraphs explain each signal as used in the basic VT100.

Protective Ground - Pin 1
This conductor is electrically bonded to the VT100 chassis. Use of this conductor for reference potential purposes is not allowed.

Transmitted Data (from VT100) - Pin 2
The VT100 transmits serially encoded characters and break signals on this circuit, which is held in the mark state when neither characters nor break signals are being transmitted.

Received Data (to VT100) - Pin 3
The VT100 receives serially encoded characters generated by the user's equipment on this circuit.

Request to Send (from VT100) - Pin 4
Asserted at all times when terminal is powered up.

Carrier Detect (to VT100) - Pin 8
Ignored at all times.

Speed Select (from VT100) - Pins 11, 19, and 23
This signal is alternately called secondary request to send. The basic VT100 maintains this line in the asserted state at all times.

Speed Indicator (to VT100) - Pin 12
This signal is alternately called secondary carrier detect and is ignored at all times.

Transmission Clock (to VT100) - Pin 15
Ignored at all times.

Clear to Send (to VT100) - Pin 5
Ignored at all times.

Data Set Ready (to VT100) - Pin 6
Ignored at all times.

Signal Ground - Pin 7
This conductor establishes the common ground reference potential for all voltages on the interface. It is permanently connected to the VT100 chassis.

Receive Clock (to VT100) - Pin 17
Ignored at all times.

Data Terminal Ready (From VT100) - Pin 20
Data terminal ready is asserted at all times.

Ring Indicator (to VT100) - Pin 22
Ignored at all times.

Table 3-1 EIA Connector Signals

Pin No.	Description
1	Protective ground
2	Transmitted data
3	Received data
4	Request to send
5	Clear to send
6	Data set ready
7	Signal ground (common return)
8	Carrier detect
9	(Not used)
10	(Not used)
11	Same as pin 19
12	(Secondary carrier detect) speed indicator
13	(Not used)
14	(Not used)
15	Transmit clock
16	(Not used)
17	Receive clock
18	(Not used)
19	(Secondary request to send) speed select
20	Data terminal ready
21	(Not used)
22	Ring indicator
23	Same as pin 19
24	(Not used)
25	(Not used)

Electrical Characteristics

VT100 Output Voltages - On all signals designated "from VT100," the mark or unasserted state is -6.0 V to -12.0 V; the space or asserted state is +6.0 V to +12.0 V.

VT100 Input Voltages - On signals designated "to VT100," -25.0 V to +0.75 V or an open circuit is interpreted as a mark or unasserted state, and +25.0 V to +2.25 V is interpreted as a space or asserted state. Voltages greater in magnitude than 25 V are not allowed. These levels are compatible with EIA STD RS-232-C and CCITT Recommendation V.28.

Optional 20 mA Current Loop Interface

In most current loop applications, the VT100 is connected in a passive configuration - that is, current is supplied to the VT100. In this mode, the transmitter and receiver are both passive, both optically isolated, and the transmitter goes to the mark state when power is turned off.

Conversion from active to passive (or vice versa) requires moving a slide switch.

In active mode either the transmitter or the receiver or both may be connected so that the VT100 sources the 20 mA of current. In active mode isolation is not present and the transmitter goes to the space state when power to the VT100 is turned off.

Figure 3-3 shows the 20 mA current loop interface connector mounted to the access cover and lists the individual pin assignments.

The electrical characteristics of the 20 mA current loop interface are shown below.

Transmitter

	Min	Max
Open circuit voltage	5.0 V	50 V
Voltage drop marking	-	2.0 V
Spacing current	-	2.0 mA
Marking current	20 mA	50 mA

Receiver

	Min	Max
Voltage drop marking	-	2.5 V
Spacing current	-	3.0 mA
Marking current	15 mA	50 mA

In addition to the above specifications for passive operation, active mode places the transmitter or receiver in series with a source of 17 V ± 5 percent and 660 ohms.

External Video Connections

In addition to the EIA interface, the VT100 can easily interface to external video devices. The video devices may act either as a slave to the VT100 when connected to the composite video output or provide synchronized video to the VT100 video section when connected to the video input. The external video connectors are the two female BNC connectors located on the back of the terminal just below the EIA connector. The upper connector, J8, is the video input while the lower connector, J9, is the video output.

Composite Video Output (J9)

The composite video output provides RS170 output generated by combining the video signal with a composite sync signal. The output contains all video data appearing on the VT100 screen except that video which comes from J8. The output has the following nominal characteristics (Figure 3-4):

1. Output impedance = 75 ohms, dc-coupled
2. Sync level = 0 V
3. Black level = approximately 0.3 V when loaded with 75 ohms
4. White level = approximately 1.0 V with a 75 ohm load

The composite sync waveform conforms to EIA RS170 standards. The vertical interval is composed of six equalizing pulses, six vertical sync pulses, and six more equalizing pulses. The timing is as follows:

Equalizing pulse width	=	2.33 μs ± 50 ns
Vertical pulse width	=	27.28 μs ± 200 ns
Horizontal pulse width	=	4.71 μs ± 50 ns
Horizontal blank width	=	11.84 μs ± 50 ns/80 column mode
	=	12.34 μs ± 50 ns/132 column mode
Front porch	=	1.54 μs ± 50 ns.

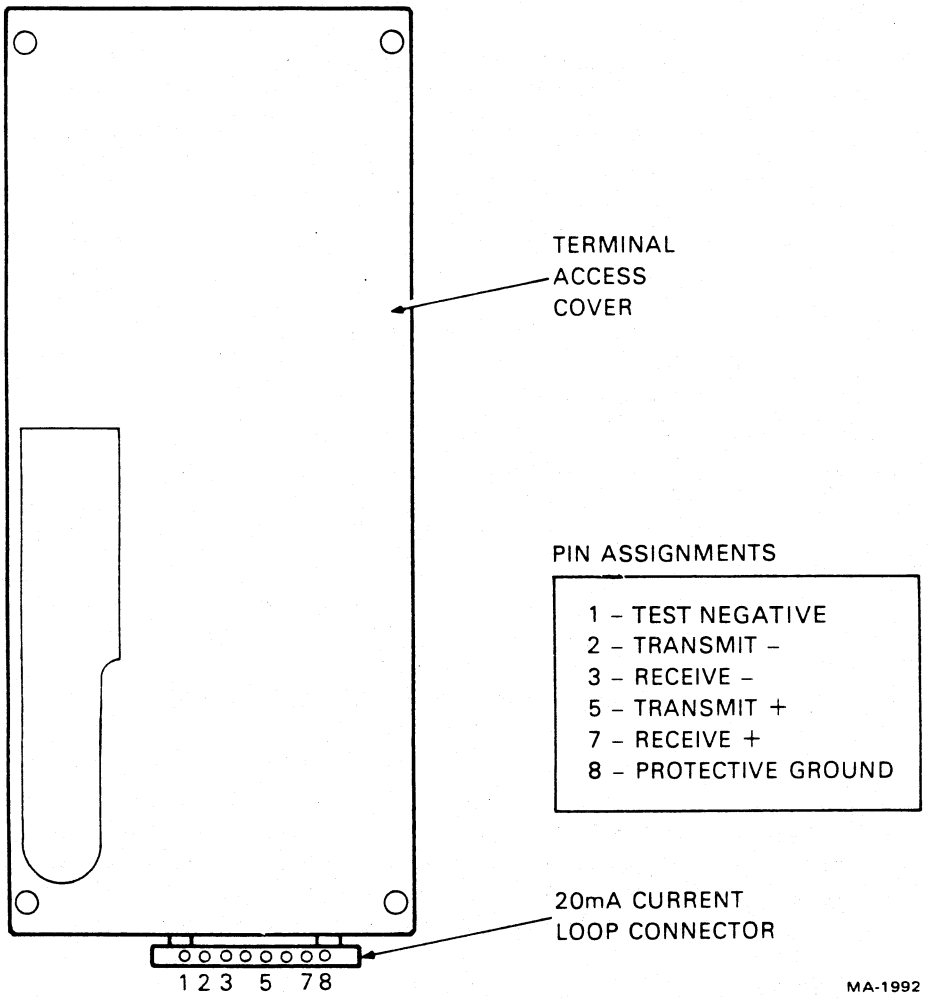


Figure 3-3 20 mA Current Loop Interface

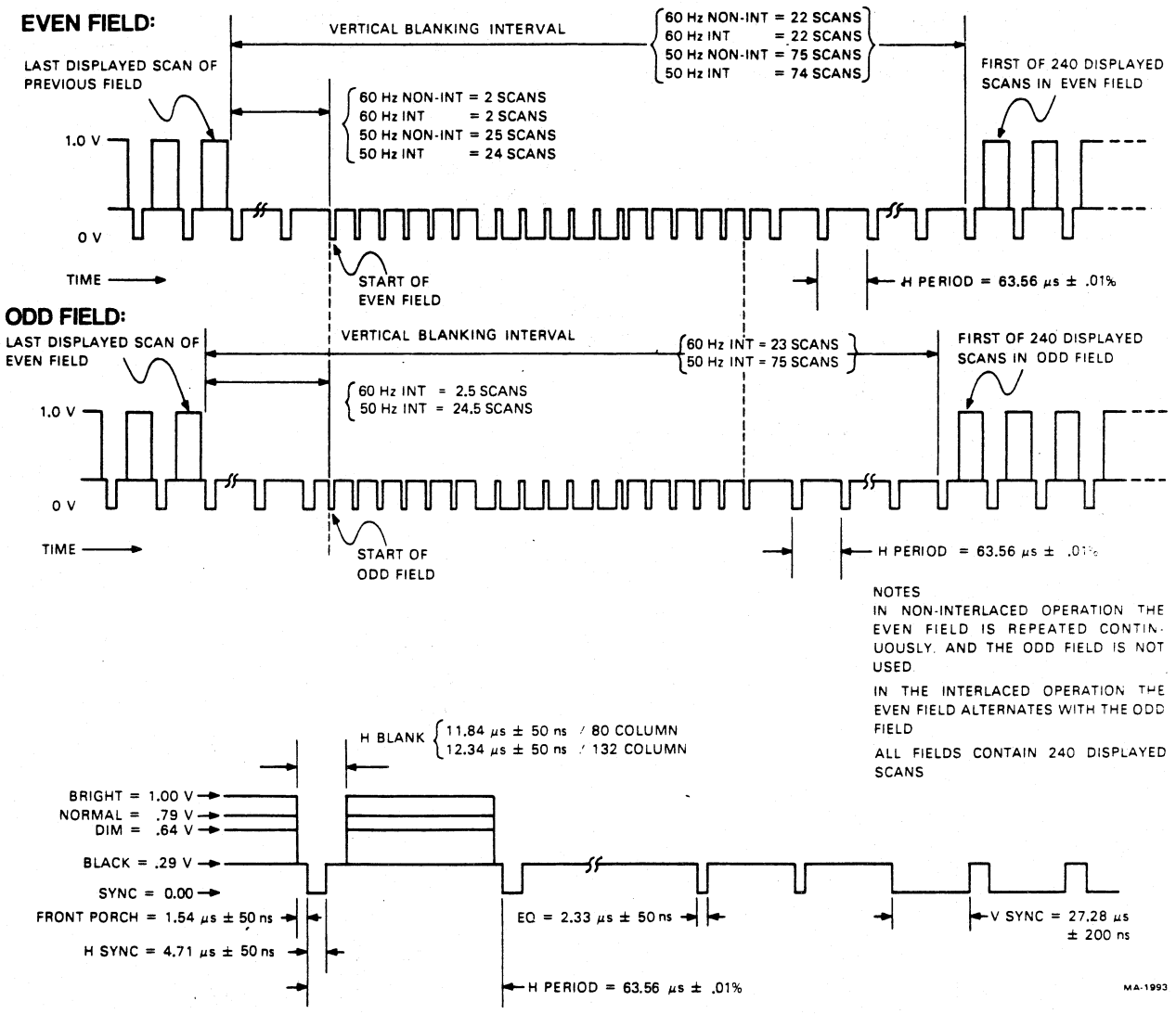


Figure 3-4 Composite Video Output

Video Input (J8)

An analog signal applied to the video input is "ORed" with the internal video signal such that the beam intensity at any point on the screen corresponds to the intensity of that signal which tends to make the beam brighter at that point. A video signal on this input affects only the internal screen and does not appear on the composite video output. This input has the following nominal characteristics:

1. Input impedance = 75 ohms, dc-coupled
2. Black level = 0 V
3. White level = 1.0 V
4. Maximum continuous input = ±2.0 V.

The external video source must be synchronized to the VT100; it may do this by referencing the composite sync on the composite video output. This means that the VT100 video input will not synchronize with any composite video source including the composite video output of another VT100.

CHAPTER 4
TECHNICAL DESCRIPTION

4.1 INTRODUCTION TO VT100 TECHNICAL DESCRIPTION

This section describes the contents of the technical description chapter and provides a technical overview of the terminal.

4.1.1 Scope of Chapter

This technical description is intended to provide an understanding of the terminal operating principles for Field Service, depot repair, and engineering personnel. The description considers the terminal to be several functional or replaceable subunits. Each subunit is described in its own section. Several subunits interact. Those interactions are discussed in the section about the subunit most involved in the particular process. For example, power-up involves the nonvolatile RAM but is described in the microprocessor section. Scrolling has its own section because it is a complex process that involves the microprocessor and video processor equally.

4.1.2 Order of Presentation

Each section describes the hardware first and the associated firmware operations second. This section contains a block diagram level discussion of the terminal hardware and firmware. More detail is provided in the functional block descriptions in later sections. Refer to the VT100 series Field Maintenance Print Set, No. MP00633, for circuit details while studying this manual.

4.1.3 Definition of Terms and Abbreviations

Many terms are written out the first time they appear, with an abbreviation or mnemonic in parentheses after it. The abbreviation is generally used after that. There is a glossary of abbreviations and signal names in the appendices of this manual. Numbers may be given in binary, octal, decimal, or hexadecimal (hex). The normal form will be decimal for scalar or ordinal values, and hex for data and addresses. Numbers are subscripted B for binary, Q for octal, H for hex, and no subscript for decimal.

4.1.4 Hardware Introduction

The VT100 is a complete computer input and output terminal that has a keyboard like a typewriter and displays its data on a video screen. It fits into two compact packages; the keyboard is flexibly attached to the main cabinet by a coiled cable. Refer to Figure 4-1-1.

The terminal consists of four basic components (not including enclosures) plus two important options. The components are the terminal controller, the keyboard, the CRT monitor, and the power supply. The options are the advanced video option and the current loop adapter option.

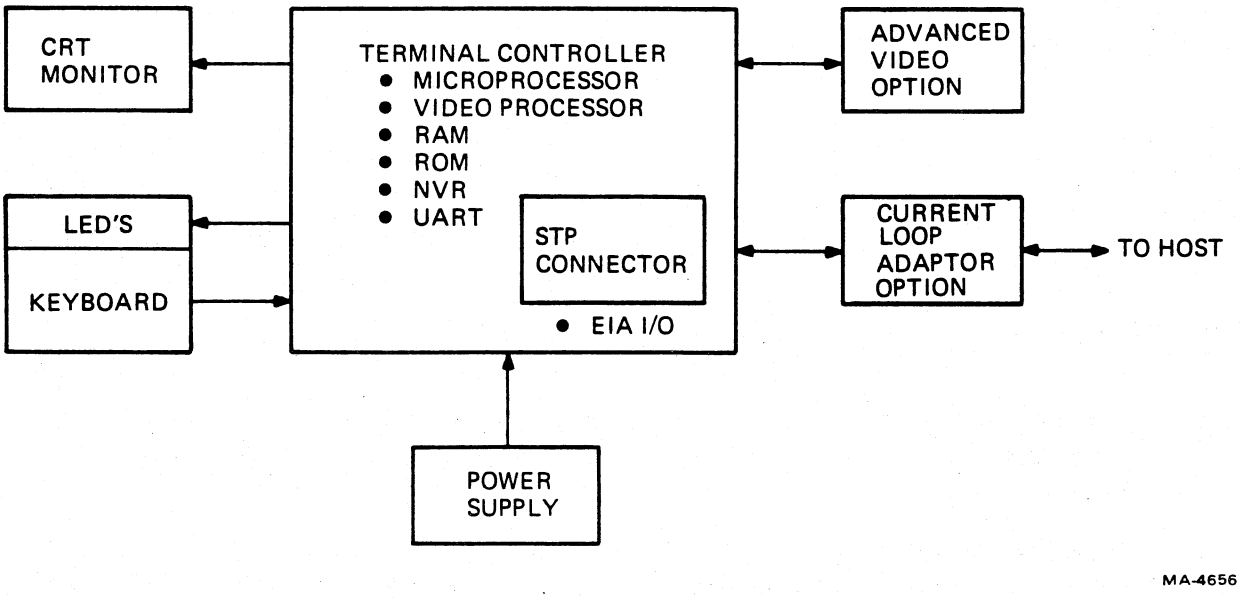


Figure 4-1-1 VT100 Components

The terminal controller is a single pc board module that manages all displays and all communication. Everything else connects to it. The terminal controlller contains these functional components:

- A microprocessor to manage terminal operations
- A video processor for converting data to recognizable patterns
- 3072 bytes of random access memory (RAM) for screen data storage and microprocessor scratch memory
- 8192 bytes of read only memory (ROM) containing the microprocessor's programming to operate the terminal with its particular features
- A nonvolatile RAM (NVR) to store the user-settable operating features without requiring hardware switches
- An asynchronous serial receiver-transmitter (UART) for data exchange with the computer
- EIA level converters to adapt the on-board input and output (I/O) signals to the communications interface
- A special connector, the standard terminal port (STP) that allows a plugged-in option to intercept terminal communications inside the terminal enclosure.

The keyboard is the typewriter-style input device for the operator. It has a loudspeaker for user feedback keyclicks and bells, and indicators that show internal states of the terminal.

The CRT monitor is a video screen that displays exchanges between the operator and the computer. It can display data in two modes: 80 characters by 24 lines, or 132 characters by 14 lines (or, with the AVO, 132 by 24). With the control circuitry on the terminal controller board, the CRT can perform many special character display functions.

The power supply converts the ac power line to the four dc voltages required by the terminal. It has a switching regulator for highest efficiency and coolest operation.

The advanced video option provides greater display capacity, plus it can carry extra firmware for the expanded functionality of other products in the VT100 series.

The current loop adapter option converts the EIA output of the terminal controller to a more noise immune standard when longer distances between the terminal and the computer are required.

4.1.5 Block Diagram Description

Figure 4-1-2 shows the VT100 terminal as a set of functional blocks. The rest of this section describes these blocks in greater detail.

4.1.5.1 Microprocessor – A microprocessor manages all terminal input and output operations. It also provides the intelligence that enables the VT100 to respond to and generate a wide range of ANSI control functions, and to emulate the characteristics of the VT52. Several of the microprocessor's program functions are effectively in series with data paths in the terminal. These functions have their own blocks in the functional block diagram to clarify the processes involved. These blocks are shaded to indicate that they are program functions or that the microprocessor controls data transfers between the blocks. The microprocessor is a computer with its instructions in program ROM (read only memory) and working memory in the scratch RAM (random access memory). Terminal parameters for start-up are stored in the nonvolatile RAM (NVR). The advanced video option (AVO) normally contains extra RAM as described below but can also contain extra program ROM.

4.1.5.2 Program ROM – The VT100 program ROM is an 8K × 8 memory containing instructions and data tables for the terminal's microprocessor. Memory comes in four 2K packages (later VT100s may have a single 8K package). Checksum data stored in each ROM allows the terminal to confirm the condition of its programming at self-test.

4.1.5.3 Scratch RAM – The scratch RAM is the portion of RAM on the terminal controller that is not used for the screen RAM. That is, the RAM is 3K bytes long, but only about 2.3K bytes are used for screen display. The rest of the RAM contains the microprocessor stack, SET-UP data, various flag bytes, the communication SILO, the keyboard buffer, and so on.

4.1.5.4 Nonvolatile RAM – The nonvolatile RAM (NVR) does not lose its data when its power is off. It stores all user-settable features and parameters and the answerback message so that they are available each time the terminal is turned on. Even the screen intensity can be stored. There are no mechanical switches needed for configuration.

4.1.5.5 Advanced Video Option – The advanced video option (AVO) contains the 1K × 8 of extra screen RAM needed to expand the display from 14 lines of 132 characters to 24 lines, plus a 4K × 4 RAM to store an extended set of attributes for all characters. The AVO also contains an additional segment of video processor to manage the four extra bits of data. Sockets for ROMs and jumper- or switch-programmable decoders allow expansion or overlay of program memory.

The AVO is a replaceable subunit of the VT100.

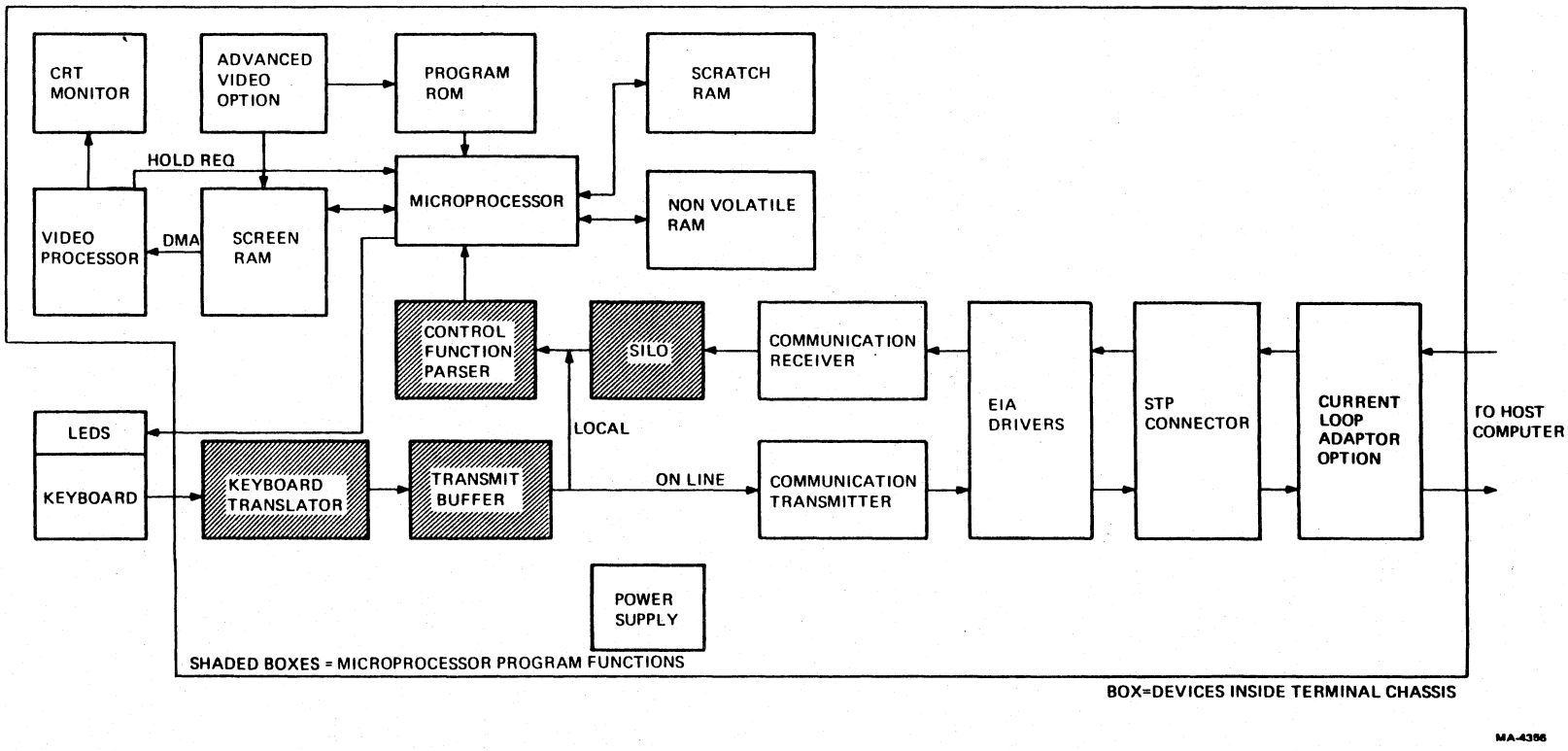


Figure 4-1-2 Functional Block Diagram

4.1.5.6 Keyboard – The keyboard is the user's input device to the terminal. The keyboard's output is a serial data signal that travels along the same wire as data coming from the terminal. The keyboard contains a bidirectional interface circuit, a set of keyswitches arranged like a typewriter, circuits to send the key information to the interface, LED indicators, and a small loudspeaker for keyclicks and bells. The connection to the terminal is a 3-wire coil cord carrying signals, power, and ground.

The keyboard is a replaceable subunit of the VT100.

4.1.5.7 LEDs – The terminal can inform the user of some internal conditions such as on-line or local and keyboard locked through the LEDs on the keyboard. The LEDs also may indicate the location of a failure during self test and are user programmable during normal operation.

4.1.5.8 Keyboard Translator – The output for each key is a number that represents the key's location (address) in the keyboard switch matrix. The microprocessor's keyboard translator translates the address to the industry-standard ASCII code.

4.1.5.9 Transmit Buffer – The ASCII codes wait in a transmit buffer until they can be transmitted. Some keys (such as the numeric keypad in application mode) produce control functions that are three bytes long. The transmit buffer is nine bytes long and thus can store at least three keys of any kind.

4.1.5.10 Communication Transmitter – The communication transmitter is one-half of a programmable universal synchronous/asynchronous receiver transmitter (PUSART) and its associated circuitry and firmware routines. The PUSART is programmed to place data in a standard asynchronous format by adding control and error detection bits to the original byte. The communication transmitter thus takes the parallel ASCII keycodes out of the keycode buffer, converts them to serial form, and delivers them to the EIA interface.

4.1.5.11 Communication Receiver – Data that the host sends to the terminal enters the communication receiver which is the other half of the PUSART. The PUSART accepts serial data from the interface and converts it to parallel form. The PUSART also checks for errors and records them in a status byte. The microprocessor reads the data and then the status byte to confirm the correctness of the data. If an error is detected, a checkerboard is displayed instead of a character to symbolize the error. If the microprocessor is busy managing the display, it devotes only enough time to the communication receiver to get the incoming code and check it for special codes requiring immediate action.

4.1.5.12 SILO – The rest of the incoming codes are stored in a part of RAM memory called a SILO. This memory maintains the order of the data as it arrives; the first data to arrive leaves first. This memory gives incoming data a place to wait when the microprocessor cannot transfer data from the communication receiver to the screen RAM as fast as it arrives. The SILO control routine checks the filling of the SILO and can issue XON and XOFF commands to the host to try to keep from overfilling. (XON and XOFF are explained in Section 4.3, Communication.)

In local mode, data from the keyboard bypasses the communication receiver and transmitter and the SILO.

4.1.5.13 Control Function Parser – When the microprocessor has enough time, it takes data from the SILO and puts it through a control function parser routine in the microprocessor. Each code is tested to see if it is in the control range (<20H or 7FH). If it is, the microprocessor acts on it immediately. Line feed, for example, causes a one line scroll. If the code is 1BH (escape), more codes are read from the SILO until the characters that define a control function are seen. Then the microprocessor executes the control function immediately or discards it if it is not a valid function. Noncontrol codes are ignored by the parser and are written into the screen RAM.

4.1.5.14 Screen RAM – The screen RAM is a memory that stores data for display on the screen (CRT monitor). The memory is organized according to the SET-UP line length specifications. Basic terminal memory can hold 24 lines of 80 characters or 14 lines of 132 characters. With the extra memory provided by the advanced video option, the screen size may increase to 24 lines of 132 characters and four additional bits are appended to each character location to allow expanded character attributes. (A character attribute modifies the display of that character relative to the preset values for the entire screen.)

Most of the time, the screen RAM is readable and writable by the microprocessor. For about 10 percent of the time, during the first scan of each 10 scan line of characters, the video processor silences the microprocessor and takes full control of the screen RAM, providing its own addresses to access the memory. This complete control of memory (by a device other than the microprocessor, which is normally in control) is called a direct memory access (DMA). The DMA allows fast access of data in memory because the microprocessor does not have to perform all the steps of addressing, reading, and writing to a destination. The video processor needs the fast access because the data rate required to display a line of characters on the CRT is greater than the microprocessor can handle.

4.1.5.15 Video Processor – The microprocessor puts displayable data in the screen RAM. The video processor direct memory accesses (DMAs) data a line at a time from the RAM. It converts the ASCII-encoded data into streams of pulses which, when converted to light on a CRT screen, appear to form characters on the screen. Custom ICs provide the complex timing and control signals required for this conversion. The video processor can be programmed by the user to perform the conversion at different rates (called refresh rates) to minimize flicker at different power line frequencies. A number of other aspects of video processor operation can be programmed as well.

4.1.5.16 CRT Monitor – The cathode ray tube (CRT) monitor is a simplified monochrome television set. It converts electrical pulse streams into dots of light by exciting a phosphor on the face of the tube with a moving electron beam. A video input from the video processor enters a cathode drive circuit that regulates the strength of the electron beam. The cathode driver is a linear amplifier that allows the CRT to display different intensities (gray scale). The monitor uses timing pulses from the video processor to drive the horizontal and vertical electron beam deflection circuits. These circuits cause the beam to travel down the screen slowly while rapidly moving sideways to draw horizontal traces called scans. This beam movement produces a pattern which is called a raster and the display system is called raster scanning. Because the beam repeatedly passes by each location on the screen, the video processor, by synchronizing its output with the motion of the beam, can make rows of dots of light align to form characters.

The screen does not hold its image after the electron beam has painted dots on it. For the eye to perceive it as continuously illuminated (i.e., without flickering) the screen must be repainted (refreshed) repeatedly some 30 or more times per second. Also, stray magnetic fields and electrical noise at the power line frequency can cause distortions in the display. If the refresh frequency is different from the power line frequency, the distortions appear to move up or down the display. This is very noticeable. Most distortions disappear by matching the refresh rate to the power line frequency. The VT100 can refresh at either of the two world power frequencies, 50 or 60 Hz, satisfying both flicker and distortion requirements. (VT100 refresh is not locked to the power line but is close enough to conceal most distortions.)

The CRT monitor, the monitor circuit board, and the flyback transformer are replaceable subunits of the VT100.

4.1.5.17 Power Supply – The VT100 power supply provides enough power to run the terminal and a few options. It is a switching supply to allow highest efficiency and to minimize the heat load on the rest of the terminal. It rectifies line voltage directly (without a transformer), and chops the resulting high dc voltage with a transistor at about 30 kilohertz. This ultrasonic ac is stepped down in a relatively tiny transformer and then regulated at low voltage to give the various outputs.

The power supply is a replaceable subunit of the VT100.

4.1.5.18 Standard Terminal Port – The standard terminal port (STP) is a shorting connector in series with the communication port, the modem control lines, and some power and timing lines. By connecting to the terminal through this port, options can exchange signals with the terminal controller or intercept terminal-host communications from inside the terminal cabinet.

4.1.5.19 EIA Interface – The Electronic Industries Association (EIA) interface used on the VT100 is the RS-232-C unbalanced bipolar voltage standard. The terminal controller has two types of ICs that provide conversion between EIA levels and the TTL levels used on the controller board. One IC is a line driver that outputs EIA levels for TTL inputs, and the other senses the EIA levels on the input line and converts them to TTL.

4.1.5.20 Current Loop Interface Adapter – The current loop adapter option plugs into the terminal controller board and mates with the EIA voltage interfaces to convert the terminal to 20 milliampere current loop interfaces. The current loop interfaces can be individually selected to be active or passive.

The 20 mA adapter is a replaceable subunit of the VT100.

4.1.6 Firmware Introduction

Figure 4-1-3 portrays the VT100 as a system with four levels of operation.

At the deepest level, the background routines continually repeat to manage functions that do not require precisely timed responses. The keyboard processor commands the keyboard to perform address scans, controls the bell and LEDs, and manages the conversion of key information from hardware-dependent codes to ASCII. The transmitter routine manages the transmission of ASCII data to the host. The received character processor examines incoming data, manages the SILO, initiates special functions as specified in the data, and writes displayable data into the screen RAM. When the terminal is in local mode, a logical shortcut bypasses the communication process and allows the keyboard data to enter the received character processor directly.

The background routines work on the internal buffers, registers, and flags which are logical devices located in hardware and RAM. These are physical locations in hardware that contain information placed there the hardware and by the firmware. The key buffers store up to three key addresses for the keyboard processor to pass through the transmit buffer to the transmitter routine for transmission to the host. The screen Ram, which stores the displayable data, is the largest segment of RAM. The scrolling flags contain data for the scrolling process in the video processor. The SILO stores data coming from the host in case the received character processor cannot transfer data to the screen RAM as fast as it arrives. The Send XOFF flag, set by the SILO manager, signals the transmitter routine to send the XOFF code to the host to halt transmission and prevent SILO overflow.

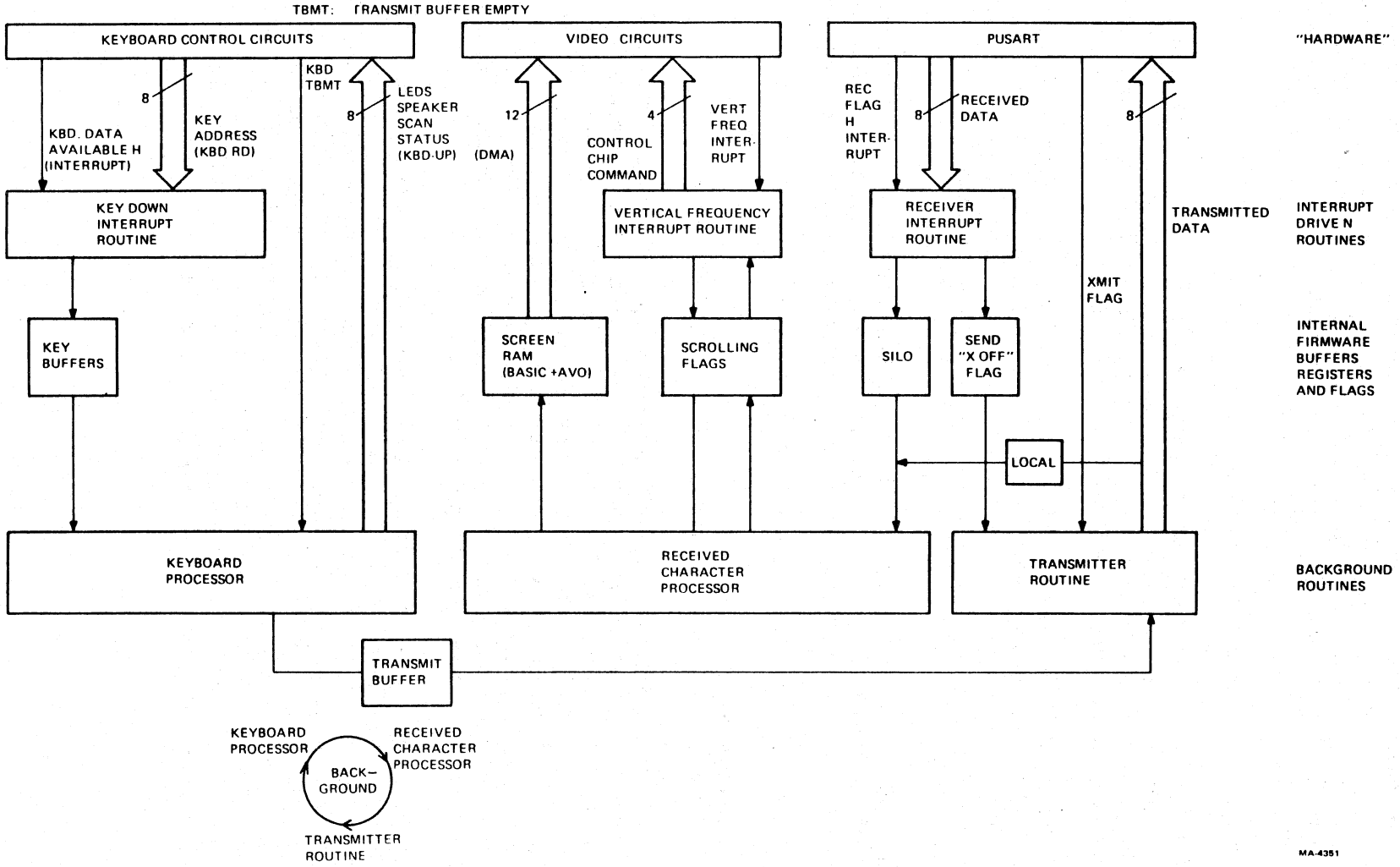


Figure 4-1-3 VT100 Firmware Block Diagram

Interrupt routines are segments of the firmware that take precedence over other business in the microprocessor because of the short-lived nature of the data that they handle. The Key Down interrupt routine is initiated by the appearance of data at the keyboard control circuits. It instructs the microprocessor to get the key address from the keyboard UART and put it in the key buffer. The Vertical Frequency interrupt routine occurs every 50th or 60th of a second and provides synchronization of video routines with the actual display timing. The Receiver interrupt routine moves incoming data from the communication transceiver to the SILO.

At the exterior level of the VT100 system, the hardware responds to the firmware by exchanging data between the user and the host computer in forms that are understandable to each.

4.2 MICROPROCESSOR

The VT100 has an 8080 microprocessor at the heart of its intelligence. The 8080 performs all the usual functions of a stored program computer, fetching instructions and data from ROM and RAM and responding to service requests from various devices in the system. Because of technical limitations in the implementation of the microprocessor hardware, some high speed counting and timing circuits and some power circuits are located in peripheral ICs made with a different semiconductor technology. These components are bipolar (8224, 8228) while the 8080 is NMOS.

4.2.1 8080 Microprocessor

The 8080 (Figure 4-2-1) contains a set of general and special purpose registers (the register array), timing and control logic which responds to machine code instructions, and an accumulator and arithmetic logic unit that perform the computations associated with the microprocessor operation.

The stack pointer is an important register that points to the bottom of the stack. The stack is a last-in/first-out area in RAM that stores information about the current process when a subroutine or interrupt branches away from the current instruction sequence. By storing this information at the beginning of an interruption and restoring it at the end of the interruption, the 8080 can continue the main program without any disturbance. This is the meaning of the interrupt process as it applies to the interrupt-driven routines mentioned in the firmware block diagram in Figure 4-1-3.

Most of the pins on the 8080 are tristate data and address lines. Four pins are power supplies and ground. The others, briefly, are:

HOLD – an input that lets another device get control of the buses when the 8080 finishes the current machine cycle. Hold Request from the video processor is the input signal.

HLDA – Hold Acknowledge output indicates that the buses will be given up for the Hold state.

INT – Interrupt Request input accepts INTR H signal that causes read of the interrupt vector address and branch to it.

READY – input for use with slow memory or I/O. If low, the 8080 enters the wait state (an indefinite portion of a machine cycle). It is not used in the VT100.

WAIT – output acknowledging the wait state. Not used by VT100.

INTE – Interrupt Enable output indicates whether interrupts have been enabled or disabled with the related instructions or by servicing an interrupt request. Not used by VT100.

0/1, 0/2 – Clock phases 1 and 2. Inputs to drive the 8080.

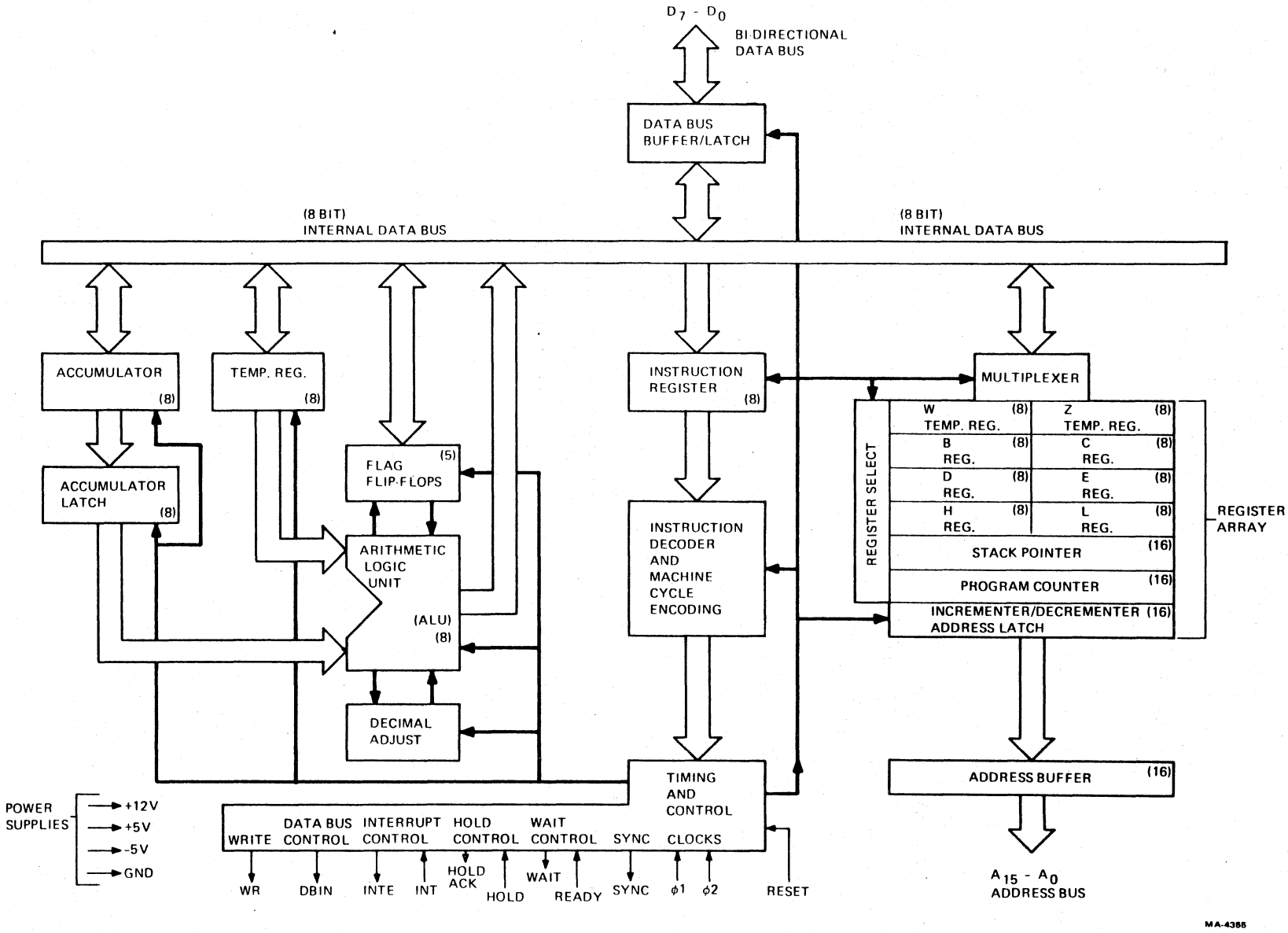


Figure 4-2-1 8080 Block Diagram

SYNC – output that indicates the beginning of each machine cycle. Combines with clock in the 8224 to produce Status Strobe (STSTB).

RESET – clears the program counter so that when it is released, program starts at location zero. Used to initiate power-up sequence and self-test.

WR – Write output controls memory and I/O writes by indicating the stable period of the data bus during a write instruction.

DBIN – Data Bus In output indicates that the data bus can accept data.

For more detail, see Intel's 8080A manual.

4.2.2 Data Bus and System Controller

The microprocessor data bus passes directly to the 8228 bus driver and system controller. This device provides TTL output buffering and level translation for the MOS 8080 bus. Because of the large number of devices on the data bus, the drive capability of some devices would be exceeded at times if all devices were on the same bus. (The keyboard UART is the weakest low-level current driver.) To distribute the load, the bus is split into those devices that communicate bidirectionally or are only read by the microprocessor, and those that are only written into. Read and writable devices are on the bidirectional data bus (DB). The write-only devices are driven by a one-way bus buffer and are on the data output (DO) bus. The terminal controller block diagram (Figure 4-2-2) shows which devices are on each bus.

The ROMs do not have sufficient high-level current capacity to drive all of the other inputs on the bus. Inactive devices have their outputs tristated but their inputs still draw enough current to accumulate a significant load over the entire bus. Pull-up resistors are connected to the bus to provide the additional current required. Their resistance is selected to supply enough current to meet high level needs on the bus without exceeding the low level sink capacity of any driving device.

Pull-up resistors are used on the output-only DO bus because the baud rate generator, a MOS device, has an input threshold higher than TTL driver E58 is guaranteed to deliver. Pull-up resistors ensure that the data lines rise enough.

An additional function of the 8228 is a combinational logic decode of the 8080 status byte. This byte, output by the 8080 at the beginning of each machine cycle, contains flag bits indicating the nature and function of the cycle. The byte is latched into the 8228 by the Status Strobe (STSTB) signal from the clock generator. In combination with three control output bits from the 8080, the system controller produces Interrupt Acknowledge (INTA) and Memory and Input/Output Read and Write (MEM WR,RD; I/O WR,RD). These signals reduce the external decoding requirements while saving pins on the 8080 package.

When the video processor asserts Hold Request during a direct memory access (DMA) of the screen RAM, the 8228 floats its outputs. Since these include the memory control signals, the video processor must provide its own memory control. The DMA Enable signal, buffered into the MEM RD line by gate E28 (pin 13), provides memory read enabling during the DMA. The other control signals are pulled high by the pull-up resistors.

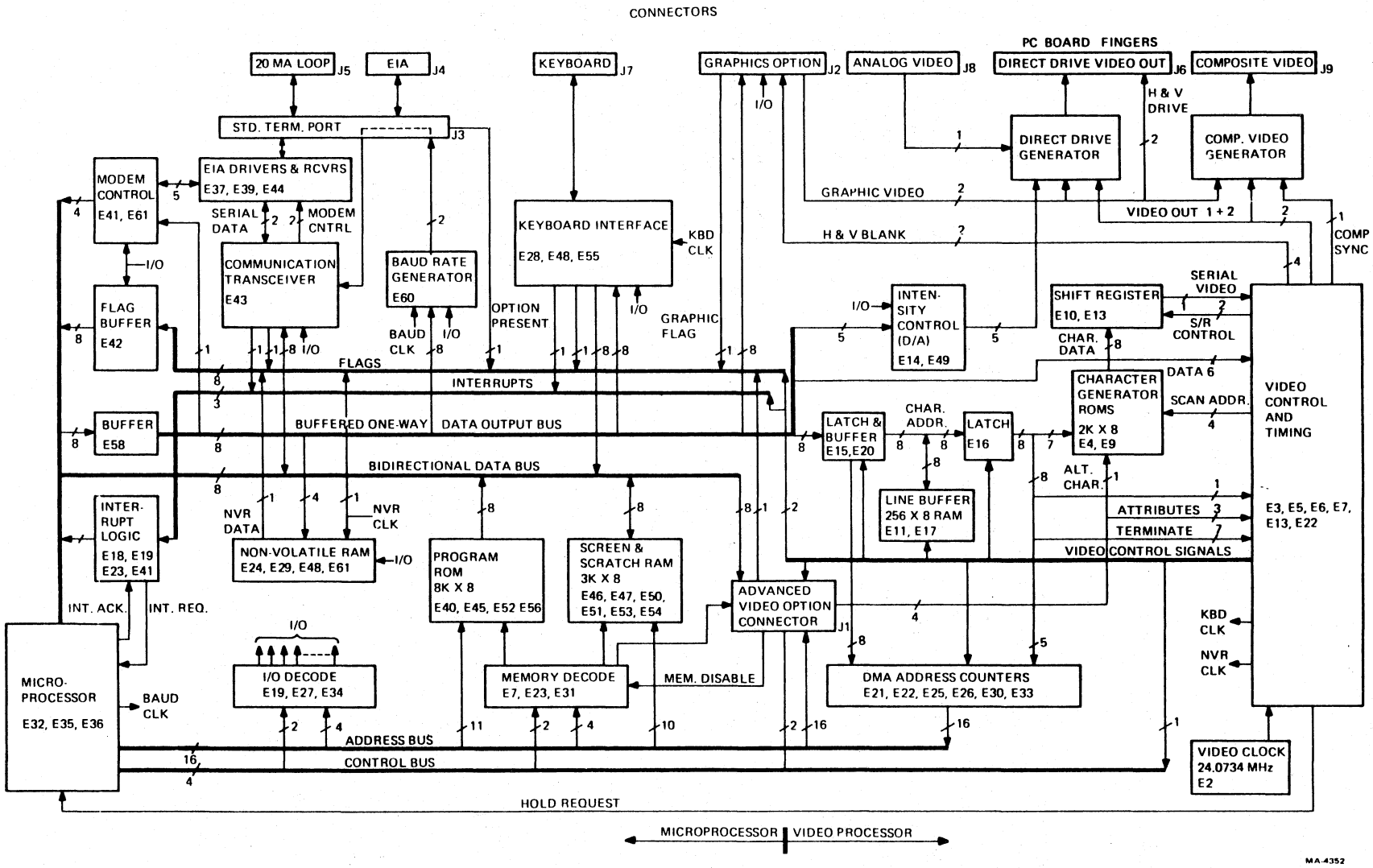


Figure 4-2-2 Microprocessor Block Diagram

4.2.3 Clock Generator

The 8224 provides the asymmetrical two-phase clock required by the 8080 logic. Its running frequency is crystal-controlled. An LC circuit on the tank input improves the crystal's mode stability. The capacitor in series with the crystal compensates for internal phase shifts in the 8224 at the high operating frequency. The 24.8832 MHz crystal frequency gets divided by 9 to produce a 361.69 ns clock period. The buffered TTL phase 2 output clocks the PUSART and the baud rate generator. 361.69 ns is the system clock period for the microprocessor.

The sync signal from the 8080 combines with an internal clock phase to produce the Status Strobe (STSTB) during the last ninth of the first state of each machine cycle. STSTB latches the status byte into the 8228 system controller.

The Ready input is not used in the VT100. It is an asynchronous input that gets synchronized to the machine cycles in the 8224. The synchronized signal can cause the microprocessor to enter a wait state during a memory access to wait for slow memory to respond. Memory used in the VT100 matches the processor speed so Ready is not used.

The Reset input is a Schmidt trigger. Its input is the +5 volt supply delayed by an RC circuit with a diode bypass for fast discharge. The Reset input is held low until well after all power supplies have settled. When the capacitor voltage reaches the Schmidt threshold, reset is released and the microprocessor begins operation at memory location 0 (the start of the firmware ROM). The inverted and noninverted reset signals clear other portions of the terminal controller.

4.2.4 Bus Timing

The bus timing diagram in Figure 4-2-3 illustrates the basic time relations between the address, data, and control lines in the microprocessor system. The figure distinguishes between write and read cycles, with the exception of the three top lines. These show the constants of the system: the two clock phases from which all timing is derived, and the address bus, that always provides the current address for either kind of cycle early in the cycle. Numbers on the diagram represent specified minimum/maximum nanoseconds between signals for normal operation.

Starting with the write cycle, note that the status strobe signal (STSTB L) shown in the read section occurs at the same point in the write cycle. Therefore, the status strobe latches the status byte into the 8228 during the first clock cycle. The 8228 delivers the decoded Memory Write L or I/O Write L (MEMW or IOW) signals in the third clock cycle when data to be written is stable. The 8080 Data Bus, DB Bus, and DO Bus graphs show the propagation delays between the three buses. The 8080 bus is the output pins on the chip. The DB bus is the output of the buffered 8228 bidirectional bus, and the DO bus is the unidirectional buffered output-only bus.

In the read cycle, the Memory Read L signal (along with I/O Read L and Interrupt Acknowledge L: MEMR, IOR, INTA) starts early to enable the chip selects and allow the data buses to stabilize. Data Bus In (DBIN) goes high before data settles but does not latch data into the 8080 until its falling edge, when data is settled. The two bus graphs show the assertion of stable data and also show the delay through the bidirectional bus buffer to the 8080 data bus.

4.2.5 Microprocessor Memory

The basic terminal controller contains 8192 bytes (8K) of program ROM and 3072 bytes (3K) of static RAM. (One byte = eight bits.) The original board utilizes four 2K × 8 ROM ICs; later versions may use a single 8K × 8 ROM. The RAM is six 1K × 4 ICs arranged in pairs. The microprocessor can address up to 64K memory locations. Some of these locations are reserved for future expansion. The memory map of Figure 4-2-4 shows the portions of addressable space that are reserved and also those areas that are available for new applications.

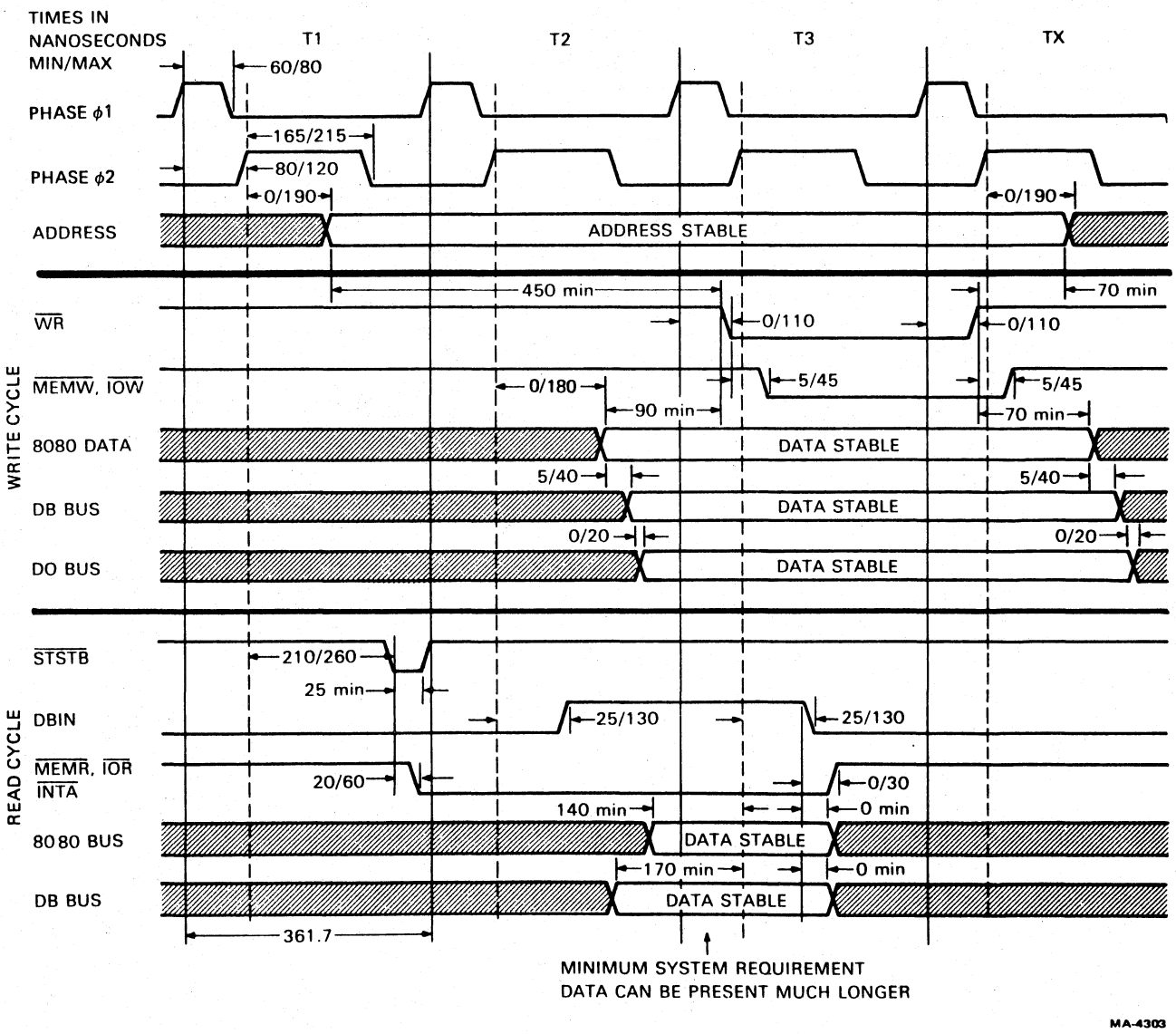


Figure 4-2-3 Microprocessor Bus Timing

KILO BYTES	ADDRESS (HEX)		DESCRIPTION	PHYSICAL LOCATION
0	0000 | 1FFF	8K X 8	BASIC ROM	BVB
8	2000 | 2BFF	3K X 8	SCREEN AND SCRATCH RAM	BVB
11	2C00 2FFF	1K X 8	AVO SCREEN RAM	AVO
12	3000 | 3FFF	4K X 4	ATTRIBUTE RAM	AVO
16	4000 | 7FFF	16K X 8	UNASSIGNED	
32	8000 | 9FFF	2K X 8 2K X 8 2K X 8 2K X 8	PROGRAM MEMORY EXPANSION (USE 2K X 8 ROM/EPROM)	AVO
40	A000 | BFFF	8K X 8	PROGRAM MEMORY EXPANSION (USE 8K X 8 ROM)	AVO
48	C000 | FFFF	16K X 8	UNASSIGNED	
64				

MA-4270

Figure 4-2-4 Memory Map

4.2.5.1 Memory Map – The basic terminal controller board contains 8K of program ROM and 3K of screen and scratch RAM. These account for the locations from 0000H to 2BFFH in memory. The advanced video option adds another 1 kilobyte of RAM (2C00H to 2FFFH) to increase the number of characters that can be displayed. The AVO also contains additional memory for character attributes. This memory is only 4 bits wide, but to address each location in correspondence with each of the 4K characters, it uses another 4K of addresses from 3000H to 3FFFH.

The next 16K locations (4000H to 7FFFH) are unassigned. However, 4000H to 4FFFH can be addressed by the video processor using the DMA address counters so 4000H to 4FFFH could be used for additional screen RAM with 5000H to 5FFFH as associated attribute storage.

Above 7FFFH is an 8K area intended for additions or changes to the program ROM in 2K segments and above that is an area intended for the same purpose but in one 8K segment. The top 16K are unassigned.

4.2.5.2 Memory Devices – Each ROM has three ANDed chip select inputs that are mask-programmed to be either active-high or active-low, eliminating the need for external inverters. The programming provides 1 of 4 decoding of the two address lines A11 and A12. The third chip select line is common to all four ROMs. In later VT100s jumpers W2 and W3 can be used to select either a high or low assertion for this single chip select to allow for 64K ROMs that do not have a programmable chip select. Table 4-2-1 shows the addressing of the ROMs.

4.2.5.3 ROM Decoding – The program ROM is enabled when the top half of memory decoder E31 is enabled and the correct address space is requested by the microprocessor. MEM RD or MEM WR from the 8228, in the absence of MEM DISABLE, enables the decoder. The ROM is in addresses 0H to 1FFFH, so A13 (the 8K bit) is not asserted during ROM reads. Bit A12 is low or high for 0–4K or 4–8K sections of ROM. The decoded outputs from both states are ORed to provide one of the select signals for the ROM. Then bits A11 and A12 at two of the chip select lines enable the outputs in one of the 2K segments. The low 11 bits address one of the 2K bytes in the enabled ROM. If the program is in one 8K ROM, A11 and A12 are used as regular address lines; only one chip select line enables its outputs.

4.2.5.4 RAM Decoding – If A13 is asserted, the memory space between 2000H and 3FFFH is being addressed. The ROM outputs are disabled and the decoded output from the top half of the decoder enables the bottom half. Now bits A10 and A11 are decoded to select 1K segments of the screen RAM. The 1K × 4 RAMs are paralleled in pairs to make each location 8 bits wide. There is 3K on the basic video board. The fourth 1K is located on the AVO; its addressing is decoded separately.

4.2.5.5 Memory Disable – Memory Disable turns off all memory on the terminal controller board. It is used by options that plug into the advanced video option connector:

1. To replace (overlay) existing memory,

2. To disable the terminal controller memory when using memory above 4000H (since the terminal controller does not decode A14, A15).

The advanced video option can contain overlaying program memory. This is a set of address locations that the AVO can be jumper-programmed to decode and provide data for. Since the main memory may also be decoding the same location, the AVO must assert MEM DISABLE to disable the main memory (ROM and RAM) so that only one data byte is asserted on the bus.

4.2.6 I/O Decoding

The I/O address space is divided into two regions: one, containing the 8251 PUSART, has address bit A01 always low; the other region contains all other I/O devices and has bit A01 always high. The list of I/O addresses in Table 4-2-2 illustrates this by the presence of hex 2 in the low half of each non-PUSART address byte.

4.2.6.1 PUSART Read and Write – When bit A01 is low, the PUSART is enabled. The I/O RD and WR signals from the 8228 control the read or write operation. Address bit A00 selects either the command or data register for the I/O operation.

4.2.6.2 I/O Read and Write – When bit A01 is high, the PUSART is disabled. Bit A01 high is one of two signals required to enable the I/O write decoder (E27). I/O WR is the other signal. Address bits A05, A06, and A07 select one of the seven writable I/O devices. These are the baud rate generator, the brightness control D/A latch, the NVR latch, the keyboard UART transmit buffer, the DC011 and DC012 video processor chips, and the graphics processor data port.

Table 4-2-1 ROM Chip Select Addressing

Address Line 11	Address Line 12	Chip Select 2	Chip Select 3	ROM Selected
0	0	Active Low	Active Low	1
1	0	Active High	Active Low	2
0	1	Active Low	Active High	3
1	1	Active High	Active High	4

Table 4-2-2 List of Hex I/O Addresses

READ OR WRITE	
00H	PUSART data bus
01H	PUSART command port
WRITE ONLY (Decoded with I/O WR L)	
02H	Baud rate generator
42H	Brightness D/A latch
62H	NVR latch
82H	Keyboard UART data input
A2H	Video processor DC012
C2H	Video processor DC011
E2H	Graphics port
READ ONLY (Decoded with I/O RD L)	
22H	Modem buffer
42H	Flags buffer
82H	Keyboard UART data output

Only three I/O devices are readable so their addresses were chosen to allow read decoding directly from the three address lines. When the 8228 asserts I/O RD, I/O WR deasserts and decoder E27 is disabled. I/O RD enables the gates in E34 to allow reading of the keyboard UART receive buffer, the flag buffer, or the modem control signal buffer, depending on which address bit is asserted.

4.2.7 Interrupt Vector

When any of the three interrupting devices (communication receiver, vertical frequency, or keyboard) sets Interrupt Request (INTR H) through gate E23, the current instruction is completed and then the microprocessor sets its Interrupt Acknowledge (INTA) status bit and performs an instruction fetch. The address requested in the fetch is the contents of the program counter. Its value is ignored in the interrupt process, but it is not incremented, as it would be in a normal fetch cycle. The INTA bit is decoded from the status word in the 8228 system controller; it enables the tristate interrupt vector buffer (E41) which then presents a restart (RST) instruction to the data bus. Main memory does not conflict with the vector buffer because the 8228, in decoding the interrupt status word, does not produce the memory read or write command bits needed for address decoding. (Refer to Table 4-2-3.)

Table 4-2-3 Interrupt Addresses

00H	Power-up (Not hardware driven)
08H	Keyboard
10H	Receiver
18H	Receiver and keyboard
20H	Vertical frequency
28H	Vertical frequency and keyboard
30H	Vertical frequency and receiver
38H	Vertical frequency, receiver and keyboard

The RST instruction disables further interrupts, pushes the current program counter contents (the location of the next instruction in the interrupted program) onto the stack and decrements the stack pointer. Then the program counter is loaded with the bits in the address field of the RST instruction. This field is produced by the interrupt signals of the interrupting devices. The signals are passed onto the data bus as bits in the address field (bits 3, 4, and 5). The rest of the instruction is hard-wired through diodes that supply high level to the other data bits during INTA and that are reverse-biased to isolate these data bus lines when the vector buffer is inactive.

The RST address field, when mapped into the same bit locations in the program counter, defines a set of eight 8-byte long memory spaces at the beginning of the memory. The first address, 0, is the starting point for the terminal controller program and is not used for interrupts. The program is normally started by a hardware reset signal that sets the program counter to 0. It can also be started by an escape sequence that the host can send to force the program to jump to zero, or in SET-UP mode the RESET key can be pressed. The other seven memory spaces, starting at 8, 16, etc., contain jumps to places in an interrupt handling routine that can mediate requests for service from any of the seven combinations of interrupting devices.

At the end of the interrupt service routine, the stack is popped, interrupts are enabled, and the interrupted program continues.

Early VT100s can disable the receiver interrupt by programming D4 in the NVR latch. However, this is never used by the VT100. Later VT100s instead, have the ability to add a Communications Transmit Buffer Empty interrupt by adding W6. The 8080 would then have to distinguish transmit and receive interrupts by testing the transmit flag on the flag buffer. This provision is not used on the VT100.

4.2.8 Power-Up and Self-Test

When power is first applied to the terminal controller board, the reset circuit in the 8224 holds the microprocessor in a halt state. Within a second, after the voltages stabilize in the power supply, the RC network at the reset input allows the input voltage to rise to the switching threshold of a Schmitt trigger. Then the reset is released with the 8080 program counter set to 0. The low 64 bytes of program are reserved for the eight interrupt service routines which can be addressed by the restart instruction (see previous section). The low 8 bytes start the power-up routine by disabling the interrupts, setting up the stack pointer, and then going immediately into the self-test routines.

Assuming there are no hard logic failures present on the board, the microprocessor attempts to perform a confidence check of the controller. Some failures are considered fatal and will stop the machine; other failures limit its operation but will not prevent its use. Fatal failures are indicated by the LEDs on the keyboard, while nonfatal errors are indicated as a single character on the screen.

The microprocessor first sends the number of the first ROM to the LEDs on the keyboard. Then it calculates a checksum of the contents of the first 2K of program. (Since firmware is treated as four 2K blocks of code, later VT100s with one 8K × 8 ROM chip operate the same way but any block failure requires replacement of the one chip.) At the time of ROM preparation, a special byte was included within each block to make the checksum equal zero if there are no errors. If there is an error, the microprocessor halts and the LEDs indicate the current ROM at the time of failure. Otherwise, the LEDs are incremented to show the next ROM number and the process continues.

The next part of the test is writing and reading the RAM. Every bit in the RAM is written with a 0 and a 1 and read each time. If the advanced video option is present (as indicated by the Option Present flag), its RAM is tested immediately after the main RAM. In the main RAM a failure halts the machine. Failure of a bit in the advanced video option RAM is indicated on the screen and the process continues. In another terminal, like the VT52, one bad bit in the screen RAM means there is one location that may not contain the right character. This can be annoying to the user but does not affect the rest of the screen. If one bit is bad in a VT100 line address, the entire screen below the affected line can become garbled and unusable. A bad bit in the scratch area could disable communication with the host. So this confidence check ensures that any RAM failure is detected immediately.

The next test checks the nonvolatile RAM by reading it. A checksum is calculated and compared with the value stored the last time the NVR was written during a save. A bad NVR does not stop the VT100 because the SET-UP values can always be reestablished from the keyboard at power-up. The NVR test is also the normal time when the terminal gets its auto SET-UP readings from the NVR. Time is saved because reading the NVR is the most time-consuming part of both the self-test and the auto SET-UP. If the NVR fails, the bell sounds several times to inform the operator, and then default settings stored in the ROM allow the terminal to work. The operator must then manually reset any parameters that differ from the default values.

To test the keyboard, the microprocessor commands the keyboard to scan once, lights all the LEDs, for about a half second, and sounds the bell. It waits for the scan to finish and then looks for the last key address 7FH at the keyboard UART. If the test fails, the terminal remains on-line, making it a receive-only (RO) terminal.

This is the end of testing.

Once the NVR data is in the scratch area in RAM, the microprocessor uses that data to program the hardware. All operating parameters that were last saved (see NVR) are recalled and the terminal is set to match them. Finally the cursor appears at column 1, line 1, and the microprocessor enters its background routine, ready for operation.

Refer to the Communication chapter for a discussion of Data and EIA tests, and to the Service chapter for a listing of the Self-Test Results tables.

4.3 COMMUNICATION TRANSCEIVER

The VT100 interfaces to its host system through a serial data port. An 8251 programmable universal synchronous or asynchronous receiver-transmitter (PUSART), illustrated in Figure 4-3-1, drives the port. This device translates between parallel and serial formats, adding or removing start and stop bits as required. The data exchanged are ASCII characters; parity may be enabled or disabled; the selectably odd or even parity bit will take the most significant bit position.

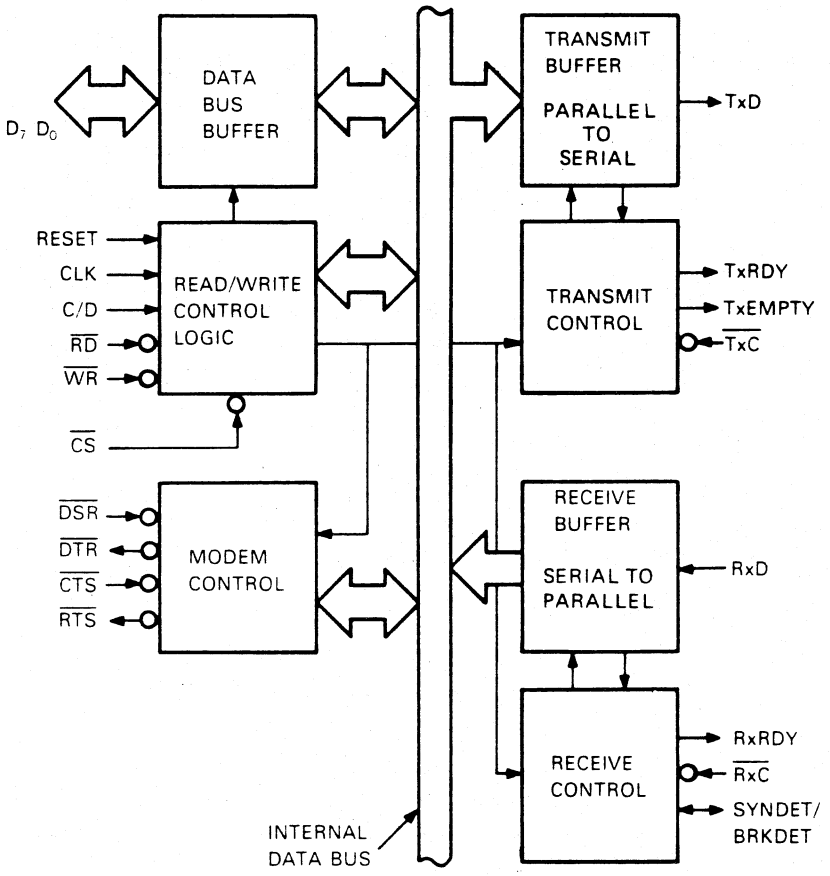
4.3.1 PUSART Principles

Most data in computer systems is exchanged as groups of bits. The bit is the smallest unit of information, but to be useful, most information must be encoded into groups of bits in standardized patterns. The VT100 operates with the standard patterns described by the American Standard Code for Information Interchange (ASCII). ASCII defines the use of 7 bits, specifying 128 different patterns that correspond to almost all of the letters, numerals, and punctuation marks used in English and several other languages. An eighth bit is reserved for an expanded standard.

The eight ASCII bits can be exchanged most rapidly over eight separate wires (in parallel), but this is very expensive to do anywhere outside the computer cabinet. Instead, the bits are rearranged to pass over a single wire one after the other. This is called serial transmission. The circuitry for converting parallel to serial and back again is complex but suited to large scale integration (LSI). The savings allowed by the use of serial lines has encouraged the development of very sophisticated but inexpensive conversion devices in LSI. At the same time, a variety of data exchange protocols has been developed. The result is an LSI device that can operate with virtually any protocol depending on the programming that it receives from its local processor. This is the PUSART. The VT100 uses one such device (Intel's 8251A) only in asynchronous mode, plus two simpler, wire-programmed asynchronous-only UARTS for the keyboard interface.

Synchronous and asynchronous describe the manner in which separate groups of bits (called bytes) are exchanged. In order for a receiver to know which bit is arriving at any given time, it must know the format of the byte and which bit of the byte is the first one. In synchronous mode, one or more special bytes are transmitted which the interface recognizes as synchronizing characters. Then all data bytes are transmitted together in rapid and precisely timed succession. Both the transmitter and receiver must have the same externally-supplied clock.

The VT100 only communicates asynchronously. Asynchronous transmission uses bits added to each data byte to provide synchronization between the transmitter and receiver. Because any two data exchanges can originate at random times with clock frequencies as much as 1 percent different, the protocol assumes random arrival of any byte of data, and relies on the synchronization information in the byte. This synchronization consists of extra bits appended to the beginning and end of the byte. One bit at each end (one start bit and one stop bit) is the most common configuration. The start bit and stop bit are defined to have specific states, and in particular, the start bit has a different state from the idling condition on the line. The interface looks for the transition from the idling state (called mark) to the start bit state (called space) and then clocks in the byte. The stop bit is the mark state, as is the idling line, so an immediately following byte has the correct mark to space transition to provide synchronization. The data bits, which occur between a start and a stop bit, are represented by a mark for a one and a space for a zero. Figure 4-3-2 shows the asynchronous data format.



PIN NAME	PIN FUNCTION
D_7 D_0	DATA BUS (8 BITS)
C/$\overline{D}$	CONTROL OR DATA IS TO BE WRITTEN OR READ
$\overline{RD}$	READ DATA COMMAND
$\overline{WR}$	WRITE DATA OR CONTROL COMMAND
$\overline{CS}$	CHIP SELECT
CLK	CLOCK PULSE (TTL)
RESET	RESET
$\overline{TxC}$	TRANSMITTER CLOCK
TxD	TRANSMITTER DATA
$\overline{RxC}$	RECEIVER CLOCK
RxD	RECEIVER DATA
RxRDY	RECEIVER READY (HAS CHARACTER FOR CPU)
TxRDY	TRANSMITTER READY (READY FOR CHAR. FROM CPU)
$\overline{DSR}$	DATA SET READY
$\overline{DTR}$	DATA TERMINAL READY
SYNDET/ BRKDET	SYNC DETECT/ BREAK DETECT
$\overline{RTS}$	REQUEST TO SEND DATA
$\overline{CTS}$	CLEAR TO SEND DATA
TxEMPTY	TRANSMITTER EMPTY

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Figure 4-3-1 8251A PUSART Block Diagram

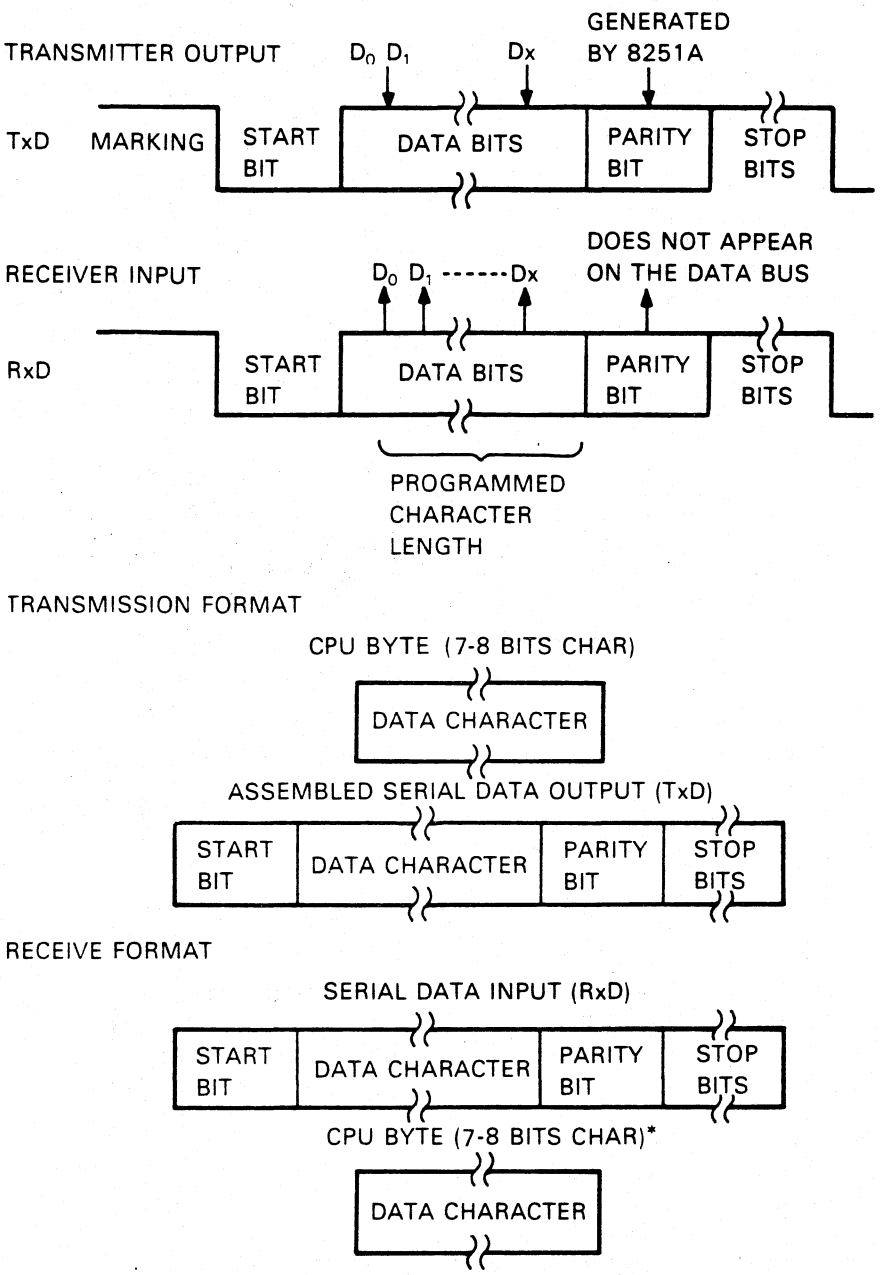


Figure 4-3-2 Asynchronous Data Format

4.3.2 PUSART Operation

The complete functional definition of the PUSART is programmed by the system's software. A set of control words must be sent out by the microprocessor to initialize the PUSART to support the desired communications format. Once programmed, the PUSART is ready to perform its communication functions. The Transmitter Ready (TxRDY) output is raised high to signal the microprocessor that the PUSART is ready to receive a data character from the microprocessor. TxRDY is reset automatically when the microprocessor writes a character into the PUSART.

Upon receiving an entire character from the serial input, the Receiver Ready (RxRDY) output is raised high to signal the microprocessor that the PUSART has a complete character ready to be read. RxRDY is reset automatically when the data is read. The PUSART cannot begin transmission until the Transmitter Enable (Tx Enable) bit is set in the command instruction and it has received a Clear To Send (CTS) input. The Transmit Data (TxD) output will be held in the marking state when the line is idle.

For a more detailed description of the PUSART's operation, refer to Intel's 8251A specification.

4.3.3 PUSART Addressing

I/O read, write and enable addressing and commands are discussed in the microprocessor I/O decoding section.

4.3.4 PUSART Programming

The microprocessor can program the PUSART to opeate with several standards and parameters. Many of these parameters are predetermined by the VT100 specifications. Character length, number of stop bits, parity enabling and format, baud rate multiplication factor, and asynchronous operation are all programmed in at power-up through the mode instruction (Figure 4-3-3) from the stored SET-UP information. Address bit A00 selects either the command register in the PUSART for writing the byte containing this information, or the transmit buffer for normal operation. A different programmable device, discussed later, provides the selected baud rate from SET-UP data.

After the PUSART mode of operation is selected by writing a mode instruction, PUSART operation is controlled by writing a command instruction (Figure 4-3-4). Once the mode instruction has been written into the PUSART, all further "control writes" (C/D=1) load a command instruction. A reset operation (internal or external) returns the PUSART to the mode instruction format.

The status of the PUSART can be read by the microprocessor by performing a read with C/D=1. Some of the bits in the status word (Figure 4-3-5) have the same meaning as output pins on the PUSART chip. The status word may be a maximum of 28 clock periods behind the event causing the update. This clock, from the microprocessor's phase 2 TTL signal, is the clock for the internal operation of the PUSART, which is a dynamic device requiring internal refresh at regular intervals.

4.3.5 Data Transmission

When the microprocessor wants to send a character out, it checks the XMIT flag at the flag buffer. If this flag is high the transmit buffer is empty and can accept data. If the flag is low, the microprocessor continues through its background program and returns to check again later.

When the flag is high, the microprocessor loads a data byte into the transmit buffer. The PUSART is double-buffered; this means that there is a second data buffer inside that is automatically loaded from the first buffer. The second buffer's contents get start and stop bits and parity (if enabled) appended and are shifted out by the continuously running clock. Immediately after the second buffer is loaded, the transmit flag goes high and the first (transmit) buffer can be loaded again.

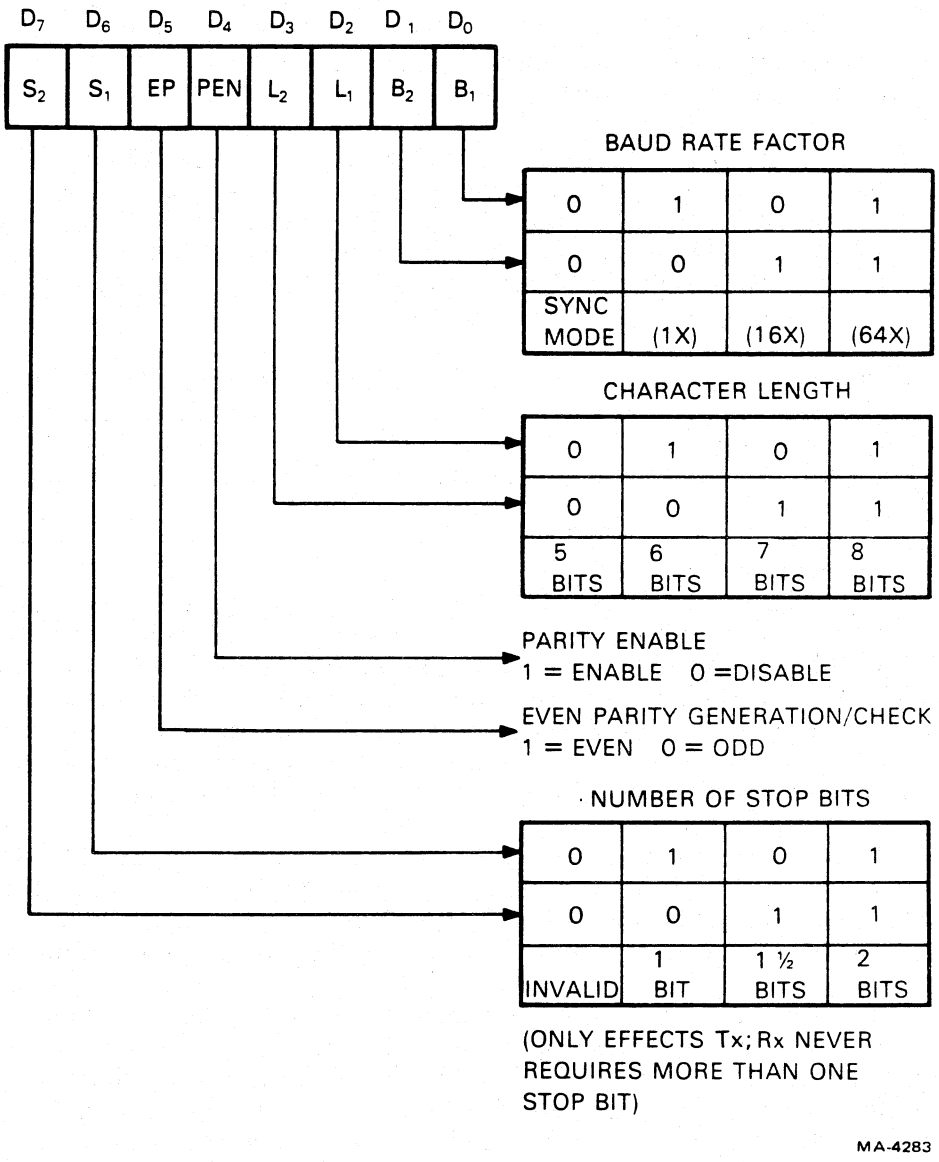
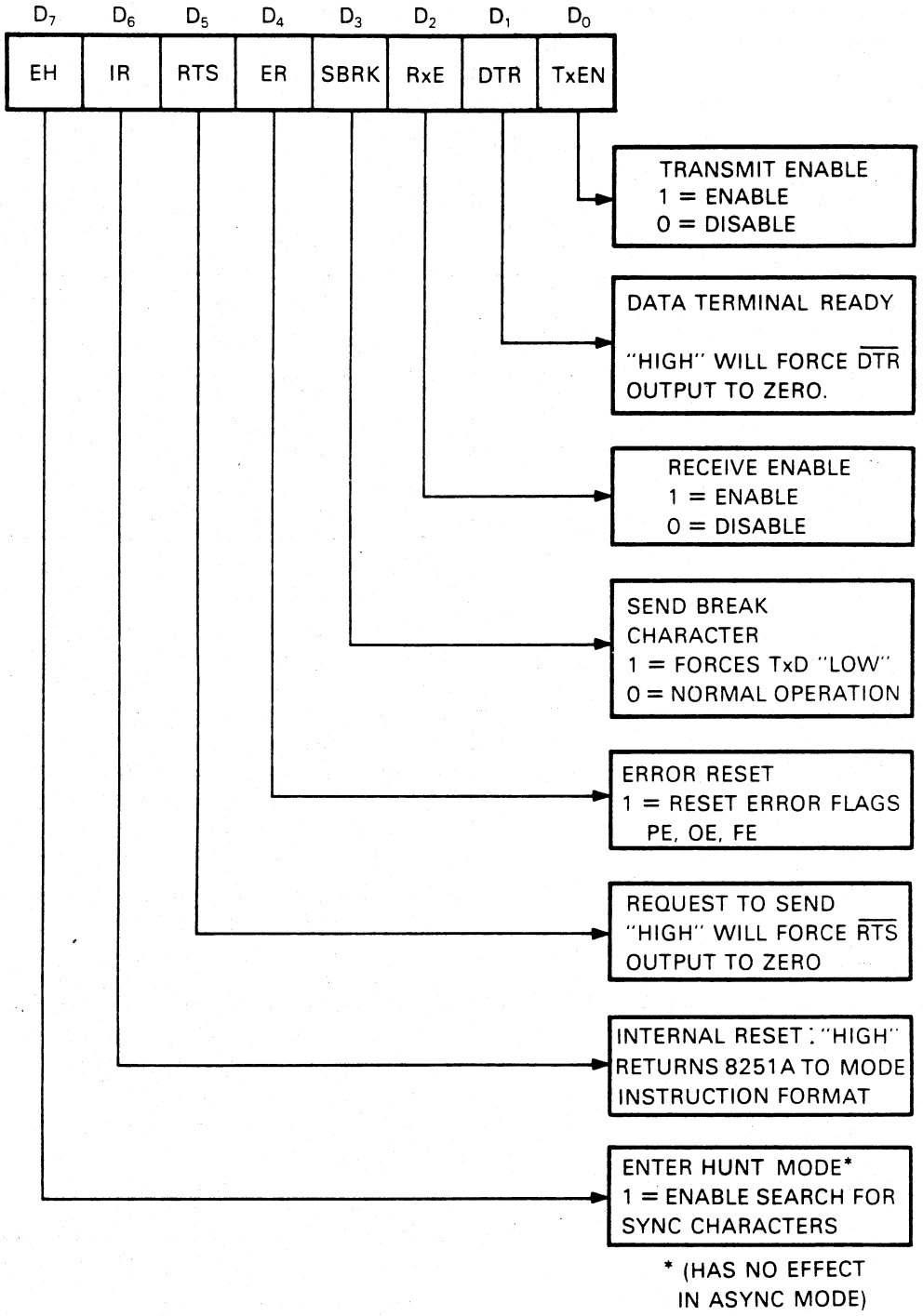


Figure 4-3-3 Mode Instruction



NOTE: ERROR RESET MUST BE PERFORMED WHENEVER RxENABLE AND ENTER HUNT ARE PROGRAMMED.

COMMAND INSTRUCTION FORMAT

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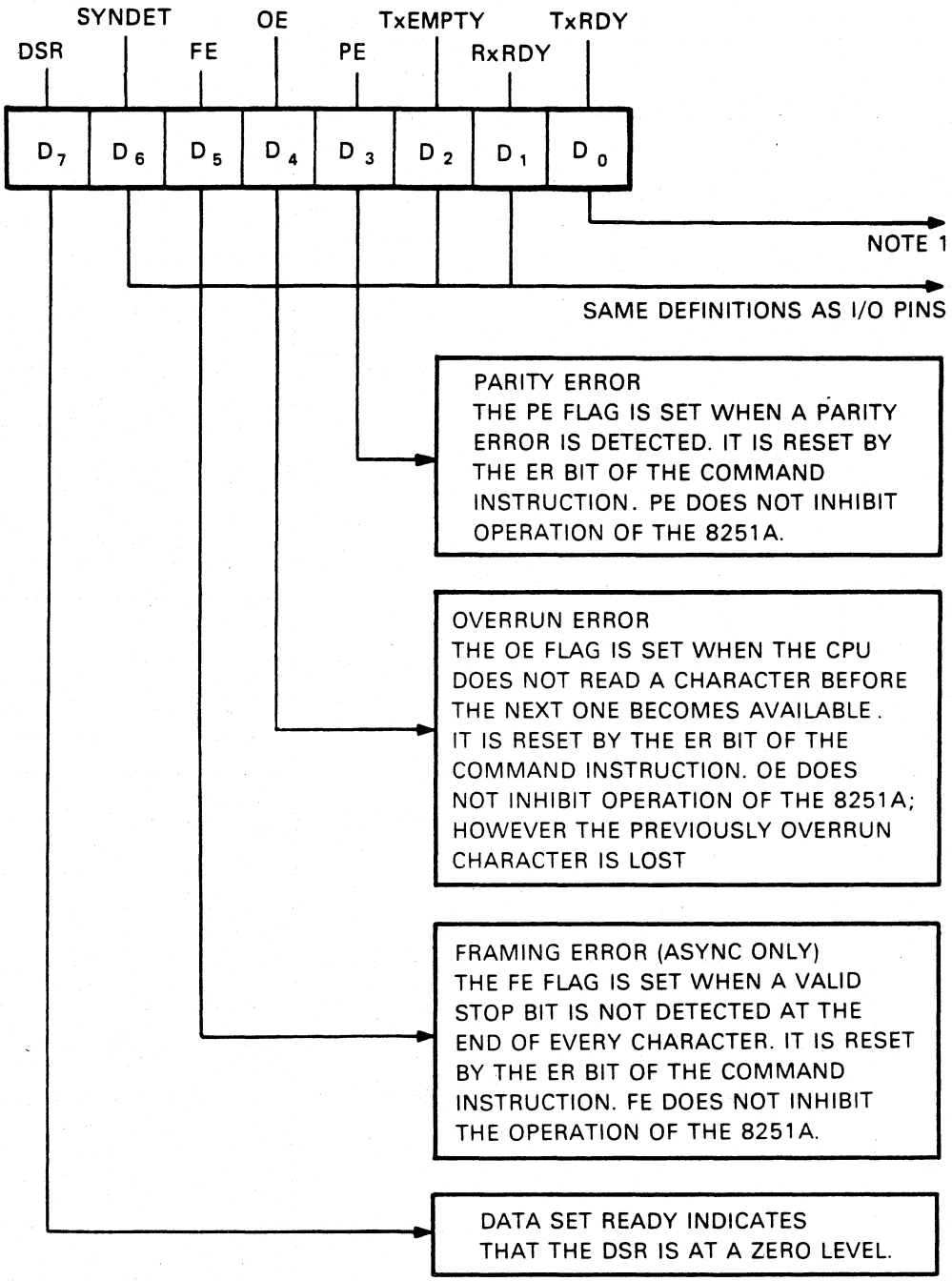
Figure 4-3-4 Command Instruction



STATUS BYTE FORMAT

NOTE 1: TxRDY STATUS BIT HAS DIFFERENT MEANINGS FROM THE TxRDY OUTPUT PIN. THE FORMER IS NOT CONDITIONED BY $\overline{CTS}$ AND TxEN; THE LATTER IS CONDITIONED BY BOTH $\overline{CTS}$ AND TxEN.

i.e. TxRDY STATUS BIT = DB BUFFER EMPTY

TxRDY PIN OUT = DB BUFFER EMPTY • (CTS-0) • (TxEN-1)

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Figure 4-3-5 Status Byte Format

4.3.6 Data Reception

Any data that appears on the receive data line is shifted into the internal receive shifting buffer. When a full character of bits has arrived, the start, stop, and parity bits are stripped. Parity is checked, and if bad, the parity error flag in the status word is set. Data is transferred to the receive data buffer, and the receive flag is set. This flag requests an interrupt from the microprocesor. The microprocessor then has the amount of time it takes the next character to shift in to read the first character. After reading the character, the microprocessor reads the status byte to check the integrity of the data. If the microprocessor does not read the receive data buffer in time, the second character writes over the first one which is lost. Then, an overrun error is reported in the status word. The checkerboard character appears for all errors.

4.3.7 Baud Rate Generator

PUSART clocks are derived from the microprocessor clock. The microprocessor clock crystal was selected to provide a frequency within the limits of the 8080 which could be readily divided to provide standard baud rates. The division occurs in programmable baud rate generator E60. This device contains two independent counters to allow different receive and transmit (split) baud rates. Each counter has 4 input lines to select 1 of 16 rates. Thus, a 1-byte load into the device can set up both send and receive rates. The baud rate generator's input register is written into as a device in the I/O address space.

E60 is factory mask-programmed with the division ratios required to get standard baud rates from the crystal frequency. The 4-bit input is an address for a ROM location containing the SET-UP information for each rate. Table 4-3-1 lists the baud rate generator divisors.

E60 was originally designed to operate with a crystal as a self-contained crystal controlled oscillator and divider. The oscillator is located elsewhere, so the oscillator inputs EXT1 and EXT2 receive the microprocessor clock driven out of phase by two inverters in E38.

Table 4-3-1 Baud Rate Generator Divisors

(Input frequency = 2.76480 MHz)

X16 Baud Rate	Divisor	Output	Freq (Hz) Error
50	3456	800	
75	2304	1200	
110	1571	1760 *	-0.006%
134.5	1285	2152 *	-0.019%
150	1152	2400	
200	864	3200	
300	576	4000	
600	288	9600	
1200	144	19200	
1800	96	28800	
2000	86	32000 *	+0.465%
2400	72	38400	
3600	48	57600	
4800	36	76800	
9600	18	153600	
19200	9	307200	

*Output frequency shown is nominal value. Include percentage error to get actual frequency.

4.3.8 Serial Interface

The serial transmit and receive interfaces are ICs that convert between TTL signals and EIA RS-232-C unbalanced bipolar signals. The electrical specifications and connector pinouts are described in Chapter 3, Installation.

4.3.9 Modem Control

Certain pins on the PUSART are labeled with standard modem control designations. These pins are readable [Data Set Ready (DSR)] or writable [Data Terminal Ready (DTR)] and [Request to Send (RTS)] as buffered bits in the PUSART's status and control bytes. Other signals from the modem pass through EIA level translators with Schmitt trigger inputs to a tristate buffer which, when enabled by the MODEM RD command, presents them to the data bus. Another signal [Speed Select (SPDS)] is written from the data bus into the NVR latch which is a convenient extra latch position. None of these signals are used to support modem control in the basic VT100. They are always programmed at power-up to allow normal full duplex operation with some modems when a standard EIA cable is installed between the modem and the VT100. See Chapter 3 for more interface information.

4.3.10 Data Types

Three kinds of data can be exchanged between the VT100 and the host: control characters, control functions, and displayable characters.

Control characters are any ASCII characters in the range 0 – 1FH. They include carriage return and line feed.

Control functions start with a control character (escape) and contain additional characters which extend the range of special actions that the terminal can perform. Cursor home is such an action. Some control functions can contain numeric parameters to modify the special actions. Direct cursor addressing is a typical example. Appendix A of this manual describes the programming and use of the control characters and functions in detail.

Displayable characters are those ASCII codes that are stored in the screen RAM, causing a character to be displayed on the screen.

4.3.11 SILO

The microprocessor checks each character as it comes in from the PUSART. Only four characters cause any special action at this time. Control codes XON and XOFF (see below) are immediately processed while NULL and DELETE are discarded. Everything else gets put in a 64 character (128 characters in later model terminals) first-in/first-out space in the scratch area of RAM called the SILO. The SILO processor routine maintains this area by updating two locations called SILIN and SILOUT. These point to the current entry and exit points in a loop of memory locations. The farther apart they are, the more characters are in the SILO. The addresses of the two points are subtracted from each other to determine the filling of the SILO. The subtraction is performed in modulo 64 (or 128) arithmetic to accommodate the rotation of the locations.

The SILO is necessary because when the microprocessor reads a character, it acts on that character completely before taking another one. For example, a line feed character causes the processing needed to accomplish a scroll. The processing time often exceeds the time between characters at the port. To save the characters that might arrive and get lost during a special action, the microprocessor responds to the received data interrupt by quickly moving the data to the SILO. Only the examination described above gets performed. After the current action is finished, the microprocessor gets the longest waiting character out of the SILO and range checks it. If it is less than 20H, it is a control character and the microprocessor processes it. If it is 20H or above, the microprocessor puts it in the next character position in the screen RAM.

4.3.12 XON/XOFF

XON and XOFF are two control codes that the terminal and host may send to each other to control the pace of data transmission. The host usually has a buffer space similar in function to the VT100's SILO. If either device has a large processing load at the same time that a lot of data is being received, the buffer or SILO can fill up. The receiving device monitors its buffer and sends Transmit Off (XOFF) when the buffer contains a predetermined number of characters. On the VT100 this value is 32 characters. (A second XOFF is sent at 112 characters in late model VT100s.) The sending device should stop transmitting until it receives Transmit On (XON). When the receiving device empties its buffer to another predetermined number of characters (16 characters on the VT100), it sends XON.

The **NO SCROLL** key on the keyboard enables and disables SILO fetching. If data continues to arrive, the SILO management routine sends XOFF or XON as required. The microprocessor keeps track of the current state and sends the opposite command the next time the key is pressed. **CTRL-S** and **CTRL-Q** send XOFF and XON directly. Coordination of various causes of XON and XOFF is discussed in Appendix A.

Because of the serial interface, several character times may elapse before the transmitter acts on XOFF and its last character passes through the receiver. This partly determines how full the buffer can be before XOFF must be sent. The other determinant is the worst case condition in split speed operation. If the terminal transmits at a low speed and receives at a high speed, the interface delay can allow several characters to arrive before XOFF stops their transmission. A detailed discussion of this problem is in Appendix A.

4.3.13 Control Function Parser

A parser is a routine that examines a sequence of characters. It then starts processes and extracts parameters based on the contents of the sequence. The term comes from the grammarian's practice of parsing (separating) a sentence into its component parts: subject, verb, object. The meanings of many sequences are being standardized throughout the data processing industry through American Standards Institute (ANSI) and International Organization of Standardization (ISO) committees. The VT100 employs a subset of several of these standards, plus it has several private sequences to allow it to perform certain DEC-specific functions like behaving as a VT52.

A character in the range below 20H is always the starting flag for the parsing process. Some functions have only the first character for their sequence; line feed (0AH) is an example. After the function is performed, the next character is taken from the SILO. If it is not in the control range, it is put on the screen. Escape (1BH) is the flag for a longer sequence. After escape, characters are taken from the SILO and range-checked as intermediate (20H to 2FH) or final (30H to 7EH) until a final character appears. The sequence is interpreted and the appropriate function performed. Then the next character is taken from the SILO and displayed if not in the control range. If a sequence is not supported by the VT100, it is parsed and then ignored.

Detailed descriptions of the functions are in the *VT100 User Guide* and in Appendix A of this manual.

4.3.14 Local

In local mode, keyboard output bypasses the communication transmitter and receiver and SILO and is acted on directly. The Data Terminal Ready signal (DTR) at the EIA interface is unasserted in local.

4.3.15 Standard Terminal Port

The standard terminal port (STP) is a printed circuit board edge connector on the basic video board that contains twenty pairs of contacts. When no board is plugged into the connector, the pairs of contacts meet. All EIA data and modem control signals plus the two baud clocks pass through this connector. Future options may utilize the signals present at this connector. For a complete discussion of the details of the STP, see the *STP Option Interface Guide*, Chapter 7.

4.3.16 Communication Self-Test

The VT100 can test its communication circuits, but because the operator must temporarily plug in a specially wired loopback connector, the test is not performed automatically. Refer to the Service chapter for instructions. There are two tests. One is a data test for either 20 mA current loop or EIA interfaces. This test transmits a pattern of data out the transmit line and examines the data as it returns through the receive line. Each bit of the data bus is tested with the eight test characters: 01H, 02H, 04H, 08H, 10H, 20H, 40H, 80H. This group of eight passes through the circuit repeatedly while the microprocessor changes the baud rate after each pass.

The second test, for EIA only, tests the modem control lines to ensure that they can be controlled. Some terminal controller modules have an etch revision at E39 that does not permit EIA testing. These modules can be recognized by the presence of extra wires attached at E39.

Table 4-3-2 lists the test connector wiring.

Table 4-3-2 Loopback Test Connectors

	From	To
EIA:	Pin 2	Pins 3 and 15
	Pin 4	Pins 5 and 8
	Pin 20	Pins 6 and 22
	Pin 19	Pins 12 and 17
20 mA:	Pin 1	Pin 3
	Pin 2	Pin 7
	Pin 5	Pin 8

4.4 KEYBOARD

The VT100 keyboard is a typewriter-like array of momentary, normally-open switches. The array is mounted in a small case with a speaker for audio feedback and electronics for interfacing the array to the terminal. The VT100 keyboard connects to the terminal controller board through a three conductor cable that plugs into the back of the terminal cabinet. The cable carries power, ground, and a complex bidirectional data and clock signal. The terminal sends the clock signal and a status word that controls the LED indictors, the bell, and the keyboard scan process. The keyboard sends the row and column address of each key that is pressed. The terminal's microprocessor then translates that address into an ASCII character and transmits it serially to the host through a UART or performs internal actions such as SET-UP and no-scroll. Refer to Section 4.3 for a discussion of UART principles.

This section describes the operation of the keyboard and its interface hardware and software in the terminal.

4.4.1 Keyboard Block Diagram (Figure 4-4-1)

The bidirectional interface separates incoming from outgoing data on the single signal line. Incoming data from the terminal contains a clock that passes directly to the UART and the address counter circuit. Then the data and clock are integrated. The duty cycle encoded data becomes serial data. The UART deserializes the terminal data and produces an 8-bit parallel output. These bits control the bell and LEDs, and start address scanning, depending on which bits were set by the terminal in the keyboard status byte.

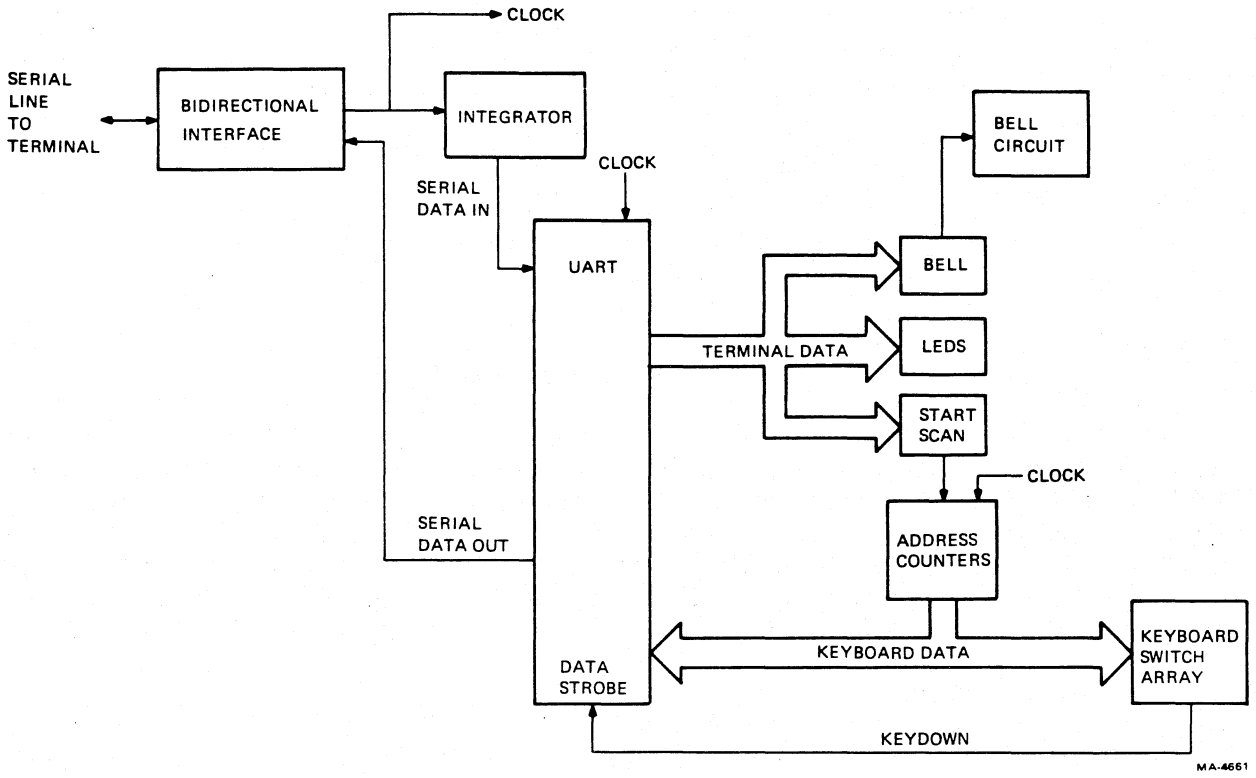


Figure 4-4-1 Keyboard Block Diagram

The address counters start on command and send row and column addresses to the keyboard switch array. When an address matches a key that is down, the Key Down signal strobes that address into the UART. The UART serializes the address and the bidirectional interface sends it to the terminal.

4.4.2 Keyboard UARTs

Information is exchanged between the terminal and the keyboard in serial form. One start bit, eight data bits, and one stop bit are transmitted using a clock derived from the horizontal timing circuits in the terminal. Besides timing the serialization of data in the terminal, the clock is also transmitted to the keyboard to time its circuits. The terminal data is a status byte that controls the keyboard by commanding key scans and other functions.

The keyboard transmits its data in the same format and with the same clock. Its data are the addresses of whatever keys are down during a scan. The last key address sent has the highest address possible and is always sent to indicate to the microprocessor that the scan is complete.

4.4.3 Keyboard Status Byte

The terminal controls the keyboard through a status byte that it sends through the interface along with the keyboard clock. The first six bits of the 8-bit byte (Figure 4-4-2) control the On-Line/Local, Keyboard Locked, and four user programmable LEDs on the keyboard. Every time the status byte is sent, it refreshes the LEDs even if no new action is being taken. The seventh bit is sent only once in a vertical interval and initiates the scanning process in the keyboard. The eighth bit, if sent only once, causes the keyboard speaker to click. (Keyclick is defeatable at SET-UP.) If the bit is sent approximately two hundred times in a row, for about a quarter second, it sounds a bell.

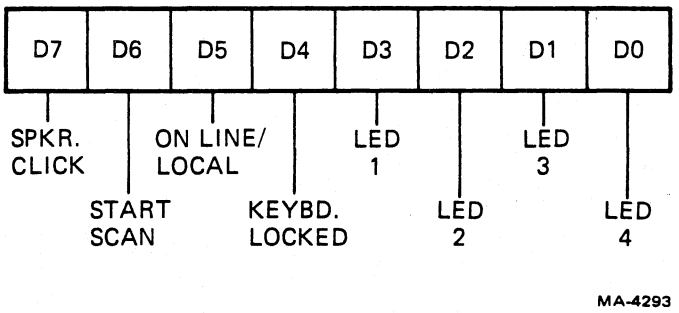


Figure 4-4-2 Keyboard Status Byte

The operating clock for the keyboard interface comes from an address line in the video processor (LBA4). This signal has an average period of 7.945 microseconds. Each data byte is transmitted with one start bit and one stop bit, and each bit lasts 16 clock periods. The total time for each data byte is 160 times 7.945 or 1.27 milliseconds. Each time the Transmit Buffer Empty flag on the terminal's UART gets set (when the current byte is being transmitted), the microprocessor loads another byte into the transmit buffer. In this way, the stream of status bytes to the keyboard is continuous.

4.4.4 Key Address Counter

Keyboard addresses are outputs from a counter that correspond to locations in a keyswitch matrix. The counter can address all locations in the matrix. If a keyswitch is closed, the counter output addressing that location is transmitted. The address counter is a pair of 4-bit binary counters arranged so that only the top seven bits go to the switch matrix. These outputs also connect directly to the UART transmit data inputs. The output of the first bit in the counter is a squarewave with a period equal to the amount of time that each key is sampled during a scan. Key Down L appears at the input to flip-flop E6 when the counter reaches the address of a key that is pressed. Half a sample period later, the first counter bit clocks the Key Down signal through flip-flop E6. The half period delay allows any glitches in the address counter to settle before Key Down asserts Data Strobe. Data Strobe loads the UART transmit buffer with the address count present at the data input at that moment. That address count represents the key that was down when Key Down was asserted.

The UART, which is double-buffered, deasserts Transmit Buffer Empty while the transmit (outer) buffer is full. This stops the counter by blocking the clock at gate E4. As soon as the data moves into the inner shifting register, the transmit buffer empties, TBMT is asserted, and the count continues. In this way, any number of key addresses can be sent to the terminal. The time the scan takes to finish varies with the number of keys down. On the first address load, when transfer from the transmit buffer into the shifting register is immediate, the UART reasserts TBMT almost immediately. For loads later in the scan, the UART deasserts TBMT for a longer period because an address that loads into the transmit buffer must wait with the counter stopped until the previous transmission is done. Because the transmission time is 160 counts and the complete address scan takes only 128 counts, there is a minimum wait of 32 counts or about 20 percent of a character transmission time between the scan of address 7FH and the transmission of address 7FH if the first key in the scan was down. (Refer to Figure 4-4-3.)

Because it is hard-wired, the highest address (7FH) always asserts Key Down and gets transmitted, indicating end of scan to the terminal. The highest bit also clocks flip-flop E3 which clears the counters and stops the count. This is the only way that the scan is terminated. The scan begins again when the terminal sends the Start Scan bit in the status byte to the keyboard. When the data arrives, the UART asserts its Data Available flag. On the next clock transition, flip-flop E6 passes a short, clock-synchro-

nized Data Available pulse to gate E5, resetting the flag in the process. E5 combines the Data Available pulse with the Start Scan bit if present to clear E3, allowing the count to begin.

After the terminal starts the scan, it waits for the 7FH address and then for a vertical interrupt (a synchronizing signal explained in VIDEO) before it will start the scan again. If there are a lot of keys down, the scan may take more than one vertical interval to finish. The keyboard ignores further requests to scan until the current scan is complete.

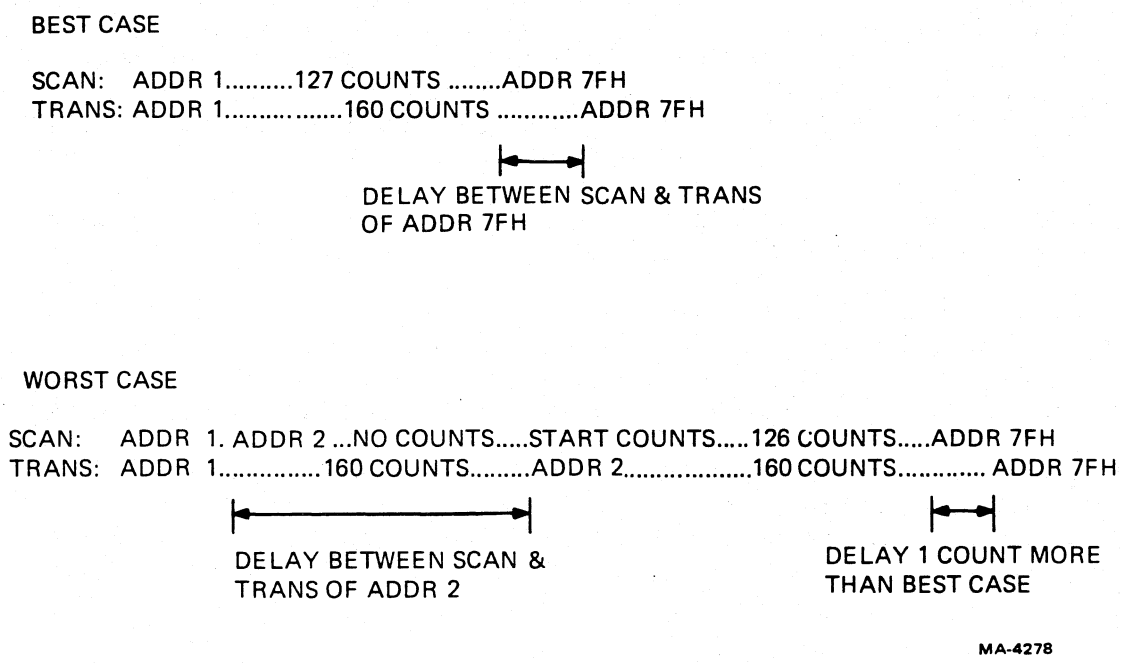


Figure 4-4-3 Key Address Transmission Delays

Here is a formula that estimates the delay between the time that the terminal asserts the start scan bit at its UART and the time that the terminal UART asserts data available upon receiving the final address 7FH. The clock driving the address counter and UART has a period of 7.945 microseconds, there is the number of addresses to the first closed key to be counted, and the serial transmission of an address takes 160 clock periods (16 clocks per bit, 8 data bits, 1 start and 1 stop bit).

	160	start scan command word to keyboard
+	m	counts to first key
+ n ×	160	for n keys down
+	160	transmission of 7FH
Total × 7.945 = microseconds		

For example, suppose that one key, #24, is down.

	160	start scan command word to keyboard
+	24	counts
+	160	transmission of key #24 address
+	160	transmission of 7FH
	504 × 7.945 = 4004 microseconds (4.0 μs)	

4.4.5 Key Scanning and Address Formation

The keyboard is an array of contact pairs arranged in 16 rows and 8 columns (Figure 4-4-4). One side of each pair is connected to all the others in its column and each column connects to +5 volts through a resistor. Each of the eight columns also connects to an input on the eight-to-one multiplexer E14. The other side of each contact pair connects to all the others in its row and to an output on one of the one-to-eight demultiplexers E11 and E13. The seven outputs of the keyboard scan counter control the multiplexer and demultiplexers. The rows are selected by the lower four bits and the columns by the upper three.

A low input to the selected column line on the multiplexer causes a Key Down L signal. If a key is pressed when the row and column address is not on its position, the unselected demultiplexer line is high and there is no change in level across the contacts. If the demultiplexer line is selected, it is low, and the closed contact pulls the column low through the resistor. Each column is scanned top to bottom as the low four address lines count; then the next column is selected and scanned. The complete keyboard scan takes about 1 millisecond when no keys are down.

The last row and column position (address 7FH) is wired to always indicate key down. This value indicates to the terminal that the scan is ended.

4.4.6 Bidirectional Interface Operation

The terminal sends data and clock to the keyboard; the keyboard sends data only. Transmission is asynchronous, full duplex, serial, 8-bit data with one start bit and one stop bit over a single signal line. Four states can exist on the line, representing the two signal states from each end of the line.

Both signals may coexist on the same wire, originate at opposite ends, and simultaneously communicate provided that sensing resistors are put at each end. The interface works by observing the voltage variations on its input (across the sensing resistor) while biasing the input in an opposite direction with its own output signals so that only input variations can cause enough change to exceed the threshold of detection.

4.4.6.1 Interface Line – Refer to the keyboard interface schematic, Figure 4-4-5a. If one side of the line is at +12 volts and the other is at ground, then by Ohm's Law, the center of the two equal resistors will be at $V/2 = 6$ volts. If both sides are at 0 or 12, the center will be identically at 0 or 12. Thus the signal line can either have no current flow but with the junction of the two resistors at either 0 or 12 volts, or the junction can be at 6 volts with current flow to the left or to the right, thereby representing the four required states.

4.4.6.2 Receiving Side – The receiving side of the keyboard interface separates the incoming signal from its own output by delivering a sample of its output to the inverting input of a comparator. Refer back to Figure 4-4-5. This provides an additional input for the comparator which compensates for the variation that occurs on the noninverting input at the same time that the output changes. R12 and R13 (both approximately 20K) and R11 (10K) are a divider providing bias to the comparator. If E8 (an open collector driver) is off (high), then the end of R11 connected to E8 is essentially at +12 volts through R15 (470). The R11, R12, R13 divider outputs 9 volts as shown in Figure 4-4-5b. If E8 is on (low), the end of R11 is at ground, and the divider outputs 3 volts (Figure 4-4-5c).

Meanwhile, the signal from the other end of the signal line is admitted to the noninverting input of the comparator through a resistor (R7) whose value is small compared to the comparator's high input impedance. The positive feedback resistor R8 provides a small amount of hysteresis to improve the circuit's noise immunity.

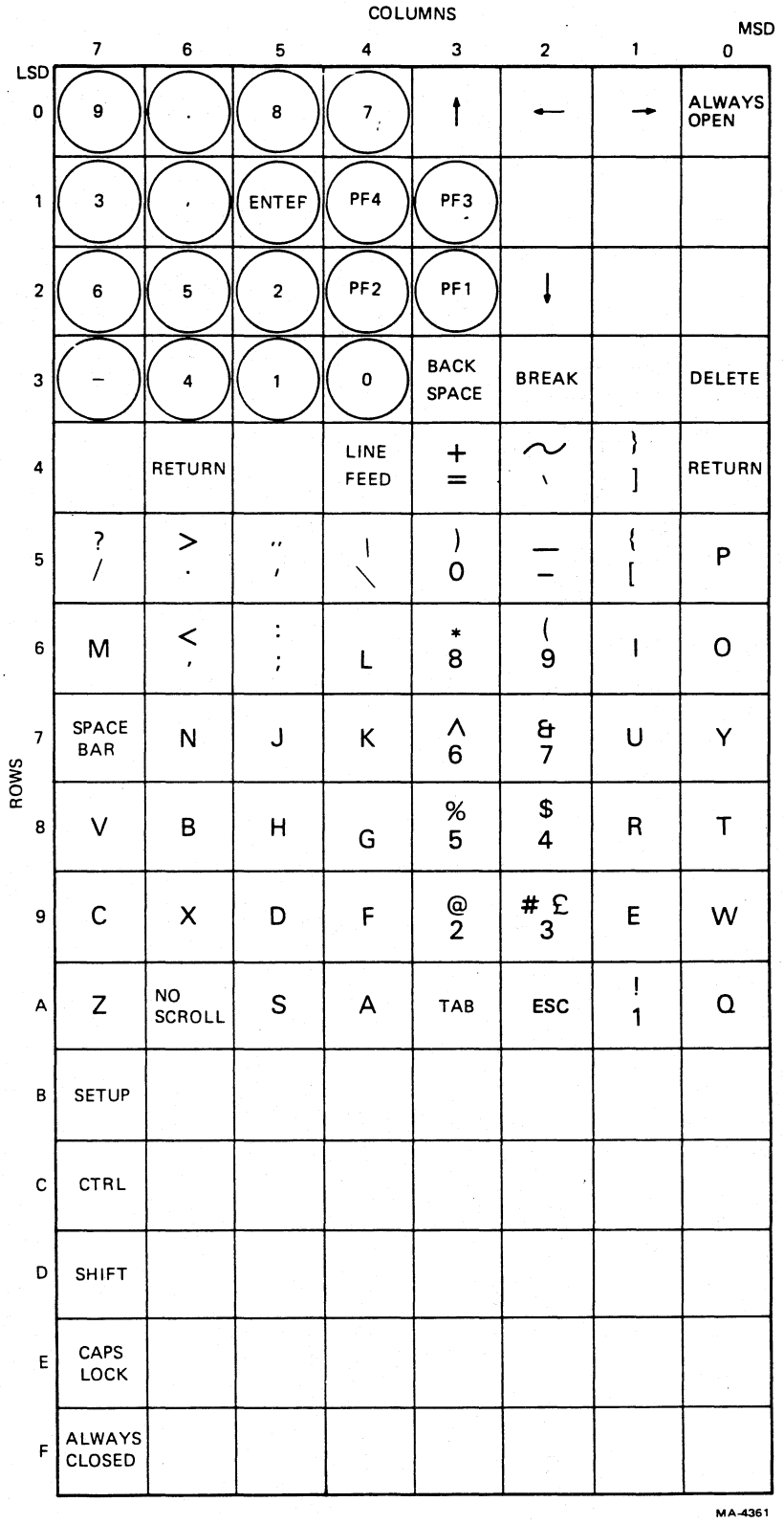


Figure 4-4-4 Keyboard Switch Array

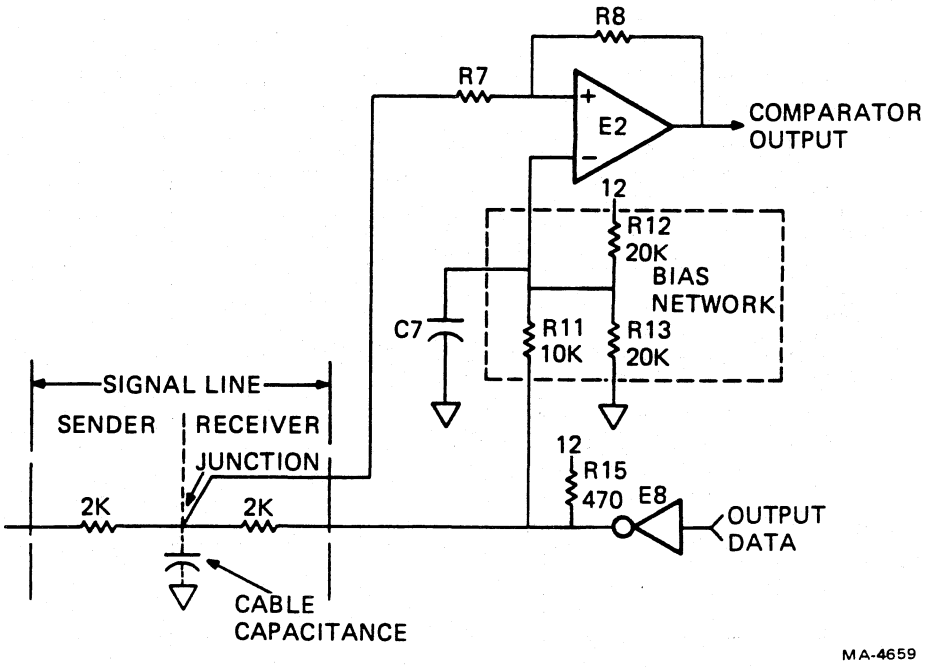


Figure 4-4-5A Keyboard Interface Circuit

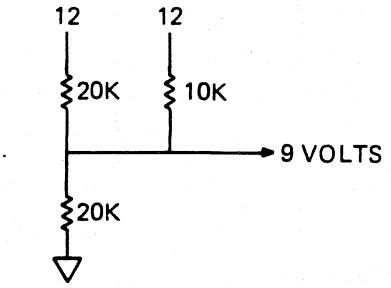


Figure 4-4-5B Bias Network – E8 High

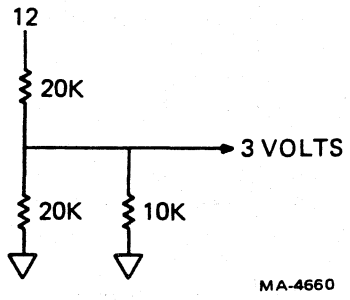


Figure 4-4-5C Bias Network – E8 Low

For the case where the junction is at 12 volts, there is no ambiguity about what signal the sender is sending. The comparator must produce a high output because the sender is outputting a high level. (The receiver is also sending a high level but no distinction between the two needs to be made.) The bias network presents a 9 volt signal to the inverting input, so the comparator sees a +3 volt difference and goes high.

For the case where the junction between the sender and the receiver is at 0 volts, there is again no ambiguity. The comparator must produce a low output because both sender and receiver are outputting low levels. The bias network presents a 3 volt signal to the inverting input, so the comparator sees a -3 volt difference and goes low.

For the case where the junction is at 6 volts, either end could be the high or low sender. The decision is made at each end by each circuit examining its own output to decide whether it or the other end is sending a particular level. If the sending end is at 0, the noninverting input sees 6 volts. The receiving end is outputting 12 volts, and the network outputs 9 volts to the inverting input. The comparator sees a difference of -3 volts and outputs low in recognition of the low level at the sending end. If the sending end is at +12, the noninverting input sees 6 volts. The receiving end is outputting 0 volts, and the network outputs 3 volts to the inverting input. The comparator sees a difference of +3 volts and outputs high in recognition of the high level at the sending end.

Table 4-4-1 summarizes the effects of the various signals.

Table 4-4-1 Keyboard Receiver Signals

Send. End	Rec. End	Non-Invert. Input (Junction)	Invert. Input	Difference	Output
0	0	0	3	-3	0
0	12	6	9	-3	0
12	0	6	3	+3	5
12	12	12	9	+3	5

4.4.6.2.1 Keyboard Cable Compensation - C7 compensates the circuit for the capacitance of the cable. If C7 were not present, the output of the comparator would glitch when the output driver on the same end of the line changed state. This would be caused by the output signal propagating immediately to the inverting input of the comparator but being delayed (by the RC time constant of the line) to the noninverting input. C7 is chosen so that the time constant of the line is the same at both inputs. Because the resistance seen at the middle of the line is approximately 1000 ohms (two 2K resistors in parallel) and the resistance seen at the inverting input is approximately 5000 ohms (one 10K and two 20K resistors in parallel), C7 is about one-fifth of the cable capacitance. The value is not critical because the ratio of the two time constants can be as large as two and still provide acceptable noise immunity.

4.4.6.3 Terminal Data Encoding - The keyboard requires a clock for its operation and is provided with one by the terminal controller side of the interface. To transmit a clock independently of data on the same wire, the terminal side of the interface generates a clock signal within which data is encoded as a pulse width modulation. The terminal circuit produces a 75 percent high pulse width output for the mark state. Data transmission causes the clock output to switch between 75 and 25 percent pulse width (duty cycle).

Figure 4-4-6 is a timing diagram that illustrates the formation of the pulse width modulation. Three nand gates, I, II, and III, combine three signals, Data, LBA 3, and inverted (not) LBA 4. The three gate outputs are wire-ANDed so that all three must have high outputs to produce a high to the out inverter, which drives the terminal's end of the bidirectional interface. The timing is not precisely correct in this drawing because the LBA signals, addresses to the line buffer in the video processor, are not pure squarewaves and have variations in their periods (see the DC011 section). These variations give the keyboard signal the appearance of clustering in groups of four, but they do not affect the operation of the circuit.

The negative transition of each output pulse occurs at the clock interval regardless of the presence of data. This transition is therefore the reference point for the keyboard clock at the receiving end.

4.4.6.4 Combined Interface Signal – Figure 4-4-7 illustrates the four possible conditions on the interface line when the effect of the clock is included. Figure 4-4-8 shows all four states and the transitions between each of them. Two series sensing resistors in the interface circuit divide the signal in half at the wire. Therefore, although the drivers swing 12 volts at each end, the figures show only 6 volt variations.

4.4.6.5 Decoding of Data from Terminal – The keyboard recovers the modulated clock signal sent by the terminal but must also separate the data from the clock. The signal is sent directly to the UART and address counter circuits as a clock. The negative edge of the clock occurs at a fixed interval while the positive edge varies according to the duty cycle modulation. The keyboard circuits use the negative edge and ignore the variable pulse width.

Data is extracted from the combined clock-data by a simple resistor-capacitor filter on one input to a comparator. The other comparator input is referred to one-half the power supply. Because the duty cycle of incoming data is either 1/4 or 3/4, the capacitor charges to that proportion of the supply voltage over the 16 clock periods of each bit. The comparator switches when the capacitor voltage rises or falls past the reference value. The short duty cycle of zeros averages to a low voltage that holds the comparator output low. The long duty cycle of ones averages to a high voltage and switches the comparator to a high state. The comparator output goes to the serial data input of the UART where it is deserialized. When all ten bits of a transmitted character are loaded into the UART, it asserts Data Available. This signal enables the bell and scan start if the appropriate bits were set in the byte. The LED bits remain latched at the parallel output of the UART until the next command byte arrives.

4.4.6.6 Keyboard Output – The keyboard UART serial output goes directly to an open collector driver that swings its end of the bidirectional signal line between 0 and +12 volts. This is shown as E8 and R15 in Figure 4-4-5a. The circuit is identical at both ends of the interface.

4.4.7 Bell

The keyclick/bell circuit provides audio feedback and attention signals for the user. A bit in the keyboard status word controls the bell. Refer to Figure 4-4-9 for the circuit. Capacitor C8 charges to +5 volts through resistor R16. The speaker connects between the capacitor and the collectors of the transistors in E1. When a single status word contains the bell bit, flip-flop E3 toggles and turns on E1. C8 discharges through the speaker and E1, generating a click. When the voltage on C8 falls low enough, it clears E3. E1 turns off and C8 charges up for the next click. The value of C8 is selected to determine the volume of the click. D8 protects the transistors from inductive spikes from the speaker.

If the bell bit is set for many words in succession, the UART latch holds the data output constant. A one clock period pulse from the Data Available flip-flop E6 gates the bell bit through E5 to form a clock to E3. As C8 discharges through the speaker and E1, E3 clears itself, turning E1 off. Then C8 charges up again until the next Data Available pulse clocks E3 on again to repeat the discharge cycle. C8 discharges fast enough so each Data Available pulse (which arrives every 1.28 ms) triggers a cycle,

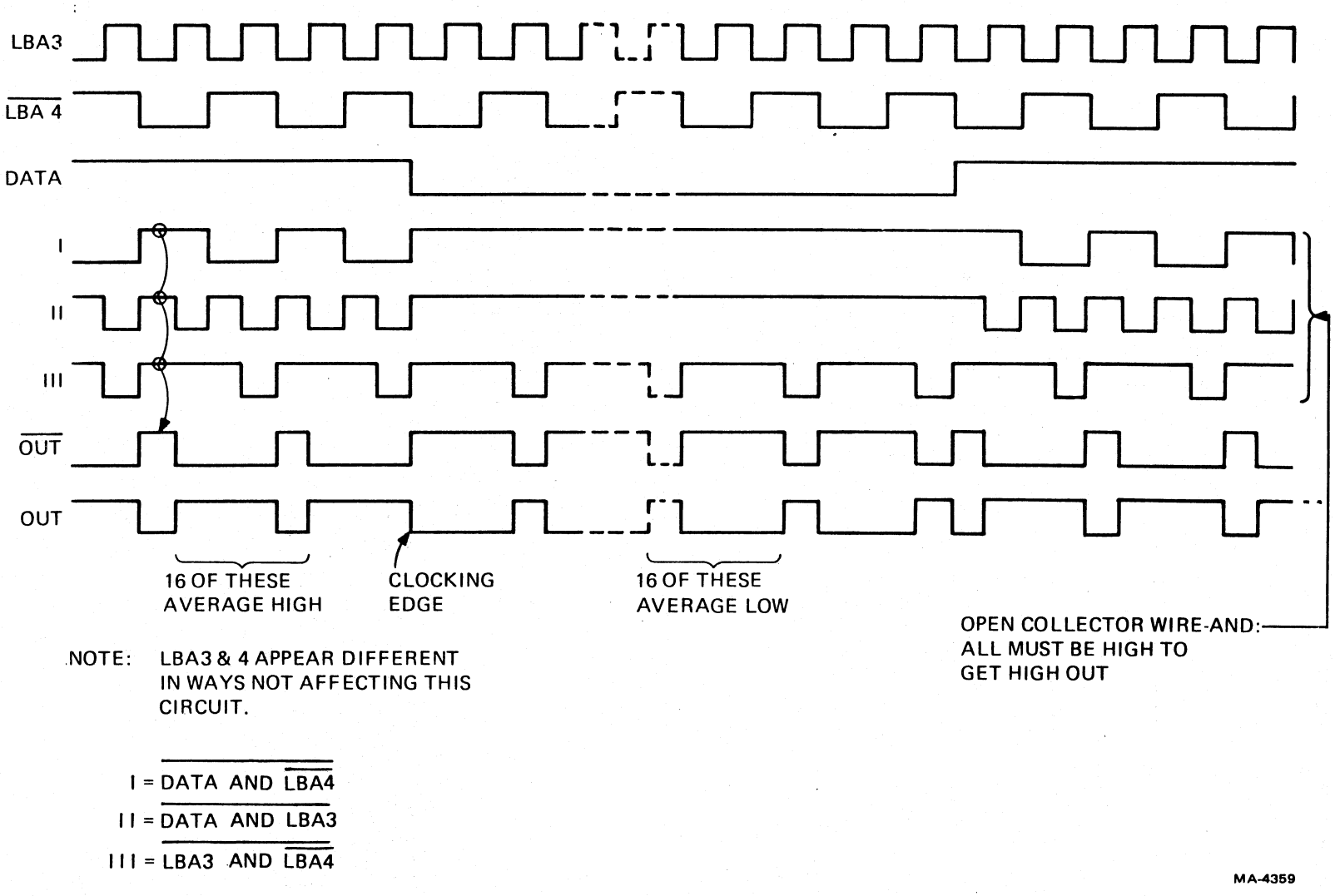


Figure 4-4-6 Encoding of Terminal Data and Clock

allowing the circuit to produce an 800 hertz tone. Bell is generated by setting the bell bit for 0.25 seconds (about 200 status words). Each cycle of the tone is at a reduced amplitude compared with the single keyclick because R16 is selected to limit C8's charging rate. The overall effect of the tone burst on the ear is that of a beep.

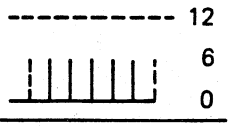
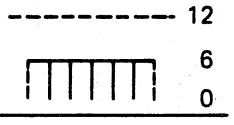
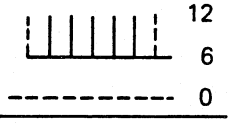
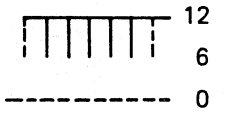
KEYBOARD	TERMINAL	INTERFACE STATE
0	0	
0	1	
1	0	
1	1	

Figure 4-4-7 Four Keyboard Interface States

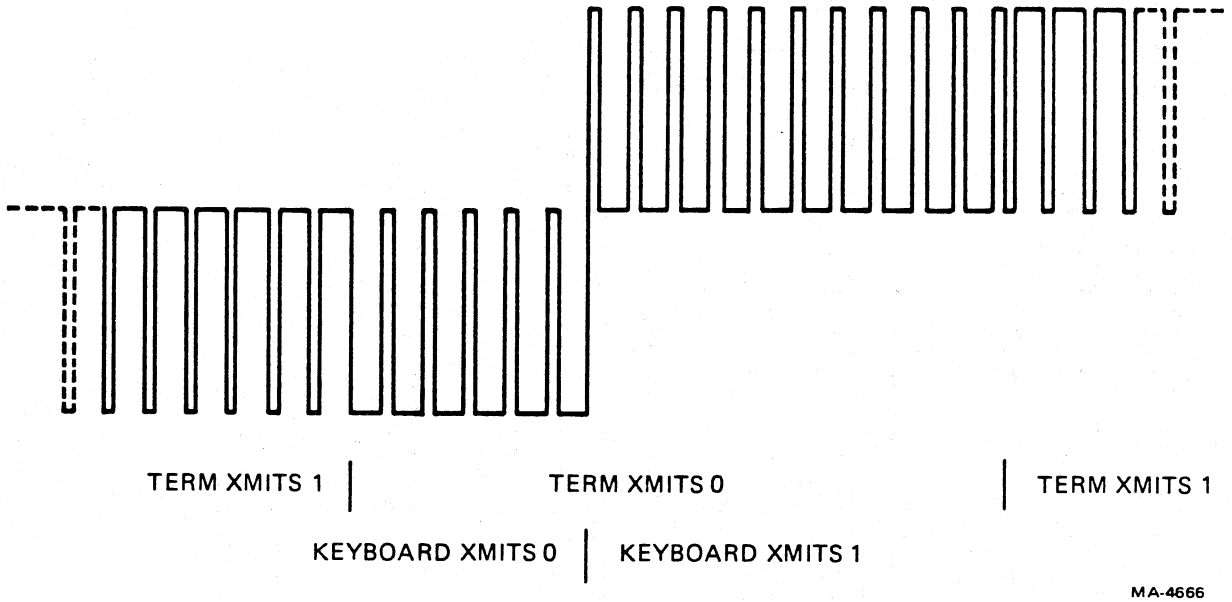


Figure 4-4-8 Keyboard Interface Signal

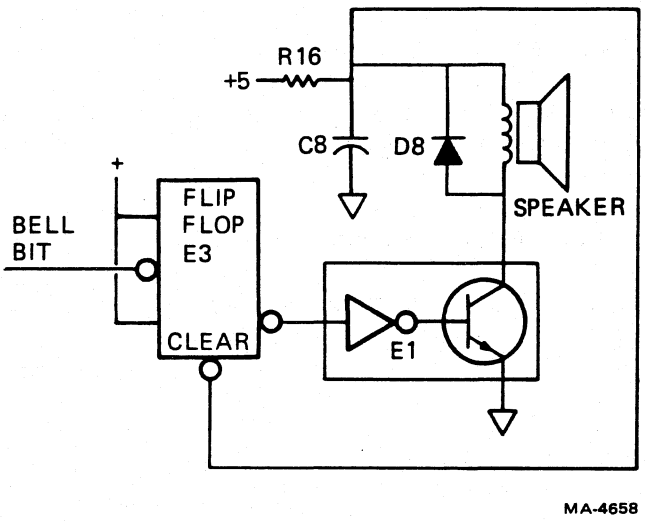


Figure 4-4-9 Bell Circuit

4.4.8 Keyboard Interrupt Routine

When the microprocessor responds to an interrupt from the keyboard UART and reads a key address from the UART data output, it immediately range tests the address. The function key addresses are all above the regular key addresses, with SET-UP the lowest at 7BH and the always down Last Key at 7FH. An incoming function key address causes a bit to be set in a flag byte called Keys (Figure 4-4-10).

When a key address below the function range arrives, the microprocessor checks the low three bits in Keys for the key count. If the count is less than three, the key address is stored in a three place New Key Address Buffer and the counter is incremented. If the count is already three, the counter is incremented but the key address is discarded.

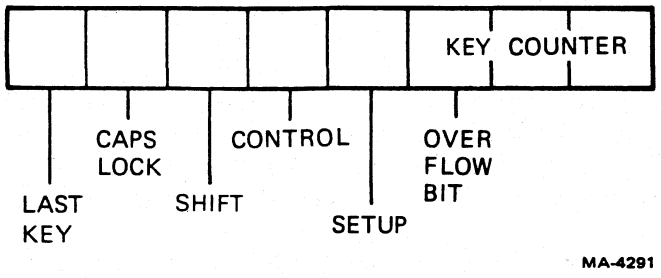


Figure 4-4-10 Keys Flag Byte

4.4.9 Logical Keyboard Processor

The logical keyboard processor is that portion of the operating firmware that manages the interpretation and transmission of keyboard data. It consists of several processes.

4.4.9.1 Key Recognition – For a key to be recognized as a new key, it must not have been down in the scan before entry is accepted. The microprocessor checks each key's history at each scan. If a key was down during the last scan, it is old and is not entered. Only new keys, those not previously seen, are entered. This system allows a key to be held down without being continuously entered at each scan. (This process and auto repeat are discussed later.)

If a key is detected as down for the first time in a while, the microprocessor assumes that it has been pressed. During the scan when the key is first down, the contacts may bounce for several milliseconds. The time window when the contact is scanned is very short. If the contact happens to be bouncing open during that interval, it is not detected in that scan but the time between scans is long so it is finished bouncing by the next scan and is detected normally. If the contact happens to be closed for the first scan while still bouncing, it is detected. It is also detected on the next scan after it has stopping bouncing but now it is an old key and is not reentered.

When the microprocessor is free to perform its background routines, it processes the results of the last keyboard scan. First it checks the high bit of the Key's byte to see if the scan is finished. If it is not, the microprocessor continues with other work (exits). If it is , the microprocessor checks the key counter overflow bit representing four or more keys sent in the scan. If the bit is set, the microprocessor clears the New Key Address Buffer and exits.

If the overflow bit is not set, the first key is taken from the new key address buffer and tested. If it is either the SET-UP or NO SCROLL key, the microprocessor acts on it immediately and branches to the appropriate routine. It then returns to the keyboard process. (Refer to the microprocessor section for a discussion of SET-UP and to the Communication section for no scroll.)

Another three place buffer contains the keys from the last scan. The microprocessor compares the three new keys with those in the old key buffer. If an old key is not in the new key address buffer, that key is cleared from the old key buffer. New keys then go into the old key buffer. Each key address is only seven bits long, so the high bit in each key entry is used to indicate how long that entry has been in the buffer. If a key is new, the bit is set to 0. This means that the microprocessor has only seen the key once. If the key appears in the new key address buffer on the next scan, the microprocessor sets the high bit to 1, converts the key address to an ASCII code, and sends it to the keycode buffer. Only one key is converted and sent in each cycle of the logical keyboard processor routine. Since the set bit indicates that the key has been sent, in the next cycle that key will be ignored and the next key will be processed.

4.4.9.2 Key Rollover – Key rollover means that more than one key can be down at the same time and be accepted. Normally the VT100 accepts 3-key rollover. If the keys were pressed during different keyboard scans, they will be accepted in the order in which they were pressed. If they were all pressed during the same keyboard scan, they will be accepted in the order of their addresses.

Certain conditions will limit the rollover to only two keys. The 2.5 key rollover specification reflects the presence of these conditions. Because there are no isolating diodes in the switch matrix, certain patterns of contact closure can produce false key down indications. Specifically, three switches closed in three corners of a rectangular pattern, as in Figure 4-4-11, will cause a fourth apparent key address to be sent to the terminal. (Refer back to Figure 4-4-3 to see how the pattern fits into the row-column configuration.) For this reason, although any number of key addresses may be sent by the keyboard during a scan, no more than three may be sent if any are to be accepted. If four or more appear, the terminal ignores all of them and waits for a scan with only three. The special function keys (SHIFT, CAPS LOCK, CONTROL, SET-UP) are in a part of the matrix where there is no pattern sensitivity and no ambiguity. They all are accepted in the same scan with the regular keys and are not counted in the 3-key maximum.

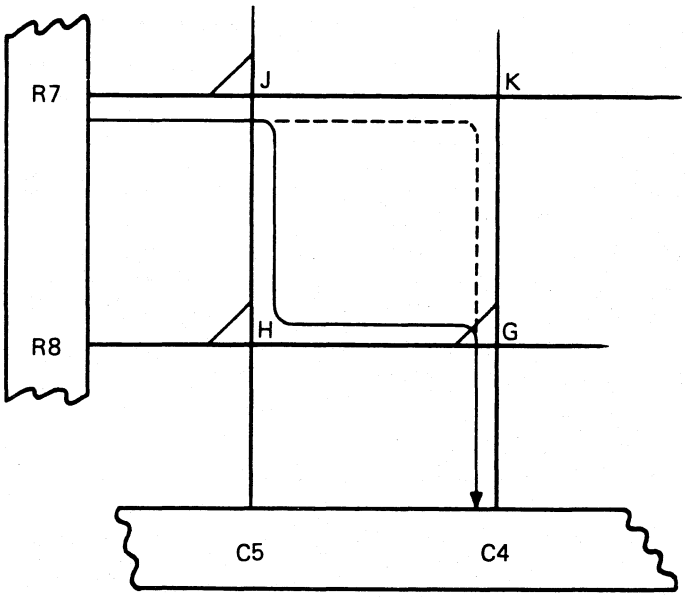


Figure 4-4-11 Sneak Path

The sneak path problem is also the reason that the keyboard processor looks for the appearance of a key in two successive scans. In Figure 4-4-11, the keys are scanned in the order J, H, K, G. Normally, the keyboard processor counts the number of keys in a scan and ignores all of them if the count is over three, as it is in this case. But it is possible for a user to briefly press keys J, H, and G and then release G before the scan is completed. Then the keyboard processor might see J, H, the false key K, and, because G was lifted just before it was scanned, register only three keys. One key would be false, but with a count of only three, all would be accepted. To prevent this, the keyboard processor looks for the same keys two scans in a row. Because the G key is released, the K key does not appear in the second scan, and only J and H appear and are accepted by the keyboard processor.

4.4.9.3 Generation of Codes – Because the keys are essentially randomly ordered with respect to the ASCII standard, the program ROM includes several look-up tables that assist in the generation of ASCII codes. Most keys convert directly from an address to an ASCII code. The codes for alphabetic keys with SHIFT or CAPS LOCK down are formed from the tables with bit 5 forced to 0 to produce uppercase alphabetic codes. Holding down the CONTROL key when another key is pressed causes another table look-up. If the key is in the table of valid control codes, that keycode is changed by forcing bits 5 and 6 to 0. For example, the ASCII code for the letter "g" is 67H. Holding down the CONTROL key and typing G transmits the ASCII code 07H.

	B7	B6	B5	B4	B3	B2	B1	B0
Normal code	x	1	1	0	0	1	1	1
Control code	x	0	0	0	0	1	1	1
Shift code	x	1	0	0	0	1	1	1

Nonalphabetic keys have a second look-up table that provides the shifted code given the unshifted code. CAPS LOCK performs the shift function only on alphabetic codes, leaving the nonalphabetics to be performed with an extra shifting action. If a key that does not make a standard control code is pressed with CONTROL, it is not sent.

4.4.9.4 Keyboard Transmit Buffer - Some keys generate three byte ASCII codes. The auxiliary keypad, for example, when in alternate mode, transmits escape sequences that a system can be programmed to interpret in a special way. Cursor control keys also send escape sequences which the operator can use to control the cursor position. To store the codes that might be generated by three simultaneous keys, a 9-byte buffer is provided for the communication port. If the buffer fills up, the keyboard is locked and the appropriate LED lights. When a key is about to be converted to ASCII and stored in the buffer, the microprocessor checks the buffer to see if there is room. Since any key might produce three bytes of code, the microprocessor must be sure that there are at least three places available in the buffer. If six 1-byte keys have been sent, the next 1-byte key leaves only two places. Therefore, the keyboard locks with only seven places filled in the buffer.

4.4.9.5 Auto Repeat - If only one key is in the old key buffer (in the logical processor), and if it appears continuously, it may be a candidate for auto-repeating. A key with control cannot repeat, and a nonrepeat table contains a few keys that do not repeat. These are SET-UP, NO SCROLL, ESCAPE, RETURN, BREAK, and ENTER.

A count-down timer gets loaded with a value each time the buffer changes. When there is no change for a while, the timer decrements to zero. This takes about one-half a second. Then the key is sent to the keyboard buffer a second time and the timer is loaded with a smaller value. This time the count lasts about one thirtieth of a second. The key is sent and the timer reset the same way until the key is lifted or another key is pressed while the first is still down. If the second key is lifted, the count continues at the fast rate. The timer is decremented every time a status byte is sent to the keyboard (every 1.27 ms).

4.5 NONVOLATILE RAM

The nonvolatile RAM (NVR) used in the VT100 can retain its data for about 10 years and 1 billion reads. This type of device is also called electrically alterable read-only memory (EAROM). It contains the programmable configuration information that would otherwise have to be reentered every time power was turned on or else stored in mechanical switches.

While the microprocessor sets up initial conditions using the specifications in the NVR, a user can change those settings at any time from the keyboard. However, the new settings are only stored in the scratchpad memory until a special Save sequence is initiated from the keyboard to store the settings in the NVR.

This section contains an overview of NVR principles, the circuitry used with this particular device, and the microprocessor's procedure for using the NVR. Information about the SET-UP data contents may be found in Section 4.7.11.

4.5.1 Principles

An NVR memory cell consists of an MNOS (metal nitride oxide semiconductor) field effect transistor whose gate is insulated with a material (silicon nitride) that can accept charge movement through itself and yet hold a charge as a superior insulator. Under high voltage conditions, electrons can migrate between the insulating layer and the substrate, leaving a net charge buried in the insulator. This is the process of erasing and writing.

An FET transistor normally has a physically determined voltage required between its gate and channel for it to conduct. A charge in the insulator between the gate and channel adds algebraically with the voltage on the gate and shifts the value of threshold voltage accordingly.

A reference voltage is applied to the gate of a memory transistor in the read process. If the threshold is below the reference, the transistor will conduct. If the threshold is above the reference, there is no conduction. Decay of the stored charge causes the difference between high and low thresholds to become smaller. At normal operating temperatures this decay takes 10 years to affect recovery of data.

Erasure consists of writing all the memory cells in a word to the same low threshold. Writing pushes the selected cells to a high threshold. The time required to write or erase is determined by the thickness of the gate insulation, the voltage used, and the temperature of the device. The thickness of insulation is a trade-off between writing time and data longevity.

The writing process damages the insulating properties of the nitride layer. With the ER1400's layer characteristics, its data retention time is at least 10 years provided that it is written less than 1000 times. The data retention time is at least 1 year if it is written between 1000 and 10,000 times.

4.5.2 NVR Device

The ER1400 (E24) is a 1400-bit memory arranged as 100 14-bit words. Data and addresses enter or leave the device in serial form through a single bidirectional line. Information is shifted with an external clock; identification of the meaning of the bit stream is made by setting three control lines that specify the operation in progress (Figure 4-5-1).

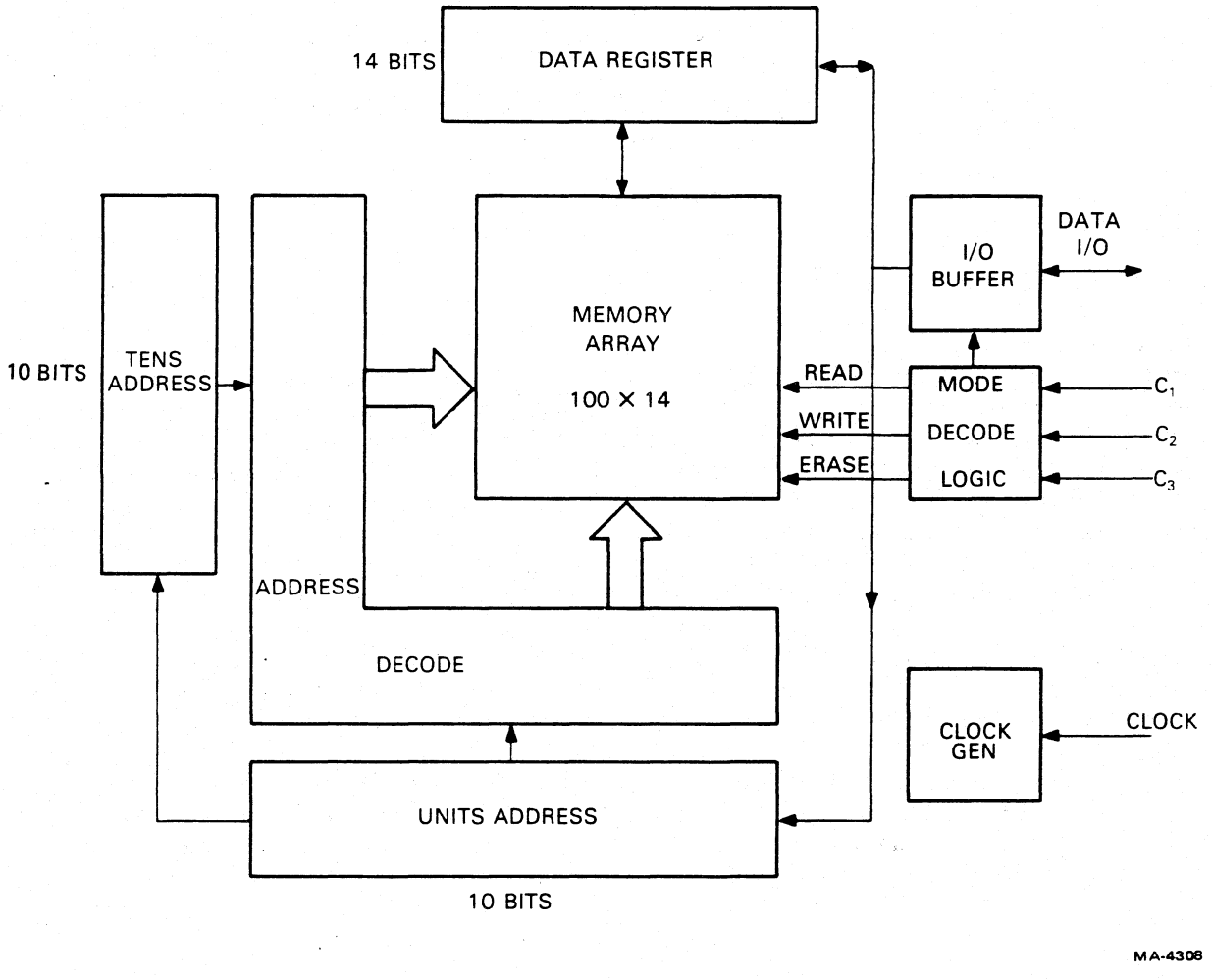


Figure 4-5-1 ER1400 NVR Block Diagram

4.5.3 NVR Control

Seven states of the three control lines give commands to the NVR device:

State	Data Bus C3	C2	C1	
0	H	H	H	Standby. The device output floats.
3	L	L	H	Accept Address. Two 1 of 10 addresses are shifted in at the clock rate. The first group is the 10's decade and the second is the 1's decade of the 1 of 100 word address.
2	H	L	H	Erase. The word stored at the addressed location is erased to all zeros.
7	L	L	L	Accept Data. The data register accepts serial data shifted from the I/O pin. The address register remains unchanged.
6	H	L	L	Write. The word contained in the data register is written into the location designated by the address register.
4	H	H	L	Read. The addressed word is read from memory into the data register.
5	L	H	L	Shift Data Out. The output driver is enabled and the contents of the data register are shifted out.
1	L	H	H	Not Used.

4.5.4 NVR Support Circuits

Several factors in the ER1400's design require special treatment by its support circuitry. It requires 35 volts for the write and erase processes. Its signal levels are specified to be Vss (the positive power supply) for the high level and 12 volts lower than that for low. The logic of these signals is negative: 1 is asserted as a low level, and 0 is asserted high. When driving data, the NVR's output actually switches between +12 and -23 volts with a high impedance in series with the negative source. This requires that an external clamping diode (D4) be present to pull the low level up to ground through the high impedance. 12 volts and ground are thus the I/O logic levels. The terminal controller is made with TTL, so open collector buffers with pull-up resistors to +12 volts are the interface.

The Standby command of the ER1400 is not used in the VT100. Instead, Accept Data serves as the command to the NVR during idle periods. The code for Accept Data is all inputs low. This arrangement protects the contents of the NVR from spontaneous writes that might occur due to the power-down behavior of E29, the 7417 open-collector buffers. E29, in powering down, tends to drop its outputs from the high to the low state in an unpredictable order. This could present a write command to the NVR before the power supply voltages drop low enough, if the NVR had been maintained in the Standby mode by keeping its inputs high. By keeping all outputs low with the Accept Data command, no new command can occur accidently during power-down.

The pull-up resistor used to drive the data input is too low an impedance for the ER1400 output to drive. Line C2 is high during state 5 when the output driver is enabled, and low when data is being input to the NVR, so transistor Q1's base is connected there. When the line goes high, Q1 turns off, raising the impedance at that point to the leakage values of Q1 and E29, and the input impedance of comparator E48. D4 clamps the output to -0.6 volts to protect the comparator input from leakage to -23 volts in the ER1400.

Later VT100s may have power down circuitry in series with the Vgg pin on the ER1400 to ensure that the -23 volt supply is cut off when the +5 volt supply is low. This would prevent writing during power-down.

The comparator is a high impedance load for the ER1400 output driver and is biased to switch at +8 volts. This threshold ensures that a wide range of output levels will still pull the low state down enough to switch the comparator. The comparator output, pulled to +5 volts by a resistor, provides the NVR DATA bit to the flag buffer. The microprocessor reads the flag buffer after it sees the NVR clock flag change, and samples the NVR DATA bit to get the serial data.

The NVR clock is the lowest frequency line buffer address signal and occurs at the horizontal line rate, 15734 kHz. This is the bit shifting rate during address and data transfers. A read operation requires only a single clock cycle to transfer data into the data register but an erase or write of a word each takes 20 milliseconds.

4.5.5 Microprocessor Management

During an NVR operation, the microprocessor uses 21 bytes of scratchpad memory to set up a group of NVR address or data bits. Each group consists of 20 bits of address or 8 bits of data with another 6 bits of fill for the 14 bit NVR word. These groups must enter the NVR serially with precise timing. The microprocessor cannot calculate the groups fast enough to keep up with the shifting process while also managing the shifting process, so it saves time by precalculating and storing each group of bits. Then it reads the stored groups, and delivers them to the NVR at the NVR clock rate through the NVR latch.

The microprocessor serializes its data by rotation in a register. It combines the data with command bits to control the NVR device. Output from the microprocessor reaches the NVR through the NVR latch. The latch is updated at each clock during an NVR operation. One unrelated signal from the communication port is routed through an extra bit in the NVR latch device.

The microprocessor reads the NVR during the power-up process. The bits are deserialized by rotation as they are read in. Although 14 bits from each NVR word are written or read, only 8 bits are used by the microprocessor. The data goes into location in the scratch portion of RAM for use during a later portion of the power-up.

4.5.6 NVR Timing

Use of the ER1400 in the VT100 takes place during normal operation of the video circuits. The 8080 must be free to operate on every scan line in order to load data and address and shift data out (the ER1400 is clocked at the horizontal rate and this signal is provided as a clock to the flag word for the 8080). Because of the above two conditions, it is necessary to ensure that all DMAs performed by the video processor are short.

The processor works fast enough to permit the display of the short message "WAIT" at the left edge of the screen. This causes the DMA to be longer but informs the operator during long save and recall sequences. The timing for all of these conditions is shown in Figure 4-5-2.

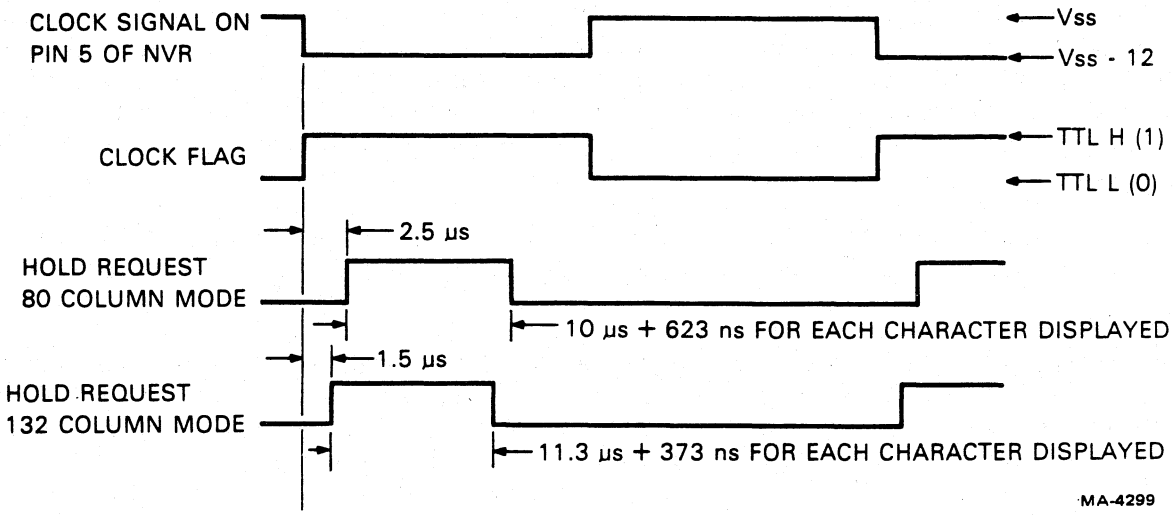


Figure 4-5-2 NVR Signals

All data and command changes to the ER1400 occur immediately following the falling edge of the clock flag (the rising edge of the signal on pin 5 of the ER1400); the data is strobed into the NVR on the opposite edge. The two one-of-ten codes for address have a single zero and nine ones (at D0 of the 8080 bus).

When the "shift data out" mode is entered as per the timing diagrams in Figure 4-5-3, the first data bit may appear when the mode is entered but will become stable 25 µs later; subsequent data bits will be shifted out on the falling edge of the clock flag (rising edge of the signal on pin 5 of the chip) and will become valid 25 µs later. This means that, following a change to "shift data out" mode or a falling edge of clock flag during this mode, a delay of 25 µs must occur before reading of the NVR data flag is attempted. The first bit shifted in when writing is the first bit shifted out when reading.

When using the ER1400, it is necessary to operate with interrupts off.

4.6 VIDEO PROCESSOR

The video processor is the heart of the VT100 display. It is composed of the devices shown on the right side of the terminal controller block diagram (Figure 4-6-1). This section discusses the general mechanism that converts data into a visible display, followed by a discussion of the two central devices (the timing and control chips) followed by a general discussion of all the other blocks on the video processor side of the block diagram. The interactions between the data paths on the left of the diagram and the processor on the right are covered in Section 4.7, Microprocessor – Video Processor Interface.

4.6.1 Introduction

The video processor converts data into an electrical signal that a CRT monitor can turn into visible letters, numbers, and symbols. The video processor works with the characteristics of the CRT monitor to do this. A brief description of these characteristics precedes an introduction to the video processor's operation.

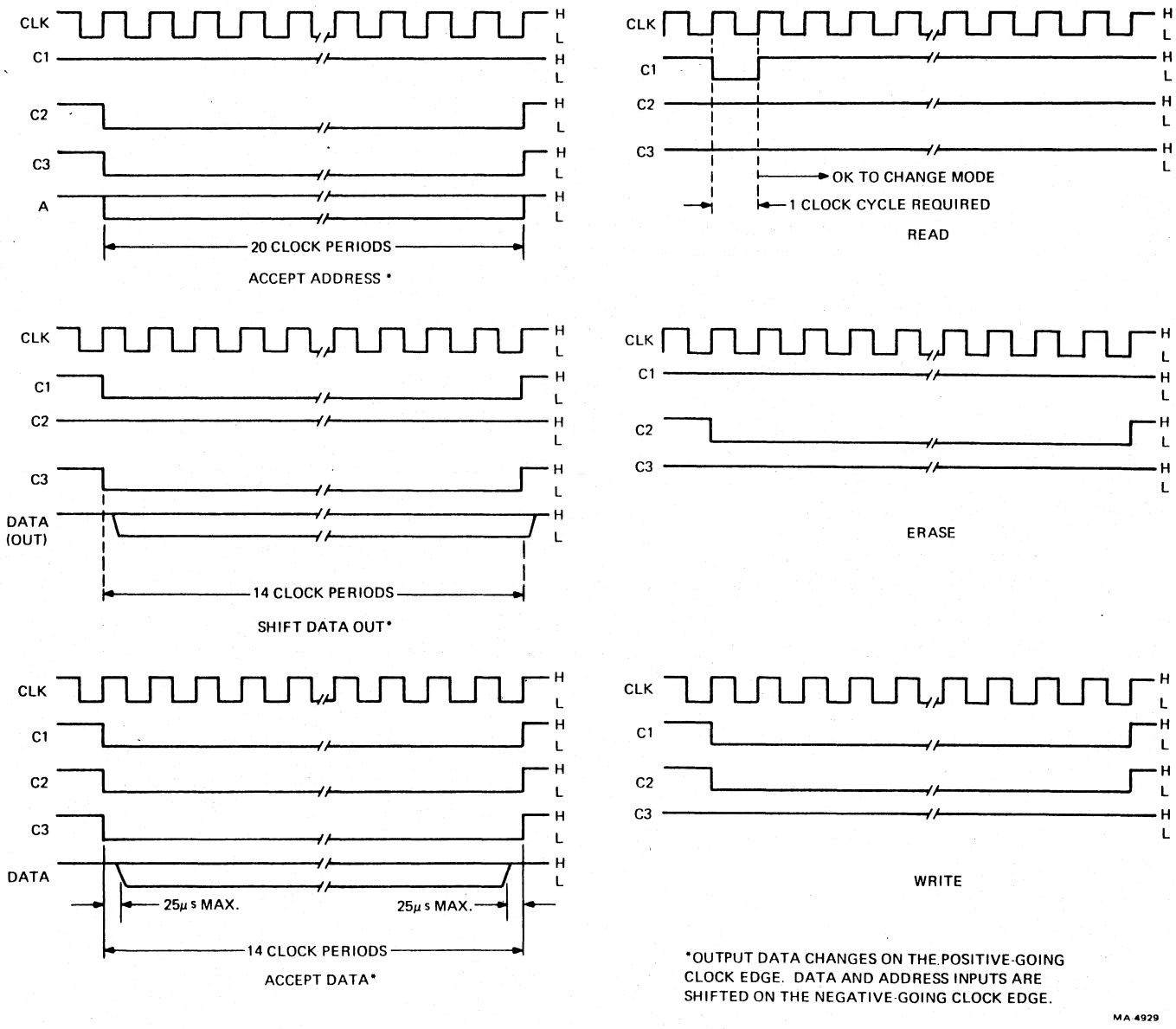


Figure 4-5-3 NVR Timing Diagrams

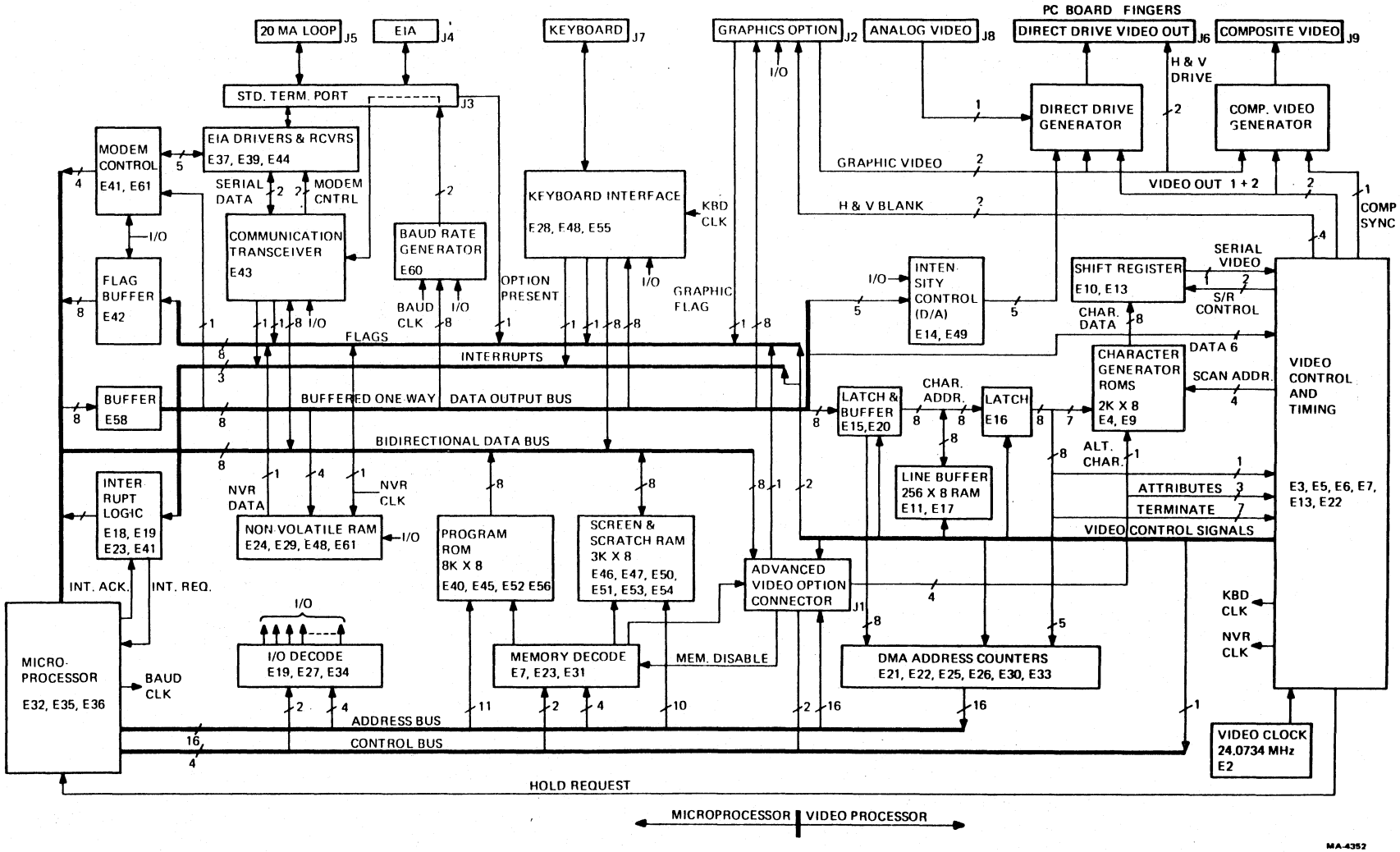


Figure 4-6-1 Video Processor Block Diagram

4.6.1.1 The Raster – The raster is that area on the CRT screen that is scanned (passed over) by an electron beam moving in a regular pattern. Deflection coils cause the beam to quickly scan a series of horizontal lines while moving relatively slowly down the screen. This scanning repeats quickly and constantly, and persistence of vision makes the entire screen look continuously scanned. The beam may be on or off, lighting the fluorescent phosphor on the face of the CRT or leaving it dark, but the beam's continuous motion traces and defines the raster.

4.6.1.2 Character Formation – As the beam moves in its horizontal scans, it can be turned on and off very fast. This means that a spot of light (called a dot) can be produced anywhere along each horizontal scan line. Each scan contains the same number of potential dots. If only one dot is lit in a scan but dots in the same position on several successive scans are also lit, the screen appears to have a vertical line on it. This ability to line up dots on different scans is the key operating feature of the video processor.

Limiting our discussion to 80 column lines for this description, each character that can be displayed on the VT100 is made up of a matrix of dots, ten wide and ten high (Figure 4-6-2). There are 800 dots in a scan and the raster is made of 240 scans. So there are 80 groups of ten dots in each scan horizontally, and 24 groups of 10 scans vertically. Each 10 dot × 10 scan group is a character cell, where a character can be displayed, and there are 80 × 24 character cells on the screen. As the electron beam scans the raster, the video processor turns the beam on and off, assembling the characters scan by scan.

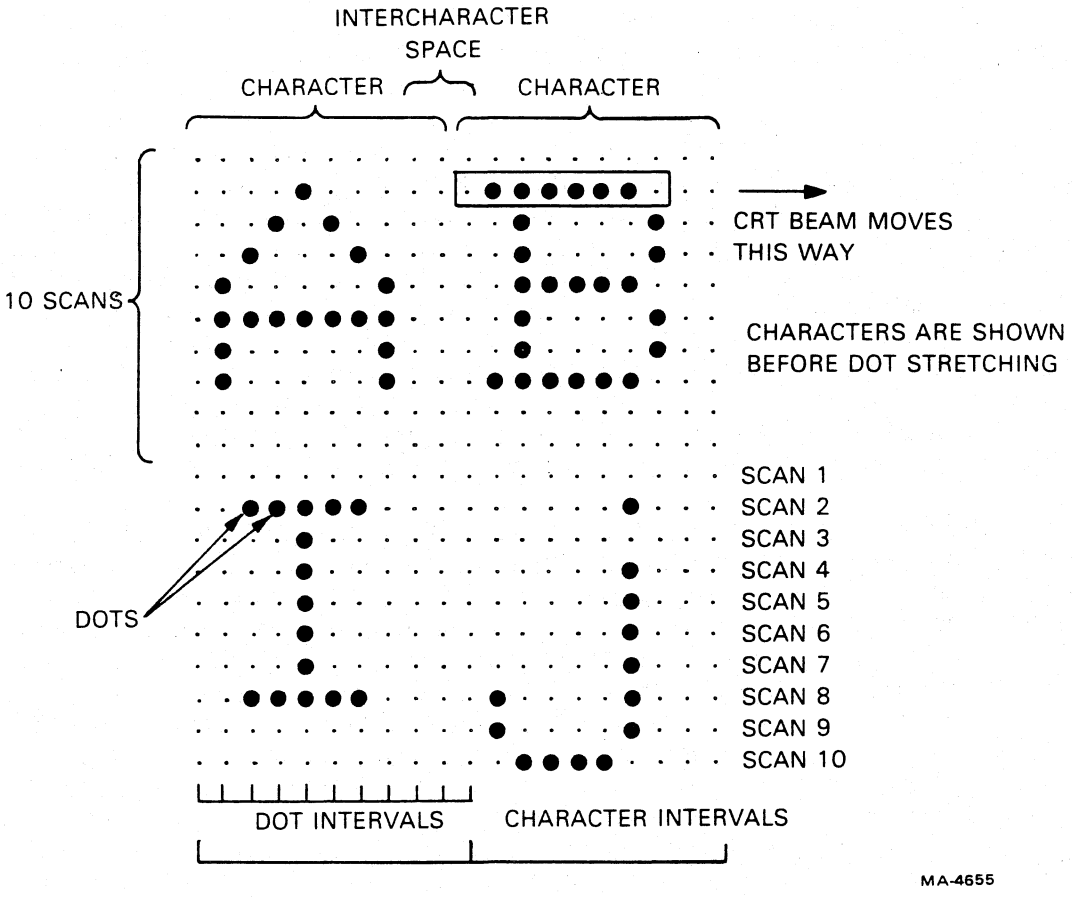


Figure 4-6-2 Dots, Scans, and Characters

4.6.1.3 Video Processor Data – When we say the characters are assembled scan by scan, we mean that only one scan of information about a character is displayed and then the same scan for the next character is displayed. This continues to the end of a line of characters. Then the next scan of the first character is displayed, followed by the same scan of the next character, and so on. Therefore, each character must enter the video processor ten times, once for each scan, and remain only until the next character in the line is displayed.

Each character in a line is stored in one of a group of adjoining locations in the screen RAM. (See Figure 4-6-3 for the video processor functional diagram.) The process of moving a line of character data from the screen RAM to the video processor takes the same amount of time as a scan. During data movement, the microprocessor cannot use the RAM. So, to give the microprocessor as much working time with the RAM as possible, the video processor accepts the line of character data for display during the first scan and stores it in its line buffer at the same time for use during the other nine scans. Movement of data from the screen RAM to the line buffer by the video processor is called direct memory access (DMA). During the DMA, the video processor provides addresses to the screen RAM with the address counters. The data is stored in the line buffer which gets its addresses from the line buffer address (LBA) outputs from the DC011 timing chip. Both kinds of addresses change values when they receive a clock (called character clock) that occurs after each 10 dots. This clock makes the character data in the video processor change at the right times to provide proper alignment of the display.

The character latches hold the data coming from the screen RAM or line buffer and ensure that the data remains stable for long enough periods to be written into the line buffer or the video shift register. The buffer between the latches is tristatable and, during non-DMA time, prevents the normal data flow on the microprocessor data bus from interfering with the video processor's reading of data from the line buffer.

4.6.1.4 Video Processor Character Generation – Data, coming either from the screen RAM for scan 1 or the line buffer for scans 2 through 10, becomes part of an address to a character generator ROM. (See Figure 4-6-4, Character Generator Example.) The rest of the address comes from a scan counter in the DC012 control chip. The scan counter addresses the ROM according to which of the ten scans is to be displayed. The 4-bit scan counter skips over the other 6 possible addresses to the ROM, so the ROM contains data in only 10 out of 16 locations. The output of the ROM is eight bits that represent the pattern of sequential dots to be displayed for that character on that scan. The eight bits enter the video shift register, a serializer that converts the eight parallel bits into a one-bit-wide stream. An extra flip-flop stores the last bit so it can be output to the stream two or three extra times (depending on line length) to fill the intercharacter space. The stream enters the DC012 control chip, where the final adjustments for video display are made, and then the video signal goes to the CRT monitor.

4.6.1.5 Attributes – Three attributes apply to the VT100 display: character, line, and screen. Character attributes provide a special appearance to characters as they appear on the CRT screen. In the basic VT100 (without an advanced video option) only one bit of memory (called the base-attribute bit) is available to each character on the screen. The original character data from the screen RAM is eight bits wide but only seven bits define the character itself. The eighth bit defines the base attribute. The attribute bit bypasses the character generator ROM and video shift register and enters the DC012. There it controls the presence or absence of the attribute as that character is displayed. The base attribute is displayed as either reverse video or underline, depending on the selection of the cursor at SET-UP, and is invoked by the base attribute bit. Reverse video appears as all 10 scans of a character cell reversed (black changes to white and vice versa). Thus, if two vertically adjacent characters are in reverse video, no black space appears between them. Underline forces the ninth scan on (off with reverse video screen attribute.) Once a character attribute or combination of attributes is set, all displayable characters sent to the terminal have that attribute regardless of where they are placed on the screen. This continues until the attribute selection is changed.

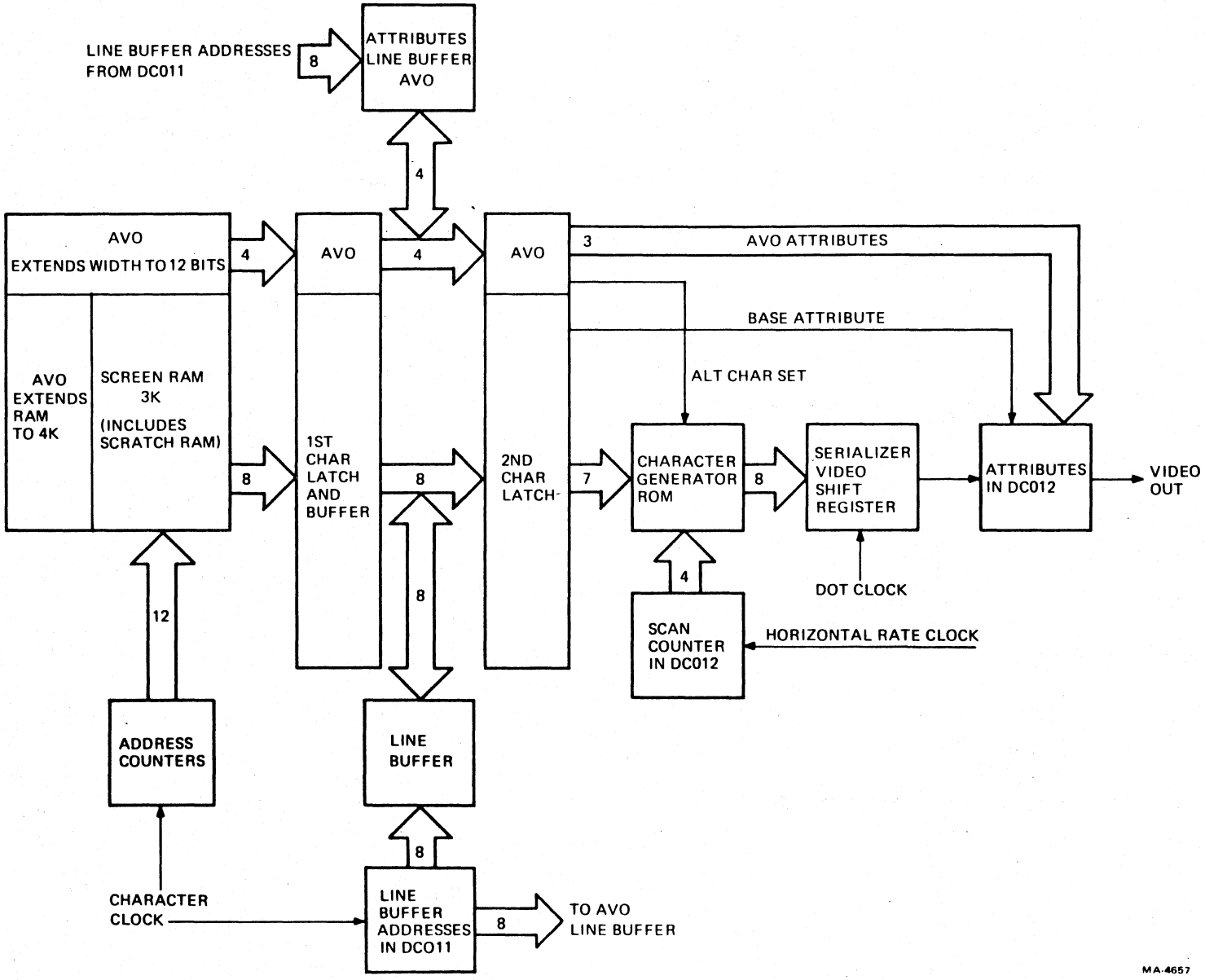


Figure 4-6-3 Video Processor Functional Diagram

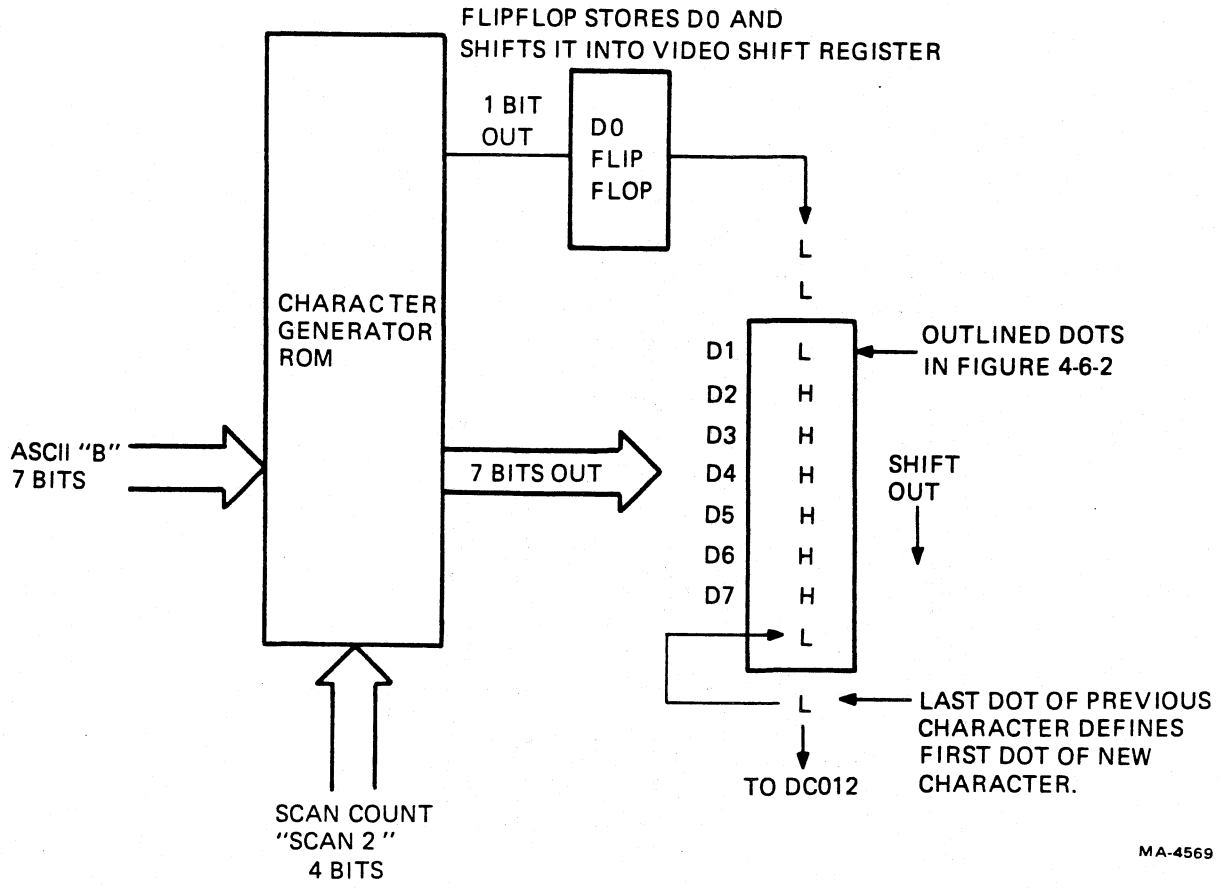


Figure 4-6-4 Character Generator Example

Line attributes are double height, double width, and scroll. The VT100 displays single-width, double-width or double-height, double-width characters on a line by line basis. All characters on one line appear in the same mode. Double-width lines are generated by displaying each dot of a character twice in the horizontal direction. Double-height, double-width lines are generated by displaying each dot of a character four times (twice horizontally and twice vertically). The top and bottom halves of a double-height, double-width line must be entered as two separate lines of characters. The scroll attribute indicates that a line is part of the scrolling region.

Screen attributes affect the entire screen's characteristics at once. They include the base attribute selection (reverse or underline as mentioned under character attributes), reverse video over the entire screen, 80 or 132 character line length, 50 or 60 Hz refresh rate (chosen according to the local power supply), interlaced or noninterlaced operation, and jump or smooth scrolling of data over the screen.

4.6.1.6 Advanced Video Option (AVO) – The AVO extends the length of the screen RAM so more characters can be displayed in 132 column mode. In addition, it allows each character to have four more attributes, for a total of five. Three of the AVO attribute bits enter the DC012 to control displayable features of each character. The fourth AVO attribute bit controls the selection of an extra character set by switching in an optional alternate character generator ROM that can provide non-ASCII characters or other special displays.

To provide the extra attribute bits, the AVO widens the entire screen RAM by 4 bits to make each character location 12 bits wide. It also contains a 4-bit wide extension of the character latches and a 4-bit wide attribute line buffer, addressed by the same LBA signals as the regular line buffer. This extension treats the attribute data with the same timing as the character part of the circuit, and matches each character with its attributes.

With the AVO present, reverse video, underline, bold, and blinking are all available singly or in combination. Reverse and underline appear as described above with the addition that if both reverse and underline are asserted, the underscore is forced dark instead of light. Bold increases the intensity of the display. The blink rate is about half that of the cursor or about 0.5 Hz. Cursor selection is independent of character attributes when the AVO is installed.

4.6.2 Timing Chip Description

The DC011 is a custom designed bipolar integrated circuit that provides most of the timing signals required by the video processor. Internal counters divide the output of a 24.0734 MHz oscillator (located elsewhere on the terminal controller module) into the lower frequencies that define dot, character, scan, and frame timing. The counters are programmable through various input pins to control the number of characters per line, the frequency at which the screen is refreshed, and whether the display is interlaced or noninterlaced. These parameters can be controlled through SET-UP mode or by the host. In the following discussion, refer to the block diagram in Figure 4-6-5.

4.6.2.1 Input Decoder – The input decoder responds to commands on the D0 H and D1 H pins (connected to D4 and D5 of the 8080 bus respectively) whenever the VIDEO WR 1 L pin is low. The outputs of the decoder select 80/132 column, 60/50 hertz refresh, and interlaced/noninterlaced modes of operation. Table 4-6-1 shows that when D1 H is low the number of columns is programmed according to the state of D0 H, and when D1 H is high the refresh rate is programmed. Interlaced mode is always selected when the column mode is set, and noninterlaced mode is selected when the refresh rate is set. The interlace mode in use depends on whether "number of columns" or "refresh rate" was selected last.

Table 4-6-1 Video Mode Selection
(Write Address = C2H)

Inputs			
D5 Pin 21	**D4 Pin 20**	**Configuration**	
0	0	80 column mode	Sets interlaced mode
0	1	132 column mode	
1	0	60 hertz mode	Sets noninterlaced mode
1	1	50 hertz mode	

In addition to strobing data into the input decoder, VID WR 1 L also acts as a reset signal for the DC011. Whenever VID WR 1 L is low, the counters in the DC011 are held in a cleared state. Resetting the counters serves no purpose in the VT100 because the remainder of the VT100 synchronizes itself to the DC011, but a reset is useful for testing both individual chips and complete modules. Because writing into the DC011 would cause the counters to reset and disturb the display, this is never done unless the mode is being changed.

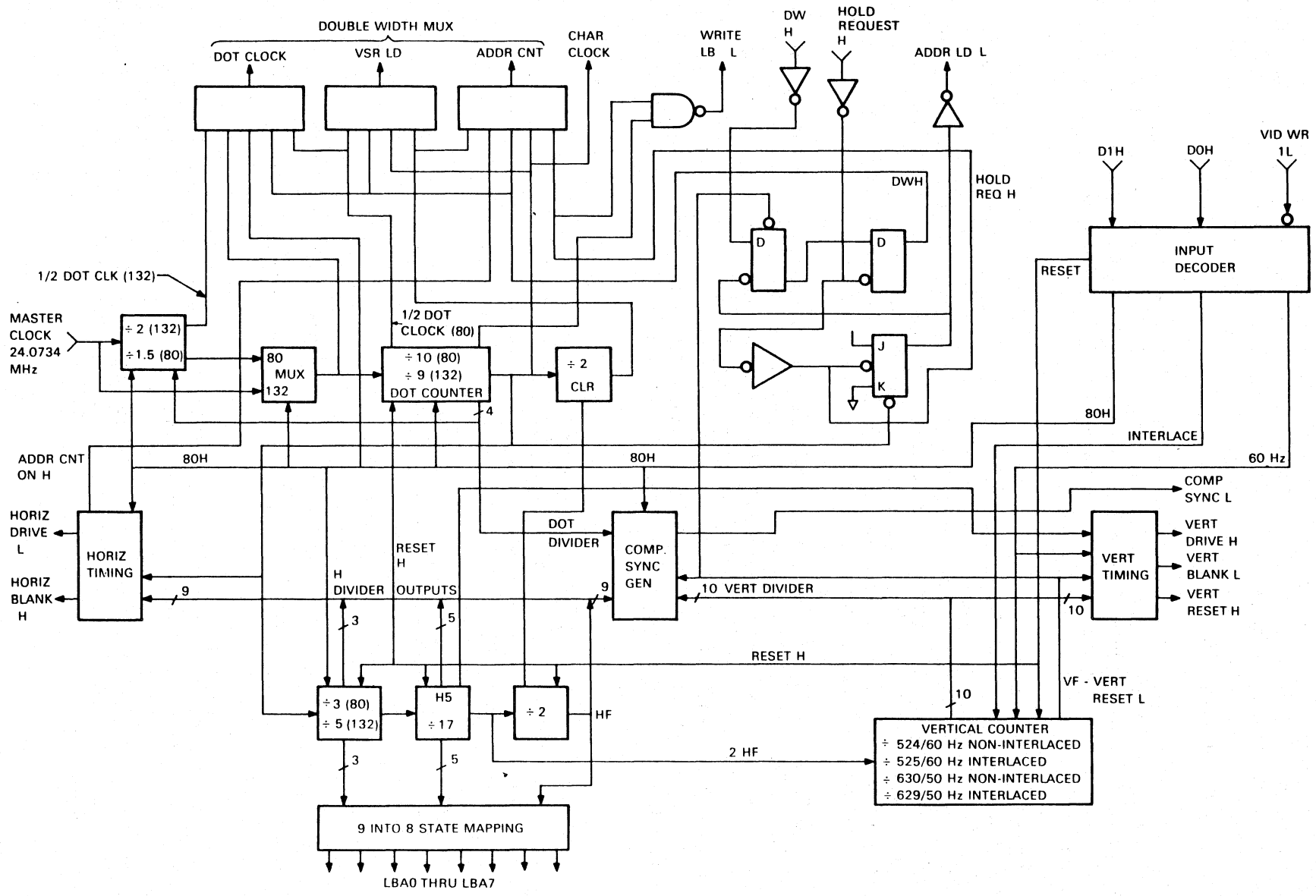


Figure 4-6-5 DC011 Block Diagram

4.6.2.2 80/132 Column Selection – The column mode is changed by modifying the divisors of three of the counters in the DC011. The first of these counters divides the input clock (MASTER CLK) by 1.5 to produce the dot rate clock for 80 column mode. The DOT CLK output provides the signal that controls the shifting of dots out from the video shift register. A multiplexer determines what rate DOT CLK will have for the entire screen by selecting either the output of the divide-by-1.5 in 80 column mode, or by selecting the 24 MHz MASTER CLK directly in 132 column mode. The other two counters affected by 80/132 selection are the dot counter and the horizontal counter.

4.6.2.3 Dot Counter – The dot counter uses four flip-flops to divide the DOT CLK that was selected by the multiplexer by 10, in 80 column mode, or by 9, in 132 column mode. The output of the dot counter is the character rate clock, which is used to move character codes in the latches that are outside the DC011. Character clock is further divided by the horizontal counter. The timing of CHAR CLK is shown in Figures 4-6-6 and 4-6-7 for each of the two column modes. CHAR CLK is unaffected by double-width mode. The output of the next-to-last flip-flop is used for the write enable signal for the line buffer RAMs (WRITE LB L). WRITE LB L is also shown in Figures 4-6-6 and 4-6-7. This signal allows the data and address changes, caused by the rising edge of CHAR CLK, to become stable before writing is enabled and then disables writing before CHAR CLK rises again. WRITE LB L is gated directly with HOLD REQ H so that it is active only during DMAs. Intermediate signals from the four flip-flops are used by various other functions in the DC011 such as the double-width multiplexer and the composite sync generator.

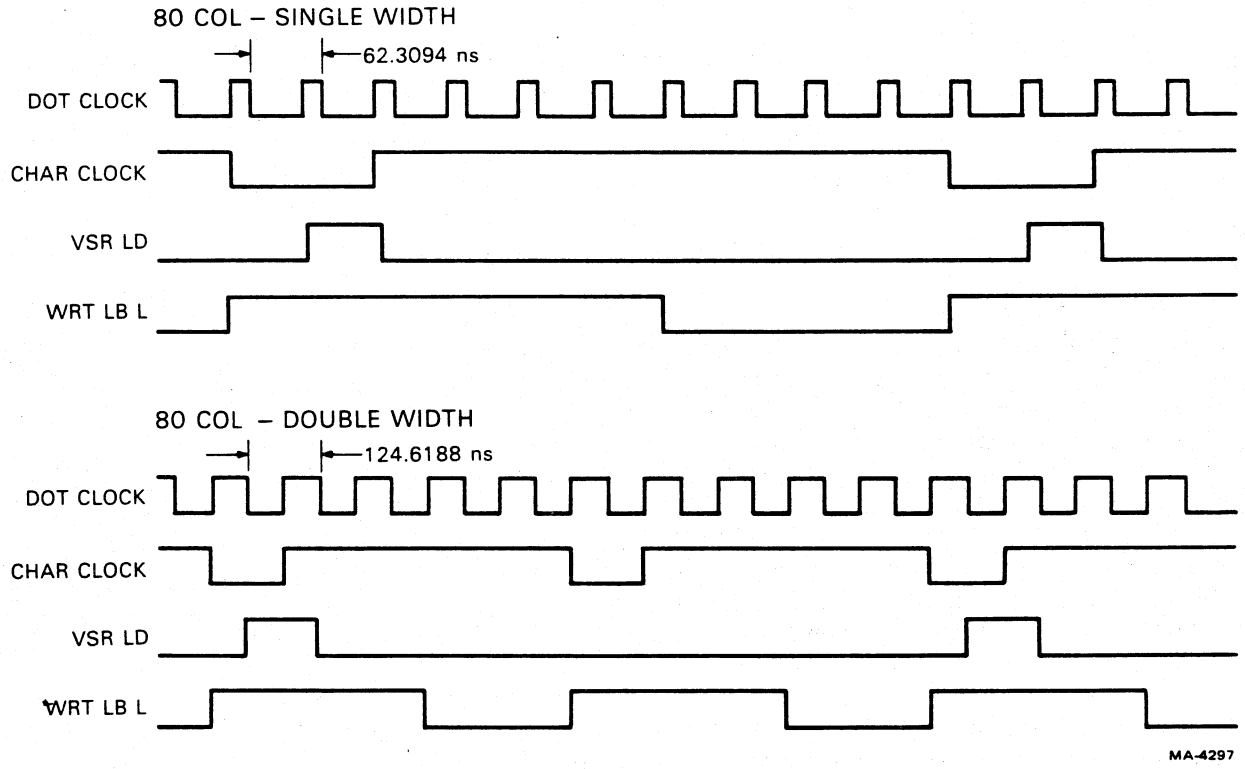


Figure 4-6-6 Video Latch Timing – 80 Column

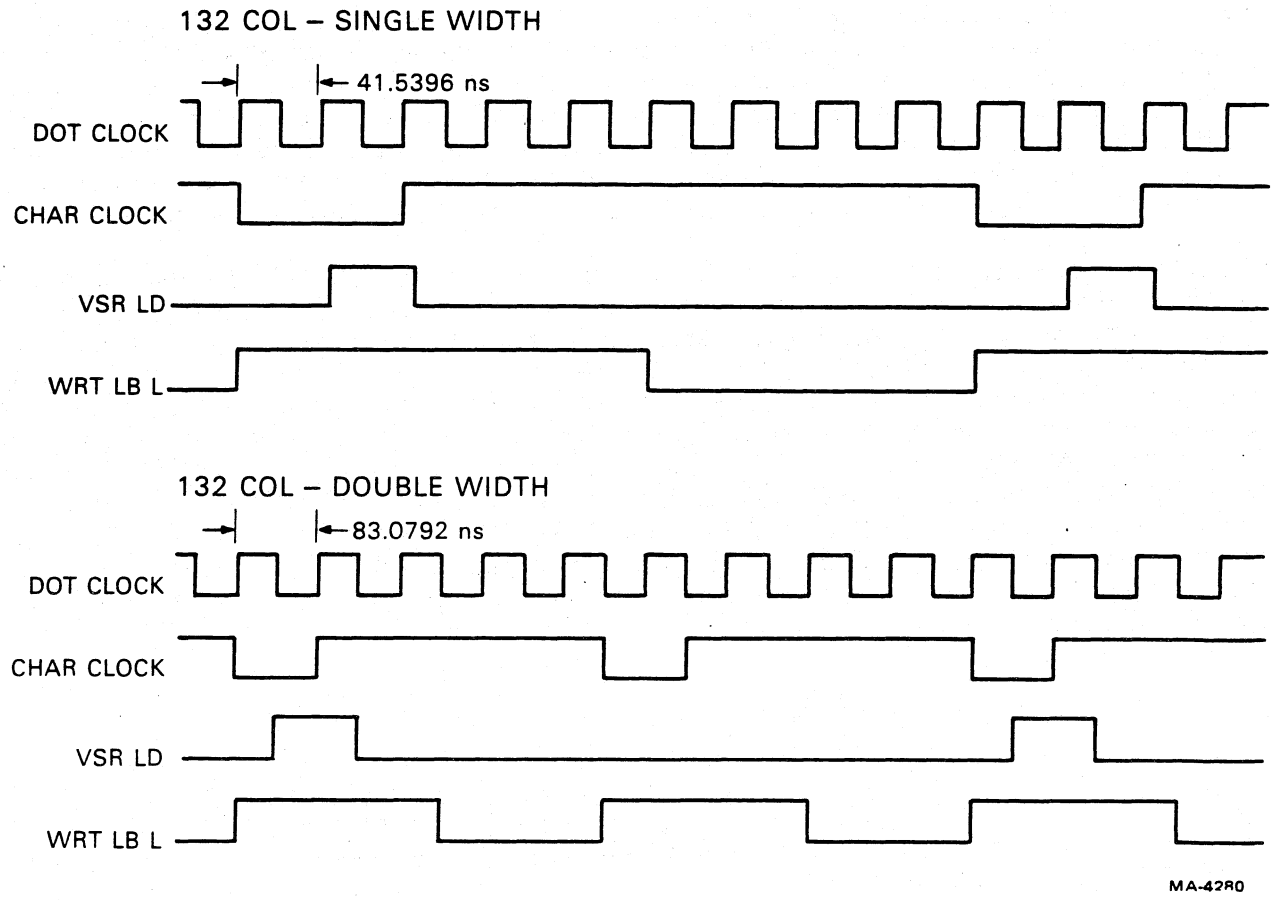


Figure 4-6-7 Video Latch Timing – 132 Column

4.6.2.4 Double-Width Multiplexer – The double-width multiplexer (MUX) produces the three signals whose timing must be changed when a line of characters is switched between single- and double-width modes. The frequency of DOT CLK must be divided in half on a double-width line so that the video shift register will shift half as often, making each dot (and therefore each character) twice as wide as it would be in single-width mode. In order for the video shift register to work properly with the half-rate DOT CLK in double-width mode, the load signal for the shift register (VSR LD H) must still come every 10 dots (80 column mode) or 9 dots (132 column mode). Therefore loads must occur at every other CHAR CLK. Similarly, incrementing the DMA address counters occurs on every other CHAR CLK to ensure that characters that are stored sequentially in the screen RAM are presented to the shift register at the correct time for each VSR LD H pulse. The different modes of DOT CLK and VSR LD H are shown in Figures 4-6-6 and 4-6-7.

In single-width mode, the double-width MUX directs the output of the 80/132 MUX to the DOT CLK pin, providing either a 16 MHz or 24 MHz output. To get the half-rate DOT CLK for 80 column mode, the double-width MUX selects the output of the first flip-flop in the dot counter, that acts as a divide-by-2 because the dot counter is dividing by 10 (10 is an even number). In 132 column mode the same selection cannot be made because the dot counter is dividing by 9. But the divide-by-1.5 is not needed in 132 column mode, so this divider is converted to a divide-by-2 and the double-width MUX selects its output when a double-width line is displayed in 132 column mode.

The load input of the video shift register used in the VT100 is a synchronous input. This means that when the load input is high, the rising edge of DOT CLK causes a parallel load to be performed instead of a shift. To get one load and many shifts for each character, VSR LD H can only last for that one cycle of DOT CLK that is adjacent to CHAR CLK. Furthermore, transitions of VSR LD H must satisfy SET-UP and hold times with respect to the rising edge of DOT CLK. In single-width modes, VSR LD H is one dot time wide, generated from the outputs of the dot counter, and its SET-UP and hold times are guaranteed by internal propagation delays. This relationship is shown in Figures 4-6-6 and 4-6-7 by a slight shift in the transitions of VSR LD H with respect to DOT CLK. In double-width mode, VSR LD H is created by selecting every other CHAR CLK (Figure 4-6-5 shows a flip-flop that divides CHAR CLK by two for this purpose) and then delaying this signal by one single-width dot time.

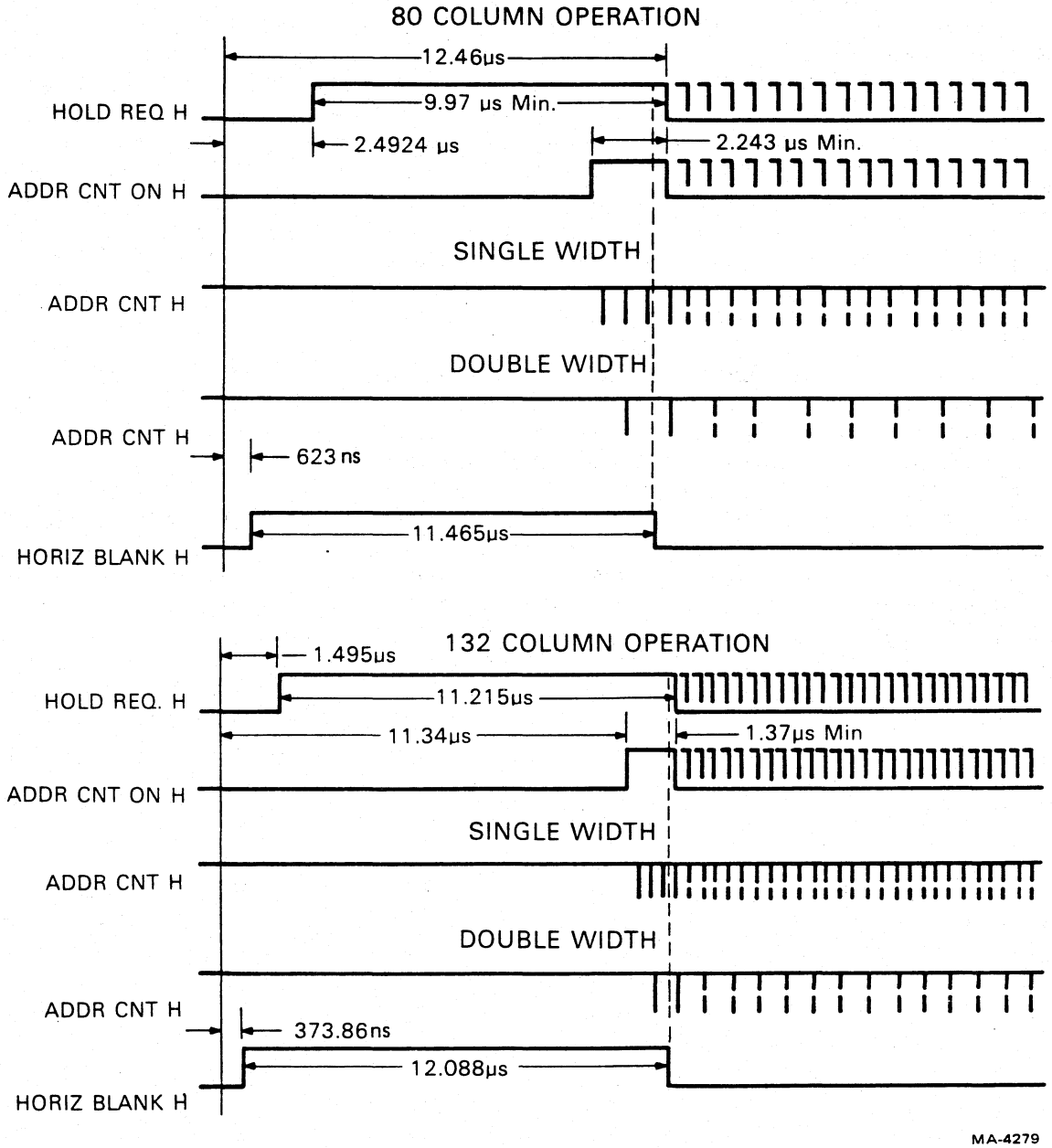


Figure 4-6-8 Address Count Timing

The signal that increments the DMA address counter (ADDR CNT) is shown in Figure 4-6-8. ADDR CNT has the same timing as CHAR CLK; the difference is that it does not run continuously. Figure 4-6-8 shows that ADDR CNT can only be generated if HOLD REQUEST H is high and that it is further controlled by a signal from the horizontal timing section (ADDR CNT ON H) that allows ADDR CNT to provide exactly three pulses (in single-width mode) before HORIZ BLANK H goes low. The three pulse delay primes the external character latches so that the dots for the first character on a line are being loaded into the video shift register at the same moment that HORIZ BLANK H enables the video at the beginning of a scan. The only change made to ADDR CNT for double-width operation is that every other pulse is deleted, beginning with the first pulse (Figure 4-6-8).

4.6.2.5 Horizontal Counter – The block diagram in Figure 4-6-5 shows the horizontal divider broken into three stages. The first divider is programmable according to the number of columns selected and is driven by CHAR CLK from the dot counter. For 80 column mode the divisor is three; for 132 column mode the divisor is five. The total division from MASTER CLK to the output of this first divider is 45, independent of mode (for 80 columns: $1.5 \times 10 \times 3 = 45$, for 132 columns: $1 \times 9 \times 5 = 45$). Therefore, the operation of all of the remaining dividers in the DC011, which are driven from the first horizontal counter, are also independent of the column mode. The second stage of the horizontal divider has a divisor of 17, which is chosen to give the required number of displayable columns plus about 28 percent more to allow time for the monitor to execute a horizontal retrace. The last stage is a simple divide-by-2 that provides the horizontal frequency. Designing the last stage to be a divide-by-2 guarantees that the signal at its input will have a frequency twice that of the horizontal frequency as required by the vertical dividers to create interlaced operation. The total division from CHAR CLK provided by the horizontal divider is 102 in 80 column mode and 170 in 132 column mode. In either mode the frequency at the output of the horizontal counter is 15.734 kHz.

4.6.2.6 Horizontal Drive and Horizontal Blank – Two timing signals are generated from the horizontal counter to control those system functions occurring at the scan rate. These signals begin at the end of a scan and last until the horizontal counter is incremented past a specific state that is decoded to turn the signals off. The monitor requires a pulse at the end of every scan to tell it when to initiate a retrace and begin the next scan; the duration of this pulse must be between approximately one-quarter and one-half of one scan. Figure 4-6-9 shows HORIZ DRIVE L as produced by the DC011; the slight difference in timing between 80 and 132 column modes is the result of design convenience and is not significant to the operation of the VT100. HORIZ BLANK H is designed to allow 83 characters during the forward scan in 80 column mode and 137 characters in 132 column mode. The extra characters are included for possible future use such as a field of indicators along the right margin of the screen or as extra symbols inserted to mark text. The rising edge of HORIZ BLANK H is synchronized to CHAR CLK to eliminate the accumulated delay of the horizontal counter. The falling edge of HORIZ BLANK H occurs between two CHAR CLKs (Figure 4-6-8) to meet some requirements of the DC012, but inside the DC012 HORIZ BLANK H is delayed to the following edge of CHAR CLK so that the beginning of each displayed scan will coincide with a character boundary. The actual video blanking occurs inside the DC012. Therefore there is no signal outside the DC012 that has the exact length of horizontal blank time.

4.6.2.7 Line Buffer Addressing – The line buffer memory stores one line of characters during a scan on which a DMA occurs and then recalls these characters on each successive scan until the next DMA. Because the line buffer is a random access memory, it has address inputs that must be provided with a sequence of addresses that change at each CHAR CLK such that each character is stored in a unique location. The horizontal counter can provide such addresses because it is incremented through a series of unique states that repeat in the same sequence on every scan. Because of the three stages that comprise the horizontal counter, there are nine flip-flops whose outputs must be converted into the eight line buffer address (LBAs) outputs. The conversion is possible because the 9 flip-flops represent a maximum of 170 states in 132 column mode (8 bits can represent 256 states). The DC011 contains gates that combine the output of the ninth flip-flop in the horizontal counter with the outputs of the other

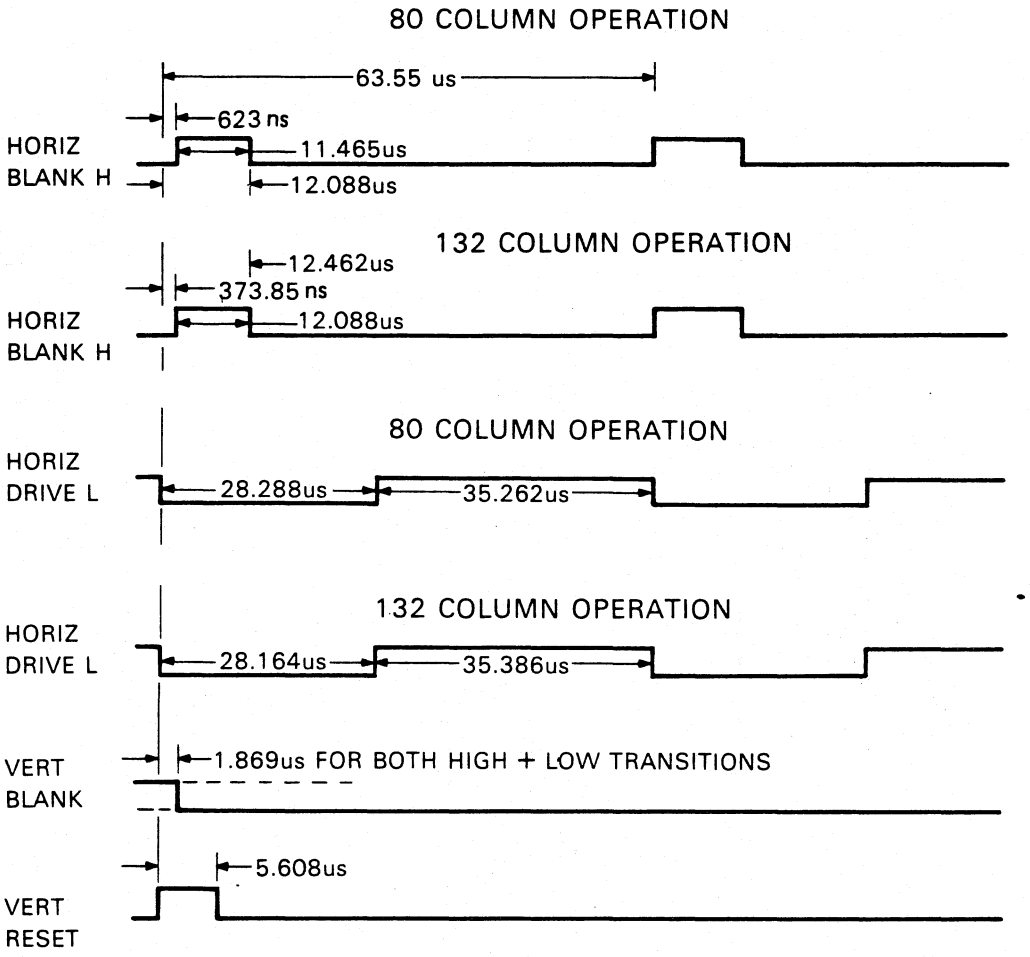


Figure 4-6-9 Horizontal Timing

eight to generate some addresses that are not otherwise represented by the eight. The resulting LBAs do not follow a normal binary counting sequence but the sequence of unique addresses repeats exactly on each scan. Figures 4-6-10 and 4-6-11 show the LBA sequence for one-half of a scan; the other half is identical except that LBA 7 is low.

Several of the LBAs are used as general purpose clocks in the VT100. LBA 3 and LBA 4 are used to generate timing for the keyboard. These signals satisfy the keyboard's requirement of two square-waves, one twice the frequency of the other, even though every 16th transition is delayed (the second stage of the horizontal counter divides by 17, not 16). LBA 7 is used by the nonvolatile RAM. The 31.468 kHz signal on LBA 6 could be used for power supply synchronization, although this is not done in the VT100.

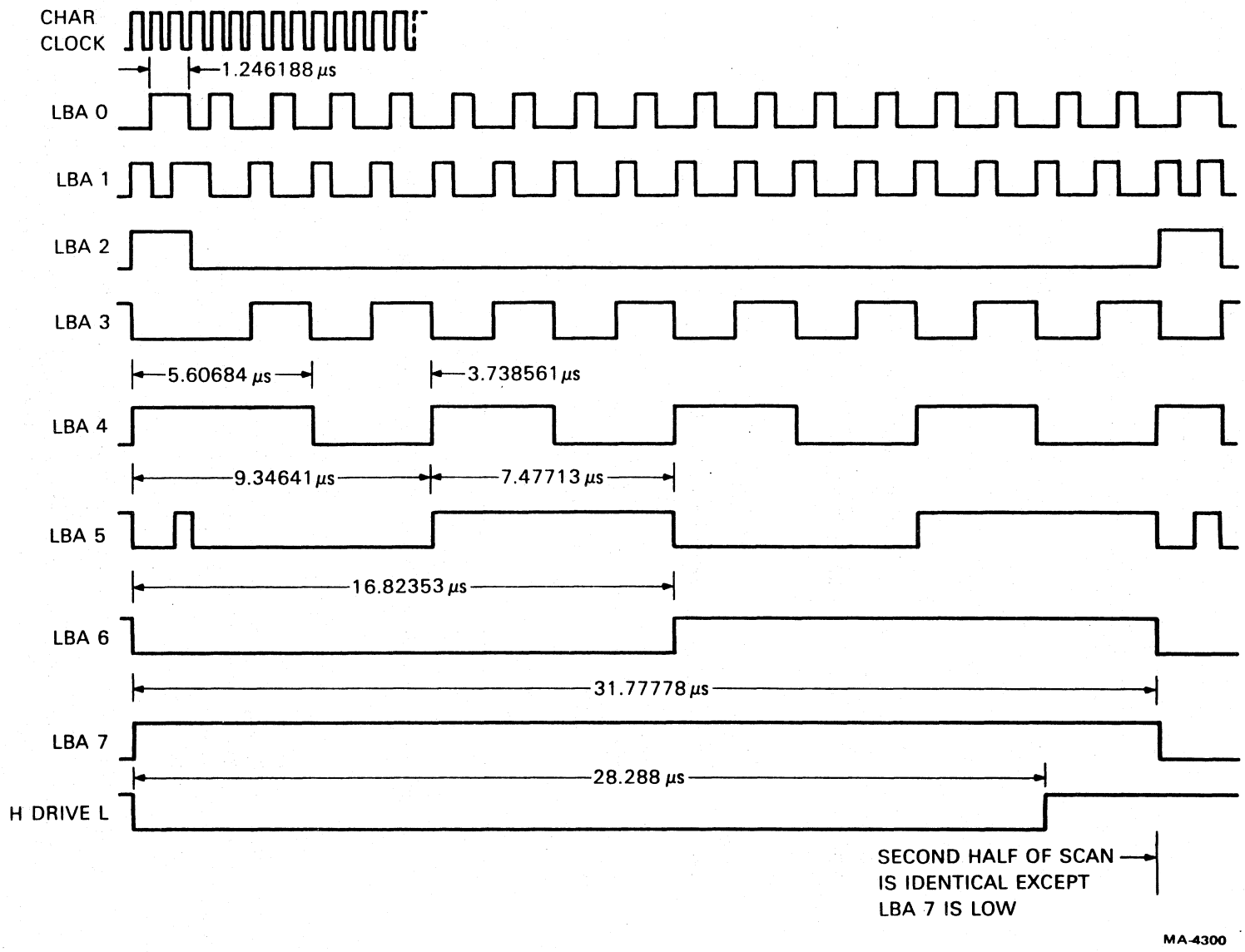


Figure 4-6-10 Line Buffer Address Outputs – 80 Column

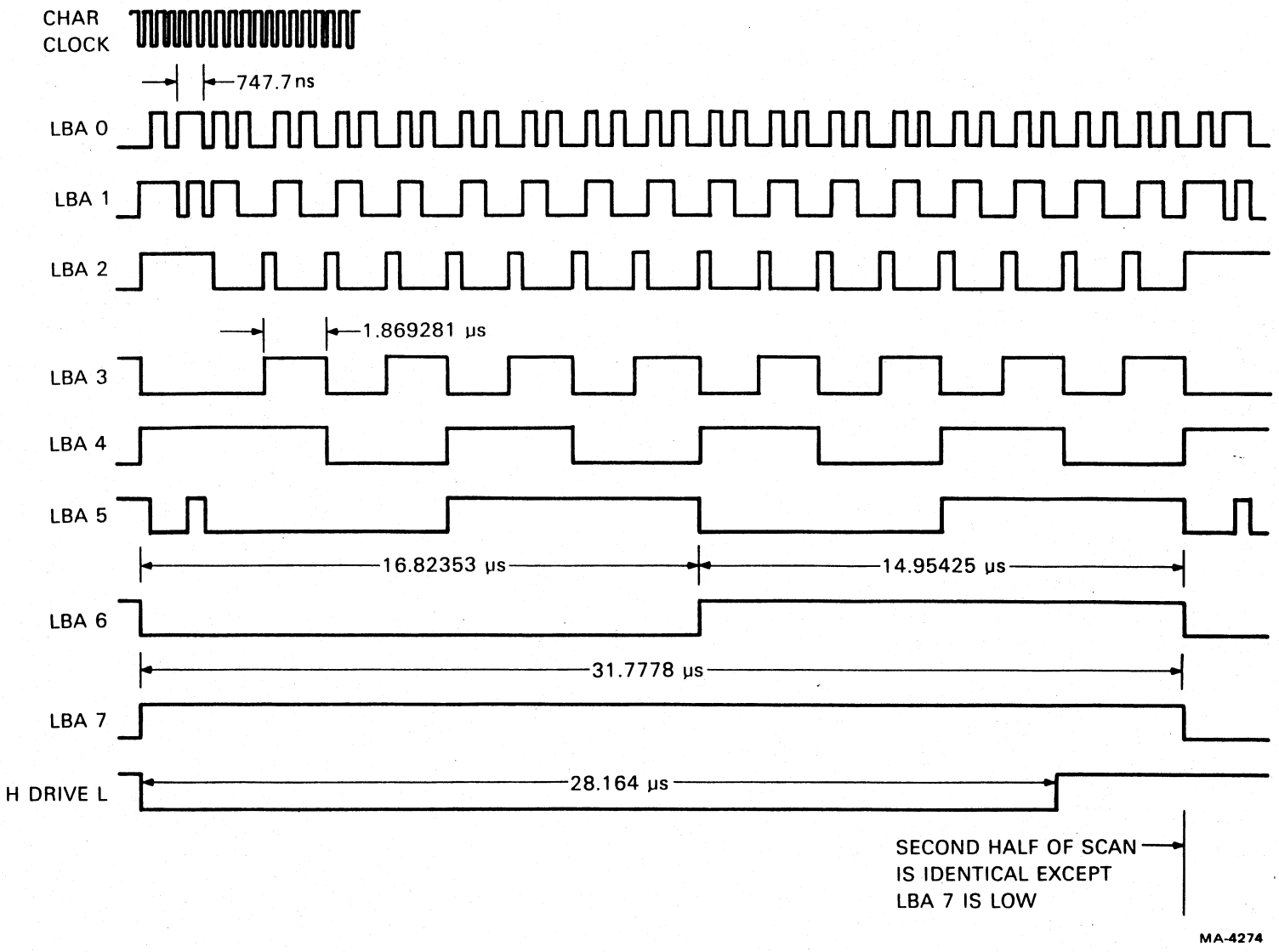


Figure 4-6-11 Line Buffer Address Outputs – 132 Column

4.6.2.8 Vertical Operation – To paint a complete picture on the screen, the monitor moves the electron beam slowly from the top of the screen to the bottom, while it is also moving the beam quickly from left to right to paint each scan. The vertical sweeps of the beam must be repeated continuously so that the picture is refreshed often enough to prevent the appearance of flicker. In television terminology, a single pass of the beam from the top of the screen to the bottom (and the data displayed during that time) are referred to as one field. A complete picture, which may contain one or more fields depending on the type of interlacing in use, is called one frame. When the VT100 is used in noninterlaced mode, each successive field is identical and therefore only one field is contained in each frame. During interlaced operation in the VT100, there are two types of fields that alternate with each other so that each frame consists of two fields. Even fields start at the top of the screen and display 240 scan lines before reaching the bottom. Odd fields place their first scan line between the first and second scans of the preceding even field and then place each additional scan between succeeding scans of the even field. Interlacing the even and odd fields gives a whole frame of 480 scans, instead of 240 scans, to provide increased vertical resolution. In noninterlaced operation, commands to the monitor to begin a new field are always coincident with commands to begin a new scan. This causes the beam to always be in the same vertical position when the first displayed scan is begun. But, in interlaced mode, odd fields begin with a command for a new frame that occurs halfway through a scan line. This causes the beam to have moved down the screen from where it would have been during an even field (by the distance that it moves in one-half of a scan) when the first displayed scan is begun. Even and odd fields are made to alternate by including an odd number of half-scans in every field. This is in contrast to noninterlaced operation, where each field contains only complete scans. The VT100 always displays the same video information on both even and odd fields. Interlaced mode is provided for future use by options that desire increased vertical resolution.

4.6.2.9 Vertical Counter – The 10-bit vertical counter, shown in Figure 4-6-5, determines the frequency at which the screen is refreshed by counting the number of horizontal scans to be included in each field. The vertical counter uses the 31.468 kHz output of the horizontal counter so that it can count the half-scans required for interlaced operation. Figure 4-6-5 lists the four available divisors that select the interlace mode and keep the refresh frequency as close to the local power line frequency as possible (to minimize interference with the screen from nearby equipment). The vertical frequencies produced by these divisors are approximately 1/20 Hz above or below the nominal power line frequency.

4.6.2.10 Vertical Outputs – Three outputs are derived from the flip-flops in the vertical counter to control the vertical refresh operations in the VT100. These signals are shown in Figures 4-6-12 and 4-6-13 for all four modes. VERT DRIVE H is issued at the bottom of the screen to initiate a vertical retrace followed by a new vertical scan. This operation is analogous to the effect of HORIZ DRIVE L on horizontal scans. The time between any two VERT DRIVE Hs is a constant, equal to an even number of half-scans in noninterlaced mode and equal to an odd number of half-scans in interlaced mode. VERT BLANK L always enables exactly 240 scans during any field and blanks any remaining scans. Furthermore, VERT BLANK L is always turned off exactly 20 scans after VERT RESET H in 60 Hz mode and 50 scans after VERT RESET H in 50 Hz mode. VERT BLANK L is always adjusted to display complete scans even during odd fields in interlaced mode. VERT RESET H initiates the DMA process at the start of every field. When VERT RESET H goes high, the DMA address counters are reset to point to address 2000H in the screen RAM, all line attributes are cleared, and the scroll counter in the DC012 is preset to the value stored in the scroll latch. (See the DC012 description for more explanation.) During noninterlaced operation and on even fields, VERT RESET H occurs at the same time as VERT DRIVE H; but, on odd fields VERT RESET H is delayed one-half of a scan to match the start of a horizontal scan. The relationship of VERT RESET H and transitions of VERT BLANK L to HORIZ BLANK H and HORIZ DRIVE L is depicted in Figure 4-6-9. Notice that VERT BLANK L always turns on or off when the video is already blanked by HORIZ BLANK H.

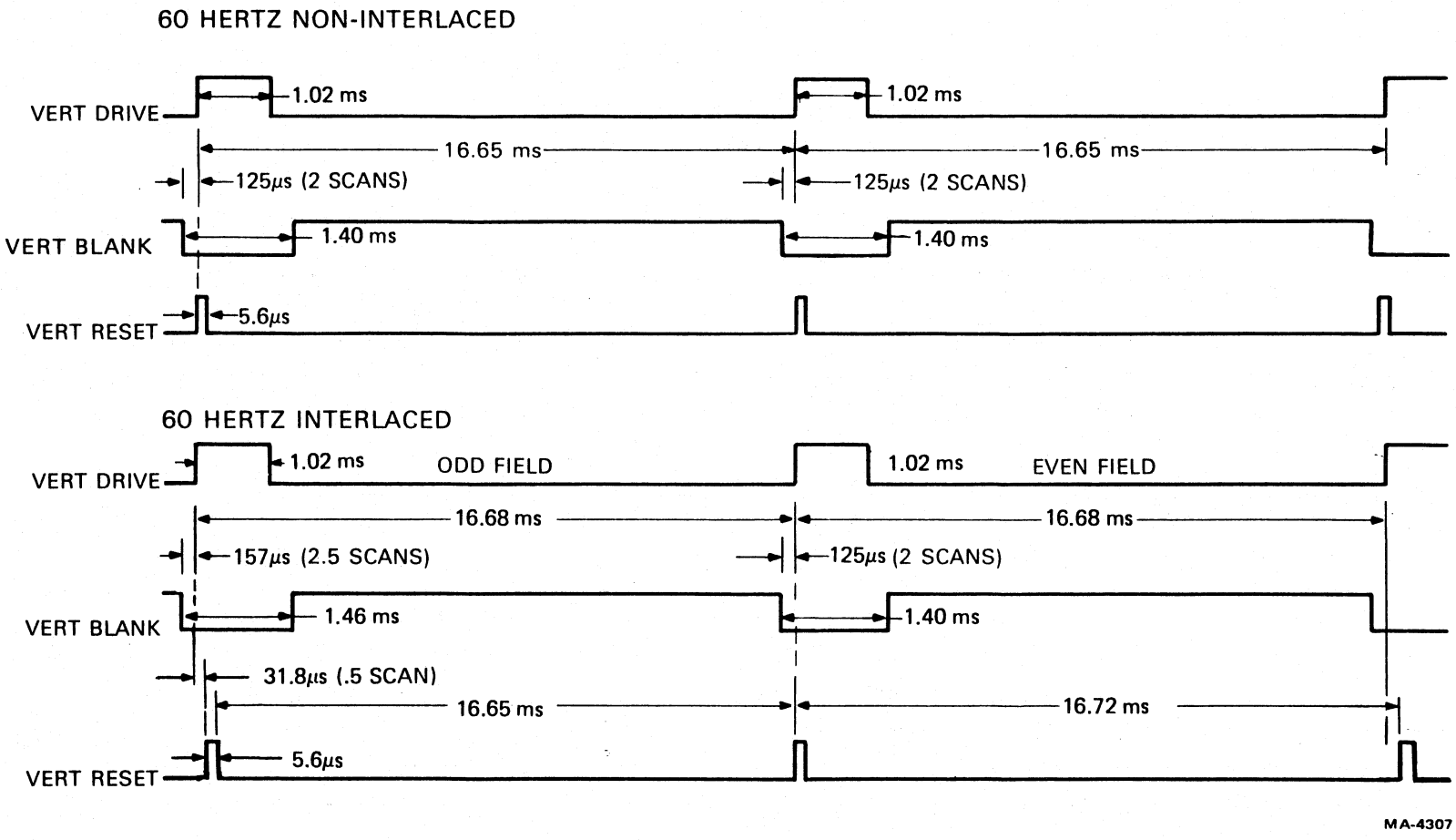


Figure 4-6-12 Vertical Signals – 60 Hz

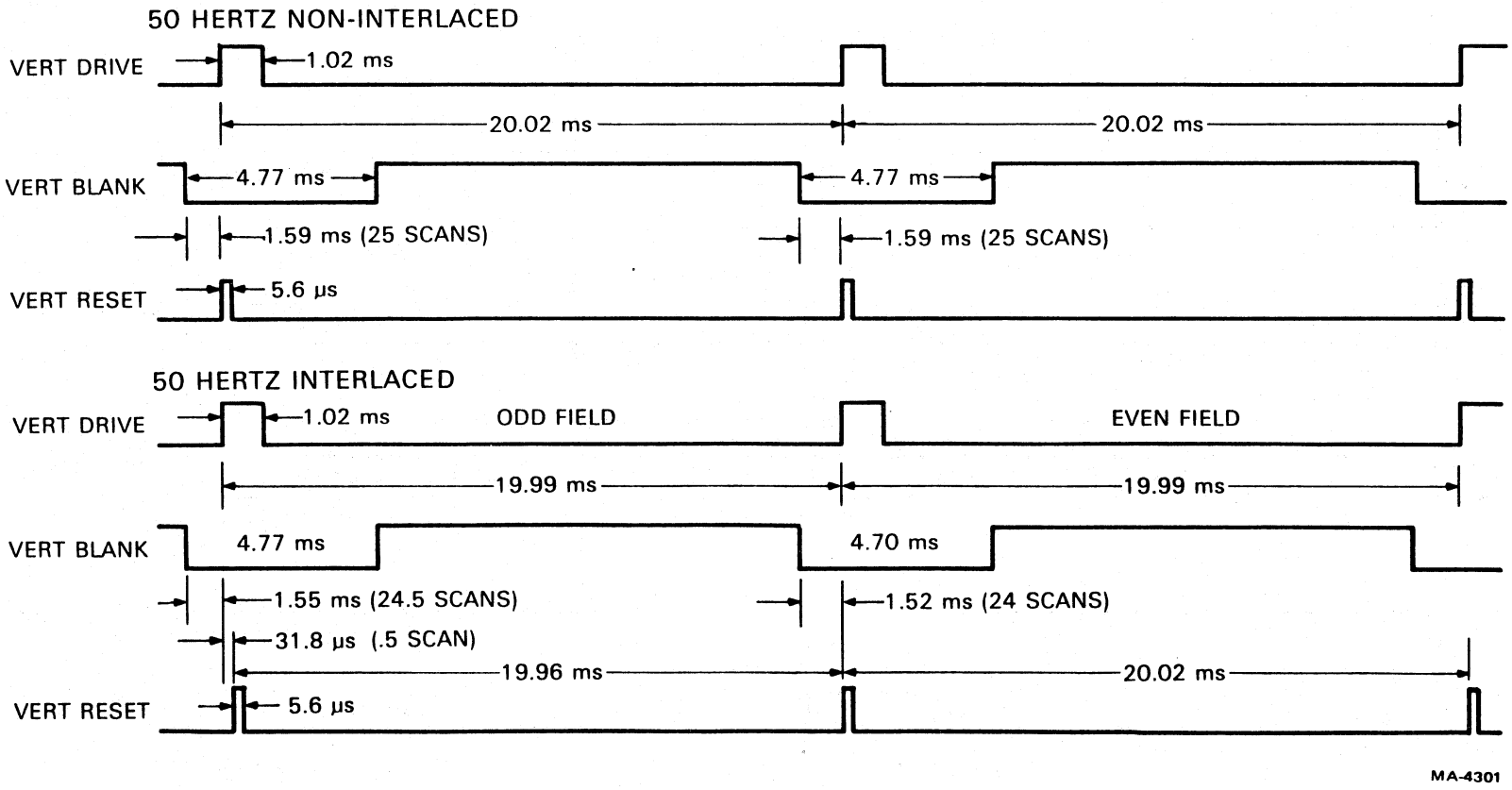


Figure 4-6-13 Vertical Signals – 50 Hz

4.6.2.11 Composite Sync – The COMP SYNC L signal supplied by the DC011 is combined with video information by the terminal controller board to produce the composite video signal that appears on J9 at the back of the VT100. An external monitor can use the composite video signal to reproduce the image displayed on the VT100 screen. This is accomplished by using the video information to control beam intensity and the composite sync waveform to synchronize the raster to the video information. The composite sync generator in the DC011 uses outputs from the dot, horizontal, and vertical counters to generate the complex timing of COMP SYNC L. COMP SYNC L consists of one of the vertical intervals depicted in Figure 4-6-14 followed by 240 horizontal sync pulses, another vertical interval, etc. The vertical synchronizing interval consists of a transition from horizontal sync pulses to six equalizing pulses, six vertical sync pulses, six more equalizing pulses, and then a return to horizontal sync pulses. Two vertical intervals are shown in Figure 4-6-14. The vertical interval that begins an odd field is similar to that which begins an even field except that the equalization and vertical sync pulses are shifted by one-half scan with respect to the horizontal sync pulses. In noninterlaced mode all fields are even fields; but, in interlaced mode every other field is an odd field. Figure 4-6-14 also shows the relationship of COMP SYNC L to both the horizontal blank time (HORIZ BLANK H modified by the DC012) and VERT BLANK L. COMP SYNC L meets the requirements of EIA RS-170 and the NTSC standards for sync pulse generators.

4.6.2.12 Hold Request, Address Load, and Double-Width – The logic associated with HOLD REQ H, ADDR LD L, and DW H is shown in Figure 4-6-5. The falling edge of HOLD REQ H sets ADDR LD L to the low state; ADDR LD L is subsequently cleared by the falling edge of CHAR CLK, thus creating a short low pulse on ADDR LD L at the end of each DMA. ADDR LD L stores, in their respective registers, all line attributes and the memory address of the next line to be accessed by a DMA. The rising edge of HOLD REQ H causes the value of DW H that was stored in the holding flip-flop by the previous ADDR LD L to be transferred to a second flip-flop whose output controls the double-width MUX. This means that the value of DW H stored at the end of one DMA by ADDR LD L does not actually become effective until the beginning of the next DMA. The holding flip-flop for DW H is cleared by VERT RESET H at the start of every field. HOLD REQ H is also used to enable ADDR CNT and WRITE LB L only during DMAs. Interactions of HOLD REQ H with other signals during a DMA are further defined in Figure 4-6-19.

4.6.3 Control Chip Description

The control chip (DC012), like the timing chip, is a custom bipolar device. It accepts attribute specifications and timing signals and delivers addresses for the character generator ROM and attributes for the video output to the monitor. It also generates the HOLD REQUEST signal that halts the microprocessor and initiates DMAs to get lines of characters. Refer to the block diagram, Figure 4-6-15.

The DC012 performs three main functions.

1. Scan count generation. This involves two counters, a multiplexer to switch between the counters, double-height logic, scroll and line attribute latches, and various logic controlling switching between the two counters. This is the biggest part of the chip. It includes all scrolling, double-height logic, and feeds into the underline and hold request circuits.

2. Generation of HOLD REQUEST. This uses information from the scan counters and the scrolling logic to decide when to generate HOLD REQUEST.

3. Video modifications: dot stretching, blanking, addition of attributes to video outputs, and multiple intensity levels.

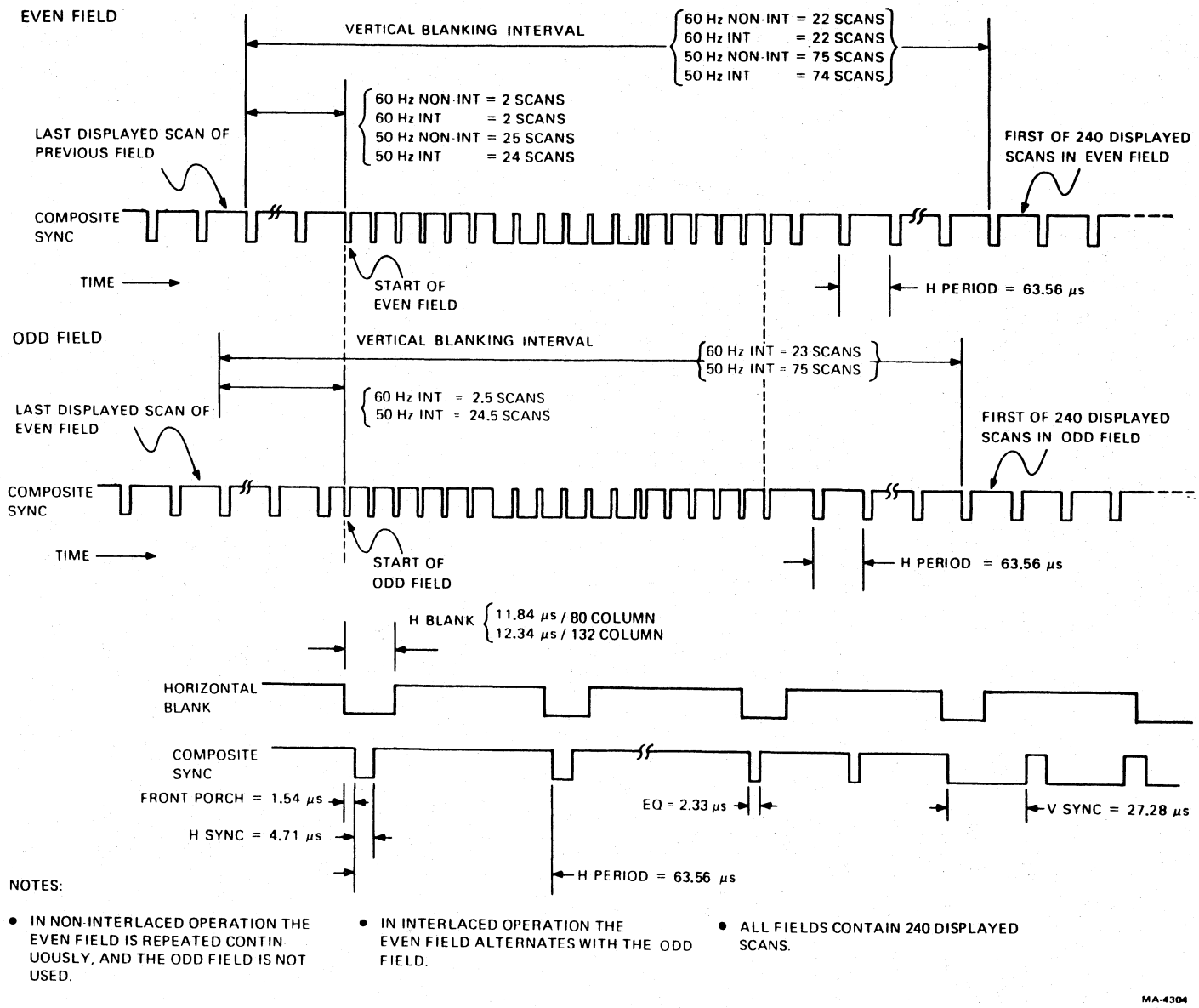


Figure 4-6-14 Composite Sync Output

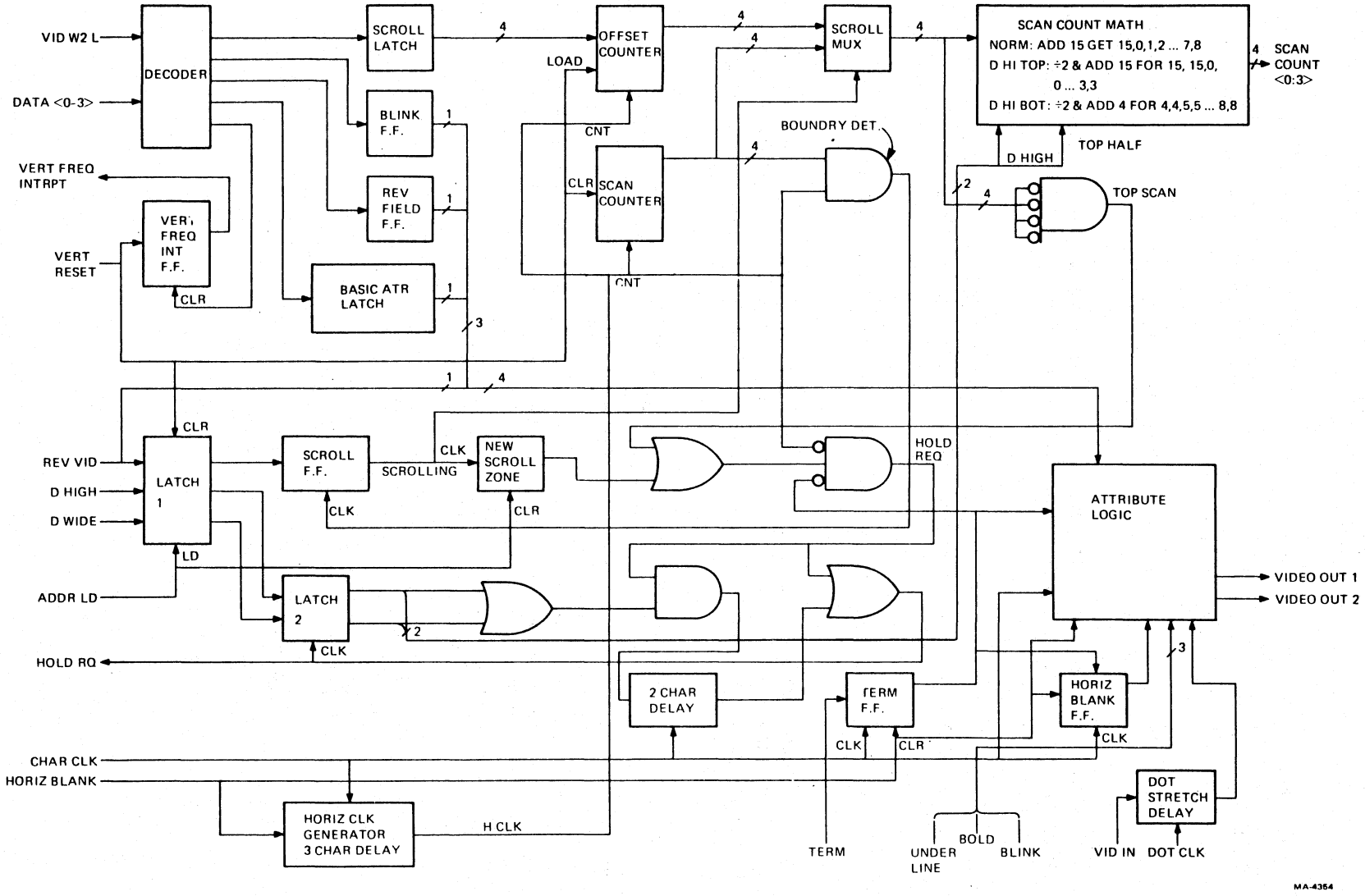


Figure 4-6-15 DC012 Block Diagram

4.6.3.1 Input Decoder Functions – The input decoder accepts a 4-bit command from the microprocessor when VID WR 2 L is asserted. Table 4-6-2 lists the commands.

The low eight values are used to load the scroll latch with the offset for smooth scroll. The scroll latch is loaded in two passes, first writing the two least, and then the two most significant bits. Because the offset is a decimal value controlling 10 display scans, the combination setting the most significant bits to 11B is not used in the VT100 (11B covers the range 12–16).

The input decoder also toggles the blink flip-flop by complementing the state of the flip-flop whenever 1000B is written. The blink flip-flop invokes blink only where the blink attribute is set.

To save external hardware the vertical frequency interrupt flip-flop is located in the DC012 because a spare pin was available. It is set by the falling edge of Vertical Reset. It is cleared by writing 1001B into the input decoder.

Set and clear of reverse field are not toggled because the absolute state is important and there is no feedback for the system to detect the current state. Therefore, the two states are explicitly set to their desired values.

1100B means set base attribute to underline and 1101B means set base attribute to reverse video. 1110B and 1111B are for future specification.

Any time the input decoder is loaded with 11XXB, the blink flip-flop gets cleared. This is the only way to initialize blink in the chip testing process. The firmware does not currently use the ability to clear the blink flip-flop but if hardcopy output was being implemented, it could be used to set the blink to a known state during a freeze.

Table 4-6-2 Control Chip Commands
(Write Address = A2H)

D3	D2	D1	D0	Function
0	0	0	0	Load low order scroll latch = 00
0	0	0	1	Load low order scroll latch = 01
0	0	1	0	Load low order scroll latch = 10
0	0	1	1	Load low order scroll latch = 11
0	1	0	0	Load high order scroll latch = 00
0	1	0	1	Load high order scroll latch = 01
0	1	1	0	Load high order scroll latch = 10
0	1	1	1	Load high order scroll latch = 11 (not used)
1	0	0	0	Toggle blink flip-flop
1	0	0	1	Clear vertical frequency interrupt
1	0	1	0	Set reverse field on
1	0	1	1	Set reverse field off
1	1	0	0	Set basic attribute to underline*
1	1	0	1	Set basic attribute to reverse video*
1	1	1	0	Reserved for future specification*
1	1	1	1	Reserved for future specification*

*These functions also clear blink flip-flop.

4.6.3.2 Attribute Latches – The line attributes are managed by two latches that store the scrolling, double height (DH), and double width (DW) bits. The first latch stores the incoming data when Address Load (ADDR LD) goes low at the end of a DMA. Scrolling means that the next line will be part of the scrolling region, DH means the next line will be double height, and DW specifies top or bottom half for double-height lines. There is no double height, single width combination, so in double height, double width is assumed. The DW pin also tells the DC012 to extend HOLD REQUEST during double width. The second set of latches for double width and double height are clocked by the rising edge of HOLD REQUEST (similar to the second latch for double width in the DC011) to invoke the attributes at the beginning of the new line. The first latch stores those attributes from the end of one DMA to the beginning of the next. It is the outputs of the second latch that invoke attributes in the chip. The scroll bit is invoked by a different signal that will be discussed later. The pin defining scrolling is the same pin as reverse video; it means scrolling when loaded in by ADDR LD L and it means reverse video at all other times. The reverse video signal passes from the input pin around the first latch directly to the attribute logic.

4.6.3.3 Scroll Counter – The scroll counter consists of two 4-bit, divide-by-10 counters called the Scan counter and the Offset counter. Both are clocked at the horizontal rate to count scans. The Scan counter is cleared by VERTICAL RESET so that it starts at 0 and counts by 10s down to the end of the screen.

The Offset counter is loaded with the contents of the scroll latch by VERTICAL RESET. The Scroll latch is loaded by the microprocessor and defines the offset between the Scan and Offset counters for an entire frame because the Offset counter is only loaded at vertical reset time. The microprocessor will load the latch with the offset for the next frame during the current frame.

At the beginning of a frame, the two counters divide by 10 but start at different numbers. If not currently scrolling, the offset is 0 and there is no functional difference between the counters. If in the middle of a smooth scroll, the offset will be some other value from 1 to 9. The scan address outputs from the chip to the character generator ROM are either the output of the Offset counter or of the Scan counter, depending on whether the current line is in or out of the scrolling region, respectively. One of the two counters is selected by a 4-bit wide multiplexer (MUX) whose output is the Counter In Use. The MUX is controlled by the scroll flip-flop which is the second latch for the scroll attribute bit. Most line attributes (double height, double width) take effect when HOLD REQUEST goes high for the line in which they are effective. They always take effect with the actual data being displayed. However, the scroll flip-flop can only change state when crossing one of the fixed 10 scan boundaries that are defined by the Scan counter reaching 0.

Each scan when the Scan counter reaches 0 is a scan on the screen where a change can occur from a nonscrolling to a scrolling region, or from a scrolling to a nonscrolling region since this is normally where one line of data changes to the next if the line were not scrolling. This is the only place changes can occur because the bottom of a nonscrolling line of characters is the place for moving into a scrolling region and the top of a nonscrolling line is the place for getting out of a scrolling region. To get into or out of a scrolling region the Scan counter must be at zero. A 4-bit Boundary Detect decoder gate is connected to the outputs of the Scan counter and clocks the scroll flip-flop when all its inputs are zero. If the input to the scroll flip-flop (from the scrolling attribute latch) has been low and goes high at the end of the previous line's DMA, then on 0 (boundary detect), the output of the scroll flip-flop, which is the control line of the MUX, causes the MUX to switch from the Scan to the Offset counter. At the bottom of the scrolling region, the last DMA in the region gets a line from the screen RAM with its scroll attribute not set so when the next 0 boundary is reached, as defined by the Scan counter, the scroll zone is exited. This is because the scroll flip-flop will get a zero input again which will switch the MUX back to the Scan counter right in the middle of the line that was partway through scrolling.

4.6.3.4 Scan Count Math - The scan count output of the scroll MUX goes through combinatorial logic that looks at the double height bit and the top and bottom half bit and decides whether those scan counts need to be modified for double height before going out of the chip. If double height is not asserted, the top and bottom half bit is ignored and the scan is passed through with 1 subtracted in modulo 16 arithmetic. (Thus, 0 becomes 15, 3 becomes 2, 9 becomes 8.) If double height is asserted and top half is asserted, then the operation is to divide the scan count by 2, and continue to subtract 1 after dividing by 2 so the first scan = 15, second scan = 15, third scan = 0. If bottom half is asserted, the operation is to divide by 2 and add 4. This particular arithmetic arrangement was designed for an external component that is no longer needed. Otherwise, dividing by 2 (and adding 5 for bottom half) would be sufficient. Table 4-6-3 shows the scan count sequences for the various modes. The scan count changes on the rising edge of HORIZ BLANK H.

Table 4-6-3 Scan Count Sequence

Normal and Double Width				Double Height Top				Double Height Bottom			
SC3	SC2	SC1	SC0	SC3	SC2	SC1	SC0	SC3	SC2	SC1	SC0
1	1	1	1	1	1	1	1	0	1	0	0
0	0	0	0	1	1	1	1	0	1	0	0
0	0	0	1	0	0	0	0	0	1	0	1
0	0	1	0	0	0	0	0	0	1	0	1
0	0	1	1	0	0	0	1	0	1	1	0
0	1	0	0	0	0	0	1	0	1	1	0
0	1	0	1	0	0	1	0	0	1	1	1
0	1	1	0	0	0	1	0	0	1	1	1
0	1	1	1	0	0	1	1	1	0	0	0
1	0	0	0	0	0	1	1	1	0	0	0

NOTE: Top line of table is first scan of character line (where HOLD REQ H occurs).

4.6.3.5 Generation of HOLD REQUEST - HOLD REQUEST is the signal to the microprocessor that makes it give up control of the data bus. Then the video processor can DMA a line of data out of the screen RAM and place the data in the line buffer. Two principle conditions can generate HOLD REQUEST. The most common is when the output of the Counter in Use = 0, meaning on the first scan of a new line of characters. (The Counter in Use, which is the output of the scroll MUX, is either the output of the offset or scan counter, depending on whether the current line is in or out of a scrolling region.) Whenever a new line of characters starts, a HOLD REQUEST is needed to get the line's data. Therefore, a detector at the output of the scroll MUX detects scan 0 of the Counter in Use.

The other condition for generating HOLD REQUEST is at the top of a new scrolling region. This is necessary because as the CRT beam moves from a nonscrolling region into a scrolling region, it switches from the last scan of a normally registered line to the first displayed scan of a line that is scrolling. Assuming the scrolling region is in midscroll, the first scan is not the 0th scan of the scrolling line, so the Counter in Use is not 0. The new scroll zone flip-flop (whose clock input comes from the scroll flip-flop that controls the scroll MUX) is triggered by entrance into a scrolling region. When the new scroll zone flip-flop is set, it forces a HOLD REQUEST even if the Counter in Use is not also 0. If the Counter in Use is 0 (implying an offset of 0 between scrolling and nonscrolling lines) there are two simultaneous causes for HOLD REQUEST.

The new scroll zone flip-flop is cleared by ADDR LD that occurs at the end of the Hold Request generated by the new scroll zone flip-flop. That is, the new scroll zone flip-flop generates HOLD REQUEST. HOLD REQUEST is cleared either by Terminate or Horizontal Blank, whichever comes first (the way the VT100 is programmed, Terminate is always first) and termination of that HOLD REQUEST feeds back through ADDR LD and clears the new scroll zone flip-flop. More about HOLD REQUEST follows a discussion of Horizontal Blank and Terminate.

4.6.3.6 Horizontal Blank and Terminate – Horizontal Blank, in addition to blanking the video output, clears the terminate flip-flop and also generates an internal timing signal (horizontal time reference) for clocking counters.

A short signal, that occurs on every horizontal scan and lasts only a few character times, is needed in the chip to clock flip-flops and to disable the decoder gates that detect boundaries and generate HOLD REQUESTS while the counters settle. Horizontal Blank cannot be used for this purpose because HOLD REQUEST and Boundary Detect (and other signals) need to be settled well before Horizontal Blank ends. The required short signal comes from a small counter triggered by Horizontal Blank and further clocked by character clock. The counter has two outputs: a two-character clock wide signal that enables and disables the boundary detect flip-flop (that drives the scroll flip-flop) and a three-character clock wide signal (H CLK) that enables the Hold Request gate. Boundary detect is enabled earlier than the HOLD REQUEST gate so that the existence of scrolling can set up the new scroll zone flip-flop before HOLD REQUEST is enabled. A gate combines the output of the new scroll zone flip-flop and the output of the boundary detector (Counter in Use = 0). The output of that gate is combined with H CLK (three character clocks long following Horizontal Blank) to generate the rising edge of HOLD REQUEST three character times after the rising edge of Horizontal Blank, and is also combined with the signal from the terminate flip-flop to end HOLD REQUEST when a terminator is detected.

If Terminate did not cut off HOLD REQUEST, then HOLD REQUEST would be disabled by the next falling edge of the H CLK signal, but the VT100 is programmed to always end HOLD REQUEST with Terminate. If the VT100 was not working right, HOLD REQUEST might be ended by Horizontal Blank.

Terminate causes a number of functions inside the DC012. The Terminate input is not direct; it is sampled on each rising edge of character clock and latched into a flip-flop. When detected, it ends any HOLD REQUEST in progress. In normal screen mode, it blanks the video output, but in reverse screen mode it forces the video output to the dim intensity level. The terminate flip-flop output feeds back to its own input, so that as soon as the flip-flop is clocked with Terminate asserted, the flip-flop latches itself up.

Once the terminate flip-flop is latched up by feedback from its output, there is only one way to clear it: through the asynchronous clear input. The flip-flop must not be cleared until Horizontal Blank has taken over blanking the video output; therefore the clear is delayed slightly (by one character time after the onset of Horizontal Blank). The clear is maintained until just before the character clock which corresponds to the first character on the screen because data on the video data bus may be undefined and might contain extraneous Terminates. These must not be detected during the horizontal blanking interval because they would latch up the terminate flip-flop for an entire scan. However, the internal signal that blanks the video outputs of the DC012 during the horizontal blanking interval cannot be used to clear the flip-flop directly because it must release the video output at the exact beginning of the first character on the screen, and the terminate flip-flop must be capable of detecting the terminator in the first character position. If the internal blanking signal was used to clear the terminate flip-flop, the release time of the flip-flop would not be satisfied, and it might miss a terminate in the first character position (as would be found in SET-UP and the top and bottom fill lines). Therefore the Horizontal Blank output of the DC011 is made to end approximately one-half character time before video unblanking to release the clear on the terminate flip-flop. Inside the DC012, the falling edge of Horizontal Blank H is delayed to the following character clock to provide the correct video blanking.

4.6.3.7 Double Width and Hold Request – The first occurrence of Terminate or Horizontal Blank at the end of a DMA normally gates Hold Request off. But in double-width mode, Hold Request is extended by two character times. This is required because each character appears twice in the external character latch pipeline. To get the first and second byte of the address of the next line correctly placed with respect to Address Load, the end of Hold Request must be delayed by two character times after Terminate or Horizontal Blank. This delay occurs either when double width is asserted alone or any time double height is asserted (because double height implies double width) by combining Hold Request with a two character time delayed version of Hold Request to give a Hold Request that starts at the normal time but ends two character times later.

4.6.3.8 Attributes – The attribute section of the DC012 basically implements Truth Table 4-6-4 which decides how to interpret various combinations of attribute inputs. A number of different inputs determine attributes applied to each character. There are the four attribute pins: Reverse Video H, Underline L, Bold L, Blink L. But there are internal signals (mostly from the input decoding section) that affect attributes also: the blink flip-flop (toggled by the input decoder to provide blink timing), the reverse/normal field flip-flop (set by input decoder), the base attribute flip-flop (set by the input decoder to select whether the reverse video pin is interpreted as reverse or underline) and the scan counts (from the output of the double height section, that enable the underline on the correct scan). These inputs are applied to a combination of gates that feed into a 4-bit latch before controlling the video outputs. This latch is clocked by character clock to change the attributes during the inter-character space.

Table 4-6-4 defines the following appearance for characters with attributes.

Normal characters appear uninverted at normal intensity by asserting VID OUT 2 whenever VID IN H is asserted. Bold characters are the same as normal characters except that VID OUT 1 and 2 are enabled. Reverse characters (exclusive-OR of reverse video and reverse screen) normally have dim backgrounds with black characters so that the large white spaces have the same impact on the viewer's eye as the smaller brighter white areas of normal characters. Bold and reverse asserted together give a background of normal intensity. Blink applied to nonreverse characters causes them to alternate between their usual intensity and the next lower intensity. (Normal characters vary between normal and dim intensity. Bold characters vary between bright and normal intensity.) Blink applied to a reverse character causes that character to alternate between normal and reverse video representations of that character. Underline causes the ninth scan of a character to be forced to white of the same intensity as the character for nonreversed characters, and to black for reverse characters.

4.6.3.9 Dot Stretcher – The dot stretcher reduces the video bandwidth required in the monitor (especially in 132 mode) by making the minimum dot width 80 nanoseconds. Wider dots give the CRT time to reach full intensity before turning off again. This makes vertical lines appear to have the same intensity as horizontal lines, rather than looking dimmer because of the brightness loss as illustrated in Figure 4-6-16. The dot stretcher works by delaying the VIDEO IN H signal by one dot time (using a flip-flop clocked by Dot Clock) and then ORing the undelayed and delayed signals. Figure 4-6-17 shows an example of the dot stretcher's operation.

4.6.4 Address Counter and Data Structure in RAM

Refer to the print set and to Figure 4-6-20. The address counter (E21, E22, E25, E30) is three presettable 4-bit binary counters cascaded to form 12 bits with an additional flip-flop that provides a 13th bit of address to the screen RAM. Vertical reset clears the counter to an initial hardwired value of 2000H so that the video processor always begins to process from that location after a vertical reset. The counter is loaded with a new address at the end of each DMA when the address load signal appears. The counter counts forward from this address at the character clock rate, using the address count (ADDR CNT H) signal. ADDR CNT H only occurs during Hold Request; thus, the counter only counts during the DMA portion of each line. The address is loaded at the end of the DMA scan

and held until the next DMA begins. The 13th bit is programmed by D4 in the high byte of a DMA address. The VT100 firmware programs this bit high to access address 2000H plus the contents of the 12-bit counter. But if D4 were programmed low DMAs would access address 4000H plus the contents of the 12-bit counter.

Table 4-6-4 Character Attribute Combinations

Attributes				Effect*		
Reverse†	Under-line L	Bold L	Blink L	Background Video (VID IN H = 0)	Character Video (VID IN H = 1)	Underline Video‡
L	H	H	H	O	N	X
L	H	H	L	O	N/D	X
L	H	L	H	O	B	X
L	H	L	L	O	B/N	X
L	L	H	H	O	N	N
L	L	H	L	O	N/D	N/D
L	L	L	H	O	B	B
L	L	L	L	O	B/N	B/N
H	H	H	H	D	O	X
H	H	H	L	D/O	O/N	X
H	H	L	H	N	O	X
H	H	L	L	N/O	O/B	X
H	L	H	H	D	O	O
H	L	H	L	D/O	O/N	O/N
H	L	L	H	N	O	O
H	L	L	L	N/O	O/B	O/B

Rev Field H	Rev Vid H	Reverse
L	L	L
L	H	H
H	L	H
H	H	L

Code in Table	Beam Intensity	VID 2 H	VID 1 H
O	Off	L	L
D	Dim	L	H
N	Normal	H	L
B	Bright	H	H
X	Not Applicable		

* For blinking, outputs are shown as OFF/ON where OFF and ON are the blink flip-flop states.

† Reverse = (reverse field H) XOR (reverse video H)

‡ Intensity of beam on underline scan

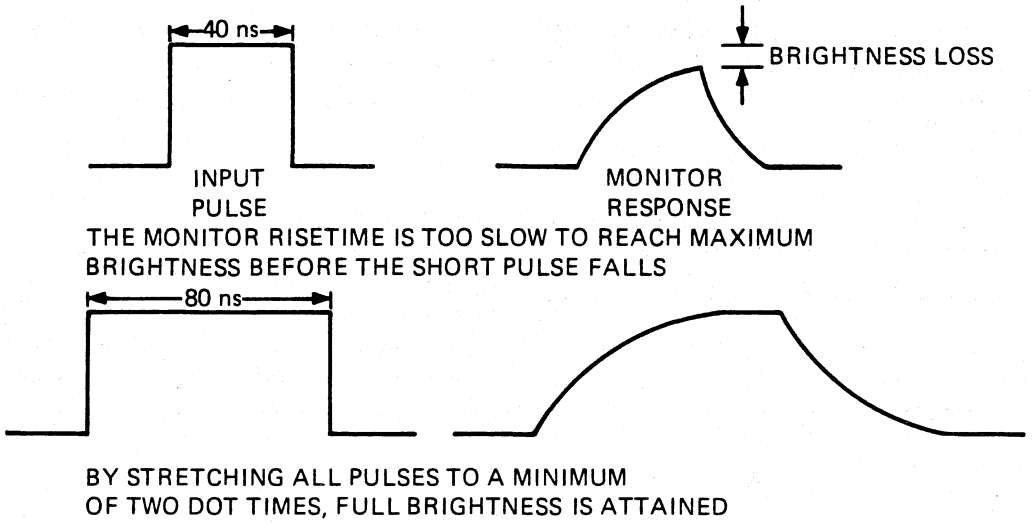


Figure 4-6-16 Dot Stretching

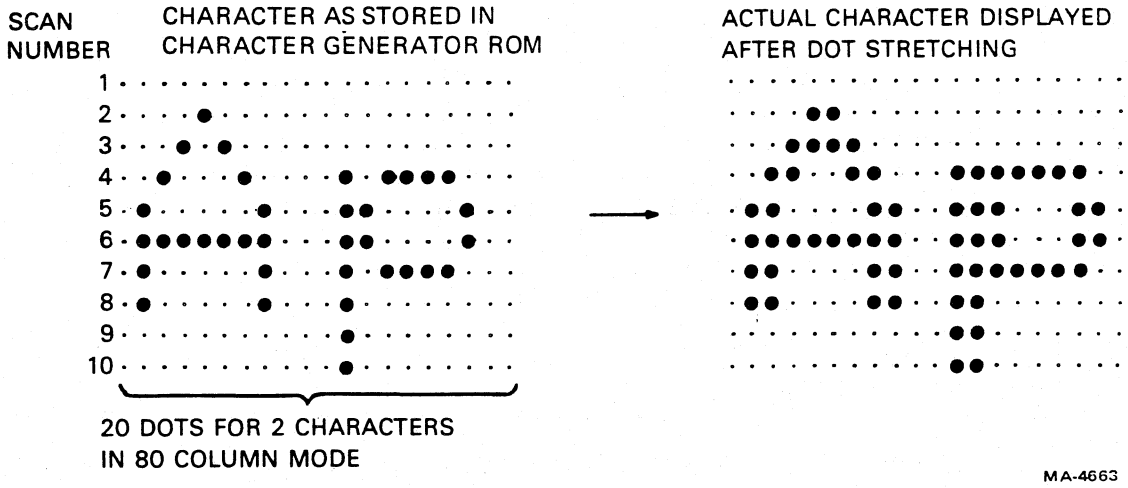


Figure 4-6-17 Dot Stretcher Example

In double-width mode, the address count pulses occur half as often as in normal width. The line buffer receives the normal number of WRITE LB pulses, however, so each character gets copied into two adjacent locations in the line buffer.

4.6.5 Address Latch Buffer

Tristatable latches (E26, E33) store the address counter outputs for a character period to increase the speed of RAM accesses that would otherwise be slowed by the long propagation delay of the counters. They provide sufficient output power to drive the address bus of the basic terminal controller board and the AVO if present. The outputs are disabled during the non-DMA period to prevent conflict with the microprocessor address bus.

4.6.6 Line Buffer

Data arrives at the screen RAM latch (E20) during a DMA cycle and is latched in by the character clock. During the DMA the tristate buffer (E15) is enabled. Data passes through it to the line buffer (E11, E17) for storage and to the character generator latch input (E16). The line buffer is a 256 × 8 RAM that can hold one full line of data including the three end bytes. The line buffer is written when WRITE LB L is asserted in the middle of each character clock period. Its outputs are disabled during the DMA by the Hold Request signal. During non-DMA operation, the screen RAM latch samples the 8080 data bus at the character rate but the tristate buffer is off so the 8080 data has no effect. However, the outputs of the line buffer are enabled and the same data is presented to the character generator latch as was presented during the previous DMA scan. The address signals for the line buffer are described in Section 4.6.2.7.

4.6.7 Character Generator

The character generator is a ROM that is addressed by the coded representations of the desired characters stored in the screen RAM. Each code is used as the high 7 bits of the address to a 2K × 8 ROM (that provides enough storage for 128 characters). (The eighth character bit is the base attribute input to the DC012.) The low four address bits are provided by the scan counter in the DC012. The seven character bits combine with the 4-bit scan count from the DC012 to give an 11-bit address to the ROM. The data stored at each (scan + character) address are 8 bits representing the presence or absence of dots of light at sequential horizontal positions within that scan. Figure 4-6-18 shows the patterns supplied in the standard VT100 character generator ROM.

If the alternate character generator ROM and the advanced video option are present, the AVO may assert ALT CHAR SET L to disable ROM E4 and enable ROM E9 when the alternate character set attribute is set.

If the AVO is installed without the alternate character ROM, any character cell in which the alternate set is selected will appear white (black if reverse video). See Appendix A (SCS) for selection of alternate characters.

If it is necessary to use a different main character set than the one provided in the VT100, but an alternate character set is not required, the following arrangement may be used.

1. Cut jumper W1 to disable the main ROM.

2. Plug a new main ROM into the alternate character ROM socket.

3. The new main ROM must be programmed exactly as the alternate ROM described in Section 6.5.1 except that the chip select on pin 18 must be programmed for high assertion.

To use a UV erasable PROM in the socket for E9 (which must have Intel 2716 pinouts), cut jumper W4 and insert jumper W5 to put +5 volts on pin 21. Only later VT100s have these jumpers. The access time of the ROM must be less than 300 ns to guarantee operation in 132 column mode.

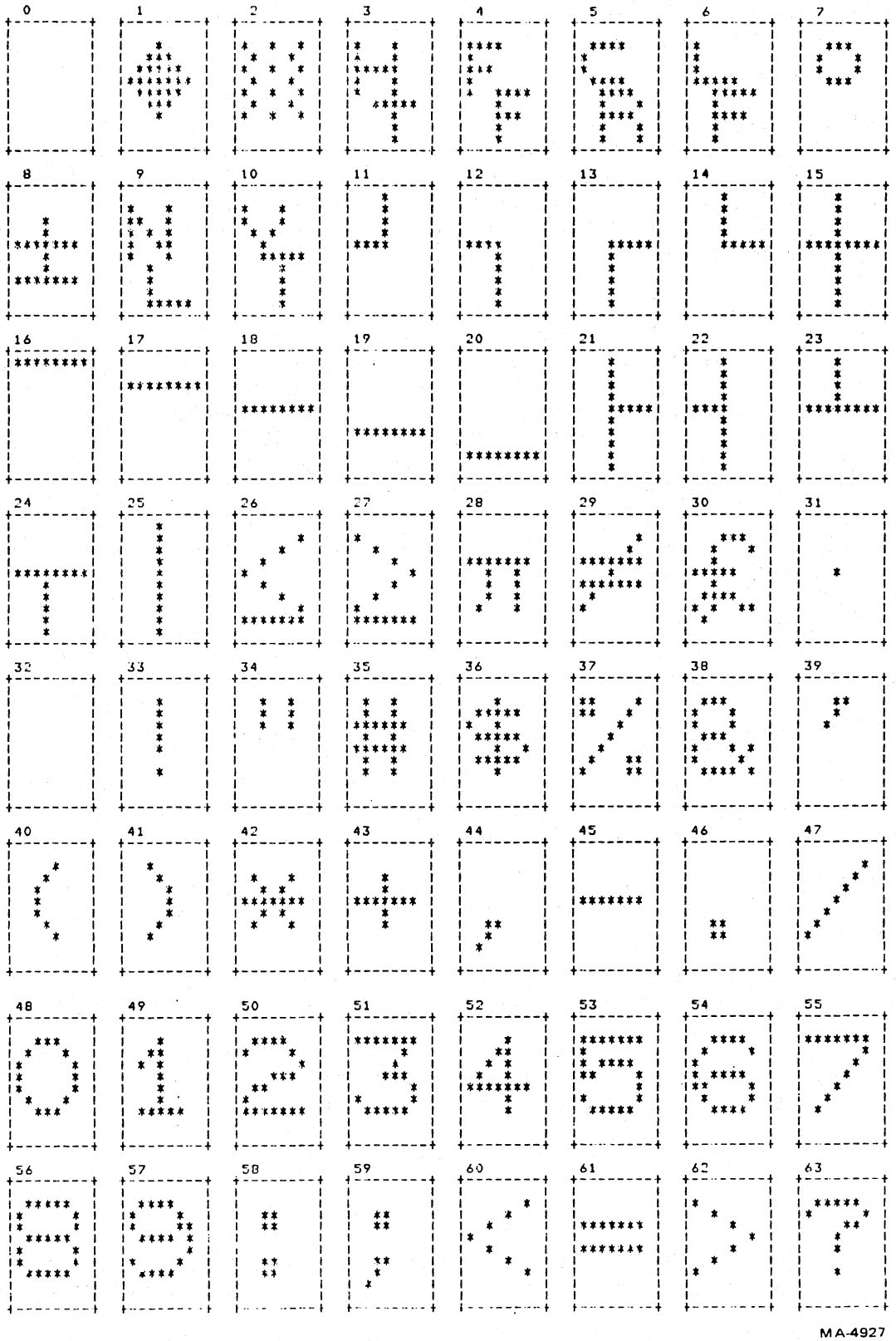


Figure 4-6-18 Character Generator ROM Patterns (Sheet 1 of 2)

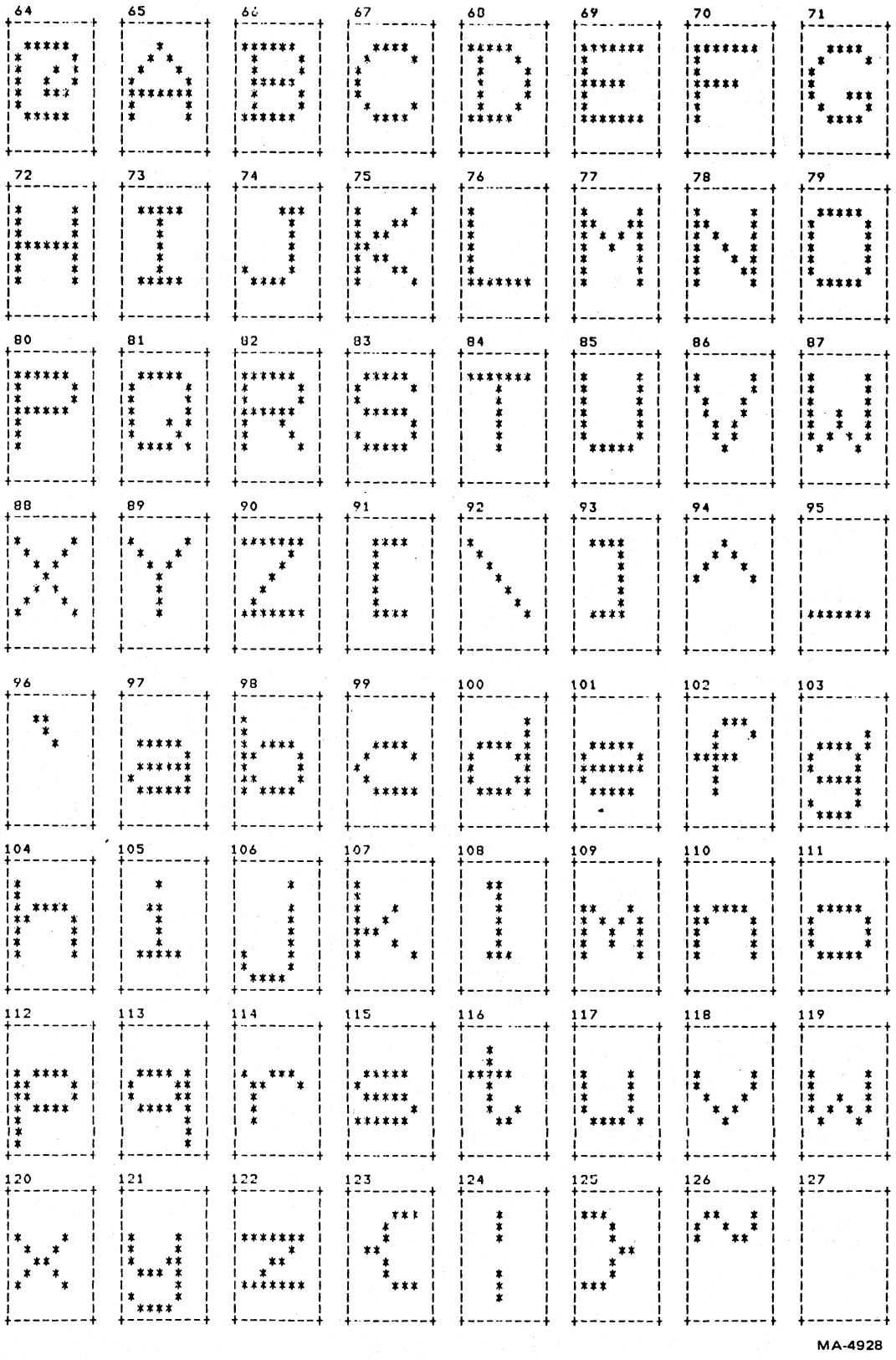


Figure 4-6-18 Character Generator ROM Patterns (Sheet 2 of 2)

4.6.8 Video Shift Register

When VSR LD H is asserted, seven of the eight output bits from the character generator ROM are latched into the shift register and one is latched into a flip-flop (Figure 4-6-4). At the same time, the last bit shifted out by the video shift register (VSR) during the previous character time is latched into the first bit position in the VSR. The VSR is continuously clocked by the dot clock. The first bit shifted out in the new character time is the same value as the last bit of the previous character, providing horizontal continuity of characters from one character cell to the next. The seven new bits are then shifted out.

Meanwhile, the flip-flop that stored the eighth bit has delivered that bit to the serial input of the shift register. This bit was shifted into each successive register position as the first eight bits were shifted out. Now the shifting continues, for one more bit in 132 mode, and for two more bits in 80 mode, causing the last bits shifted out to be the value that was stored in the flip-flop.

VSR LD H then latches the next character into the VSR and flip-flop, with that last, multiply-shifted bit in the first position. In this way, one bit from the character ROM defines the two or three dots between characters, while seven bits define the character itself.

At the end of the scan, horizontal blanking forces the flip-flop output low. Since blanking lasts more than one character time, the low level will be shifted to the first position before the start of the next line. This ensures that the first dot on the next scan will be at the screen background level.

4.6.9 Terminator

The 7 bits of each character address in a line go to an 8-input terminator detector gate as they are passed to the character generator ROM. Only seven bits are examined because the eighth bit is an attribute and does not contribute to the uniqueness of a character. The last bytes in each line are a terminator character and two address bytes. Only the terminator character activates the gate. During the character time when the terminator reaches the detector gate, the first address byte is at the input to the character generator latch and the second address byte is at the input to the screen RAM latch. On the next character clock, the terminator causes the DC012 to blank the display and end the Hold Request. The latch outputs now contain the two address bytes. The low order byte is at the inputs to counters E30 and E25, while the low four bits of the high byte are at E21. The fifth bit is at the input to flip-flop E22. This bit is normally high; it allows future development of screen RAM size. The high three bits go to the line attribute inputs to the DC012.

The address load (ADDR LD L) pulse, timed to arrive before the next character clock after the terminator, loads the address counters, flip-flop, and DC012 inputs with the two final bytes. The counters and flip-flop designate the address of the first character of the next line to be displayed.

4.6.10 DMA Cycle Timing Diagram

Figure 4-6-19 shows the complex timing in the video processor during the first scan of each new line of characters. The entire scan is shown, with the repeating portion compressed into the area represented by dashed lines. The diagram is for 80 columns, single width display as the VT100 is currently programmed. Diagrams in the DC011 timing chip description (Section 4.6.2) show the differences in signals in other modes.

The first line shows the Character Clock. This continuous signal is the time reference for all DMA events.

The terminator occurs at the end of the previous scan. TERM L goes low for one character clock and then goes to an unspecified state which depends on the random characters that appear at the terminator detector gate. Character Clock continues to shift data through the character latches but invalid data are present in the character latches and stored in the line buffer until just after DMA ENA is

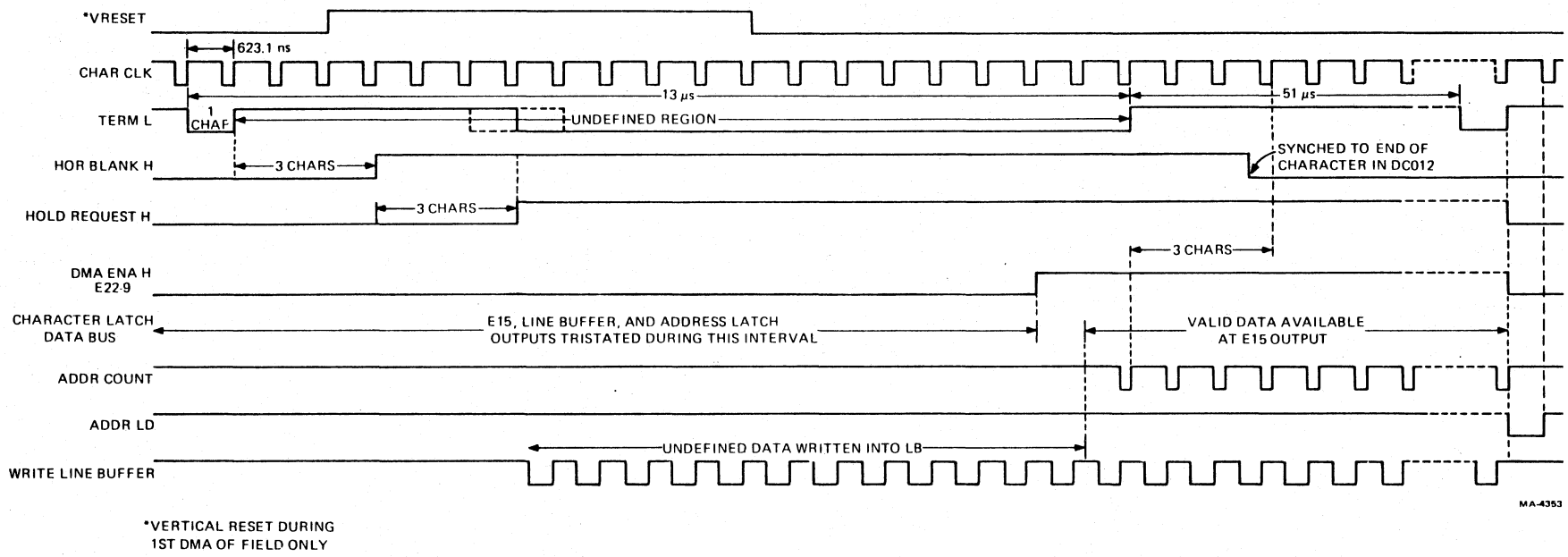


Figure 4-6-19 DMA Cycle Timing Diagram

asserted. The terminator forces the video output to black or white (depending on normal or reverse screen) effectively blanking the end of the line (Section 4.6.11). It also ends any DMA process in progress. The terminator's blanking effect is taken over by Horizontal Blank, and the terminate flip-flop in the DC012 is held cleared until just before the first character in the next scan. This prevents undefined data from triggering the flip-flop and blanking the whole scan.

Horizontal Blank occurs 3 characters after Terminate in 80 column mode and 5 characters after in 132 column mode. It forces all video to black (regardless of normal or reverse screen) for the horizontal retrace interval. The Horizontal Blank signal, as an output from the DC011, ends one-half character before the video actually needs to unblank. This early transition releases the clear for the terminate flip-flop in the DC012. The blank signal is resynchronized to Character Clock in the DC012.

Hold Request silences the microprocessor so that the video processor can DMA data out of the screen RAM. It is initiated when the scan counter in use is equal to 0, or at the setting of the new scroll zone flip-flop. The terminate flip-flop must be cleared for Hold Request to occur. The start of Hold Request is delayed by three character times from Horizontal Blank to allow the counter in use to settle before the 0-boundary is detected. Hold Request is ended by the detection of terminate at the end of a DMA scan.

DMA Enable is generated from Hold Request and the microprocessor's hold acknowledge (HLDA) by discrete logic on the board (E22). It is enabled by the first rising edge of LBA4 if HLDA from the 8080 is available. This ensures that the 8080 has given up the bus before DMA ENA H enables the DMA address counters onto the bus and drives MEM R low. DMA ENA H is cleared by the end of HOLD REQUEST H. While the use of LBA4 ensures that enough time has elapsed from the start of HOLD REQUEST H to guarantee that the 8080 is in its hold state, the use of HLDA H on the D input of the DMA Enable flip-flop is required to prevent HOLD REQ from preventing a power-up cycle in the 8080.

The character latch data bus is shown to be tristated from the start of Hold Request until the start of DMA Enable. Then it starts moving data through the video circuits.

Address Count begins three character times before the end of Horizontal Blank (Section 4.6.2.4).

Address Load is triggered by the falling edge of HOLD REQUEST H. It stores the line attributes for the next line and loads the address counters with the pointer address bytes at the end of the DMA line of characters. This address is the location of the first character of the next line to be DMA'd.

Write Line Buffer L is described in Section 4.6.2.3.

Figure 4-6-20 is an expansion of the DMA timing showing the contents of the various storage devices at different times at the beginning of the active display of a scan.

4.6.11 Video Blanking

The display is blanked by Horizontal Blank during the horizontal retrace interval, and by Vertical Blank during the vertical retrace interval. These hardware signals ensure that the CRT beam is turned off while it moves backward through the active screen area. Horizontal Blank controls the video signal inside the DC012. Vertical Blank controls the video signal at the video output circuit. Figure 4-6-21 shows a frame of video divided into segments of one horizontal and vertical movement of the electron beam over the CRT face with respect to time. Figure 4-6-21 plots the screen and its invisible regions by relating the screen area to the state of blanking at any given time. The top-left corner represents the first visible dot position. The terminator position is the place where no data is displayed but Horizontal Blank has not yet taken effect. Horizontal Blank then takes effect all through the horizontal retrace period and unblanks just in time for the first dot of the next scan. After 240 scans, Vertical Blank turns off the beam while the beam returns to the top of the screen.

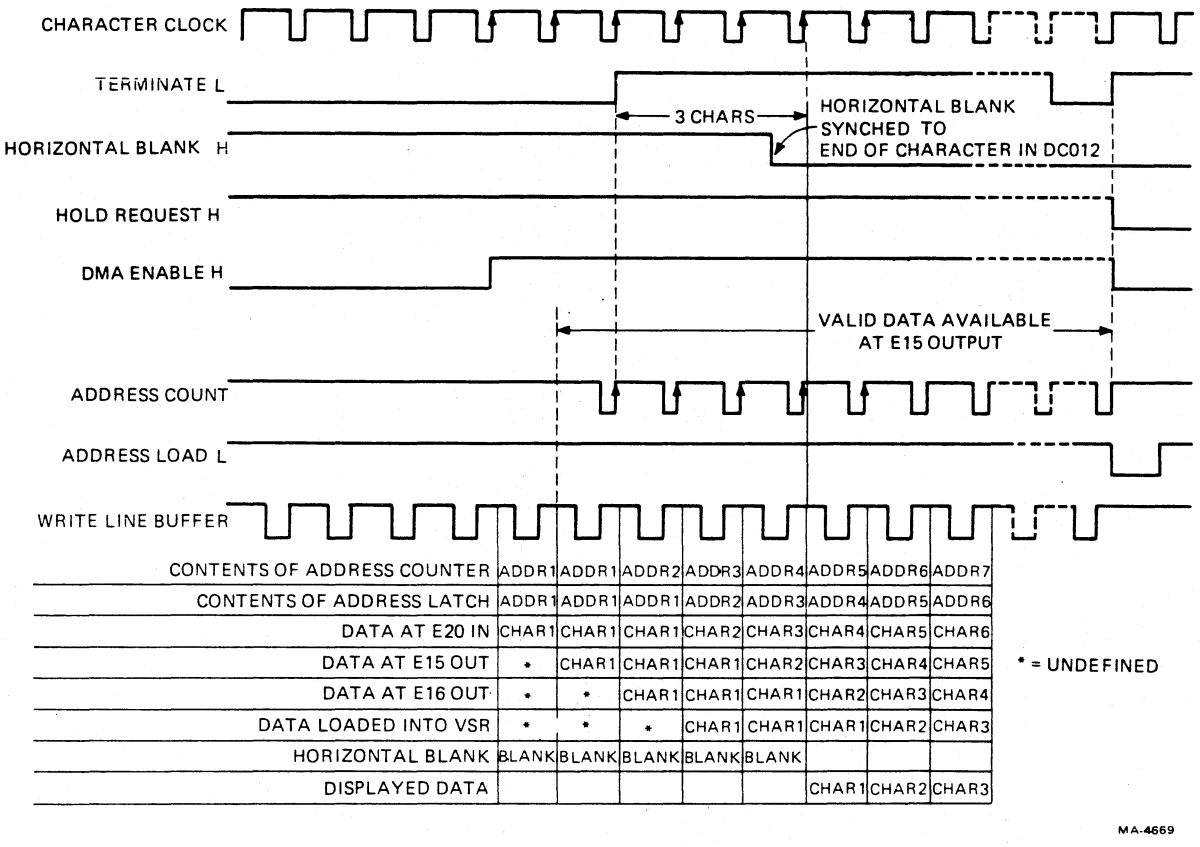


Figure 4-6-20 Character Latch Timing

The horizontal blanking signal is timed to provide 83 columns of unblanking in 80 column mode, and 137 columns of unblanking in 132 column mode. The VT100 is currently programmed so that the three or five extra columns are blanked by Terminate. In normal screen mode, this termination forces the beam to black, but in reverse screen, termination forces the beam to the screen background intensity. This means that in reverse screen mode, the last character that can fit on the screen is three or five characters in from the right edge of the illuminated screen. Because hardware blanking allows 83 or 137 columns on the screen, future program developments may allow the microprocessor to format the screen RAM for this ability. The main adjustment is to the position of the terminator and address bytes relative to the starting location of the line. Terminate, as the first character in the line, creates short lines during the vertical blanking interval to conserve memory while maintaining synchronization of the line address system.

4.6.12 Video Input and Output

Refer to the print set for the circuits discussed in the next three sections.

4.6.12.1 Direct Drive Video – The two video outputs from the DC012, Video Out 1 and Video Out 2, are combined with Vertical Blank in two open collector nand gates (E7). The outputs of the open collector gates are wire-ANDed with Graphic 1 and 2 IN (E29) from any option board that may be present. The combined outputs of E7 and E29 pass through and either float the base of Q4 to +12 V through R38, R39, and R36 or R37, or pull Q4's base down to some value determined by one, the other, or both resistors R36 and R37 in parallel. These four conditions represent the four levels of intensity visible on the screen: black, dim, normal, and bright.

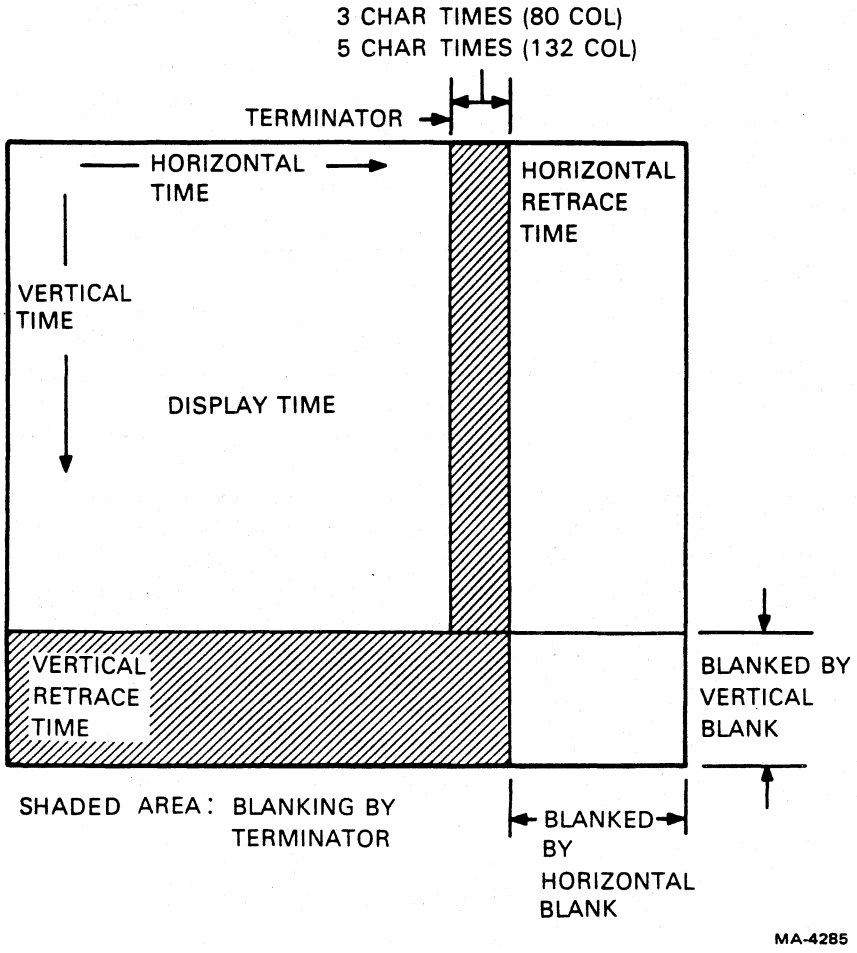


Figure 4-6-21 Video Blanking

4.6.12.2 Composite Video Out – The combined outputs of E7 and E29 control the voltage at Q2's base through R31, R32, and R33 in the same manner as described above. At the same time, composite sync controls Q2's base through R33 and R30. The result is a 75 ohm output from the terminal controller consisting of four intensity levels (including black) and composite sync. This signal can directly drive a standard video monitor or sync can be extracted to synchronize an external device for input to the terminal. The output is dc coupled. Although the use of dc coupling is not in strict agreement with EIA specification RS-170, this presents no problem with most monitors because they are usually ac coupled. See Figure 3-4 for an illustration of the composite video output.

4.6.12.3 Video In – The video input stage terminates a standard video signal in 75 ohms. R43 and D7 bias Q5 into linear operation, while C16 passes video around the bias network. R44 suppresses oscillation in the stage and D6 protects the transistor from a reversed polarity input. D5 biases the base of Q3 and R41 is the load resistor for the amplifier. R42 stabilizes the amplifier by emitter feedback. The video input affects only the picture on the internal monitor as described below; it does not appear at the Composite Video output.

4.6.13 Intensity Control

The video input and output circuits can produce a range of voltages (as compared with circuits that can produce only two values, white or black levels for example). To do this they are biased into linear

operating conditions. High current biasing provides the necessary high speed operation. Because of the high power dissipation that results, the video circuits use discrete transistors.

Direct Drive Video is the output from the terminal controller to the video monitor's cathode driver transistor. It is a combination of Video Out 1 and 2 signals from the video processor, and by means of a parallel transistor Q3, the signal from the video input (labelled Graphics Video In on schematic sheet BV4). The monitor already receives horizontal and vertical deflection signals directly from the terminal controller, so the terminal's video input only requires picture information. If the blanking level on the video input is greater than zero volts, the screen background intensity cannot be black. Note that composite sync on the input is also ignored by the terminal controller, because the terminal's timing is produced entirely by a crystal and cannot be synchronized to external signals. As explained in Chapter 3, external sources may be synchronized with the composite sync signal that appears at the output jack.

Q3 and Q4, in parallel, are one amplifier with common emitter and collector resistors. The emitter feedback resistor is R40, connected to +12 volts. The collector load is the input impedance of the monitor to ground in parallel with R54 and any one of 32 parallel combinations of R49, 50, 51, 52, and 53. This arrangement allows either transistor to set the minimum current through the collector and emitter resistors with the voltage that appears on its base. The other transistor then cannot reduce the current by being turned off. It can increase the current, however, if it receives a larger base voltage. Thus the output is always proportional to the greater of the two inputs. Two identical input signals do not add up because of the common emitter resistor. If the voltage on Q3's base is more positive than the voltage on Q4's base, a voltage at the base of Q4 causes a 0.6 volt different voltage at R40 (both emitters), and current to maintain that value will flow through Q4 and R40 (as well as the collector load). If the same voltage as at Q4's base is applied to Q3's base, the voltage at the emitters will not change due to the identical voltage drops across the two base-emitter junctions. There is no current change and so the output remains constant. D8 and R48 provide an extra 0.6 volts of bias for the cathode drive transistor in the monitor. C17 bypasses the diode for video signals.

The 32 combinations of resistors in the collector load of the output stage are produced by connecting any of the selected resistors to ground through an open-collector buffer. The buffer inputs come from the D/A (digital to analog) latch. This latch is written into as an I/O device by the microprocessor. In SET-UP mode, the microprocessor uses the up and down cursor keys as inputs to a 5-bit software up-down counter. At each vertical reset, the microprocessor writes the current contents of the counter into the latch. Thus there are 32 possible intensity levels available, controlled from the keyboard, and frequently updated to minimize the effects of soft errors. Note that the variable intensity only applies to the internal monitor.

4.7 MICROPROCESSOR - VIDEO PROCESSOR INTERFACE

The microprocessor communicates with the video processor in the following ways.

1. During setup, the microprocessor reads the setup specifications and writes them into the DC011 and DC012 to establish screen attributes.

2. The contents of the screen RAM directly control the display of the lines and characters. This region of memory contains the displayable characters, their attributes, the line attributes, and the addresses that link one line to the next. The microprocessor modifies and updates this information in the intervals between DMAs. During each DMA, the video processor copies one line of characters from the screen RAM for display on the screen.

3. During smooth scrolling, the microprocessor updates the scroll latch in the DC012.

This section describes the processes of control through the screen RAM and scrolling. The meaning and mechanism of the line and character attribute bits and the DMA process are discussed in the video processor section. The setup process is discussed in the 8080 section.

4.7.1 Screen Memory Organization

Three bytes of control data are located at the end of each line of characters (Figures 4-7-1 and 4-7-2). The first byte, called the terminator, is 7FH and is a unique character that the video processor recognizes as the end of the line. (The high bit is not tested by the terminator gate but is set to zero to avoid complications in the attribute circuits.) Five bits of the next byte and all of the last byte are an address

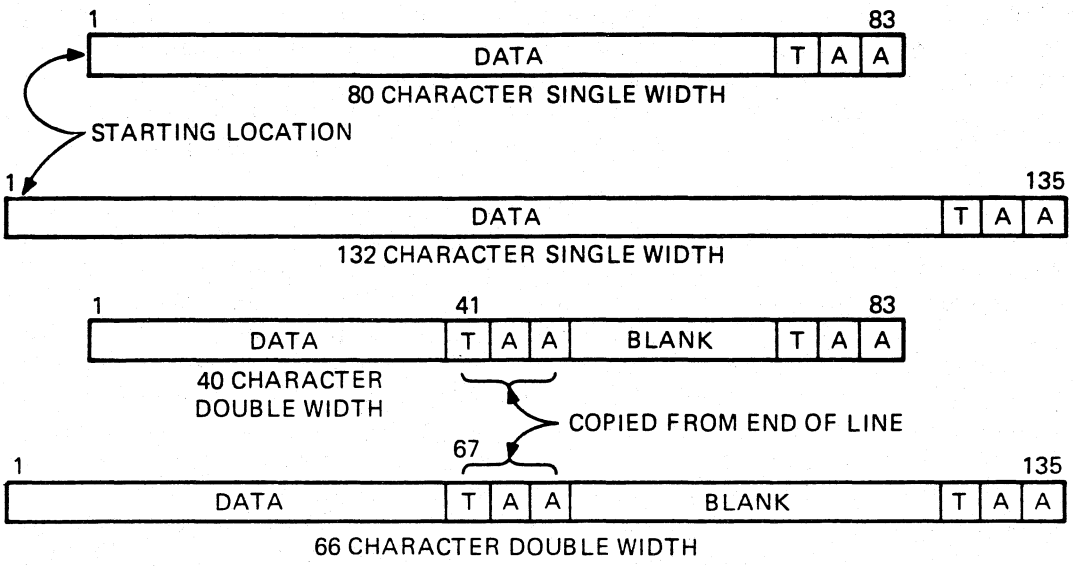


Figure 4-7-1 Line Organization

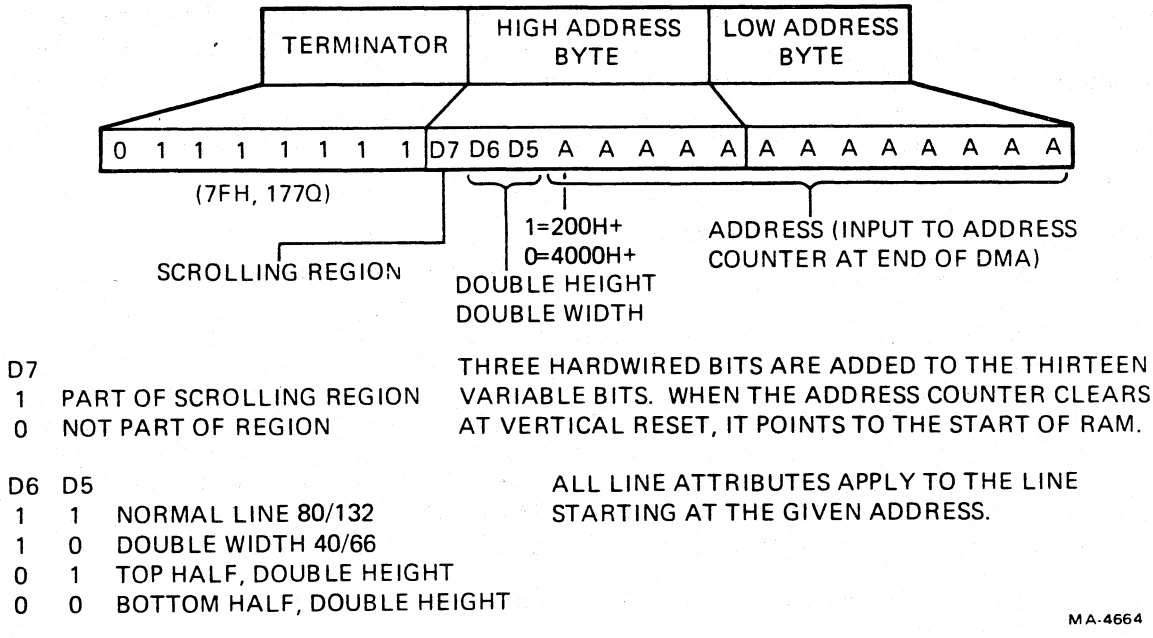


Figure 4-7-2 Terminator and Address Bytes

pointing to the first character of the next line to be displayed. The three remaining bits in the first byte define the line attributes of the line pointed to by the address. The high bits of the address are hard-wired at the address latch so that when vertical reset clears the address counter, it will point to the ROM-RAM boundary at 2000H.

During power-up or reset the microprocessor writes terminators and addresses into the screen RAM according to the specified line length and refresh rate. The 50/60 Hz refresh choice causes the microprocessor to arrange fill lines to place the beginning of the display in the right time slot relative to the vertical reset and vertical blanking signals. The line length determines the locations of the control bytes. For 80 column lines, the memory space is arranged in 83 byte intervals; for 132 columns, the interval is 135.

The memory organization for 80 column, 60 Hz mode is shown in Figure 4-7-3. Location 2000H is the start of the RAM space. When Vertical Reset resets the DMA address counter in the video processor to zero, the counter latch points to this location. The first 18 bytes are fill lines. Byte 2 is the only one written differently when 50 Hz refresh is selected. The change causes a longer fill time during the longer vertical blanking interval.

About 700 bytes of RAM are reserved for the microprocessor stack, scratchpad, and setup areas. The rest of the 3K RAM is devoted to screen information. At program start, the microprocessor reads the contents of the NVR into the setup area (Section 4.7.11). Then the microprocessor reads the setup parameters, erases the screen area and writes in terminator and address/attribute bytes at the selected line length intervals. The address at the end of each line points to the first location of the next line. At start-up, this is the next physical location. The end of the last line points to a fill line which points to itself. The fill line repeats until vertical reset.

4.7.2 Fill Line Operation

The video processor clock is constant so it always takes the same amount of time to refresh the screen. At any refresh rate there are some fill lines needed at the beginning of the frame so the data can be displayed starting a few lines down from the top edge of the picture tube. At the slower refresh rate, the video processor must idle for awhile between frames. Figure 4-7-4 illustrates the vertical position of the electron beam in the CRT as a function of time for the two refresh rates. The beam sweeps down the display area at the same rate for both refresh rates but because 50 Hz has a longer interval between sweeps, the beam travels farther off the ends of the display. While the beam is off screen, fill lines maintain synchronization in the video processor address system. More fill lines are needed at the top and bottom of a 50 Hz screen than a 60 Hz screen. Figures 4-7-5 and 4-7-6 show the top-of-screen fill line operation for both refresh rates. Starting at location 2000H, the terminator-address triplets point successively to one another and then to the first displayable line of data in the screen RAM. The change of one byte in the group changes the fill line delay from two lines for the 60 Hz refresh rate to five lines for the 50 Hz refresh rate. Figure 4-7-7 shows how the single bottom fill line repeats itself as many times as needed until vertical reset stops it and clears the address counter to 2000H.

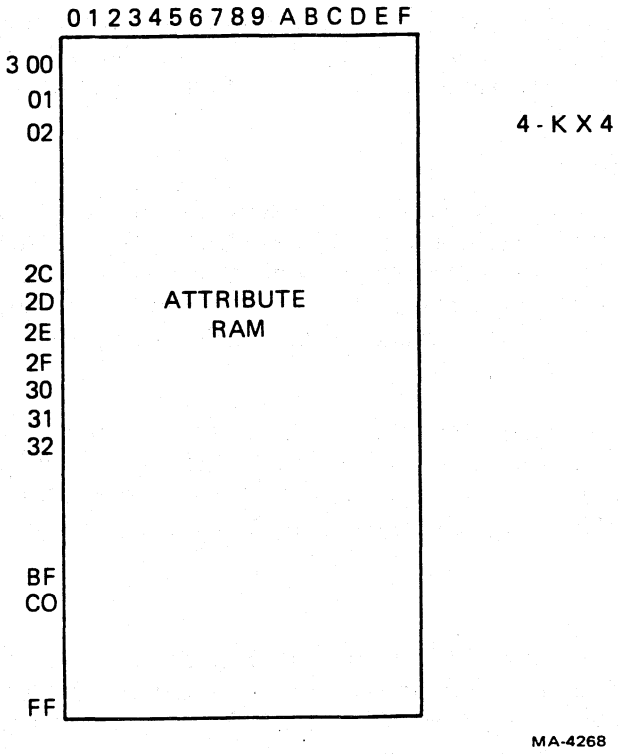


Figure 4-7-3 Screen RAM Organization – 80 Column, 60 Hz
(Sheet 1 of 2)

4.7.3 Line Organization

In 132 column mode 25 lines are set up in the RAM for a 24 line screen, and 15 lines are set up for a 14 line screen. With the advanced video option, 25 lines are set up for either 80 or 132 column lines. Except during a smooth scroll, only 24 lines are seen. But the microprocessor keeps the 25th line erased in reserve, and when a scroll takes place, the 25th line becomes visible as the new top or bottom line (depending on scroll direction). All new characters after the command that caused the scroll go into this line. In preparation for a full screen scroll up, the microprocessor writes the address of the repeating fill line into the 25th line pointer as well as the 24th line pointer. This saves processing time during the address rearranging which is a part of each scroll.

The line organization changes when the first scroll occurs. Pointer addresses are revised any time a line is added to or removed from the screen. The extra line is used whenever the screen needs to be scrolled up or down. Then the extra line is displayed and the old top or bottom line is scrolled off screen, erased, and made available as the new 25th line.

To understand the pattern of address changes, consider the display to consist of two parallel entities: a physical screen and a logical screen.

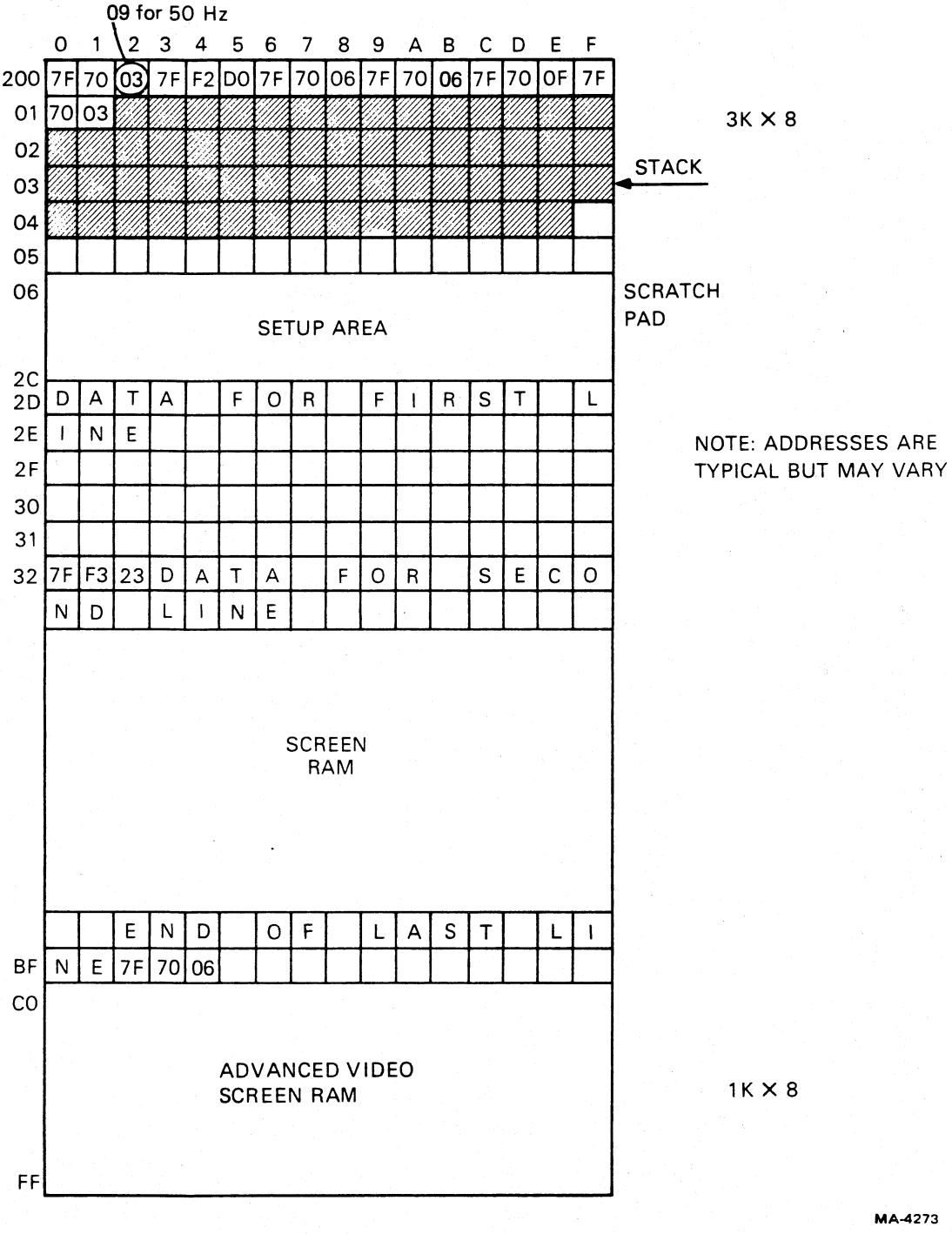


Figure 4-7-3 Screen RAM Organization – 80 Column, 60 Hz
(Sheet 2 of 2)

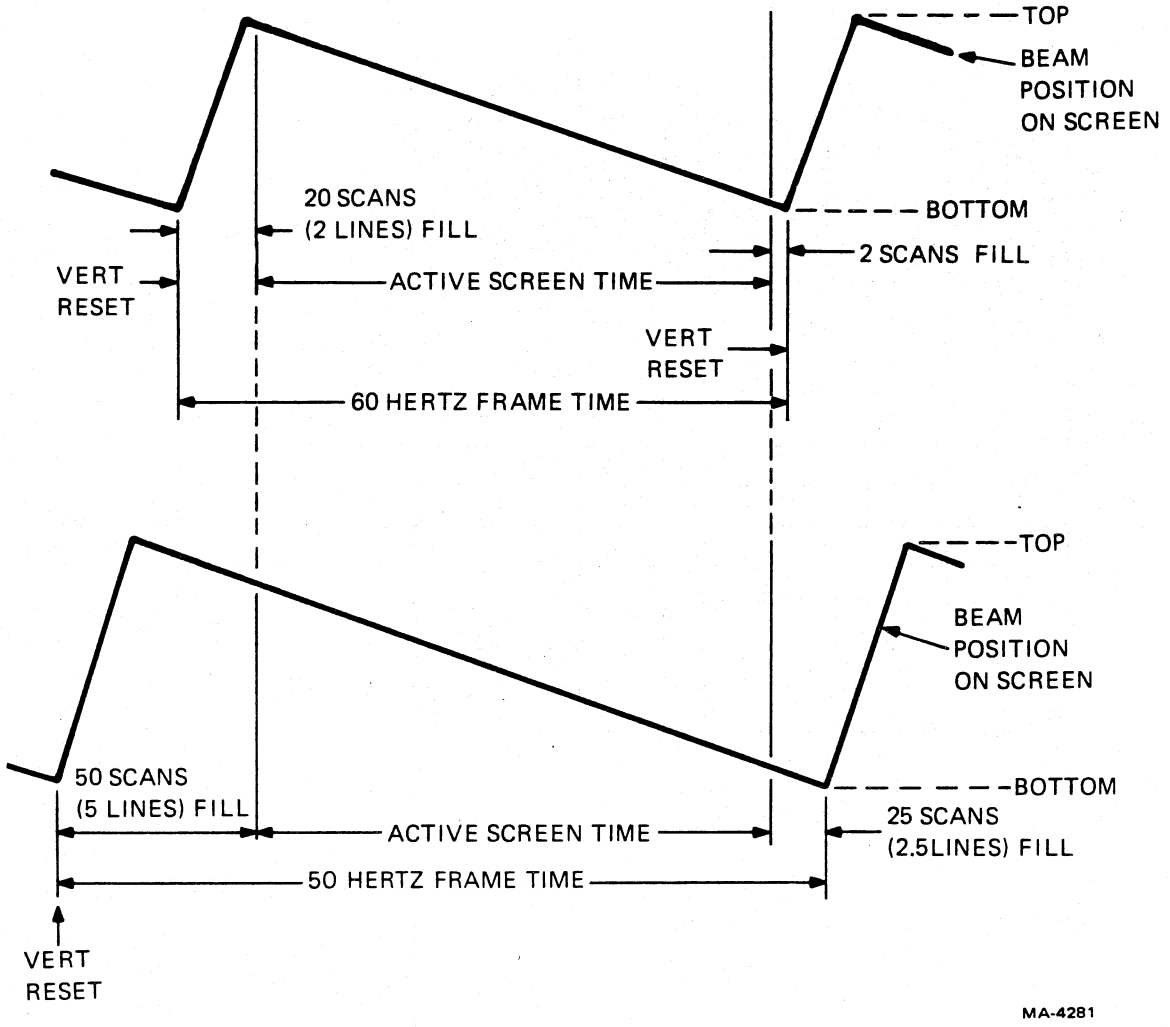


Figure 4-7-4 Need for Fill Lines

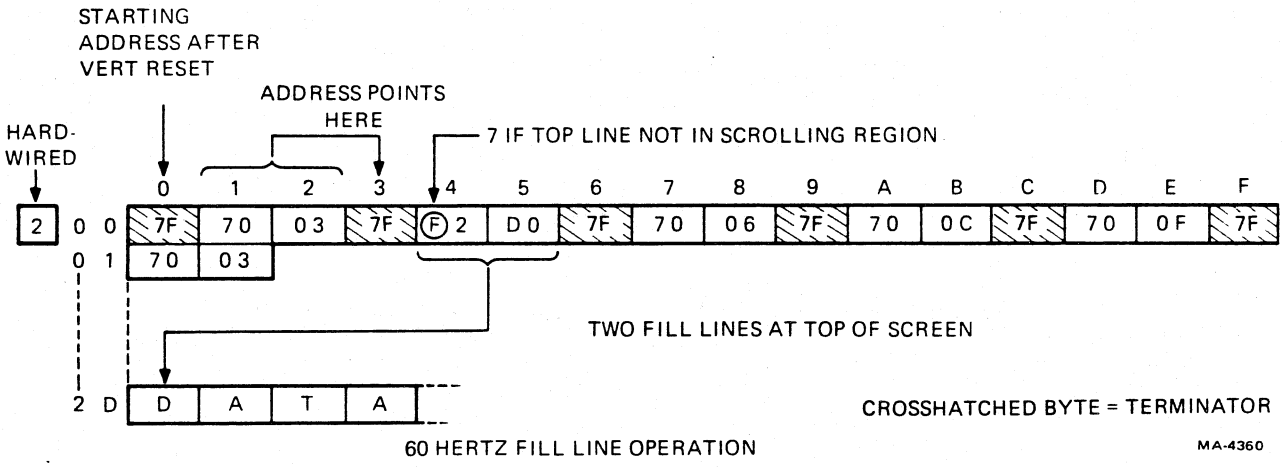


Figure 4-7-5 Fill Line Operation – 60 Hz

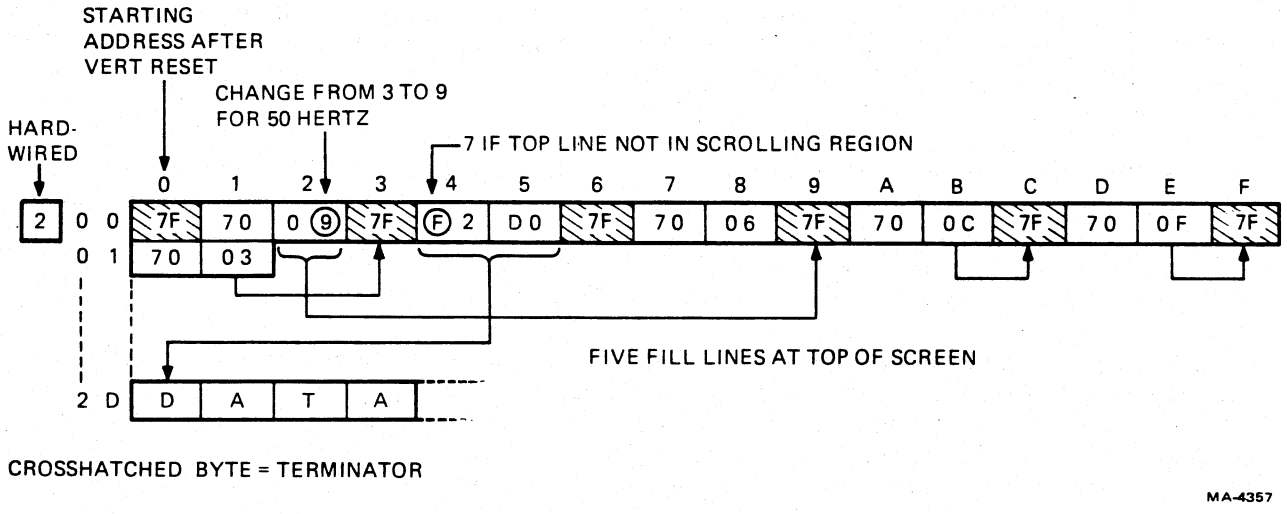


Figure 4-7-6 Fill Line Operation – 50 Hz

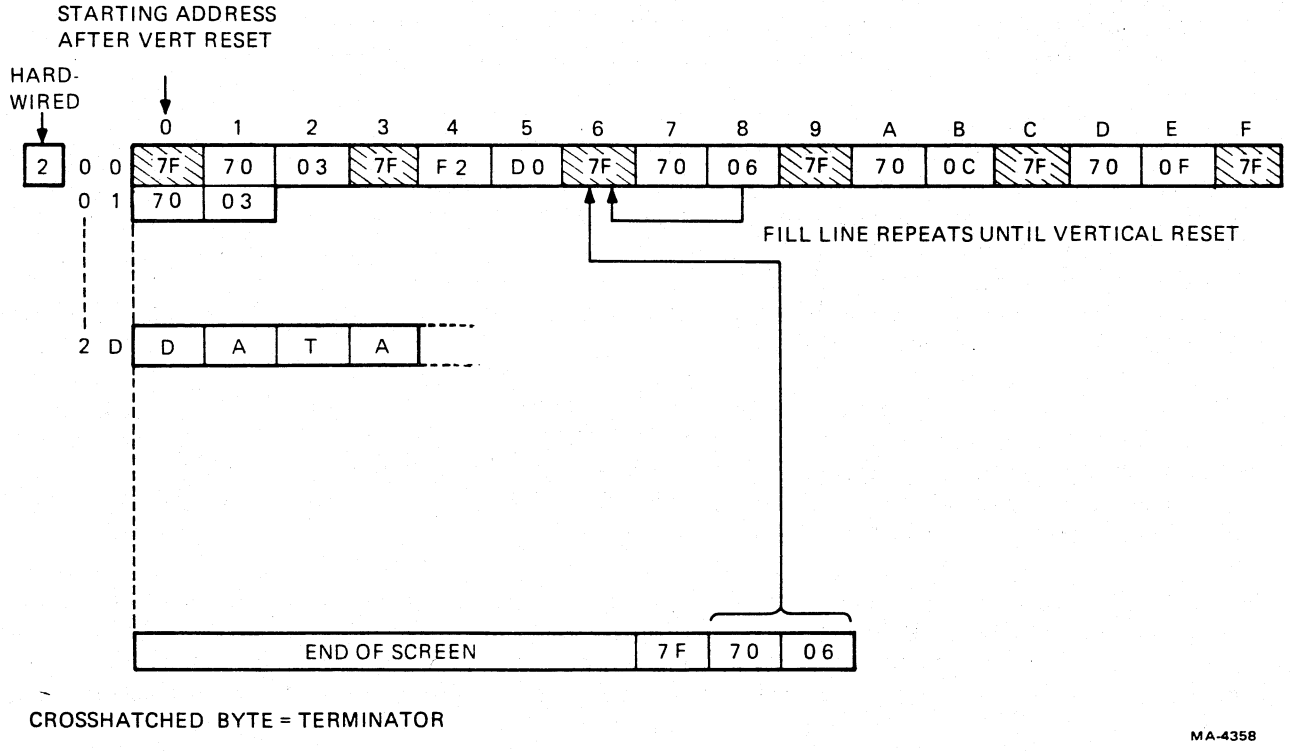


Figure 4-7-7 End of Screen Fill Line Operation

4.7.3.1 Physical Screen – The physical screen is the memory organization already described. The key feature of the physical screen is the pointer address, contained in each line, that causes the hardware to chain the lines into a sequence for display. After a series of split screen scrolls, the physical screen will contain some arbitrary sequence of line addresses.

For example, if the original order of lines was 1,2,3,...23,24, the new order might be 16,13,24,...1,8. With only this organization, a command to insert a line at the fifth position on the screen would require the microprocessor to follow the various pointers around the RAM until it reached the fourth such pointer in order to learn where the physical address of the current fifth line was in the RAM. Instead, a list of locations is maintained in the logical screen.

4.7.3.2 Logical Screen – The logical screen is a 25-entry table that points the microprocessor to the proper locations for shuffling (rearranging) line addresses and placing the cursor in the screen RAM. The table is set up in a contiguous area of memory starting at the location named LATOFS (Line Address Offset Table). Figure 4-7-8 shows LATOFS after at least one split screen scroll and in the process of another split screen scroll. Each entry in LATOFS is the number of a line in the physical screen. The position of an entry in LATOFS refers to the position of a line on the screen. The microprocessor updates LATOFS just before each scroll so that the microprocessor can rewrite line addresses during the vertical interval. The microprocessor reads the table to learn which line in RAM is available for writing as the new 25th line or which line is being used at a given position on the screen. For example, to insert a character in the fifth line, if the fifth entry in LATOFS is "20," the microprocessor calculates the starting address of the 20th physical line in RAM. The character address can be calculated from that starting address and the cursor position within the line.

4.7.4 Address Shuffling

Consider the case of a full screen upward jump scroll. The line in LATOFS #25 is the extra line, not seen except during smooth scrolls. When a line is jump-scrolled off the screen, it becomes the extra line, and the RAM area that was line 25 becomes the new last line. The scrolled-off line is erased and its first location is noted as the starting point for new data entry into the RAM. The physical screen addresses that chain in which the displayed lines must be revised. And since the last fill line must point to the new first line, which formerly was the second line, the revisions must be done before that last fill line is DMA'd into the video processor.

When a line feed is received, four numbers are stored in memory. These are Shuffle Address 1 and 2 (SHUFAD) and Shuffle Data 1 and 2 (SHUFDT). SHUFAD contains the location of the address that must be changed, and SHUFDT contains the new address that will be inserted there. The two sets are for the pointer above the line that will be scrolled off, and for the pointer on the end of the line that will be the new next-to-last line (Figure 4-7-9).

The process of changing the addresses is called shuffling because most of the computation is done in advance. The change is made quickly in a simple point-swap-point-swap sequence. One other item prepared in advance is the pointer on the 25th (to become the new last) line. The pointer on the present last line is copied onto the new line. The shuffling process takes less than 550 microseconds (the time between DMAs). The screen's apparent jump up or down is entirely the result of the revision of pointer addresses. If, for example, the shuffle occurs during the 15th line, no effect will be visible until the end of the frame, when the extra line is pointed to but is outside the viewable area. After vertical reset, however, the shuffled address at the top of the screen will point to the old second line. The first line is gone, and now there is room on the screen for the extra line and it appears.

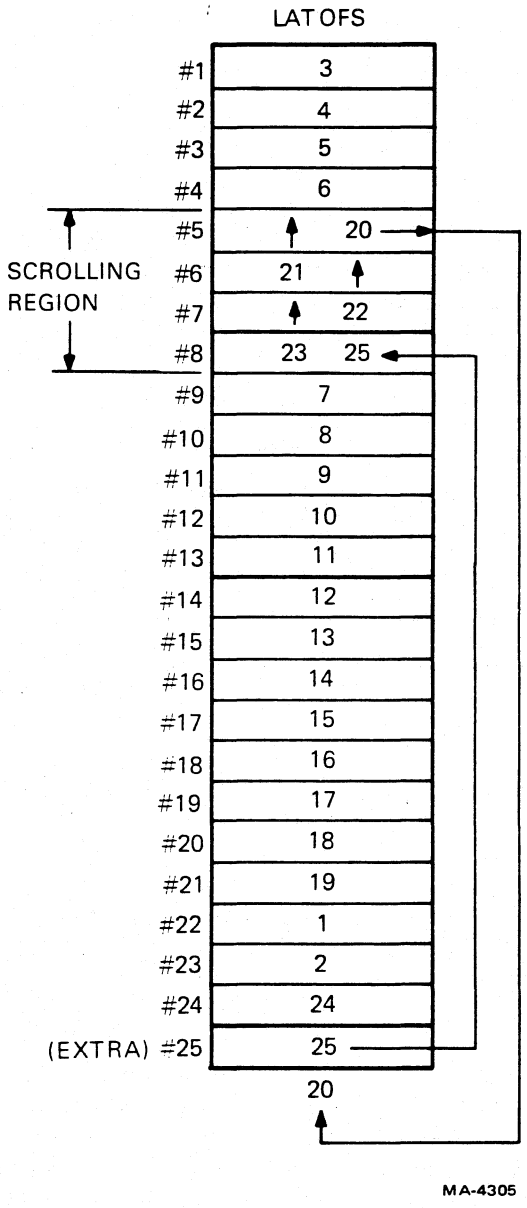


Figure 4-7-8 Line Address Offset Table

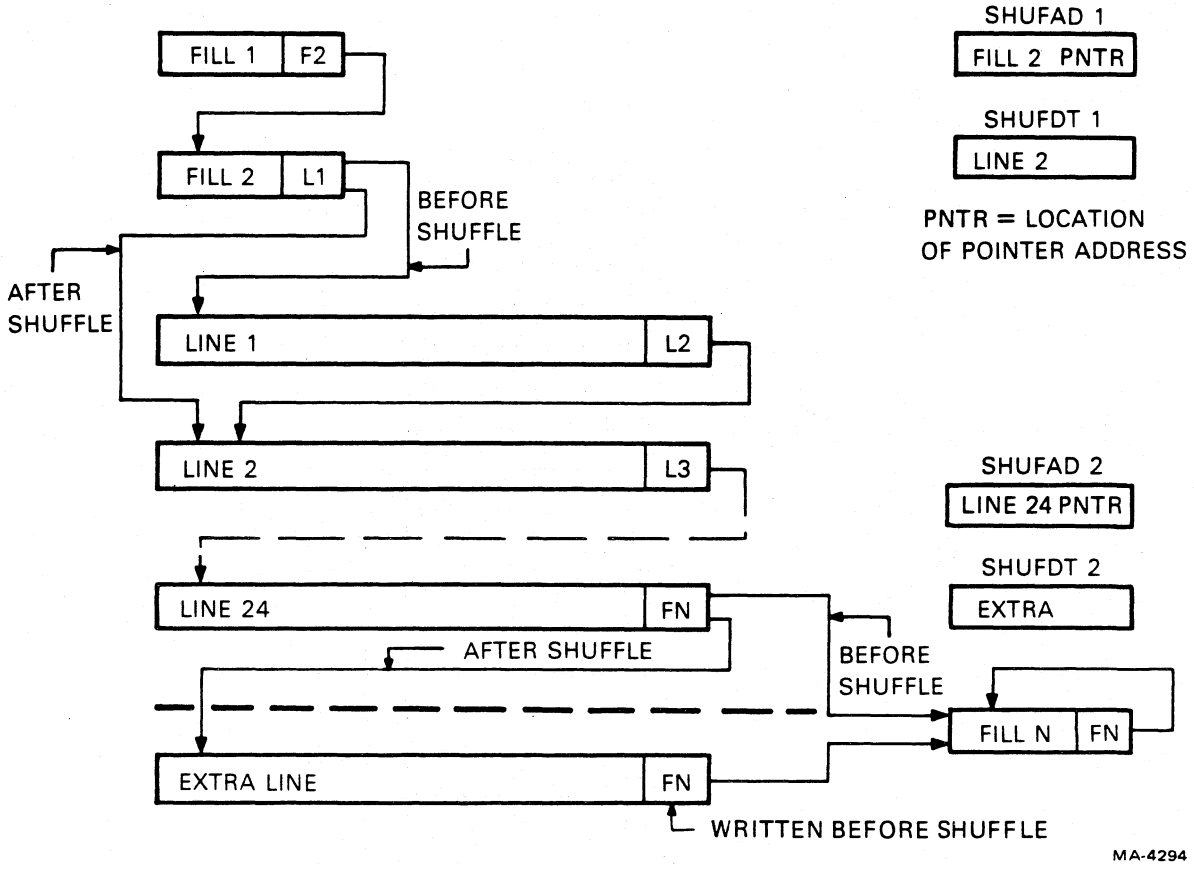


Figure 4-7-9 Full Screen Address Shuffle

4.7.5 Shuffle Timing

The shuffles for smooth and split screen scrolls must be synchronous with vertical reset to avoid disrupting the appearance of the display. Therefore, only one line feed can be executed during a frame. However, in the case of full screen jump-scrolling, the address shuffle may occur at any time. This increases the rate at which line feeds can be executed and improves the terminal's throughput.

While full screen jump scrolling may occur at any time relative to vertical reset, the two other kinds of scroll are sensitive to the time when shuffling occurs. If a split screen scroll region (say 10 lines in the middle of the screen) is revised while the display is scanning that region, only the change at the bottom of the region would take effect during that frame. The extra line would appear at the bottom of the region and the following lines on the screen would be pushed down one line from their locations in the previous and succeeding frames. The appearance would be that of a flash of mixed-up data below the scrolling region. Therefore, all changes are made during the vertical interval, ensuring that the proper number of lines is consistently displayed because the video procesor cannot ever attempt to execute only part of a shuffle sequence.

Logically the screen still flashes in full screen scrolling, but because the extra last line is displayed beyond the end of the screen, Vertical Blank blanks the display. The shuffle is a two part process, with the two address bytes transferred in separate operations. If the shuffle is not complete before the DMA that accesses the shuffled address starts, the address that gets read may not be valid, and garbage may be displayed thereafter. The random start of the shuffle process relative to the video processor's DMA timing causes this error.

4.7.6 Scrolling Region

A scrolling region may be established on the screen, on a horizontal line basis, within which data may be inserted or lines scrolled without affecting the positions of data outside the region. Only one region may be defined at a time, but it may be repeatedly redefined. Full screen scrolling is a special case in which the region margins and the screen margins are the same. A control sequence defines the region by specifying the line numbers of the top and bottom of the region. When the control sequence arrives, the microprocessor stops taking characters from the silo and waits for the current scroll to end. It then checks the parameters for legality (top less than bottom, bottom less than 14 or 24). If they are bad, the sequence is ignored and the next character is taken from the silo. If they are good, they are stored in locations labelled Top and Bottom. Then starting at the pointer address on the last fill line, the microprocessor sets the fill line's scroll attribute bit to scroll or no scroll (depending on the specification for top margin) and jumps to the end of the addressed line, setting its scroll attribute bit. The microprocessor continues down through the screen RAM until it reaches the point to line #Top, the line that will be at the top of the scrolling region. It sets the attribute bit there to scroll. Jumping down through the region, the microprocessor continues setting line attributes to scroll until it reaches line #Bottom, the bottom line in the scrolling region. From there to the end of the screen it sets the bit to no scroll.

4.7.7 Split Screen Jump Scrolling

When a line feed is received, during the remainder of the current frame the microprocessor rotates LATOFS and prepares for the shuffle. The line number at LATOFS #25 (25 in Figure 4-7-8) moves up to the bottom position in the scrolling region (LATOFS #8). The line at LATOFS #5 (20) moves to LATOFS #25, and all the other lines in the scrolling region of LATOFS are moved up one position. The shuffle buffers are set up. (See Figure 4-7-10.) SHUFAD 1 contains the location of the pointer address at the end of the last line before the scrolling region and SHUFDT 1 contains the pointer address for the new first scrolling region line. SHUFAD 2 contains the location of the pointer address at the end of the new last scrolling region line and SHUFDT 2 contains the pointer address for the first line after the scrolling region.

While the LATOFS and shuffle preparations are underway, data may be coming into the terminal. Data received after the line feed stay in the silo until the LATOFS rotation is completed. Just before rotation, LATOFS 25 points to the number of the next RAM line that data should go to. The microprocessor records that location and then performs the rotation and shuffle preparation. Then it resumes writing the data into the line previously noted. When vertical interrupt occurs, the shuffle is performed and the new line is displayed. If no new line feed is received, data will continue to be written into the same line.

4.7.8 Smooth Scroll

Become familiar with the operation of the scan counter as described in the video processor section (4.6.3.3) before studying this description.

In smooth scroll operation, the VT100 changes the positions of the lines on the screen slowly, so the eye can follow and read the data as it goes by. Instead of moving one character height or 10 scan lines in a single frame, the data moves up or down one scan line in each frame. The smooth scroll rate is thus 6 lines per second at 60 Hz frame rate. Operation is the same for full or split screen smooth scroll. For any given line feed, the effect on the screen is delayed by two frames. Line feeds may queue up so that scrolling is continuous.

Smooth scroll is enabled by a bit in the setup memory that causes the microprocessor to perform all scrolls as smooth scrolls. Whenever a line's scroll attribute bit is set, it receives its scan count from the offset counter. At vertical reset, the scan counter, used for nonscrolling lines, always resets to zero, but the offset counter is loaded with the contents of the scroll latch. The microprocessor loads the scroll latch with an offset value. If a jump scroll is involved, the offset is always zero. If a smooth scroll is involved, the microprocessor loads an offset value according to the number of frames that have passed since the line began moving.

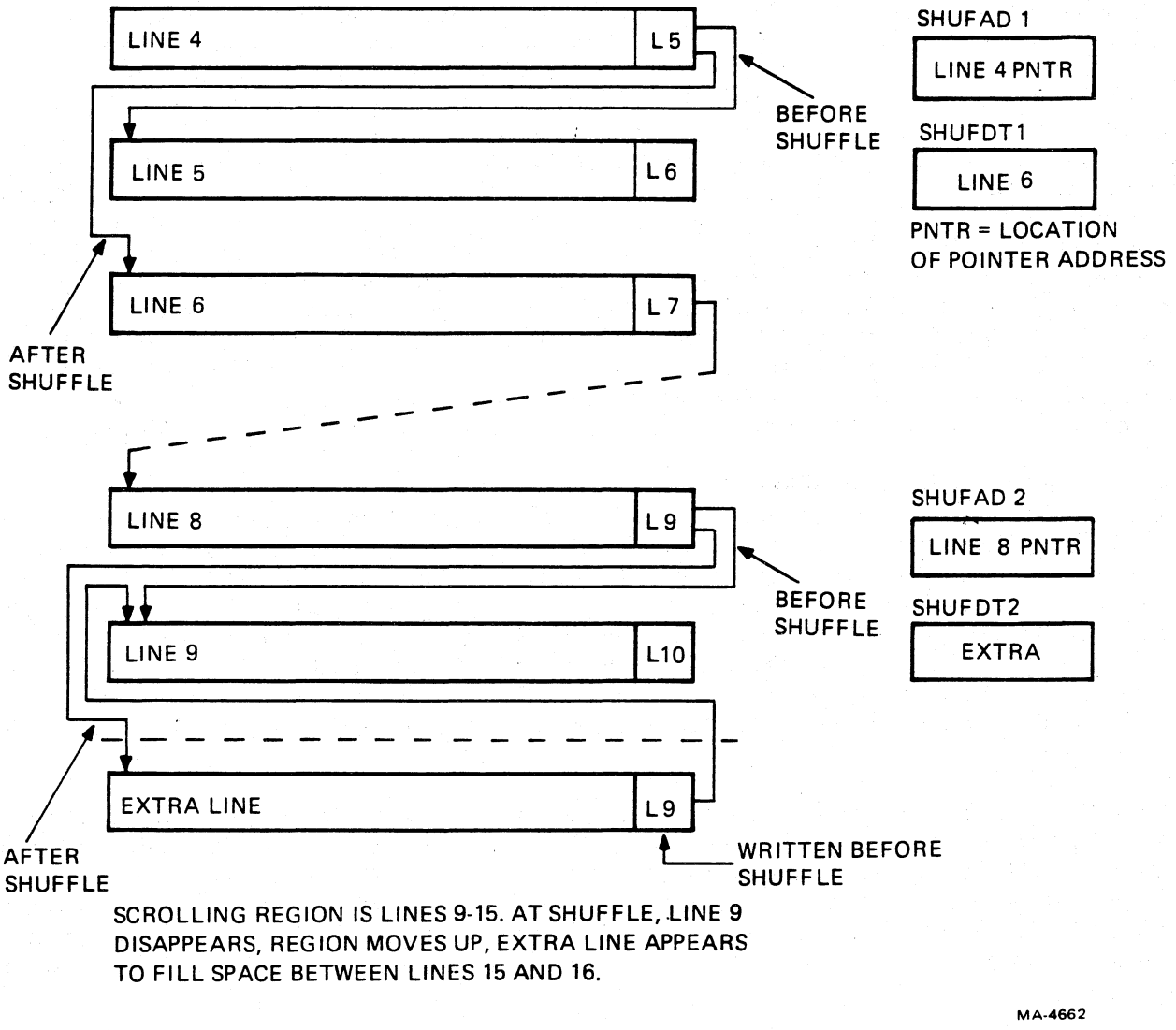


Figure 4-7-10 Split Screen Address Shuffle

When a line feed is received the microprocessor waits for the current scroll to end. It sets an internal scroll-pending flag. Then, at the next vertical interrupt, during the frame before scrolling begins, the shuffling process makes its preparations but only to add the 25th line to the display. During smooth scrolling, all the lines will be visible together. The microprocessor, which keeps count of the number of frames in the scroll, loads the scroll latch in the DC012 with an offset value of one. Then, when the second vertical interrupt occurs, the microprocessor performs the address shuffle, the offset counter receives the 1 from the scroll latch, and the microprocessor loads the scroll latch with 2. As the frame begins, the character generator ROM, driven by the offset counter, displays its second scan row on the top line of the scrolling region. The rest of the scrolling region is moved up by the same amount, so the last scan in the scrolling region is the top scan of the 25th line.

Succeeding frames contain the data moved up scan by scan as the microprocessor loads the scroll latch with larger offset values each time. During the ninth such frame, only one scan from the top line and nine scans of the bottom line are visible. The microprocessor loads 0 into the scroll latch. If the

microprocessor made no other change, then on the next frame, the data which had been moving slowly up would jump back down to its original position. Therefore, another address shuffle is performed at vertical reset. The top line of the scroll region is discarded and the 0 offset applies to the former second line. The old top line is erased and becomes the new 25th line that will appear in the next scroll.

4.7.9 Split Screen Smooth Scrolling

In a split screen smooth scroll, the scan count to the character generator ROM must switch between the normal scan counter and the offset counter. (Please remember that full screen scroll is a special case scrolling region, and that jump scrolling is a special case offset count of 0.) The scrolling attribute bits, which were set when the control sequence that defined the region arrived, operate the counter multiplexer (MUX).

Refer to Figure 4-7-11 and suppose that the smooth scrolling region extends from line 5 to line 8. The scroll is shown at its midpoint. The scrolling attribute bits at the ends of lines "Fill" through three define lines one through four to be outside the scrolling region. Each line's DMA has occurred when the scan counter, which always starts together with the top scan on the screen, is equal to zero. A DMA always occurs:

1. when the counter in use (MUX output) is zero, or
2. when the MUX first selects the offset counter.

The offset counter is loaded with its offset at vertical reset. The switch between scan counter and offset counter may only occur when the scan counter (NOT the MUX output) is zero.

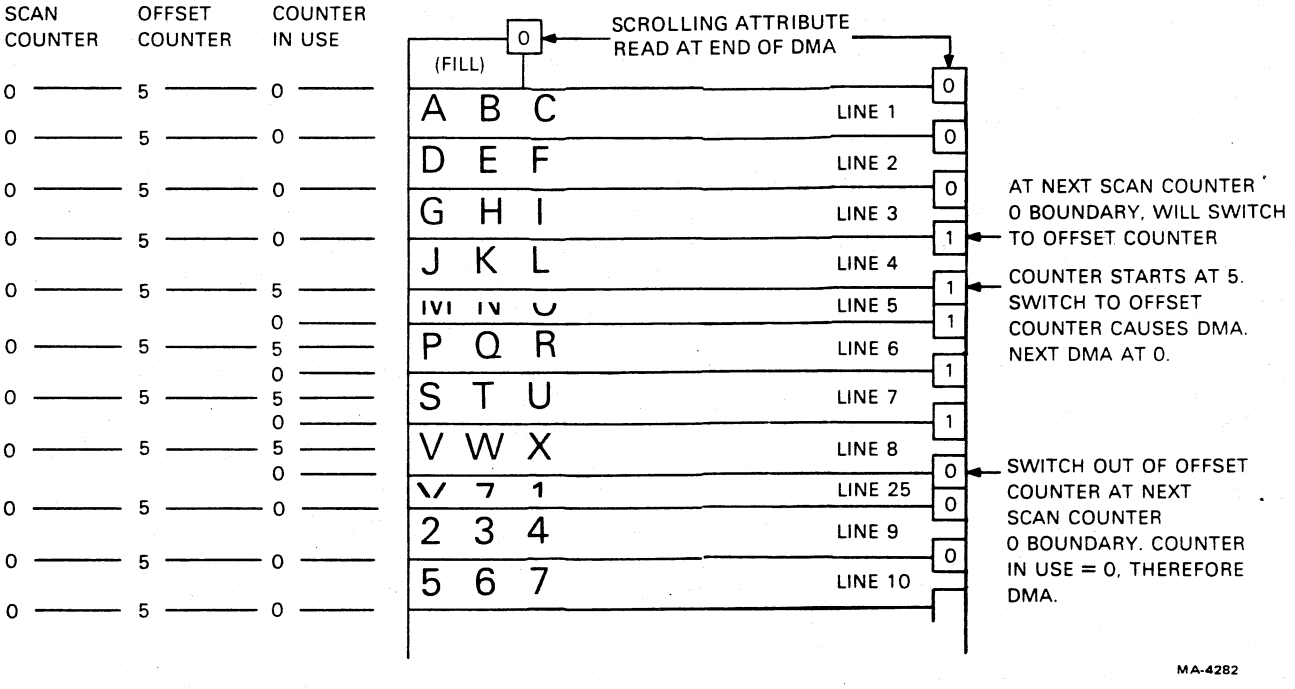


Figure 4-7-11 Split Screen Smooth Scroll at Midpoint

The scrolling attribute bit on line 4 enters the DC012 during the DMA. However, it does not cause the MUX to switch until scan 0 of the next line. Because of the switch to the offset counter, line 5 begins with a DMA but it starts displaying with scan 5 because of the offset counter. Its attribute bit enters the DC012 at the end of the DMA. Five scans later the counter in use is 0, so another DMA occurs. Because the scan counter did not reach 0 before the DMA, the scrolling attribute bit from line 5 is ignored. Line 6 DMAs and its attribute bit enters the DC012. Line 6 is present for all 10 scans and so as the scan counter passes through zero, the DC012 accepts control from the line 6 attribute bit.

This special case (pointer to the second line in the scrolling region while the smooth scroll is in progress) is the only occasion when an attribute bit is ignored. The double height and width bits in the same byte are accepted at the moment the DMA for the corresponding line begins.

As line 5 begins to roll off the screen, the extra line in memory, line 25, becomes visible. It becomes the new line 8 when line 5 is gone. Line 25 carries a non-scroll attribute bit because the next line (which the address on line 25 points to) is not in the scrolling region. Line 25 was DMA'd in when the counter in use was 0 so it starts with its top scan. But the attribute bit is accepted when the scan counter reaches 0 five scans later. Now the counter in use is 0 again because of the shift back to the scan counter so another DMA occurs, bringing in line 9, which also carries a non-scroll attribute bit. The rest of the screen thus appears in non-scroll fashion.

4.7.10 Cursor

The microprocessor keeps a running account of the cursor position. It starts at the reset position, line 1 - column 1 (top left corner) and responds to any change in position that might result from receiving a new character, a cursor position command, a line feed, etc. The microprocessor calculates the appropriate screen RAM address from the combination of previous line and column plus change in position, or from the specified line and column in a direct cursor address (DCA) control sequence. The microprocessor then records the current setting of the base attribute bit of the character at that address and then periodically inverts the attribute bit, showing the operator that the cursor is located at the spot on the screen where the attribute appears and disappears.

When a line scrolls on the screen, its location in RAM remains the same. To keep the cursor at the same screen location as before, representing the cursor moving down through the lines, the microprocessor calculates a new address for the cursor at the same column number but in the RAM location corresponding to the next line. Then, after resetting the attribute at the old location to its original value, it records and then toggles the attribute bit at the new location.

The attribute bit that the microprocessor toggles and the appearance on the screen depend on the setup selection of the cursor attribute and on the absence or presence of the AVO. If the AVO is not installed, the microprocessor toggles the eighth bit in each character word. A setup selection of reverse video causes the microprocessor to set the DC012 to interpret its base attribute input (REV VID H) as reverse video. If setup specifies that underline is to be used for the cursor, the DC012 is set to interpret the base attribute as underline instead of reverse. Notice that without the AVO the cursor selection determines the appearance for all characters on the screen that have the attribute asserted. Furthermore, the microprocessor will accept the commands for either reverse or underline to assert the attribute.

With the AVO present, the microprocessor tells the DC012 to interpret the base attribute as reverse video. The cursor selection in setup determines whether the microprocessor toggles the base attribute bit (eighth character bit) to get reverse video or one of the bits in the AVO RAM to get underline. With the AVO present, cursor selection is independent of attributes and all attributes are available at the same time.

4.7.11 SET-UP

The SET-UP area is a portion of the scratch RAM. It contains 8-bit bytes that are passed between the RAM and the NVR. Here is a list of the SET-UP area contents. This list is subject to change.

22 bytes	Answerback message (20 characters and 2 delimiters)
17 bytes	Tabs encoded in bits
1 byte	80/132 column mode
1 byte	Intensity
1 byte	Mode byte for PUSART
1 byte	On-Line/Local
1 byte	Switchpack 1 (scroll, autorepeat, screen, cursor)
1 byte	Switchpack 2 (bell, keyclick, ANSI/VT52, XON/XOFF)
1 byte	Switchpack 3 (US/UK #, wrap, new line, interlace)
1 byte	Switchpack 4 (parity sense, parity, bits/char, power)
1 byte	Switchpack 5 (STP – visible only when option installed)
1 byte	Transmit baud rate
1 byte	Receive baud rate
1 byte	Parity
1 byte	Checksum for NVR

When the SET-UP key is pressed, the SILO locks and any scroll in progress is allowed to finish. Now the 25th line (Extra) is available for one of the lines at the bottom of the screen. Another 135 bytes are available as line Extra2 for use as the other of the two bottom lines, or for the NVR buffer area and the "Wait" message displayed during NVR operations. Another 125 bytes are the SET-UP screen RAM. They store the words "SET-UP A" twice (for double height) and the words "To exit press SET-UP" with the three lines' terminator and address bytes, plus 19 more terminators and addresses for the 19 blank lines in the middle of the SET-UP screen.

For SET-UP A, the microprocessor performs a routine to fill the line at the bottom of the screen with a ruler. The other free line displays the cursor and letters "T" to indicate tab positions. Then the microprocessor counts from the beginning of the tab bytes in the SET-UP area to find the bit corresponding to the column number where the cursor is. If the bit is set, the microprocessor writes the letter "T" in the current cursor position. Keys (Set/Clear Tab, Clear All Tabs) on the keyboard can toggle the setting of the bit in the SET-UP area, and the microprocessor writes or erases the "T" to agree.

For SET-UP B, the microprocessor displays the data contained in the switchpack and baud rate area by writing corresponding information into the bottom line. Switchpack 5 is only displayed if the Option Present flag is asserted at the STP. The other free line is not written into but is used to display the cursor position and to display the answerback message when the message is being entered. The switchpack data is changed by a key on the keyboard (Toggle 1/0).

The non-switchpack data is changed by separate keys. These include parameters that display themselves – line/local (displayed in the LEDs) and 80/132 column, seen on the screen. Transmit and receive are displayed numerically as is parity in later models. Switching between SET-UP fields and starting Reset can also be done with separate keys on the keyboard.

4.8 MONITOR

Two monitors have been used in VT100 prodection. Early VT100s used DEC part number 30-14590. Later terminals used DEC part number 30-16080. Most of the circuitry in these monitors is standard television technique, and this description simply highlights the signal path. An overview of the general principles of the horizontal section is included because this circuit is not intuitively understandable from an examination of the schematic. It is also the likely candidate for failure because of high stresses in the components.

4.8.1 Monitor Description: 30-16080 (Elston)

4.8.1.1 Video Driver – The cathode driver stage gets its operating supply of 38 volts from a winding of the flyback transformer. R108 is the collector load resistor. C101 bypasses the emitter resistor to improve high frequency response. The stage is intended to be biased by the driving circuit (direct video out in the terminal controller). R105 couples the video signal to the cathode limiting current flow if the CRT arcs.

4.8.1.2 Brightness – The brightness control circuit gets its –150 volt operating supply from the horizontal output circuit. A charge pump (C104, C105, CR103, CR104) produces a large negative voltage by inverting the large positive swings in the stage. The brightness voltage returns to the +38 volt video output power supply, rather than ground, to allow the brightness control output to vary from –42 to +17 volts. The brightness control potentiometer R109 varies the bias on the first grid of the CRT. C107 bypasses currents resulting from internal CRT arcs from the high voltage anode and also bypasses video signals from the grid to ground.

4.8.1.3 Vertical Oscillator – The vertical oscillator receives its synchronizing drive through inverter-buffer Q298. R331 and C314 are a low pass filter on the input for noise immunity. The input is ac-coupled so that if the drive stops in either a high or low state, the circuit can self-oscillate to keep the beam moving on the CRT.

Basically, the oscillator is an RC timer with R333 and R334 through CR304 charging a capacitor made of C318 and C319 in series. As the voltage across the capacitor rises, emitter follower Q309 drives the output amplifier Q310 so that its collector current rises at the same rate. CR304 is two diode drops to compensate for the drops in Darlington Q309 so the voltage at the base of Q310 is the same as the voltage at the top of C318. When Q308 receives a vertical drive pulse, it discharges the capacitor.

R341 and R342 are positive feedback to the junction of C318 and C319. As Q310's emitter voltage rises with increasing current, the two resistors couple that voltage back to the timing capacitor. This makes the voltage across the capacitor rise faster than it would with only the charging current from R333 and R334. But because the rise in capacitor voltage causes Q310 to turn on more, the feedback voltage increases as well. The exponential rise in Q310's output current that results closely matches the variations in L301's current. This is explained more under Linearization (Paragraph 4.8.1.6).

4.8.1.4 Self-Oscillation – If the vertical circuit does not receive a drive signal, it oscillates by itself to keep the electron beam moving to prevent a phosphor burn. The self-oscillation period is longer than the period between vertical drive pulses so the drive pulses, when present, always control the vertical scanning rate.

Without a drive signal, Q308 is off. The regular RC circuit produces a rising voltage at the base of Q310. While Q310's output moves the electron beam, its base voltage is coupled to Q308 through R335 and CR302. When the voltage rises above the diode drops of CR302 and Q308 base-emitter junction, Q308 turns on, discharging the timer and cutting off Q310. The retrace voltage that forms at L301 is coupled by R344, C316, and R339 back to Q308 to keep it on long enough to complete a retrace even though the voltage from Q310's base (that started the cycle) has started to decrease. After the voltage at L301 falls (due to current flow to the yoke), the drive to Q308 is gone, Q308 turns off, and the self-oscillation cycle begins again.

4.8.1.5 Vertical Output – Consider L301, which is a large inductor, to be a constant current source. Assume that the yoke starts with a current that deflects the beam to the top of the screen, and Q310 is off. The current flows out of L301 through C321 and into the yoke. Q310 now turns on with a gradually rising voltage on its base. Q310 thus draws an increasing amount of current from the junction of L301 and the yoke. Because L301's current is relatively constant, this means that less current is avail-

able for the yoke, so as Q310's current increases, the yoke's current decreases. Eventually Q310 passes all of L301's current and the yoke current is 0 with the beam in the center of the screen. As the current in the collector of Q310 increases further, the current in the yoke reverses and adds to the current coming from L301. This opposite current deflects the beam toward the bottom of the screen. Now the vertical drive pulse turns Q310 off, and L301 produces a large positive voltage to try to maintain its constant current. This voltage rapidly reverses the current in the yoke and makes the beam return to the top of the screen very fast. Q310 turns back on and the cycle repeats.

C320, R338, and R340 limit the voltage across L301 during vertical retrace.

4.8.1.6 Linearization – Because L301 is not an infinitely large inductor, it is not a perfect current source. Current through it decreases gradually until the beam reaches the center of the screen and then increases again toward the end of the cycle. This non-ramp component of the current would cause character height to vary from top to bottom if allowed to pass to the yoke. The exponential drive to Q310 as a result of feedback causes Q310 to accept the varying current from L301 at the same time that a ramp current through the yoke is maintained.

4.8.1.7 Horizontal Driver – The horizontal driver receives a TTL level drive pulse from the terminal controller. R468 limits the base current to Q413. C435 provides noise immunity for the drive input.

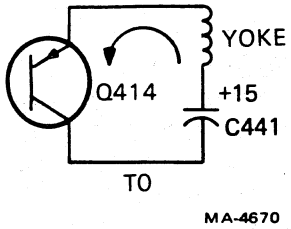
When the input is high, Q413 is on. With pin 6 of transformer T403 pulled low by Q413, and with about half the supply voltage at pin 4, there is approximately 6 volts across the primary winding 4-6. The secondary winding 3-2 sees one quarter of this voltage across itself due to the 4:1 turns ratio, but no current flows because Q414's base-emitter junction is reverse biased. Meanwhile, current increases through winding 4-6 while Q413 is on, storing energy in T403's core. When the drive signal falls, turning Q413 off, winding 3-2 reverses polarity. Current now flows from T403 winding 3-2 through Q414's base-emitter junction, Q414 saturates, and the horizontal output functions as discussed below.

When the drive signal goes high again at the beginning of horizontal retrace, Q414 needs to turn off very quickly to minimize dissipation. The purpose of opposite polarities in T403 is to force Q414 off by turning Q413 on. When Q413 turns on, winding 3-2 reverses polarity again and this voltage forces Q414's base-emitter junction into a reverse biased state, rapidly discharging Q414's stored base charge and cutting off Q414's collector current.

R470 limits the peak current through Q413. R470, and R471 (if present), limit the on time of Q414. C443 (if present) speeds up the turn-off of Q414. C436 limits the peak voltage that develops across Q413 caused by leakage inductance in the primary of T403 that prevents complete coupling of the primary energy into the secondary. C437 filters Q413's power supply.

4.8.1.8 Horizontal Deflection Operation – The horizontal output circuit consists basically of Q414, CR406, C438, C441, and the horizontal deflection yoke. Assume that the beam is at the center of the screen during a scan. Refer to the waveform diagram (Figure 4-8-5) for reference points T0 through T4.

Figure 4-8-1 Horizontal Deflection Current – T0

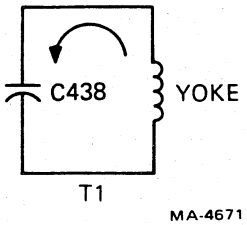


T0: Right Half of Scan (Figure 4-8-1)

Initial Condition: Current through the yoke is zero. C441 is charged to +15 volts. Q414 is on.

Action: Current now flows out of the yoke through Q414, pushed by the voltage across C441. The voltage across C441 is nearly constant so the current through the yoke's inductance increases linearly. As the current increases, the beam moves to the right of the screen. The magnetic field building in the yoke stores energy.

Figure 4-8-2 Horizontal Deflection Current – T1

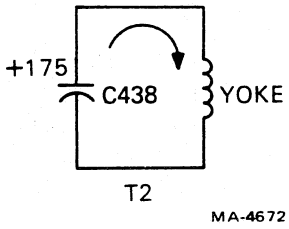


T1: Start of Retrace (Figure 4-8-2)

Initial Condition: Current out of the yoke is maximum. Q414 is switched off. C438, which had been grounded by Q414, has 0 volts across it.

Action: Current continues to flow out of the yoke by inductive inertia as the stored magnetic field collapses. C438, which is a small valued capacitor, quickly charges to a high voltage. This voltage opposes current flow and causes a rapid reduction in current. The beam quickly returns to the center of the screen.

Figure 4-8-3 Horizontal Deflection Current – T2

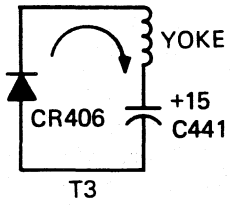


T2: Middle of Retract (Figure 4-8-3)

Initial Condition: Current through yoke is zero. C438 is charged to +175 volts.

Action: The high voltage across C438 causes a rapid rise in current into the yoke. The beam moves to the left of the screen.

Figure 4-8-4 Horizontal Deflection Current – T3



T3: Start of Scan (Left Half) (Figure 4-8-4)

Initial Condition: Current into the yoke is maximum. C438 is discharged.

Action: Inductive inertia makes the top of the yoke slightly negative, forward biasing CR406 to provide a return path for current out of the bottom of C441. The yoke current gradually decreases as the magnetic field collapses and discharges into C441 against the voltage across C441. The beam moves to the center of the screen.

T4: Return to T0

4.8.1.9 Horizontal Output Circuit – (Refer to Figure 4-8-5.) L403 adds a variable inductive reactance that controls current in the circuit to vary the scan width. L402 is a magnetically biased inductor whose reactance varies nonlinearly with changes in yoke current. This, with R481 and C442, provides correction for nonlinearity caused by the decaying exponential rate of current increase in the yoke caused by the yoke's resistance. It does this by allowing more voltage across the yoke at the end of the scan. This is needed because as current increases, the voltage drop increases across the resistance of the yoke, tending to reduce the rate of current increase.

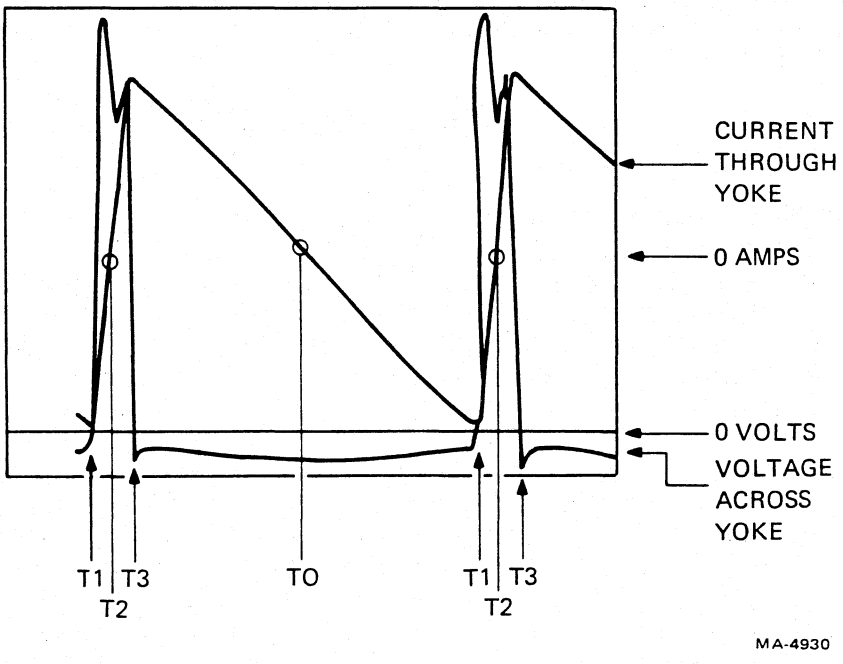


Figure 4-8-5 Horizontal Deflection Waveforms

Power enters the circuit through the primary of the flyback transformer. CR408 and C439 work with an autotransformer winding on the primary to boost the stage's operating voltage to +15 volts. The output circuit shuttles yokvbe current back and forth between C438 and C441, losing only a small amount of power in resistive losses. Therefore, the average current through the flyback primary is small (approximately 800 mA). C438 is relatively small so that the voltage drop across its reactance can provide "S" correction for the horizontal scan. This compensates for the difference between the arc of the tube face and the arc of the beam's deflection. Each time Q414 turns off, a 175 volt pulse, lasting the interval of horizontal retrace, appears at the dotted end of the flyback primary. This pulse passes into the flyback secondary to provide high voltages for the CRT.

4.8.1.10 High Voltage and Focus – When the 175 volt pulse appears on the flyback primary at retrace, the flyback secondary produces 12 kV which is rectified by CR407 and filtered by the capacitor made by the aquadag (graphite) coatings on the inside and outside of the CRT's glass envelope. Screen and focus grid voltages of about 370 volts come from a lower voltage winding on the flyback and are rectified by CR409. For the cathode driver, 38 volts comes from another winding and is rectified by CR102.

4.8.2 Monitor Description: 30-14590 (Ball)

4.8.2.1 Video Amplifier – The video amplifier consists of Q101 and its associated circuitry. The incoming video signal is applied to the monitor through J101-8 and R101 to the base of Q101.

Transistor Q101 has a nominal gain of 15, and operates as a class B amplifier. Q101 remains cut off until a dc-coupled, positive-going signal arrives at its base and turns it on. R103 provides series feedback that makes the terminal to terminal voltage gain relatively independent of transistor parameters and temperature variations. R102 and C101 provide emitter peaking to extend the bandwidth to 12 MHz.

The negative-going signal at the collector of Q101 is direct coupled to the CRT cathode. The class B biasing of Q101 allows a large video output signal to modulate the CRT's cathode and results in a maximum available contrast ratio.

Overall brightness of the CRT screen is also determined by the negative potential at its grid which is varied by the brightness control.

4.8.2.2 Vertical Deflection – Q102 is a thyristor used as a programmable unijunction transistor and with its external circuitry forms a relaxation oscillator operating at a vertical rate. The sawtooth forming network consists of A101, C103, and C104. These capacitors charge exponentially until the voltage at the anode of Q102 exceeds its gate voltage at which time Q102 becomes essentially a closed switch, allowing a rapid discharge through L101. The rate of charge or frequency is adjustable by A101. The oscillator is synchronized by a negative pulse coupled to its gate from the vertical drive pulse applied externally at J101-9.

A divider network internal to A101 sets the free running frequency by establishing a reference voltage at the gate. This programs the firing of Q102 and amounts to resistive selection of the intrinsic standoff ratio. Frequency is controlled by passive components only. CR101 provides temperature compensation for Q102 while controlling the gate impedance to allow easy turn on and off of Q102. L101 forms a tuned circuit with C103 and C104 during conduction of Q102 which provides a stable control on the dropout time of Q102 to assist in maintaining interlace. Q103 collector to base forward diode clamping action prevents the voltage from swinging too far negative during this flywheel action.

The sawtooth at the anode of Q102 is direct coupled to the base of Q103. This stage functions as a Darlington pair emitter follower driver for the output stage Q104. It presents an extremely high impedance in shunt with A101 and prevents the Beta dependent input impedance of Q104 from affecting the frequency of the sawtooth forming network.

Linearity control of the sawtooth is accomplished by coupling the output at Q103 emitter resistively back into the junction of C103 and C104. This provides integration of the sawtooth and inserts a parabolic component. The slope change of the sawtooth at Q103 output is controlled by the setting of A102. The output at Q103 is coupled into a resistive divider.

Height control R110 varies the amplitude of the sawtooth voltage applied to the base of Q104 and controls the vertical raster size on the CRT. C105 limits the amplitude of the flyback pulse at Q104 collector.

The vertical output stage Q104 uses an NPN power transistor operating as a class AB amplifier. The output is capacitively coupled to the yoke. L1 provides a dc connection to B+ for Q104. It has a high impedance compared to the yoke inductance that causes most of the sawtooth current of Q104 to appear in the yoke. R114 prevents oscillations by providing damping across the vertical yoke coils.

4.8.2.3 Horizontal Deflection

4.8.2.3.1 Low Level Stages – The purpose of Q105 and Q106 is basically to process the incoming horizontal drive signal into a form suitable to drive the output stage Q108. The duty cycle of Q108 becomes essentially independent of the amplitude and pulse width of the drive pulse. This is a necessary condition to assure stability and reliability in the output stage. In addition, these stages provide a horizontal video centering adjustment by delaying retrace with respect to the horizontal drive pulse.

The drive pulse is presented to Q105 via J101-6. The base circuit of Q105 includes a clamp and a differentiator that makes Q105 output insensitive to drive pulse amplitude and width changes. The only requirement is that pulse amplitude be of 2.5 volts minimum and pulse width should be 10 to 40 microseconds. Q105 with Q106 functions as a monostable multivibrator with Q107 being a slave that provides a positive feedback. Specifically, when Q105 is turned on by the drive pulse, it discharges C112 at a rate determined by the setting of A103. When C112 is discharged to 1.75 volts, Q106 turns off. This change of state turns Q107 on and the base drive to Q106 from R128 is shunted through Q107. Q106/Q107 remains in this state for nominally 25 microseconds until C112 recharges through A103 to 8.25 volts. At this time, Q106 is biased on again by the current through A103. The multivibrator is now in a state in which Q106 is on and Q105/Q107 is off. It remains in this state until the next drive pulse occurs or power is turned off. C112 is the only timing capacitor in the circuit and has two time constants associated with it. Primarily, the charge path between pin 1 and pin 3 of A103 determines the on time of Q107. The discharge path through the video centering control and Q105 determines the delay between application of the drive pulse and the start of retrace (turn on of Q107).

4.8.2.3.2 High Level Stages – These stages consist of Q107 driving the output stage, Q108, and its associated circuitry through T101. Q107 is an inverting slave of Q106 and is driven alternately into saturation and cutoff as are all stages in the horizontal circuit. Q107 output is transformer coupled to the output stage with phasing of T101 chosen such that Q108 turns off when Q107 turns on. This allows Q108 to turn off quickly, thus minimizing dissipation. A careful review shows that Q108 turns off at a variable delay time after receipt of the drive pulse. This action causes retrace to begin.

During conduction of the driver transistor, energy is stored in the coupling transformer. The polarity at the secondary is then phased to keep Q108 cut off. As soon as the primary current of T101 is interrupted due to the base signal driving Q107 into cutoff, the secondary voltage changes polarity. Q108 now saturates due to the forward base current flow. This gradually decreases at a rate determined by the transformer inductance and circuit resistance. However, the base current is sufficient to keep Q108 in saturation until the next polarity change of T101.

The horizontal output stage has two main functions:

1. to supply the deflection coil with the correct horizontal scanning currents and

2. to develop high voltage for the CRT anode and dc voltage for the CRT bias, focus, and accelerating grids, as well as the dc voltage for the video output stage.

Q108 acts as a switch that is turned on or off by the rectangular waveform on the base. When it is turned on, the supply voltage plus the charge on C123 causes deflection current to increase in a linear manner and moves the beam from near the center of the screen to the right side. At this time, the transistor is turned off by a polarity change of T101 that causes the output circuit to oscillate. A high reactive voltage in the form of a half cycle negative voltage pulse is developed by the deflection coil inductance and the primary of T2. The peak magnetic energy that was stored in the deflection coil during scan time is now transferred to C122 and the deflection coil distributed capacity. During this cycle, the beam is returned to the center of the screen.

The charged capacitances now discharge into the deflection coil and induce a current in a direction opposite to the current of the previous part of the cycle. The magnetic field thus created around the coil moves the scanning beam to the left of the screen.

After slightly less than half a cycle, the decreasing voltage across C122 biases the damper diode CR111 into conduction and prevents the flyback pulse from further oscillation. Magnetic energy that was stored in the deflection coil from the discharge of the distributed capacity is now released to provide sweep for the left half of scan and to charge C123 through the rectifying action of the damper diode. The beam is now at the center of the screen. The cycle repeats as soon as the base of Q108 becomes positive with respect to its emitter.

C123 serves to block dc current from the deflection coil and to provide "S" shaping of the current waveform. "S" shaping compensates for stretching at the left and right sides of the picture tube because the curvature of the CRT face and the deflected beam do not follow the same arc.

L103 is an adjustable width control placed in series with the horizontal deflection coils. The variable inductance allows a greater or lesser amount of deflection current to flow through the horizontal yoke and varies the width of the horizontal scan.

Linearity control is provided by modifying the deflection coil voltage. During retrace, an auxiliary winding on the flyback transformer supplies a pulse that charges C119 through rectifier diode CR112 and L102. This voltage is then applied in series with the deflection coil when the damper diode turns on at the start of trace. The voltage is sawtooth shaped and has the effect of decreasing the deflection coil current as a function of the sawtooth shape. This compensates for the stretch normally found on the left side of the screen due to the deflection coil and system RL time constant. Linearity is optimized by adjustment of L102 that acts as an impedance to the pulse from T2.

The negative flyback pulse developed during horizontal retrace time is rectified by CR110 and filtered by C117. This produces approximately -130 Vdc which is coupled through the brightness control R117 to G1 of the CRT.

This same pulse is transformer-coupled to the secondary of T2 where it is rectified by CR2, CR113, and CR114 to produce rectified voltages of approximately 12 kV, 400 V, and 32 V respectively. 12 kV is the anode voltage for the CRT, 32 V is used for the video output stage, and the 400 V source is used for G2 and G4 voltages for the CRT.

4.9 POWER SUPPLY

The VT100 series power supply is a switching supply that has 95 watts capacity with four separate voltage outputs. Figure 4-9-1 is a block diagram of the power supply.

4.9.1 Power Input

The input to the supply consists of an electromagnetic interference (EMI) filter, an on/off switch, a fuse, and a 120/230 volt select switch. Either on 120 Vac or 230 Vac input, thermistors R1 and R50 reduce the start-up inrush currents to safe levels. For 120 Vac operation a voltage doubler rectifier is used; for 230 Vac operation a full wave bridge rectifier is used. The storage voltage across both C9 and C14 varies with the input line voltage from 200 to 360 Vdc. R19 and R20 are bleeder resistors.

4.9.2 Start-Up Circuit

Transformer T2 is a start-up transformer that supplies the power to start the control circuit. The ac voltage on the primary of T2 is stepped down, rectified, and filtered by C33. The dc voltage is applied to the input of +12 volt regulator Z2. The output passes through two diodes D24 and D25 to the control circuitry. When the unit is turned on, the only voltage supplying power to the control circuit is from the regulator Z2. After the outputs come up, the +12 output is fed back through diode D34 to the control circuitry. This voltage, being higher than that delivered by the start-up circuit, will back bias D24 and D25, isolating the Z2 regulator. This scheme of returning the output through D34 enables the power supply to also meet its ride-through specification (ability to supply power during brief outages).

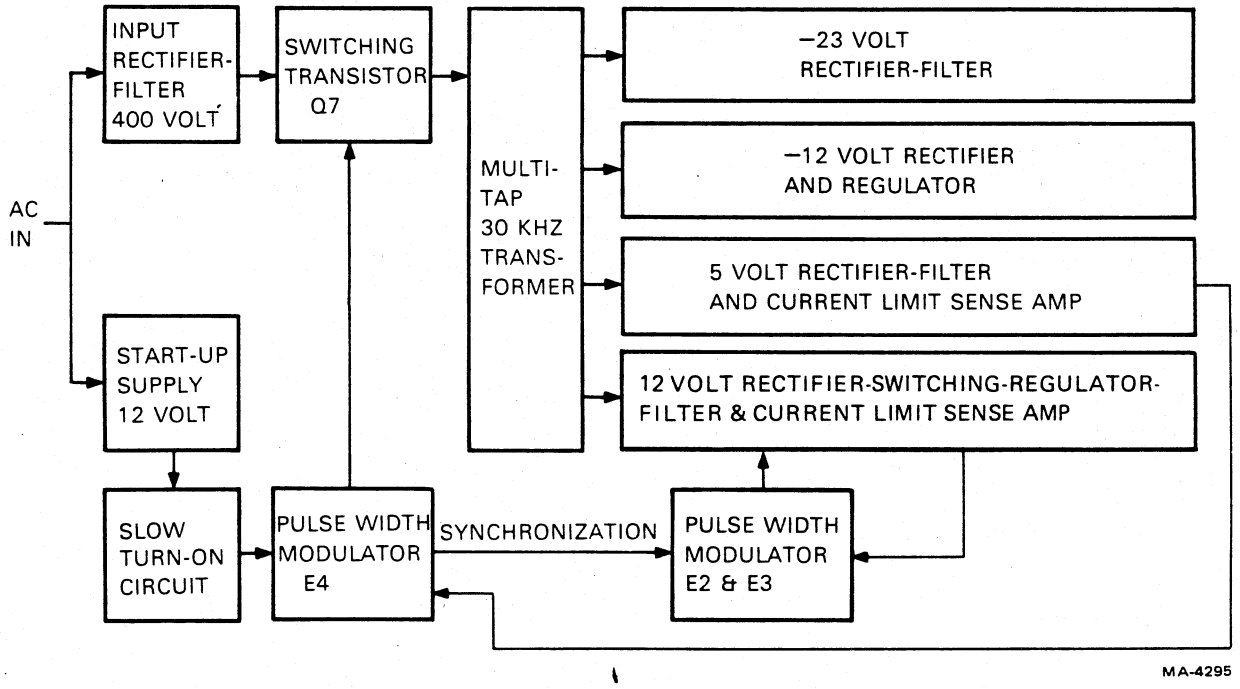


Figure 4-9-1 VT100 Power Supply Block Diagram

4.9.3 Control Circuit

The control circuit in the VT100 power supply is designed around the 3524 pulse width modulator (PWM) IC. It houses a voltage reference, error amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switcher, current limit circuit, and a shutdown circuit. Refer to the regulator IC block diagram in Figure 4-9-2 and the power supply timing diagram in Figure 4-9-3.

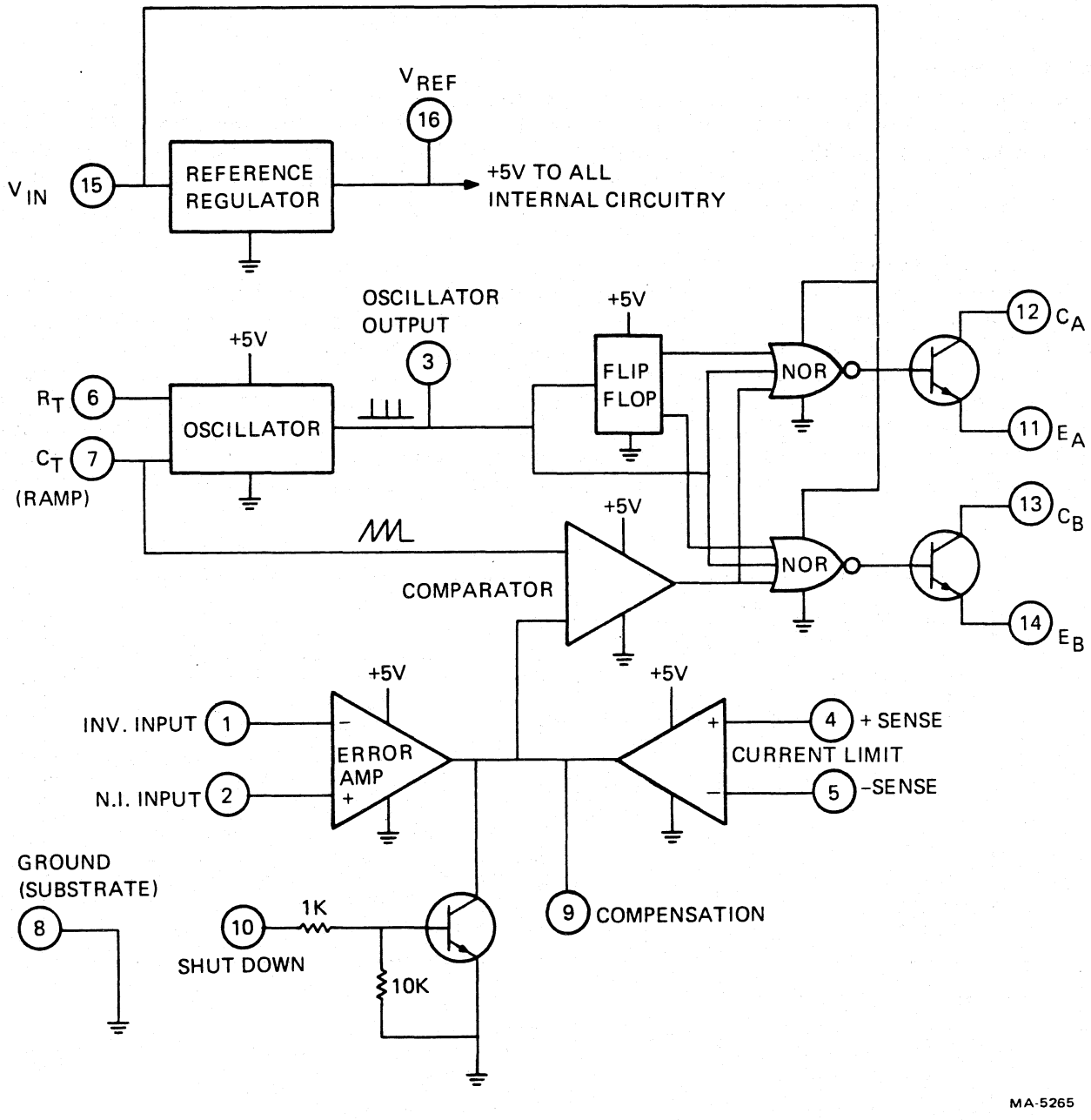


Figure 4-9-2 3524 Regulator Block Diagram

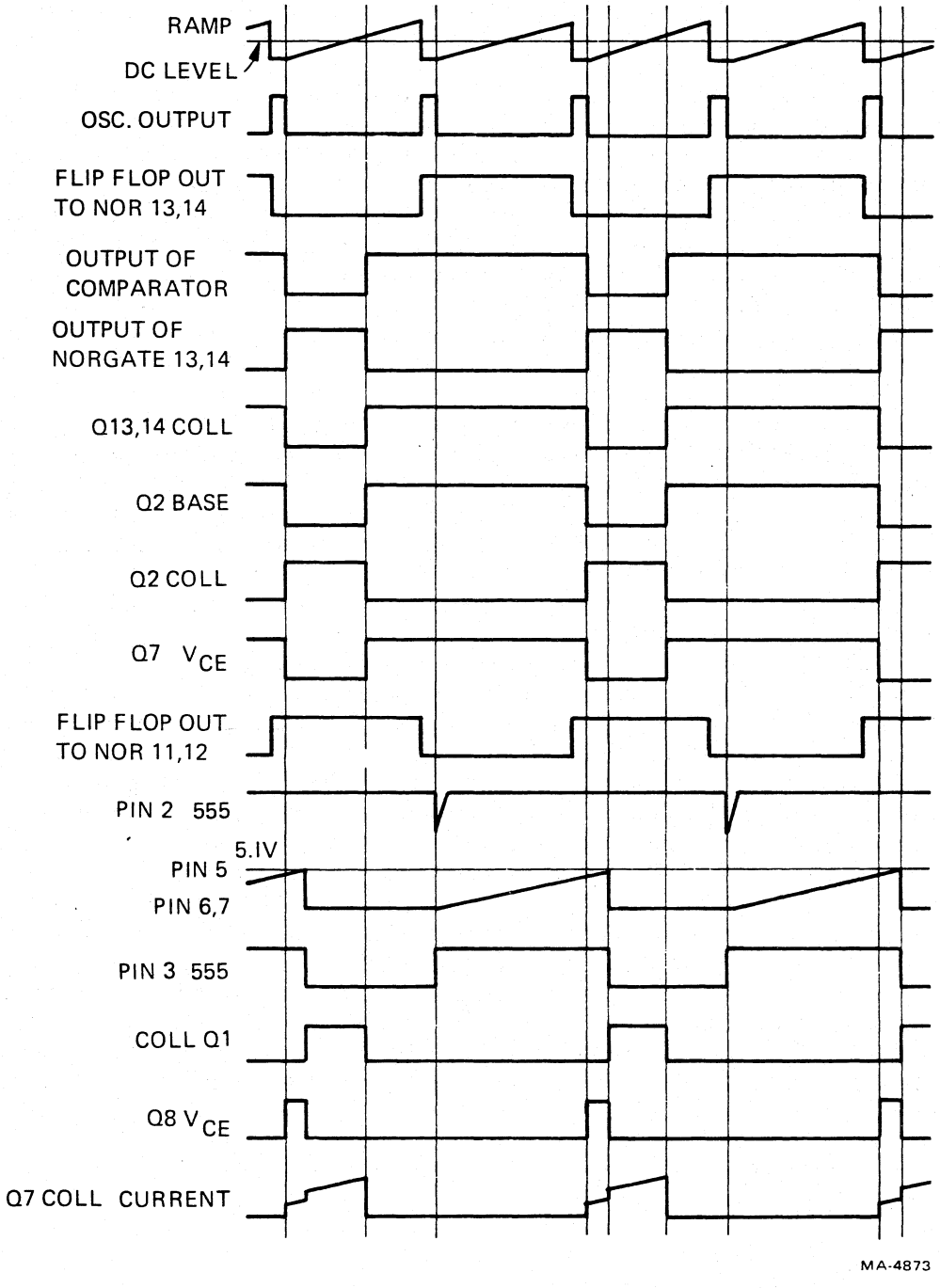


Figure 4-9-3 Power Supply Timing Diagram

The oscillator frequency is determined by resistor R18 and C7. The ramp generated by C7 is used as a reference for the comparator. The discharge time of C7 determines the pulse width of the oscillator output pulse. This pulse is used as a blanking pulse to ensure that the outputs of the 3524 cannot turn on simultaneously. Capacitor C5 ensures that the blanking pulse is wide enough.

The error amplifier in the 3524 is a transconductance amplifier with an output (pin 9) impedance of approximately 5 megohms. Pin 9 is a convenient point to place the compensation network, R30, C17 and R13. It is also an ideal point at which to turn off the switching regulator and also to put the slow-turn-on circuit. The slow-turn-on circuit consists of D39, R51, D40, and C34. When the power supply is initially turned on, pin 9 is pulled to ground by C34 through D39. As C34 charges slowly and exponentially, pin 9 follows, turning the power supply on slowly and exponentially. The current that charges C34 comes from pin 9 and the +12 volt start-up. Pin 9 operates at a dc level that is determined by the input error voltage into the amplifier. C34 eventually charges to +12 volts, thus back biasing D39. When the supply is turned off, C34 discharges through D40, allowing the supply to be ready for another soft start.

The inverting side (pin 1) of the input to the error amplifier is tied to the +5 volt output through a dividing network, R32 and R48. The noninverting side (pin 2) is referenced to a 5.1 volt zener, D38, through a divider network, R41 and R49. An error appearing at the input causes pin 9 (output of the error amplifier) to shift. This dc level shift is tied into an input of a comparator. As mentioned earlier, the ramp generated by C7 is tied into the other input of the comparator. This is the means by which the regulator is pulse width modulated. The actual frequency of the oscillator is 60 kHz. The switching frequency of the power supply is one-half that of the oscillator, 30 kHz, because only one of the single-ended outputs is used. This output, pin 13, a pulse width modulated wave, turns transistor Q4 on and off. When Q4 is off, Q3 supplies base current to Q2, turning it on. D7 and D8 are antisaturating diodes. R14 limits the base drive, and R15 and C4 are a speed-up circuit to turn Q2 on and off fast. When Q2 is on, Q7 (high voltage switch) is off. Current flows from +12 through R11, D6, and winding 5,6 of pulse transformer T3 through transistor Q2 to ground. The circuit remains in this state until the base drive to Q2 is removed by the control circuit. When Q2 turns off, the voltage across T3 winding 5,6 reverses, causing all the dotted ends of windings in T3 to become negative. Current starts to flow into the base of Q7. This causes collector current to flow. This current flows through winding 1,2 of T1, through the transistor and winding 2,1 of T3. The current in winding 2,1 of T3 produces current flow in windings 3,4 and 7,8 of T3. The action that takes place is regenerative and causes Q7 to snap on. When Q7 conducts, energy is transferred from the primary of T1 to the secondary. The positive voltage at terminal 5 of T1 charges capacitor C6 through D14 and R21. The voltage at terminal 5 depends on the conduction time of the switch. When the control circuit switches Q2 on, C6 discharges through D9, winding 5,6 of T3 and transistor Q2. The current through winding 5,6 of T3 makes all dotted ends positive on T3. The negative polarity on the base of Q7 turns it off. D11 is across T3 and Q2 for noise immunity. Diodes D41, D12, and D3 are antisaturation diodes. C19, R27, and D27 form the snubbing network.

Winding 1,3 of T1 is a reset winding. On turn-off, this winding clamps the collector of Q7 to two times the storage voltage. It is also used for resetting the high frequency transformer core.

4.9.4 Outputs

There are four secondary outputs. The -23 volt output is rectified by D28, filtered by C18, and passed on through a 300 ohm resistor. The output goes to two zeners mounted on the video board. The 300 ohm resistor limits power dissipation in the zeners and also dissipates all power under short circuit conditions.

The -12 volt output consists of a rectifier diode (D29), filter capacitor (C20), and a regulator Z1.

The voltage at winding 9,10 of T1 is rectified by D36 and goes into an averaging network L2 and C31.

The catch diode, part of D36, completes the conduction path when Q7 is off. When Q7 is on, there is a voltage on the secondary with pin 9 being positive. D36 is forward biased and current flows through L2. This causes the inductor current to increase at this time. With the switch open, stored energy in the inductor forces the current to continue to flow to the load and return through the catch diode (D39). The voltage across L2 is now reversed and is approximately equal to the output voltage. During this time the current in L2 decreases. The average current through L2 equals the load current. Since C31 keeps the output voltage constant, the load current will also be constant.

The +12 volt output circuitry works the same way as above except the voltage at winding 4,5 is turned on by Q8 and turned off by the voltage at terminal 5 going negative.

The current limit circuits for the +5 and +12 outputs have identical configurations; only some resistance values differ. The voltage at pin 5 of the comparator referenced to the junction of R16 and R37 is compared to the voltage drop across R37. When the voltage across R37 increases to a point where pin 6 is more positive than pin 5, E1 switches and pin 7 goes low, pulling pin 9 of E4 to ground and thus turning off the switching regulator.

The +12 volt control circuitry is synchronized to the 3524 pulse width modulator at a 30 kHz rate. When pin 12 of E4 is high, capacitor C15 charges up from the +12 start-up through R29, R26, and D13. The polarity on the capacitor is such that when pin 12 of E4 goes low, the emitter of Q6 is pulled negative with respect to the base which is at ground. Q6 saturates, pulling pin 2 of E3 down, thereby allowing the ramp generated at pins 6 and 7 by C13 to ramp up. Pin 6 is the threshold pin. The input to this pin is compared to the voltage at pin 5. When the voltage at pin 6 is equal to that of pin 5, pin 7 discharges capacitor C13 and pin 3 of E3 goes low. Whenever the voltage at pins 6 and 7 is ramping up, the output of E3, pin 3, is high.

C13 is the timing capacitor for the +12 volt pulse width modulator. C13 is charged from a voltage-controlled current source. The voltage at pin 5 of E3 is connected to the 5 volt reference. Thus, when the voltage across C13 reaches 5 volts (pin 6 of E3), the output of E3 pin 3 drops low, turning Q1 off and thereby turning Q8 on. Q7 and Q8 are turned off simultaneously when Q2 is turned on. The pulse width that determines the length of time Q8 is on is determined by the rate of voltage rise on capacitor C13. The faster C13 charges, the longer Q8 conducts. The error voltage that determines the rate of rise on C13 is generated by error amplifier E2. The noninverting input of the error amplifier is referenced to D38, a 5.1 volt zener. The inverting input is divided up by R2 and R3 and senses the +12 volt output. Any difference creates an error signal on pin 6 of E2. This increase or decrease in voltage at pin 6 divided by R33 generates a proportional change in current through Q5, thereby changing the rate of voltage charge on capacitor C13. As described above, the change in rate of charge affects the pulse width.

R4, C1, and R5 are the compensating components of error amplifier E2. D1 and D2 are antisaturating diodes. R6 limits the base drive and R7 and C3 are a speed-up circuit to turn Q1 on and off.

4.9.5 Power Supply Specifications

4.9.5.1 Input Specifications

Voltage

Single phase, 2 wire	90–128 V rms (switch-selected) 180–256 V rms
Frequency	47–63 Hz
Current	2.2 A rms max. @ 115 V rms; 1.1 A rms max. @ 230 V rms.
Input power	250 VA apparent 150 W max.
Power factor	Ratio of input power to apparent power is greater than 0.6 at full load and minimum input voltage. The VT100 appears capacitive to the line.
Leakage current	When installed in VT100 terminal, current to ground is 0.5 mA max. Each line to ground at 250 V rms sine, 50 Hz.
Current limiting	When installed in video terminal, 3.0 A normal blow fuse.

Electrical Magnetic Interference Susceptibility

Conducted transients	Single voltage transient without causing system degradation: 600 V @ 2.5 W/sec max.
Single voltage transient, survival	1000 V @ 2.5 W/sec max.
Average transient power, survival	0.5 W max.
Conducted cw noise	Unit operates without error at conducted noise levels up to 10 kHz – 30 MHz: 3 V rms.
	RF Field Susceptibility: 10 kHz – 30 MHz: 2 V/M; 30 MHz – 1 GHz: 5 V/M with power supply installed in video terminal.
Power line disturbance	

Ride through capability	The VT100 power supply provides a minimum of 20 ms ride through during a power outage condition. Ride through capability is at low line and full load. During this time, all power supply outputs must be within their specified limits.
Overvoltages	The VT100 power supply withstands for one second, an overvoltage of 110% of the maximum input voltage(s) specified in Section 4.9.5.1.1 without causing system degradation or damage.
Undervoltages, disturbances, and outages	The VT100 power supply is capable of withstanding undervoltage disturbance and power interruptions without physical damage.
Hi-Pot	Input to frame for 1 min. — 2.15 kV dc; input to output for 1 min. — 2.5 kV rms

Output Specifications

General	DC outputs are provided by the dc output distribution. DC output specifications are defined at the dc distribution buses. Distribution systems must be designed per this document since no output voltage adjustments are provided.
Output power	+5 V @ 1.5 A min to 11.0 A max. +12 V @ 1.0 A min to 2.75 A max. −12 V @ 0.0 A min to 0.5 A max. −23 V @ 10 mA

+5 V Specifications

Total regulation	±5%
Static line regulation	±0.75%
Static load regulation	±2.0%
Long term stability	0.1% – 1000 hrs
Thermal drift	±0.025% – deg C
Ripple	150 mV p-p for f < 66 kHz
Dynamic load regulation	±2.2% (see notes)
Noise	1% peak at f greater than or equal to 100 kHz (noise is superimposed on ripple)

+12 V Specifications

Total regulation	±5%
Static line regulation	±0.5%
Static load regulation	±1.0%
Long term stability	0.1% – 1000 hrs
Thermal drift	±0.025% – deg C
Ripple	240 mV p-p for f < 66 kHz
Dynamic load regulation	±1.1% (see notes)
Noise	1% peak @ f greater than or equal to 100 kHz (noise is superimposed on ripple)

−12 V Specifications

Total regulation	±5%
Static line regulation	±0.5%
Static load regulation	±1.0%
Long term stability	0.1% – 1000 hrs
Thermal drift	±0.025% – deg C
Ripple	240 mV p-p for f < 66 kHz
Dynamic load regulation	±1.1% (see notes)
Noise	1% peak @ f greater than or equal to 100 kHz (noise is superimposed on ripple)

−23 V Specifications

Total regulation	±10%
Static line regulation	±2%
Ripple	500 mV p-p

NOTES

1. **For all outputs, the long term stability and thermal drift specifications apply after a 5 minute minimum warmup, measured at the dc distribution buses with an averaging meter.**

2. **Dynamic load regulation is measured in +25% load steps from a starting point of 75% of full load. Measurements are made at the power supply terminals.**

3. **Zener diodes for −23 V supply are located at the load and not on the power supply.**

Regulation limits

Regulation limits are measured at the dc distribution buses. The root sum squared of errors due to the following conditions:

1. Initial tolerance
2. Static and dynamic input voltage
3. Gradual load changes over the load range minimum to full load
4. Operation over the temperature environment specified for the VT100
5. Long term stability per 1000 hours
6. Ripple and noise must remain within the total regulation limits stated above.

Ripple and noise	Ripple and noise must be measured with a wide band oscilloscope in the differential mode between ground and the output under test. The oscilloscope must be grounded so as to minimize spurious responses. The specification applies only to repetitive voltage variations that occur while operating with a constant input voltage and fixed load.
Overload protection	
+5 V output	Current limit with foldback. Limit point is 18 A max; foldback is 6.0 A max.
+12 V output	Current limit with foldback. Limit point is 6 A max; foldback is 3 A max.
−12 V	Internal current limit of the 3-terminal regulator is per DEC specifications PS-19-12048-02.
−23 V	Current limited to less than 150 mA.
Voltage adjustments	None. 1.68 kg (3.7 lbs) max.

4.9.5.2 Cooling – Cooling is by natural convection. Adequate space must be provided around the supply to allow a free flow of air. The power supply was designed with capability greater than the basic VT100 requirements so that options could be easily added in the future. Since the form factor and power dissipation of these options is not known, additional air flow and thermal profile testing should be conducted as part of the option design to determine if convection cooling is sufficient.

4.9.5.3 Base Product Power Requirements – The basic VT100 terminal controller, monitor, and keyboard have the following combined maximum power requirements:

+5 V	2.5 A
+12 V	1.8 A
−12 V	0.03 A
−23 V	12 mA (no other device should use this voltage).

The advanced video option uses +5 V, 1.1 A maximum power.

CHAPTER 5
VT100 SERIES SERVICE

5.1 INTRODUCTION

This chapter contains troubleshooting and repair information for VT100 series terminals. All terminals in the series are based on the VT100. Therefore, the VT100 can always be isolated as a separate unit. This allows you to determine if the trouble lies within the VT100 hardware or the hardware added to the terminal to make it a variation.

5.2 TROUBLESHOOTING

This section contains the troubleshooting information for the VT100 series of terminals.

5.2.1 Troubleshooting the Basic VT100

The VT100 has a series of internal self-tests that help isolate failures to a field replaceable unit (FRU). Paragraph 5.2.7 describes the tests and how to run them. Tables 5-1 and 5-2 show the error codes, the detected failure, and the FRU you should replace.

Table 5-1 Keyboard LED Error Codes

Keyboard LEDs					
L1	**L2**	**L3**	**L4**	**Error**	**Replace FRU**
Off	Off	Off	On	ROM 1	Terminal controller
Off	Off	On	Off	ROM 2	Terminal controller
Off	Off	On	On	ROM 3	Terminal controller
Off	On	Off	Off	ROM 4	Terminal controller
Off	On	Off	On	Main Data RAM	Terminal controller

Table 5-2 VT100 Display Error Codes

Error Char.	Error Detected: AVO	NVR	KBD	Data Loopback	EIA	Replace
1	X	–	–	–	–	Advanced video
2	–	X	–	–	–	Terminal controller
3	X	X	–	–	–	Advanced video and terminal controller
4	–	–	X	–	–	Keyboard
5	X	–	X	–	–	Advanced video and keyboard
6	–	X	X	–	–	Terminal controller and keyboard
7	X	X	X	–	–	Advanced video, terminal and keyboard
8	–	–	–	X	–	Terminal controller
9	X	–	–	X	–	Advanced video and terminal controller
:	–	X	–	X	–	Terminal controller
;	X	X	–	X	–	Terminal controller and advanced video
>	–	–	X	X	–	Keyboard and terminal controller
=	X	–	X	X	–	Advanced video, keyboard and terminal controller
<	–	X	X	X	–	Terminal controller and keyboard
?	X	X	X	X	–	Advanced video, keyboard and terminal controller
@	–	–	–	–	X	Terminal controller
A	X	–	–	–	X	Advanced video and terminal controller
B	–	X	–	–	X	Terminal controller
C	X	X	–	–	X	Advanced video and terminal controller
D	–	–	X	–	X	Keyboard and terminal controller
E	X	–	X	–	X	Advanced video, keyboard and terminal controller
F	–	X	X	–	X	Keyboard and terminal controller
G	X	X	X	–	X	Advanced video, keyboard and terminal controller
H	–	–	–	X	X	Terminal controller
I	X	–	–	X	X	Advanced video and terminal controller

Table 5-2 VT100 Display Error Codes (Cont)

Error Char.	Error Detected					Replace
	AVO	NVR	KBD	Data Loopback	EIA	
J	–	X	–	X	X	Terminal controller
K	X	X	–	X	X	Advanced video and terminal controller
L	–	–	X	X	X	Keyboard and terminal controller
M	X	–	X	X	X	Advanced video, keyboard and terminal controller
N	–	X	X	X	X	Keyboard and terminal controller
O	X	X	X	X	X	Advanced video, keyboard and terminal controller

5.2.2 Troubleshooting Basic VT100 Variations Without Self-Test

If the terminal appears to be faulty, perform the following procedure. If the problem is not solved by this procedure, refer to Table 5-3 for a list of typical problems.

1. Turn the power switch to the off position and check the following items.

   a. *Power cord.* Make sure the cord is connected securely at both the terminal and the wall outlet. Check the wall outlet with another device, such as a lamp, to make sure it is providing ac power.

   b. *Voltage selection switch and fuse.* Make sure the switch is in the correct position and the fuse is good.

   c. *Keyboard coiled cord.* Check that the cord is securely plugged into the keyboard connector at the back of the terminal.

2. Turn the power switch to the on position. The terminal performs the power-up test. Refer to the power-up test description (Paragraph 5.2.7.1) for more information about the power-up test. If the terminal does not power up correctly, refer to Table 5-3.

3. If needed, perform the Computer Port Data Loopback Test. Refer to the data and EIA loopback test descriptions (Paragraphs 5.2.7.2 and 5.2.7.3) for more information about the data loopback test.

Table 5-3 lists the most common VT100 failures and the associated symptoms. To use this table select the symptom that matches the terminal failure.

Table 5-3 Basic VT100 Troubleshooting Procedure

NOTES

1. **This procedure assumes that only one field replaceable unit (FRU) has failed. Symptoms displayed may be representative of a multiple failure; as a result, symptoms may change as FRUs are replaced. Always troubleshoot to the current symptoms.**

2. **Spare parts do fail. Do not ignore the possibility of a failure just because the module has been replaced once.**

3. **You must turn off the power before disconnecting or replacing any FRU.**

Symptoms	Probable Cause	Corrective Action
No response when power switch is set to ON. The CRT filament and LEDs are not on.	Not plugged in; no power at wall socket.	Plug in VT100; use different wall socket if possible.
	Main power fuse	Replace fuse. (If fuse blows again there is a possible shorting problem. Use appropriate troubleshooting methods).
	Power supply	Replace power supply.
	AC line cord	Check for open or short and replace line cord.
	Power distribution harness	Replace harness.
No response when power switch set to ON and CRT filament is on.	Power supply	Replace power supply
	Terminal controller board	Replace board.
	Power distribution	Replace harness.
No audible tones when terminal is turned on. LEDs are on. (Most usual hard failure symptoms.)	Controller	Replace.
	Keyboard	Replace.
	Keyboard cable	Replace.
	Speaker	Replace.

Table 5-3 Basic VT100 Troubleshooting Procedure (Cont)

Symptoms	Probable Cause	Corrective Action
No audible alarms and indicators when terminal turned on and none of the LEDs are on.	Keyboard disconnected.	Connect.
	Keyboard cable	Replace.
	Keyboard	Replace.
	Connectors	Check and reconnect.
	Controller	Replace.
Cursor does not appear on screen after terminal powered up. CRT filament is on.	Screen brightness too low.	Adjust monitor brightness.
	Controller	Replace.
	Monitor board	Replace.
	Flyback transformer	Replace.
	DC power harness	Replace.
	CRT and yoke assembly	Replace.
Cursor does not appear on screen after terminal is powered up. CRT filament is not on. Keyboard functional.	Monitor fuse open.	Replace monitor board.
	Monitor board	Replace.
	DC power harness	Replace.
	CRT and yoke assembly	Replace.
Random characters appear on screen.	Controller	Replace.
Horizontal or vertical line appears on screen.	Monitor connectors	Check and reconnect.
	Monitor board	Replace.
	CRT and assembly	Replace.

Table 5-3 Basic VT100 Troubleshooting Procedure (Cont)

Symptoms	Probable Cause	Corrective Action
Screen display distorted. Characters narrow on left or right side of screen.	Monitor is misadjusted.	Adjust monitor.
	Monitor board	Replace.
	Flyback transformer	Replace.
	CRT and yoke assembly	Replace.
	Controller	Replace.
Screen rolling.	Ball monitor misadjusted	Adjust.
	DC power harness	Check.
	Controller	Replace.
	Monitor	Replace.
Display presentation bows in or out	Yoke pincushion incorrectly misadjusted.	Replace CRT and yoke assembly.
Display presentation jumpy.	Interlace feature on.	Turn feature off.
	Power feature set incorrectly.	Set feature to correct line frequency.
	Controller	Replace.
	Power supply	Replace.
	Monitor board	Replace.
	Flyback transformer	Replace.
Wrong character appears on screen when typed in LOCAL	Graphics or alternate character set, or alternate keypad mode or cursor key mode is selected.	Clear condition with power up or reset.
	Keyboard	Replace.
	Controller	Replace.

Table 5-3 Basic VT100 Troubleshooting Procedure (Cont)

Symptoms	Probable Cause	Corrective Action
Wrong character appears on screen when typed in ON-LINE with loopback installed.	Graphics or alternate character or alternate keypad mode or cursor key mode is selected.	Clear condition with power up or reset.
Terminal functional in LOCAL mode.	Transmit and receive speed not the same.	Change speed setting.
	Controller	Replace.
Wrong characters appear on screen when typed ON-LINE and connected to computer. Terminal functional with loopback connector.	Receive and/or transmit speed set incorrectly.	Set speeds to match computer.
	Bits per character feature set incorrectly.	Set feature to match computer.
	Parity feature set incorrectly.	Set parity and/or parity sense feature to match computer.
	Communications line	Check communications facilities.
Double characters	Local echo set on full-duplex system (VT1XX-AC, VT132 only)	Set correct feature.
Messages received are incomplete.	XON/XOFF feature set incorrectly.	Set feature.
	Computer does not recognize XON/XOFF sequence.	See Chapter 3 of *VT100 User Guide.*
	Controller	Replace.
Checkerboard character appears on screen instead of character typed (ON-LINE with computer).	Parity feature set incorrectly.	Set parity and/or parity/sense feature match computer.
	Controller	Replace.
	Communications facility problem	Check communications facility.

Table 5-3 Basic VT100 Troubleshooting Procedure (Cont)

Symptoms	Probable Cause	Corrective Action
All characters displayed as a white area (black with reverse screen).	Alternate character set selected and not available.	Clear condition with power-up or reset.
Only top or bottom half of characters appear on the screen.	Incorrect use of double-height escape sequence	See Chapter 3 of *VT100 User Guide.*
SET-UP features do not work correctly (multiple alarms may sound on power up or recall). Error 2 displayed on screen.	Save operation not performed.	Perform save operation.
	Controller	Replace.
Terminal does not respond to Escape sequences.	ANSI/VT52 feature set incorrectly.	Set ANSI/VT52 feature to correct compatibility.

5.2.3 Troubleshooting the VT105

The troubleshooting procedure for the VT105 consists of the following two steps.

1. Isolate to the base VT100 configuration and troubleshoot the terminal.
2. Perform the internal VT105 waveform generator tests described in Chapter 6.

To isolate to the base VT100, disconnect the graphics interface cable from J2 on the VT100 controller board. Now perform the troubleshooting procedures outlined for the basic VT100.

To troubleshoot the VT105 graphics module, reconnect the graphics interface cable to J2 on the VT100 controller board. Perform the testing procedure outlined in Chapter 6. When performing the test sequence remember to type the sequence exactly as written. If an error appears retype the sequence to verify that there is an error and then replace the VT105 graphics board.

5.2.4 Troubleshooting the VT132

The troubleshooting procedure for the VT132 is the same as the basic VT100. The only difference between the two machines is the advanced video option (AVO) board. On the VT132 the AVO board is standard and contains four ROMs. In addition the ROMs on the video controller board are different. To replace the terminal controller board, remove the ROMs from the new VT100 controller board and substitute the VT132 ROMS. To replace the advanced video option board, configure the new AVO board jumpers or switches for VT132 application, and plug in the VT132 ROMs. Paragraph 5.4 contains information on board configuration.

5.2.5 Troubleshooting the VT125

The VT125 is a VT100 terminal that has an intelligent graphics processor installed between the terminal and the communications connectors (Figure 5-1). A problem in the graphics components can also prevent the terminal from working as a text terminal. You can isolate any problem with the VT125 to the VT100 components or the graphics components.

If any of the following conditions exist, remove the graphics components from the terminal by performing the appropriate procedures in Paragraph 5.4.

- The VT125 cannot complete its power-up test
- Any of the keyboard indicators L1 through L4 are on at the end of the power-up test
- The complete screen flashes

After you remove the graphics components, test and troubleshoot the terminal as a VT100. When the terminal passes its VT100 power-up and data looback tests, reinstall the graphics components and perform the VT125 tests (Paragraph 5.2.8).

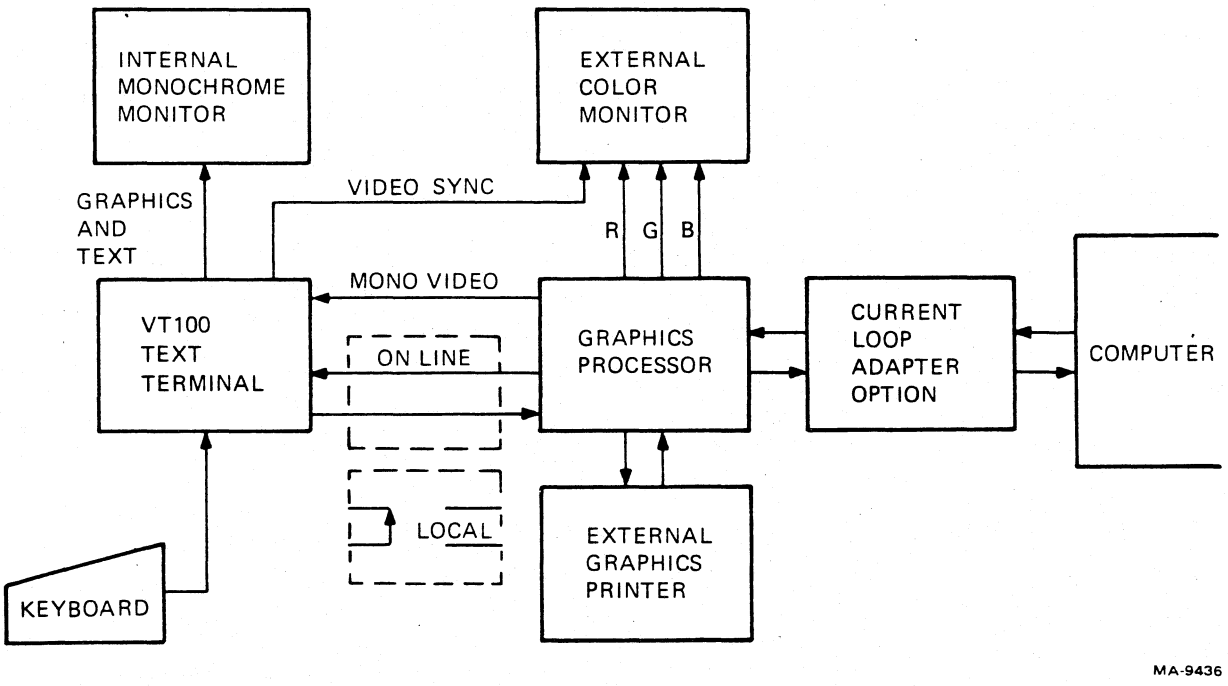


Figure 5-1 VT125 General Block Diagram

5.2.5.1 VT125 Self-Test Error Codes – If a character appears under the blinking cursor at the top left corner of the screen, or a message appears in the center of the screen, check Table 5-4 for the meaning of the error code character or message. Note that a character displayed can indicate more than one error. To clear the error indication after the error is corrected, reset or power up the terminal.

The self-test code characters indicate the following three types of errors.

Advanced video option (AVO) if installed	If the advanced video option fails, the terminal operates with the basic VT100 text capabilities.
User permanent SET-UP feature memory failure (Memory)	If the user permanent SET-UP feature fails, the terminal operates using default SET-UP feature selections for each feature. (Refer to Chapter 6 for more information on the SET-UP feature memories.)
Keyboard missing or malfunction (Keyboard)	If only the keyboard fails, the terminal ends the test ON-LINE so it may operate as a receive-only terminal. The SET-UP feature selections cannot be changed.

There are several other problem indicators. The solutions are listed in the suggested order of FRU replacement.

Indication	Problem	Solution
VT125 Off-Line	VT100 text terminal is LOCAL. LOCAL was saved in SET-UP, or there is a user permanent memory problem. Terminal can only process received graphics.	Put terminal ON-LINE and save the feature in SET-UP.
VT125 BM Error	Video bit map memory has one or more bad pixels.	Replace graphics board.
VT125 EC Error	Computer port failed data loopback test. Terminal can only operate as text terminal in LOCAL.	Replace graphics board, paddle board, 24-pin cable.

Indication	Problem	Solution
VT125 IC Error	Internal communications failure – VT125 cannot communicate with VT100. Terminal can only process received graphics.	Replace graphics board, paddle board, 24-pin cable.
VT125 SC Error	Auxiliary port failed data loopback test. Terminal cannot send data to printer.	Replace graphics board, paddle board, 24-pin cable.
VT125 VG Error	Vector generator could not draw sample shape. Graphics probably does not work, but terminal may communicate normally.	Replace graphics board.

A box is drawn around the margin of the graphics screen area.* If any part of the box is missing or distorted, replace the graphics board.

If no graphics data appears, but the VT100 section of the terminal operates correctly, the 16-pin cable may be bad.

If an external color monitor has trouble displaying graphics information, but the internal monitor displays correctly, the ground wire from the chassis to the graphics processor board video connector bracket may be loose.

Table 5-4 shows the possible error characters displayed on the screen and the failure indicated by each character. Note that a character displayed can indicate more than one error.

*Not on all units

Table 5-4 VT125 Displayed Error Codes

Character Displayed	Faults Detected AVO	Memory	Keyboard
1	X	–	–
2	–	X*	–
3	X	X	–
4	–	–	X†
5	X	–	X
6	–	X	X
7	X	X	X

Message Displayed	Faults Detected
VT125 OK	None (normal power-up test results)
VT125 Offline	VT100 text terminal is LOCAL – LOCAL was saved in SET-UP, or there is a User Permanent Memory problem.
VT125 BM Error	Video bit map memory one or more bad pixels
VT125 EC Error	Computer port
VT125 IC Error	Internal communications
VT125 SC Error	Auxiliary port
VT125 VG Error	Vector generator

*Also, bell tones are generated – perform a save and recall in SET-UP.
†Check that keyboard is properly connected.

5.2.6 Troubleshooting the Options

Troubleshoot the options after the basic terminal is checked and found to be good. Then perform the option checkout procedure for the suspected faulty option as outlined in Chapter 6. If the option does not check out correctly, replace the option module.

5.2.7 VT100 Internal Self-Tests

The VT100 contains five self-test programs in the basic ROM memory.

Power-up test
Data loopback test
EIA test
Video adjust pattern keyboard test
SET-UP display test

Each test isolates a failure to the faulty module, so you can repair the terminal in a minimum amount of time. If the VT1XX-AC Printer Port Option is installed, use the test procedures for that option.

NOTE

In command sequences, control keys are labelled in angle brackets <KEY>. Control keys are The special keys that do not display on the screen. Press that key and type the rest of the sequence as shown.

5.2.7.1 Error Codes – If executing any self-test produces an error, the test stops automatically. The screen may display a random pattern of characters. Error indications are error codes displayed on the keyboard LEDs (L1 through L4, listed in Table 5-5), or an error code character displayed in the upper left corner of the screen, under the blinking cursor. If one or more errors occur while the test is repeating continuously, the entire screen flashes from white to black to white about once a second as an alarm. This continues until the terminal is reset.

Table 5-2 shows the error characters that may appear on the screen, and the FRU that you should check or replace.

5.2.7.2 Power-Up Test – The terminal automatically performs the following tests during power up.

1. Writes a 1 and a 0 in each bit location of RAM on the basic terminal controller board to verify that the RAM can store each bit.

2. Writes a 1 and a 0 in each bit location of RAM on the advanced video option (AVO) board to verify that the option RAM can store each bit. If the AVO board is not present, The terminal automatically skips this part of the test.

3. Reads the contents of the nonvolatile RAM (NVR), calculates a checksum, and then compares the checksum to the checksum stored in the NVR.

4. Reads the contents of each ROM chip, calculates a checksum, then compares the checksum to the checksum stored in each ROM chip.

5. Turns on all keyboard LEDs on, rings the keyboard bell for one-quarter second, and looks for the end-of-scan character from the keyboard to determine if the keyboard is functioning properly.

Use one of the following procedures to start the power-up test.

1. Turn the terminal power on.

   or

2. Type the following sequence to perform the test once. The terminal must be in ANSI-compatible mode (in SET-UP B, group 2 switch 3 = 1).

   <ESC>[2;1y

   or

3. Type the following sequence to perform the test continuously. The terminal must be in ANSI-compatible mode (in SET-UP B, group 2 switch 3 = 1).

   <ESC>[2;9y

   or

4. Enter SET-UP and press the **0** key (reset).

NOTE

The continuously running test ends only if it finds an error or you turn power off.

Any error found by the power-up self-test appears on the terminal screen and/or LEDs L1 through L4 on the keyboard. Tables 5-5 and 5-6 define the error codes.

Table 5-5 LED Error Codes

Error	L1	L2	L3	L4
ROM 1 checksum error	Off	Off	Off	On
ROM 2 checksum error	Off	Off	On	Off
ROM 3 checksum error	Off	Off	On	On
ROM 4 checksum error	Off	On	Off	Off
Main data RAM error	Off	On	Off	On

Table 5-6 Displayed Error Codes

Display Char	Fault Detected AVO	NVR	KBD	Data	EIA	Display Char	Fault Detected AVO	NVR	KBD	Data	EIA
1	X	–	–	–	–	@	–	–	–	–	X
2	–	X	–	–	–	A	X	–	–	–	X
3	X	X	–	–	–	B	–	X	–	–	X
4	–	–	X	–	–	C	X	X	–	–	X
5	X	–	X	–	–	D	–	–	X	–	X
6	–	X	X	–	–	E	X	–	X	–	X
7	X	X	X	–	–	F	–	X	X	–	X
8	–	–	–	X	–	G	X	X	X	–	X
9	X	–	–	X	–	H	–	–	–	X	X
:	–	X	–	X	–	I	X	–	–	X	X
;	X	X	–	X	–	J	–	X	–	X	X
<	–	–	X	X	–	K	X	X	–	X	X
=	X	–	X	X	–	L	–	–	X	X	X
>	–	X	X	X	–	M	X	–	X	X	X
?	X	X	X	X	–	N	–	X	X	X	X
						O	X	X	X	X	X

NOTE

See Table 5-3 to determine the correct module to replace.

5.2.7.3 Data Loopback Test – In the data loopback test the VT100 transmit and receive lines connect to each other via a special external connector. The test transmits a predefined set of characters. The terminal receives the characters and compares them to the characters transmitted. If the characters do not match, an error is then flagged.

Use the following procedure to perform the data loopback test.

1. Install the appropriate data loopback connector. Connector PN 12-15336 is for EIA communications (Figure 5-2); connector PN 70-15503-00 is for 20 mA current loop communications (Figure 5-3).

2. Make sure the transmit and receive speeds are the same.

3. Place the terminal in ANSI-compatible mode (in SET-UP B, group 2 switch 3 = 1).

4. Place the terminal ON-LINE.

5. Type the following sequence to perform the test.

   <ESC>[2;2y

   or

6. Type the following sequence to perform the test continuously.

   <ESC>[2;10y

NOTE
The continuously running test ends only if it finds an error or you turn power off.

Any error displays an error code on the screen. Table 5-6 defines the error codes.

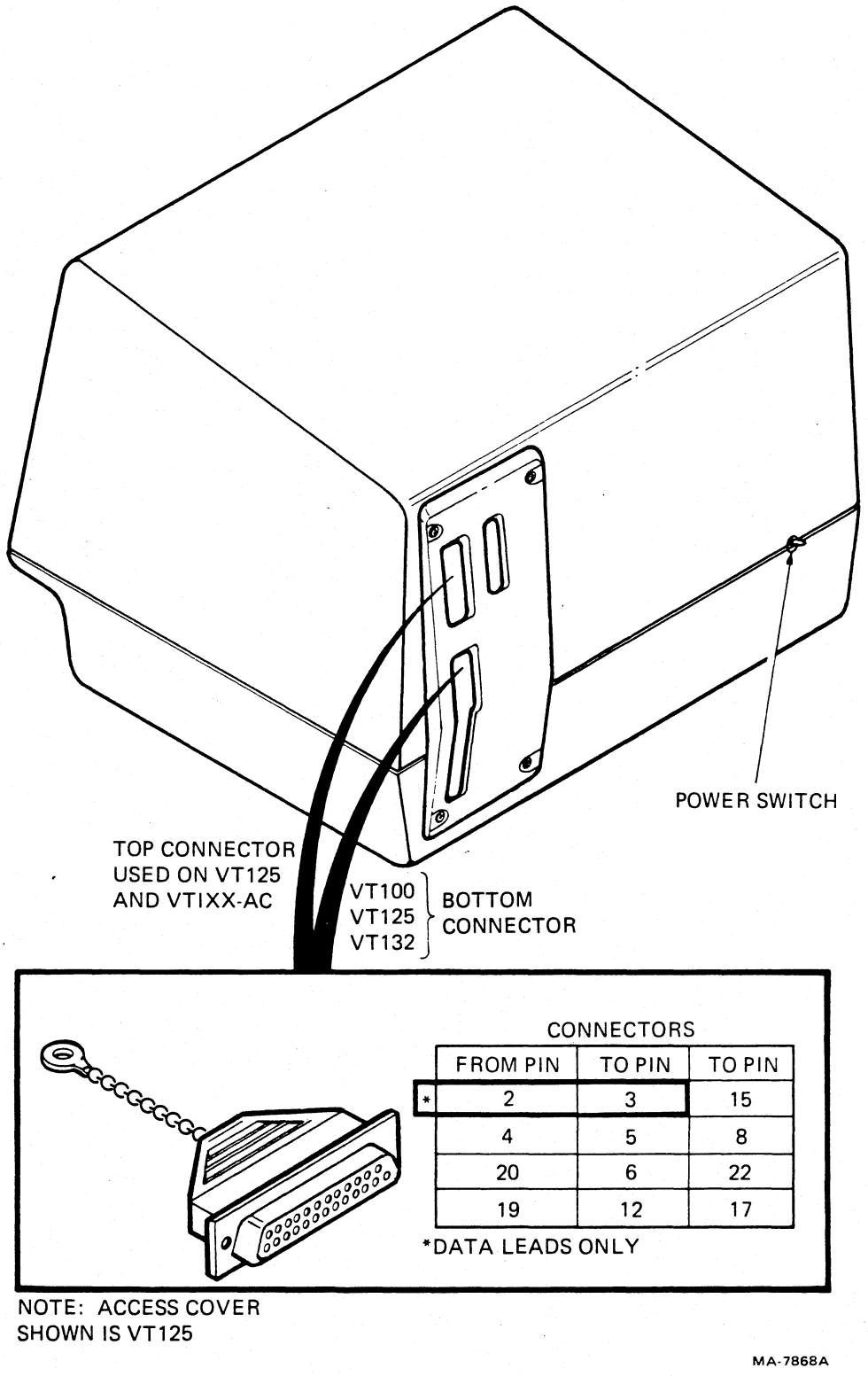


Figure 5-2 EIA Loopback Connector

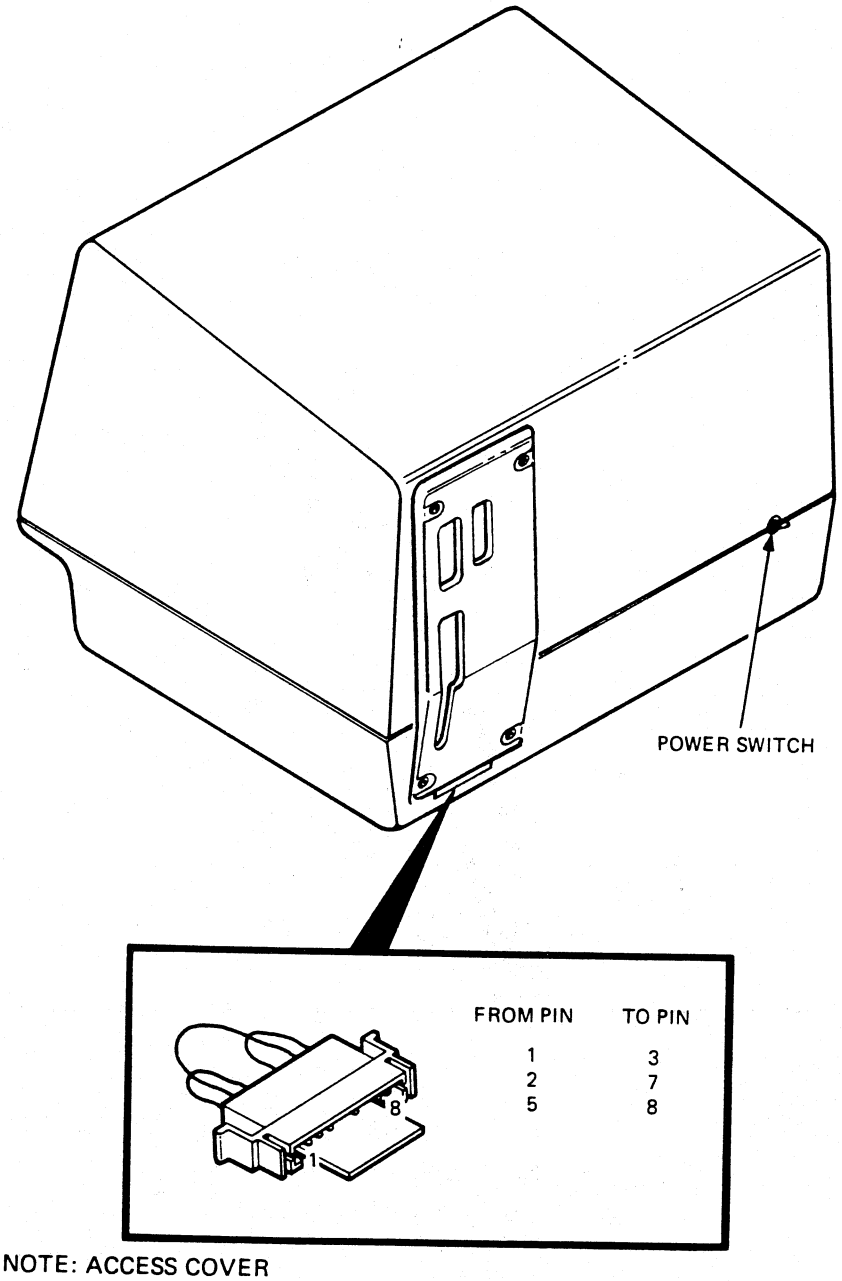


Figure 5-3 20 mA Loopback Connector

5.2.7.4 EIA Test – The EIA test checks that the following signals can be set to a 1 or a 0.

Data Terminal Ready	Request to Send
Data Set Ready	Clear To Send
Carrier Detect	Ring Indicator
Speed Select	Speed Indicator

Use the following procedure to perform the EIA test.

1. Install the EIA data loopback connector, PN 12-15336.
2. Make sure the transmit and receive speeds are the same.
3. Place the terminal in ANSI-compatible mode (in SET-UP B, group 2 switch 3 = 1).
4. Place the terminal ON-LINE.
5. Type the following sequence to perform the test once.

   <ESC>[2;4y

   or

6. Type the following sequence to perform the test continuously.

   <ESC>[2;12y

NOTE
The continuously running test ends only if it finds an error or you turn power off.

Any error displays an error code on the screen. Table 5-6 defines the error codes.

5.2.7.5 Keyboard Tests – The power-up test verifies the presence or absence of a keyboard. You can test individual keys by placing the terminal OFF-LINE and enabling keyclick. All keys typed should produce a click except **NO SCROLL, CAPS LOCK, SHIFT, BREAK,** and **CTRL.** Typing the keys should cause the corresponding character to appear on the screen. Typing **CTRL-G** should cause the bell to sound. This checks both the bell circuitry and the **CTRL** key. Keys typed with **CAPS LOCK** and **SHIFT** verify the operation of those keys. After you enable XON/XOFF and place the terminal ON-LINE, the **BREAK** and **NO SCROLL** keys should produce a click when typed.

5.2.7.6 SET-UP Screen Test – In SET-UP the terminal exercises all its display functions. The functions available in the base VT100 include double-height, double-width characters (SET-UP A), double-width, single-height characters (TO EXIT PRESS "SET-UP"), and reverse or underline base attribute (selected by the cursor setting and displayed by the cursor and the tab ruler).

The VT100 with advanced video option includes these basic functions, plus other functions such as 24 lines with 132 columns (test with the video adjust pattern, Paragraph 5.2.7.7), and more character attributes.

You can check the following features using the keyboard controls.

Intensity (up and down arrow keys)
80/132 column
Transmit and receive speeds
Reset
Smooth/jump scroll
Auto repeat
Reverse screen
Margin bell
Keyclick
US/UK character set
Wraparound
ON-LINE/OFF-LINE control

Check smooth scrolling by filling the screen with E's (Paragraph 5.2.7.7) and pressing line feed while OFF-LINE.

To perform the test, enter the two SET-UP displays and check that the details agree with those in the sample displays in Chapter 6. To test the advanced video option, check that the words SET-UP A blink in bold, the words TO EXIT PRESS "SET-UP" are underlined, and the tab ruler has alternating normal and reverse video sections, even if you selected the underline cursor.

5.2.7.7 Video Adjust Test – The video adjust test provides a screen full of E's for display height, width, and linearity adjustments. The test pattern is internal to the terminal and is not sent to the host computer.

Use the following procedure to display the test pattern.

1. Place the terminal in ANSI-compatible mode (in SET-UP B group 2 switch 3 = 1).

2. Place the terminal LOCAL.

3. Type the following sequence.

   <ESC>#8

5.2.8 VT125 Tests

The VT125 terminal has several self-tests available for checking terminal operation. Some of these are the self-tests of the VT100 terminal that the VT125 Graphics Processor resides in. The other tests are for the graphics processor itself. To perform the VT100 tests as described in Paragraph 5.2.7, disconnect the graphics components from the terminal controller.

The power-up test is performed each time the terminal is powered up. The other tests may be performed after the power-up test is completed. To perform the other tests, the terminal must be disconnected from the communication line, have an external loopback connector installed, and be ON-LINE with the ANSI/VT52 SET-UP B feature selected to ANSI (SET-UP B switch 2-3 = 1). When the tests are completed, turn the power switch off, remove the loopback connector, and connect the communication cable.

NOTE

A continuously running test ends only if it finds an error or you turn power off.

5.2.8.1 Loopback Connector Installation – Use the following procedure if the test needs a loopback connector installed on the terminal.

1. With the power switch off, disconnect the communication cable.
2. Install the loopback connector on the EIA connector. Refer to Figure 5-2. The EIA loopback connector is PN 12-15336.
3. If the 20 mA Current Loop Adapter Option is installed, perform one of the following steps.
   a. Use the loopback connector (PN 70-15503-00) included with the option.

      or

   b. Disconnect the current loop option cable from the terminal controller board (inside the access cover) and use the EIA loopback connector.

NOTE
Do not use the EIA loopback connector at the same time as the current loop connector.

5.2.8.2 VT125 Power-Up Test – The VT125 has a built-in power-up test to check terminal operation. The test checks general operation of the VT100, including the advanced video option (if installed), user permanent SET-UP feature memory, and keyboard. The test also checks general operation of the graphics processor, including the bit map memory.

To perform the power-up test, either turn the terminal on or (if power is already on) enter SET-UP and press the **0 (RESET)** key. Install a loopback connector and use the following procedure if the test must run continuously.

1. Turn the power switch on. The terminal performs the power-up test.
2. Type one of the following sequences to perform the test.

<ESC>[4;1y	Performs test once.
<ESC>[4;1;9y	Performs test continuously.

NOTE
You can also perform this test with the VT100 power-up test sequence (ESC[2;1y). The continuously running test ends only if it finds an error or you turn power off.

The test gives the following indications.

- Keyboard and screen flash on and off.
- All keyboard indicators turn on and off, and either the ON LINE or LOCAL indicator turns on.
- The wait message appears on the screen and then is erased.
- A bell tone sounds.

- A band of light appears at the top of the screen and then is erased.
- A second bell tone sounds.
- A message on the screen gives the result of the VT125 power-up test, and a box is drawn* around the margins of the graphics screen area.

NOTE
Messages do not appear on the screen until the terminal warms up.

- The text cursor appears in the upper-left corner of the screen.

The power-up test provides three possible error indications. (Refer to Paragraph 5.2.7.1 for more information about error indications.)

- Displays error on screen as a character or a message.
- Displays error on keyboard indicators L1 through L4.
- Sounds several bell tones.

5.2.8.3 VT125 Computer Data Port Loopback Test – The computer port data loopback test checks that the VT125 can transmit and receive characters over the computer dat port. To perform this test, you must connect the transmit and receive lines to each other with an external loopback connector. The terminal transmit and receive speeds must be the same (300 baud or faster). Use the following procedure to perform the test.

1. Turn the power switch on. The terminal performs the power-up test.
2. Type one of the following sequences to perform the test.

<ESC>[4;1;2y	Performs power-up test and computer data port loopback test.
<ESC>[4;1;2;9y	Performs power-up test and computer data loopback test continuously until failure.

The test gives the following indications. (Refer to Paragraph 5.2.8.2 for power-up test indications.)

- Either the ON-LINE or LOCAL indicator turns on.
- The wait message appears on the screen and then is erased.
- The cursor appears in the upper-left corner of the screen.
- If the computer data loopback test fails, the message "VT125 EC Error" appears on the internal monitor.

*Not on all units

5.2.8.4 VT125 Auxiliary Port Loopback Test – The auxiliary port data loopback test checks that the VT125 can transmit and receive characters over the auxiliary data port. To perform the test, you must connect the transmit and receive lines to each other with an external loopback connector. The auxiliary port speed must be 300 baud or faster. Use the following procedure to perform the test.

1. Turn the power switch on. The terminal performs the power-up test.

2. Type one of the following sequences to perform the test.

<ESC>[4;1;3y	Performs power-up test and auxiliary data port loopback test.
<ESC>[4;1;3;9y	Performs power-up test and auxiliary data port loopback test continuously until failure.

The test gives the following indications. (Refer to Paragraph 5.2.8.2 for power-up test indications.)

- Either the ON LINE or LOCAL indicator turns on.
- The wait message appears on the screen and then is erased.
- The cursor appears in the upper-left corner of the screen.
- If the test fails, the message "VT125 SC Error" appears.

5.2.8.5 VT125 Display Test – This test requires you to check the internal monitor screen and the color monitor screen (if present) for correct operation. The screen cycles through the four intensity levels of each of the three primaries and white to test the output memory. The computer data port must have the loopback connector installed. Use the following procedure to perform the test.

1. Turn the power switch on. The terminal performs the power-up test.

2. Type one of the following sequences to perform the test.

<ESC>[4;1;4y	Performs power-up test and display test.
<ESC>[4;1;4;9y	Performs power-up test and display test continuously until failure.

The test gives the following indications. (Refer to Paragraph 5.2.8.2 for power-up test indications.

Monochrome

Step 1	White	Light Grey	Dim Grey	Black
Step 2	Black	White	Light Grey	Dim Grey
Step 3	Dim Grey	Black	White	Light Grey
Step 4	Light Grey	Dim Grey	Black	White
Step 5	White	Light Grey	Dim Grey	Black

Color				
Step 1	Light Green	Light Red	Light Blue	Black
Step 2	Black	Black	Black	Black
Step 3	Black	Light Red	Black	Black
Step 4	Dim Blue	Dim Red	Dim Green	Dim Grey
Step 5	Light Blue	Light Red	Light Green	Light Grey

5.2.8.6 VT125 Video Bit Map Memory Test – This test checks that every bit in both video bit map planes can be written to both 1 and 0. The computer data port must have the loopback connector installed. Use the following procedure to perform the test.

1. Turn the power switch on. The terminal performs the power-up test.
2. Type one of the following sequences to perform the test.

<ESC>[4;1;5y	Performs power-up test and video bit map memory test.
<ESC>[4;1;5;9y	Performs the power-up test and video bit map memory test continuously until failure.

The test gives the following indications. (Refer to Paragraph 5.2.8.2 for power-up test indications.)

- The screen fills with levels of intensity (or color) moving from top to bottom.
- If this test fails, the message "VT125 BM Error" appears.

5.3 VIDEO ALIGNMENT

This section describes the alignment of both the Ball Brothers and Elston video monitors. Always check each adjustment, because many adjustments affect each other. However, if a check shows the correct indication, skip that adjustment and go to the next procedure.

Make all adjustments under the following conditions.

- Normal video (white characters on a dark background; SET-UP B, switch 1-3 = 0)
- 80 characters per line
- ANSI mode (SET-UP B, switch 2-3 = 1)
- LOCAL mode
- Out of SET-UP
- CRT alignment template attached to the screen
- Top cover removed
- Screen filled with E's (after brightness adjustment)
- Type **ESC#8**

5.3.1 Alignment Template

Figure 5-1 shows the alignment dimensions used in this procedure. If the mylar adjustment templates (PN 94-03220-03 and PN 94-03270-03) are not available, use the dimensions in Figure 5-4 to make a paper template. Paragraph 5.3.1.1 and Figure 5-5 describe the procedure. You can perform the adjustments with the paper template or mylar template.

5.3.1.1 Making a Paper Template – You need a pencil, a ruler, a triangle (or anything that can help you draw a right angle), and a sharp knife.

1. Mark a dot in the center of a piece of stiff paper.
2. Measure the dimensions to the top and bottom, and mark with dots.
3. Draw the top and bottom lines (using the triangle if needed).
4. Mark off the left and right sides and draw those lines at a right angle to the top and bottom lines.
5. Measure the width of the "red shaded area" in Figure 5-4 and mark a dot at each of the four sides.
6. Draw a line through each dot to form a box around the box already drawn.
7. Mark an area in the middle of each side to leave for support, and cut out the rest of the band of paper.
8. Measure from the center through each outer corner and cut the paper away so you can center the paper template on the CRT between the marks at the bezel corners.

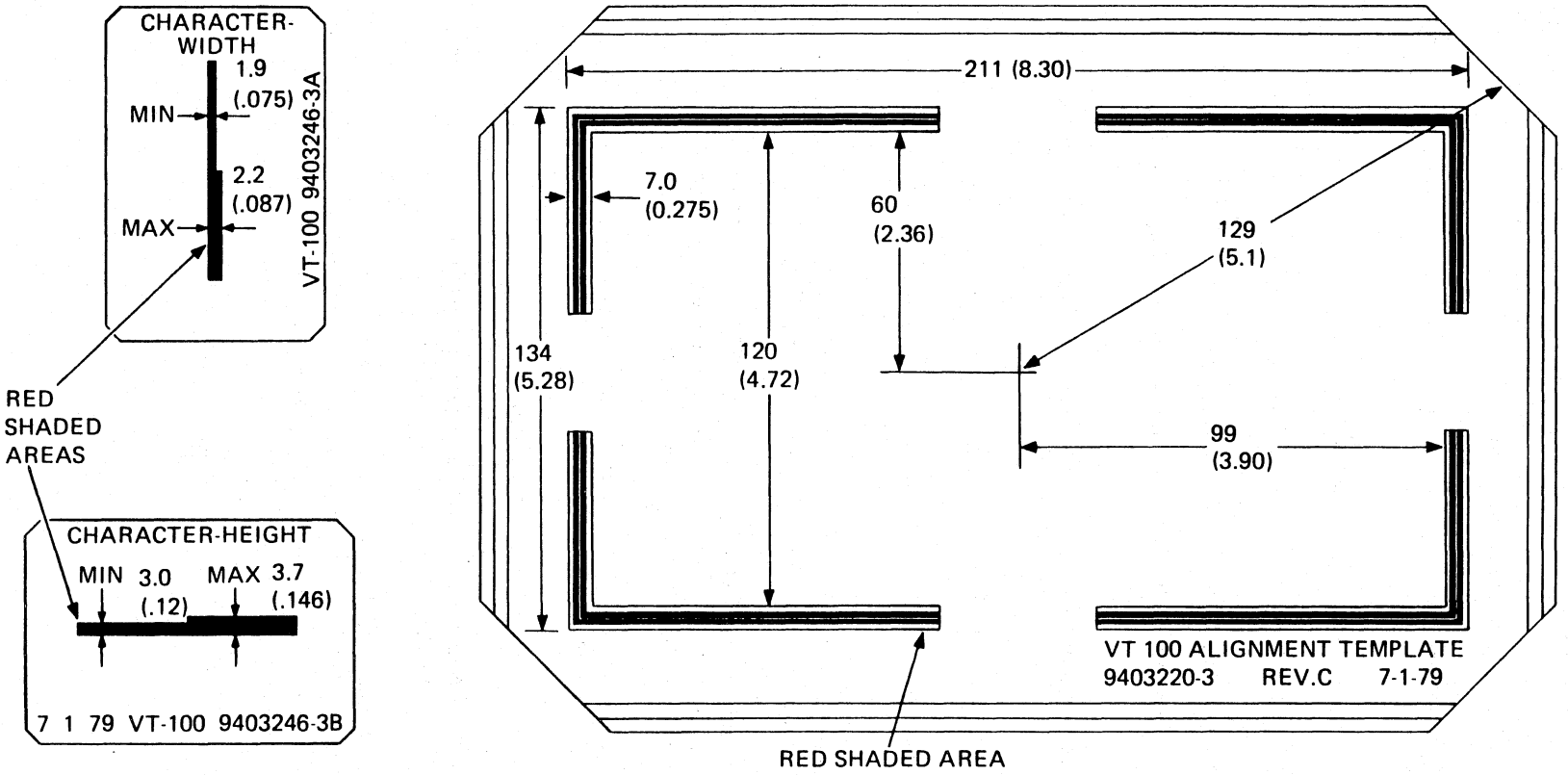
5.3.1.2 Attaching the Template – The CRT template (PN 94-03220-03) stays attached to the screen during all adjustment procedures. (If you are using the paper template, you may have to remove it for brightness and linearity.) Use the following procedure to attach the template to the CRT.

1. Using the bezel around the screen as a guide, mark the four edges of the screen with a water-soluble marker (felt-tip pen).
2. Remove the terminal top cover (Paragraph 5.4.11).
3. Tape the CRT alignment template to the screen, with the four corners of the template all the same distance from the marks you made in step 1.

5.3.2 Monitor Adjustments (Ball Brothers)

The following paragraphs describe the alignment of the Ball Brothers video monitor. You can easily identify the Ball monitor by the location of the flyback transformer (on the horizontal brace above the CRT's neck). This monitor also has a small connector board on the CRT yoke assembly.

Make all adjustments under the conditions listed in Paragraph 5.3.



NOTE: MEASUREMENTS ARE IN MILLIMETERS
EXCEPT VALUES IN PARENTHESIS ARE IN INCHES.

MA-2069A

Figure 5-4 Video Alignment Templates

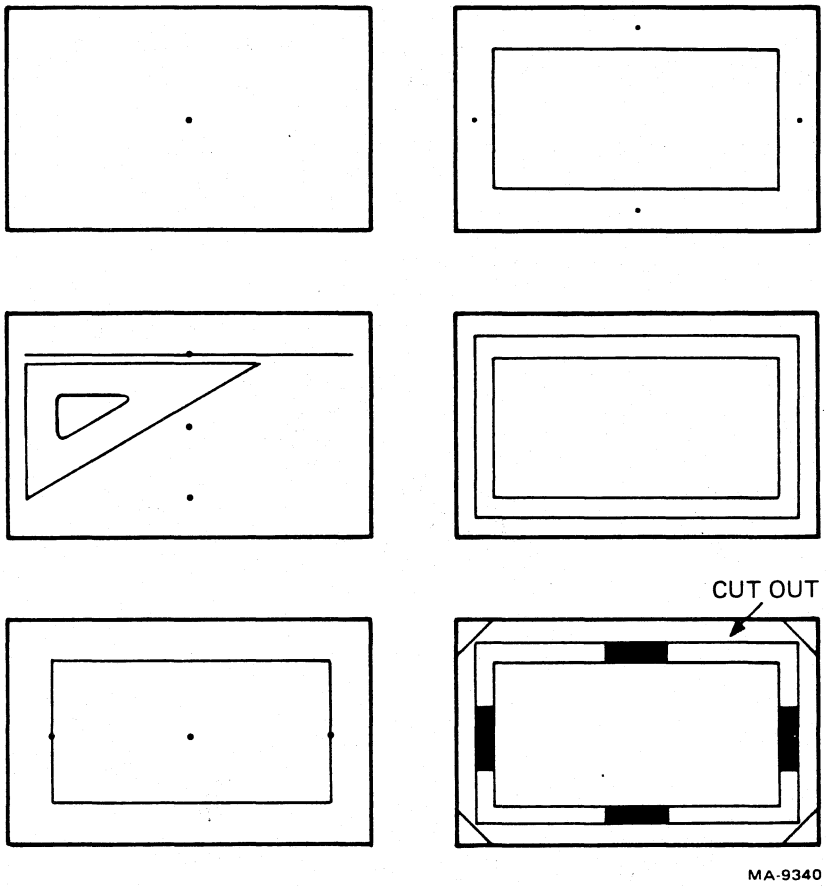


Figure 5-5 Paper Alignment Template

5.3.2.1 Brightness – Use the following procedure to adjust the brightness control on the monitor board.

1. Let the terminal warm up for at least five minutes.
2. Increase the screen brightness to the maximum level by pressing the ↑ key in SET-UP.
3. Adjust R117 (Figure 5-6) until you see the display raster. Then turn R117 in the opposite direction until the raster disappears.
4. Return the brightness to a medium level by pressing the ↓ key in SET-UP.

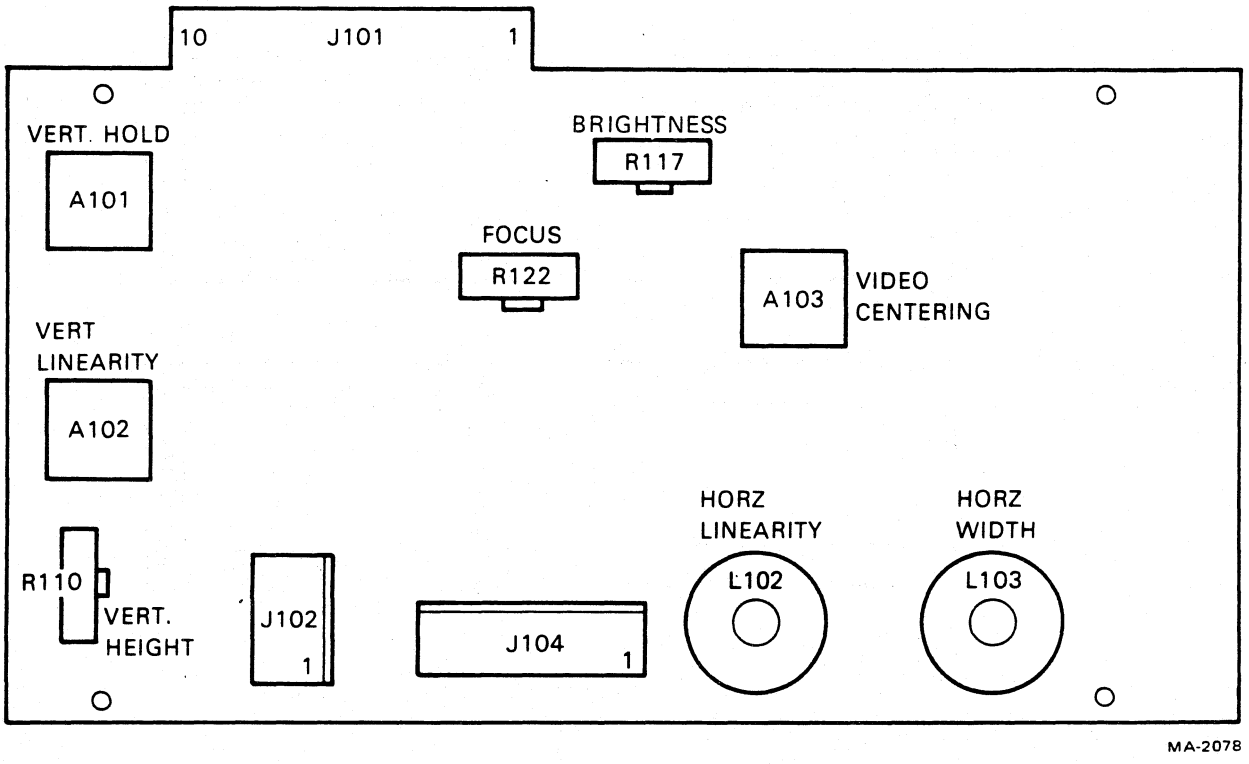


Figure 5-6 Ball Video Monitor Board Adjustments

5.3.2.2 Yoke Rotation – Use the following procedure to check and adjust the yoke.

1. Check that all four sides of the screen display are parallel to the red shaded area of the alignment template.

2. Loosen the yoke collar clamp screw (Figure 5-7) and turn the yoke until the four sides of the screen display are parallel to the edges of the red shaded areas of the alignment template.

3. Check that the yoke is pushed all the way forward toward the face of the CRT. Hold the yoke in place and tighten the yoke collar clamp screw.

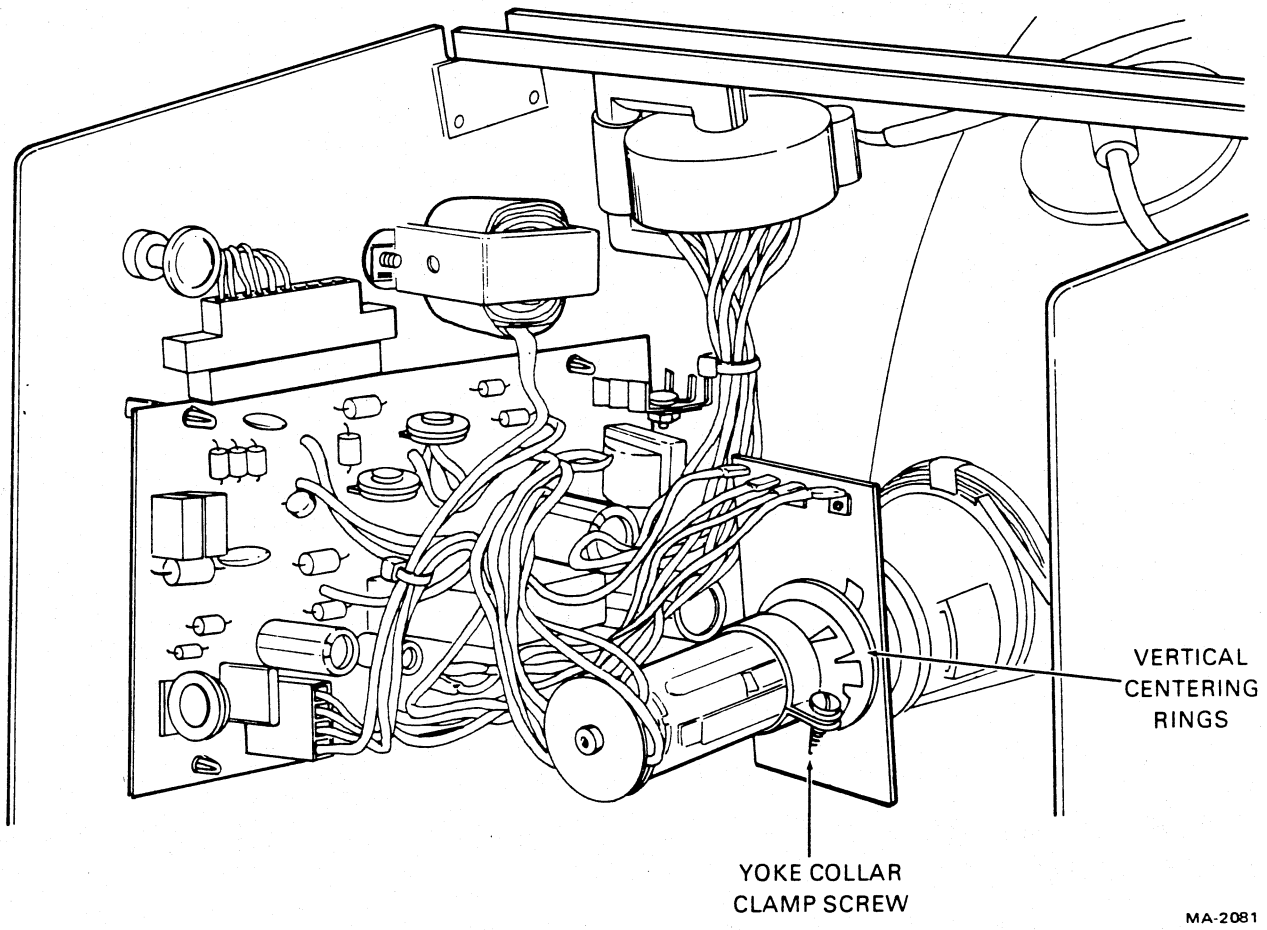


Figure 5-7 Ball Monitor CRT Adjustments

5.3.2.3 Vertical Height – Use the following procedure to check and adjust the height of the screen display.

1. Check that the top and bottom display lines are covered by the red shaded area of the adjustment template.

2. Adjust the vertical height control R110.

5.3.2.4 Horizontal Width – Use the following procedure to check and adjust the width.

1. Check that the first and last columns of the display are covered by the red shaded area or the adjustment template.

2. Adjust the horizontal width coil L103 with a monitor alignment tool (PN 29-23190-00).

5.3.2.5 Centering – Use the following procedure to check and adjust the display centering.

1. Check that the display is centered in the red shaded area on the alignment template.

2. Turn A103 fully counterclockwise.

3. Center the presentation by rotating the centering tabs on the yoke (Figure 5-7).

NOTE
You can use A103 to move the display presentation a small distance horizontally. If A103 is incorrectly adjusted, the left side of the screen may be distorted.

5.3.2.6 Vertical Linearity – Use the following procedure to check and adjust the character height over the complete screen.

1. Use the character height template (PN 94-03270-03) to check that the heights of the characters located near the four corners and the center of the display are between the minimum and maximum sections of the template.

2. Adjust the vertical linearity control A102.

3. Check and adjust the vertical height and vertical hold if needed.

5.3.2.7 Horizontal Linearity – Use the following procedure to check and adjust the character width over the complete screen.

1. Use the character width template (PN 94-03270-03) to check that the widths of the characters located near the four corners and the center of the display are between the minimum and maximum sections of the template.

2. Adjust the horizontal linearity coil L102 with a monitor alignment tool (PN 29-231290-00).

3. Check and adjust the horizontal width if needed.

5.3.2.8 Vertical Hold – Use the following procedure to check and adjust the vertical hold setting.

1. Turn vertical hold control A101 fully counterclockwise. If the display is not stable (tearing or rolling), turn A101 clockwise until the display is stable. Note the position of the control and continue turning clockwise until the display is not stable. Then turn the control counterclockwise to the position halfway between the positions where the display is not stable.

2. Check and adjust the vertical height and vertical linearity if needed.

5.3.2.9 Focus – Use the following procedure to check and adjust the focus of the screen display.

1. Increase the brightness to the maximum level with the ↑ key in SET-UP. Decrease the brightness eight steps by pressing the ↓ key eight times.

2. Look at the characters at the four corners and in the center of the screen. All the dots in the vertical segment of the E should be visible in each character.

NOTE
Some operators may want the focus incorrectly adjusted to suit personal preference.

If the focus is adjusted correctly, go to step 4.

3. Adjust R122 (Figure 5-6) for the best overall character display.

4. Remove the CRT alignment template, clean the marks from the screen, and replace the terminal top cover if no more adjustments are needed.

5.3.3 Monitor Adjustments (Elston and DIGITAL)

The following paragraphs describe the alignment of the Elston video monitor. You can easily identify the Elston monitor by the location of the flyback transformer (on the monitor sideplate opposite the monitor board). Also, the Elston CRT yoke assembly does not have the connector card.

Make all adjustments under the conditions listed in Paragraph 5.3.

5.3.3.1 Brightness – Use the following procedure to adjust the brightness control on the monitor board.

1. Increase the brightness to the maximum level with the ↑ key in SET-UP.

2. Adjust R109 (Figure 5-8) until you can see the display raster. Then turn R109 in the opposite direction until the raster disappears.

3. Return the brightness to normal intensity by pressing the ↓ key in SET-UP.

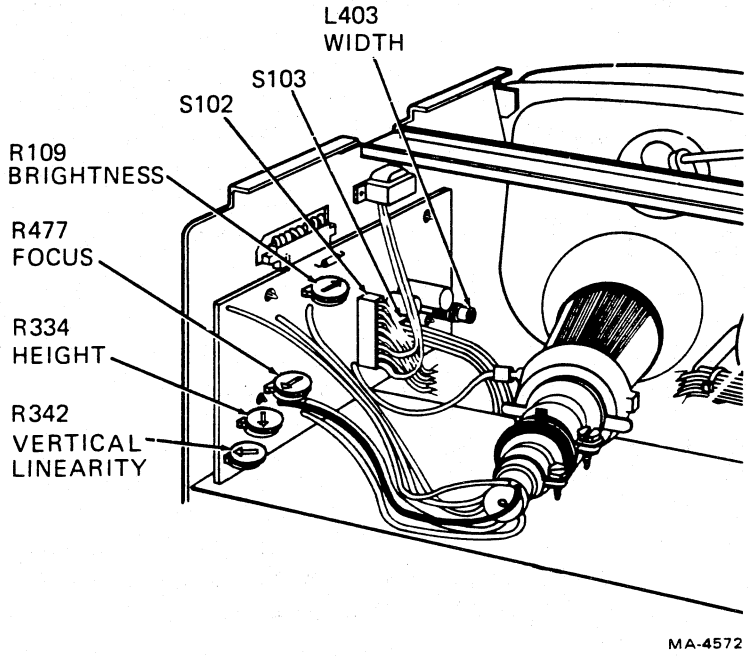


Figure 5-8 Elston Video Monitor Board Adjustments

5.3.3.2 Yoke Rotation – Use the following procedure to check and adjust the yoke.

1. Check that all four sides of the display are parallel to the red shaded area of the alignment template.

2. Loosen the yoke collar clamp screw (Figure 5-9) and turn the yoke until the four sides of the display are parallel to the red shaded area of the alignment template.

3. Check that the yoke is pushed all the way forward toward the face of the CRT. Hold the yoke in place and tighten the yoke collar clamp screen.

5.3.3.3 Vertical Height – Use the following procedure to check and adjust the overall display height.

1. Check that the top and bottom lines of the display are covered by the red shaded area of the adjustment template.

2. Adjust the vertical height control R334.

5.3.3.4 Horizontal Width – Use the following procedure to check and adjust the overall display width.

1. Check that the first and last columns of the display are covered by the red shaded area of the adjustment template.

2. Adjust the horizontal width coil L403 with a monitor alignment tool (PN 29-23190-00).

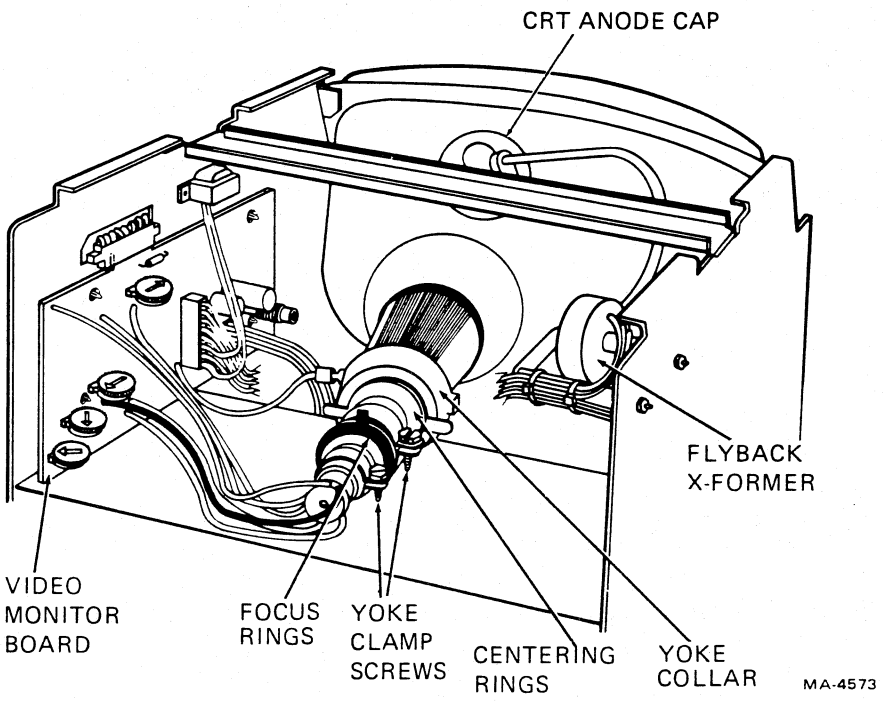


Figure 5-9 Elston Monitor CRT Adjustments

5.3.3.5 Centering – Use the following procedure to check and adjust the display centering.

1. Check that the display is centered in the red shaded area on the alignment template.

2. Center the presentation by rotating the frontmost centering rings on the neck of the CRT (Figure 5-6).

5.3.3.6 Vertical Linearity – Use the following procedure to check and adjust the character height over the complete screen.

1. Use the character height template (PN 94-03270-03) to check that the height of the characters located near the four corners and the center of the display are between the minimum and maximum sections of the template.

2. Adjust the vertical linearity using R342.

3. Check and adjust the vertical height if needed.

5.3.3.7 Focus – Use the following procedure to check and adjust the focus.

1. Increase the brightness to maximum level with the ↑ key in SET-UP. Decrease the brightness eight steps by pressing the ↓ key eight times.

2. Look at the characters at the four corners and in the center of the screen. You should see the individual dots in the vertical segment of the E in each character.

NOTE
Some operators may prefer the focus incorrectly adjusted.

If the focus is adjusted correctly, go to step 5.

3. Adjust R477 (Figure 5-8) for the best overall character presentation.

4. Adjust the focus rings furthest from the yoke for the best focus at all four corners (Figure 5-9). Readjust R477 if needed.

5. Remove the CRT alignment template, clean the marks from the screen, and replace the terminal top cover if no more adjustments are needed.

5.4 MODULE REMOVAL AND REPLACEMENT

This section contains information for removal and replacement of mechanical subassemblies in VT100 series terminals. Unless otherwise noted, each procedure applies to all terminals in the series.

Figure 5-10 lists all of the removal procedures in this chapter and the sequence to perform them in. For example, Figure 5-10 shows that to remove the dc power harness, you must first remove the top cover, bottom cover, and power supply removal procedures.

5.4.1 Access Cover

Use the following procedure to remove the terminal access cover.

1. Remove power from the terminal by disconnecting the ac plug from the ac outlet.

2. Unplug the keyboard.

3. Unplug any connectors from the composite video input/output jacks.

4. Disconnect the communications cable.

5. Disonnect the printer interface cable if installed.

6. Use a flat-blade screwdriver to loosen the four captive screws holding the access cover (Figure 5-11).

7. If the 20 mA current loop option is installed, gently pull the access cover away from the terminal about two inches. Then reach in and disconnect J5 from the terminal controller board.

To install the access cover, perform steps 1 through 7 in reverse.

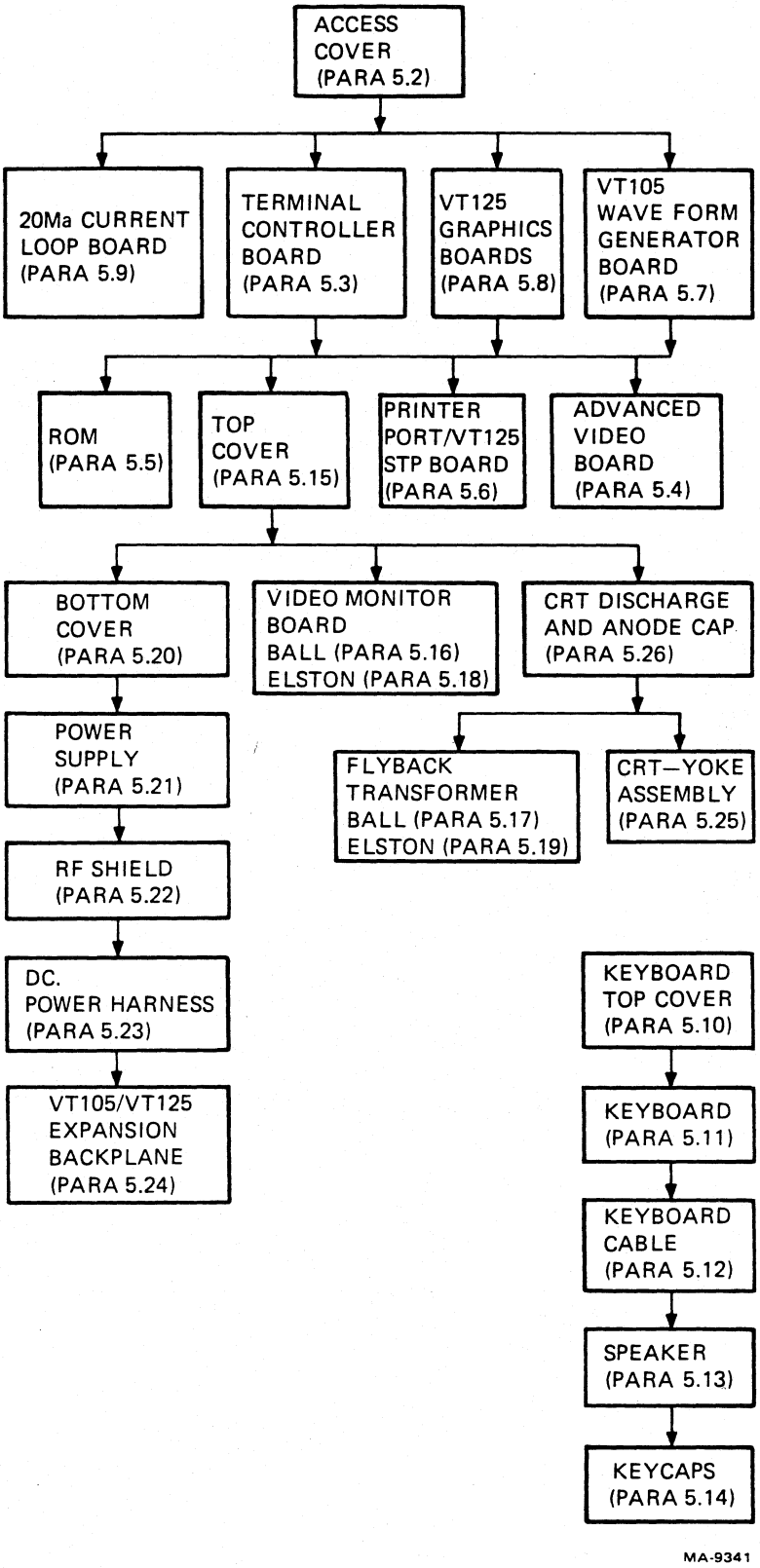


Figure 5-10 Removal Procedures Sequence

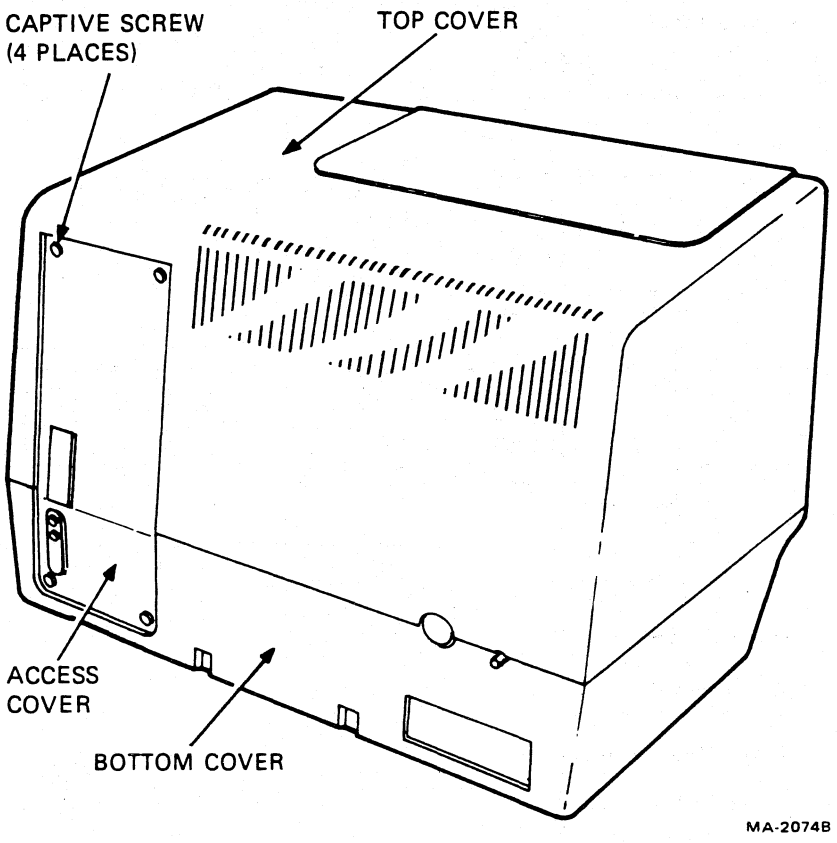


Figure 5-11 VT100 Terminal (Rear View)

5.4.2 Terminal Controller Board

Use the following procedure to remove the terminal controller board.

1. Remove the terminal access cover (Paragraph 5.4.1).

2. Pull the terminal controller board partially out of the card cage. Disconnect the ground wire (if present) from the metal bracket at the EIA connector.

   a. If the terminal is a VT105, disconnect the graphic interface cable from the terminal controller board (Paragraph 5.4.6).

   b. If the terminal is a VT125, refer to Paragraph 5.4.7. After separating the boards, remove the terminal controller board from the card cage. Remove the screw holding the STP board to the terminal controller. Then remove the board.

3. Remove the advanced video board and/or the printer port/STP board if they are installed on the terminal controller board (Paragraphs 5.4.3 and 5.4.5).

To install the terminal controller board, perform steps 1 through 3 in reverse. Make sure to reconnect any ground wires.

NOTE

Always replace an FCC-certified terminal controller board with another certified board. There is a key in the connector to prevent swapping. Do not use an FCC-certified board in a noncertified terminal. The VT125 must use a certified board. The noncertified board is PN 54-13009-00. The certified board is PN 54-13009-03.

Check the terminal controller board for the correct ROM configuration. On -W series and printer ports, you must move the old ROMs to the new board. Refer to Paragraph 5.4.4 for ROM procedures. Refer to Paragraph 5.5 for ROM location information. Remember to reconfigure the terminal to the customer's original SET-UP selections (which should be listed on the keyboard SET-UP label).

The VT105 and VT125 cables are 16-pin cables connecting to an 18-pin connector. The VT105 fits into the top 16 connector sockets and VT125 fits into the bottom 16 connector sockets. Do not misalign the cable in the connector. Refer to Paragraphs 5.4.6 and 5.4.7.

5.4.3 Advanced Video Option Board

Use the following procedure to remove the advanced video (AVO) board.

1. Remove the access cover (Paragraph 5.4.1).
2. Remove the controller board (Paragraph 5.4.2), and, if present, the graphics boards (VT105, Paragraph 5.4.6; VT125, Paragraph 5.4.7)
3. Grasp the advanced video board by its edges and gently but firmly lift the board straight up and off the terminal controller board (Figure 5-12).

To install the advanced video board, perform steps 1 through 4 in reverse.

NOTE

Check the AVO board for the correct ROMs, jumpers, and switch settings (Paragraph 5.5).

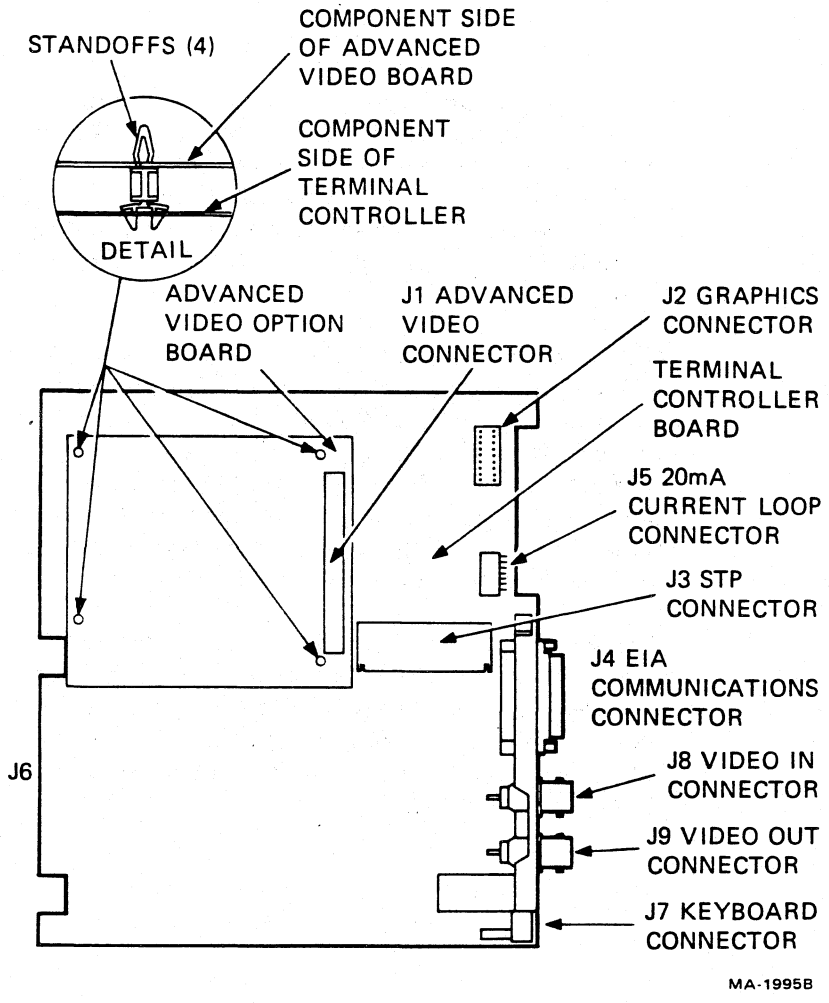


Figure 5-12 Terminal Controller with Advanced Video Board

5.4.4 ROMs

If a ROM is defective, or if the terminal is a variation with special ROMs, this procedure describes how to replace them. Refer to Paragraph 5.5 for ROM positions and part numbers.

1. Remove the old ROM.

2. Unpack the new ROM from its container, but do not remove the ROM from the conductive foam. Gently press the foam against the surface of the terminal controller board to remove static charges. Then remove the ROM from the conductive foam.

3. Refer to Figure 5-13 and align the ROM so the notch on the end is on the same side as the notch on the board socket. Check that all ROM pins are evenly spaced and straight before trying to insert the ROM into the board socket.

4. Using even pressure, press the top of the ROM until it is completely seated into the socket. If you feel a lot of friction, remove the ROM and check for proper pin placement.

5. After the ROM is inserted, make sure all ROM pins are properly seated in the socket.

5.4.5 Printer Port/VT125 STP Board

Use the following procedure to remove the printer port/VT125 STP board.

1. Remove the access cover (Paragraph 5.4.1).

2. Remove the terminal controller board (Paragraph 5.4.2), and, if present, the graphics boards (VT105, Paragraph 5.4.6; VT125, Paragraph 5.4.7).

3. Remove the screw and washer holding the STP connector on the terminal controller board (Figure 5-14).

4. Disconnect the STP board from the STP connector on the terminal controller board.

5. On a VT125, remove the 24-pin flat cable.

To install the printer port/STP board, perform steps 1 through 5 in reverse. For a VT125, refer to Figure 5-15 to install the 24-pin cable.

NOTE

Check the printer port/option board to make sure the correct jumpers are installed or switches set. Refer to Paragraph 5.5 for configuration information.

If you remove the printer port/STP board from the terminal, check that pairs of contacts of STP connector J3 short together to make electrical contact. Adjust separated contacts with a scribe.

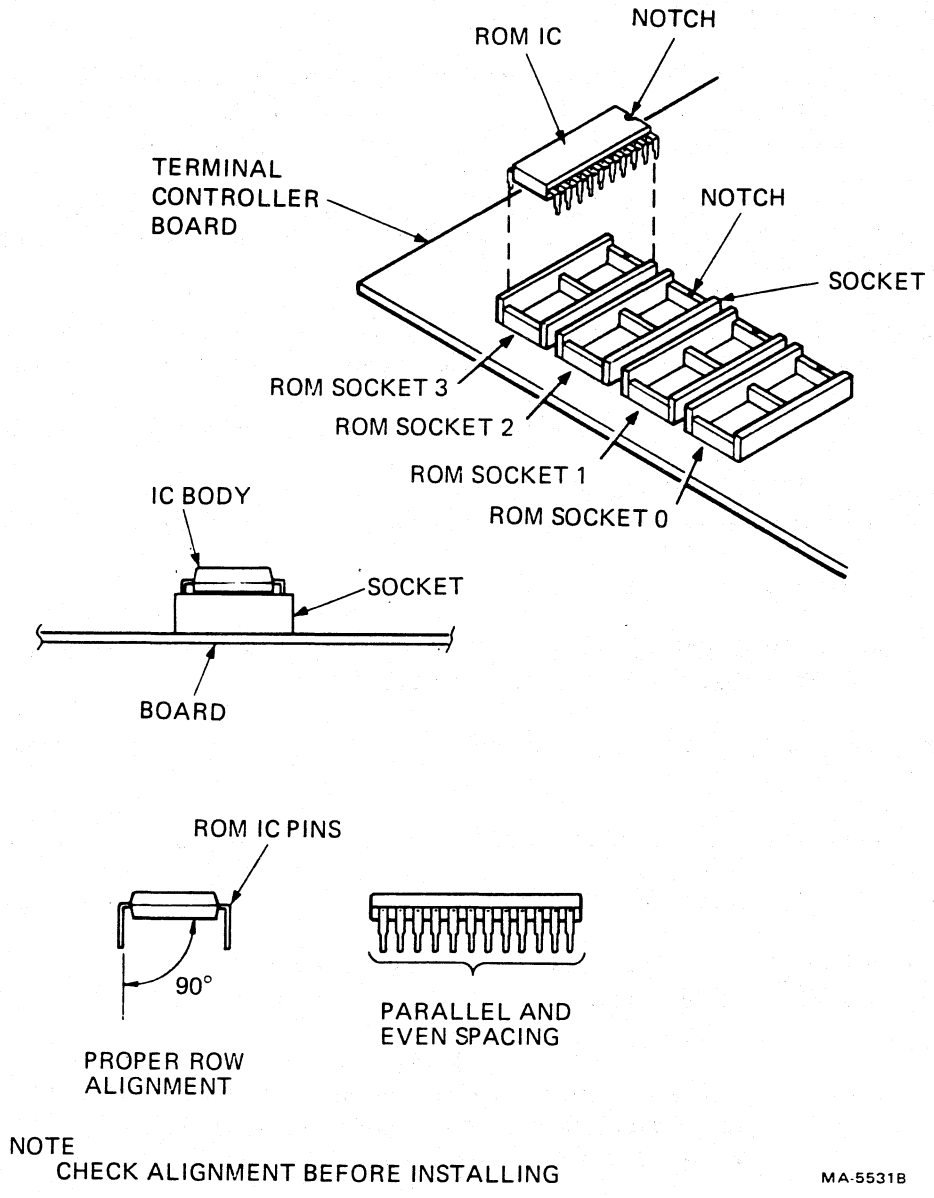


Figure 5-13 Terminal Controller Board ROM Installation

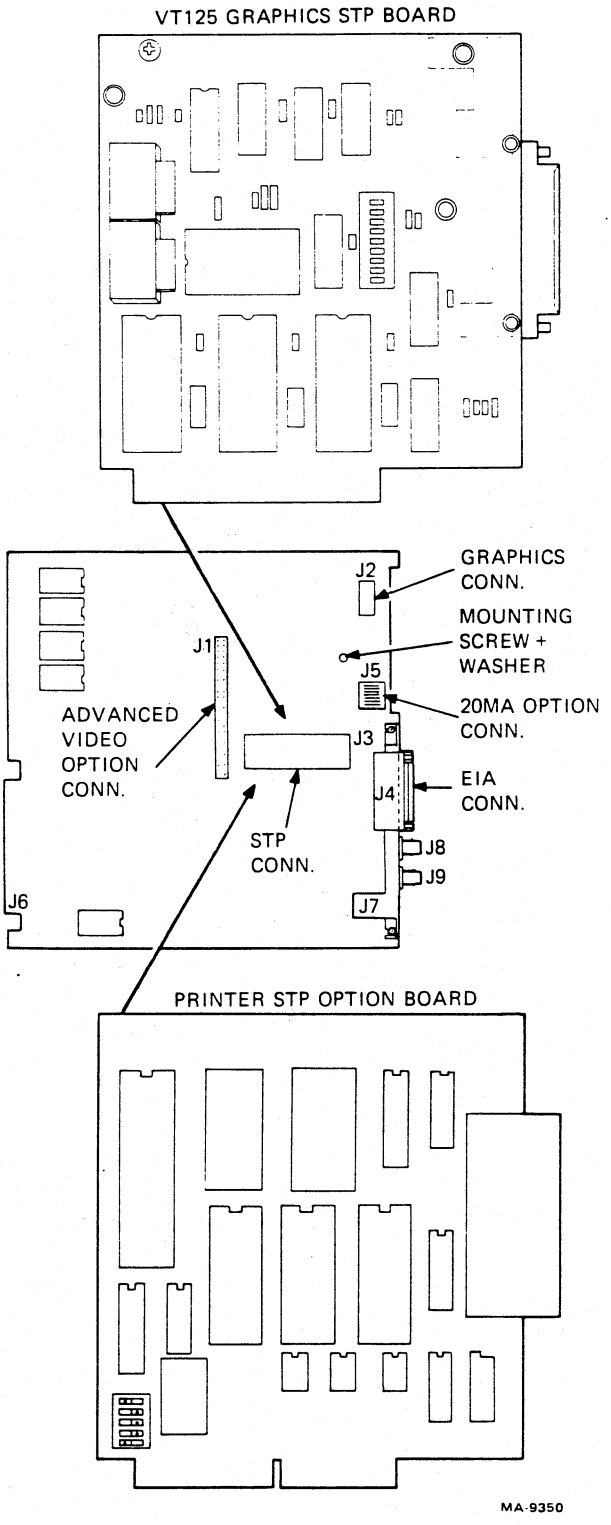


Figure 5-14 Installing Printer Port on VT125 STP Board

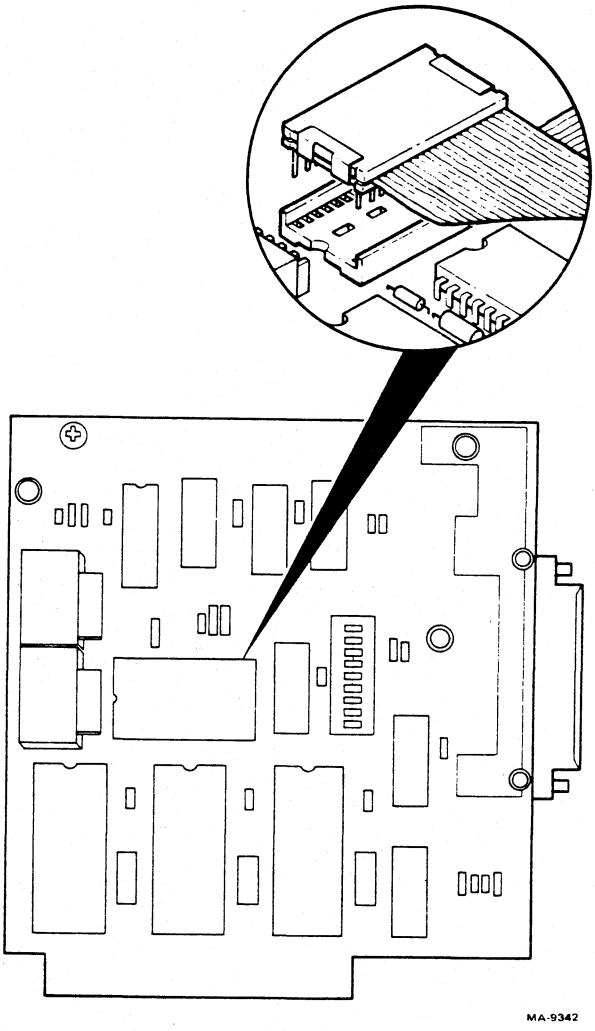


Figure 5-15 VT125 24-Pin Flat Cable on STP Board

5.4.6 VT105 Waveform Generator Board

Use the following procedure to remove the VT105 waveform generator board.

1. Remove the access cover (Paragraph 5.4.1).

2. Disconnect the graphic interconnecting cable from XE90 on the waveform generator board (Figure 5-16).

CAUTION

The graphic interconnecting cable connectors are easily damaged. To prevent damage, use a small screwdriver to alternately lift each end of the connector until it releases from the module.

Refer to Figure 5-16 for correct orientation when reconnecting this cable.

3. Remove the waveform generator board by gently but firmly pulling the board straight out of J2 on the backplane.

To install the waverform generator, perform steps 1 through 3 in reverse.

5.4.7 VT125 Graphics Board

Use the following procedure to remove the VT125 graphics board.

1. Remove the access cover (Paragraph 5.4.1).

2. Pull the terminal controller board and the graphics board partially out of the card cage. Disconnect the ground wire from the BNC connector bracket on the graphics board.

3. Remove the screw holding the STP board to the terminal controller and remove the board (Figure 5-14). Remove the 24-pin cable from the STP board and the graphics board. Remove the 16-pin cable from the terminal controller connector.

4. Pull the graphics board out of the cage.

To install the graphics board, perform steps 1 through 4 in reverse (Figures 5-17 and 5-18).

NOTE

The 16-pin cable connects to the bottom 16 connector sockets. Do not misalign the cable in the connector (Figure 5-17).

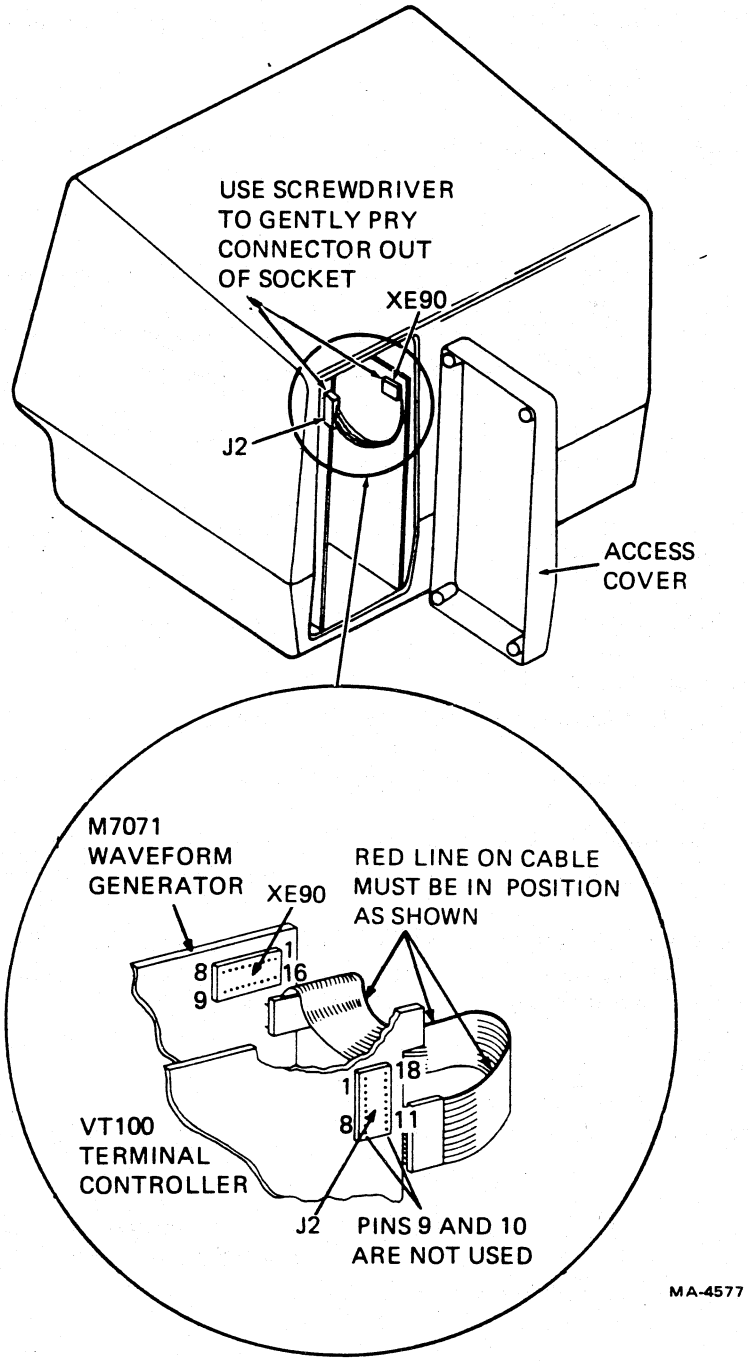


Figure 5-16 VT105 Interconnections

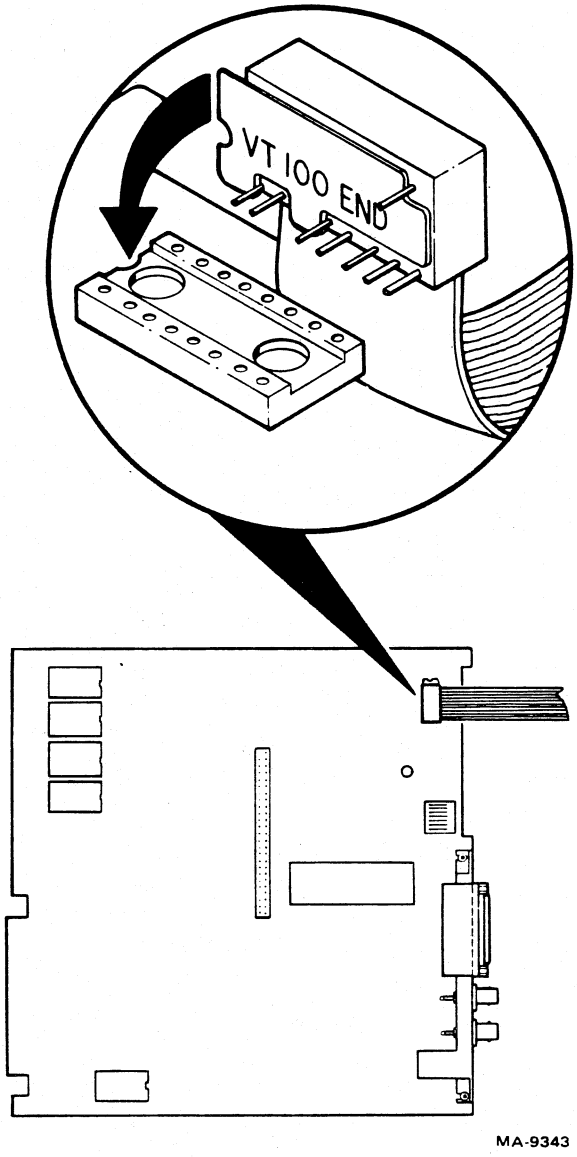


Figure 5-17 VT125 16-Pin Flat Cable on Terminal Controller

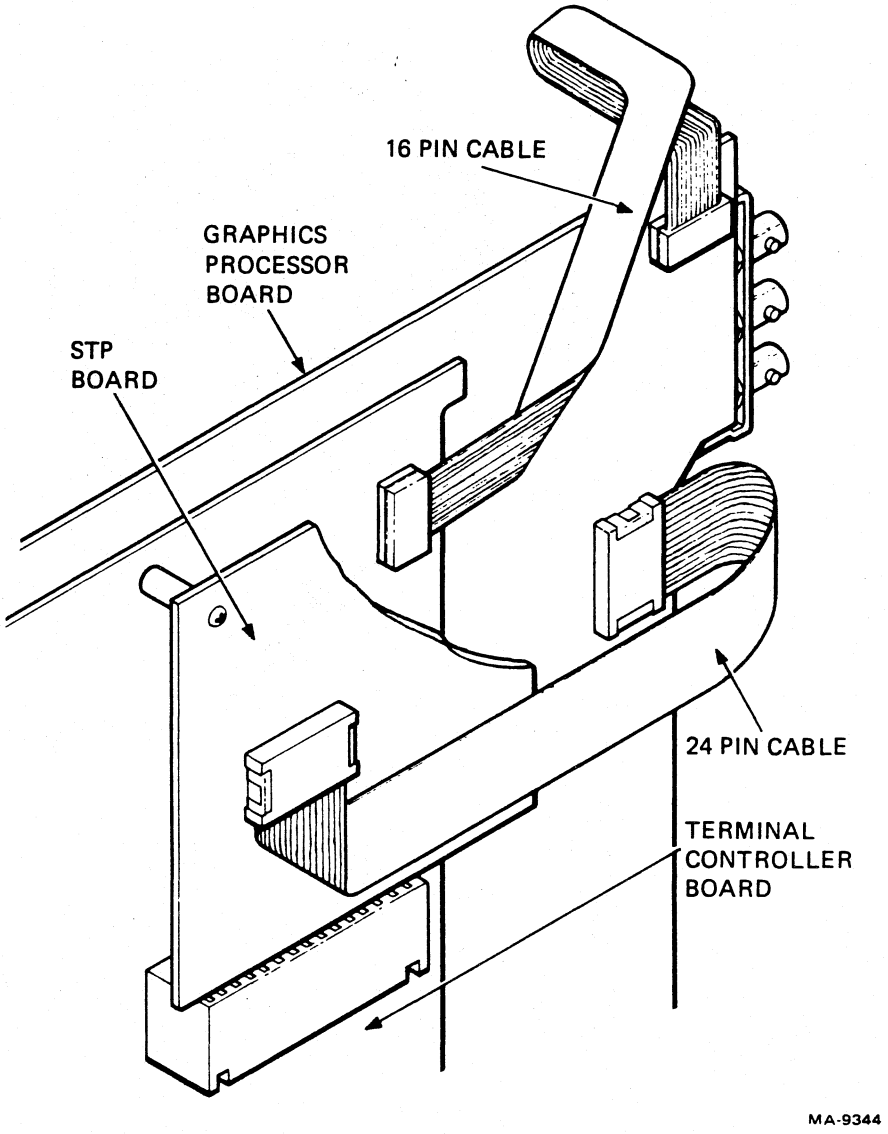


Figure 5-18 VT125 Graphic Cable Connections

5.4.8 20 mA Current Loop Board

Use the following procedure to remove the 20 mA current loop board.

1. Remove the access cover (Paragraph 5.4.1).
2. Use a Phillips screwdriver to remove the two screws holding the Mate-N-Lok connector to the bottom of the access cover.
3. Use a Phillips screwdriver to remove the three screws holding the 20 mA current loop board to the access cover. Then remove the board.

To install the 20 mA current loop board, perform steps 1 through 3 in reverse.

5.4.9 Keyboard Top Cover

Use the following procedure to remove the keyboard top cover.

1. Remove power from the terminal by disconnecting the ac plug.
2. Unplug the keyboard from the monitor.
3. Use a flat-blade screwdriver to loosen the captive screws holding the keyboard together (Figure 5-19).
4. Remove the top cover by lifting it straight up.

To install the keyboard top cover, perform steps 1 through 4 in reverse.

5.4.10 Keyboard

Use the following procedure to remove the keyboard.

1. Remove the keyboard top cover (Paragraph 5.4.9).
2. Disconnect keyboard cable J2 from the keyboard.
3. Remove the keyboard.

To install the keyboard, perform steps 1 through 3 in reverse.

For a terminal with a printer port, move the **PRINT/ENTER** key from the defective keyboard to the new keyboard. For a VT132 keyboard, move the special keycaps to the new board.

5.4.11 Keyboard Cable

Use the following procedure to remove the keyboard cable.

1. Remove the keyboard top cover (Paragraph 5.4.9).
2. Remove the keyboard (Paragraph 5.4.10).
3. Disconnect the keyboard cable from the speaker.
4. Remove the keyboard cable.

To install the keyboard cable, perform steps 1 through 4 in reverse.

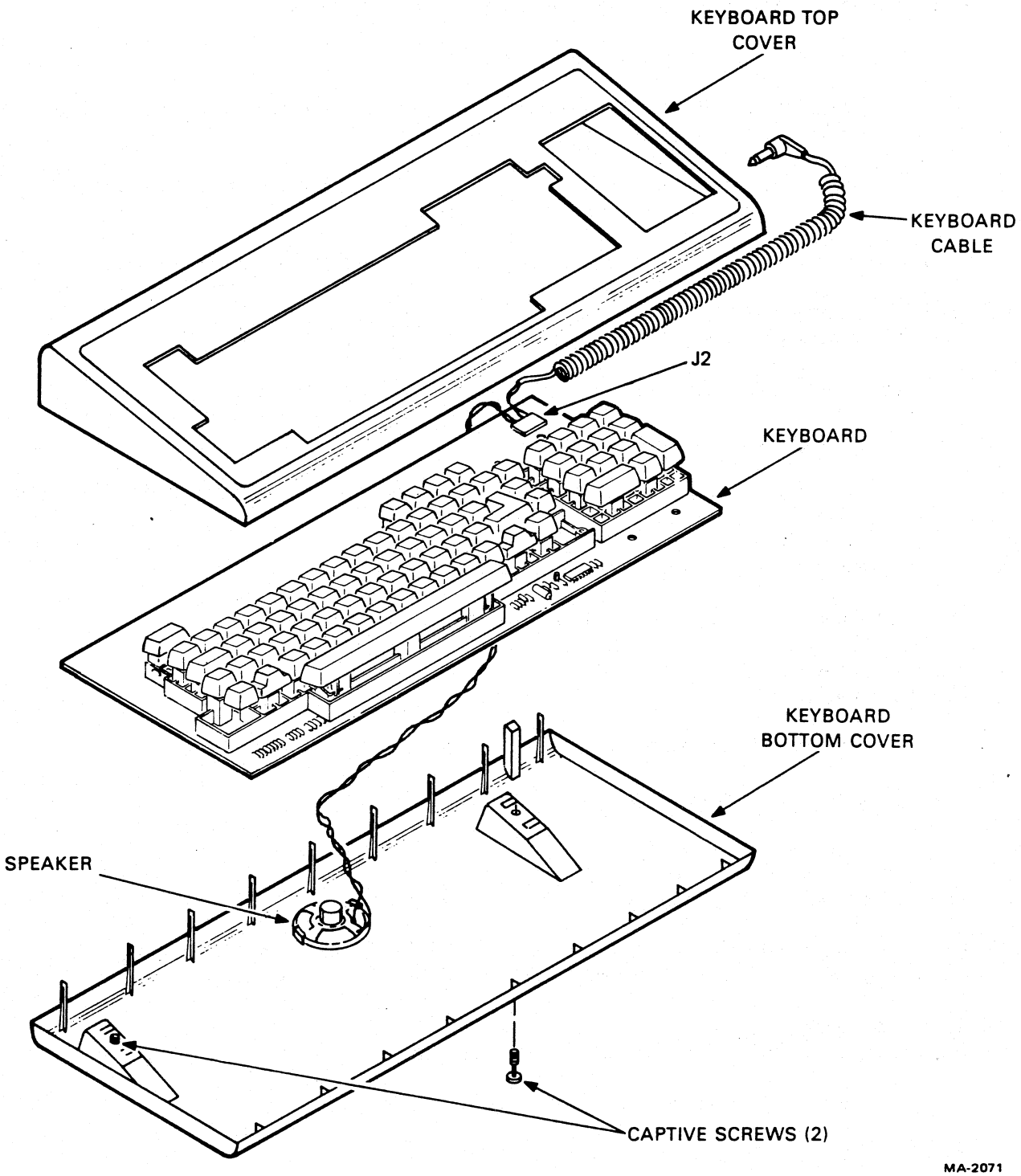


Figure 5-19 Keyboard Disassembly

5.4.12 Keyboard Speaker

Use the following procedure to remove the keyboard speaker.

1. Remove the keyboard top cover (Paragraph 5.4.9).
2. Remove the keyboard (Paragraph 5.4.10).
3. Remove the keyboard cable (Paragraph 5.4.11).
4. Remove the speaker by sliding it toward the front edge of the keyboard cover.

To install the keyboard speaker, perform steps 1 through 4 in reverse.

5.4.13 Keycap

Normally the only tool you need to install keycaps is a keycap puller. In some cases you may need a pair of long nose pliers. Use the following procedure to remove and replace keycaps.

1. Remove power from the terminal by turning it off.
2. Starting at the upper-left corner of the keyboard, insert the keycap puller between the first cap to be replaced and the adjacent keycap (Figure 5-20).
3. Squeeze the puller legs around the cap and slowly pull straight up to remove keycap (Figure 5-20).
4. If the adapter does not come off with the keycap (Figure 5-20), carefully remove adapter with long nose pliers. Reinstall adapter in the keycap, making sure the pointed end faces the front of cap.

NOTE

In some keyboards the adapter and the keycap may be one molded part.

5. In a very few cases the plunger may also come off. If so, take care to prevent the spring from flying out. Refer to Figure 5-20 and replace the plunger and spring as follows.

CAUTION

You must follow this procedure carefully to prevent damage to key contacts.

   a. Slide spring into plunger. Place spring and plunger in slot, and over key contacts. Make sure cross piece of plunger is vertical, not horizontal.

   b. Slowly push plunger down until cross piece touches contacts. Release plunger and check that contacts are separated.

6. Locate proper replacement keycap. Gently press keycap straight down on plunger until it is fully seated.
7. Repeat steps 1 through 6 for each keycap you replace.
8. Store all unused keycaps in shipping bag for later use.

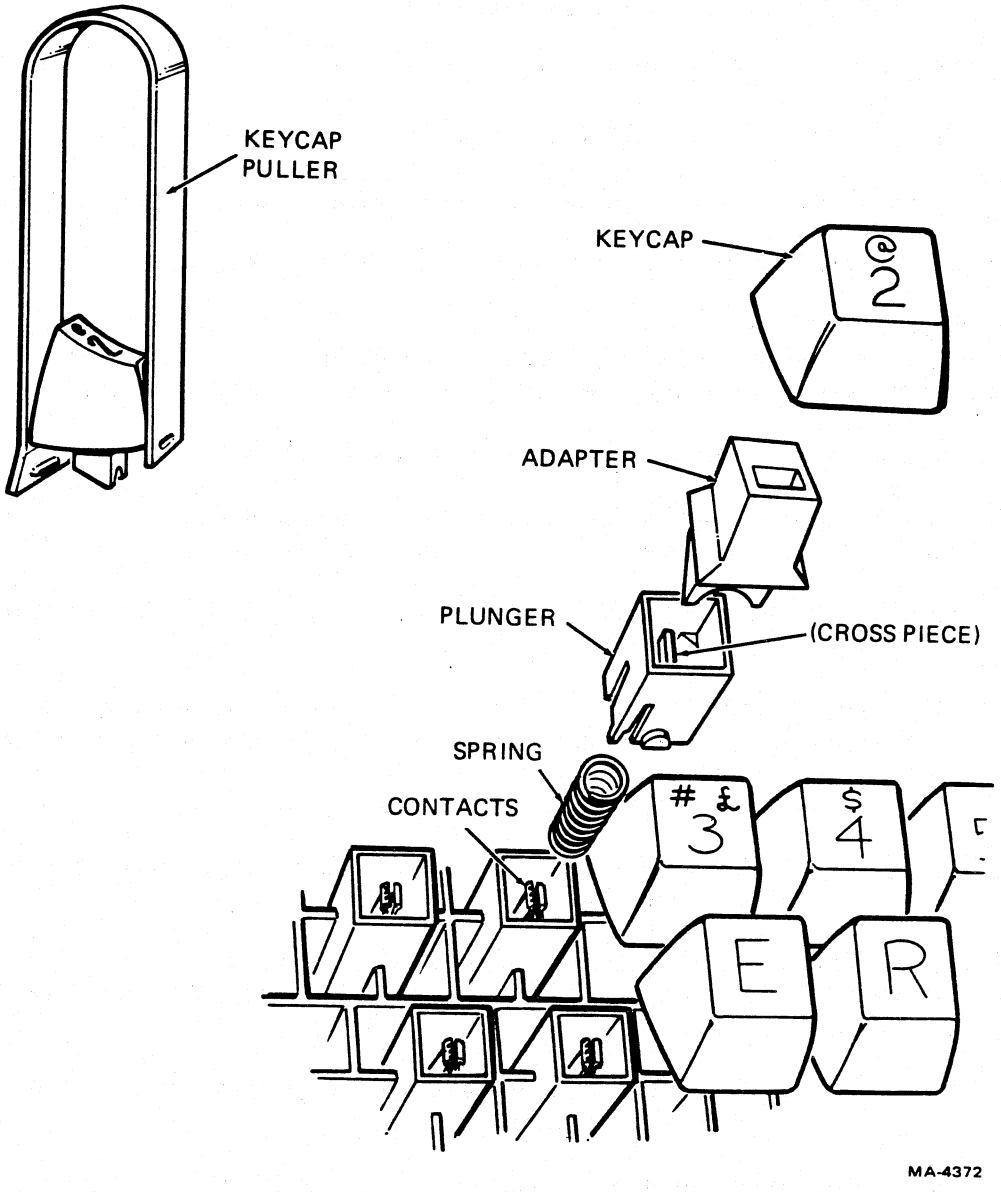


Figure 5-20 Keycap Removal

Use the following procedure to test the new keycaps.

1. Place terminal off-line.

2. Press each new keycap (both lowercase and uppercase) and make sure the proper character(s) appear on the screen.

5.4.14 Top Cover

Use the following procedure to remove the top cover.

1. Remove power from the terminal by disconnecting the ac plug.

2. Unplug the keyboard.

3. Use a small flat-blade screwdriver (or a scribe on newer terminals) to release the two front pop fasteners located under the front lip (Figure 5-21).

4. Use a small flat-blade screwdriver to release the two rear pop fasteners located on the lower rear edge of the bottom cover (Figure 5-21).

5. Remove the top cover by lifting it straight up.

To install the top cover, perform steps 1 through 5 in reverse.

5.4.15 Video Monitor Board (Ball Monitor)

Use the following procedure to remove the video monitor board on a Ball monitor.

1. Remove the top cover (Paragraph 5.4.14).

2. Remove the circular connector from the base of the CRT (Figure 5-22). Bend the wire harness up and out of the way.

3. Disconnect the four wires from the yoke connection card.

   Tab 1 – White with Yellow
   Tab 2 – Red
   Tab 3 – Blue
   Tab 4 – Brown

4. Disconnect 4-wire connector J102 at the bottom of the video monitor board.

5. Disconnect 7-wire connector J104 at the bottom-center of the video board. Move the harness up and out of the way.

6. Disconnect the green ground wire.

7. Disconnect video input cable J101 from the top edge of the video monitor board.

8. Release the four standoffs and remove the video monitor board.

To install the video monitor board, perform steps 1 through 8 in reverse.

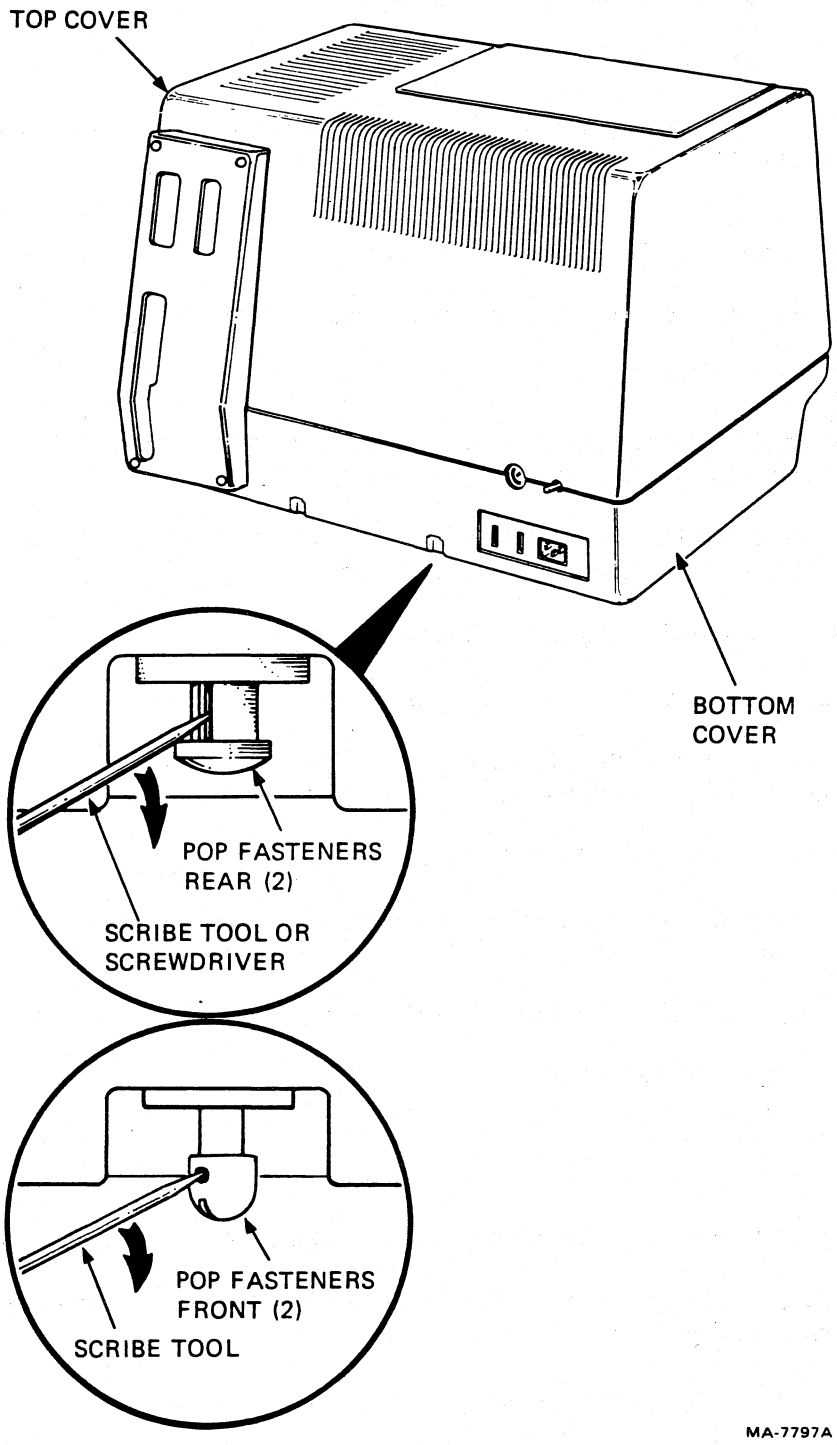


Figure 5-21 Top Cover Removal

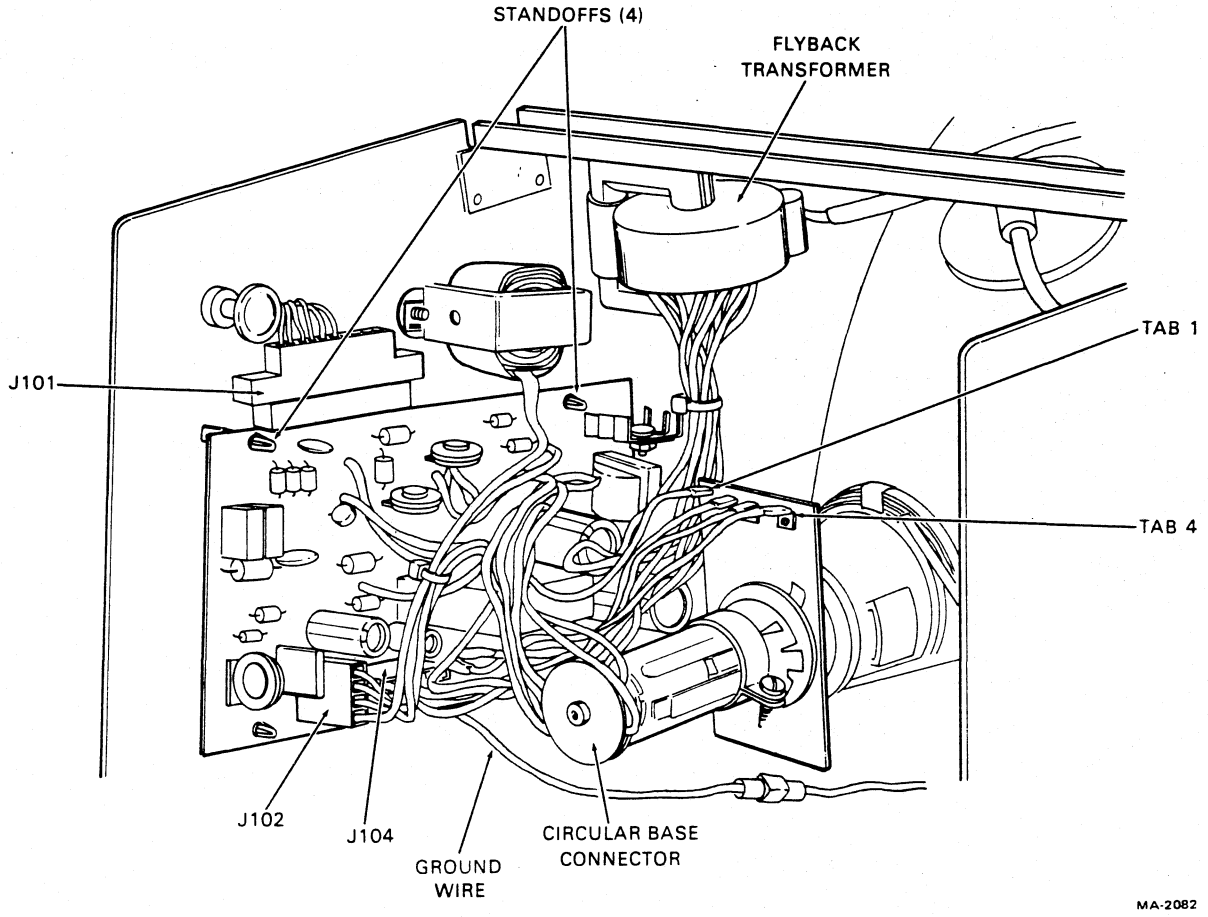


Figure 5-22 Ball Video Monitor Board Removal

5.4.16 Flyback Transformer (Ball Monitor)

Use the following procedure to remove the flyback transformer from the Ball monitor.

WARNING

The CRT anode may contain a stored high voltage. Refer to Paragraph 5.4.25 for the anode discharge procedure.

1. Remove the top cover (Paragraph 5.4.14).
2. Disconnect 7-wire connector J104 at the bottom-center of the video monitor board. Move the harness up and out of the way (Figure 5-22).
3. Discharge the high voltage at the CRT anode. Refer to Paragraph 5.4.25 for the procedure.
4. Disconnect the CRT anode wire from the CRT. Refer to Paragraph 5.4.25 for the procedure.
5. Use a 1/4-inch nutdriver to remove the two nuts mounting the flyback transformer to the horizontal crossbrace, and remove the transformer.

To install the flyback transformer, perform steps 1 through 5 in reverse.

5.4.17 Video Monitor Board (Elston or DIGITAL)

Use the following procedure to remove the video monitor board from an Elston or DIGITAL monitor.

1. Remove the top cover (Paragraph 5.4.14).
2. Remove the circular connector from the base of the CRT (Figure 5-23).
3. Disconnect the white wire connecting the video monitor board to the yoke ground lug.
4. Disconnect the 8-pin connector from the video monitor board.
5. Disconnect the 4-pin connector from the video monitor board.
6. Disconnect the video input connector from the top edge of the video monitor board.
7. Release the four standoffs and remove the video monitor board.

To install the video monitor board, perform steps 1 through 7 in reverse.

CAUTION

Do not misalign the 8-pin connector when reconnecting the cable. You may damage the monitor board if the connector is not correctly installed.

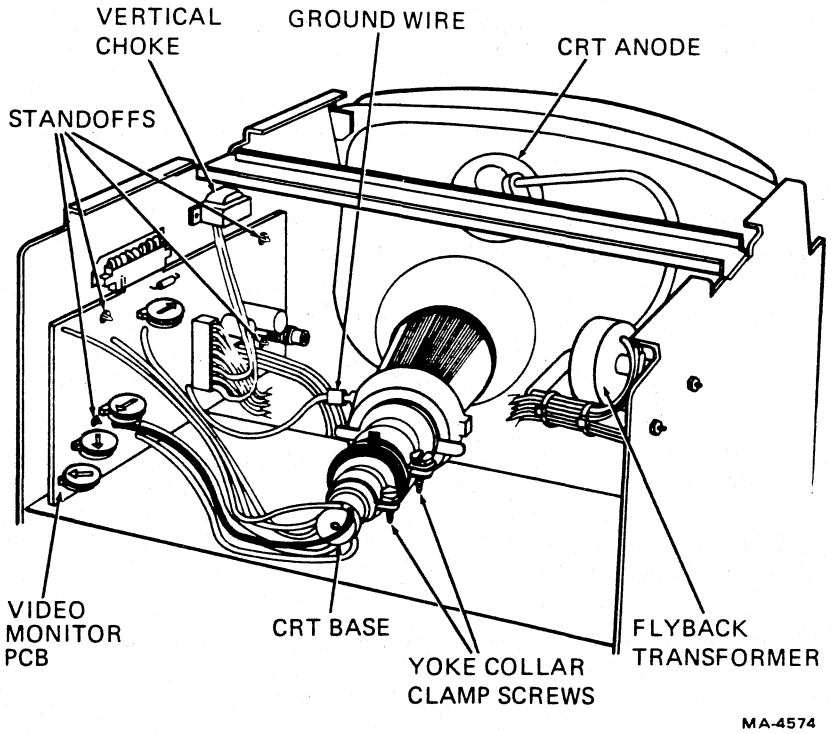


Figure 5-23 Elston/DIGITAL Video Monitor Board Removal

5.4.18 Flyback Transformer (Elston or DIGITAL)

Use the following procedure to remove the flyback transformer from an Elston or DIGITAL monitor.

WARNING

The CRT anode may contain a stored high voltage. Refer to Paragraph 5.4.25 for the anode discharge procedure.

1. Remove the top cover (Paragraph 5.4.14).
2. Disconnect the 8-pin connector from the video monitor board.
3. Remove the screw and washer securing the vertical choke to the monitor chassis. Remove the vertical choke.
4. Discharge the high voltage at the CRT anode. Refer to Paragraph 5.4.25 for the procedure.
5. Disconnect the CRT anode wire from the CRT. Refer to Paragraph 5.4.25 for the procedure.
6. Use a 1/4-inch nutdriver to remove the two nuts mounting the flyback transformer to the monitor chassis.

To install the flyback transformer, perform steps 1 through 7 in reverse.

CAUTION

Do not misalign the 8-pin connector when reconnecting the cable. You may damage the monitor board if the connector is not correctly installed.

5.4.19 Bottom Cover

Use the following procedure to remove the bottom cover.

1. Remove the top cover (Paragraph 5.4.14).
2. Disconnect the power cord from the terminal.
3. Turn the terminal over on its side and remove the four shipping screws (if present) securing the bottom cover to the chassis. Discard the screws and turn the terminal up.
4. Locate the four pop fasteners holding the frame to the base and release the fasteners by pulling the plungers up.
5. Grasp the metal frame and lift the frame up and out of the terminal bottom cover.

To install the bottom cover, perform steps 1 through 6 in reverse.

5.4.20 Power Supply

Use the following procedure to remove the power supply.

1. Remove the top cover (Paragraph 5.4.14).

2. Remove the bottom cover (Paragraph 5.4.19).

3. Locate the three pop fasteners on the side of the chassis. Release the pop fasteners by pulling the plungers out (Figure 5-24).

WARNING

Capacitors C9, C14, and the surrounding circuits contain a 300 Vdc charge. To discharge the capacitors, leave the power supply plugged into the terminal for a minimum of four minutes after the power cord is removed.

To assure complete discharge of the capacitors after the power supply is out of the terminal, short the capacitors with an insulated wire as shown in Figure 5-25.

4. Grasp the power supply by the end plate and remove by pulling it straight out.

To install the power supply, perform steps 1 through 4 in reverse. Note that there is a grounding tab on the chassis at the back that fits into a small slot in the end of the power supply's switch plate.

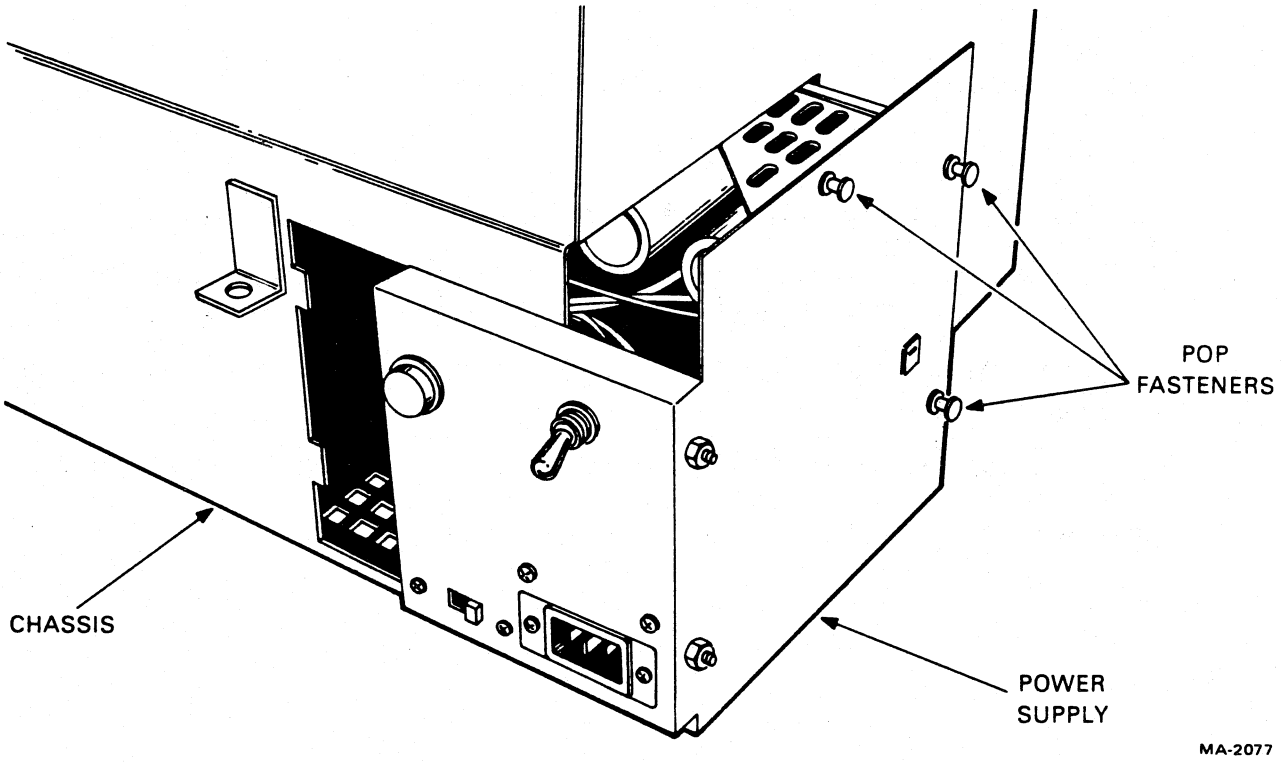


Figure 5-24 Power Supply Removal

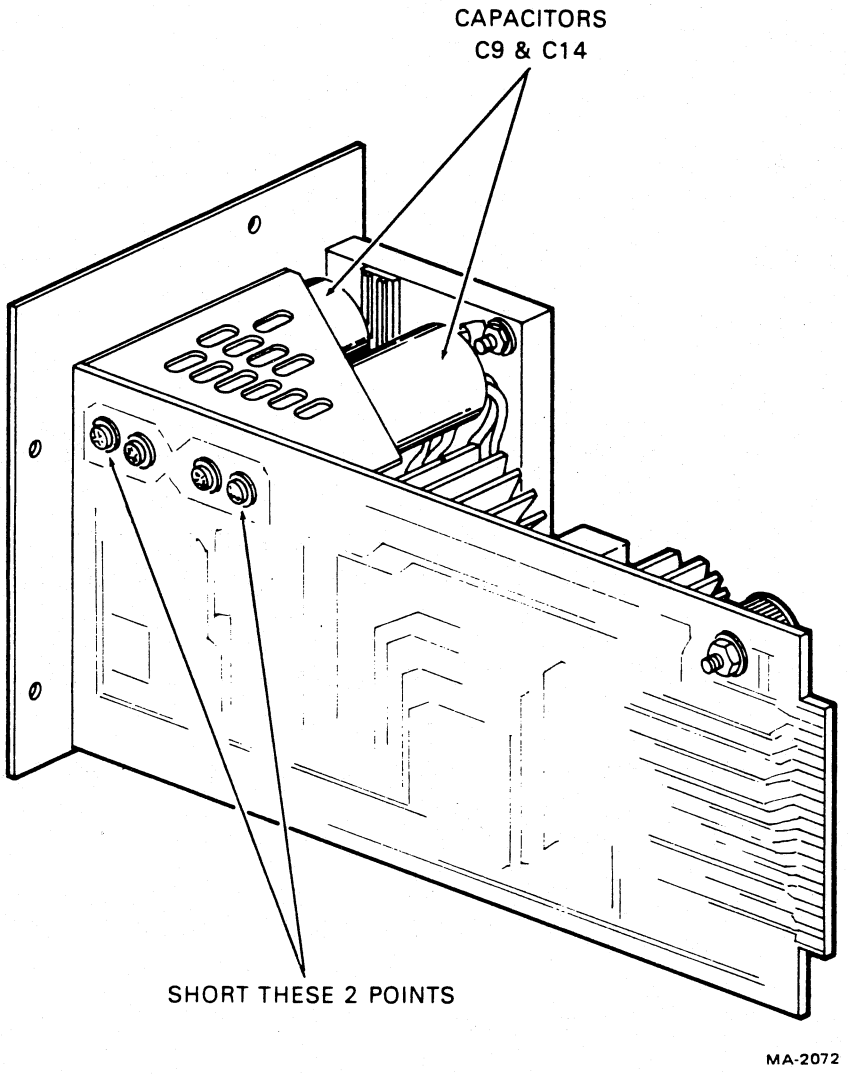


Figure 5-25 Power Supply Capacitator Discharging

5.4.21 RF Shield

Use the following procedure to remove the RF shield for the VT125.

1. Remove the top cover (Paragraph 5.4.14).
2. Remove the bottom cover (Paragraph 5.4.19).
3. Remove the power supply (Paragraph 5.4.20).
4. Remove the terminal controller board (Paragraph 5.4.2) and, if present, the graphics boards (VT105, Paragraph 5.4.6; VT125, Paragraph 5.4.7).
5. Loosen, but do not remove, two Phillips screws at the top of the shield (Figure 5-26).
6. Set the chassis on end with the cage up.

NOTE

The terminal rests on several parts that stick out on the bottom. Set the terminal on a protected surface to prevent damage.

The bumpers attached to both sides of the chassis protect the terminal during shipping. You can remove them now if necessary.

7. Loosen, but do not remove, two Phillips screws at the bottom of the shield.
8. Slide the shield off the cage. Push the ribbon cable (front of the terminal) and the ground wires (at access opening) as needed to avoid catching the wires on the sheet metal.
9. Tighten the four screws temporarily and set the terminal on its bottom.

To install the shield, perform steps 1 through 9 in reverse. At step 8, compress the metal contact fingers on the shield (Figure 5-26) by pressing on the shield until the indicated parts touch.

5.4.22 DC Power Harness

Use the following procedure to remove the dc power harness.

1. Remove the top cover (Paragraph 5.4.14).
2. Remove the bottom cover (Paragraph 5.4.19).
3. Remove the power supply (Paragraph 5.4.21).
4. Remove the terminal controller board (Paragraph 5.4.2) and, if present, the graphics boards (VT105, Paragraph 5.4.6; VT125, Paragraph 5.4.7).
5. Remove the RF shield if present (Paragraph 5.4.21).
6. Disconnect 10-pin edge connector J101 from the video monitor board.
7. Remove the card cage by releasing the two pop fasteners (remove two Phillips screws on newer terminals) that hold the top of the card cage to the chassis. Tilt the card cage out slightly, then lift the card cage out of the bottom holding clips (chassis slots on newer terminals).

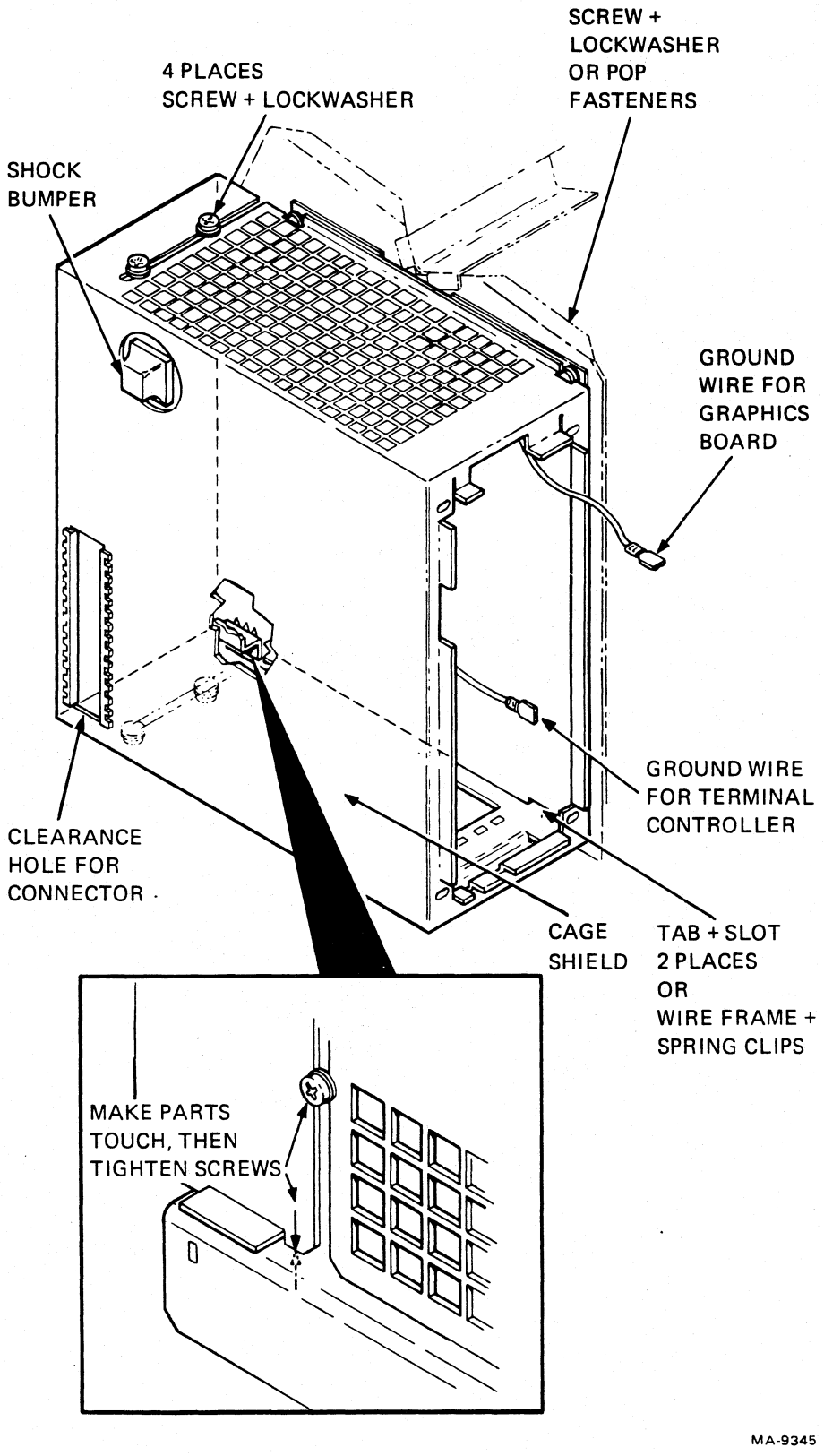


Figure 5-26 FCC Shield on VT100 Cage

8. Disconnect the ground wire from the 10-pin connector to the monitor chassis.

9. *For a VT100:* Remove the two E-ring fasteners (spread the spring clips on late model terminals) holding the 22-pin edge connector to the card cage, then remove the connector (Figure 5-27).

   For a VT105 or VT125: Disconnect the 22-pin edge connector from the expansion backplane (Figure 5-28).

10. Remove the two E-ring fasteners (spread the spring clips on newer terminals) holding the 18-pin edge connector to the chassis, then remove the connector.

11. Remove the dc power harness.

To install the dc power harness, perform steps 1 through 11 in reverse.

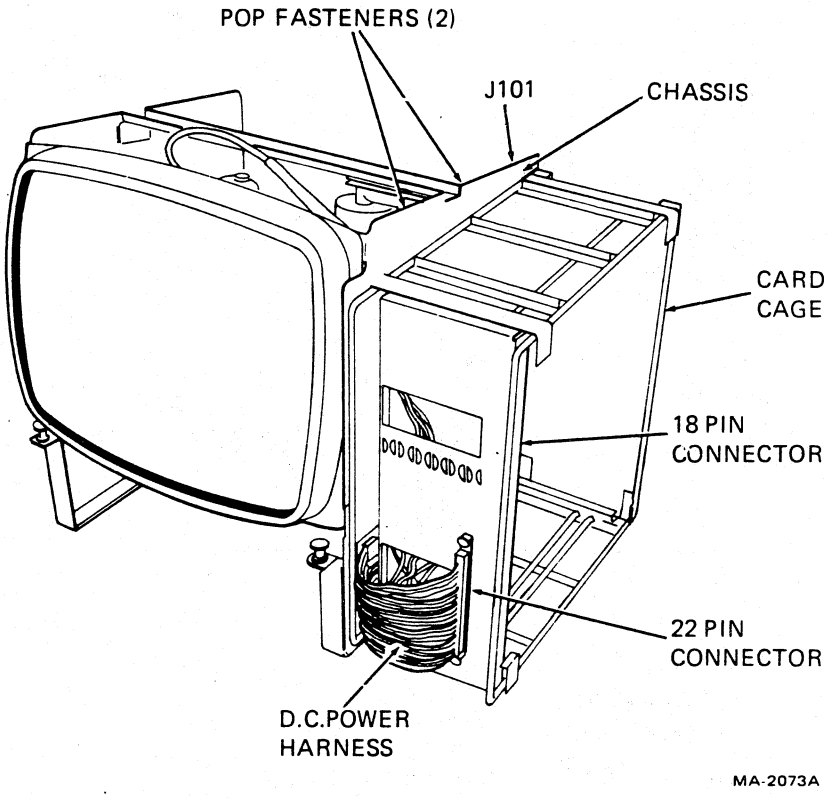


Figure 5-27 VT100 DC Power Harness Removal

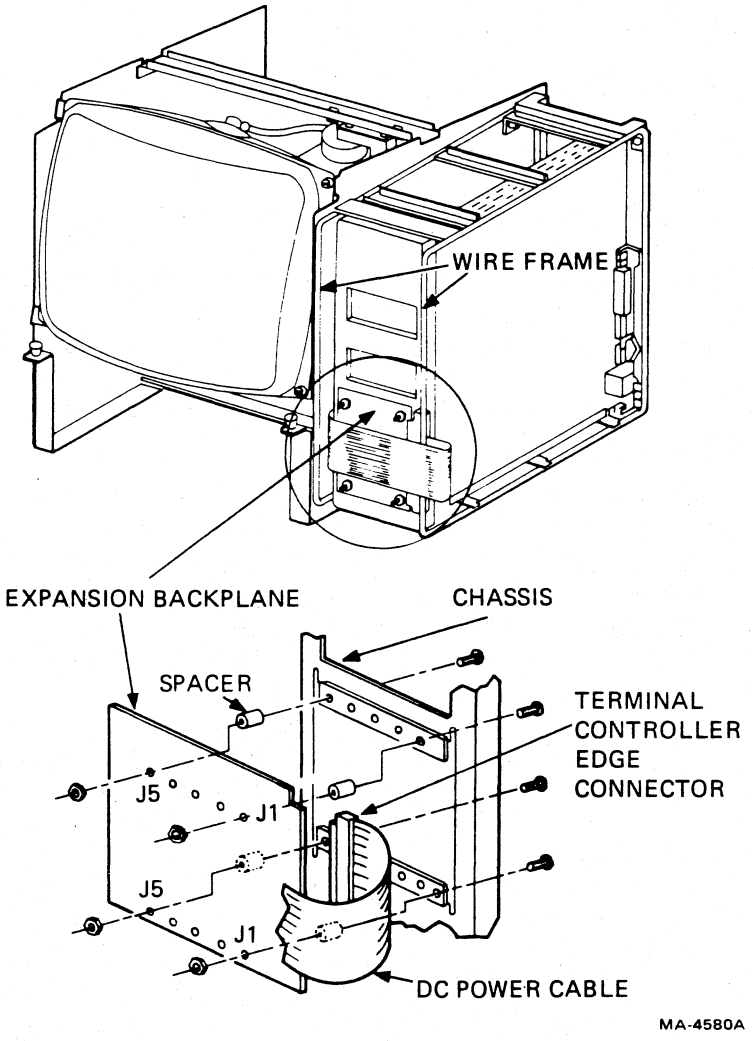


Figure 5-28 Expansion Backplane

5.4.23 VT105/VT125 Expansion Backplane

Use the following procedure to remove the VT105/VT125 expansion backplane.

1. Remove the access cover (Paragraph 5.4.2).
2. Remove the terminal controller and graphics boards (Paragraphs 5.4.2, 5.4.6, 5.4.7).
3. Remove the top cover (Paragraph 5.4.14).
4. Remove the bottom cover (Paragraph 5.4.19).
5. Remove the power supply (Paragraph 5.4.20).
6. Remove the RF shield if present (Paragraph 5.4.21).
7. Disconnect the ground wire from the 10-pin connector to the monitor chassis.
8. Disconnect the 22-pin edge connector from the expansion backplane (Figure 5-28).
9. Remove the four screws and nuts, and two spacers securing the expansion backplane to the card cage.

To install the expansion backplane, perform steps 1 through 6 in reverse.

5.4.24 CRT and Yoke Assembly

You can repair Elston terminals with new CRT and yoke assemblies without replacing the complete chassis assembly (Field Service Monitor Assembly). If you replace the CRT and yoke on Ball monitors, replace the flyback, choke, and monitor board with Elston parts at the same time.

WARNING
High voltage is present at the CRT anode. Refer to Paragraph 5.4.25 for the anode discharge procedure.

1. Disconnect the terminal from the power outlet.
2. Remove the top cover (Paragraph 5.4.14).
3. Discharge the CRT anode (Paragraph 5.4.25).
4. Disconnect the CRT high voltage anode wire (Paragraph 5.4.25).
5. Disconnect the circular connector from the CRT base (Figure 5-23).
6. Disconnect the white wire connecting the video monitor board to the yoke ground connector.
7. Disconnect the 4-pin yoke connector from the monitor board.

8. Remove the top two, then bottom two screws from the CRT frame while supporting the assembly from the bottom of the CRT.

9. Remove the CRT yoke assembly.

WARNING
Handle the tube by the sides next to the face, never by the neck. Do not rest the tube on its neck.

To replace the CRT yoke assembly, perform steps 1 through 8 in reverse.

NOTE
Refer to Paragraph 5.4.26 for the proper CRT storage and disposal procedures.

5.4.25 CRT Discharge and Anode Cap

Use the following procedures to discharge the CRT anode, and remove and install the anode cap.

CRT Anode Discharge

Before you service the CRT or its associated circuits, you must discharge the anode. You can safely use either of the following methods (Figure 5-29).

- Connect the plug end of a VOM lead to chassis ground, and discharge the anode by touching the probe to the CRT anode.

- Gently slip the end of an insulated-handle screwdriver under the plastic anode cap on top of the CRT while shorting the other end of the screwdriver to an unpainted area of the CRT frame.

Anode Cap

Disconnect the heavy CRT anode wire from the CRT as follows.

1. Note the position of the anode wire.

2. The connector holds itself in place with spring barbs in the depression of the tube (the anode socket). You must push against one barb, allowing the other side to clear the lip of the anode socket (Figure 5-30).

3. Push at a right angle in the direction that the wire enters the rubber cap.

4. While pushing across, push up on the cap to free one barb.

5. Now push up in the opposite direction to free the other barb.

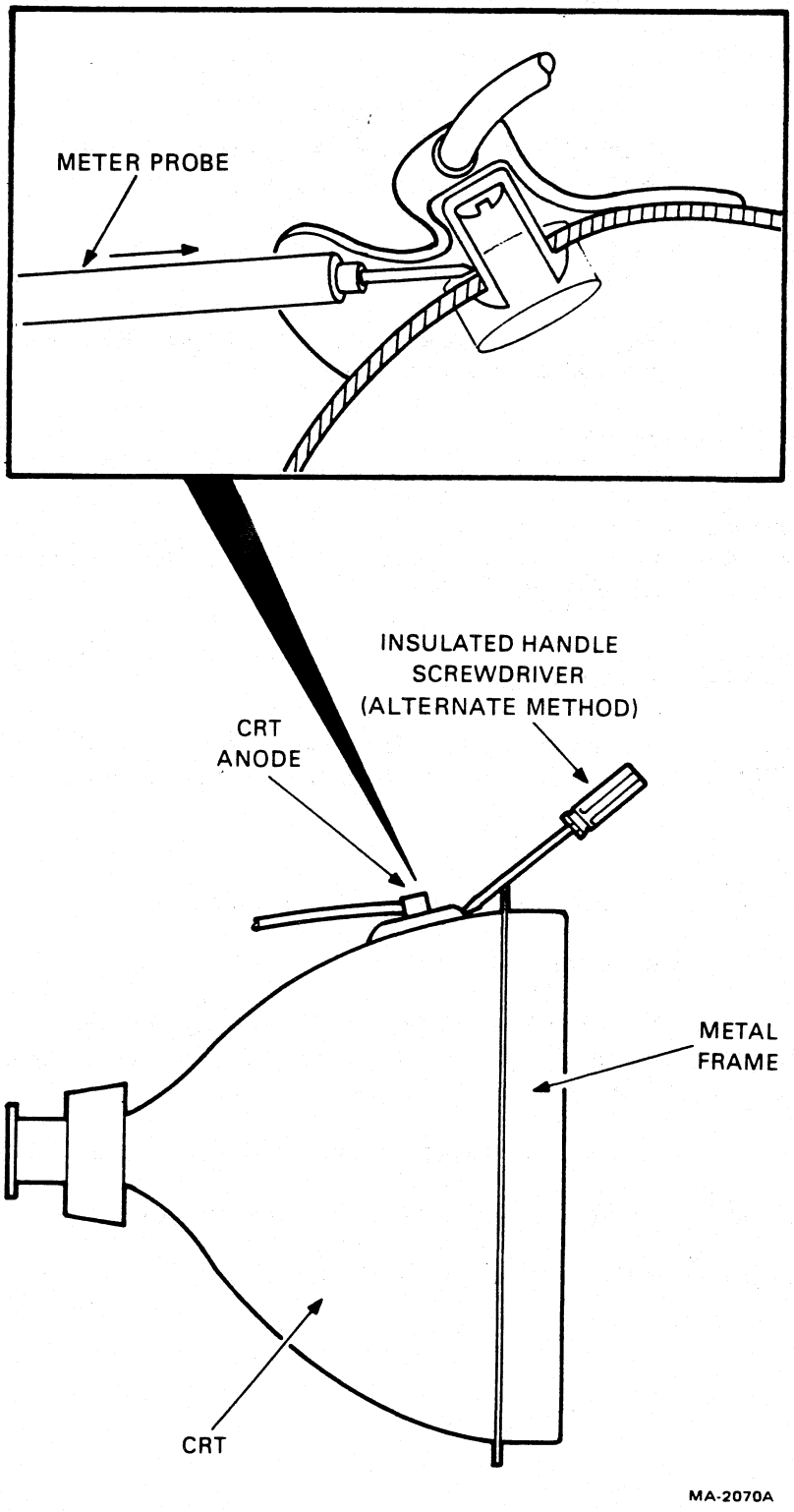


Figure 5-29 CRT Anode Discharging

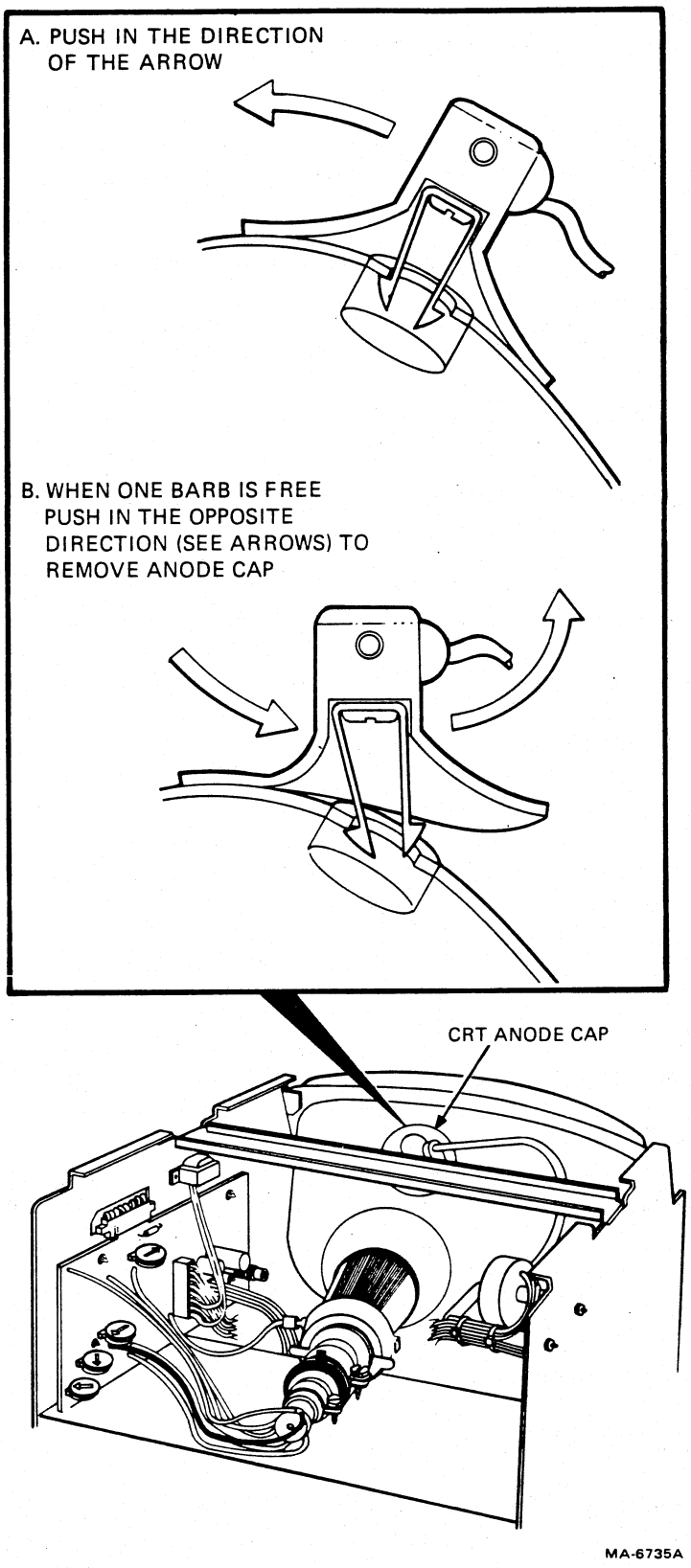


Figure 5-30 Removing Anode Cap

5.4.26 Field Handling of CRTs

You must use the following procedures when handling CRTs in the field.

CRT Replacement

1. Replace CRTs only in areas where risks and exposure are limited to trained Field Service personnel.

2. Only DIGITAL service personnel should be in the area during replacement.

3. Any serviceperson relacing a CRT must wear, at least, safety glasses with side guards, or goggles and gloves. The part numbers are as follows.

Goggles	PN 29-16141
Gloves	PN 29-16146

4. Before servicing the CRT or its associated circuits, you must discharge the anode (Paragraph 5.4.25).

CRT Handling

Take the following precautions when handling any CRT.

- Handle the CRT by the sides next to the tube face. Never handle the CRT by the neck.
- Do not allow the neck to strike anything.
- Never rest a CRT on its neck.
- Never scratch the glass of the CRT. Be particularly careful of this when working around the CRT with any tool.
- Never touch the glass of a CRT with a hot soldering iron.

CRT Storage

All CRTs must be stored in a closed shipping container or correctly mounted in the product. Never store a CRT without a protective enclosure.

CRT Disposal

If a regional disposal procedure does not exist in your area, use the following steps to safely dispose of a CRT. Destroy any CRT that is to be scrapped and not returned for repair.

WARNING

Use extreme caution when performing this procedure.

1. Place the bad CRT in the container that the new CRT was received in.

2. Close and seal the container, leaving only the end of the CRT neck exposed (Figure 5-31).

3. Slowly crush the CRT evacuation point with a pair of pliers or wire cutters. The evacuation point is located in the center of the CRT neck end. If the procedure is done correctly you will hear a quick rush of air. This means that the CRT no longer has a vacuum and can no longer implode.

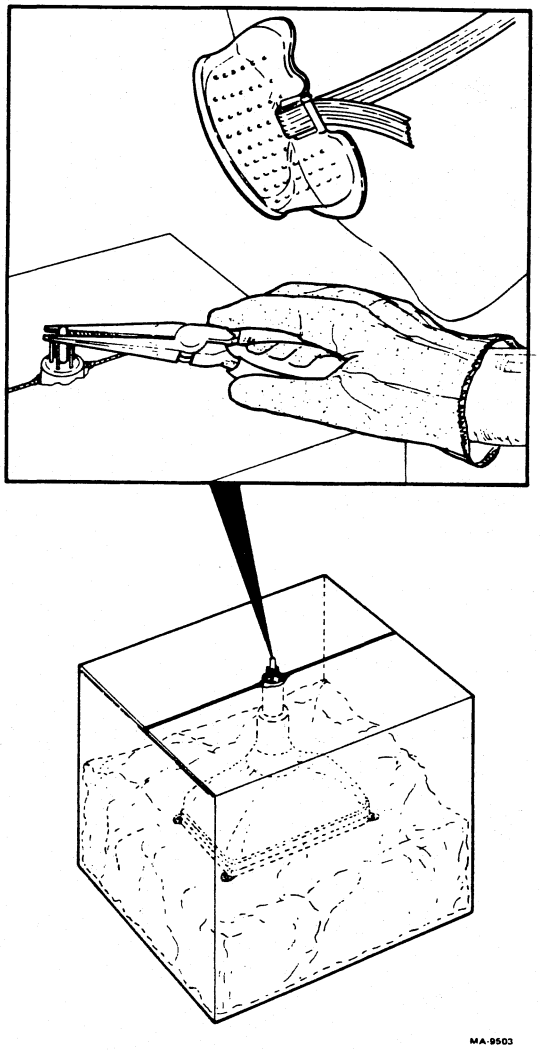


Figure 5-31 CRT Disposal

5.5 BOARD CONFIGURATIONS

This section contains the information required to configure all boards in the following terminals.

VT100 and all optional configurations
VT105
VT125
VT132

5.5.1 Terminal Controller Board

Use Table 5-7 with Figure 5-32.

5.5.2 Advanced Video Option Board with Jumpers

Use Tables 5-8 and 5-9 with Figure 5-33

5.5.3 Advanced Video Option Board with Switches

Use Tables 5-9 and 5-10 with Figure 5-34.

5.5.4 VT1XX-AC Printer Port Option

The factory settings are switches 1 and 5 on; switches 2, 3, and 4 off. Do not change these settings. See Figure 5-35.

5.5.5 VT105 Waveform Generator Board

See Figure 5-36.

5.5.6 VT125 Graphics Terminal STP Board

See Figure 5-37.

Table 5-7 Terminal Controller Board ROMs

Used In	ROMs Used				Character Generator
	ROM 0	ROM 1	ROM 2	ROM 3	
VT100	23-031E2 or 23-061E2	23-032E2	23-033E2	23-034E2	–
VT100-WC-WK	23-095E2	23-096E2	23-139E2	23–140E2	23-094E2
VT100/VT1XX-AC	23-095E2	23-096E2	23-139E2	23-140E2	–
VT132	23-095E2	23-096E2	23-097E2	23-098E2	–
	or 23-180E2	23-181E2	23-182E2	23-183E2	–
VT125 and VT105	23-061E2	23-032E2	23-033E2	23-034E2	–

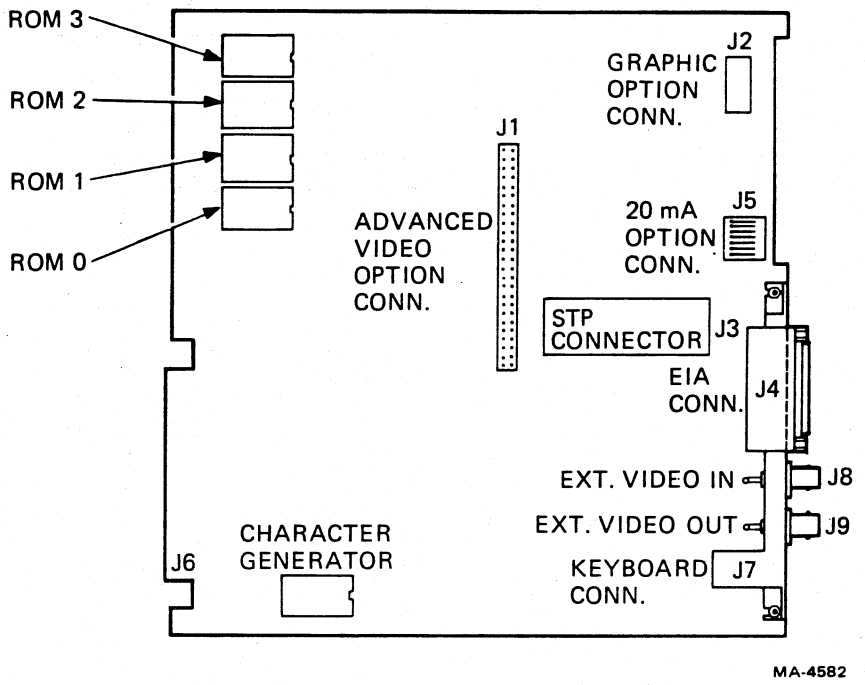


Figure 5-32 Terminal Controller Board

Table 5-8 Advanced Video Option (AVO) Jumpers

	Jumpers Installed													
Used In	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
VT100	–	–	–	–	–	–	–	–	–	–	–	–	–	–
VT100-WA-WB	X	–	–	–	–	–	X	–	–	–	–	–	–	–
VT100-WC-WK	–	–	–	–	–	X	–	–	–	–	–	–	–	–
VT100/VT1XX-AC	–	–	–	–	–	X	–	–	–	–	–	–	–	–
VT132 (ROMs 99–100) (with basic video ROMs 95–98)	–	–	–	–	–	X	–	–	–	–	–	–	–	–
VT132 ROMs 236–239 or PROMs 224–227 (with basic video ROMs 180–183)	–	–	–	–	–	X	–	X	–	–	X	–	–	X
VT125	–	–	–	–	–	–	–	–	–	–	–	–	–	–

Table 5-9 Advanced Video Option (AVO) Board ROMs

Board Used In	ROMs Used			
	ROM A	ROM B	ROM C	ROM D
VT100	–	–	–	–
VT100-WA-WB	23-069E2	–	–	–
VT100-WC-WK	23-152E2	–	–	–
VT100/VT1XX-AC	23-284E2 or 23-186E2	23-185E2 or 23-187E2	–	–
VT105	–	–	–	–
VT132	23-099E2 or 23-236E2 or 23-224E2	23-100E2 or 23-237E2 or 23-225E2	– 23-238E2 23-226E2	– 23-239E2 23-227E2
VT125	–	–	–	–

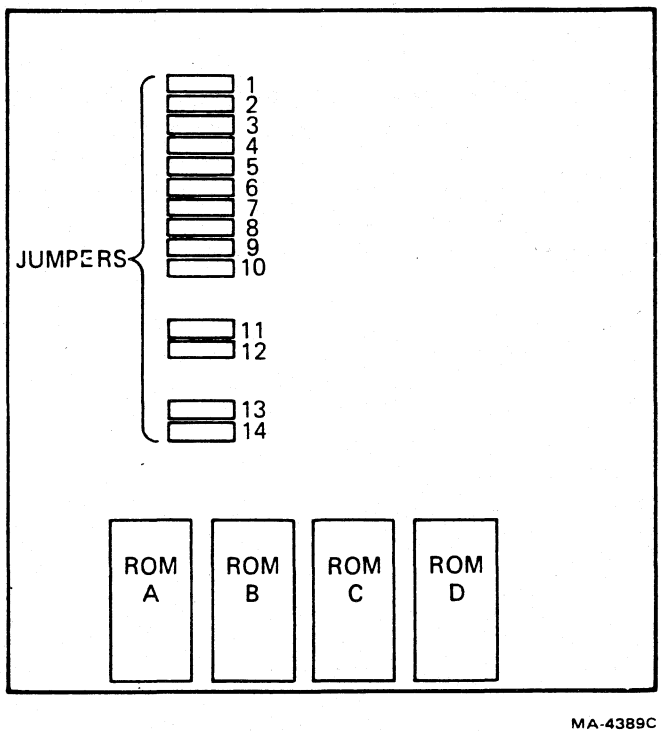


Figure 5-33 Advanced Video Option Board with Jumpers

Table 5-10 Advanced Video Option Switches

Board Used In	Switches Closed															
	S1								S2							
	8	7	6	5	4	3	2	1	8	7	6	5	4	3	2	1
VT100	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
VT100-WA-WB	X	–	–	–	–	–	X	–	–	–	–	–	–	–	–	–
VT100-WC-WK	–	–	–	–	–	X	–	–	–	–	–	–	–	–	–	–
VT100/VT1XX-AC	–	–	–	–	–	X	–	–	–	–	–	–	–	–	–	–
VT132 ROMs 99–100 (with basic video ROMs 95–98)	–	–	–	–	–	X	–	–	–	–	–	–	–	–	–	–
VT132 ROMs 236–239 or PROMs 224–227 (with basic video ROMs 180–183)	–	–	–	–	–	X	–	X	–	–	X	–	–	X	–	–
VT125	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–

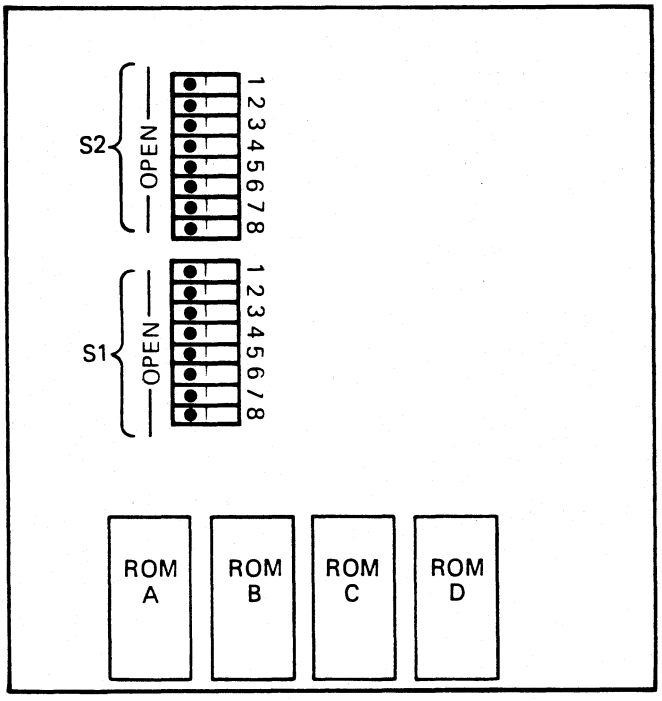


Figure 5-34 Advanced Video Option Board with Switches

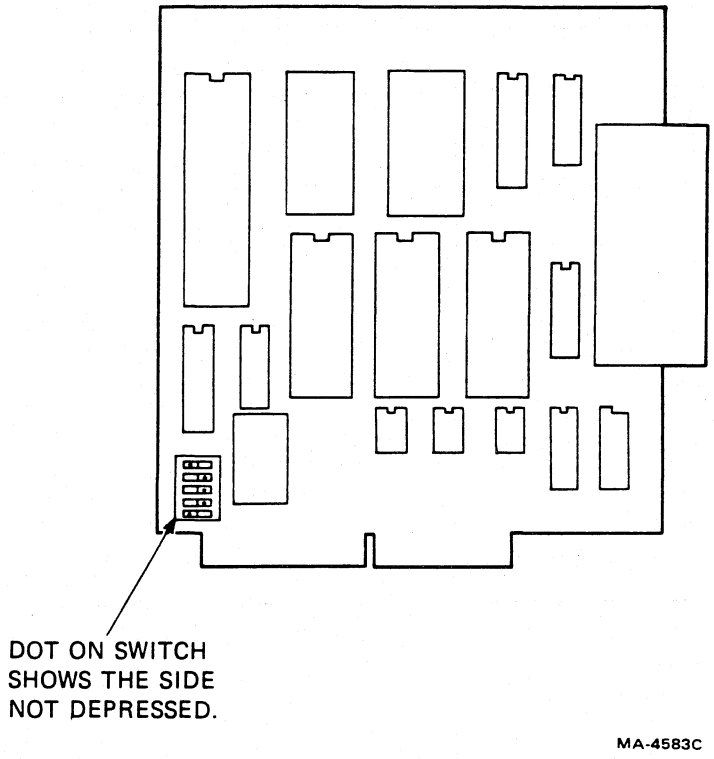


Figure 5-35 VT1XX-AC Printer Port Option Board

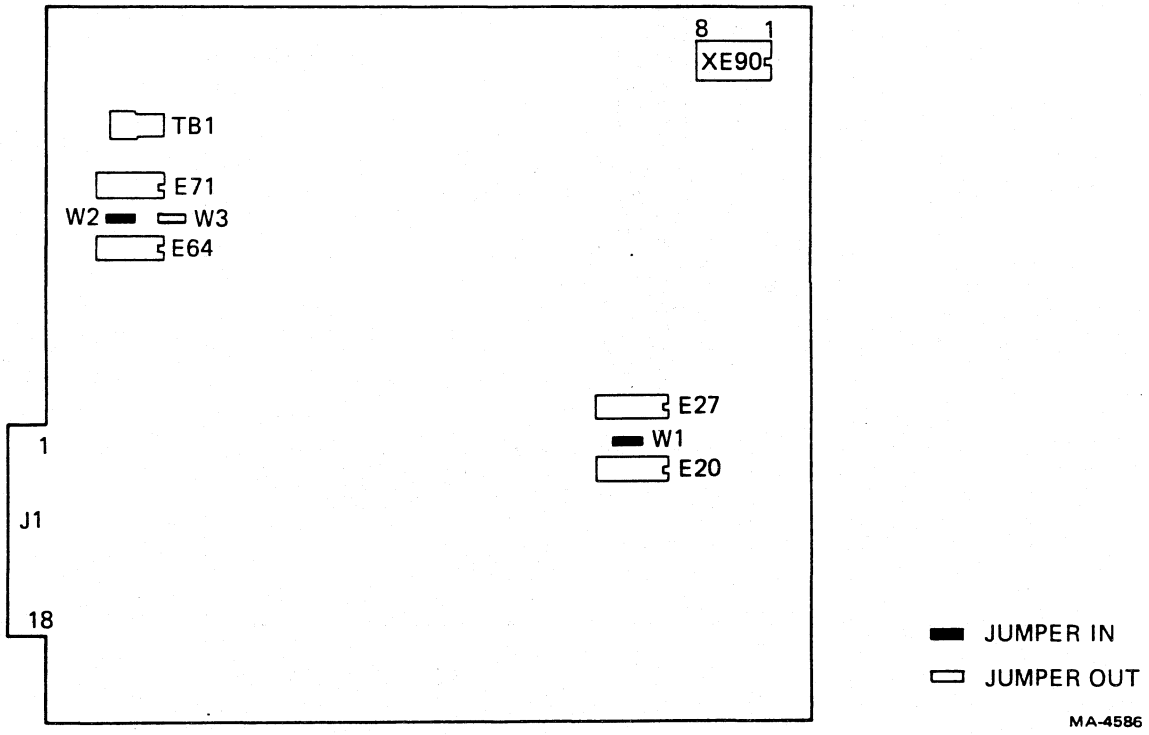


Figure 5-36 VT105 Waveform Generator Board

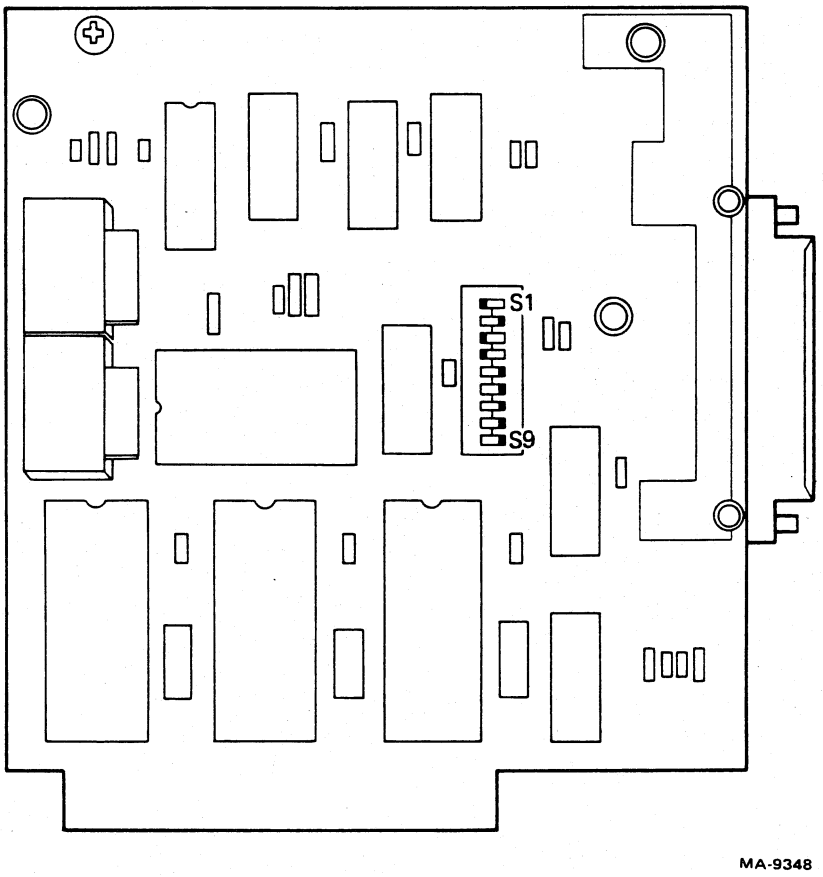


Figure 5-37 VT125 STP Board

5.6 COMPONENT LEVEL TROUBLESHOOTING

This section helps you to troubleshoot the terminal controller, microprocessor, power supply, and CRT monitor to the component level.

5.6.1 Troubleshooting the Terminal Controller

Refer to Paragraph 5.2 to isolate problems to a field replaceable unit (FRU) such as the terminal controller board. This section explains diagnosis of problems within the board.

Check the power supply for proper voltages and ripple. Make sure the voltage switch is not set to 230 volt on a 115 volt system. Check that all board edge contacts are clean and well seated.

The following four self-test results may appear on the screen or keyboard.

No valid LED code
LEDs indicating fatal error
Nonfatal errors with screen display
No indicated error

This section explains the major areas in the terminal to check for each of the self-test results.

5.6.1.1 Microprocessor – This section explains the four possible self-test results and how to troubleshoot them.

5.6.1.1.1 No Valid LED Code – If the LEDs show some random value not found in Table 5-1, several areas must be checked. ROM 1 containing the self-test routines may be at fault; the 8080 may be halted or in an inappropriate routine; there may be a hard failure on the data or address bus. (See Paragraph 5.6.1.2.)

With ROMs, first try to reseat them in their sockets to ensure good contact. Check the chip select lines to be sure the ROM is being selected.

Check the clock signals to the 8080 from the 8224 (E32-6, -10, -11). Check that the Ready and Reset signals are both high (E32-4 and -1). Check for the Sync signal (E32-5) every 3 to 5 clock periods. If there is no Sync, check Hold Request L (E35-13) which should go high for approximately 60 microseconds every 635 microseconds. Check for the Status Strobe (STSTB L) (E32-7). Hold Acknowledge (HLDA, E35-21) should toggle in step with Hold Request. If the clocks are present and Sync is entering E32 but Status Strobe does not appear, E32 is probably bad. If all these signals are okay, the problem is most likely not in the 8080 circuits.

If Hold Request is always high, the video processor is bad even though it may be able to drive the monitor. Grounding pin 1 of the Test MUX (E1) disconnects Hold Request, and while the self-test reports keyboard and NVR failures, the microprocessor is able to work. E1 also removes the master clock from the video processor, so the monitor should be disconnected (to protect it). Connect E1 pin 2 to 3, and E1—6 to 5 and 11 to run the microprocessor.

Check the data and address buses for toggling during the power-up test. Almost every address gets looked at during the test, and every data bit changes state, so that is the best time to check for stuck bus lines. Restart the test for each line by shorting C10 momentarily with a clip lead.

Connections made at E1 can serve to force either the microprocessor or the video processor off the buses. That is, asserting Hold Request L to the 8080 (with a clip lead from ground to pin 11) keeps the video processor off the buses, and asserting Hold Request H (with a clip lead from E1-16 to E1-6 or -10) keeps the microprocessor off the buses.

Check that the interrupt input is not stuck high (E35-14) if Interrupt Enable goes high. If the video processor works there should be a vertical frequency interrupt every 16.7 ms. If the processor is stuck in some kind of loop because some device is always calling it, the possibilities can be narrowed by looking at each of the devices' interrupts and flags.

5.6.1.1.2 LEDs Indicating Fatal Error – If the power-up self-test never manages to finish, the LEDs may display a number indicating the area of failure. Table 5-1 relates LED indications to areas of trouble. LED indications mean the error is a fatal one, which means the terminal cannot function at all. (If the self-test finishes, the LEDs are cleared.) Only the ROMs and the main RAM cause such a failure. The table indicates the ROM to check if a ROM number is displayed. Try reseating the ROMs in their sockets to ensure good contact. Check the chip select lines to be sure the ROM is being selected. There is no simple way to determine which of the six RAM chips is bad if a RAM failure is indicated. One-at-a-time replacement of all six chips is the only way to find and fix a bad RAM chip. But check the memory decoders' ability to address the RAMs before the RAMs themselves are blamed.

5.6.1.1.3 Nonfatal Errors with Screen Display – Nonfatal errors do not disable the terminal completely, although they may limit its usefulness. A keyboard failure, for example, still lets the terminal operate in receive-only mode. Nonfatal errors have codes assigned to them for display on the screen at the end of self-test. (See Table 5-2.) The data loopback and EIA tests are considered nonfatal because the microprocessor must work properly before the tests can run at all; but if they fail, the terminal cannot communicate. To troubleshoot nonfatal problems, see the following paragraphs.

5.6.1.1.4 No Indicated Error – Many video processor and monitor problems (see below) do not affect the microprocessor, so most self-tests cannot detect the problems. But if the screen fills with garbage or goes blank after the keyboard beeps with all LEDs on at the same time (indicating completion of self-test), the video processor or monitor may be at fault. (If the NVR fails its test, a number appears on the screen and the keyboard beeps several times. If garbage or nothing appears when the beeps occur, the problem is probably in the video processor rather than in the NVR circuit.) Because you know the microprocessor is good after completion of self-test, the screen RAM probably contains proper control data (terminators and line addresses). Therefore, you should be able to troubleshoot the video processor (garbage: Paragraph 5.6.1.2) or the monitor (blank: Paragraph 5.6.4) as the first step. Run the self-tests again after fixing the video processor; other nonfatal errors may appear then.

Areas not directly tested by self-test (because they have no effect on the microprocessor) are as follows.

NVR Write (tested by Saving)
Graphics port
Video processor (check with SET-UP screen test)
Monitor
Correctness of baud rates (only confirms match between send and receive)
Keyboard switches

Some video processor functions must work for the self-test to pass. For the microprocessor to work, these video processor signals must be close to frequency.

LBA 3 and 4
LBA 7 (NVR clock)

In addition, Hold Request cannot be stuck asserted and the NVR flag buffer must work.

5.6.1.2 Video Processor – There are two classes of video processor failure: 1) those that prevent proper movement of data from the screen RAM and through the character latches, terminator detection, line address counters, (DMA problems in general), and 2) all other problems. Those include the line buffer, character generator ROMs, video shift register, smooth scroll, attribute, and scan count control in the DC012, the analog video circuits, and monitor drive signals.

The areas in class 1 are difficult to troubleshoot because failures at any point in the loop from screen RAM data to screen RAM line addressing can cause the same kind of symptoms. The following section contains a suggested basic approach to the problem. The areas in class 2 have more straightforward troubleshooting, because the character data can be considered valid and failures with a particular symptom are probably caused by a single kind of problem. No further detail is provided here. In either case, make sure you understand the technical descriptions in Chapter 4 before spending any time trying to troubleshoot these circuits.

A dual-trace, triggered oscilloscope with delayed sweep is essential for servicing the video processor. Trigger the scope on Vertical Reset and examine each line for signals according to the DMA timing diagram (Figure 4-6-19) in Chapter 4. Check the continuous signals from the DC011. These include everything except Address Load, Address Count, and Write Line Buffer. All others should be checked against their timing diagrams for the respective screen modes. Any output affected by double width/double height may be in either possible state.

Now check signals in this order.

1. Vertical Reset

2. Address counter outputs E21, E22, E25, E30 (not the latches). All should be zero except E22-5 at Vertical Reset.

3. Hold Request starting after time specified in Figure 4-6-19.

4. DMA Enable

5. Address Count and Write Line Buffer

6. While triggered on Vertical Reset, delay sweep to the region shown in Figure 4-6-20. Watch for the data defined by Figure 4-7-5, Fill Line Operation at positions within the character latches as shown in the chart in Figure 4-6-20.

7. Check for Terminate L during the time that Horizontal Blank is going low.

8. On the following character clock, Hold Request should go low causing Address Load to go low and Address Count to stay high.

9. Check the address in address counter outputs (E21, E22, E25, E30) according to Figures 4-7-2 and 4-7-5.

10. Check for unasserted line attributes at E6-23 and E5-1, -26, -27.

11. Adjust sweep delay to observe the second DMA period.

12. Check the length of Hold Request. If twice as long as normal, this means that double width mode has been invoked by some incorrect signal at Address Load time. Because the screen RAM does not contain properly formatted data for double width, the video processor cannot display a normal screen.

Any other failures of address loading cause the second DMA to read from the wrong area of the screen RAM.

Later DMAs may fail when early ones are okay if, for example, a high bit on the address counter is stuck low. Then only higher address lines (lines later in the screen) are affected. This assumes that no scrolling has been attempted since power-up, because that would eliminate the correspondence between screen position and address order.

5.6.1.3 Communications – Most aspects of the communications channel operation are under program control, so the microprocessor must be fully functional (power-up self-test passed) for the interface to work at all. The communications channel is tested with the data loopback connector (either EIA or 20 mA) installed. Then you can start self-tests to check the channel operation. If there is a failure, leave the loopback connector installed. Typing on the keyboard in on-line mode provides data movement to the transmitter (and receiver if the transmitter works).

Check the STP connector contacts. All interface signals pass through these normally shorted contacts. Check the baud rate clocks. The baud rate generator (E60) or its two-phase input drivers (E38) may be bad. Check that the transmit and receive frequencies are as selected (16 times baud rate). E60 may accept changes on one side but not the other. At the PUSART, check the EIA line driver and receiver chips (E39 and E44) and check for pulses on the address (E43-11, -12) and I/O control lines (E43-10, -13) and on the interrupt flag lines (E43-14, -15).

Modem control problems are probably either the STP contacts or the EIA driver or receiver chips. Check the enable line to the modem flag buffer (E-41). (Also check the modem control signal at the NVR latch E-61.)

5.6.1.4 Nonvolatile RAM – The NVR is the only device that uses −23 volts (E24-2). The video processor must be providing LBA 7 as a clock with 12 volt swing at E24-6. Q1 must present a very high impedance when it is off or read data will be lost. Check the NVR latch E-61 and the flag buffer E-42.

5.6.2 Troubleshooting the Keyboard

During the self-test, check to see that the LEDs flash and that the bell sounds. Failure of these does not cause the keyboard to fail but this is the best time to make sure that they work.

If the keyboard fails self-test, the terminal automatically becomes a receive-only terminal. The number 4 is then visible on the screen under the blinking cursor. Keyboard failure means the microprocessor attempted to start a scan but did not get any results back. (The always-down "last key" should always be returned.) The problem could be at either end of the keyboard interface but is more likely at the cable or connectors, or in the keyboard circuitry (because of its greater exposure to the environment). Either the on-line or local LED should be on if the keyboard has 12 volt power and the 5 volt regulator works. If power is good, check the interface line for the presence of signals from the terminal. Refer to Paragraph 4.4 in Chapter 4 for an illustration of normal signal appearance.

On the interface, if the clock from the terminal is on the interface line, it should also be at E9-8. Serial data input (1 bit for every 16 clocks) should be at the output of the integrator E2-1. Serial data output should be at E9-12 (TTL level) and E8-8 (12 volt swing).

A clock signal always comes from the terminal, and command bytes come continuously, starting every 1.28 milliseconds. Every 50th or 60th of a second, one command byte includes a bit that triggers the START SCAN L signal (E5-11) which should start the address counters. KEY DOWN L (E6-12) should appear once each scan to represent the last address (for simplicity, make sure that no keys, including CAPS LOCK are down) and should drive the DATA STROBE L input to the UART (E12-23). TBMT H (Transmit Buffer Empty) (E12-22) should go low when DATA STROBE is asserted. TBMT H goes low for only a few clock periods when only one key address is being sent. More keys held down causes TBMT H to stay low for more time for each additional key. When TBMT H is low, the clock cannot pass through E4 to drive the counter clock input (E7-14); it can at all other times. At the end of a scan, E3-1 goes high and holds the counter CLEAR inputs. The START SCAN L signal (E5-11) resets E3 to allow the count to continue.

If no signals are coming from the terminal (and this assumes that the phone jack on the board is good) check for clock signals LBA3 and LBA4. These come from the video processor, so if the display works they should be present. If they are, check E18-1 and E18-2 (TTL and 12 volt respectively). Also, if the terminal works otherwise, the microprocessor should be regularly loading the keyboard status byte into the UART for transmission. Check for Keyboard Write (KBD WR L) at E55-23 approximately every 1 ms in response to KEYBOARD TBMT (E55-22) which should go high every 1.28 ms. Make sure that serial data comes out from pin 25.

If data is coming from the keyboard but is not getting read by the microprocessor, check that data reaches the serial input pin 20, and that each received word sets KEYBOARD DATA AVAILABLE H. Check that the KEYBOARD DATA AVAILABLE H interrupt signal reaches the Interrupt Vector Latch E41-2 and the microprocessor through E23-8. Finally, in response to the interrupt, the microprocessor should strobe KBD RD L at E55-4 and -18. KBD DATA AVAILABLE should go low.

5.6.3 Troubleshooting the Power Supply

The power supply has two basically different sections: one is low power control circuitry and the other is highly stressed power components. The current limiting circuits are supposed to protect the supply well enough to prevent fuse blowing in spite of short circuits, so if the fuse blows repeatedly there is probably a major problem.

The power switching transistor Q7 and its companion D19 are the usual failure, because they are subjected to the most stress in the circuit. When they fail, other components may also fail. Check D41, R22, the input rectifier diodes, and the two thermistors. Heavy currents could cause the thermistors to crack. Sources of stress include connecting the supply to 230 volts when set to 115 volts, and shorting of any transformer secondary. If the fuse blows but Q7 is okay, check C9, C14, the input rectifiers (the two connected to the thermistors are the ones used in 115 volt operation), R19, and R20.

If Q7 repeatedly blows, the control circuit may be driving it incorrectly. Lift one side of R22 to shut off the power circuit and examine the control circuit. (The absence of voltage at the output causes the control circuits to produce maximum pulse widths, and the 12 volt startup supply's regulator Z2 gets hot from having to provide continuous output. But it is safe.) Look for a strong pulse on Q2's collector, a ramp on Q5's collector, a squarewave on Q1's collector, a negative going pulse on pin 2 of E3 and a 12–13 microseconds squarewave on pin 3. (Refer to Figure 4-9-3, Power Supply Timing Diagram, in Chapter 4.)

The -12 and -23 volt supplies are individually current-limited; the -12 by its three terminal regulator's self-protection, and the -23 by a 10 watt resistor in series. The $+5$ and $+12$ volt supplies shut down the entire supply if either supply's current limiter is triggered. Check for shorts by checking the voltages across R37, R44, and R45. If there are no shorts and the supply does not turn on, and startup voltage (10.8 volts at the banded end of D25) is present, lift one side of D10. This diode carries the SHUTDOWN L signal from the current limiters to pin 9 of the 3524 control chip. This isolates the problem to the comparators (E1). Check the comparators by measuring their inputs: for the $+12$ circuit, measure the input with respect to the inboard side of series resistor R37; for the $+5$ circuit, measure with respect to the inboard side of R44 and R45. Pin 5 should be positive with respect to pin 6, and pin 3 should be positive with respect to pin 2.

The slow turn-on circuit might also keep the supply off. Lift D39 to disconnect it and use an autotransformer to bring the supply up gradually.

If there are oscillations or instability in the $+5$ volt control loop, check C31 and L2, C17, R31, and R30. If there are oscillations in the $+12$ volt control loop, check C26, L1, R4, C1, R5. Excess sensitivity in the current limit circuits can also cause apparent output instability. There is some interaction in the operation of the supply because the $+5$ volt supply must deliver at least its minimumm current for the $+12$ volt supply to be able to meet its regulation specification. Therefore the supply should not be operated without some load.

5.6.4 Troubleshooting the CRT Monitor

Most monitor problems are due to blown horizontal output transistors and diodes. These components are the most stressed in the circuit. Listen to the monitor when checking it: the only normal sound is a slight 15 kHz whistle.

Other problems include a dark screen (with normal sounds), a horizontal line on the screen, and sync problems (rolling or tearing horizontally or vertically). If the screen is dark, turn up the brightness control on the monitor board, press **SET-UP**, and bring the intensity to maximum with the cursor up key. If there is a faint display or no display, check the horizontal drive operation, check the CRT voltages and filament, and check the video output from the terminal controller. The high voltage is probably okay if the horizontal frequency sound from the flyback is normal. The voltages to check then are the control, focus, and screen grid biases.

A horizontal line on the screen indicates a failure in the vertical oscillator.

For rolling or tearing, check the horizontal and vertical drive signals coming from the terminal controller and be sure that these signals reach the monitor board. (On the Ball monitor board the vertical hold control should be properly adjusted to ensure good lockup to the drive signal.)

5.6.5 Troubleshooting the Options

See Chapter 6.

CHAPTER 6
OPTIONS

6.1 SET-UP PROCEDURES

This section chapter summarizes the SET-UP information for the following terminals.

VT100 – all variations, including VT1XX-AC
VT105
VT125 – including VT1XX-CB, -CL
VT132

This section does not provide detailed information on any SET-UP features, or explain how to change any of the features. For detailed information, see the user guide shipped with the terminal.

6.1.1 SET-UP A

Figure 6-1 shows a typical SET-UP A display. The same display appears in all VT100 series terminals.

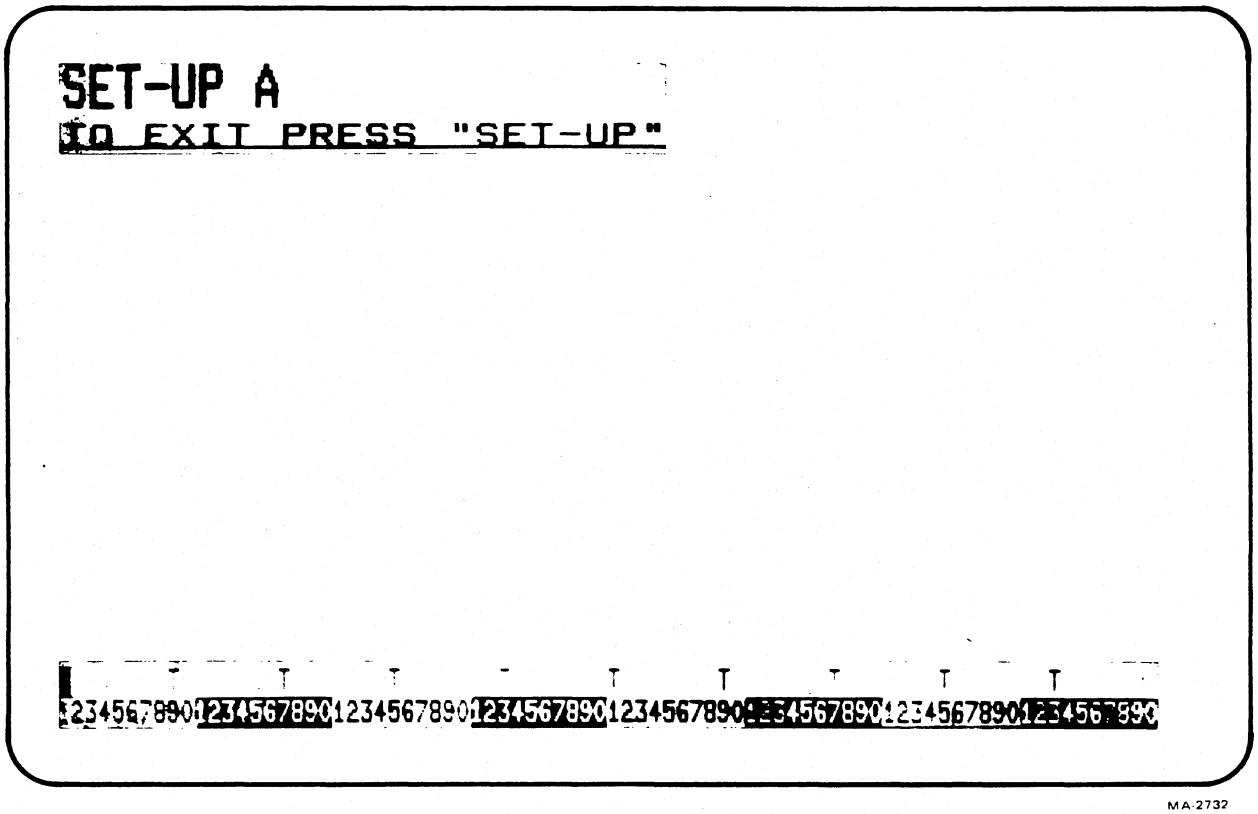


Figure 6-1 SET-UP A with Advanced Video Option (AVO)

6.1.2 SET-UP B

Figure 6-2 shows the SET-UP B display for the basic VT100 terminal, and Figure 6-3 the SET-UP B display for the VT100 terminal with VT1XX-AC printer port. Note the fifth switch group in Figure 6-3. This group appears if an option is installed in the STP connector on the terminal controller board.

Figure 6-4 shows the SET-UP B summary for the VT100-AA, -AB, -WA, and -WB terminals. Figure 6-5 shows the SET-UP B summary for the VT100-WC and -WK word processing terminals, the VT132, and the VT100 with VT1XX-AC printer port. Figure 6-6 shows the SET-UP B summary for the VT105. Figure 6-7 shows the SET-UP B summary for the VT125.

6.1.3 SET-UP C

Figures 6-8, 6-9, and 6-10 show the three different types of SET-UP C displays. Only some word processing VT100s (VT100-WC through VT100-WK), the VT100s with printer port (VT1XX-AC), and the VT132s contain a SET-UP C. Figures 6-11 and 6-12 show the VT1XX-AC and VT132 SET-UP C features, and the possible settings.

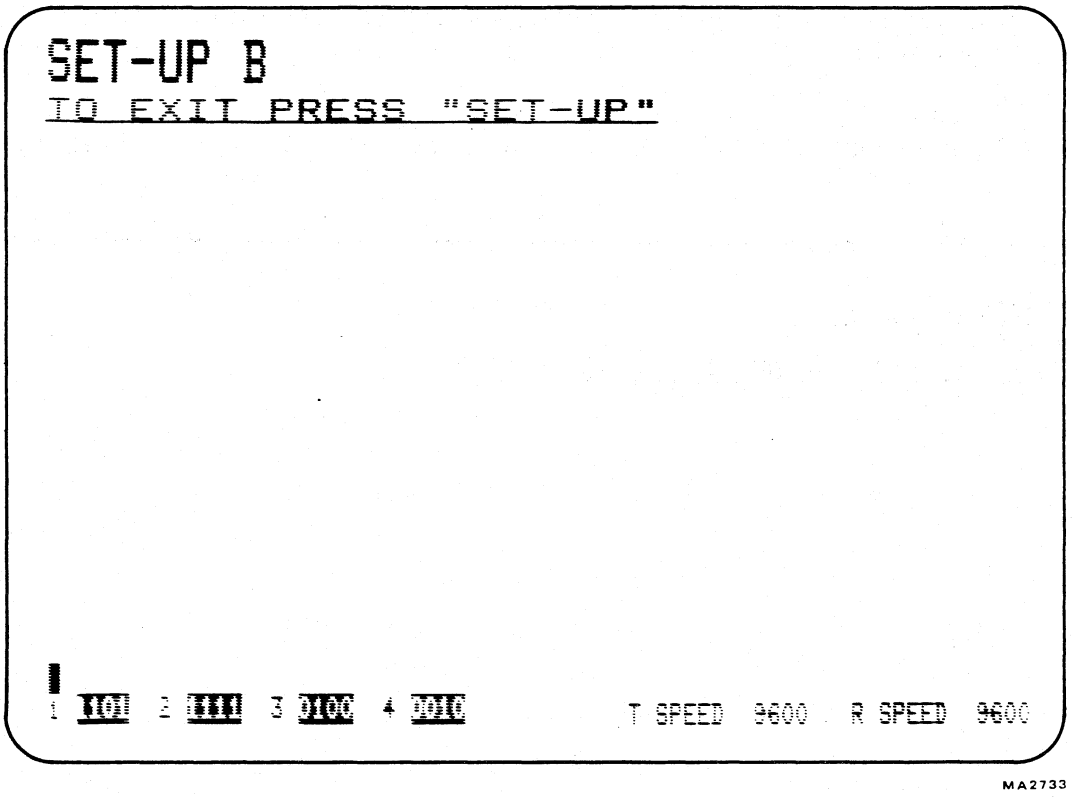


Figure 6-2 VT100 SET-UP A

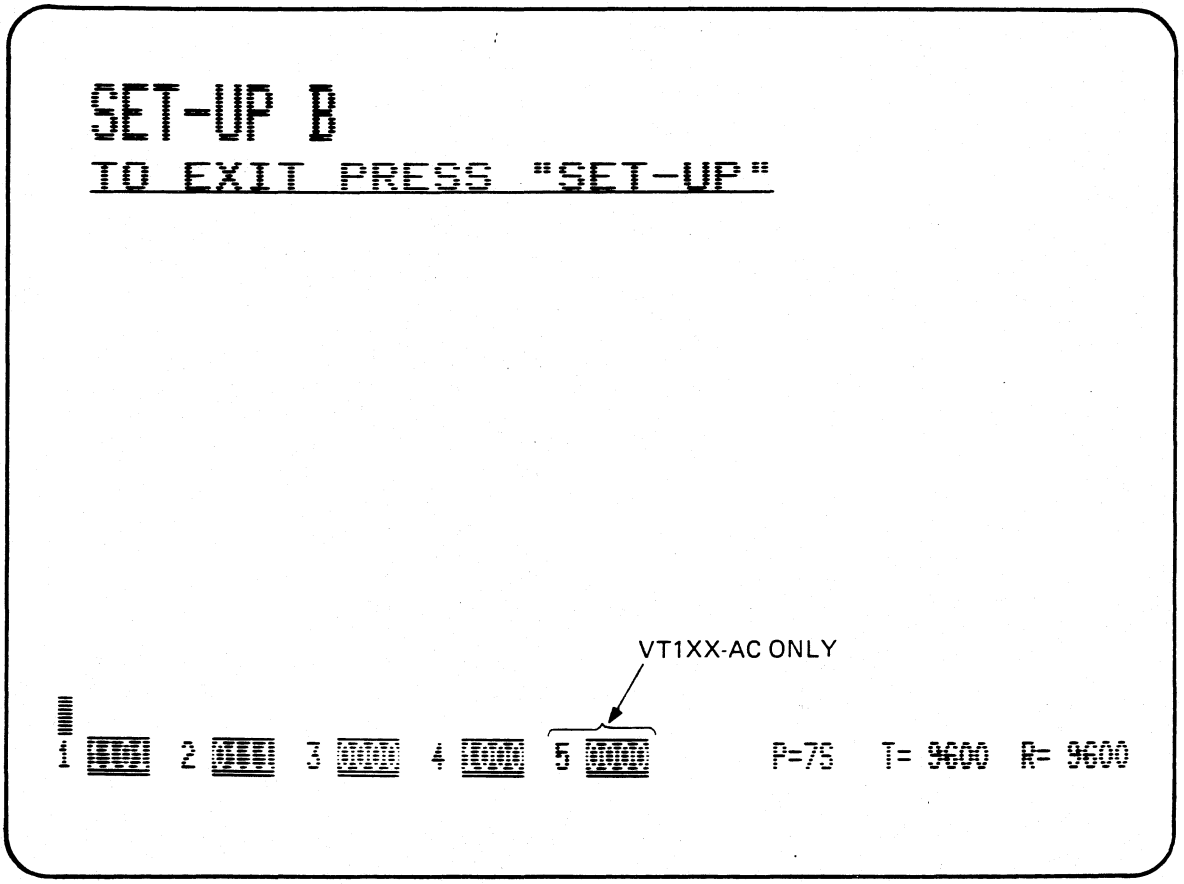


Figure 6-3 VT100-WC, -WK, VT132, VT1XX-AC SET-UP B

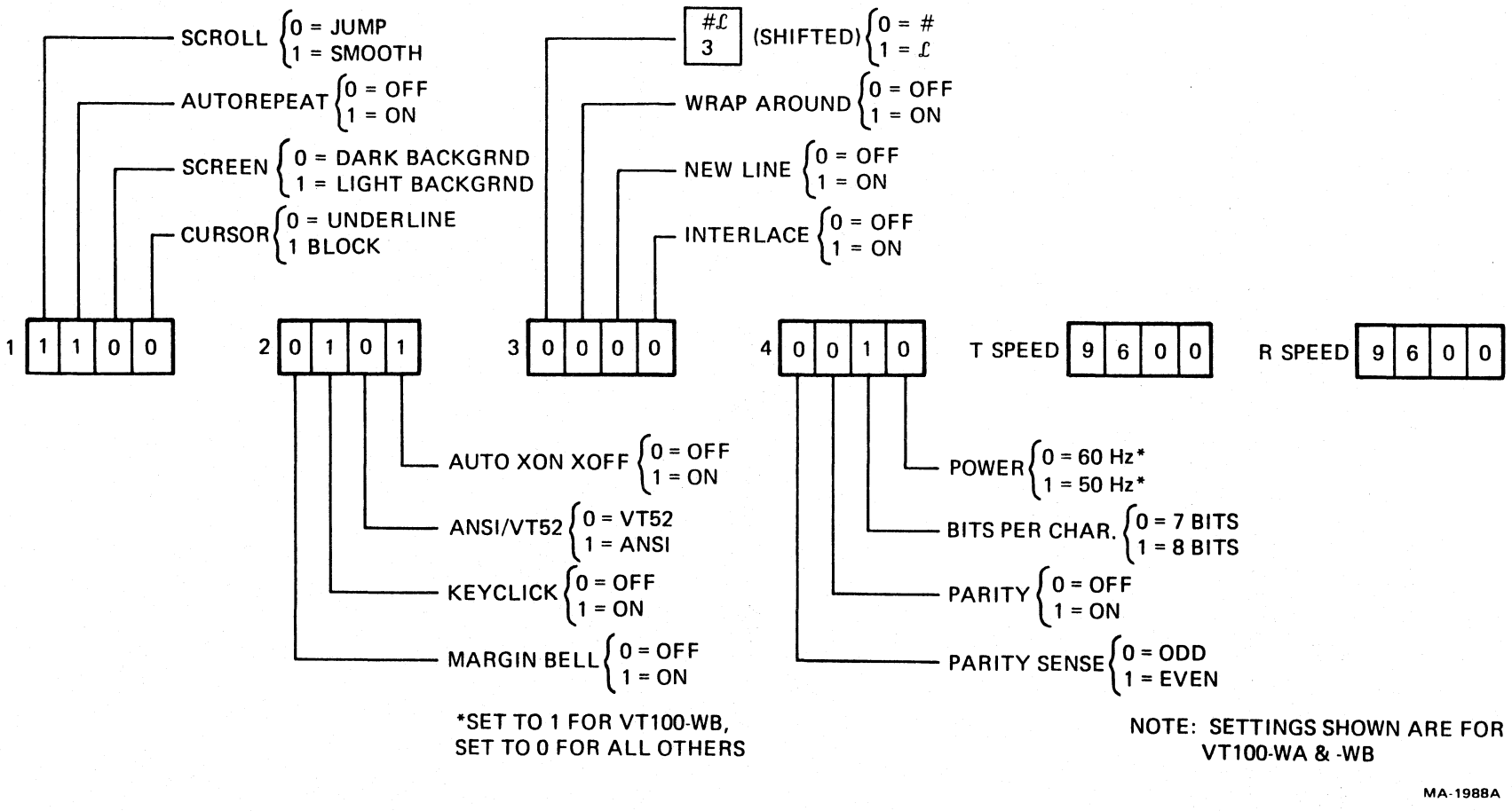


Figure 6-4 VT100-AA, -AB, -WA, -WB SET-UP B Summary

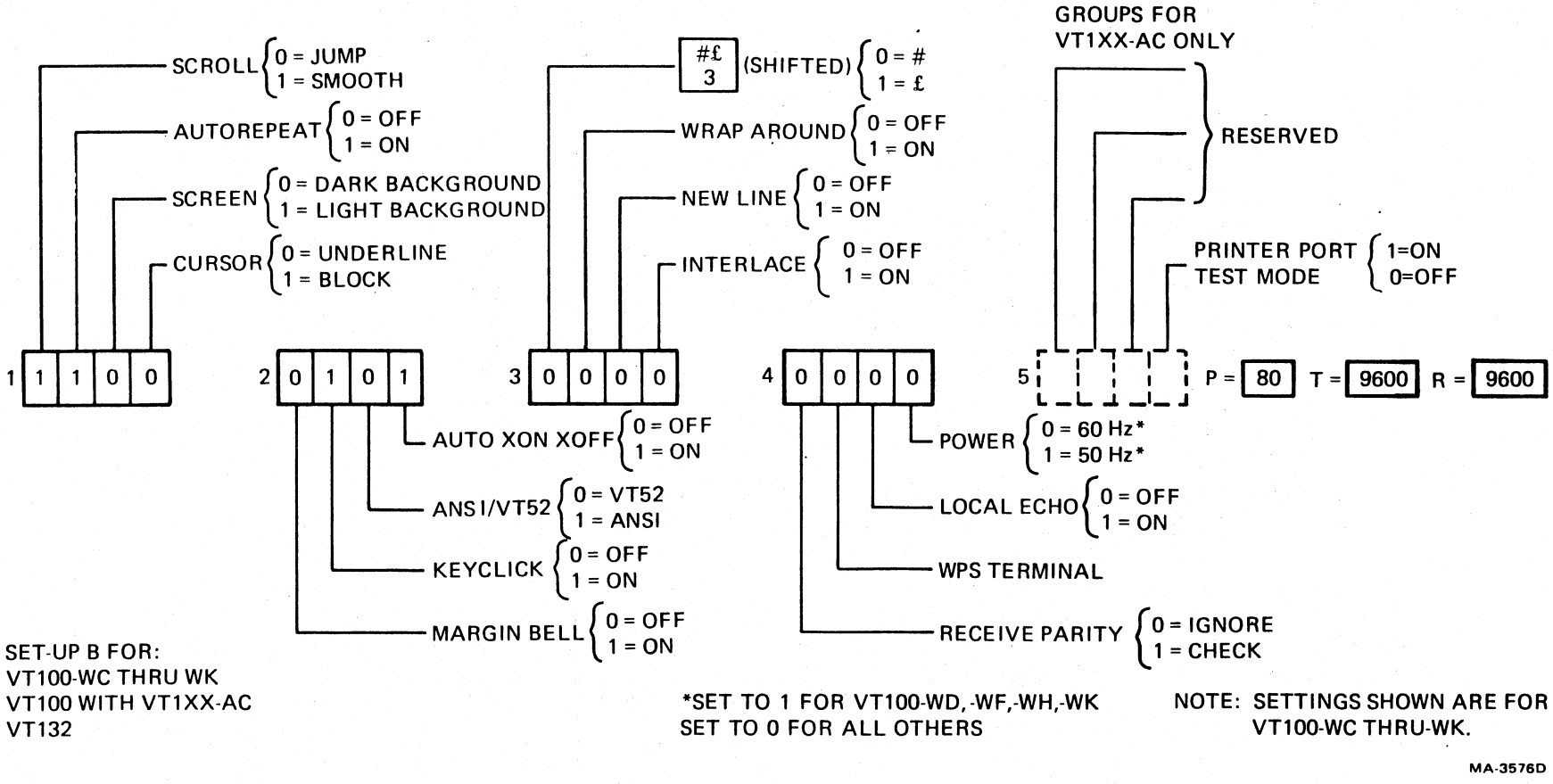


Figure 6-5 VT100-WC, -WK, VT132, VT1XX-AC SET-UP B Summary

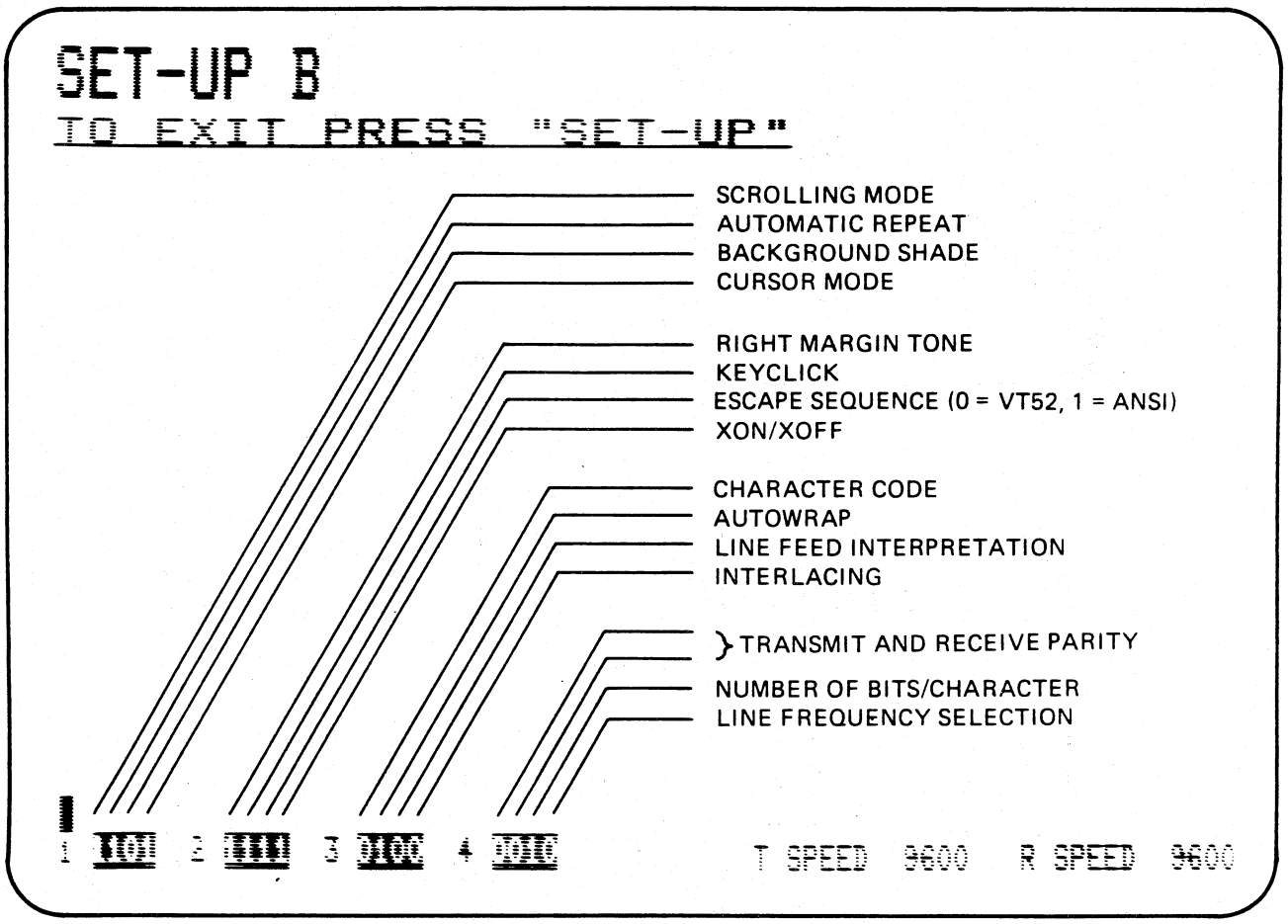


Figure 6-6 VT105 SET-UP B Summary

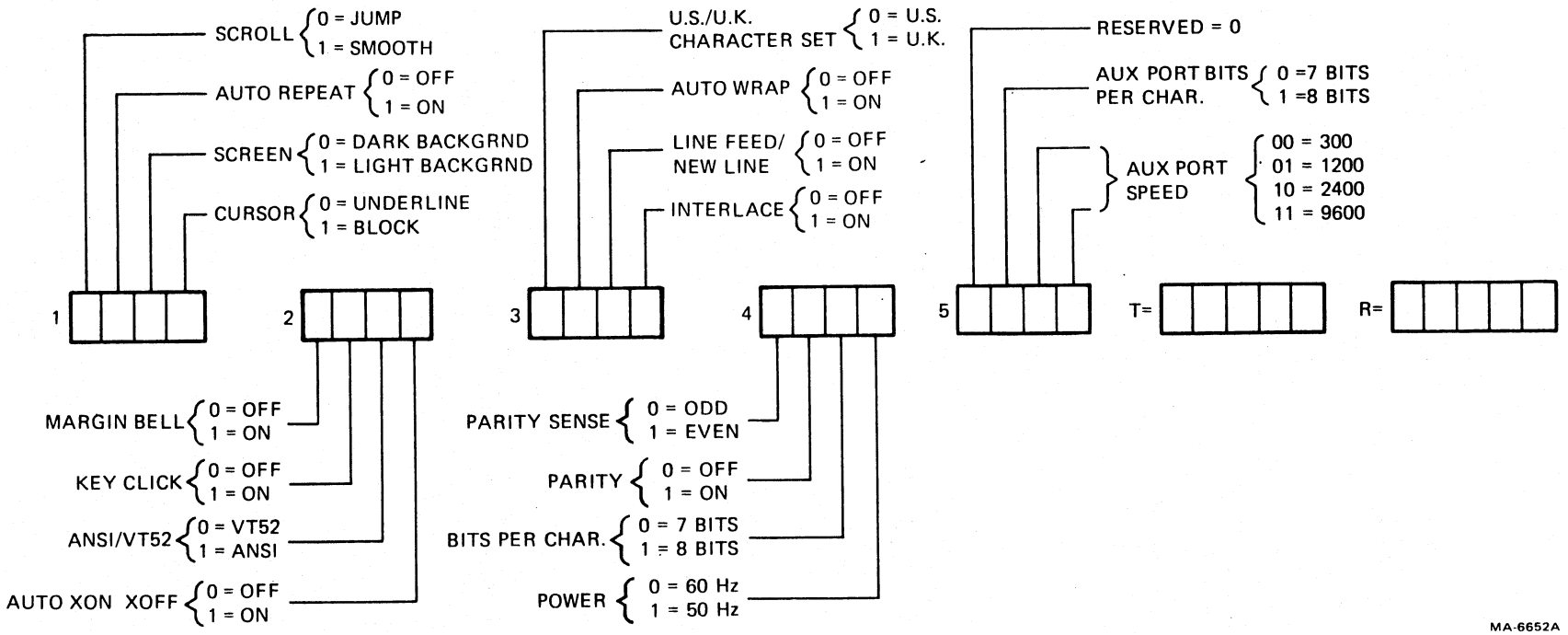


Figure 6-7 VT125 SET-UP B Summary

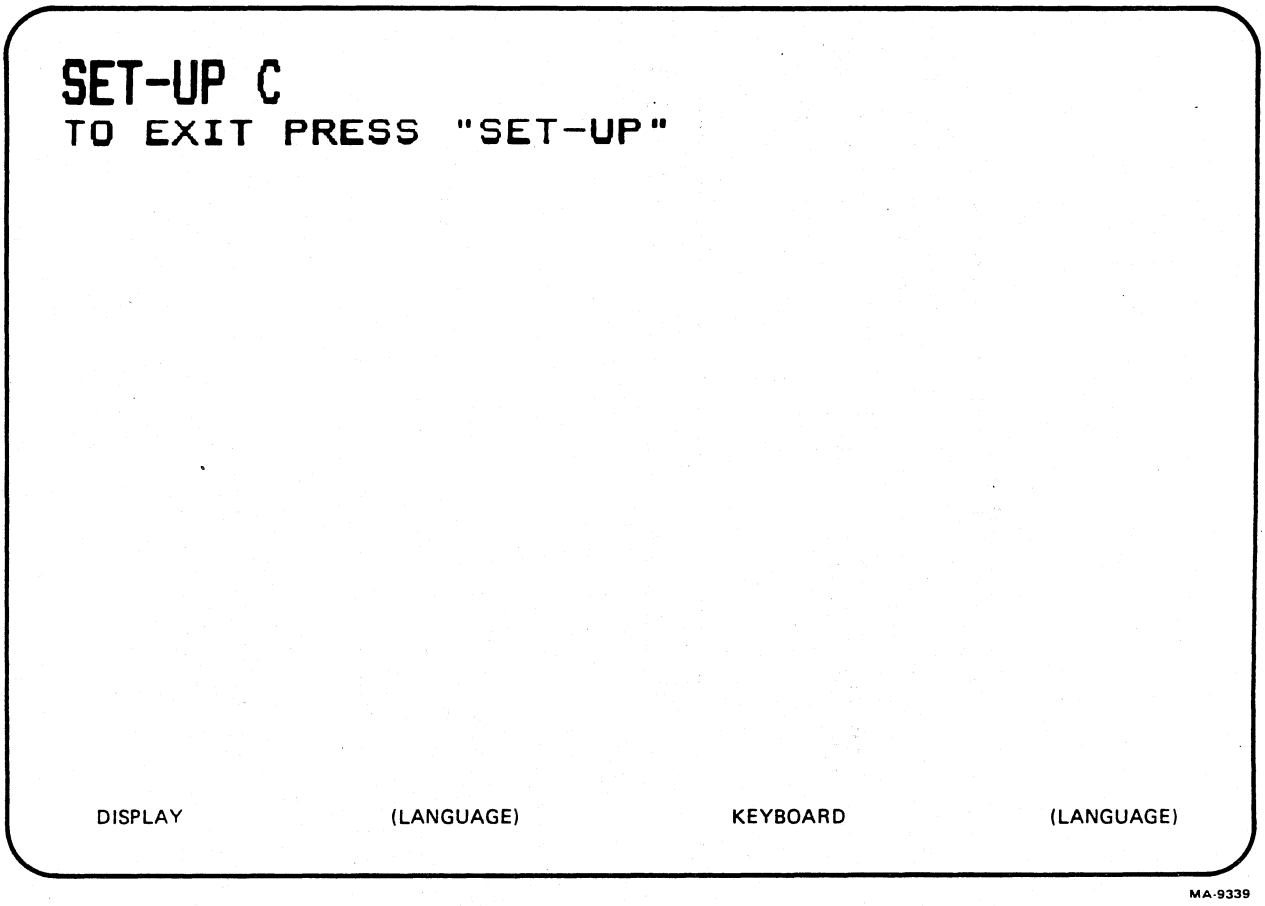


Figure 6-8 VT100-WC, -WK SET-UP C

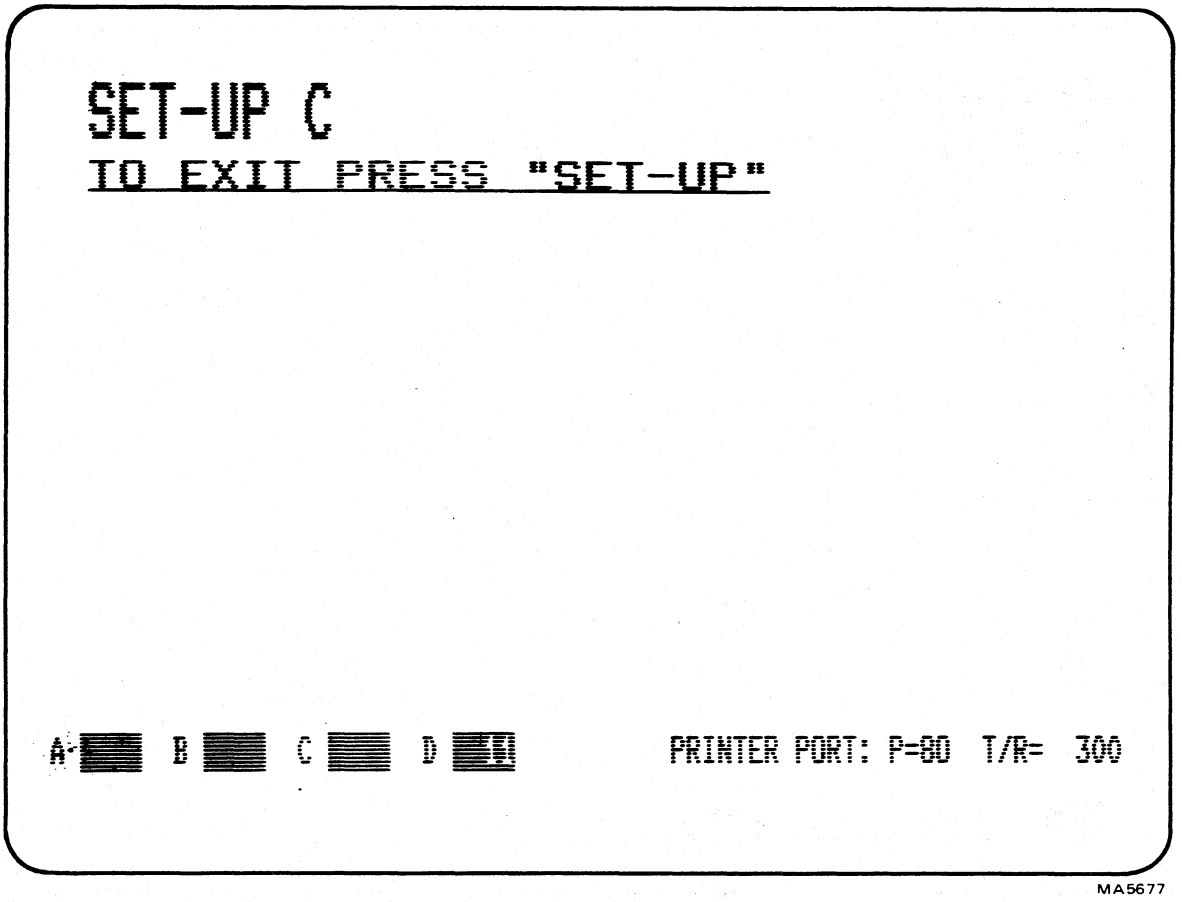


Figure 6-9 VT1XX-AC SET-UP C

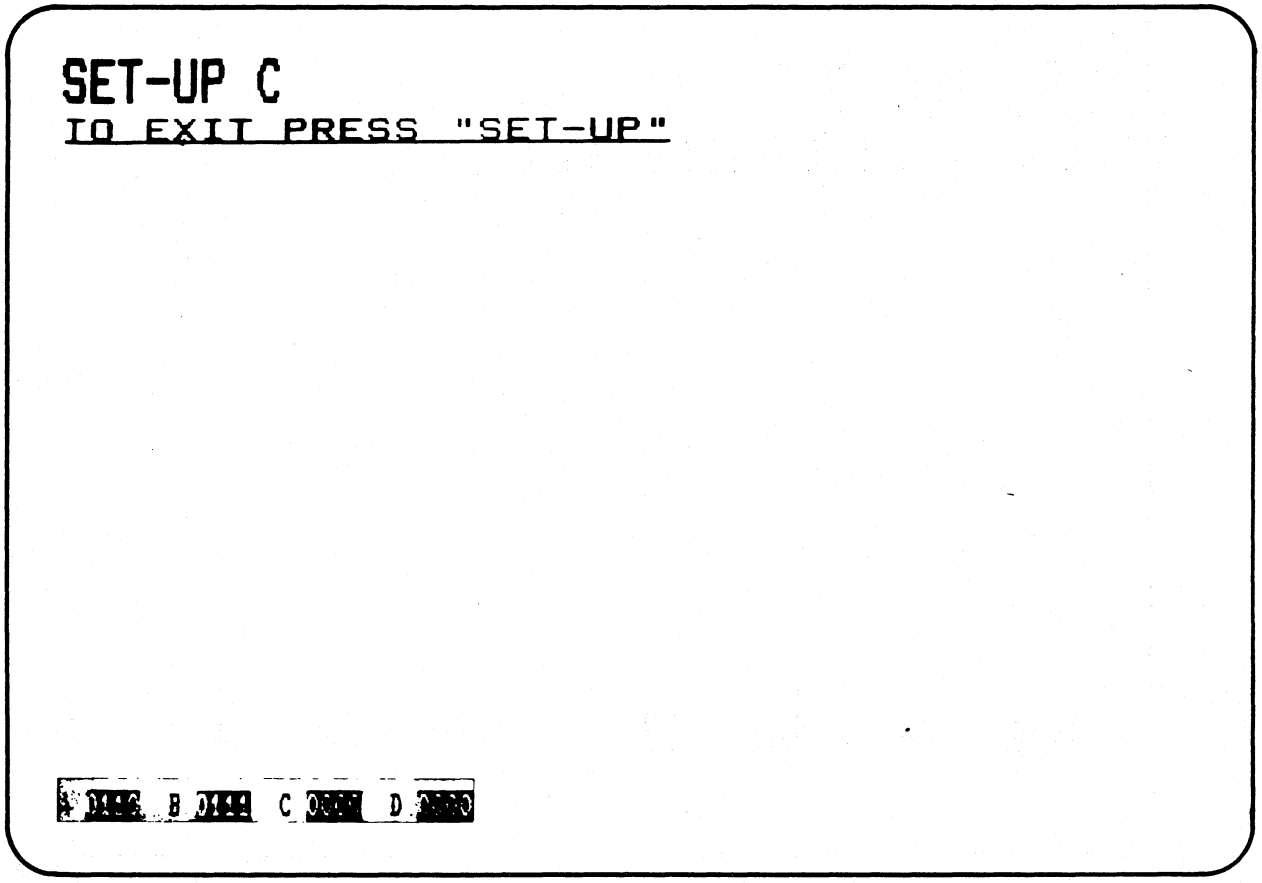


Figure 6-10 VT132 SET-UP C

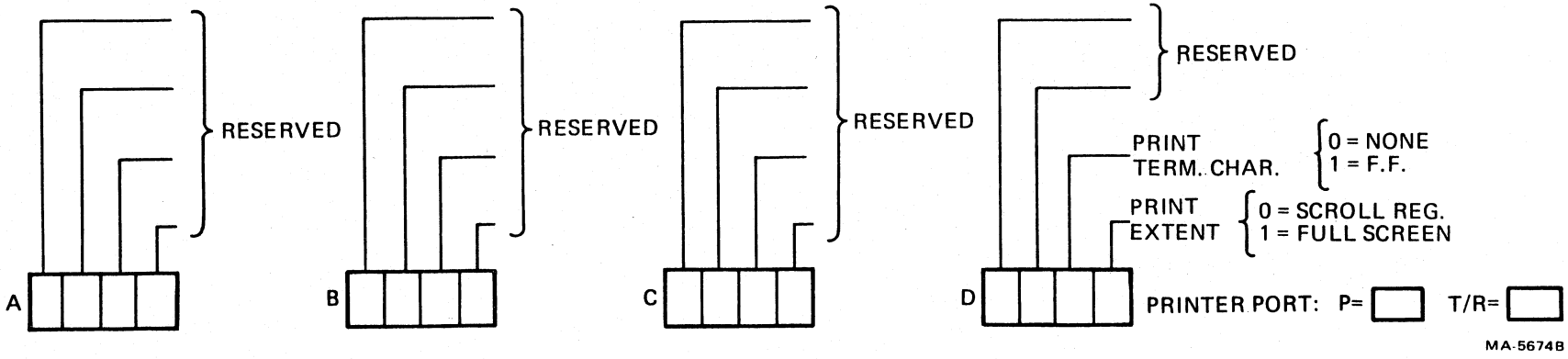


Figure 6-11 VT1XX-AC SET-UP C Summary

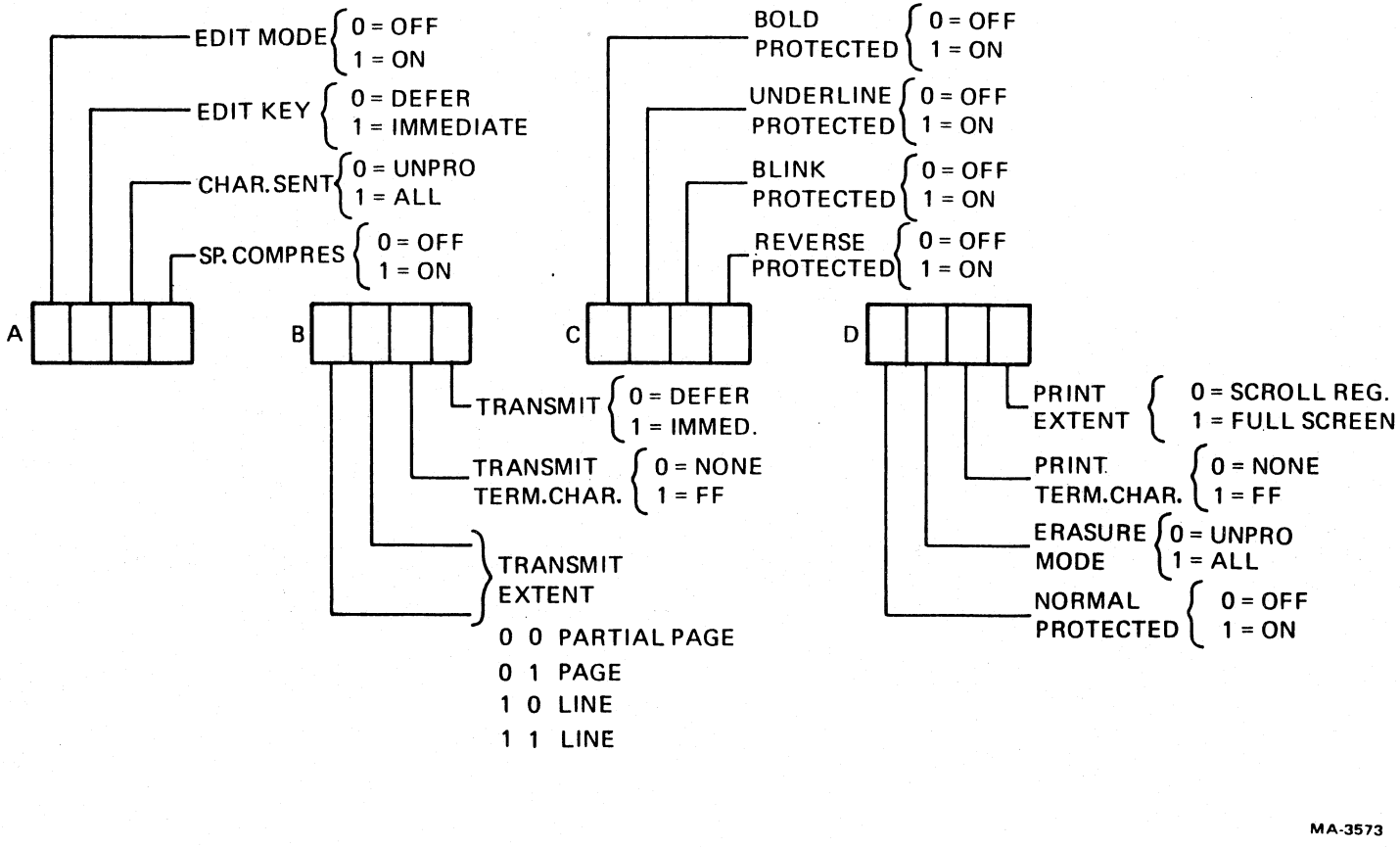


Figure 6-12 VT132 SET-UP C Summary

6.2 ADVANCED VIDEO OPTION

The advanced video option (AVO) provides the extra memory required for the VT100 to display 24 132-character lines, an extra 4 bits of memory per character for character attributes, plus space for extra program ROM. Additional hardware in the AVO are the address decoders for memory expansion, and the 4-bit wide set of character-clocked latches for the attribute data. Refer to the video processor functional diagram (Figure 4-6-3) to see how the AVO functions with the basic video circuitry.

6.2.1 Advanced Video Option Installation

Use the following procedure to install the advanced video option.

1. Remove the terminal access cover.
2. Remove the terminal controller board.
3. Place the terminal controller board on a flat surface with the component side up.
4. Locate the four mounting holes drilled in the terminal controller board; mount a standoff in each. (Figure 6-13).
5. Grasp the advanced video board by the edges and carefully align the connector pins with the connector on the terminal controller board. Gently but firmly mount the advanced video board onto the terminal controller board.
6. Reinstall the terminal controller board. You must install the terminal controller board in the leftmost slot in the card cage.
7. Reinstall all cables removed.
8. Reinstall the access cover.

6.2.2 Advanced Video Option Checkout

Use the following procedure to check out the operation of the advanced video option.

1. Turn the terminal power on and verify that no error was detected during the power-up self-test.
2. Press the **SET-UP** key. The words "SET-UP A" should blink in boldface, the words "TO EXIT PRESS SET-UP" should be underlined, and the ruler should contain alternating normal and reverse video fields.
3. Place the terminal in 132-column mode and then in LOCAL mode.
4. Exit SET-UP and type the following sequence.

   <ESC> < <ESC>#8

   The screen should now display 24 lines × 132 columns.

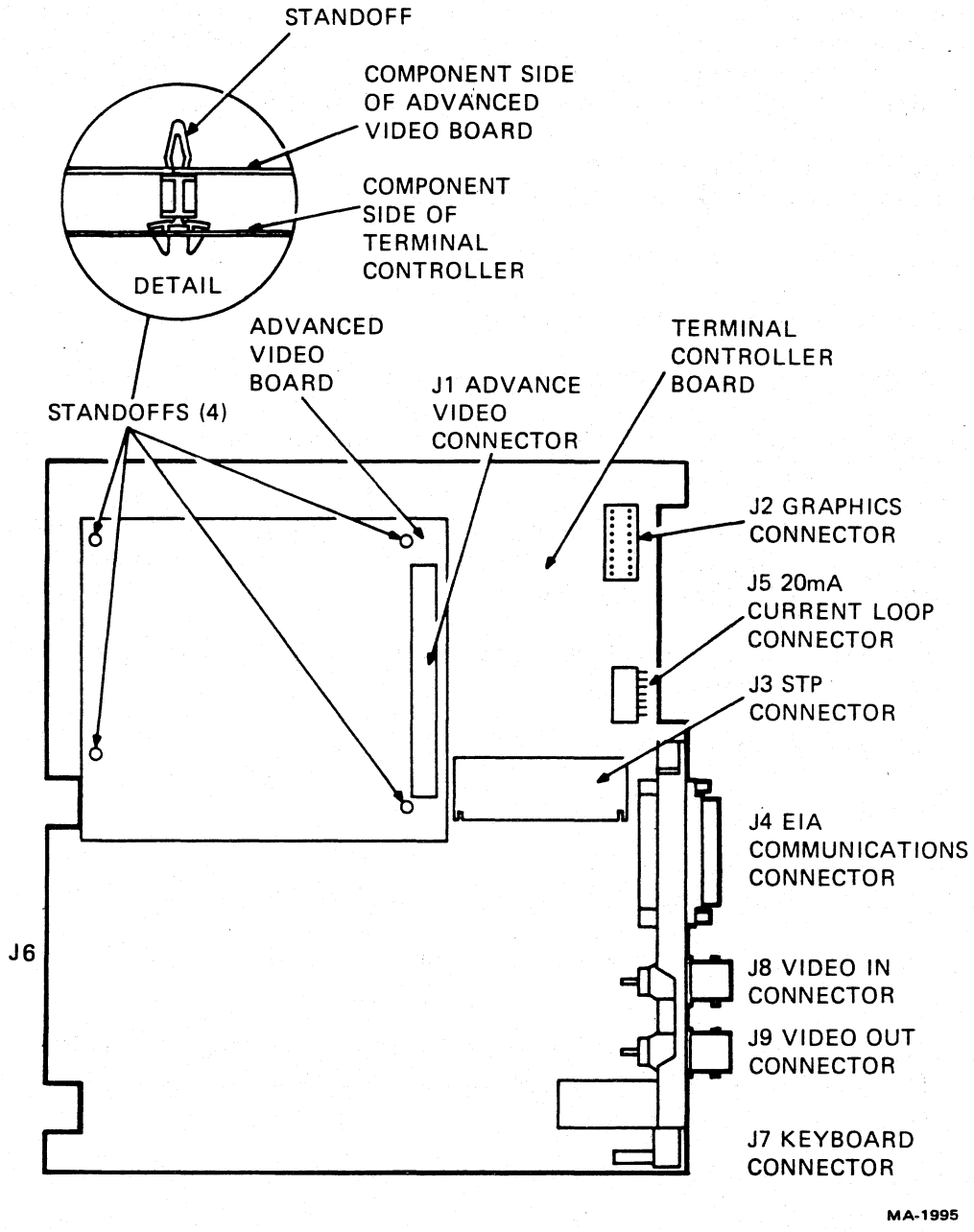


Figure 6-13 Advanced Video Option Installation

6.2.3 Program Memory Expansion

Basic program memory resides on the basic video board and may be patched in any or all of its 2K segments, or it may be overlayed by one 8K × 8 ROM on the advanced video board as follows.

Patch Address (Hex)	ROM Type	Jumpers Used	Patch PROM Loc	IC Type*
0000-07FF	ROM A	W1	E19	Intel 2716 or 2316E
0800-0FFF	ROM B	W2	E17	Intel 2716 or 2316E
1000-17FF	ROM C	W3	E13	Intel 2716 or 2316E
1800-1FFF†	ROM D	W4,W8, W11,W14	E8	Intel 2716 or 2316E

Overlay Address (Hex)	ROM Type	Jumpers Used	ROM Loc	IC Type*
0000-1FFF	ROMS A, B,C,D	W1,W2,W3 W4,W5,W10, W12,W13	E8	Signetics 2664

You can expand program memory by up to 14K bytes, using one 8K × 8 ROM and up to three 2K × 8 EPROMs, if no 2K × 8 patches were implemented. ROMs may both patch and expand; however,each socket may either patch the address range given above or expand in the range given below, but not both.

Expansion Address (Hex)	ROM Type	Jumpers Used	Expansion Program Memory Loc	IC Type*
8000-87FF	2K × 8	–	E19	Intel 2716 or 2316E
8800-8FFF	2K × 8	–	E17	Intel 2716 or 2316E
9000-97FF	2K × 8	–	E13	Intel 2716 or 2316E
98FF-9FFF†	2K × 8	W8,11,14	E8	Intel 2716 or 2316E
A000-BFFF‡	8K × 8	W6,10,12,13	E8	Signetics 2664

Or for addressing convenience use the following range.

Expansion Address (Hex)	ROM Type	Jumpers Used	Expansion Program Memory Loc	IC Type*
8000-9FFF‡	8K × 8	W7,10,12,13	E8	Signetics 2664
A000-A7FF	2K × 8	–	E19	Intel 2716 or 2316E
A8000-AFFF	2K × 8	–	E17	Intel 2716 or 2316E
B000-B7FF	2K × 8	–	E13	Intel 2716 or 2316E
B800-BFFF†	2K × 8	–	E8	Intel 2716 or 2316E

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* May be used only if 8K overlay or 8K expansion has not been implemented.

† These parts must have an access time of 350 ns maximum.

‡ If basic ROM has been overlayed by 8K × 8 RAM, program memory cannot be expanded by another 8K × 8, but only by three of the 2K × 8 patches as shown above.

You must install either W5, W6, or W7 in all configurations, if none of these jumpers is required by the above specification. Install one that enables the 8K ROM in an unused address space.

You can use jumper 15 in place of jumper 10, or jumper 16 in place of jumper 9, if a high asserted chip select is desired on an 8K ROM.

6.2.4 Alternate Character Set

If the AVO is present and an alternate character ROM is installed on the terminal controller, you can select an alternate character set on a character-by-character basis. The alternate character set can provide an additional 127 characters. If the AVO is installed without the alternate character ROM, any character cell in which the alternate set is selected appears white (black if reverse video). See Appendix A (select character sets) for selection of alternate characters.

6.2.4.1 Alternate ROM Description

1. Size: 2048 words × 8 bits

2. Speed: 300 ns access time if 132 column operation is desired; 550 ns access time is sufficient for 80 columns only.

3. Pin-out (Intel 2316E equivalent)

Pin No.	Pin Name	Use for Alternate Character ROM
1	A7	Character address 3
2	A6	Character address 2
3	A5	Character address 1
4	A4	Character address 0
5	A3	Scan address 3
6	A2	Scan address 2
7	A1	Scan address 1
8	A0	Scan address 0
9	D0	Fill bit
10	D1	Rightmost character bit/character data 1
11	D2	Character data 2
12	GND	Ground
13	D3	Character data 3
14	D4	Character data 4
15	D5	Character data 5
16	D6	Character data 6
17	D7	Leftmost character bit/character data 7
18	CS2	Chip select – asserted low
19	A10	Character address 6
20	CS1	Chip select – asserted low
21	CS3	Chip select – asserted low (Paragraph 6.2.4.2 below)
22	A9	Character address 5
23	A8	Character address 4
24	Vcc	+5 volts

6.2.4.2 Character ROM Programming Instructions

1. Chip selects must always be asserted low.

   (To allow use of pin compatible UV erasable PROMs, pin 21 may be tied to +5 V by removing W4 and inserting W5. The speed restrictions listed above still apply.)

2. A high coming from a character data pin produces a dot on the screen. A high from the fill bit causes the right space, between the character in which the bit is asserted and the following character, to be filled on the scan(s) for which the bit is asserted. One-dot-wide horizontal spaces in a character are filled by the dot stretcher.

   The following scan and character addresses are in hex.

3. Scan addresses

Scan Address	Character Scan Number (Figure 4-6-17)	
F	1	Normally blank in VT100 main ROM
0	2	Top of normal uppercase character
1	3	
2	4	
3	5	
4	6	
5	7	
6	8	Bottom of normal uppercase character
7	9	Normal descenders (underline scan)
8	10	Normal descenders
9-E		Not displayed

4. Character address 7FH is not displayed and should be left blank. Character addresses 20H–7EH are accessed by ASCII codes 20H–7EH respectively when the VT100 character set is set to "alternate character ROM" (Appendix A, select character sets). Character addresses 0H–1FH are accessed by ASCII codes 5FH–7EH respectively, and character addresses 20H–5EH respectively, when the VT100 character set is set to "alternate special graphics" (Appendix A, select character sets).

6.2.5 AVO Technical Description

This section provides a technical description of the advanced video option board.

6.2.5.1 Extended Character and Attribute Memory – The complete address and data buses from the microprocessor enter the AVO through the circuit board connector. Bits A00 through A09 directly access 1K of 8-bit RAM (E18 and E20) when A10, A11, and SEL 8–12K enable the RAM chip selects. The Select Attribute RAM (SEL ATT RAM) signal, decoded on the basic video board, enables the 4K × 4 memory (E2, E7, E10, E14) for writing and reading attributes. When read by the microprocessor, these 4K words appear in address space 3000H to 3FFFH and the four bits of each word appear on D0–D3. The attribute bits are read and written by the microprocessor through buffer E11 which is configured to drive the four bits in one direction or the other. One half of E9 and a pull-up resistor form an OR gate, so that data is output from the board when MEM RD and SEL ATT RAM are both asserted. During a DMA by the video processor, the four attribute bits are read in parallel with the seven character address bits and one attribute bit from the memory on the terminal controller. This is done by enabling the RAM outputs to the attribute latches whenever an address in the range of 2000H through 2FFFH is accessed during a DMA.

6.2.5.2 Character Attribute Latches – The attributes have their own set of character-clocked latches to provide complete synchronization of attribute and character data in the video processor. At the assertion of Hold Request and DMA Enable, data passes from the attribute RAM to the input of latch E5. As with the characters in the character latches the attributes shift through D1-4 of E5, then through E9 to the attributes line buffer E4 for storage, and again through D5-8 of E5 to the attribute inputs to the video processor on the basic video board. The attributes line buffer (E4) is addressed by the same LBA signals as the line buffer on the basic video board.

6.2.5.3 Program ROM Decoding – The AVO has sockets for four 2K or one 8K and three 2K ROMs. You can select the address blocks that these ROMs operate in with wire jumpers (or switches in newer models) on the AVO board. Flexible decoders can address the ROMs as extended program memory or a ROM can overlay an existing block of program. When existing memory is being overlayed or memory above 4000 H is being addressed, the Memory Disable signal is asserted to turn off memory on the basic video board.

6.2.6 Troubleshooting the AVO

This is mostly an extension of the character latches in the video processor. You may suspect problems in the AVO if character attributes will not work (check with the SET-UP Screen Test). Also, a portion of the screen RAM resides on the AVO. Problems are evident if the screen is full in 132 column mode. (Type **<ESC> # 8** in local mode to get the E test pattern.) Check the power connections, memory decoders, and the memory disable control line.

Self-test tests the AVO RAM. If you suspect errors in the AVO, but it passed self-test, the problem may be on the attribute latch (video processor) side of the AVR RAM control circuits.

6.3 20 mA CURRENT LOOP ADAPTER

The VT100 current loop adapter converts the Electronic Industries Association (EIA) standard serial voltage input and output from the basic video board to 20 mA current signals. You can separately switch both receiver and transmitter to operate either passively or actively.

6.3.1 20 mA Current Loop Option Installation

Use the following procedure to install the 20 mA Current Loop Option.

1. Remove the terminal access cover.
2. On the new terminal access cover with the 20 mA current loop card, set the TRANS switch to the NORMAL position (Figure 6-14). (If the terminal must provide current on the receiver line set the switch to the ACT position.)
3. Set the REC switch to the NORMAL position (Figure 6-14). (If the terminal must provide current on the receive line set the switch to the ACT position.)
4. Connect P5 to J5 on the terminal controller board (Figure 6-13).
5. Install the terminal access cover containing the 20 mA current loop option in place of the old access cover.
6. Connect the communications line to the Mate-N-Lok connector on the bottom of the access cover.
7. Perform the 20 mA current loop option checkout.

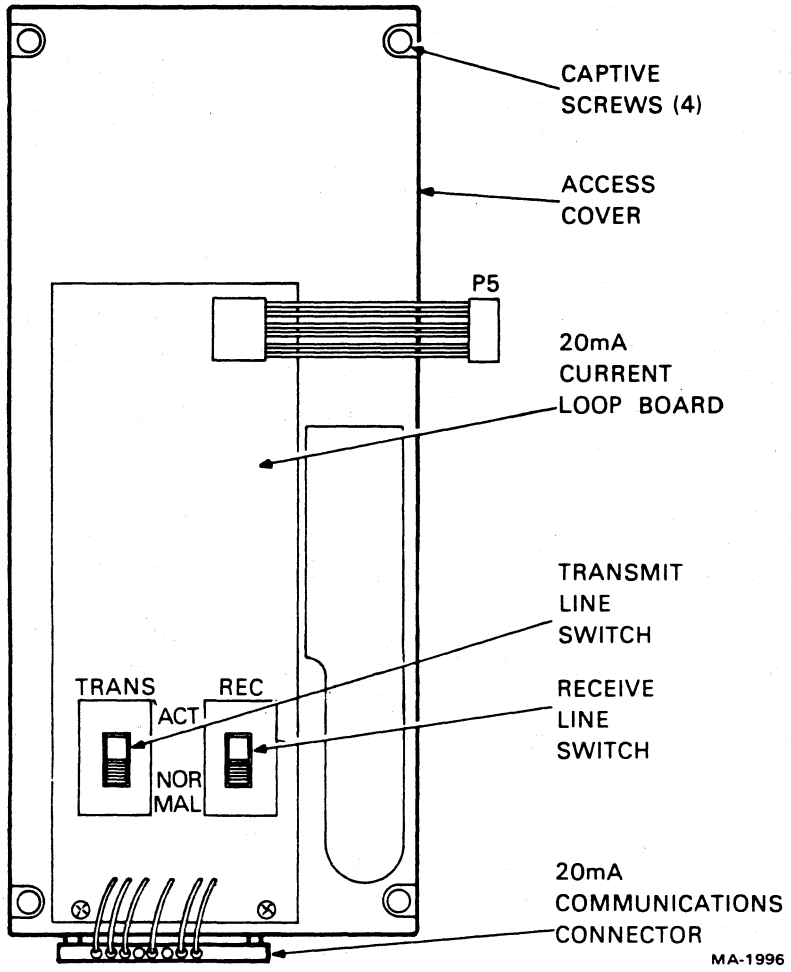


Figure 6-14 20 mA Current Loop Option

6.3.2 Configurations

In most current loop applications, the VT100 is connected in a passive configuration – that is, current is supplied to the VT100. In this mode, the transmitter and receiver are both passive, both optically isolated, and the transmitter goes to the mark state when power is turned off.

Conversion from active to passive mode (or vice versa) for either transmit or receive side is switch-selectable.

In active mode either the transmitter, or the receiver, or both may be connected so that the VT100 sources the 20 mA of current. In active mode, isolation is not present, and the transmitter goes to the space state when power to the VT100 is turned off.

6.3.3 20 mA Current Loop Option Checkout

The VT100 contains an internal test called the data loopback test. In the data loopback test the VT100 transmit and receive lines are connected to each other via a special external connector. A predefined set of characters are then transmitted. The terminal receives the characters and compares them to the characters transmitted. If the characters do not match an error is then flagged.

Use the following procedure to check out the operation of the 20 mA current loop option.

1. Disconnect the terminal from the communications line.

2. Remove the terminal access cover containing the 20 mA current loopback board and set both switches to the NORMAL. Reinstall the access cover.

3. Connect the 20 mA loopback connector (PN 70-15503-00) to the Mate-N-Lok connector on the bottom of the access cover.

4. Place the terminal in ANSI-compatible mode (in SET-UP B, group 2 switch 3 = 1).

5. Type <**ESC**> **[2;2y** to perform the data loopback test.

   After the test is complete, the screen clears and the message "WAIT" appears in the upper-left corner of the screen. The test takes about six seconds to run.

6. A loopback error is shown by an 8 in the upper-left corner of the screen. If an error is detected, check the 20 mA board connectors and switch settings and then repeat step 5.

7. After the test is complete, return the 20 mA current loop board switches to the original positions, remove the loopback connector, replace the access cover, and reconnect the terminal to the communications line.

NOTE

The terminal can use either 20 mA or EIA communications. If EIA is used on a terminal containing the 20 mA option, the cable connecting the 20 mA option board to the terminal controller board at J5 must be disconnected.

6.3.4 Current Loop Principles

The current loop system was designed for teletypewriter communications between remotely located stations. The 20 mA current was designed to operate the selector electromagnet that decodes data in teleprinters. All teletypewriters on a circuit were in series so that any station could signal all the other stations simultaneously by passing and interrupting the current through all stations' selector magnets. Today, decoding of the current signal is performed electronically, rather than mechanically, but the good noise immunity of the system has kept it around as a reliable way to run lengthy in-house terminal drops at low cost. Figure 6-15 defines the states of the interface line.

6.3.4.1 Current Loop Adapter Description – This section describes both the transmitter and receiver sides of the current loop adapter.

6.3.4.1.1 Transmitter Side – An EIA-to-TTL level converter (E3) inverts the VT100 output signal, but a second stage reinverts it. The TTL signal switches a pair of paralleled open-collector drivers that drive the LED inside an opto-coupler. Resistor R11 limits the LED current. The LED output controls the conductance of the phototransistor inside the opto-coupler. The transistor's base is tied to its emitter by R13 and its base is tied to its collector by D5 to improve its switching speed.

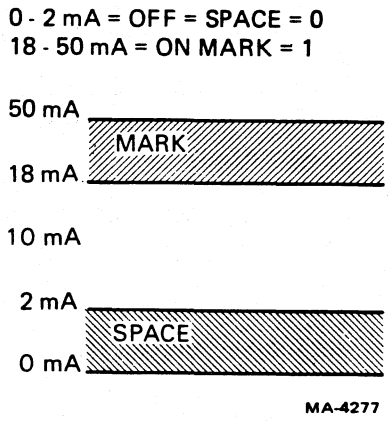


Figure 6-15 Interface States

When the phototransistor is conducting, the base drive for Q3 is diverted and Q3 and Q4 are cut off to put the transmitter in the space state. The only current that can flow in the space state passes through D3, which is a constant current diode rated for 1 mA. When the phototransistor is cut off, D3 provides base drive to Q3 and forces the transmitter to the mark state. Use of the constant current diode D3 allows sufficient base drive to Q3 to keep the transmitter in the mark state when the phototransistor is cut off or when power is removed from the VT100. But D3 still limits the current through the transmitter in the space state to less than 2 mA even with 50 volts across the circuit.

In passive mode the transmitter can control the flow of current from an external current source. In active mode the transmitter is placed in series with current supplied from the +5 volt and −12 volt power supplies and limited by series resistance.

6.3.4.1.2 Receiver Side – Passive: The optional capacitor on the input gives line transient immunity. The LED in opto-coupler E1 accepts current from a remote source limited by R2 and Q1. To ensure proper recognition of the off state, R1 draws 3 mA to bypass low level currents around the LED. If the line current rises to make the voltage drop across R2 greater than 0.6 volts, transistor Q1 turns on to shunt excess current around the LED. Besides protecting the LED, this also improves speed by reducing saturation of the LED and transistor. D1 protects the circuit from reverse connection of the signal line.

Active: With switch SW2 in the up position, the adapter provides power for the line: +5 volts and −12 volts through similar resistors R8 and R9. The remote device passively switches current to activate the circuit.

The phototransistor in the opto-coupler controls the base current to Q2. R5 speeds up Q2's turn-off by pulling the base down faster. C1 speeds Q2 turn-on. R3 prevents the phototransistor from saturating by allowing the base and emitter voltages to rise until excess base charge can be removed by conduction through R4.

The output is pseudo EIA (RS-232) because it assumes that a particular receiver device is being used which happens to accept a 0 as a mark. The normal RS-232-C specification calls for +6 = space and −6 = mark. D4 shunts −12 in case someone connects the EIA signal to the exposed connector while the current loop is installed. It protects E2 pin 3. R7 pulls up to give high drive to the 1489EIA receiver – TTL converter on the basic video board.

6.3.5 Interface Signals

The currrent loop option interfaces to external communication equipment through an 8-pin Mate-N-Lok connector as described below.

Pin No.	Signal Name	Description	
		Passive Mode	**Active Mode**
1	Negative Test Voltage	V− with a series resistance of 480 ohms ±5%.	
2	Transmit negative (T−)	Current flows away from this terminal.	Current flows into this terminal which is connected to V− via a series resistance Rs.
3	Receive negative (R−)	Current flows away from this terminal.	Current flows into this terminal.
4	(Not used)		
5	Transmit positive (T+)	Current flows into this terminal.	Current flows away from this terminal. The equivalent voltage source is (V+)−Vd with a series resistance Rs.
6	(Not used)		
7	Receive positive (R+)	Current flows into this terminal.	Current flows away from this terminal which is connected to V+ via a series resistance Rs.
8	Ground		

V− = −12 Vdc ±5%
V= = +5 Vdc ±5%
RS = 330 ohms ± 5%
Vd = 2.0 V maximum

6.3.6 Interface Specifications

Transmitter	**Min**	**Max**
Open circuit voltage	5.0 V	50 V
Voltage drop marking	0.0 V	2.0 V
Spacing current	–	2.0 mA
Marking current	20 mA	50 mA

Receiver	**Min**	**Max**
Voltage drop marking	–	2.3 V
Spacing current	–	3.0 mA
Marking current	15 mA	50 mA

6.3.7 Troubleshooting the Current Loop Adapter

Except for incorrect setting of the normal (active) and passive selection switches and connector problems, malfunction is probably due to bad semiconductors.

6.4 VT105 GRAPHICS PROCESSOR

This section describes the VT105 waveform generator module, M7071. The M7071 complements the VT100 alphanumeric terminal by adding graph drawing capabilities. Together they comprise the VT105 alphanumeric and graphic terminal. This section describes the following items.

- the graph module in a block diagram format
- decoding the input
- establishing mode of operation
- phase lock loop timing
- rectangular aspect ratio graph drawing field
- square aspect ratio graph drawing field
- loading the registers
- loading graph memories
- generating baselines
- loading vertical and horizontal lines
- generating strip charts
- combining video out

6.4.1 Enabling Graphic Information

On initializing the VT105, the M7071 forces the GRAPHICS FLAG low so the VT100 terminal controller module recognizes that the graphics option is installed.

To enter the graph drawing mode, an escape sequence ESC 1 is needed. The terminal remains in this mode until ESC 2 is received. In this mode, graphics data is passed to the M7071 on parallel data lines. When data is passed, the GRAPHICS FLAG goes high and stays high until the data is stored in the static random access memories (RAMs). This signal is sensed by the VT100 terminal controller, and does not pass another character to the M7071 until this signal goes low.

The M7071 also uses the following signals from the VT100.

DO 00 H – DO 06 H – The parallel 7-bit graphic information in the form of a character to the M7071.

DO 07 H – This signal is used by the VT105 for hard copy.

RESET H – The M7071 uses this signal on power up to initialize its registers. Pressing the **RESET** key during SET-UP mode also generates this signal.

HORIZ BLK H – Defines the horizontal blank time of 11.4 μs. The horizontal active time is 52.1 μs; the total period is then 63.5 μs.

VERT BLK L – Vertical blank time is 1.016 ms. Vertical active time is 15.24 ms for a total period of 16.256 ms.

WR GRAPHICS L – A pulse passed to the M7071 to strobe the parallel data (DO 00 H – DO 06 H) into the input latch.

GRAPHICS 1 IN L and GRAPHICS 2 IN L – The video output from the M7071.

The following paragraphs provide a brief discussion of the waveform generator block diagram, Figure 6-16.

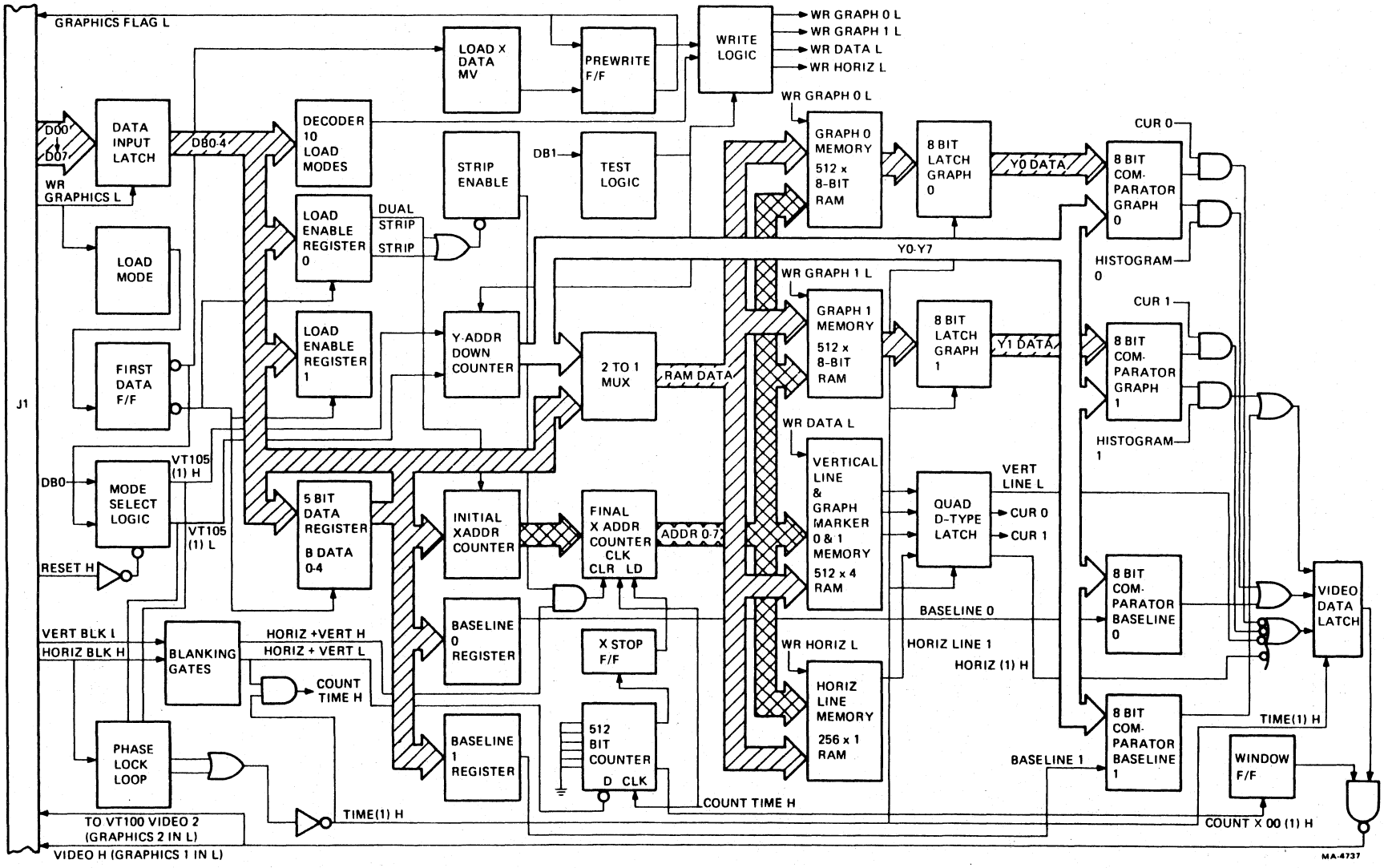


Figure 6-16 M7071 Waveform Generator Block Diagram

6.4.1.1 Writing Data to the Waveform Generator (block diagram discussion) – Data in the form of 7-bit ASCII characters is received by the data input latch. The first character must be a control character to give instructions to the waveform generator module as to where to place the next data information. Is the next data to be loaded into the registers or into the graph memories? Is it horizontal line data or vertical line data? The control character is loaded into a binary to decimal decoder that enables 1 of 10 load modes. (See Paragraph 6.4.1.3 to decode the input character.)

One of these modes is load enable register 0; another is load enable register 1. These two registers store the information as to the type of graph desired (line graph, shaded graph, or strip chart) and the desired graph features (horizontal lines, vertical lines, and graph markers). Both registers use either one or two data characters to enable the desired graph features. The First Data flip-flop keeps track of these two data characters. Two data characters form a data word.

The second data character following a load enable register 1 command enables the mode select logic. Data bit 0 of this character determines the aspect ratio of the graph to be displayed on the video screen. When this bit is set to 1, the square aspect ratio is enabled. This aspect ratio is a new feature of the VT105 and uses all 240 scan lines on the terminal. When this bit is set to 0, the rectangular aspect ratio is selected. This aspect ratio is compatible with previous DECgraphic video terminals (i.e., VT55) and uses only 230 scan lines of the terminal for the graph display. This later aspect ratio is also enabled during the power-up sequence of the terminal (by RESET H).

The outputs of the mode select logic go to a phase-lock-loop to establish the two timing signals necessary to set up the rectangular and square aspect ratios. These are 10.4 MHz and 12.4 MHz, respectively. The phase-lock-loop has a phase detector to monitor the horizontal blank signal from the VT100 and divides the frequency of this signal by a set number for each aspect ratio.

Another function of the decoder is to select the memory into which the data is to be loaded. This may be Graph 0 memory, Graph 1 memory, vertical line and graph marker memory, or horizontal line memory. Data to these memories must always be in the form of two data characters (one data word). A 5-bit data register holds the first character while waiting for the second. Then they are both parallel loaded through a 2-line to 1-line multiplexer, becoming RAM DATA to the inputs of each of the memories. The memory enabled to "write" at this time is determined by the decoder. The load enable signal from the decoder is synchronized by the First Data flip-flop and the Load X-Data multivibrator. One of the following signals is enabled to the memories.

WR GRAPH 0 L
WR GRAPH 1 L
WR DATA L
WR HORIZ L

Data is then written into the appropriate memory, as shown in Figure 6-16.

Data for the shade lines (base lines) is loaded into Baseline 0 register and/or Baseline 1 register.

Data for the starting X-address is loaded into the initial X-address counter. The final X-address counter is loaded to this starting X-address at the end of the current scan (by the 512-bit counter). Data for successive X-address positions in memory only require one control character. The final X-address counter increments the position in memory for placing the new data.

When a strip chart is enabled (from register 0), the clear input to the final X-address counter is disabled. This counter does not reset to zero, but rather it follows the initial X-address counter. New data increments the X-address and is added to the end of the graph. This new data is the last data to be read from memory. Previous data is read one position earlier causing a shift in the video graph to the left.

6.4.1.2 Reading Data from the Waveform Generator (block diagram discussion) – As long as the terminal is in graph mode, the *enabled* graph data is read continuously from the waveform generator module. The Y-address down counter is initially preset to one of two values: 240 lines for the square aspect ratio, or 230 lines for the rectangular aspect ratio. The output of this counter is enabled through the 2-to-1 multiplexer, becoming RAM DATA to strobe the row address of the memories. As each scan proceeds across each row, the X-address counter strobes the column address of the memories.

The output of each memory is strobed into a corresponding D-type data latch. This provides buffering, as well as an input source for rewriting the data back into memory so it is not lost. The data from each memory is sent to a respective 8-bit comparator where the data is compared to the Y-address (Y0–Y7).

If both inputs are high at the same time, a high output is sent to the video data latch to intensify that position on the screen. If a histogram is enabled, all points below the graph position are also intensified. If a cursor (graph marker) is enabled, 16 points are intensified on the screen creating a short vertical line on the graph at a specific graph point. If a shade line (base line) is enabled at a specific Y-address: (1) all X-address positions on that line are intensified on the screen; and (2) all positions between the graph data and the shade line are also intensified. If a vertical line is enabled at a specific X-address, that X-address is intensified on each scan creating a vertical line on the screen.

All data is presented to the video data latch. At alternate times Histogram 0 and Histogram 1 data are gated out. This allows two shaded graphs to be displayed on the screen and still be discernible in overlapping areas. Graph markers, horizontal lines, and vertical lines are clocked to the output every TIME (1) H pulse. This timing comes from the phase-lock-loop previously mentioned.

The blanking gates keep track of both horizontal and vertical blank times from the VT100 and create the signal HORIZ + VERT H. This signal is used to clear the X-address counter and a 512-bit counter. Every COUNT X 00 (1) H from this counter clock the window flip-flop at the proper time to gate the video to the VT100 terminal controller. These signals are VIDEO H (GRAPHICS 1 IN L in the VT100) and VIDEO 2 (GRAPHICS 2 IN L).

6.4.1.3 Decoding the Input – When the data received is one of the control characters listed in Table 6-1, bits 0–3 of the character are used to determine which control signal to enable. Only one set of control characters is used for one M7071. The extended character set is primarily used for a second M7071 installed in the same terminal to enable up to four graphs or strip charts. These bits are sent to a binary to decimal decoder (Figure 6-17) that enables only one of the outputs at a time.

Table 6-1 Control Characters

Char	Octal Code	Enable Signal	Unit 0 Ext Char	Unit 1 Octal Code
@	100	Load Baseline	P	120
A	101	LD ENABLE 0 L	Q	121
B	102	LD GRAPH 0 L	R	122
C	103	LD CURSOR 0 L	S	123
D	104	LD HORIZ L	T	124
H	110	LD X L	X	130
I	111	LD ENABLE 1 L	Y	131
J	112	LD GRAPH 1 L	Z	132
K	113	LD CURSOR 1 L	[	133
L	114	LD VERT L	\	134

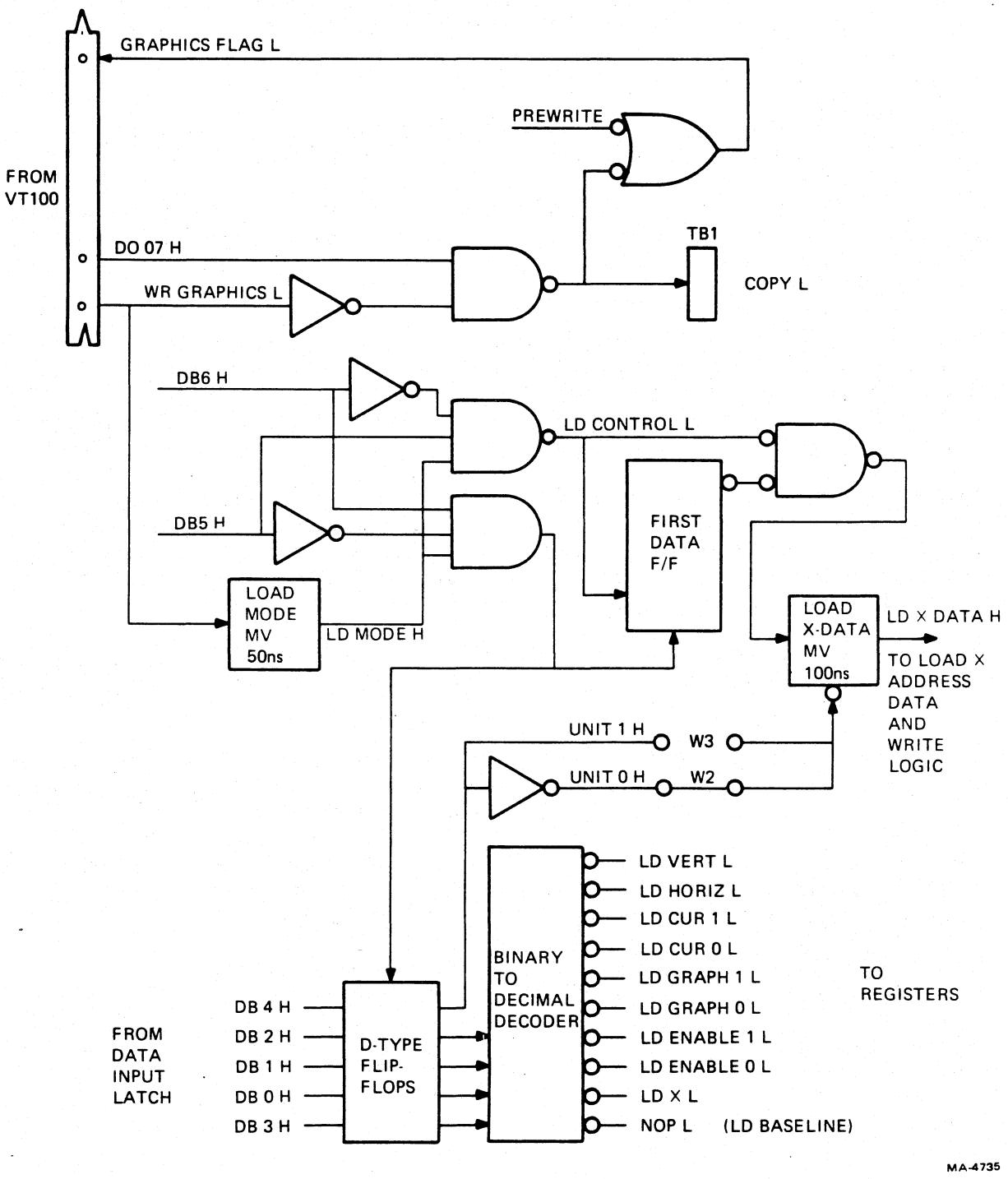


Figure 6-17 Decoding the Control Character

The extended character set is reserved for future expansion. Current software does not support the extended character set. Discussion in this chapter is limited to unit 0 to avoid confusion.

Data bit 4 is used to load X-data and select Graph 1.

Two ASCII characters are necessary to transmit a complete data word. Data bits 5 and 6 monitor these data bits. The first flip-flop keeps track of the first and second data characters.

Data bit 7 (DO 07 H) forces the GRAPHICS FLAG high to halt further transmission from the VT100 terminal controller while the video screen is being copied by a hard copy unit. Signal COPY L is sent to the hard copy unit on TB1. The hard copy unit must detect and hold this signal low while it copies the screen.

6.4.1.4 Selecting Mode of Operation – There are two formats or modes for setting up the display: rectangular format and square format. The rectangular format uses a 10.4 MHz signal to display graphic data on the video screen in an area 230 dots high by 512 dots wide, as shown in Figure 6-18. The square format increases the rate of transmission to 12.4 MHz. The same graphic information is displayed in a more compact area, as shown in Figure 6-19.

Rectangular Aspect Ratio – In the rectangular aspect ratio graph drawing field, (Figure 6-18) space is provided in the left margin for one character. Under the graph field, there is space for one line of characters. To set up the left margin, a delay is needed before starting the graph. Two signals (1.2 μs and 320 ns) are added together to create a 1.52 μs delay after horizontal blank time. This time allows space for one character in the left margin before starting the first X-address of the graph.

The horizontal line counter is initially loaded to 230 scan lines. Twenty-three lines of characters, each having a 10-line scan cell, can print within the graph drawing field. A 24th character line can print under the graph field.

Square Aspect Ratio – In the square aspect ratio graph drawing field, (Figure 6-19) additional delay must be achieved before starting the first X-address. A 640 ns pulse clocks a counter loaded to divide by 8. A 5.12 μs delay occurs before starting the graph centering the graph field on the screen.

The square aspect ratio uses the full vertical screen area of 240 scan lines; 24 lines of alphanumeric data can be placed on the graph field. Up to eight characters may be placed on the screen to the left of the graph field; up to seven may be placed to the right of the graph field.

6.4.1.5 Decoding Field Selection – Selecting the field is accomplished by data bit 0 (DB 0) in the second data character following a Load Enable Register 1 instruction. The first flip-flop (Figure 6-20) keeps track of the first and second data characters. The second data character enables FIRST (1) L which clocks DB 0 into the VT105 mode select flip-flop. If DB 0 is high, the square field is enabled. If DB 0 is low, the rectangular field is selected.

The signal RESET H (INIT L) from the VT100 terminal controller clears the mode select flip-flop and also enables the rectangular field.

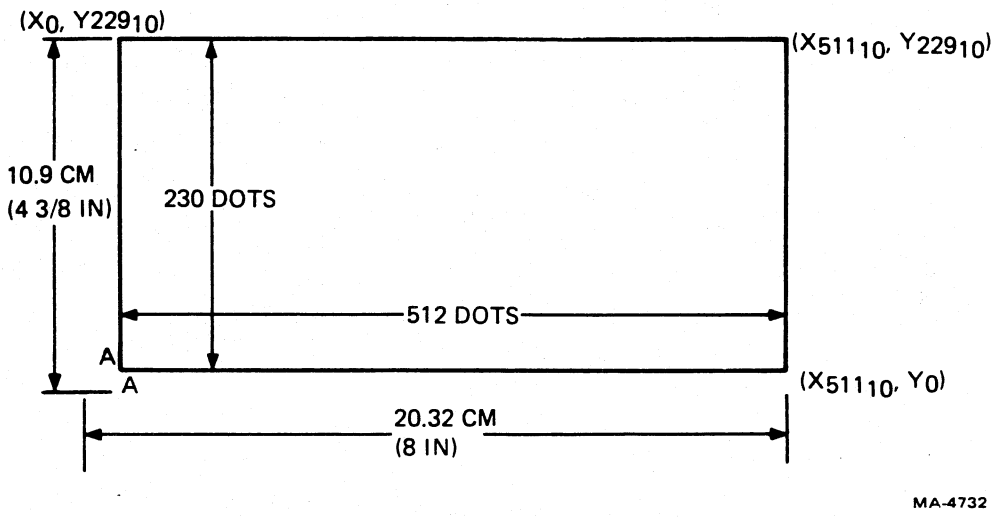


Figure 6-18 Rectangular Aspect Ratio Graph Drawing Field

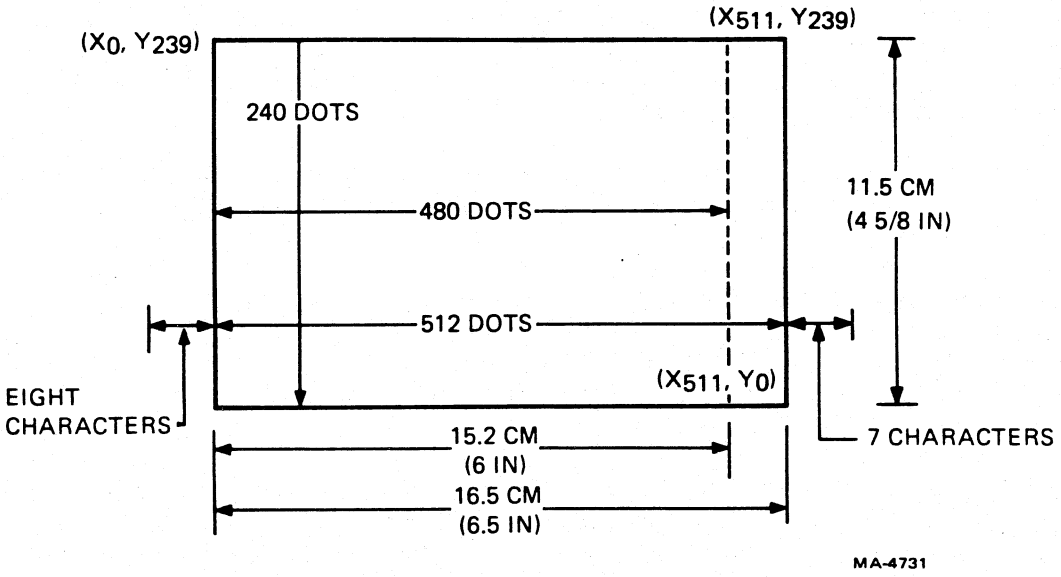


Figure 6-19 Square Aspect Ratio Graph Drawing Field

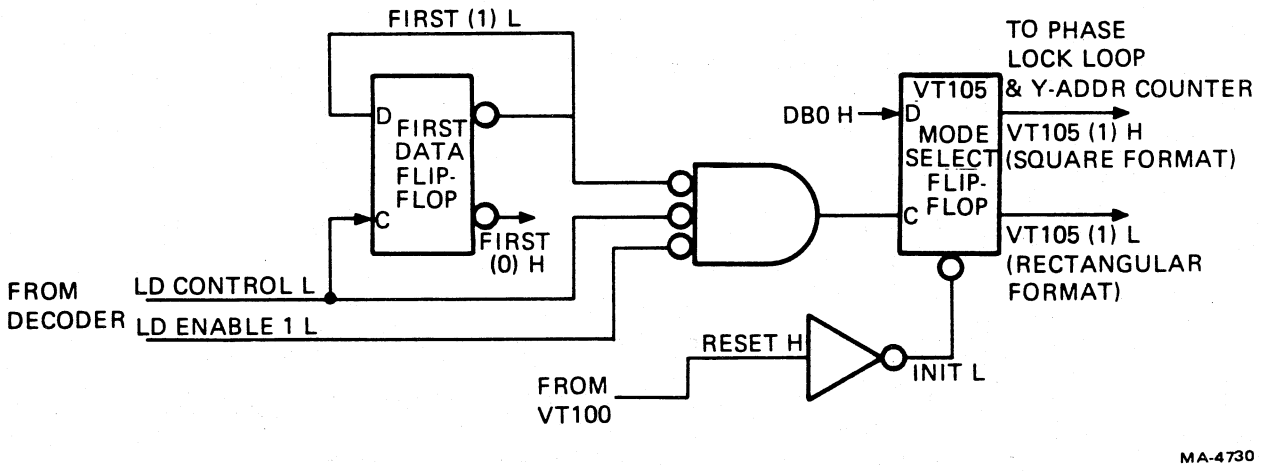


Figure 6-20 Selecting Mode of Operation

6.4.1.6 Phase-Lock-Loop Timing – A 10.4 MHz signal and a 12.4 MHz signal are needed to achieve the rectangular and square aspect ratio, respectively. A phase-lock-loop (Figure 6-21) generates and maintains these frequencies. The HORIZ BLK L signal from the VT100 terminal controller is used at one input to a phase detector. The phase detector monitors the output of the voltage controlled oscillator (VCO) to detect any frequency drift. The output frequency is divided by the number N in a counter to approximate the HORIZ BLK L input. The value for N is 662 for the rectangular aspect ratio and 800 for the square aspect ratio.

Should the frequency drift, the difference between the leading edge of the inputs to the phase detector is presented as a voltage change to the VCO and either raises or lowers the output frequency to compensate for the drift.

6.4.1.7 Establishing Desired Display – Selecting the desired graph, shading the graph, single or dual strip chart operation, and adding vertical and horizontal lines is initially stored in registers, shown in Figure 6-22. The signals LD ENABLE 0 L and LD ENABLE 1 L from the decoder enable register 0 and register 1, respectively. The first data flip-flop monitors the characters to enable the proper register to store the type of graph desired.

Loading Register 0 – The letter A, when typed on the keyboard or coded in a program, enables register 0. One or two data characters may follow this letter. The first data character is clocked into a D-type flip-flop to determine the graphs or histograms desired (Figure 6-23). DB 0 H must be set to display the graphic features enabled in register 0 and register 1; if 0, the graphic display is turned off.

A second data character may be used to set up baselines (shade lines) or strip charts (Figure 6-24). The state of the signal BASELINE CTRL determines whether Baseline 0 or Baseline 1 is to be loaded. If low, Baseline 0 may be loaded; if high, Baseline 1 may be loaded. See Paragraph 6.4.1.10 for more details on baselines.

DB 3 H enables the signal STRIP H to allow Graph 0 or Graph 1 to be a strip chart. DB 4 H enables STRIP H and DUAL STRIP H. Both signals are required to display both Graph 0 and Graph 1 as strip charts. Refer to Paragraph 6.4.1.15 for more information on strip charts.

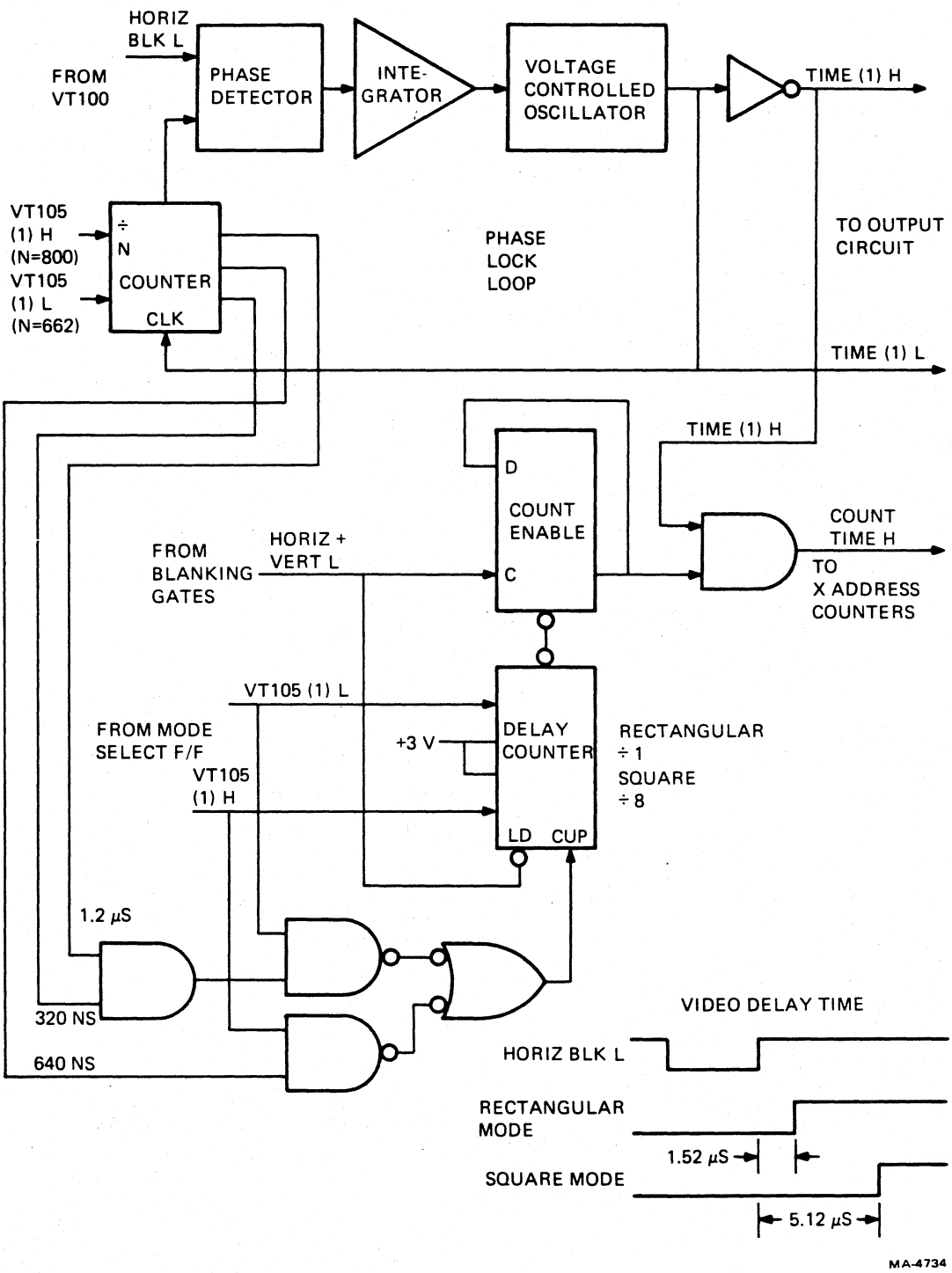


Figure 6-21 Phase-Lock-Loop Timing

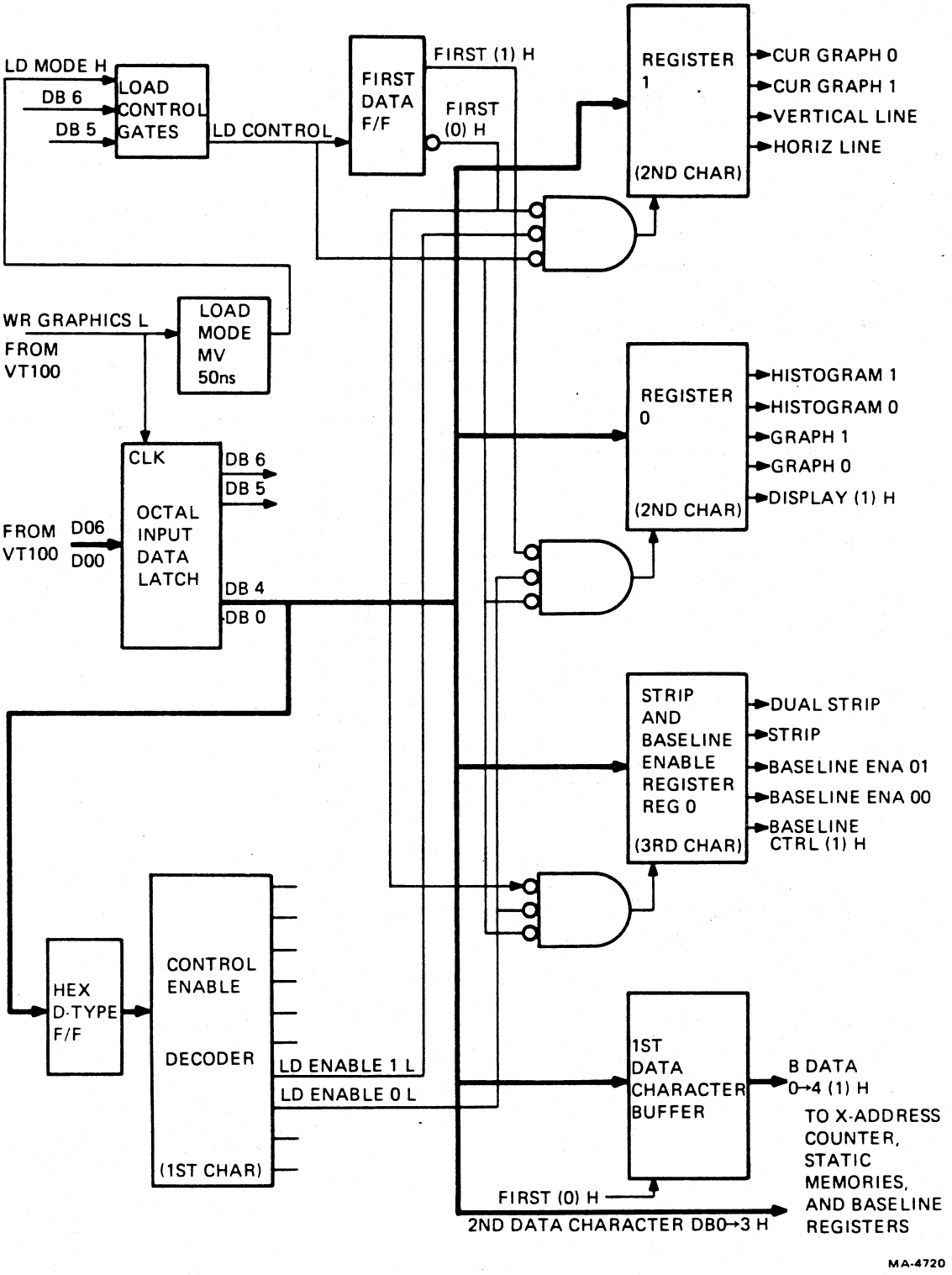


Figure 6-22 Loading the Registers

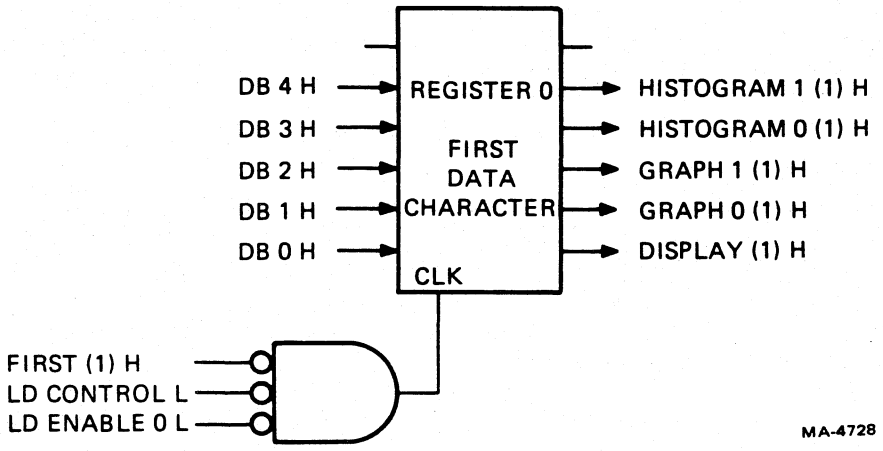


Figure 6-23 Register 0 (1st Data Character)

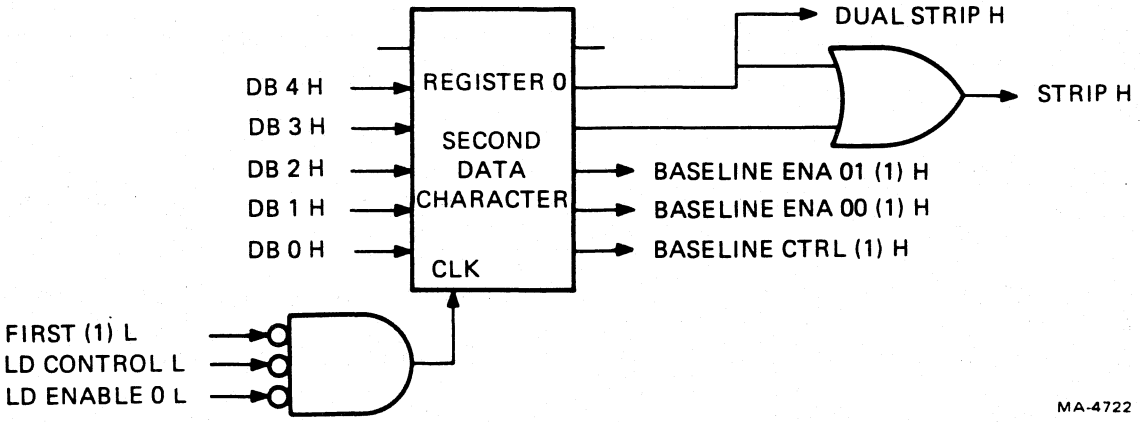


Figure 6-24 Register 0 (2nd Data Character)

Loading Register 1 – The letter I produces the signal LD ENABLE 1 L to enable register 1. One or two data characters may follow this letter. The first data character enables horizontal lines, vertical lines, and graph markers, as shown in Figure 6-25.

A second data character following the letter I enables the desired field and the interactive graphics test (Figure 6-26). The square field is established when data bit 0 is set to 1; the rectangular field is selected when DB 0 equals 0. The rectangular field is also selected during the initial power-up sequence of the terminal by the signal RESET H (INIT L) from the VT100 terminal controller.

The interactive test is used to check the M7071 in LOCAL mode of operation. See Paragraph 6.4.2.

6.4.1.8 Loading X-Address Information – In order to load the horizontal address of a dot or line, two data characters must be transmitted. The first character contains the lower five bits of the binary X-address and is stored in a register while waiting for the second character with the upper bits. When both characters are received, the signal LD X DATA H loads the initial X-address counter, (Figure 6-27). When the current scan is complete, this data is loaded into the final synchronous X-address counter and presented to the random access memories.

During a write data program, the signal LD X DATA L clocks the pre-write flip-flop which triggers the write monostable multivibrator. The write multivibrator enables one of four write pulses to the RAM memories, either WR GRAPH 0 L, WR GRAPH 1 L, WR HORIZ H, or WRITE DATA L. This latter pulse is the write input signal to the vertical line and graph marker static RAMs. If either of the graph write pulses or WRITE DATA L is present, the initial X-address counter is incremented to be ready for the next data point.

When the pre-write flip-flop is cleared, GRAPHICS FLAG L is sent to the VT100 terminal controller, confirming that the data has been stored in the static RAMs, and they are ready to receive a new data word.

6.4.1.9 Loading Graph Memories – Characters B and J produce signals LD GRAPH 0 L and LD GRAPH 1 L from the decoder. When enabled by the write multivibrator, these signals become WR GRAPH 0 L and WR GRAPH 1 L that determine into which memory to write the data.

The second and third characters of a load graph instruction form an 8-bit Y-value. This data passes through a two-line to one-line multiplexer becoming RAM DATA 0–7 (1) H, (Figure 6-28). The data is then written into memory in the address, XADD 0–7, from the X-address counter.

Each RAM memory has $256_{10} \times 4$ bits of space available. Four of these are connected together to provide 512×8 bits of memory for each graph. The signal X ADDR 8 L enables the upper memory addresses, location 256 to 511.

The M7071 uses a down-counter for a Y-address monitor. For the rectangular field, the down counter is initially loaded with address 230_{10} each time the scan reaches the bottom of the screen. The scan then starts at the top-left corner of the screen. After each row of X-address information is processed, the Y-address monitor is counted down one increment. (For the square field, the down counter is initially loaded with address 240_{10}.)

In order to read memory, only the X-address must be available. The position of the graph data is compared with the current Y-address of the scan. If they are equal and the graph is enabled, the position on the screen is intensified.

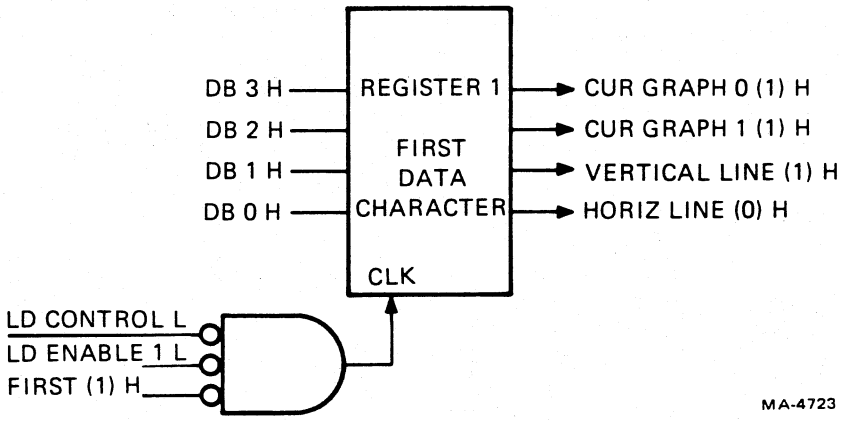


Figure 6-25 Register 1 (1st Data Character)

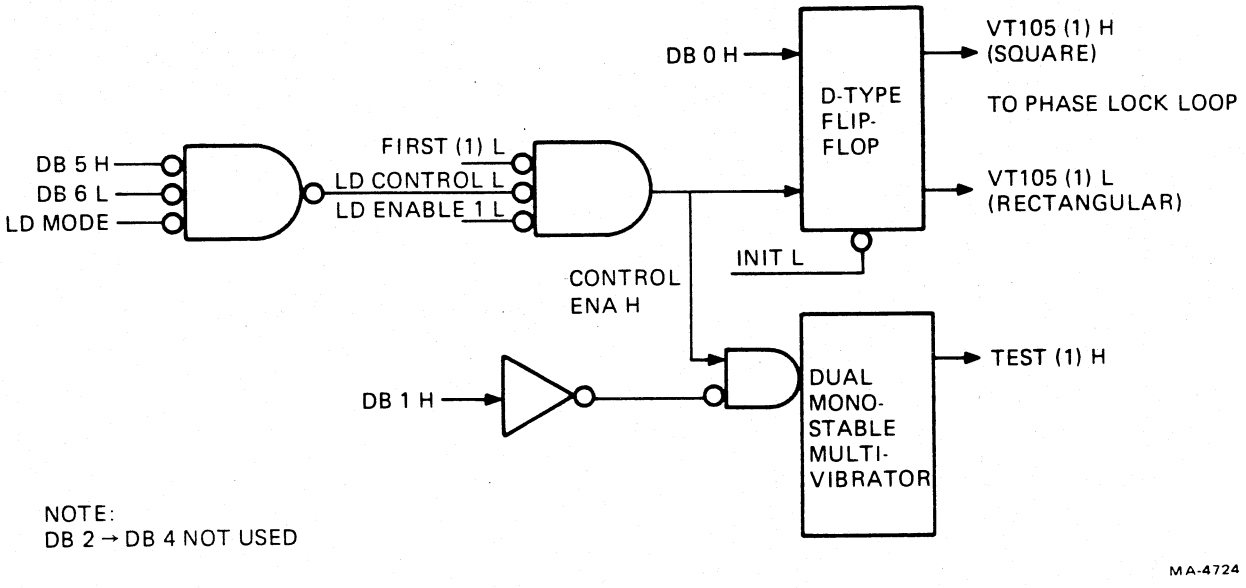


Figure 6-26 Register 1 (2nd Data Character)

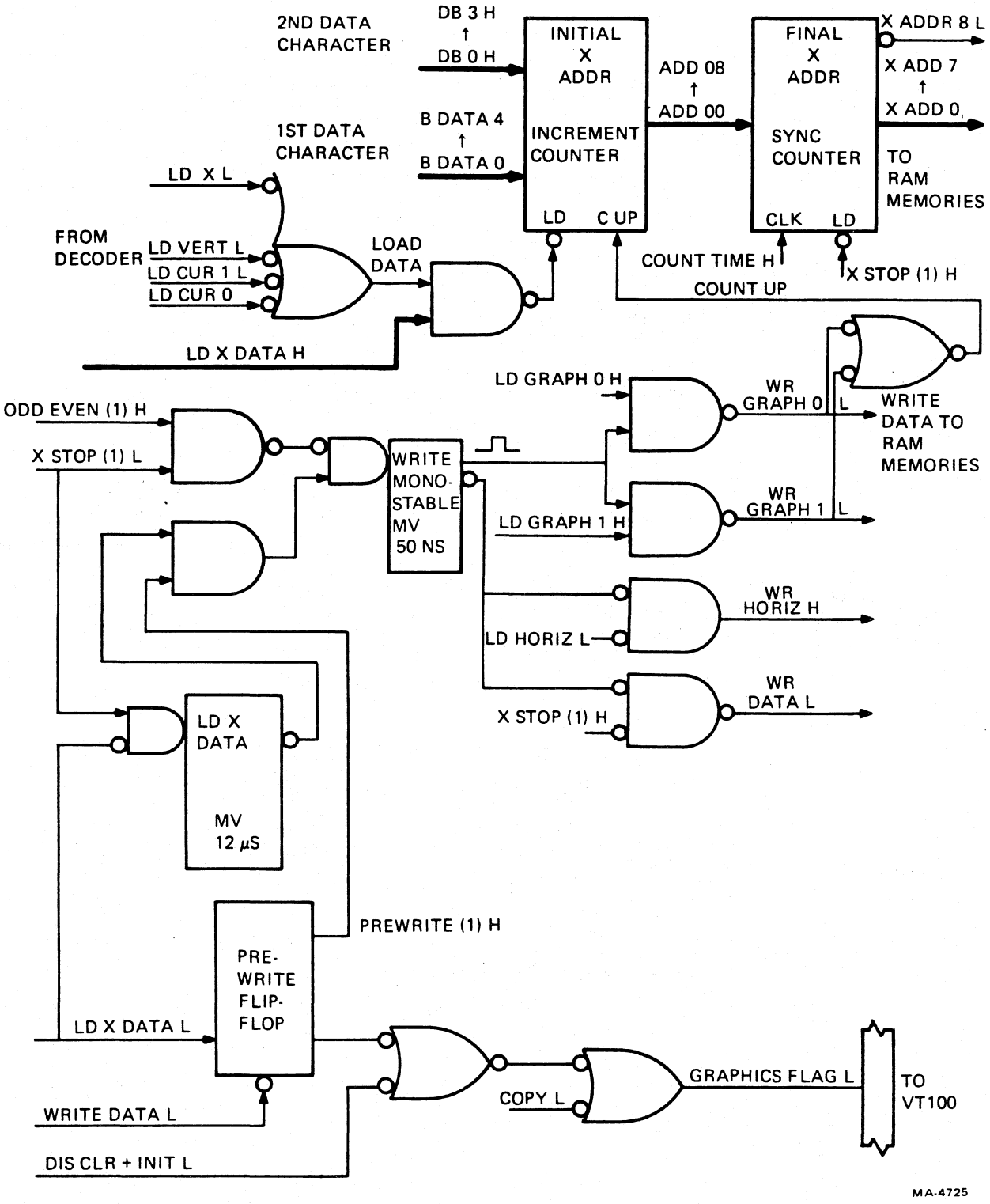


Figure 6-27 Loading Address Data

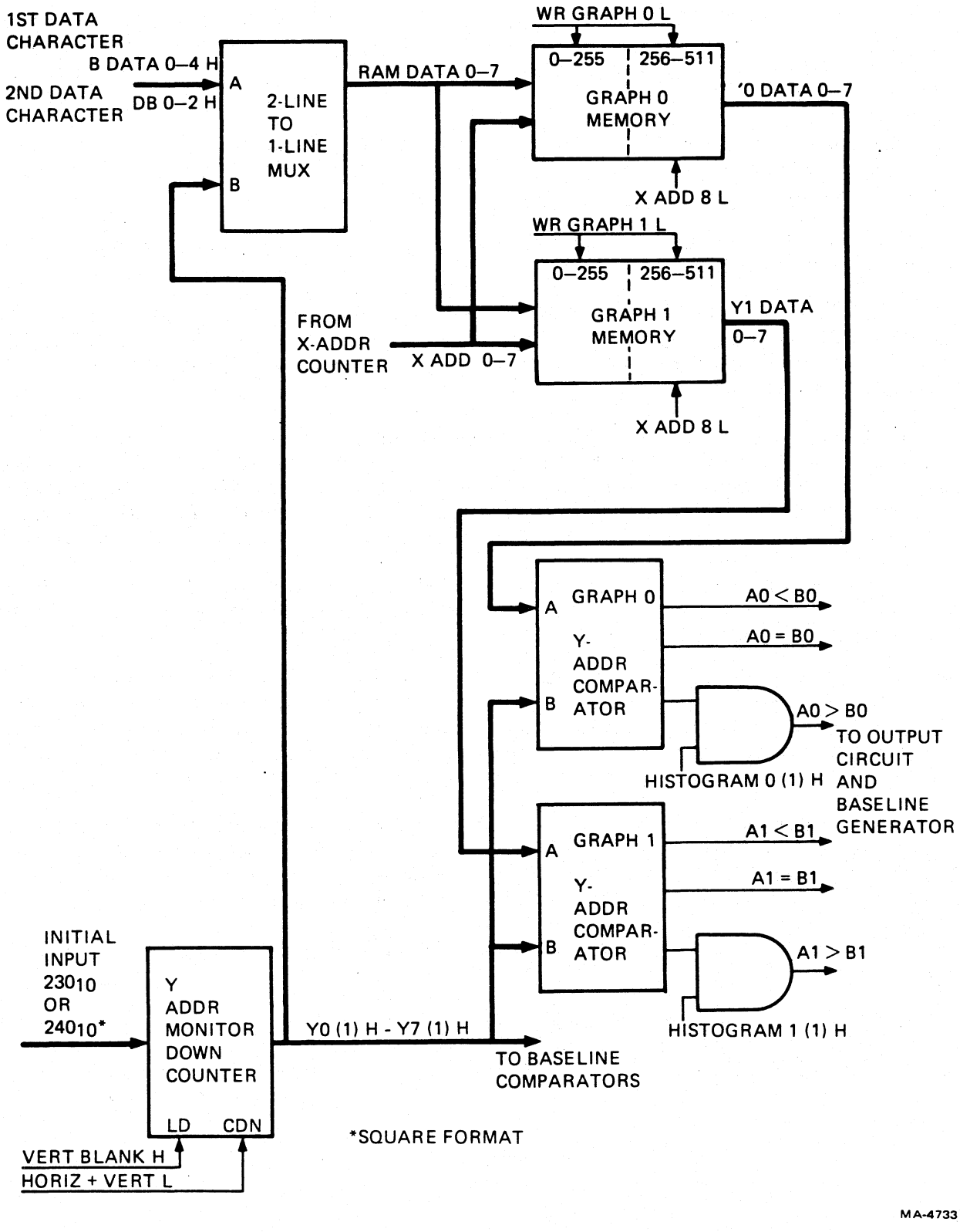


Figure 6-28 Graph Memory and Y-Address Monitor

6.4.1.10 Generating Baselines (Shade Lines) (Figure 6-28) – Data bit 0 in the second data character following a load register 0 creates a signal called BASELINE CTRL (1) H. If high, this signal loads a baseline for Graph 1; if low, it loads a baseline for Graph 0. (See Paragraph 6.4.1.7 for loading register 0.)

The position of the baseline is determined by two data characters following the character @ (NOP). As the scan proceeds from top to bottom, its Y-address is compared with the position of each baseline. When they are equal, the baseline is intensified on the screen.

6.4.1.11 Enabling a Histogram (Shading a Graph) – This section explains how to enable a histogram, with or without a baseline.

Without a Baseline (Shade Line) Enabled – Enabling a histogram intensifies points below a graph to the bottom of the graph drawing field. Data bits 3 or 4 in register 0 enable HISTOGRAM 0 (1) H and HISTOGRAM 1 (1) H, respectively. These signals, shown in Figure 6-28, enable all points below the graph determined by the Y-address comparator.

With a Baseline (Shade Line) Enabled – When its baseline is enabled, a graph is shaded between the graph line and its baseline. To do this, two sets of comparators are used. One comparator, shown in Figure 6-28, monitors the position of the graph with respect to the current scan. The other (Figure 6-29) compares the position of the baseline with that of the current scan. Together, they determine the points to be intensified. The baseline can be moved up or down, and the intensified area changes accordingly.

Bits 3 and 4 in register 0 enable Histogram 0 and Histogram 1, respectively. These bits should not be enabled if the baseline is enabled for that particular graph. Shading the histogram to line 0 eliminates the visual effect of shading only those areas between the graph and the movable baseline.

6.4.1.12 Loading Vertical Lines – Vertical lines are loaded with two data characters following the letter L. Bit 4 of the second data character [B DATA 9 (1) H] with LD VERT H from the decoder provide the data input (DI3) to the vertical line and graph marker memory. The other bits of the two data characters transmit the X-address in memory where the vertical line is to be stored. (See Figure 6-30.) If B DATA 9 (1) H is high, the vertical line is loaded; if low, the line is erased at that address.

Memory is continuously read by the X-address counter. Data in the current address is monitored by a D-type latch and is enabled only if VERTICAL LINE (1) H is present in register 1. This causes VERT LINE L to be sent to the output circuit. Every other point at a particular X-address is intensified to create a vertical line. Up to 512 vertical lines can be enabled on the graph field.

As the vertical line is read from the static RAM, its position is fed back (item C in Figure 6-30) and rewritten into the RAM so as not to lose the data.

When the strip chart feature is enabled, vertical lines follow the graph address in a wraparound fashion; that is, vertical lines move from right to left with the strip chart graph. When the current address exceeds address 511_{10}, the vertical line data is taken again from the beginning, address 0, 1, 2 . . ., etc.

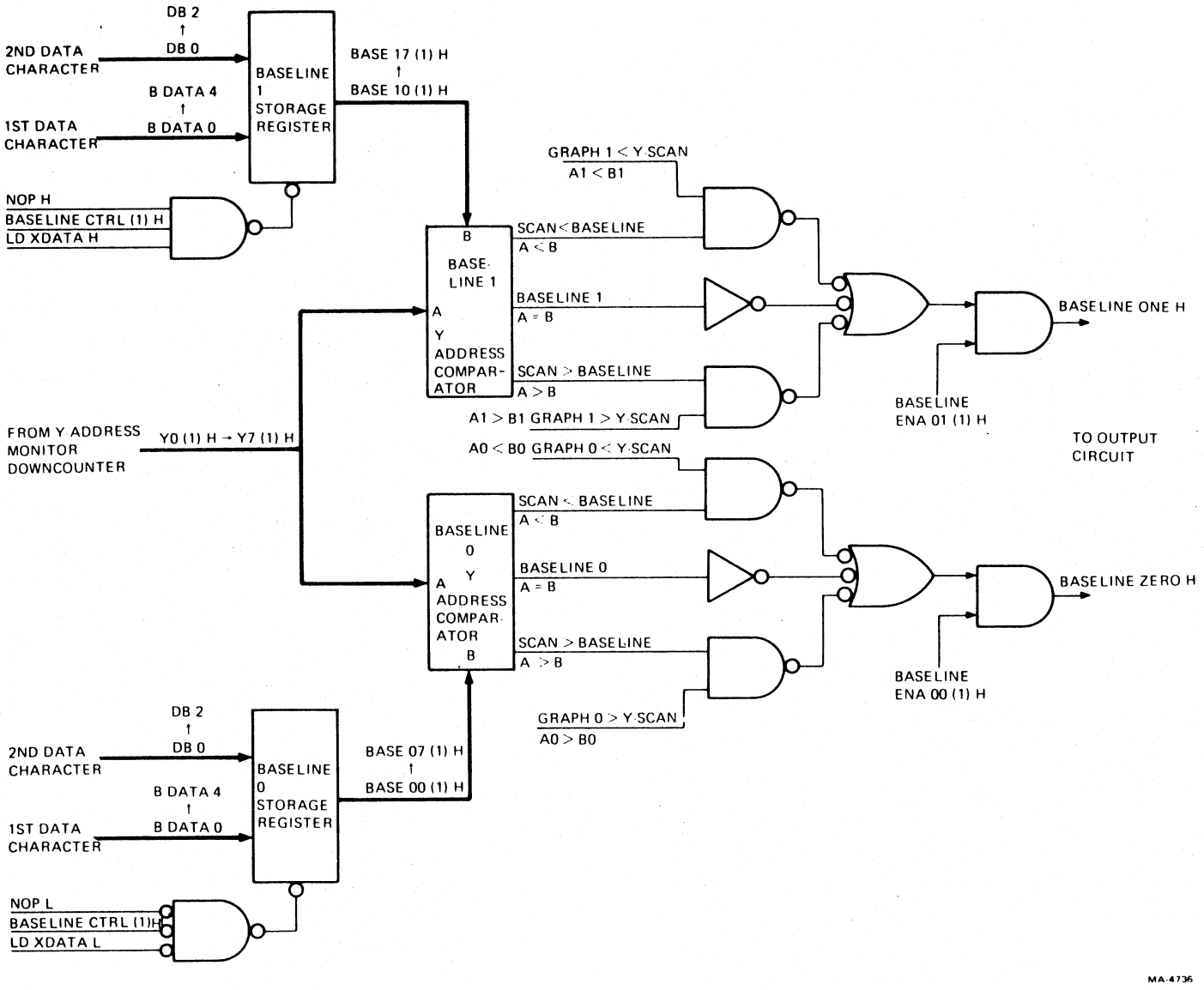


Figure 6-29 Baseline (Shade Line) Registers and Comparators

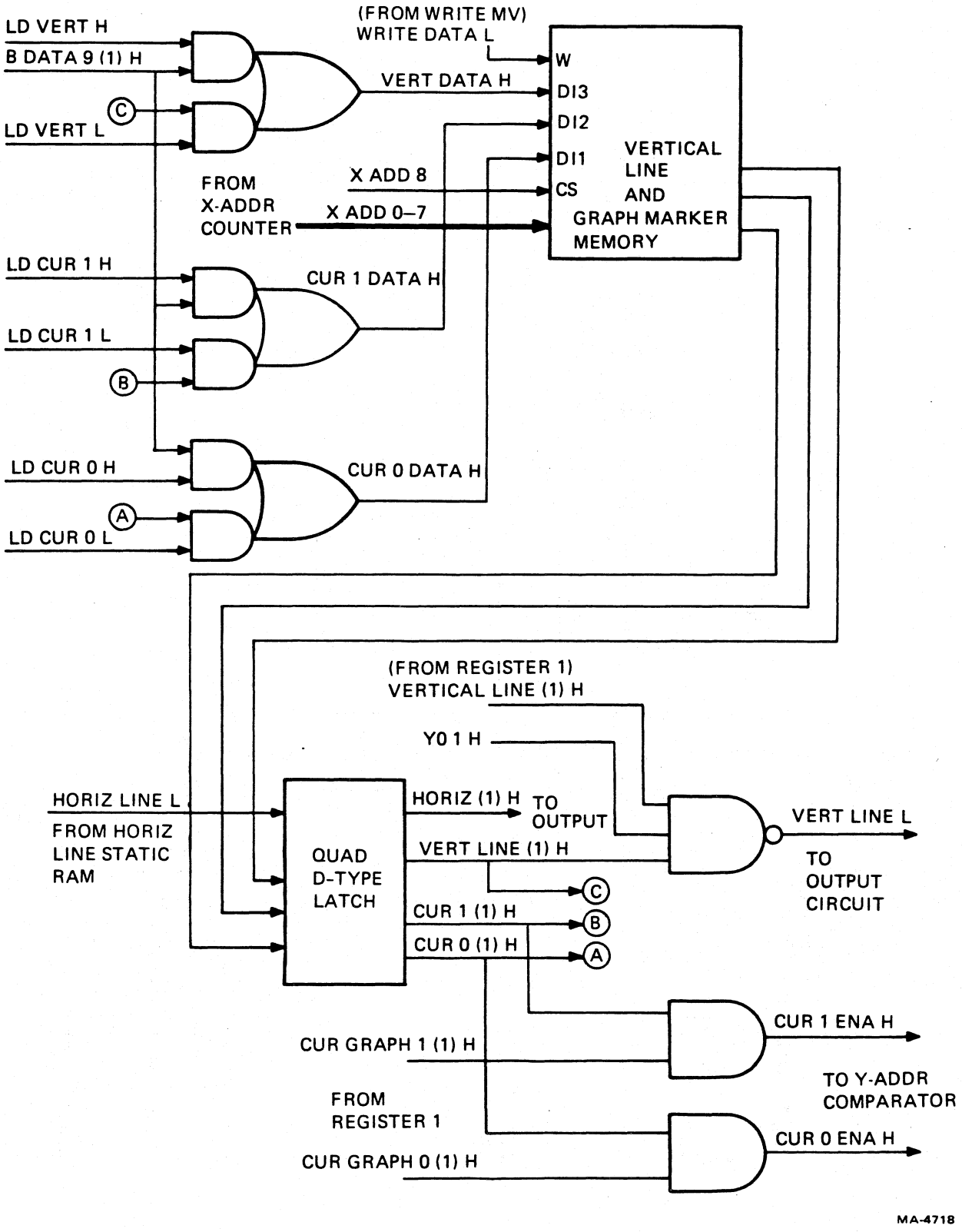


Figure 6-30 Vertical Line and Graph Marker Memory

6.4.1.13 Adding Graph Marker – The graph marker in the VT105 is a short vertical line that straddles the graph. For each graph marker, 16 additional dots on the screen are enhanced above and/or below the graph point. The number of dots above or below the graph point is hardware-dependent according to the current graph position. If the graph is at the top of the screen, the 16 dots are all below that of the graph point; if at the bottom, they are all above the graph point.

Loading a graph marker is accomplished by two data characters following the letters C or K. These letters are decoded as LD CUR 0 H and LD CUR 1 H, shown in Figure 6-30. When bit 4 of the second data character [B DATA 9 (1) H] is a one and WRITE DATA L is present, a graph marker is loaded in the address formed by the two data characters. If bit 4 is a zero, the graph marker is erased.

When the graph marker is enabled and read from memory, an equal condition is forced from the lower four bits of the Y-address comparator (Figure 6-31). The upper 4-bit comparator holds this equal condition until one of its bits changes. This does not happen until the Y-address has decremented 16 lines. The graph data point may be on any one of these 16 lines causing the graph marker to vary in number of dots above and below the graph point.

As the X-address is incremented, the output of the vertical line and graph marker memory is monitored by a D-type latch. As with the vertical line data, the graph marker data is also fed back into memory (items A and B in Figure 6-30) and wraps around when in strip chart mode.

6.4.1.14 Generating Horizontal Lines – A horizontal line is loaded with the character D. The two data characters following the D represent an 8-bit Y-position of a horizontal line. Data bit 4 in the second data character enables the signal DIS CLR + INIT H that allows the A inputs to the two-line to one-line multiplexer (Figure 6-32) to be gated out. The data, or address of the line, is then presented to the 256 × 1 static RAM memory. Data bit 4 [B DATA 9 (1) H] is also the data to be written into memory. If it is a one, a horizontal line is stored; if zero, a line is erased at that address.

A down-counter is used for tracking the Y-address when reading data from memory. To read from memory, only the Y-address is needed. A complement of the data in memory is the output. From register 1, HORIZ LINE (1) L enables all points at that Y-address creating a horizontal line. The signal 320 ns allows only every other dot to be displayed to decrease its intensity.

6.4.1.15 Generating Strip Charts – Strip charts are enabled by the second data character following a load enable register 0 instruction, as shown in Figure 6-33. Data bit 3 (DB 3 H) of this register enables the single strip chart feature; either Graph 0 or Graph 1 can be incremented from right to left across the screen.

Data bit 4 (DB 4 H) of this register enables the dual strip chart feature; both Graph 0 and Graph 1 data can be incremented from right to left across the screen. This must be done in the following sequence.

Data Entry	**Character(s) Transmitted**
Enable Graph 0	B
Enter Graph 0 data	Two data characters
Enable Graph 1	J
Enter Graph 1 data	Two data characters

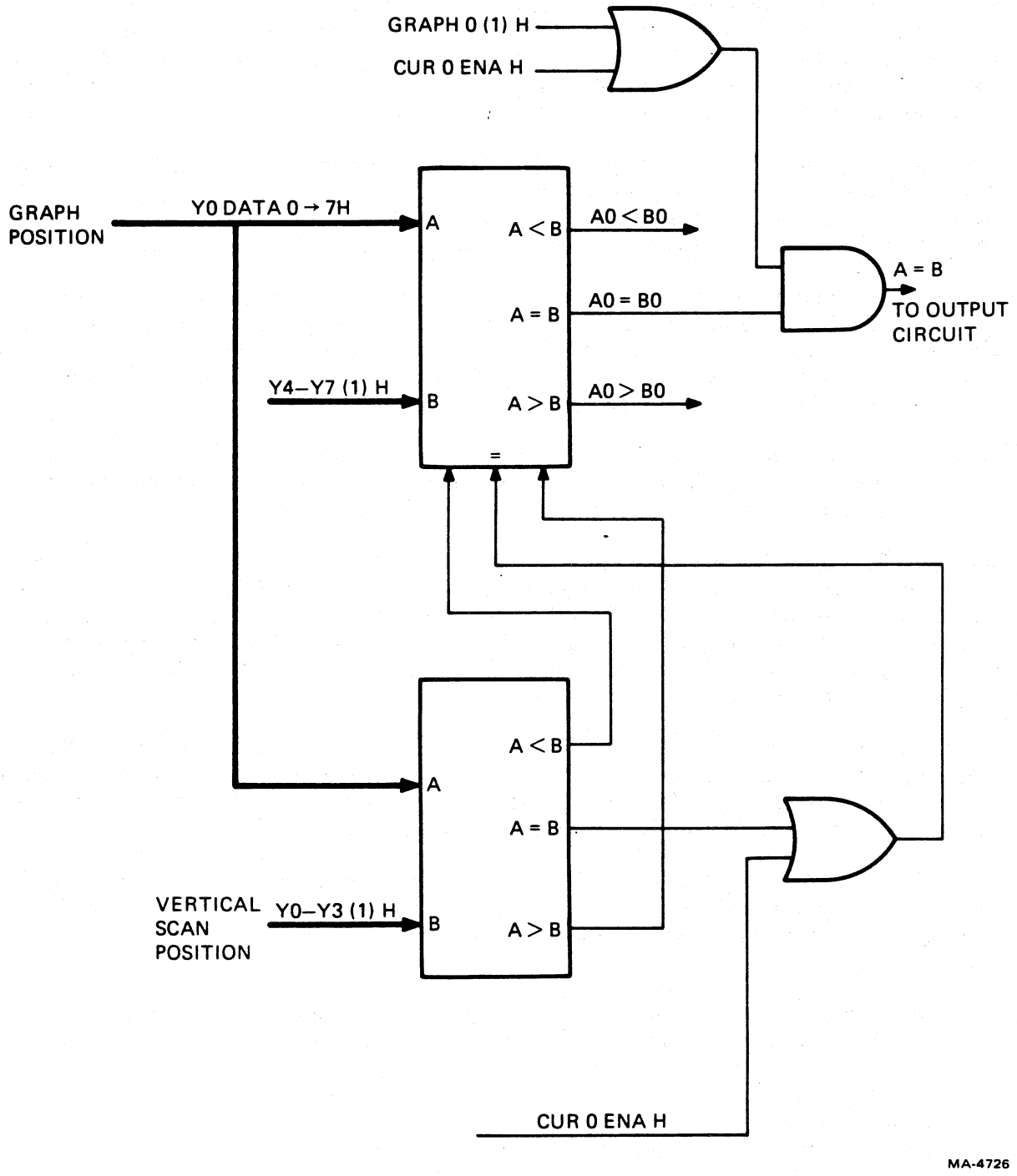


Figure 6-31 Graph Marker Y-Address Comparator

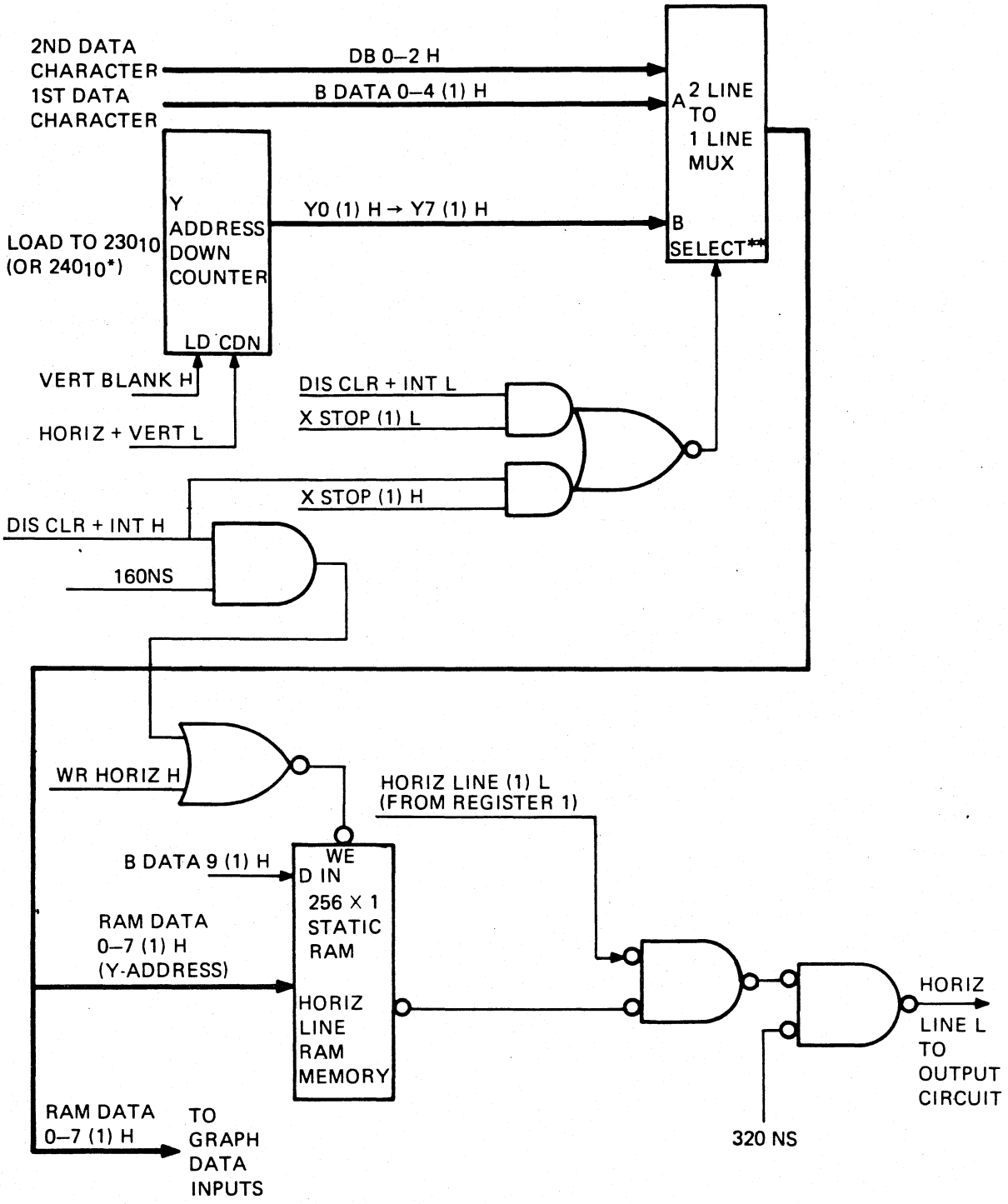


Figure 6-32 Horizontal Line Memory

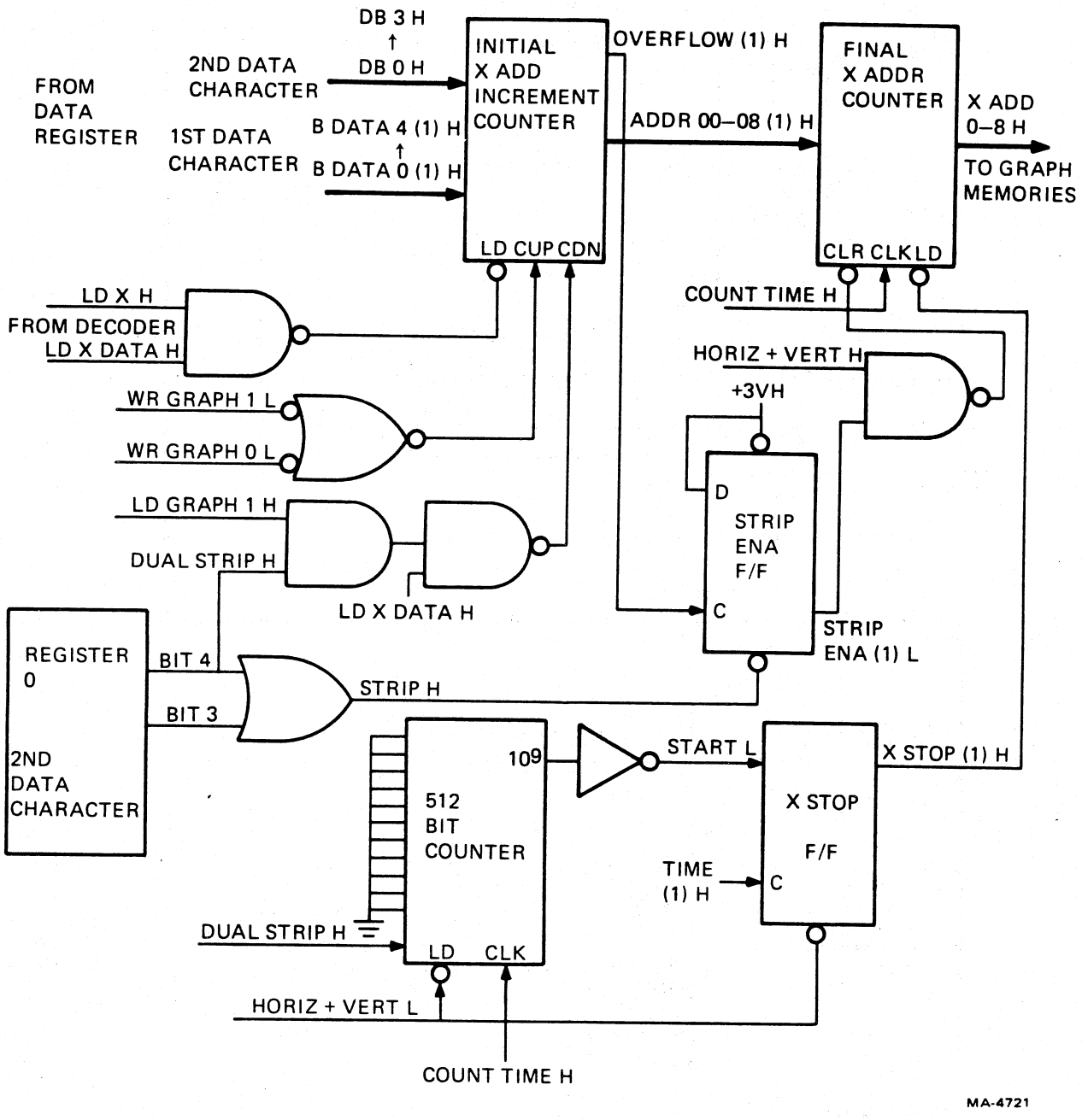


Figure 6-33 Generating Strip Charts

Single Strip Chart Operation – Two X-address counters are used to create the strip chart motion. Without the strip chart feature enabled, the final X-address counter is cleared to zero at horizontal blank time (by HORIZ + VERT H). With a strip chart enabled, this clear signal is disabled allowing the final X-address counter to follow the initial X-address counter counting in a wraparound manner.

Data is loaded into the graph as usual for addresses up to 511. At address 512, an overflow occurs in the initial X-address counter. OVERFLOW (1) H clocks the strip enable flip-flop disabling the clear signal to the final X-address counter.

A 512-bit counter monitors the horizontal scan position and enables the load signal for the final X-address counter only after completing the current line. New data increments the X-address and is added to the end of the graph. This new data is then the last data to be read from memory. Previous data is read one position earlier causing a shift in the video graph to the left.

When the strip chart is disabled, the final X-address counter is cleared at horizontal (or vertical) blank time regardless of its current count. This causes the displayed video graph to reposition itself as the counter is reset to zero.

Dual Strip Chart Operation – For dual strip chart operation, data bit 4 in register 0 must be set, creating the signal DUAL STRIP H. Data for both Graph 0 and Graph 1 must be placed at the same X-address and shifted simultaneously. Refer to the timing diagram (Figure 6-34) and the following sequence of events.

1. An instruction to load Graph 0 is received. WR GRAPH 0 L is placed on the count-up input to the initial X-address counter. The data is written into Graph 0. After 50 ns, WR GRAPH 0 times out, and the counter increments one address.

2. When the command to load Graph 1 is received, the Initial X-address counter counts down one address.

3. WR GRAPH 1 L is placed on the count-up input to the initial X-address counter. Data is written into Graph 1. After 50 ns, the initial X-address counter increments one address.

When the initial X-address counter is incremented, this new address is loaded into the final X-address counter at the end of the current graph line [as X STOP (1) H goes low]. The last data word entered in each graph is the last X-address read.

Incrementing the initial X-address counter, by adding a new data word to each graph, causes the final X-address counter to access that data last in both memories. This causes both graphs on the screen to shift simultaneously one unit to the left for each new set of data words.

The 512-bit counter that monitors the graph drawing field is initially loaded to a 1 in dual strip chart mode. A count of 512 is reached one count time earlier, eliminating the last bit position on the graph. This removes the switching motion that would be visible on the screen while alternately plotting data on Graph 0 and Graph 1.

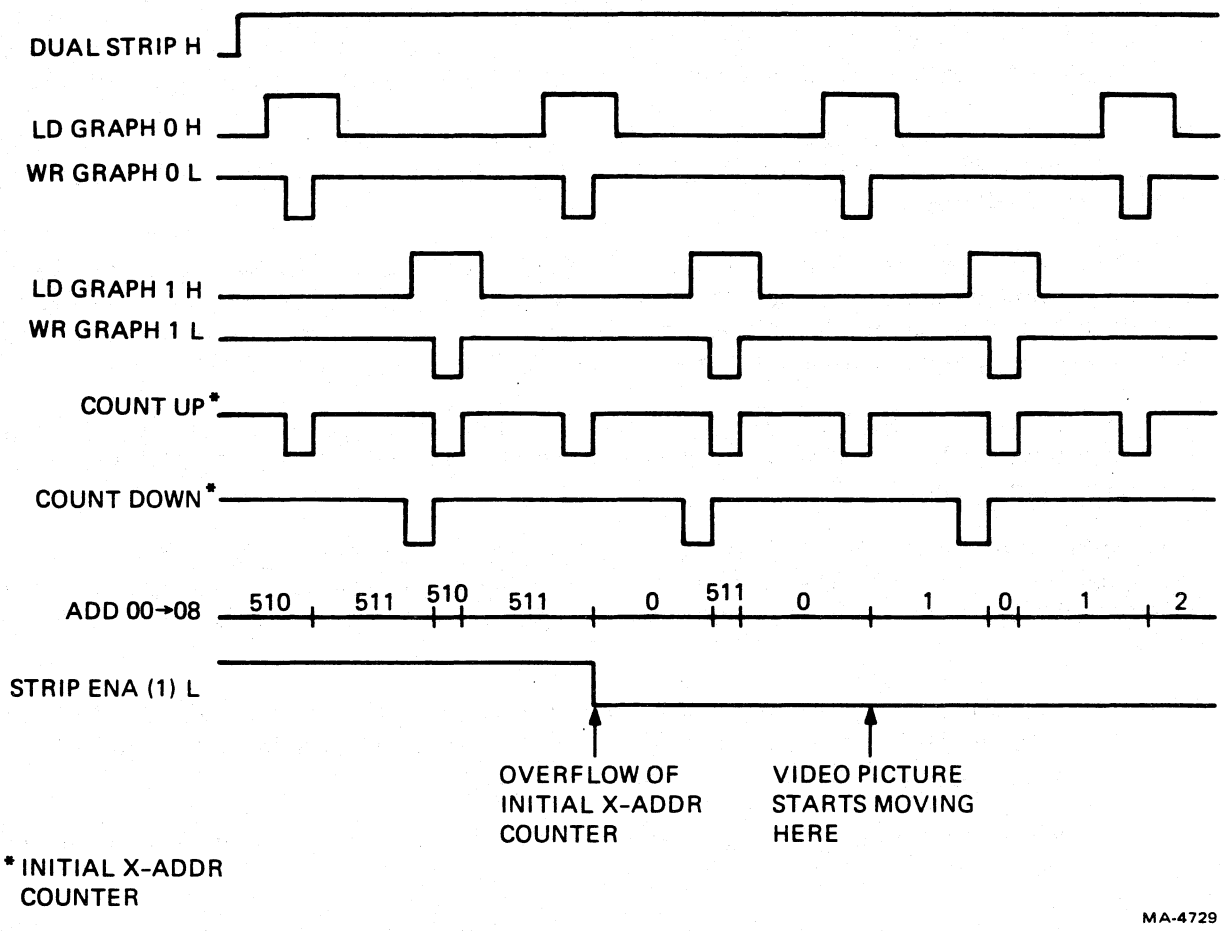


Figure 6-34 Dual Strip Chart Timing Diagram

6.4.1.16 Combining Video Out and Timing – All data signals generated within the M7071 are combined to form one video output to the VT100 terminal controller (Figure 6-35)

The timing signals are developed by the phase lock loop using HORIZ BLK L from the VT100 terminal controller. (See Paragraph 6.4.1.6.)

Graph 0 and Graph 1 data, horizontal lines, vertical lines, and Graph 0 and Graph 1 markers are presented to the video output every TIME (1) H. At COUNT TIME H the 512-bit horizontal counter clocks the window flip-flop to gate the data out.

Histogram 0 or Histogram 1 data is alternately enabled to the video output with TIME (0) H and TIME (1) H. This allows both shaded graphs to be discernible in areas on the screen where they overlap.

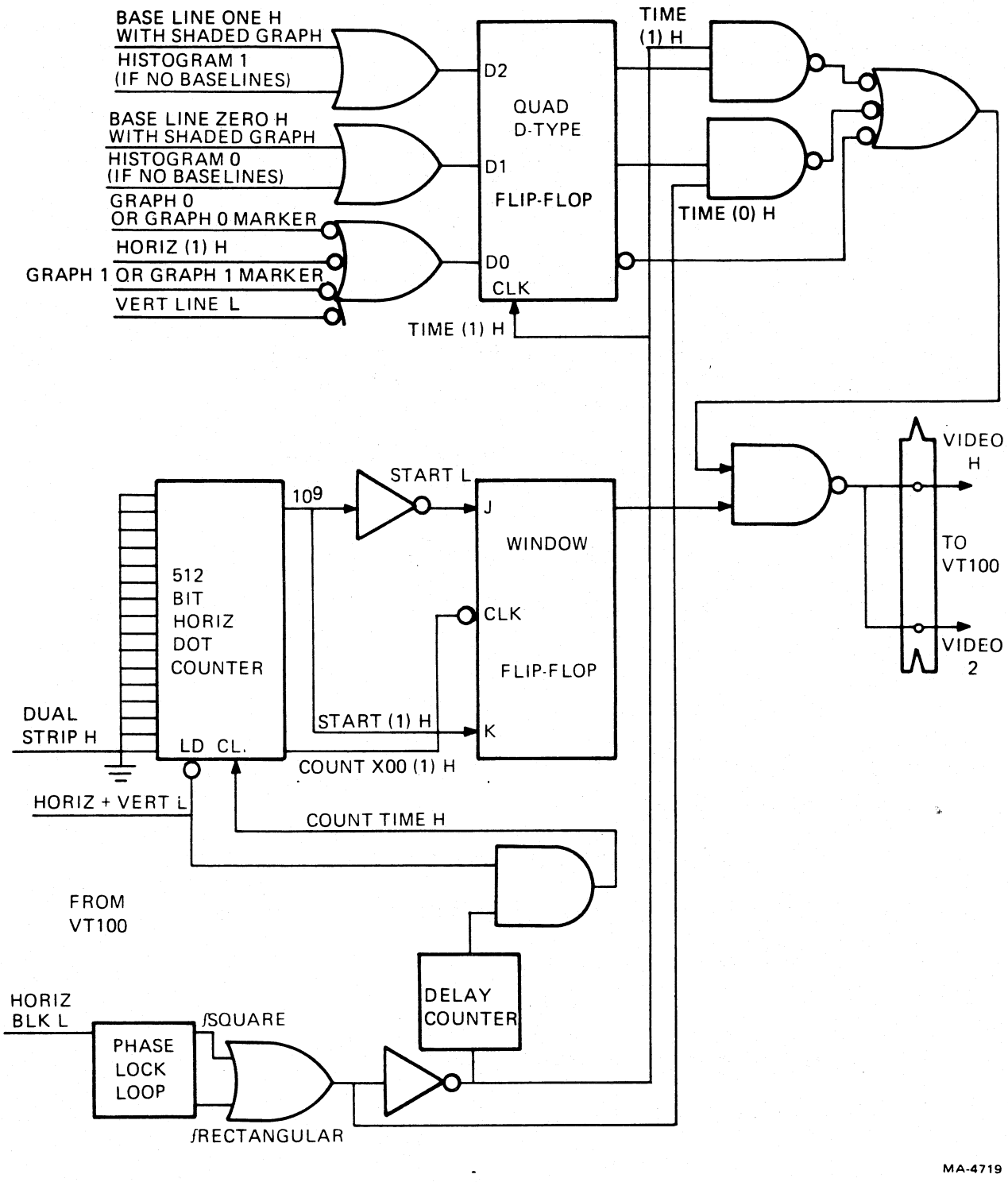


Figure 6-35 Combining Video Out

6.4.2 VT105 Graphic Test Procedure

The interactive test feature of the VT105 is a series of displayable test patterns. These patterns verify that all waveform generator features are operating correctly. Perform these data tests in the order indicated.

NOTE

The tests described in this procedure are run in the rectangular format. The tests may also be run in the square format, but the test patterns are slightly different.

Do not use the SPACE BAR unless the word <SPACE> is spelled out.

Remember to use the SHIFT key for uppercase symbols; the CAPS LOCK key is only used for uppercase letters.

If at any time the wrong character is entered, initialize the registers and memories by typing the following sequence.

A<SPACE><SPACE>I 0 I<SPACE> "

Then reenter the test data.

6.4.2.1 Test Setup

1. Place the terminal LOCAL.
2. Turn on the auto repeat feature (in SET-UP B group 1, switch 2 = 1).
3. Type the following sequence.

   <ESC>1 I<SPACE><SPACE> I<SPACE> "

6.4.2.2 Test Graph 0, Histogram 0, and Graph 0 Markers

1. Type the following sequence.

   A#

   The graph test pattern in Figure 6-36 is now on the screen.

2. Type the following sequence.

   A)

   The histogram test pattern in Figure 6-37 is now on the screen.

3. Type the following sequence.

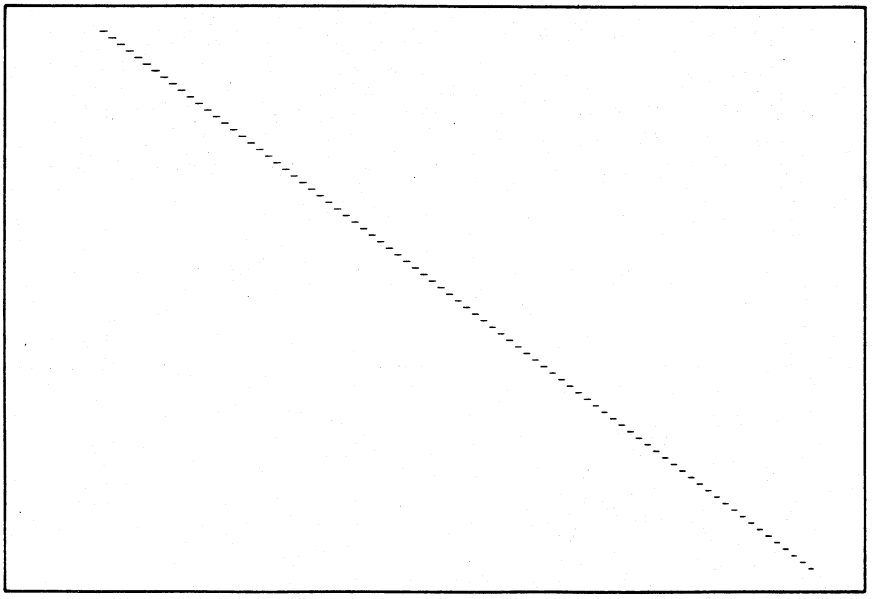
   I$

   The graph marker test pattern in Figure 6-38 is now on the screen.

4. Type the following sequence.

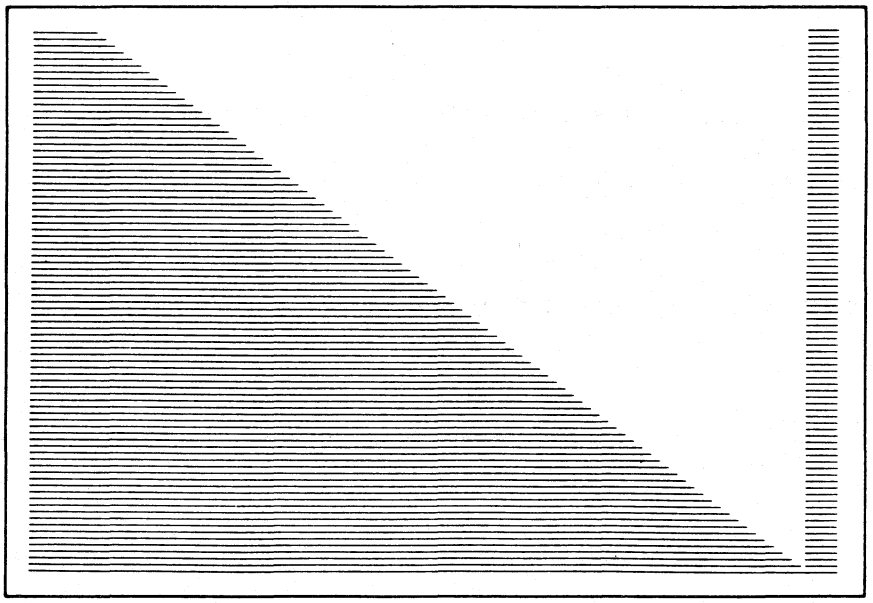
   I<SPACE> A<SPACE>

   The graph 0, histogram 0, and graph 0 markers are now disabled.



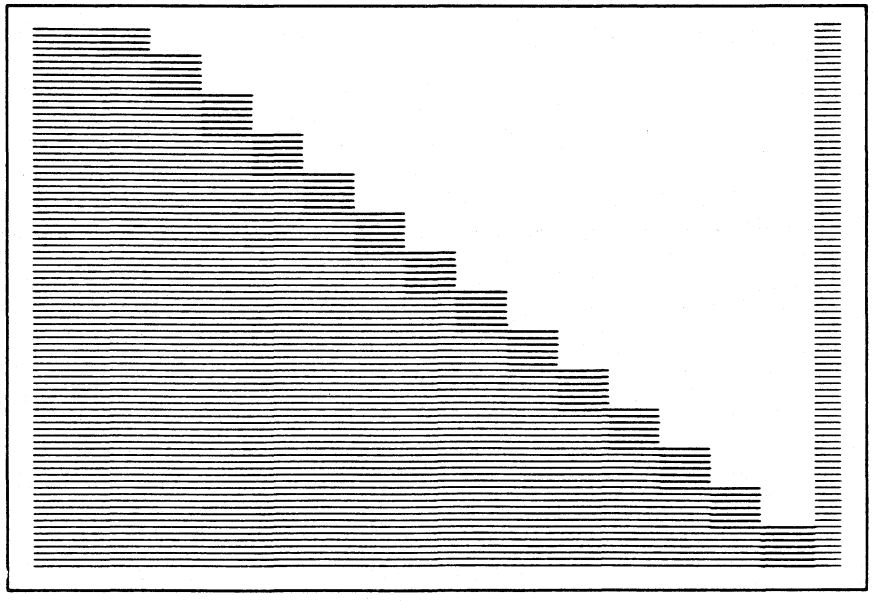
MA-4741

Figure 6-36 Graph Test Pattern



MA-4742

Figure 6-37 Histogram Test Pattern



MA-4743

Figure 6-38 Graph Marker Test Pattern

6.4.2.3 Test Graph 1, Histogram 1, and Graph 1 Markers

1. Type the following sequence.

   A%

   The graph test pattern in Figure 6-36 is now on the screen.

2. Type the following sequence.

   A1

   The histogram test pattern in Figure 6-37 is now on the screen.

3. Type the following sequence.

   I(

   The graph marker test pattern in Figure 6-38 is now on the screen.

4. Type the following sequence.

   I<SPACE> A<SPACE>

   The graph 1, histogram 1, and graph 1 markers are now disabled.

6.4.2.4 Test the Horizontal Lines

1. Type the following sequence.

   A!I!

   The horizontal line test pattern in Figure 6-39 is now on the screen. Note that the test pattern appears to be a series of vertical lines. This is the correct test pattern.

2. Type the following sequence.

   I<SPACE>

   The horizontal line test pattern is now disabled.

6.4.2.5 Test the Vertical Lines

1. Type the following sequence.

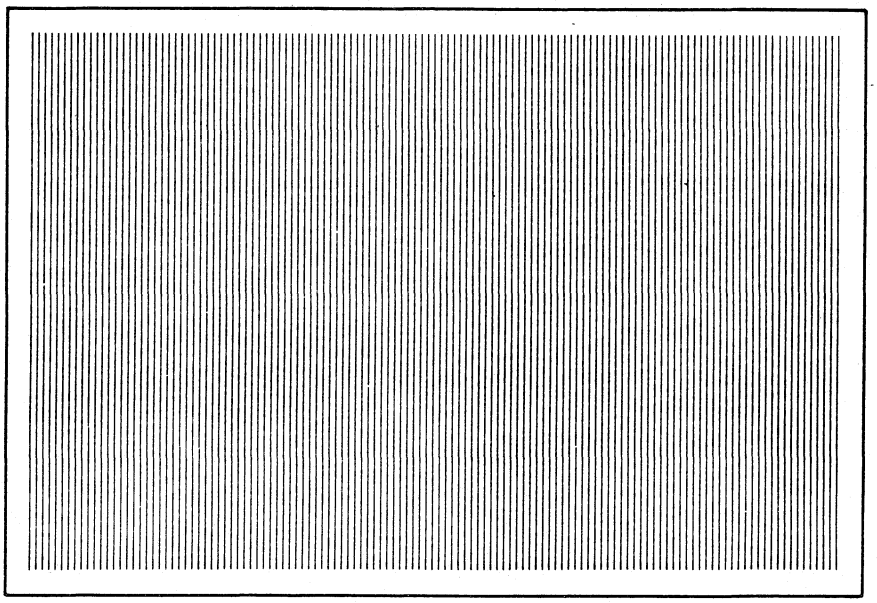
   A!I"

   The vertical line test pattern in Figure 6-40 is now on the screen. Note that the test pattern appears to be a series of horizontal lines. This is the correct test pattern.

2. Type the following sequence.

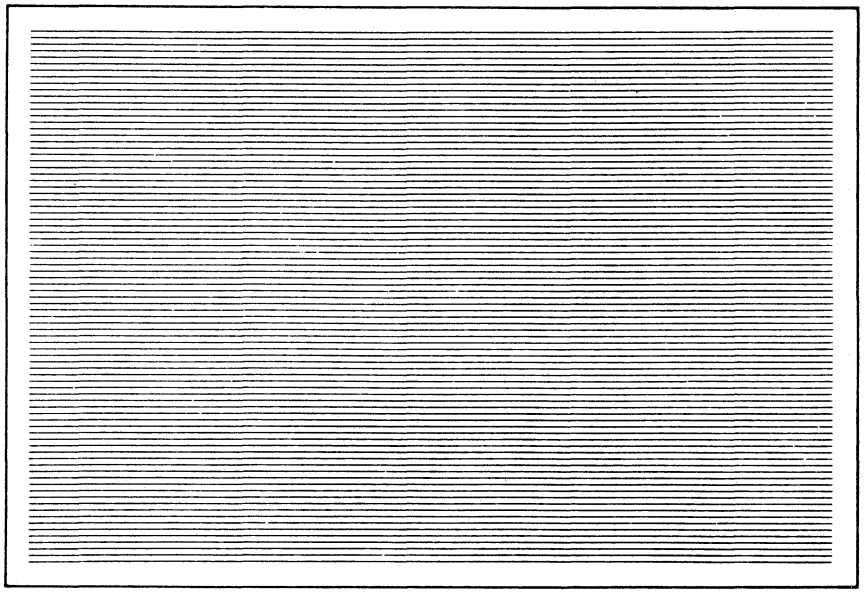
   I<SPACE>

   The vertical line test pattern is now disabled.



MA-4744

Figure 6-39 Horizontal Lines Test Pattern



MA-4745

Figure 6-40 Vertical Lines Test Pattern

6.4.2.6 Test Shade Line 0 (Baseline 0)

1. Type the following sequence.

   A#"

   The shade line test pattern in Figure 6-41 is now on the screen.

2. Type the following sequence.

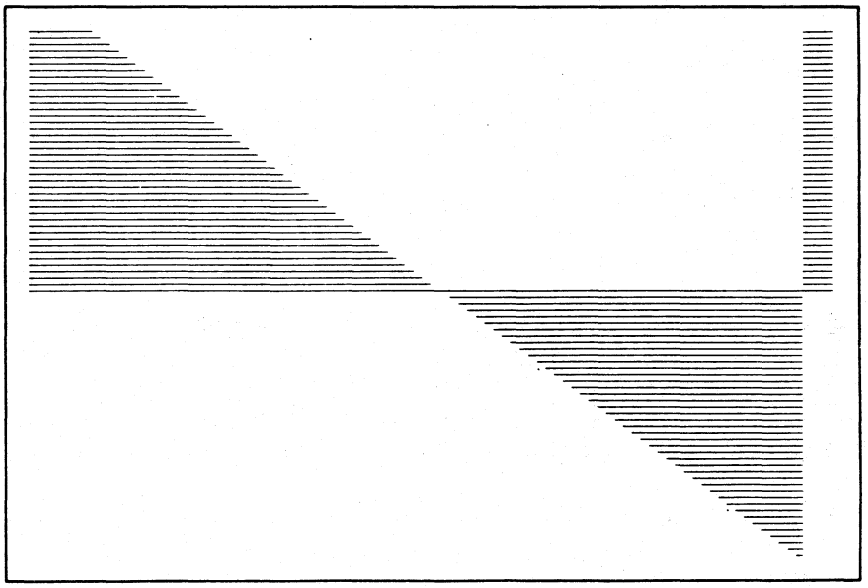
   @11 22 33 44 55 66 <SPACE><SPACE>

   The shade line shifts upward with each pair of numbers typed.

3. Type the following sequence.

   A<SPACE><SPACE>

   The shade line 0 test pattern is now disabled.



MA-4746

Figure 6-41 Shade Line (Baseline) Test Pattern

6.4.2.7 Test Shade Line 1 (Baseline 1)

1. Type the following sequence.

   A%%

   The shade line test pattern in Figure 6-41 is now on the screen.

2. Type the following sequence.

   @11 22 33 44 55 66 <SPACE><SPACE>

   The shade line shifts upward with each pair of numbers typed.

3. Type the following sequence.

   A<SPACE><SPACE>

   The shade line 1 test pattern is now disabled.

6.4.2.8 Test Strip Chart 0

1. Type the following sequence.

   I<SPACE>"A+(

   The histogram test pattern shown in Figure 6-37 is now on the screen.

2. Type the following sequence.

   H??B

   The strip chart test pattern shown in Figure 6-42 is now on the screen.

3. Type any sequence of two numbers. This moves the graph to the left. The SPACE BAR enters a 0 as in Figure 6-42, 11 enters data at line 49, 22 enters data at line 82, etc. Hold down the number key if in auto-repeat mode.

4. Type the following sequence.

   A<SPACE><SPACE>

   The strip chart test pattern is now disabled.

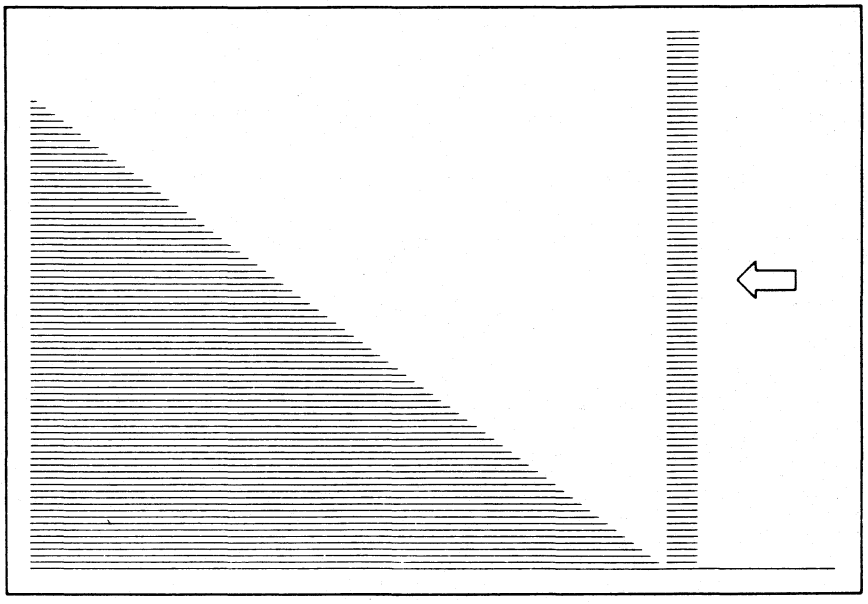


Figure 6-42 Strip Chart Test Pattern

6.4.2.9 Test Strip Chart 1

1. Type the following sequence.

   I< SPACE>"A5(

   The histogram test pattern in Figure 6-37 is now on the screen.

2. Type the following sequence.

   H??J

   The strip chart test pattern in Figure 6-42 is now on the screen.

3. Type any sequence of two numbers. This moves the graph. The SPACE BAR enters a 0 as in Figure 6-42, 11 enters data at line 49, 22 enters data at line 82, etc. Hold down the number key if in auto-repeat mode.

4. Type the following sequence.

   A<SPACE><SPACE>

   The strip chart test pattern is now disabled.

6.4.2.10 Exit the Graphic Test Mode

1. Type the following sequence.

   I0<SPACE> A<SPACE><SPACE> I<SPACE><SPACE><ESC>2

   The terminal is now in interactive mode.

6.5 VT1XX-AC PRINTER OPTION

The VT1XX-AC option provides an interface between a VT100/VT132 terminal and a serial printer.

6.5.1 Option Installation

Use the following procedure to install the VT1XX-AC option in a VT100/VT132 terminal.

1. Turn terminal power off and remove the terminal access cover (Paragraph 5.4.1).

2. Remove the terminal controller board (Paragraph 5.4.2).

3. If installed, remove the advanced video board (AVO) from the terminal controller board (Paragraph 5.4.3).

4. Reconfigure the VT100 terminal controller board. This consists of removing the ROMs 0, 1, 2, and 3 from the controller board, and replacing them with the ROMs shipped with the printer option. Figure 5-32 shows the ROM locations on the terminal controller board. The VT132 does not use the ROMS sent with the printer option kit. Table 5-7 lists the ROMs used in each product.

NOTE

If the terminal controller board ever fails, remove the printer port ROMs. Then, move the ROMs that come with the replacement terminal controller board to the defective board before returning it for repair.

5. Reconfigure the advanced video board (AVO). This consists of removing any ROMs mounted on the board and replacing them with the ROMs shipped with the printer option. Also check, and change if necessary, the jumpers or switches on the AVO board. Figures 5-33 and 5-34 show the new ROMs installed on the AVO board. Tables 5-8 and 5-9 show the correct switch positions and jumper locations for the AVO board. Table 5-7 lists the ROMs used in each product.

NOTE

Do not discard the ROMs removed in step 6 until after the terminal and option have been successfully tested. If the AVO board ever fails, remove all ROMs from the board before the board is returned for repair.

6. Install the AVO board on the terminal controller board (Paragraph 5.4.3).

7. Install the printer interface option board in the STP connector, J3, of the terminal controller board (Paragraph 5.4.5).

8. Reinstall the terminal controller board in the terminal.

9. If installed, remove the 20 mA current loop option board and connector from the access cover. Reinstall the option board and connector in the new access cover shipped with the printer option (Paragraph 5.4.8).

NOTE

Discard the old access cover after the terminal and printer option have been successfully tested.

10. Attach the option designation label to the rear of the terminal. Attach the new SET-UP label to the bottom of the keyboard. If the terminal is a VT132, transfer the SET-UP settings to the existing label.

11. Reconnect all cables you removed from the rear of the terminal in step 1.

12. Perform the printer option checkout procedure.

6.5.2 Printer Port Option Checkout Procedure

Two different test programs check out the printer interface; the power-up and the printer interface data loopback test.

NOTE

The terminal will fail the NVR section of the power-up test (error code 2) when first powered up after the printer option is installed. Correct the condition by performing a save operation on the current contents of the NVR.

6.5.2.1 Power-Up Test – You can start the power-up test in any of the following ways.

- Turn the terminal power switch on
- Reset the terminal in SET-UP mode
- Type the following sequence in LOCAL.

  <ESC>[2;1y

The terminal displays Wait while executing the test. When successfully completed, the screen clears.

NOTE

The continuously running test ends only if it finds an error, or you turn off power. The VT1XX-AC is not tested during a continuous test.

The error indications for this test are as follows.

- Lighted keyboard indicator (other than ON LINE or LOCAL)
- Character displayed on screen under the blinking cursor
- Unlighted VT1XX-AC indicator (located on the printer interface board)

Table 6-2 shows the keyboard indicator error codes and their meanings.

Table 6-3 shows the error character displayed on the screen under the blinking cursor. Any errors detected by the test appear on the terminal screen as a character in the upper-left corner.

NOTE

If character 4 appears, check that the keyboard is plugged in.

Table 6-2 Keyboard Indicator Error Codes

Error	L1	L2	L3	L4
ROM 0 checksum	Off	Off	Off	On
ROM 1 checksum	Off	Off	On	Off
ROM 2 checksum	Off	Off	On	On
ROM 3 checksum	Off	On	Off	Off
Main data RAM	Off	On	Off	On

Table 6-3 Displayed Error Codes

Character	Fault Detected AVO	NVR	KBD	DATA
1	X	–	–	–
2	–	X	–	–
3	X	X	–	–
4	–	–	X	–
5	X	–	X	–
6	–	X	X	–
7	X	X	X	–
8	–	–	–	X
9	X	–	–	X
:	–	X	–	X
;	X	X	–	X
<	–	–	X	X
=	X	–	X	X
>	–	X	X	X
?	X	X	X	X

6.5.2.2 Printer Interface Data Loopback Test – Use the following procedure to perform the printer interface data loopback test.

1. Turn the power switch off. Install the data loopback connector (PN 12-15336) onto the printer interface connector (the upper EIA connector). The data loopback connector is also used to perform the EIA communication interface data loopback test.

2. Turn the power switch on. The terminal performs the power-up test.

3. Enter SET-UP B and place the terminal in the ANSI-compatible mode (group 2 switch 3 = 1). Perform a save operation.

4. Place the terminal in printer port test mode (SET-UP B group 5 switch 4 = 1).

5. Enter SET-UP C. Select the proper printer transmit/receive speed. Use either the **7** or **8** key on the main keyboard to select the speed.

6. Place the terminal ON-LINE and exit SET-UP mode. The screen now displays: PRINTER PORT TEST MODE

7. Type one of the following sequences.

   <ESC>[2;2y (single pass test)

   or

   <ESC>[2;10y (continuously running test)

NOTE

The continuously running test ends only if it finds an error, or you turn off power.

Any error detected by the test appears on the terminal screen as a character in the upper-left corner. Table 6-3 shows the possible error codes. A printer interface data loopback test error is shown by an X in the Data column.

6.6 VT1XX-CB, -CL KIT

The VT1XX-CB, -CL kit includes all the parts needed to install a VT125 Graphics Processor in a VT100 or VT105. This section explains the procedure.

NOTE

Before installing the graphics processor, check the ROMs and the etch revision level on the terminal controller board (step 3 of this procedure). Compare the numbers of the ROMs on the board with the numbers in Figure 6-43. They should be equal or larger.

Check the etch number on the solder side of the board. Look for the number 5013008 followed by a letter. If the letter is D, E, etc., you can use the board. If the letter is A, B, or C, you cannot use the board. Use the EIA line filter connector (included in kit) with a Revision F board.

If the board does not meet either of these prerequisites, consult your Field Service branch office.

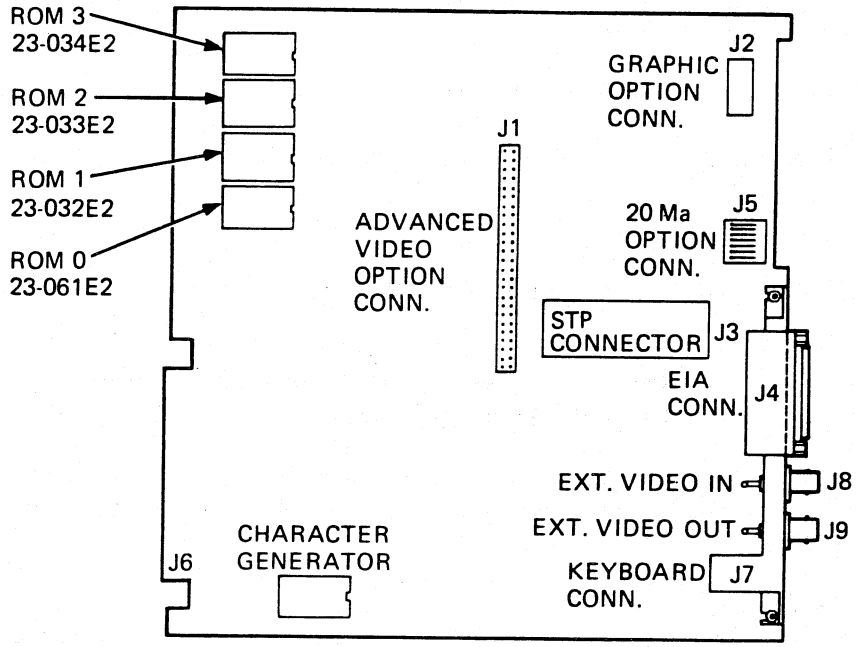


Figure 6-43 Check ROM Numbers

6.6.1 Installation

You need the following tools to install the VT125 graphics processor.

- 1/4-inch nutdriver
- 2 Phillips screwdrivers
- Needlenose pliers
- 3/16-inch blade screwdriver

Use the following procedure to install the VT125 graphics processor in a VT100 or VT105.

1. Turn off power and remove the access cover (Paragraph 5.4.1).
2. Remove the top and bottom covers (Paragraphs 5.4.14 and 5.4.15).
3. Remove the terminal controller board (Paragraph 5.4.2).

4. *For a VT100:* Remove the terminal controller edge connector by performing one of the following two steps.

   a. Release the two retaining rings from the edge connector with needlenose pliers.

   b. Lift the clips at the top and bottom of the edge connector and discard.

   For a VT105 or VT125: Disconnect the power cable from the VT105/VT125 expansion backplane, and remove the backplane (Paragraph 5.4.23).

5. The new expansion backplane has two capacitors on it, and its terminal controller edge connector has an alignment key in it. Remove this key with needlenose pliers unless installing the option in a terminal with a Revision F or higher terminal controller board. Install the new expansion backplane with four 12.7 mm (1/2 in) × 4-40 screws and kep nuts and four 6.4 mm (1/4 in) spacers. Install the screws at the connector positions marked J1 and J5 on the board (Figure 6-44). The dc power cable must be flat against the chassis or the backplane will not fit.

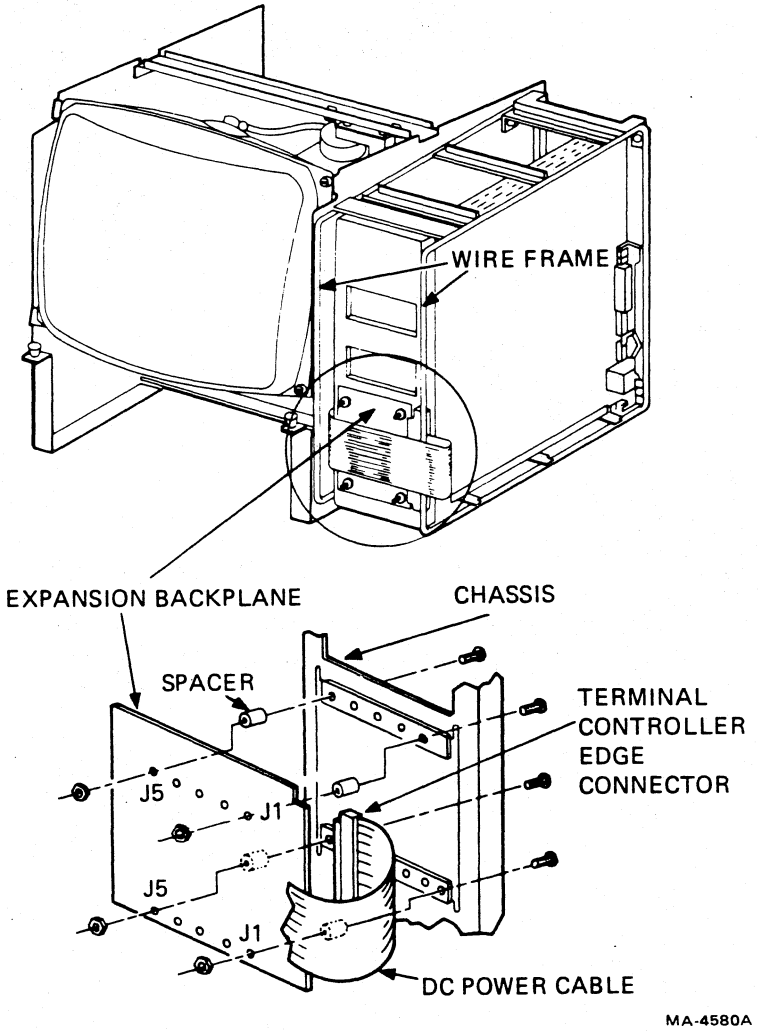
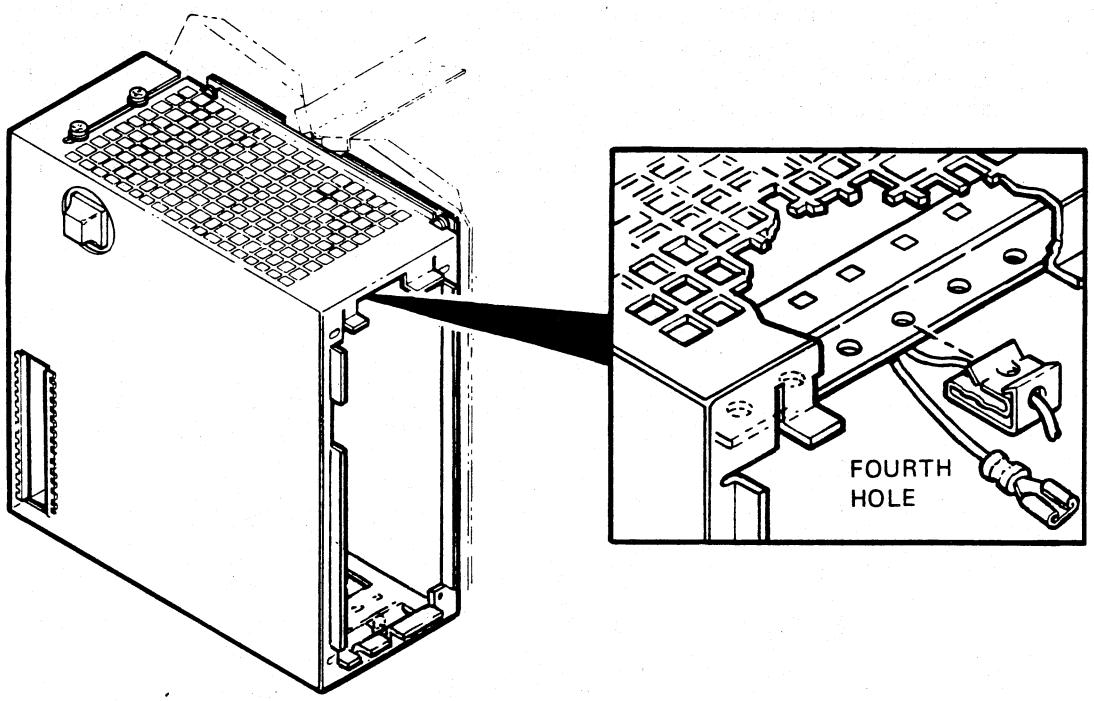


Figure 6-44 Installing Expansion Backplane

6. Bend the dc power cable around so the opening faces the CRT. Use needlenose pliers to remove the alignment key (if installed) from the connector opening in the dc power cable. Install the connector onto the board edge connector, passing the cable around the wire frame (if present).

7. Install card guides into the top and bottom of the card cage at the VT125 connector position.

8. At the fourth hole from the left on top of the chassis (over the BNC bracket), press the ground clip with a wire onto the chassis (Figure 6-45).



NOTE:
INSTALL CLIP BEFORE
INSTALLING SHIELD.

MA-9460A

Figure 6-45 Installing Ground Clip

9. Install the FCC RF shield (Paragraph 5.4.21).

10. Put the chassis into the bottom and top covers (Paragraphs 5.4.14 and 5.4.19).

11. Slide the terminal controller board partially into the chassis.

12. Install the VT100 end of the 16-pin flat cable connector to the lower 16 pins of the terminal controller board's graphics connector (marked J2 on the terminal controller board), with the cable entering from the right (Figure 6-46).

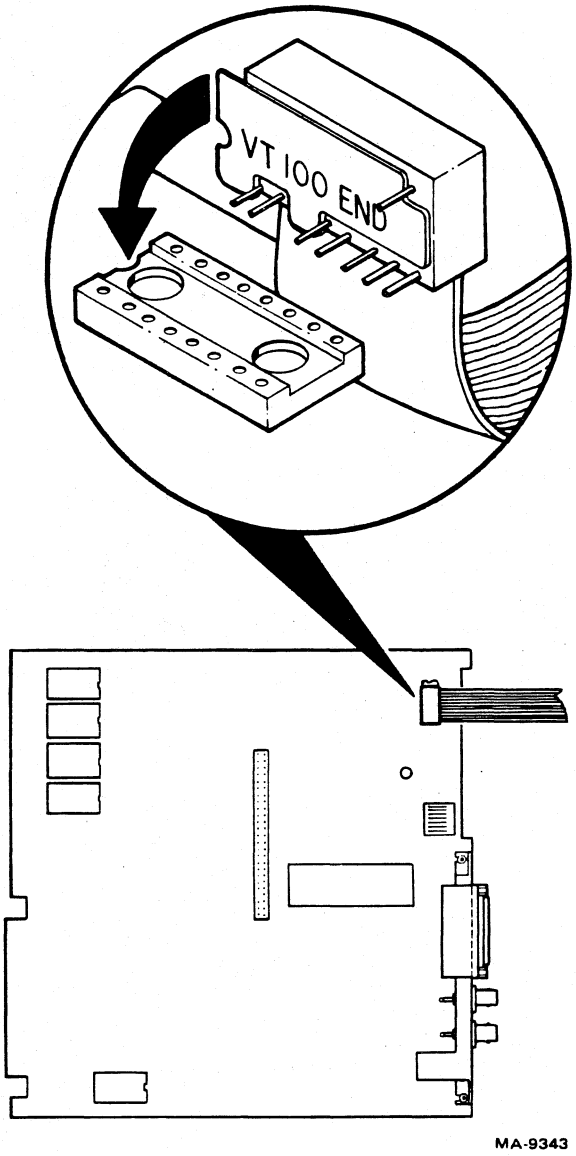


Figure 6-46 16-Pin Flat Cable on Terminal Controller

13. Install the STP paddle board in the STP connector. Lift the 16-pin cable slightly if needed to clear the spacer when inserting the STP board. Attach the STP board to the terminal controller board with the supplied screw and washer (Figure 6-47).

14. Find the end of the 24-pin cable that has pin 1 on the cable side. Fold the cable under itself to the right approximately 30 mm (1 in) from the connector. Install that end into the socket on the STP board with the cable down (Figure 6-48).

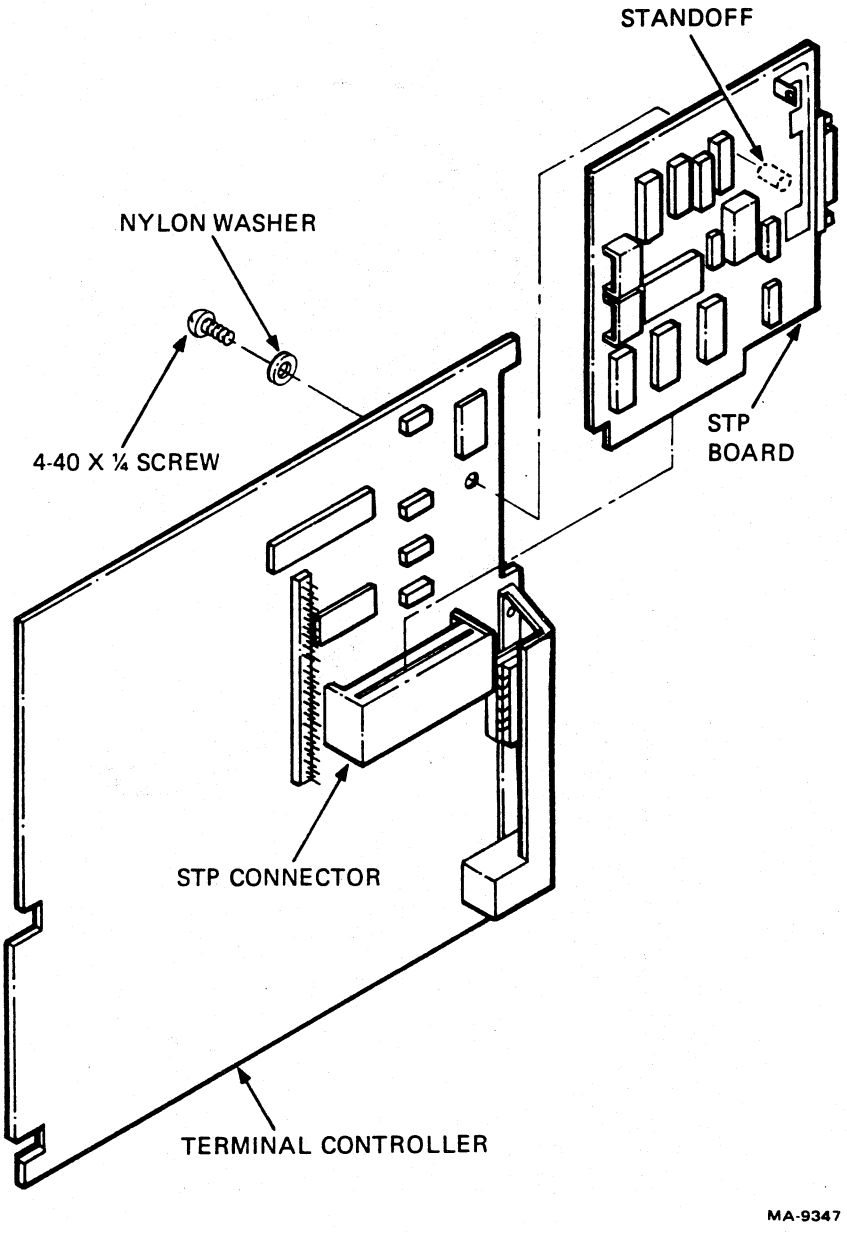


Figure 6-47 Installing STP Board

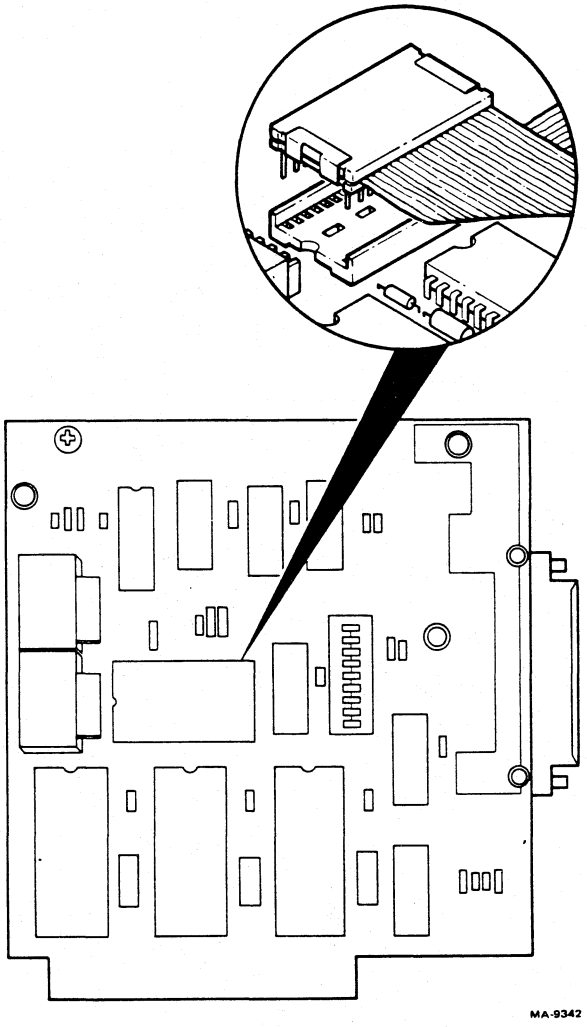


Figure 6-48 24-Pin Flat Cable on STP Board

15. Install the VT125 board into the chassis so that it sticks out approximately 5 cm (2 in) more than the terminal controller board.

16. Arrange the 16-pin graphics connector with the cable entering from above and install it into the connector at the top edge of the VT125 board (Figure 6-49).

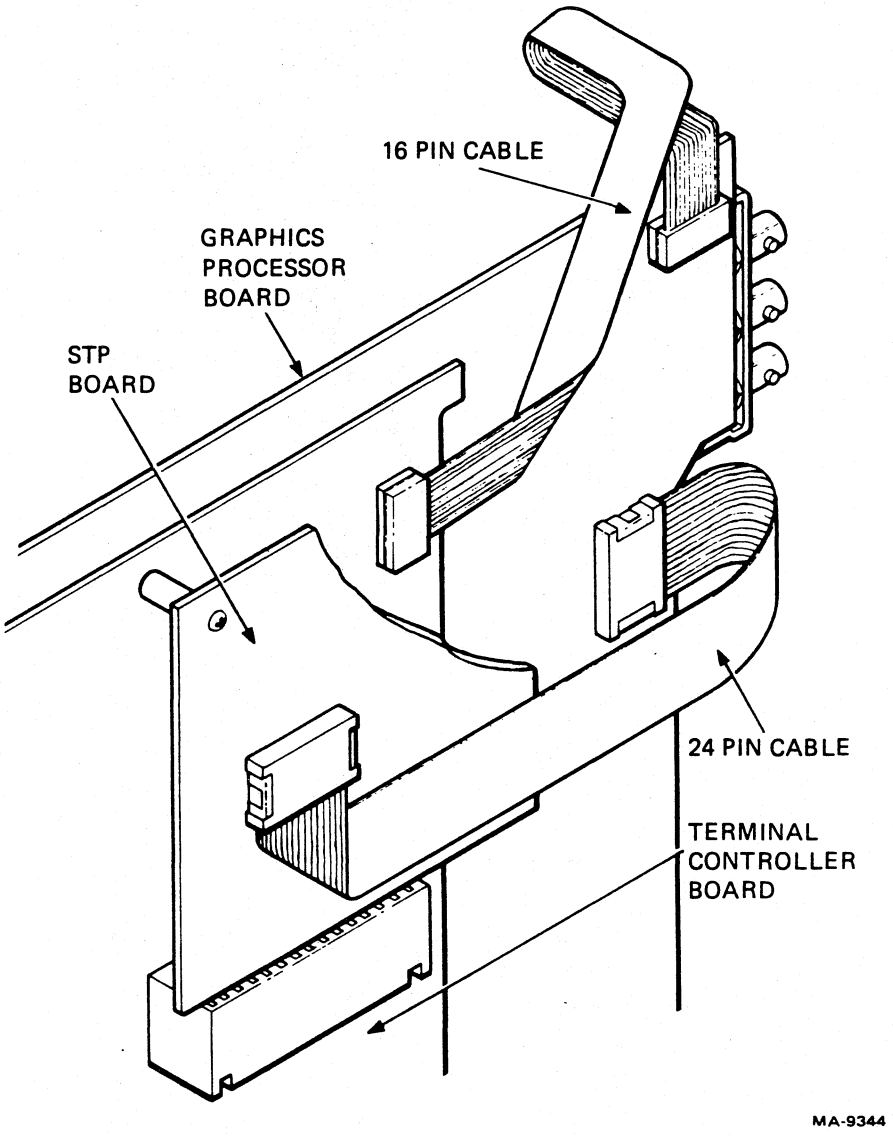


Figure 6-49 Graphic Cable Connections

17. Arrange the 24-pin connector with the cable entering from the right and install it into the 24-pin socket at the right edge of the VT125 board (Figure 6-49).

18. Check the switches on the STP board and set switches 1, 3, and 4 off, with all the other switches on (Figure 6-50).

19. Connect the ground wire from the top of the chassis to the quick-connect terminal on the BNC connector bracket (Figure 6-51).

20. Slide both boards into the chassis together, taking care not to stretch the cables. Seat both boards in their sockets one at a time.

21. If the 20 mA adapter is installed on the VT100, remove the adapter board from the VT100 access cover and install it into the new access cover. (Refer to Paragraph 6.3.1.)

22. Install the 20 mA connector cable (if present) to the red connector on the terminal controller board.

23. Adjust the cables in the access opening and install the access cover. Tighten the four screws carefully.

24. If using the EIA interface on a Revision F etch board, make sure to install the EIA line filter connector (Figure 6-51A).

25. Attach the new SET-UP label to the bottom of the keyboard.

6.6.2 Graphics Option Checkout Procedure

Perform the test procedures described in Paragraph 5.2.8. If you have display problems at power-up, recheck the flat cables for correct positions. Refer to Figures 6-45, 6-47, and 6-48.

NOTE

The terminal will fail its power-up test with a 2 indication the first time you turn it on after installing the option. Check the SET-UP features and save them by typing SHIFT/S in SET-UP.

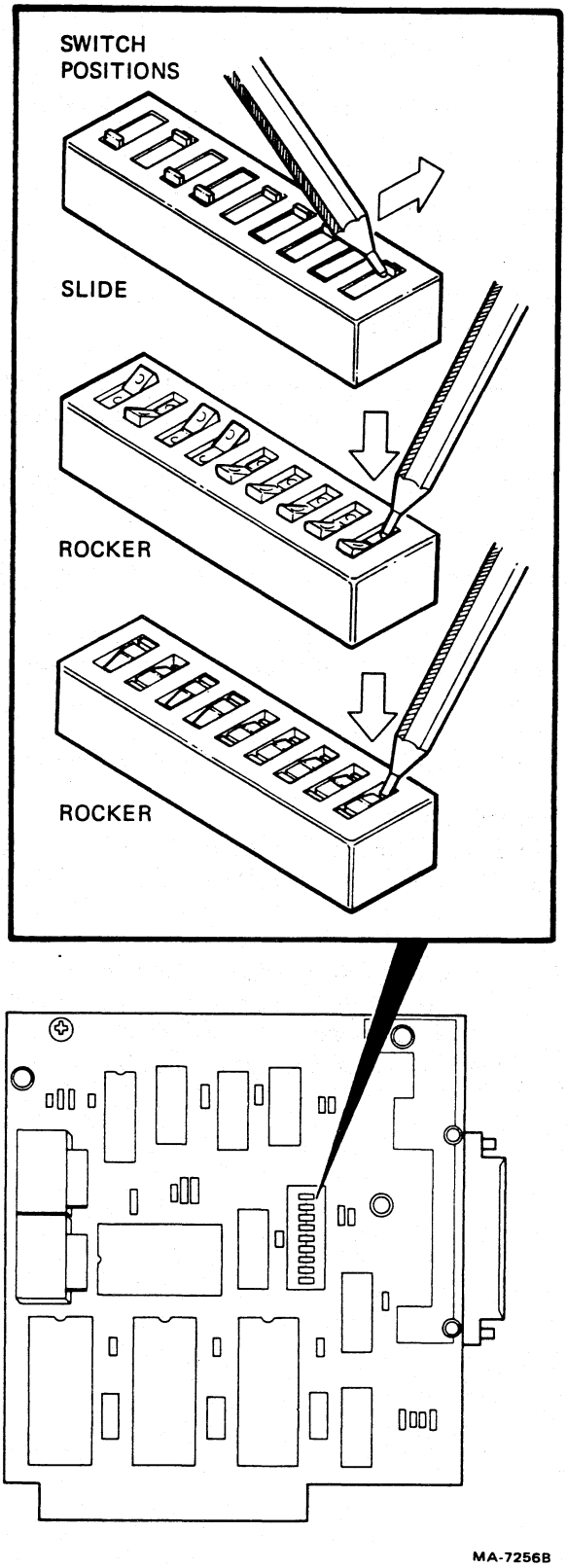


Figure 6-50 STP Board Switch Types

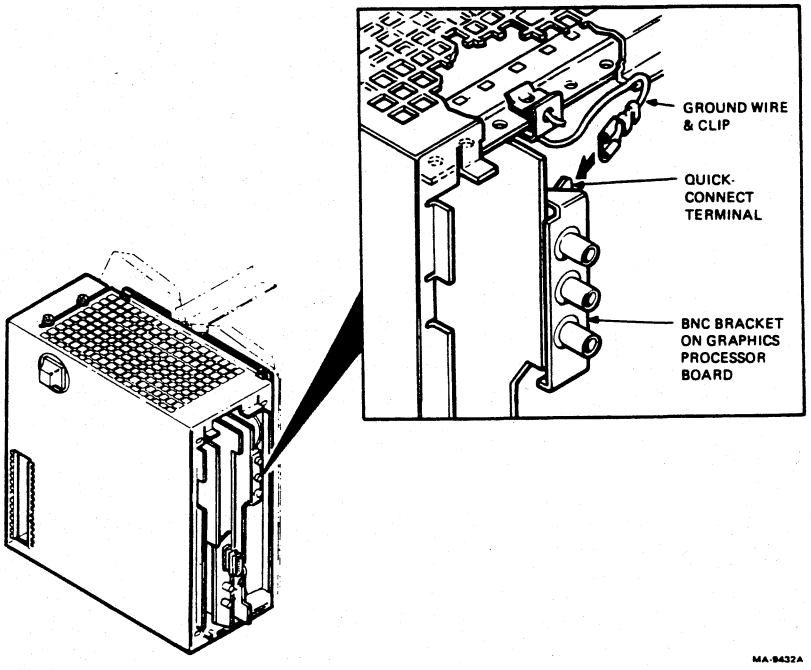


Figure 6-51 Connecting BNC Bracket Ground Wire

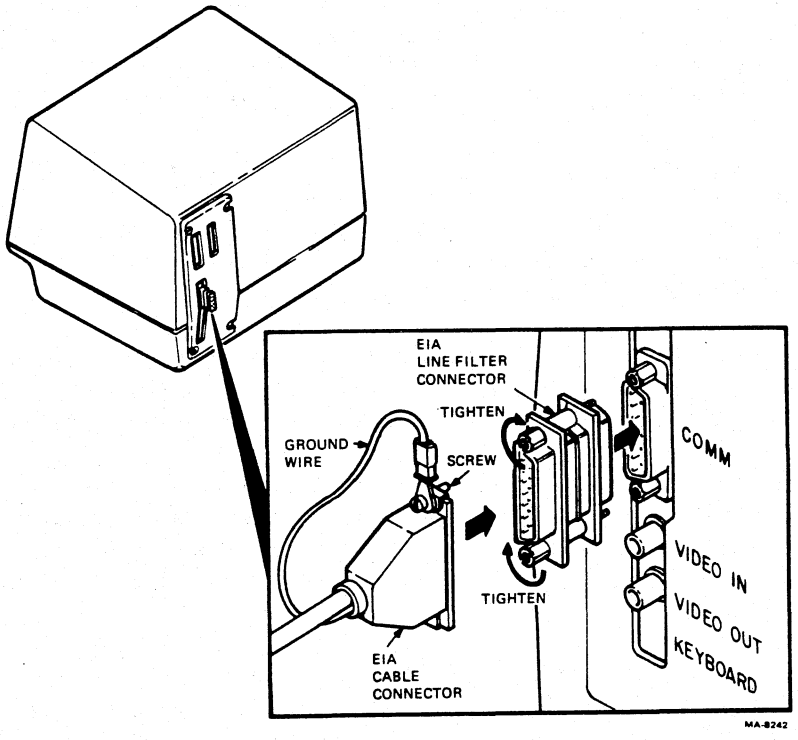


Figure 6-51A EIA Line Filter Connector

6.7 VT125 GRAPHICS PROCESSOR TECHNICAL DESCRIPTION

The VT125 is a graphics display terminal with medium resolution graphics for business and scientific applications. The VT125 combines bit map architecture with the alphanumeric capability of the VT100 video terminal. The VT125 is a smart terminal that directly executes DIGITAL's general-purpose graphics descriptor, ReGIS (Remote Graphics Instruction Set). ReGIS lets you create and store pictures as ASCII text and efficiently send those pictures to remote displays. The VT125 also has an auxiliary data port for making hard copies of the display with the DECwriter IV Graphics Printer. For users who have VT105 programs, the VT125 includes a VT105 emulator.

The VT125 is a VT100 video text terminal and a graphics processor in one package. The graphics processor processes graphics commands from a computer to generate an image in its own memory. Then it sends a video representation of that image to the VT100 text terminal's internal monitor screen and to an optional external color monitor. It can also send a bit map representation of the image to a graphics printer. If the VT125 receives data that is not graphics commands or other commands to the graphics processor, the graphics processor sends the data to the VT100 for processing and display as text or VT100 control functions.

The VT125 graphics processor is also available as an option that uses the VT100 chassis, power supply, and display to add graphics to a VT100.

The VT100 is described in detail in Chapter 4. This chapter is a detailed description of the graphics processor and its interface to the VT100. This chapter has two sections: an overview description that explains the parts of a block diagram, and a detailed description that uses detailed diagrams and the *VT125 Field Maintenance Print Set.*

6.7.1 Block Diagram Description

The VT125 graphics processor (Figure 6-52) is a bit map graphics display system. The system has a bit map memory and devices for writing and reading data in memory. The system writes into the bit map under control of the graphics descriptor ReGIS. (See the *VT125 User Guide.*) The system reads data out of the bit map under the timing control of the VT100 terminal, for display on the VT100 screen or an external color monitor. The next paragraphs describe the parts of the system.

The *bit map* is at the center of the block diagram. The bit map memory has one data storage address for each pixel on the display screen. The number of addresses available controls the resolution of the bit map. A collection of addresses with one bit at each address is called a plane. The bit map in the VT125 has two bits of memory at each address, so it has two planes. This lets the VT125 display up to four colors or intensities at one time. See the *VT125 User Guide* for more details.

The *8085 microprocessor* (lower right) controls most of the graphics processor. This microprocessor has a read only memory (ROM) for its instructions and dynamic read-write memory for its operations. It connects to the graphics processor and to other systems, through its input/output bus (I/O BUS).

The *STP board* is part of the graphics processor option, but it plugs into the STP connector on the VT100 terminal controller board. It connects to the graphics processor board (mono board) via a 24-wire cable. The STP board connects the graphics processor to the serial data path between the VT100 text terminal and the external host computer. The board also has the serial interface for the auxiliary port, often used with a graphics printer.

The graphics processor also connects to the VT100 terminal controller board via a 16-wire cable through the graphics connector. This connector brings the graphics processor's monochrome video output to the VT100 for display on the VT100's screen. The graphics connector also brings the VT100 display timing signals to the graphics processor to synchronize the two devices so their outputs can appear on the same screen.

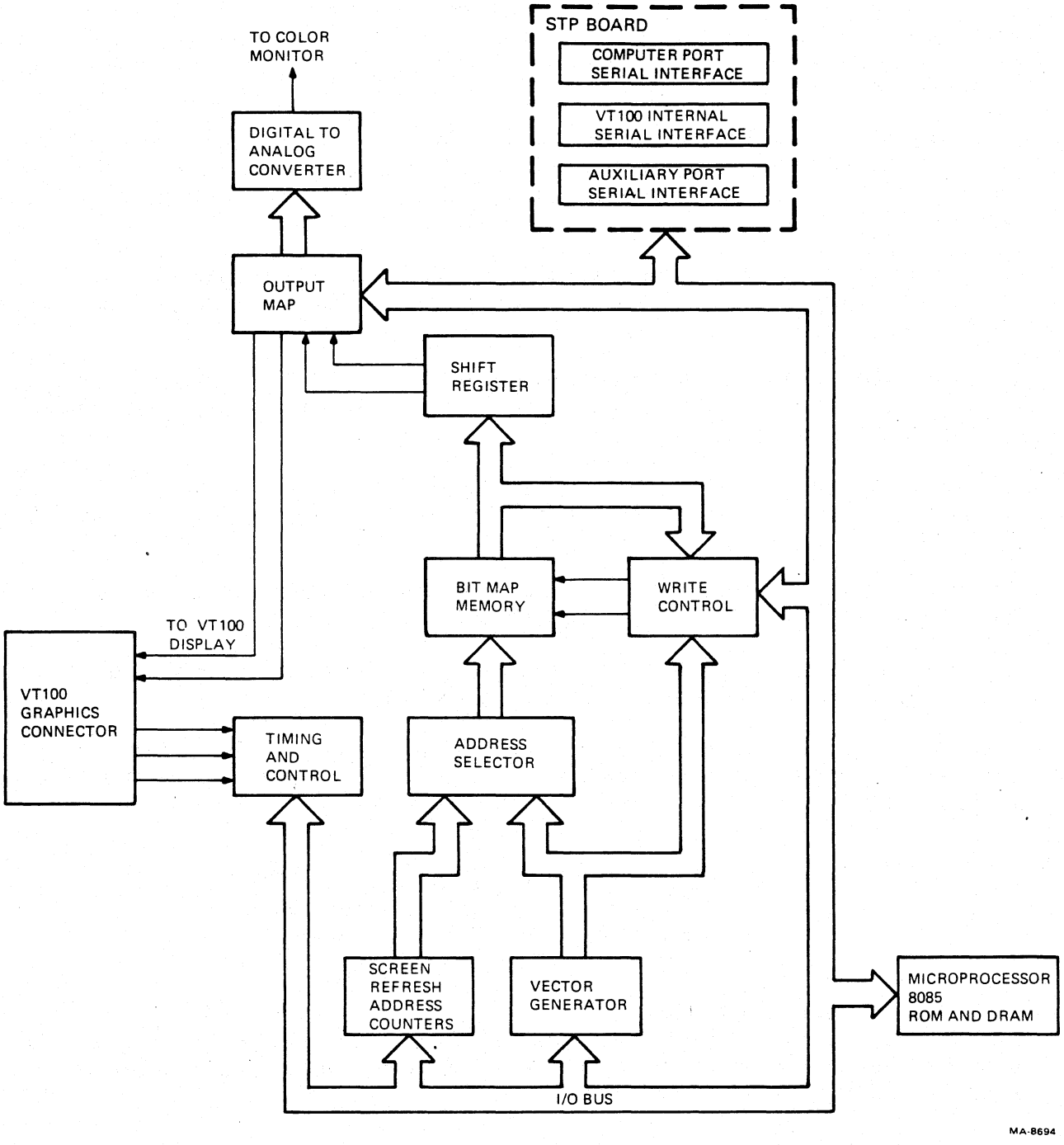


Figure 6-52 VT125 Graphics Processor Block Diagram

The *output map* is a small memory loaded by the microprocessor. It holds four sets of values that represent colors or intensities on video monitors. Two bits for each pixel in the bit map select one of the four sets of values at display time. ReGIS commands from the user set up the output map to correspond to the desired appearance of the display.

The *digital to analog converter* (DAC) takes a value from the output map at display time and converts the value to three analog voltage levels that an external color video monitor can use. (Another value from the output map passes unconverted to the DAC on the VT100 terminal controller for the internal video monitor.)

The *timing and control section* takes signals from the VT100 and uses them to synchronize the graphics processor's operations. This section produces many signals to control the vector generator and screen refresh processes.

A pair of *counters* provide the screen refresh addressing for the display. All the bit map locations appear on the screen every 60th of a second in synchronization with the scanning beam in the video monitor cathode ray tube (CRT).

For each address produced by the refresh counters, 12 bits are read out of the bit map. The *shift register* moves the 12 bits out to the video monitor (through the output map) one at a time, shifting at the pixel rate.

The *vector generator* computes the locations of pixels for drawing straight lines (called vectors in graphics) into the bit map much faster than the microprocessor.

The *write control* reads the contents of the location that the vector generator computes, and then writes a new value into the location according to user specifications.

The *address selector* controls the addressing of the bit map. Display refresh happens all the time, so the vector generator must share the bit map address bus with the refresh address counters. Timing signals switch the address selector between the two address sources.

NOTE

The following discussion is keyed to the VT125 Field Maintenance Print Set. All device numbers (for example, E45, Q6, R19) refer to components in that print set.

6.7.2 Microprocessor and Memory

The 8085 microprocessor supervises or controls all VT125 graphics processor activities. The microprocessor operates with firmware stored in a 24K × 8 read only memory (ROM), and with a 16K × 8 read/write memory (RAM) that serves four functions.

- scratchpad memory for the microprocessor computations
- buffer memory for the six transmit and receive data ports
- dynamically allocated macrograph storage
- storage for three loadable character sets

6.7.2.1 Memory, I/O, and Bus Operation – The microprocessor has two types of data transfer operations, memory and input/output (I/O). Paragraph 6.7.2 describes the use of memory.

I/O devices in the VT125 include serial data interfaces (UARTs), a status buffer, and data registers. Figure 6-53 is a block diagram of the microprocessor address and data paths.

The microprocessor uses a partially multiplexed bus to transmit data and addresses. The memory and I/O data use 8 bits. The memory address bus uses 16 address bits. The lower 8 address bits share the bus with the 8-bit data in the system. The shared bits are also the I/O address bus (but the same I/O address data also appears on the high 8 bits). A signal from the 8085 called address latch enable (ALE) appears briefly while an address is present on the bus. ALE strobes the low 8 address bits into a latch. The latch supplies the memories with their low 8 address inputs while data is being transferred. When the latch holds the address, the bus is cleared of address information. If the 8085 is reading, it sends a read signal (RD L), and a data byte appears on the bus from the accessed location. If the 8085 is writing into memory, it sends data and a write signal (WR L) to the RAM, which stores the data on the bus in the accessed location. Another signal from the 8085 called IO/$\overline{M}$ selects the I/O or memory buses so that the lower 8-bits of the 16-bit memory address do not conflict with the 8-bit I/O address.

The read only memory (ROM) holds the instructions that run the microprocessor. The ROM is three 8K $\times$ 8 ICs in three of four available IC positions. Each IC has 13 address inputs, plus a chip select line that enables the IC's outputs. A separate decoder selects one of the chip select lines according to the decoder's higher address line inputs.

The dynamic read/write memory (DRAM) is eight 16K $\times$ 1 ICs that are all addressed and read at the same time. Each IC holds all 16K locations for of the 8 data bits. Each DRAM needs 14 address bits to address all 16K bits, but the IC saves pins by dividing the 14 bits into two groups of 7 bits that it uses sequentially (Figure 6-54). An IC (E21) under control of the refresh controller selects between the two groups. One row of 128 locations is addressed during the row address strobe (RAS) portion of the address cycle. Then one column is addressed during the column address strobe (CAS) portion of the cycle. Any data in that location appears at the output during CAS. If the WRITE signal is low at any time during CAS, the data on the input is stored.

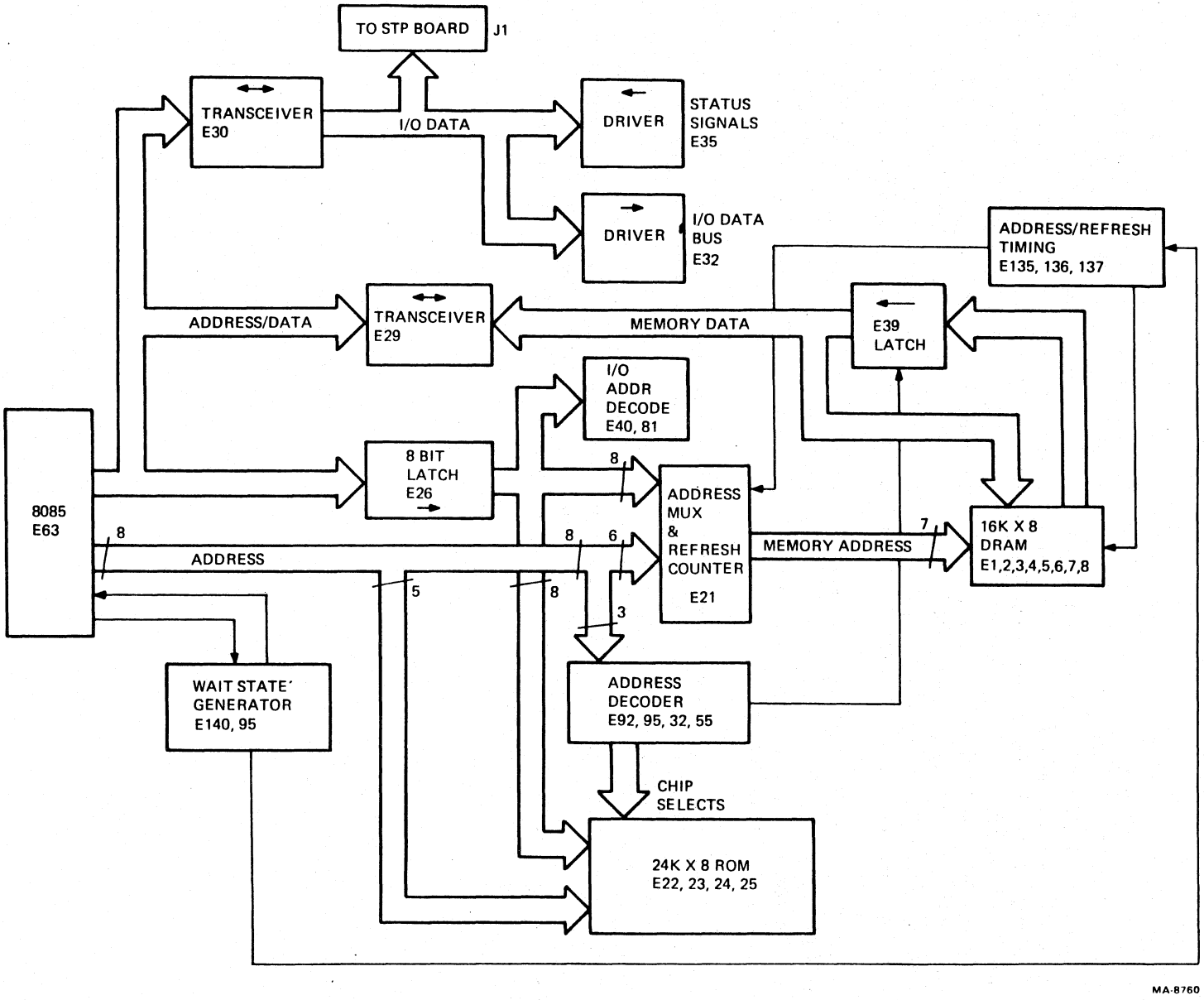


Figure 6-53 Microprocessor Address and Data Paths

6.7.2.2 Refresh Control – The graphics processor has only dynamic read-write memories (DRAM). These memories store more data and use less power than the static RAMS used in the VT100. They are also more complicated to use. A static memory circuit has a two-transistor bistable latch at each memory location. This circuit has two states, with one or the other transistor turned on. The circuit holds either state, without new inputs, as long as power is on.

The dynamic memory circuit has one transistor and a capacitor at each memory location. It stores data as a charge on the capacitor. This charge leaks away over time, so the memory location must be read and rewritten before the charge becomes unmeasurable. This process is called refresh, and must happen within 2 milliseconds of the last write.

The IC includes some of the circuitry for a refresh. When any row of 128 columns is addressed during the RAS portion of the address cycle, all 128 bit locations are refreshed. But the microprocessor does not always access to all 128 rows within every 2 milliseconds. A 7-bit counter is needed to address the rows consistently. The clock is not on the IC because extra pins would be needed to control the refresh process, to prevent it from interfering with accesses to the DRAM. Therefore, two external circuits control the addressing and the timing of the refresh.

The first external refresh control circuit is the microprocessor memory control timing sequencer (Figure 6-55). This circuit (with the WAIT state generator) controls the timing of refresh; it also controls reading and writing to the DRAMs. The timing sequencer consists of a ROM (E135) and a latch (E137). The ROM has eight address inputs. The addresses point to groups of data that, when latched, are the control signals that drive the refresh process. The latch is strobed by a 6 MHz clock made from the 3 MHz 8085 clock to provide synchronization to the 8085 times states. (The time relationship between the 6 MHz clock input to the 8085 and the 3 MHz 8085 CLK output is too loosely specified to be useful in this circuit. Generating one signal from the other provides the tighter tolerance that is needed.) E12 and E50 perform the doubling. The sequencer produces five signals: REF EN/$\overline{\text{CNT}}$ (Refresh Enable/$\overline{\text{Count}}$), ROW/$\overline{\text{COL}}$, RAS, CAS, and WE L (Write Enable Low).

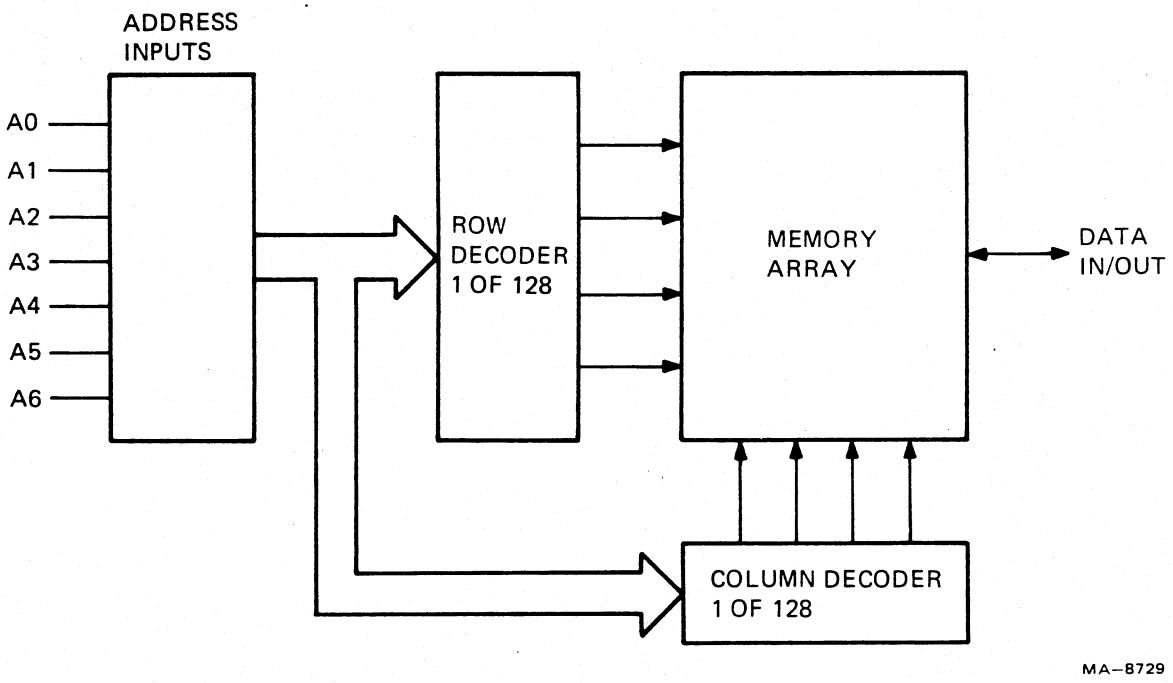


Figure 6-54 DRAM Block Diagram

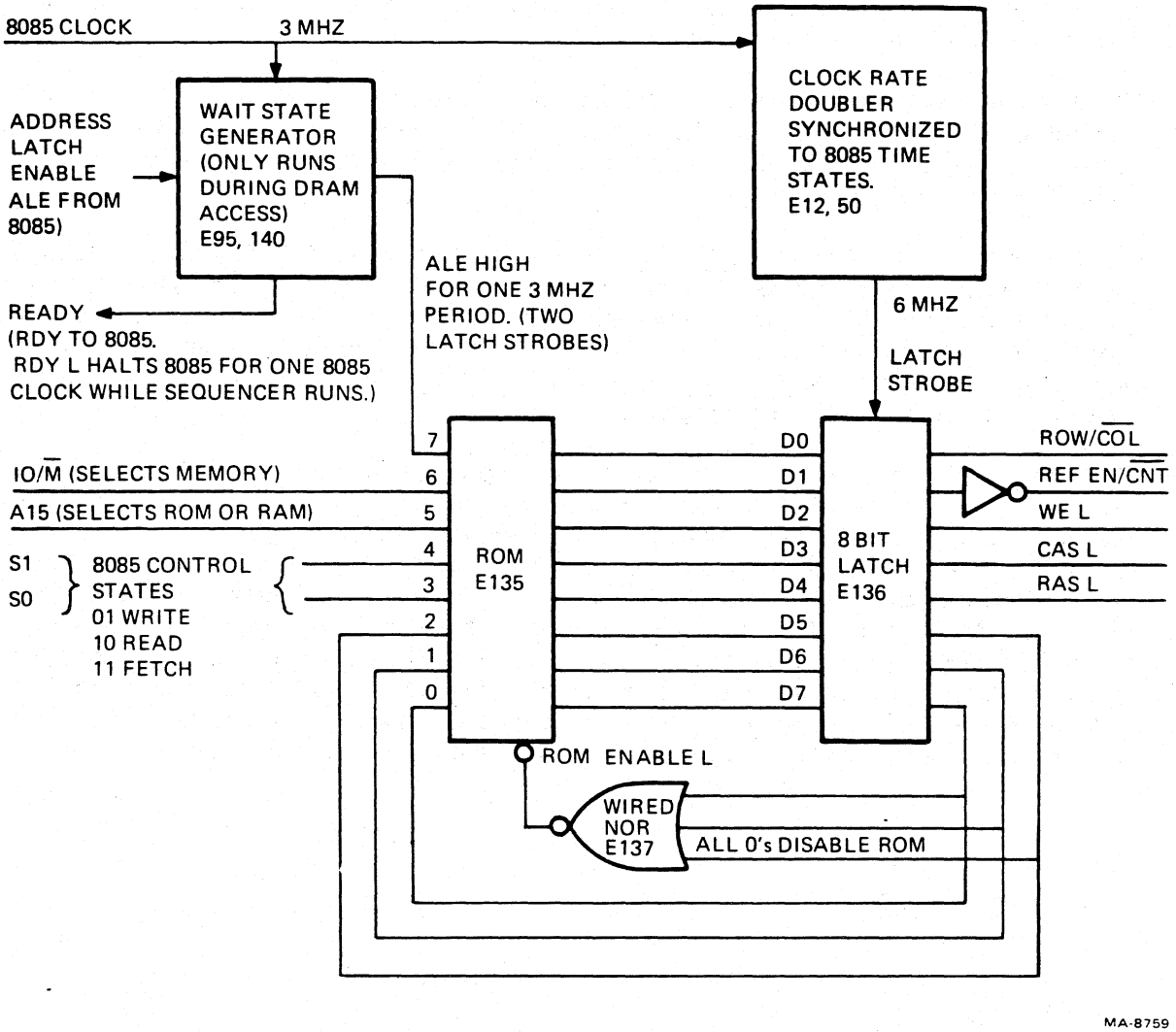


Figure 6-55 Microprocessor Memory Control Timing Sequencer

The second external refresh control circuit is the address multiplexer and refresh counter (E21) (Figure 6-56). When the REF EN/$\overline{\text{CNT}}$ signal from the control timing sequencer goes high, a refresh cycle begins. Refresh counter E21 puts the contents of its internal 7-bit counter on the DRAM address lines. The RAS signal from the control timing sequencer strobes the 7-bit count into the DRAMs, refreshing the addressed row of 128 data bits in each DRAM IC.

When the REF EN/$\overline{\text{CNT}}$ signal from the control timing sequencer goes low, the refresh cycle is completed and the refresh counter increments by one. The new counter contents are used in the next refresh cycle. Now the address multiplexer part of E21 passes microprocessor address data to the DRAM if needed. There are 14 address bits from the microprocessor to address the 16K DRAM. The ROW/$\overline{\text{COL}}$ signal from the control timing sequencer controls the multiplexer to select one of two groups of 7-bits. While the ROW/$\overline{\text{COL}}$ signal is high, the RAS signal from the control timing sequencer strobes the row address bits into the DRAM. Then ROW/$\overline{\text{COL}}$ goes low, and CAS from the control timing sequencer strobes the column address bits in. WE L goes low for a write memory access.

6.7.2.3 DRAM Control Timing Sequencer Details

There are three groups of address inputs to the ROM.

1. The signals on ROM inputs 3–6 come from the 8085. They indicate the type of cycle needed. For example, inputs 3, 4, and 5 high, and 6 low indicate an opcode fetch from RAM. These signals stay fixed for the entire cycle.

2. The signal on ROM input 7 is ALE from the 8085 (extended to two clock periods in the WAIT state generator). ALE indicates the beginning of an address bus transaction. The control timing sequencer starts its outputs at this signal. ALE goes low after two clocks, but the data is arranged in the ROM to handle the change in addresses.

3. The signals on ROM inputs 0–2 are outputs from the ROM itself. Each ROM data location provides a 3-bit address for the next location in the cycle. The latch holds this address (along with the control signal outputs) for one clock period. The data from the ROM includes another address, so at the next strobe the latch provides a new address to 0–2 on the ROM. Figure 6-57 shows the ROM outputs for the opcode fetch from DRAM cycle. Note that the octal value of any time state's Next Address 0–2 outputs is the same as the least significant digit of the next time state's ROM location. The last location in a cycle has all 0s in the low 3 bits. When the 0s are latched on the next clock, the wired-NOR output of E137 goes high and disables the ROM. Disabling the ROM forces the ROM's outputs to all 1s.

Address latch enable (ALE) is the signal the 8085 puts out at the beginning of every machine cycle. ALE is always defined; it never becomes tristated or random. However, all the other inputs to the ROM address lines may vary. A15 from the microprocessor address bus, for example, may become tristated in the last state of a machine cycle (according to the 8085 system timing diagrams). Therefore, the ROM is disabled for the last clock of a machine cycle to prevent errors.

The ROM has all 1s in all locations that can be addressed with ROM inputs 7 low and 0–2 all 1s. So the outputs do not change state until ALE goes high. Then the ROM address inputs point to a location that has some value other than 1s in the low 3 bits. On the next clock, the ROM address changes to the new location. The WAIT state circuit extends ALE to two clock cycles; ALE is the most significant bit of the ROM address, so the first two states in the ROM are in the upper half of the ROM address range. On the next clock, ALE goes low, so the ROM is addressed in the lower half of its range.

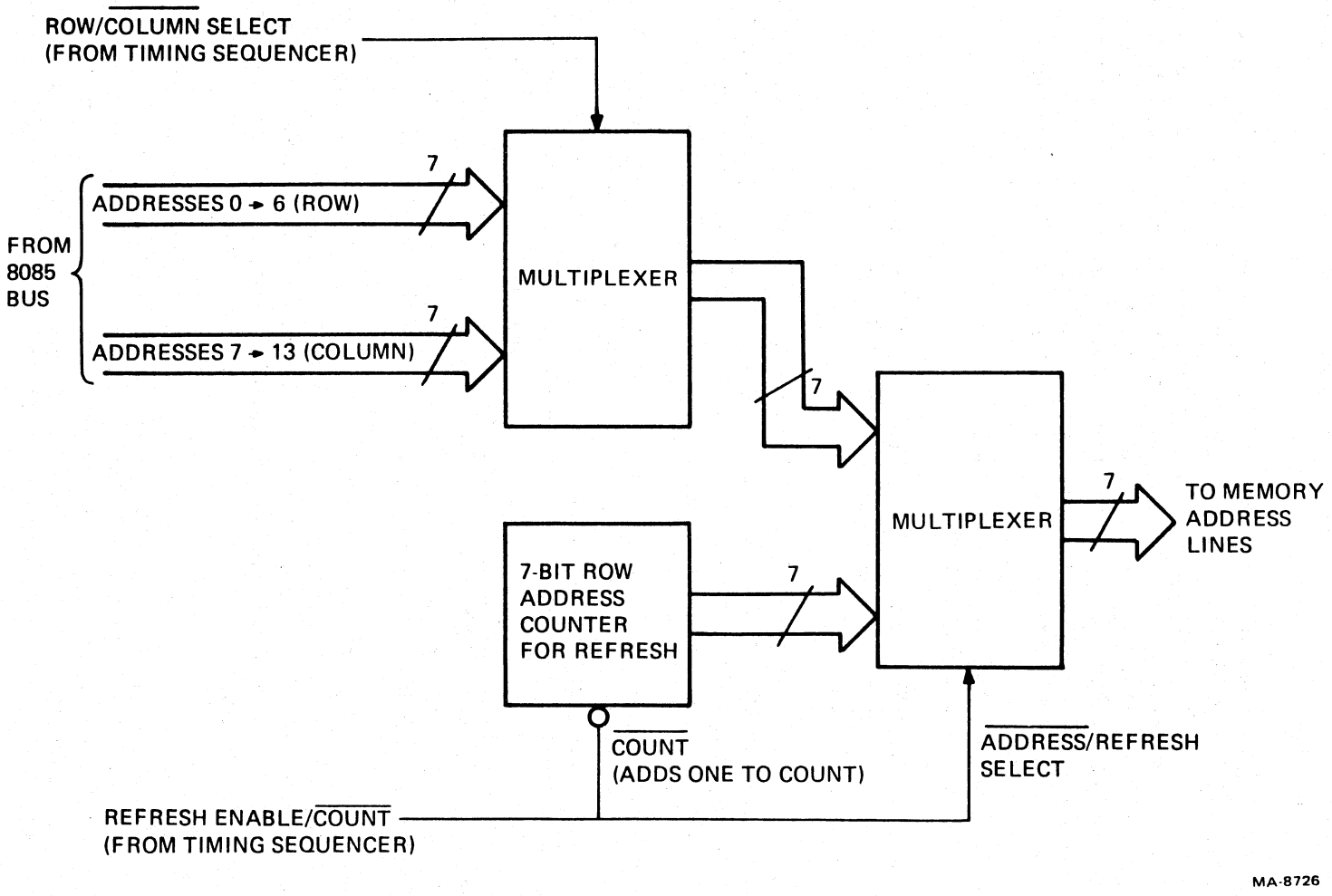


Figure 6-56 Address Multiplexer and Refresh Counter

6.7.2.4 The Microprocessor DRAM Memory Cycle

This section refers to the timing diagram for an opcode fetch from DRAM (Figure 6-57) to illustrate a DRAM memory cycle with refresh. During opcode fetch from DRAM, the 8085 reads the DRAM at one location. Then the refresh control refreshes the DRAM at 1 of 128 locations controlled by E21's internal counter.

During the first clock, ALE points the ROM to a location that sets ROW/$\overline{\text{COL}}$ high and sets REF EN/$\overline{\text{CNT}}$ low, incrementing E21's 7-bit counter (ROM location 277). The address multiplexer and refresh counter (E21) puts the low 7 bits of the 8085 bus address on the DRAM address lines. Next Address 0–2 point to ROM location XX1 (octal). The other inputs still point to 27X(octal). The following events occur in order on the next seven latch strobes.

- ROM location 271 has RAS go low to strobe the ROW bits into the DRAM. Next Address 0–2 point to location XX2. ALE goes low, but the new address contains the correct data.
- ROW/$\overline{\text{COL}}$ goes low and E21 puts the high 7 bits of the 8085 bus address on the DRAM address lines. Next Address 0–2 point to location 073.
- CAS goes low and the DRAMs put their data on the bus. Next Address 0–2 point to 074.
- RAS goes high (data is still on the DRAM outputs while CAS is low) and REF EN/$\overline{\text{CNT}}$ goes high. E21 puts the 7-bit count on the DRAM address bus. (ROW/$\overline{\text{COL}}$ is ignored.)
- CAS goes high and RAS goes low again and refreshes 1 of the 128 rows in the DRAMs, as selected by the 7-bit count. Next Address 0–2 point to 076.
- Next Address 0–2 all are 0s and they disable the ROM, forcing all its outputs high.
- All signals go high.

Similar processes occur in other memory cycles. The read from DRAM is an RAS–CAS cycle with ROW/$\overline{\text{COL}}$ selecting the address bits. The write to DRAM is the same cycle, but with write enable (WE L) low before CAS. CAS then performs the write. This early write keeps the data outputs tristated. (Tristating would allow the input and output lines to connect. However, for bus loading reasons, a data latch isolates and buffers the input and output lines.) The opcode fetch from ROM and I/O microprocessor cycles doesn't access the DRAM, so the timing sequencer adds a quick refresh by holding Refresh Enable high, setting RAS low, then ending the cycle.

6.7.3 Timing

Timing for the VT125 comes from several circuits (Figure 6-58). The VT100 signals are Horizontal Blank (HORIZ BLANK H), Vertical Blank (VERT BLANK L), and a 24 MHz clock. Two dividers make slower clocks from the 24 MHz for the graphics processor and the microprocessor. HORIZ BLANK H controls blanking in the VT100, but it is not the actual VT100 blank time. (Another signal provides the signal's end time, in synchronization with VT100 characters.) On the graphics processor board, HORIZ BLANK H goes through a synchronization circuit to align it with the graphics processor clock (16 MHz). VERT BLANK L goes to the state sequencer as a control input. VERT BLANK L also combines with HORIZ BLANK H in the synchronization circuit. The output is a complete video blanking control signal that blanks the display through the output map.

The state sequencer controls all bit map operations, both reading and writing. Different operations use different combinations of sequencer outputs, but all operations take the same number of states. Signals from the microprocessor, vector generator, and other sources select the sequence to use. The sequencer counter provides the clock for the states of each sequence.

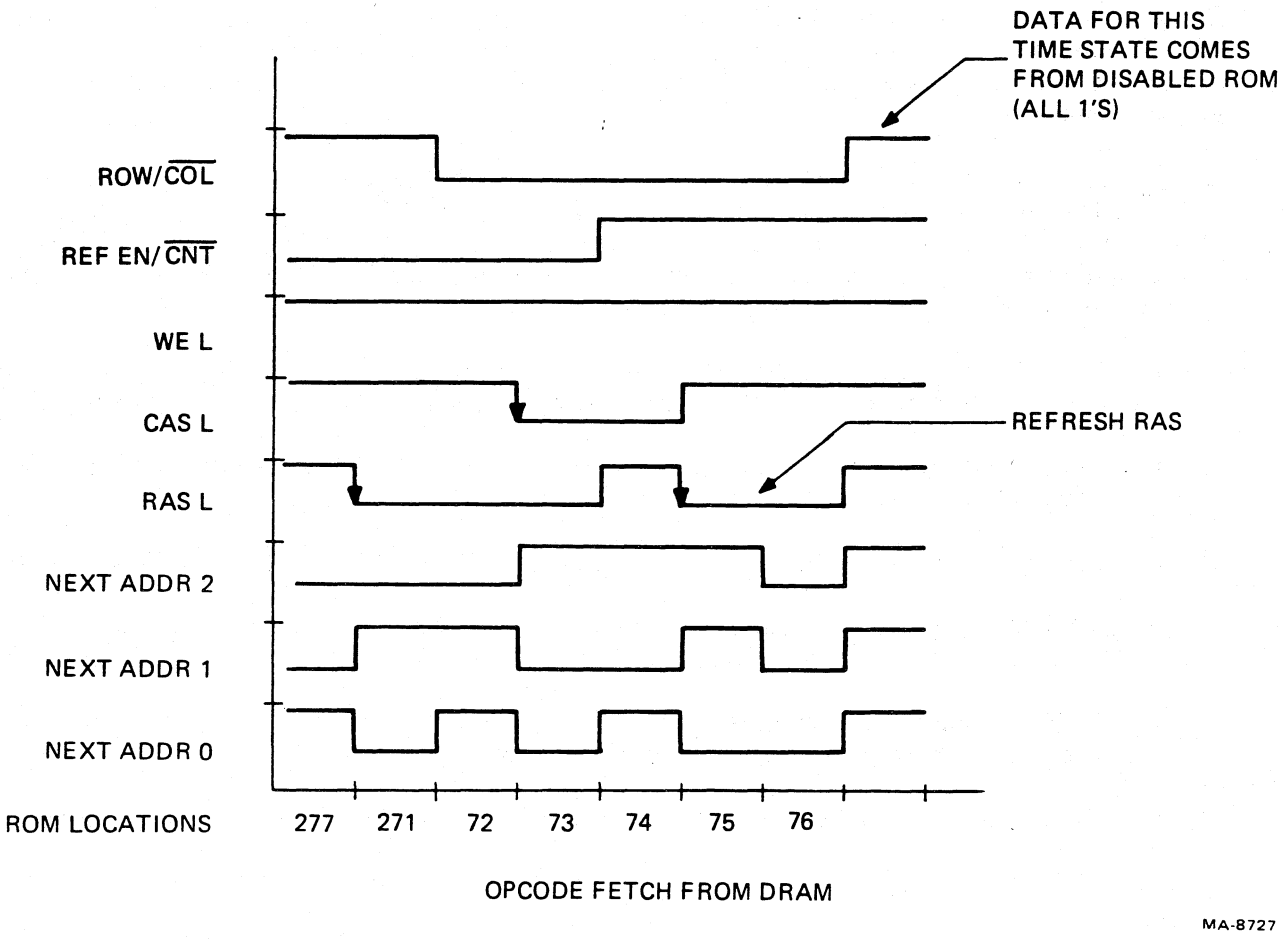


Figure 6-57 Opcode Fetch from DRAM

The vertical and horizontal counters provide bit map read addresses for display refresh. The microprocessor can load the counters with offsets from the I/O bus. Offsets can make the image appear in a different place on the screen from where it was created. The horizontal counter counts only in 12-pixel groups, so a separate, smooth offset counter lets the image move by 1 to 12 pixels at a time. A pause signal from the smooth offset counter synchronizes the state sequencer at the beginning of each horizontal scan.

Several small synchronization circuits adjust microprocessor and vector generator control signals to the timing of the state sequencer.

6.7.3.1 Clocks – The master clock for the VT125 is the 24.0734 MHz video processor clock from the VT100 graphics connector. This clock keeps the graphics processor video output synchronized with the VT100 video processor output. However, the 24 MHz clock is not used directly, but divided into several smaller clocks. It is divided by 1.5 to give a 16 MHz pixel rate clock. The 16 MHz clock is used in several places, including inputs to other dividers for pixel-related processes. The 24 MHz clock is also divided by 4 and 8. The 6 MHz signal is the 8085 clock source, and the 3 MHz signal is the clock for the internal operation of the UARTs on the STP board. The phase of the internal 8085 clock is too loosely specified relative to the 6 MHz input for timing that must be synchronous with the 8085. A multiplier makes 6 MHz from the 8085 3 MHz clock output to drive the refresh controller.

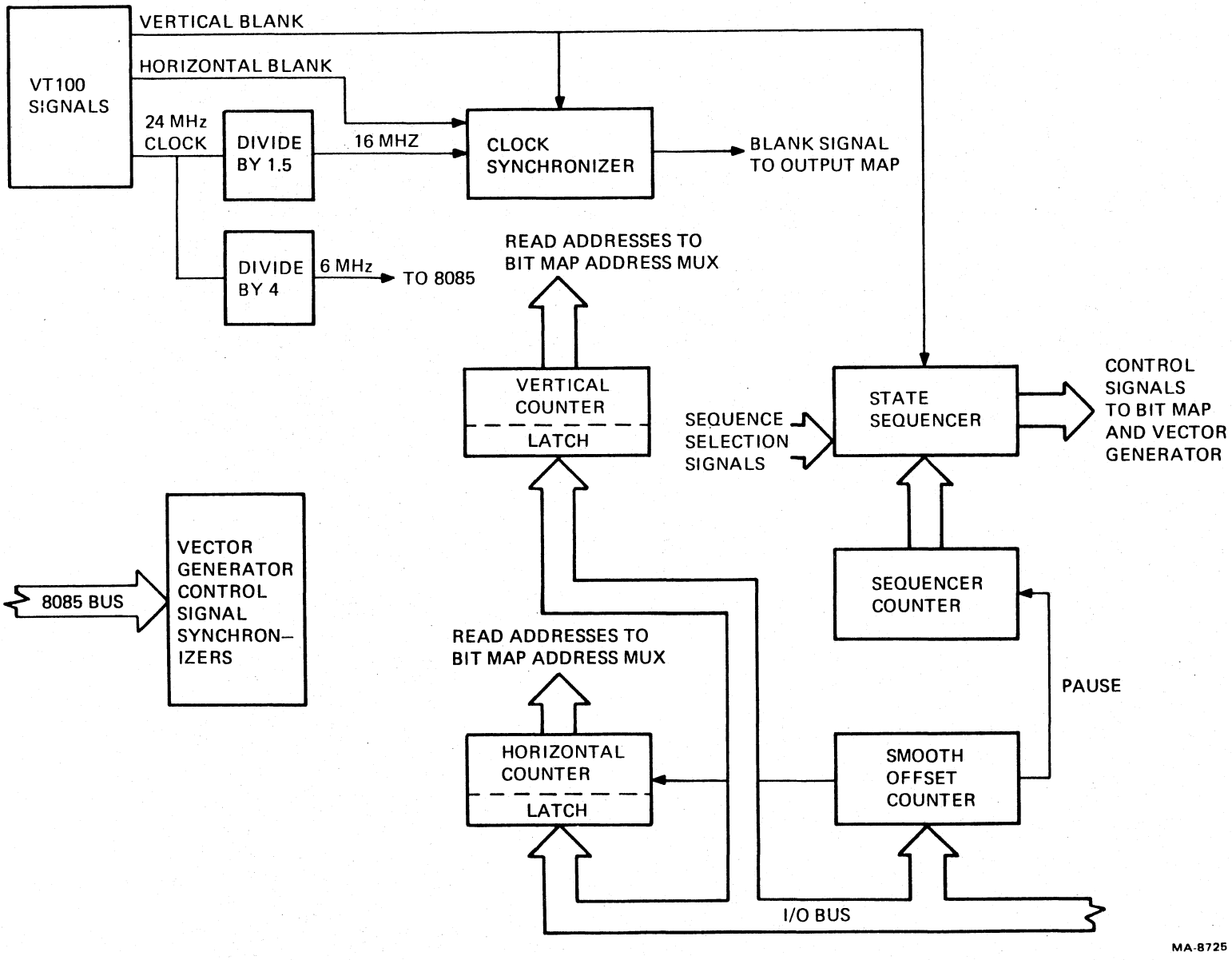


Figure 6-58 VT125 Timing Block Diagram

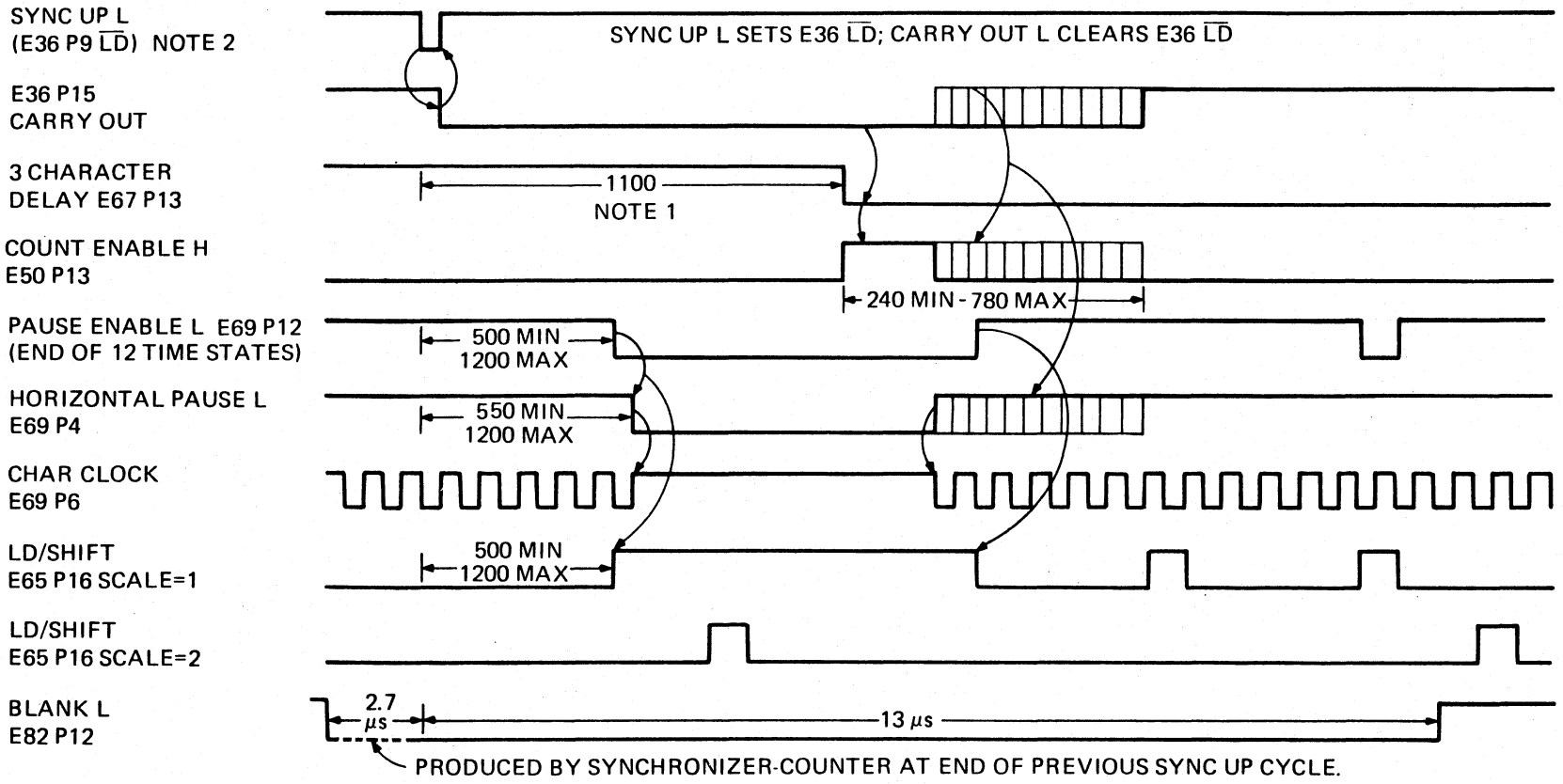
6.7.3.2 Horizontal and Vertical Counters – The horizontal and vertical counters provide the addresses for reading the bit map memory to the raster-refreshed screen. The vertical counter has 8 bits to count each of the 256 scans of memory. The HORIZ PAUSE L signal is the clock for the vertical counter, because that signal occurs once each horizontal scan. Thus, the vertical counter increments once each scan. The horizontal counter has 5 bits to count each of the 64 groups of 12 pixels in each scan. Each time a read from the bit map occurs, 1 bit from each of the 12 RAMs of each memory plane is loaded into a 12-bit-long shift register. The first input bit appears at the shift output of each shift register during the load signal. When the load signal ends, the next clock moves the next bit to the output. The shift process continues while the vector generator reads or writes to the bit map. The LD/SHIFT (Load/Shift) signal from the state sequencer controls the operation of the shift register and clocks the H position counter.

6.7.3.3 Offsets – Assuming the default address axes, offset is the distance between the top left corner of the screen and the address space origin (location [0,0]). An offset of [100,100], for example, means that the display location [0,0] moves to the right and down by 100 pixels each. Vertical offsets are produced by loading some new number into the vertical offset latch (LD V OFFSET). (Both latches are always loaded with standard offset values that adjust the display relative to the blank signals.) The V STROBE signal loads the offset value into the vertical counter which then counts as usual from that value. Horizontal offsets are more complicated. (See Figure 6-59.)

The horizontal counter provides addresses to groups of 12 pixels at a time. (This is because each horizontal counter address accesses 12 DRAMs in each plane at the same time. These are the 12 bits that are shifted out.) Therefore, a horizontal offset that changes the horizontal counter output by 1 changes the display position by 12 pixels. To provide more control of the offset, a separate smooth offset circuit delays the start of the count by 1 to 12 counts. The count actually begins before BLANK L ends, so the effect of the delay is to move the display by 1 to 12 pixels. Larger changes, of course, are made with the offset latch.

The HORIZ PAUSE L signal is the output of the smooth offset circuit. The signal loads the rough horizontal offset value from the horizontal offset register, but it does not return to a high state until the smooth offset counter completes its count of 1 to 12. The low state keeps the H position counter from counting, so the HORIZ PAUSE L signal both loads the rough offset and provides control of the counter by the smooth offset circuit.

HORIZ PAUSE L also stops the state sequencer. When HORIZ PAUSE L goes high, the state sequencer starts. HORIZ PAUSE L can go high only on the rising edge of the shift clock, because of the smooth offset circuit. Therefore, LD/SHIFT comes from the state sequencer, some integral number of 16 MHz clocks after HORIZ PAUSE L. LD/SHIFT is ANDed with the second half of the 8 MHz clock to make LD/SHIFT CLK at the end of the LD/SHIFT pulse. If LD/SHIFT is delayed by one 16 MHz clock shift, the anding happens with the wrong phase of 8 MHz and LD/SHIFT CLK. After two clock shifts, the 8 MHz clock is the correct phase again. To prevent LD/SHIFT CLK from appearing in the wrong half of LD/SHIFT, the 8 MHz clock is inverted every other pixel offset; this gives the correct signal level for ANDing with LD/SHIFT. When the display is scaled, the Shift Clock is 8 MHz and each smooth offset delay is an integral number of 8 MHz clocks. So the phase of LD/SHIFT does not change relative to the Shift Clock, and the 8 MHz clock is not inverted.



NOTE 1: ALL TIMES IN NS EXCEPT WHERE SPECIFIED.

NOTE 2: TIMING SIGNAL FROM START OF H BLANK TIME.

MA-8730

Figure 6-59 Smooth Scroll Offset Timing

6.7.3.4 Scaling – Scaling means changing the size of an object in the display. In the VT125, the complete display changes at the same time, and there are only four size choices. The display can be times 1 (X1, default), X2 in horizontal direction, X2 in vertical direction, or X2 in both directions. The VT125 performs scaling by changing the rate that data moves from memory; this means a given pixel appears for a longer period of time, while the video raster scanning operates without change. Vertical scaling is simple. A signal from the 8085 adds a divide-by-2 circuit to the count input of the vertical address counter. Then, only every second HORIZ PAUSE L increments the vertical address, so each pixel appears in two sequential scans. Scaling only affects the counter-incrementing rate, so offsets are not scaled.

Horizontal scaling is more complicated. It begins with a change in the pixel-shifting rate (SHIFT CLK) from 16 MHz to 8 MHz. Now each pixel appears twice as wide in the display, which is scanning without change at 15.7 kHz. If not for write circuit time limits, all of the bit map timing could be slowed from 16 MHz to 8 MHz. But LD/SHIFT loads the shift registers every 12 counts at 16 MHz, which would load new data with only 6 of the pixels displayed. So LD/SHIFT changes to load every 24 counts at 16 MHz. And alternate pixel offset inversion of the 8 MHz clock for LD/SHIFT is not performed.

6.7.3.5 State Sequencer – The state sequencer has three main parts: a counter, a bit map control section made of two ROMs and their latches, and a vector generator section made of one ROM and its latch.

The counter (E62) has an 8 MHz clock input, four count outputs, and a carry output that loads the counter with a starting value to make the count self-repeating and equal to 12 (modulo 12). The counter counts down from 1011 (decimal 11, the starting value) and carries at 0000 (decimal 0). The counter changes output states once each 8 MHz cycle, so the fastest state sequencer change is at a 4 MHz rate (250 ns period). The clock comes from the smooth offset circuit that turns the clock off for a portion of the horizontal blank period (Figure 6-59).

The bit map control ROMs and latches (E64, E65, E66, E83) provide control signals that the bit map needs to refresh the screen continously. They also provide the control signals that the vector generator needs to access the bit map in synchronism with the screen refresh process.

ROM E64 and its latch E65 provide the following signals.

- SYNC to synchronize microprocessor control signals
- X SCALE to indicate horizontal scaling to other circuits
- V STROBE to load the vertical offset into the vertical refresh address counter
- LD/SHIFT to load the bit map shift registers and then shift the data to the screen
- RA and RB signals that address the register file to select the data for the vector generator in synchronism with the refresh process

ROM E66 and its latch E83 provide the following signals.

- VG STROBE to control the vector generator read from the bit map and latch the carry bit from the adder
- WR/RD to switch the bit map address multiplexer between the vector generator (write) and the refresh (read) address circuits

- CAS to the bit map DRAMs
- RAS TIME to the RAS/CAS selector for the bit map
- four RAS signals to four groups of 3 bit map DRAMs. All four RAS signals cycle for each screen refresh read, but one of the four doubles its rate when the vector generator is accessing its group (determined by the X0 and X1 inputs to the ROM).

The vector generator control ROM and latch (E71, E70) only provide signals when the microprocessor sends GO L to enable the ROM when a vector is needed. The signals are as follows.

- ERASE L, which continuously forces the WR/RD signal from ROM 66 to the read state, so the timing circuit can write the background value to every location in the screen
- SHIFT ENA, which is not used but could lock the pattern multiplier to a single bit output if used
- C In, which is a carry in to the adder to convert a 1's complement number into a 2's complement number
- D LOAD, which is synchronized with VECTOR CLK in another circuit to control the error register
- WRITE L, which writes a pixel into the bit map at the computed location
- DONE L, which signals the end of the vector after the down counter sends DCNT DONE L. DCNT DONE L is synchronized with D LOAD to make the FINISH signal
- VECTOR CLK, which increments the position registers after new data is written in the current position
- STROBE ERROR L, which loads the adder's output into the error register

6.7.3.6 Blanking and Clock Synchronization – The VT125 gets its timing signals from the VT100. They are the 24 MHz clock, and Horizontal Blank, and Vertical Blank. But the graphics screen area is different from the text screen area, so the VT100's blanking time is not correct for the VT125. There is a 2.3 character difference between the start of the text area and the start of the graphics area (more in VT105 compatibility mode). Therefore, the VT125 creates its own blanking signal, using Horizontal Blank from the VT100 for synchronization.

First, HORIZ BLANK H goes through a latch and gate circuit to produce a single clock-wide pulse (SYNC UP L) at the beginning of the VT100's horizontal blank. After horizontal blank starts, the first clock latches the high signal on pin 2 of E120. The second clock latches it on pin 19, which connects to one input of a NAND gate. The third clock latches it on pin 16, which connects to one input of an XOR gate. The XOR gate, with only one of its inputs high, outputs high to the other input of the NAND gate. The NAND gate outputs SYNC UP L. The fourth clock latches HORIZ BLANK H on pin 15, which connects to the other input of the XOR gate. The XOR gate, with both inputs the same, outputs low to the NAND gate. The NAND gate output goes high and ends SYNC UP L, which lasted one clock time.

In the VT100, HORIZ BLANK H from the DCO11 that enters the DC012 ends a partial character time early. The actual end here is not critical. The DC012 extends the signal with the character clock to make blanking end on a character boundary. The DCO11 HORIZ BLANK H end time can vary as much as one VT125 pixel time due to temperature changes and long term drift in gate delays within one VT100, or component differences between VT100s. If the actual end time is between two pixel times, synchronization of the graphics horizontal blank can jitter between the two pixel times from one vertical interval to the next. A microprocessor-controlled circuit prevents the annoying appearance of the first pixel in each horizontal scan, blanking and unblanking randomly at speeds up to the vertical scan rate.

The problem with drifting signals is that the clock might rise at the same time as HORIZ BLANK L causing race conditions. Latch E120 is the place where this is most evident. If HORIZ BLANK L goes high in time before the next rise of 16 MHz, then it gets latched properly. But if H BLANK L is late enough, the latch may miss it and have to catch it on the next clock tick. This would cause SYNC UP L to occur one clock time late. At the same time the counters E84, E67, and E68 are counting normally from the 16 MHz clock. They expect to count to 768 each scan. If HORIZ BLANK L is normal, then at SYNC UP pin 14 has a high level during that count. But if HORIZ BLANK L is missed at latch E120, then when SYNC UP occurs a clock tick later, the count at pin 14 is low. Then SYNC UP strobes the inverted count into flip-flop E52, which latches itself up. The microprocessor reads E52's output, CLK OUT H, to determine if the rising edge of HORIZ BLANK L is too close to another transition to give clean results. Then the microprocessor waits until a safe time (relative to RAS signals occuring in the memories) and commands the clock to invert with CLK SHIFT. The inversion moves the rising edge of the clock away from the rising edge of H Blank. CLK SHIFT is a toggled, rather than set, signal. It only changes when drifts cause the rise times to coincide, and its result is always a move away from a critical state, in whatever direction. A few scans later, the microprocessor clears the CLK OUT flip-flop to allow the monitoring to continue.

SYNC UP L, derived from HORIZ BLANK L, loads 0s into counter E84. (The complete counter – E84, E67, E68 – is loaded with a value that provides a three-character delay to the start of the graphics display area, relative to the VT100 text area.) SYNC UP L goes away on the next high state of the 16 MHz clock. A few scans after the Vertical interrupt signal, before vertical blank ends, the microprocessor reads a signal on its status register that indicates whether the clock is synchronized correctly or not. If not, the microprocessor commands the circuit to use the inverted clock with CLK/SHIFT H. (This signal comes from an unused modem control line on the internal communication VT100 UART on the STP board.)

The V STROBE signal loads the vertical offset into the vertical address (Figure 6-60). V STROBE occurs at the end of vertical blank and is synchronized with enable vertical sync (ENA VERT SYNC) from the synchronization circuit. The offset value loaded into the counter compensates for the difference in time between the start of the screen and the end of blanking.

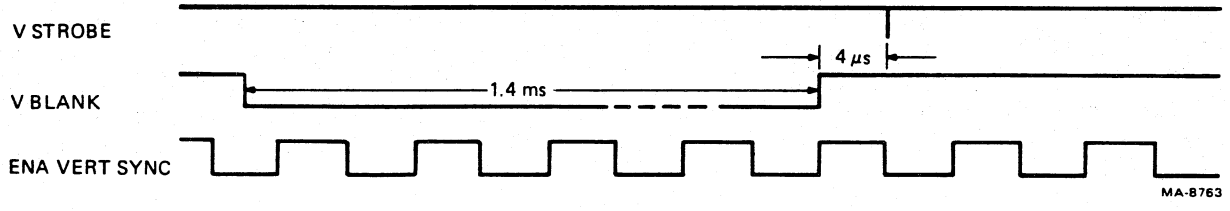


Figure 6-60 V STROBE Timing

6.7.4 Vector Generator

The vector generator is a special circuit that writes straight lines (called vectors in graphics) into the bit map much faster than the microprocessor can. A vector can be specified with three items: starting point, direction, and length. The microprocessor puts that information in a fast, dedicated circuit that performs a process called Bresenham's algorithm to draw the vector.

6.7.4.1 Circuit – The vector generator is made of several parts (Figure 6-61).

The X and Y position counters address the bit map for most operations. The microprocessor loads the position counters with the starting point coordinates for the vector to be drawn.

The down counter stops the vector generator when the vector is completed. The microprocessor loads the counter with the length of the major axis of the vector to be drawn. Then, as the vector generator computes and draws each pixel, the counter decrements by one. When the counter overflows, it outputs the Done signal, which stops the vector generator.

The register file holds the X and Y lengths of the end point (Figure 6-62) and the direction of the vector. (The fourth word in the file is not used.) The microprocessor loads these values before starting the process. The vector generator's data path is 8 bits wide, so the longest vector that can be drawn in a single step is 256 pixels. The microprocessor has to reload the vector generator with more segments to complete a long vector.

The adder uses binary arithmetic methods to subtract the length of the shorter axis of the vector from the length of the longer axis.

The direction control ROM has 5 input bits: 3 bits of direction (the same as the 8-pixel vector directions), 1 bit that indicates whether the direction is one of the pixel vector directions or between them, and the carry output from the adder. If the direction is between the pixel vector directions, that bit makes the ROM accept the carry output to decide when to increment or decrement the minor axis. The ROM ignores carry if the direction is one of the pixel vector directions. Then one or the other or both X and Y counters increment(s) or decrement(s) every time. The ROM's four outputs select the direction and specify the count of each position counter.

The error latch and multiplexer hold the results of the adder's operation to subtract from in the next cycle. The multiplexer selects the input for the latch. The input comes from the adder during a vector operation, but it comes from the microprocessor during setup for the vector. The microprocessor loads a calculated value into the latch to make vectors skip from scan to scan in an orderly manner.

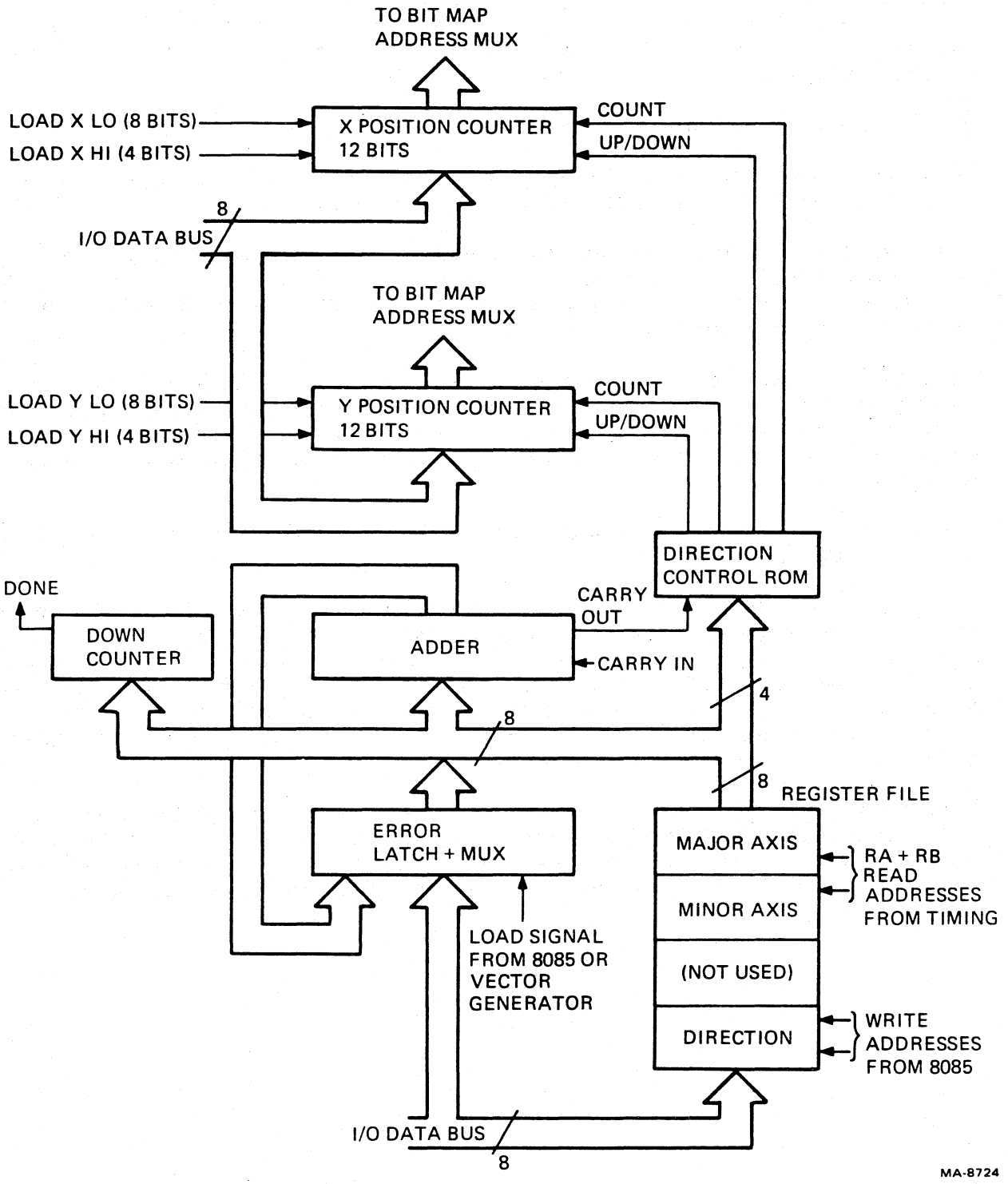


Figure 6-61 Vector Generator

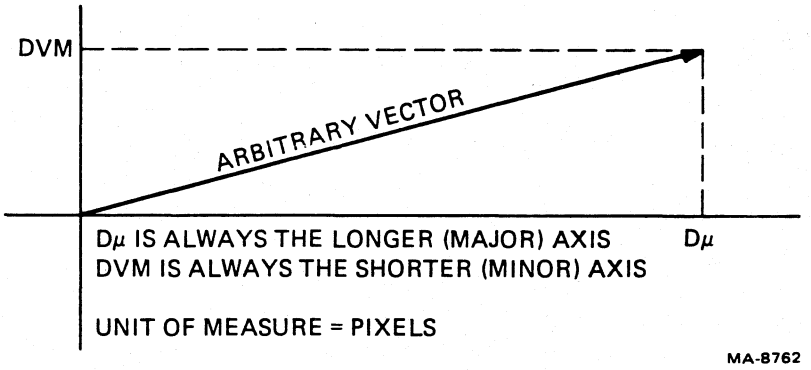


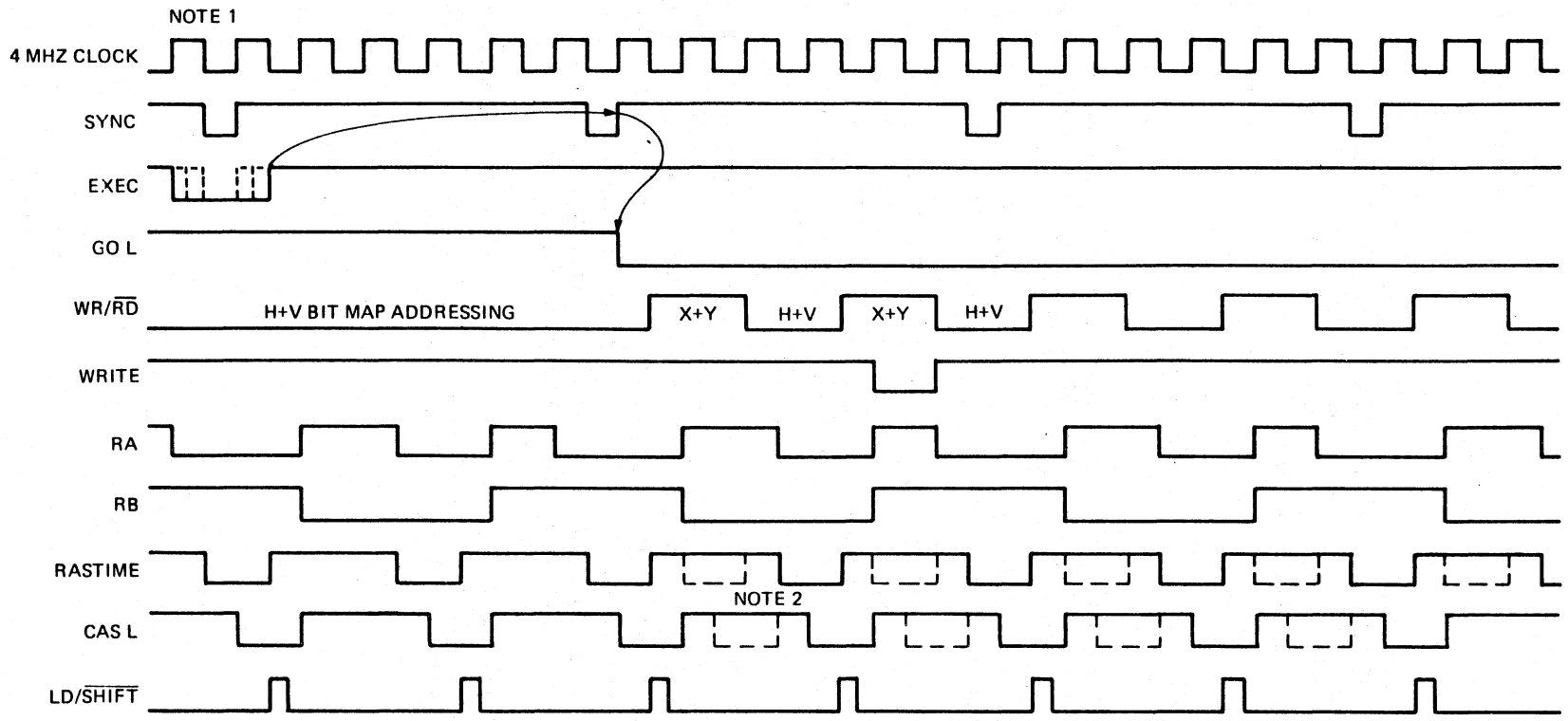
Figure 6-62 Derivation of Dμ and DVM

6.7.4.2 Vector Generator Timing – The microprocessor sends an Execute signal to the vector generator after it loads parameters into the vector generator (Figure 6-63). EXEC L from the microprocessor is synced to the state sequencer by SYNC. The result is GO L, a signal that switches the state sequencer from bit map reading only (for screen refresh) to a shared read/write cycle. The vector generator X and Y counters share the address lines to the bit map with the H and V counters.

Before GO L, only H and V addresses are accessed. (See RAS TIME and CAS L on Figure 6-63.) LD/SHIFT loads twelve data bits from the bit map memories into the shift register. LD/SHIFT also increments the H counter. After 12 pixel clocks (6 transitions of the 4 MHz state sequencer clock, or halfway through the sequence) another LD/SHIFT loads new data. Each H and V bit map read takes half of the time available, and one quarter of a state sequence.

GO L is synchronized to occur while the bit map contents from an H and V read are loaded into the shift registers. After GO goes low, the bit map address multiplexer, under control of the WR/RD signal, selects the initial X and Y values (loaded by the microprocessor) to address the bit map. A circuit described in Paragraph 6.7.5 selects the addressed pixel bits and creates a new pair of bits to write back into the bit map at the same location. While the circuit is preparing data for writing, the bit map address multiplexer returns to the H and V counters and writes the modified data into the bit map. To shift out, the multiplexer switches back to the H and V counters for 12 more pixels.

At the same time, the vector generator computes the next location to draw a pixel. The computation makes the X, Y, or both counters increment or decrement by one count. Then the X and Y counters provide an address to read, modify, and write the next pixel in a vector.



NOTE 1 SIGNALS ARE LATCHED BY 8 MHZ. 1/2 CYCLE SHIFT NOT SHOWN.

NOTE 2 DOTTED SIGNALS SHOW ADDED BIT MAP MEMORY ACCESSES WHEN VECTOR GENERATOR IS RUNNING.

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Figure 6-63 Vector Generator and Bit Map Address Timing

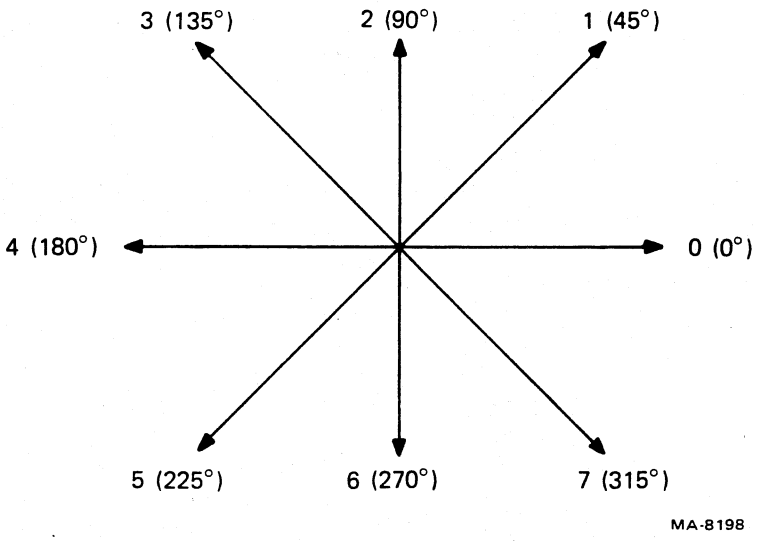


Figure 6-64 Basic Vectors

In this method, any vector starts at some X and Y coordinate in the bit map plane (the current value in the position counter), and ends at another X and Y coordinate. The differences between the two Xs and two Ys are the axes of the vector. The signs of the differences determine the direction of the vector. The direction controls incrementing or decrementing of each position counter. The longer axis is called the major axis and the shorter axis is called the minor axis. (References to Dμ and DVM are from the original mathematical analysis.)

The length of the major axis loads into a counter that counts down after each pixel is written. The counter stops the vector generator when the vector is done. The length of the major axis also loads into an arithmetic device (the adder) where the length of the minor axis is subtracted from the major. After each subtraction, one pixel is written. Then the position counter that controls the major axis is incremented or decremented. If the value remaining in the adder before the subtraction is smaller than the value of the minor axis, the next subtraction causes the adder to carry. Then the minor axis counter is incremented or decremented and a pixel is written.

The next series of figures and tables shows the computation and writing of pixels in more detail. The rules listed refer to the changes needed in the algorithm to correct for odd-Y simulation. The microprocessor computes start and end values with 512 Y addresses, but the vector generator only has 256 Y addresses to write in.

6.7.4.3 Drawing Vectors – The vector generator produces basic and arbitrary vectors. The basic vectors are shown in Figure 6-64). These are the pixel vector directions referred to in the *VT125 User Guide*. There are eight basic vector directions, 45 degrees apart. These vectors are the easiest for the vector generator to draw. From any position, a vector along one of these directions changes one or both coordinate values with every pixel write. For example, in the 0 direction, any vector is drawn by incrementing X, writing a dot, incrementing X, writing a dot. Once the direction is specified, the vector generator circuit does not make any decisions about when to change a position counter's value.

For arbitrary vectors, the vector generator must decide whether to change one counter after writing a pixel. For example, an approximately 15 degree angle vector increments its Y value only once for every four X value increments. The vector generator method for deciding when to increment is Bresenham's algorithm.

Calculation 1

Error register	=	002_8
DVM register	=	374_8 (1's complement of 3)
Carry in	=	001_8
Error register	=	377_8
		No carry

Decrement
major and minor axes.

Strobe

Error register	=	377_8
Dμ register	=	005_8
Error register	=	004_8
		Carry

Strobe

Direction – Decrement X and Y,
and do a Pixel Write.
Decrement the down counter.

5 – 1 = 4

Down counter = 4

Draw Vector. (Use these rules.)

1. Do not write in direction 2 from an odd line or 6 from an even line.

2. Do not write if the direction is 5 or 7, the scan line is even (Y0), and the last direction was 6.

3. Do not write if the direction is 1 or 3, the scan line is odd, and the last direction was 2.

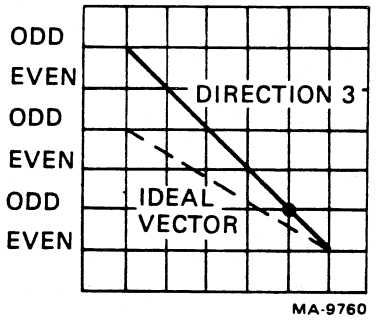


Figure 6-65 Calculation 1

Calculation 2

Error register	=	004_8
DVM register	=	374_8
Carry in	=	001_8
Error register	=	001_8 Carry

Decrement
major axis.

Strobe → Set Carry flip-flop.

Error register	=	001_8
Dμ register	=	005_8
		006_8

Error register = 001_8 (No Error CLK)

Strobe

Direction – Decrement X
and do a Pixel Write.
Decrement down counter.

4 – 1 = 3

Draw vector.

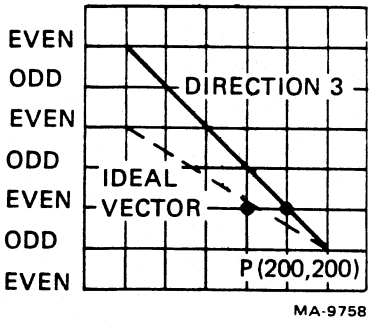


Figure 6-66 Calculation 2

Calculation 3

Error register	=	001_8
DVM register	=	374_8
Carry in	=	001_8
Error register	=	376_8
		No carry

Decrement
major and minor axes.

Strobe

Error register	=	376_8
Dμ register	=	005_8
Error register	=	003_8
		Carry

Strobe

Direction – Decrement X
and Y. Do a Pixel Write.
Decrement down counter.

3 – 1 = 2

Draw vector.

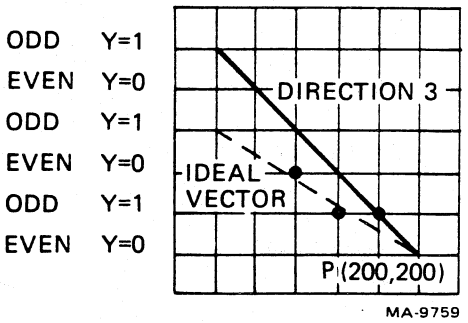


Figure 6-67 Calculation 3

Calculation 4

Error register	=	003_8
DVM register	=	374_8
Carry in	=	001_8
Error register	=	000_8 Carry

Decrement *major axis.*

Strobe

Error register	=	000_8
Dμ register	=	005_8
		005_8
Error register	=	000_8

Strobe

Direction – Decrement X and do a Pixel Write. Decrement down counter.

2 – 1 = 1

Draw vector.

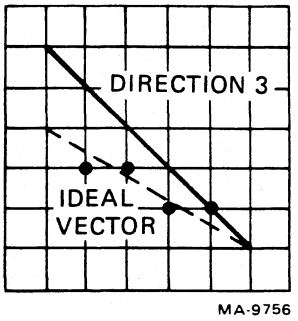


Figure 6-68 Calculation 4

Calculation 5

Error register	=	000_8
DVM register	=	374_8
Carry in	=	001_8
Error register	=	375_8
		No carry

Decrement
major and minor axes.

Strobe

Error register	=	375_8
Dμ register	=	005_8
Error register	=	002_8
		Carry

Strobe

Direction – Decrement X
and Y, and do a Pixel Write.
Decrement down counter.

1 – 1 = 0

Draw vector –
vector is complete.

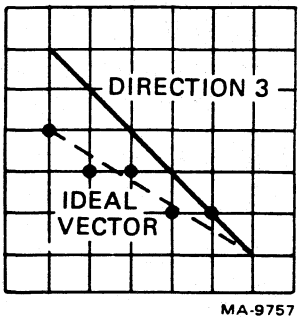


Figure 6-69 Calculation 5

6.7.4.4 Vector Calculation Timing – Twelve time states are needed to perform a calculation (Figure 6-70). These 12 time states are divided into 4 groups. The 4 groups are repeated until the vector is drawn. The four sequential groups are as follows.

1. DVM time
2. Dμ time
3. WOPS time
4. Direction time

The following paragraphs describe the separate functions that take place in each group.

- *DVM Time* – The error register is added to the DVM register plus carry in. The sum is loaded into the error register by error clock. The carry output of the adder is strobed into the carry flip-flop. (The error register is loaded at the start of the vector with one half the major axis value, ignoring the remainder.)
- *Dμ Time* – The contents of the error register are added to the Dμ register. If the carry flip-flop is reset, the vector ROM allows an error clock pulse that loads the result of the add into the error register. If the carry flip-flop is set, the vector ROM does not allow an error clock pulse to occur. This means the contents of the error register remain unchanged.

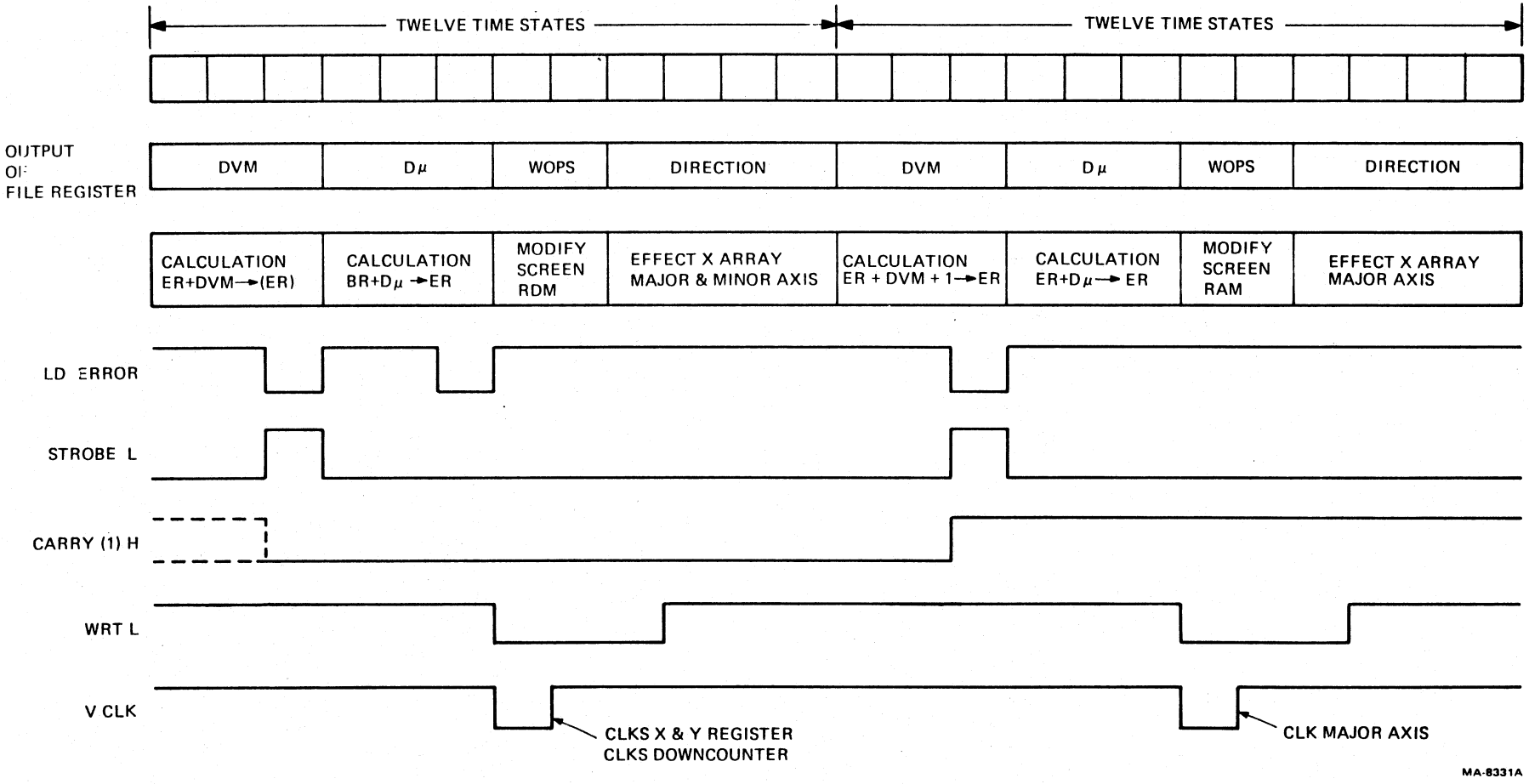


Figure 6-70 Arbitrary Vector Timing

- *WOPS (Write Operations) Time* – The modified data bits are written into the bit map location specified by the X and Y counters.

  The direction ROM circuit produces INHIBIT WRITE L, which must be high for the write control to write to the bit map. There are three conditions that prevent a write operation from occurring.

  1. Do not write in direction 2 from an odd line or 6 from an even line.

  2. Do not write if the direction is 5 or 7, the scan line is even (Y0), and the last direction was 6.

  3. Do not write if the direction is 1 or 3, the scan line is odd, and the last direction was 2.

- *Direction Time* – The outputs of the direction register, bits F3 – F0, are inputs to the direction ROM. An arbitrary vector is drawn in direction 3 when the input bits of the direction ROM equal B (hex). The direction ROM input bits F0 – F2 determine the direction affected. Direction 3 is a negative direction. If the carry bit is a 1, only the major axis counter is decremented. If the carry bit is a 0, both the major and minor axis counters are decremented.

  The vector sequence ends when the V clock signal clocks the down counter to 0. This resets the GO flip-flop.

6.7.5 Bit Map Write Control

The vector generator computes the series of memory locations that make a vector. The bit map write data generator controls the data stored for each pixel in the vector. The appearance of a pixel is controlled by two groups of data.

1. Information stored in two planes at the pixel location

2. Information stored in four locations in the output map (section 6...).

Each pixel has 2 bits of information, and those 2 bits select one of the four output map locations during screen refresh.

A multifunction circuit under microprocessor control selects one of the four combinations of two bits to write for each pixel. Briefly, after the vector generator computes a pixel location, the current contents of the location are read. Depending on the user's write mode, the contents are logically combined with one bit of a pattern and the results are written back to the current location.

6.7.5.1 Block Diagram – The bit map write control circuit has the following parts (Figure 6-71).

Two 1-of-12 selectors (one for each plane). Data always comes from each bit map plane 12 pixels at a time. When the vector generator addresses the bit map, the bottom four bits of the address select the desired pixel data.

Write control RAM. Eight locations hold 2 bits each. The microprocessor loads the RAM before the vector operation according to the user's write mode. The RAM addresses are 2 bits of the current pixel from the bit map, and 1 bit from the pattern register. See the *VT125 User Guide* for a complete description of the operation of the Custom Writing Control. (The IC has 16 locations of 4 bits each. The VT125 uses only 8 locations and stores only 2 data bits. Each data bit is in 2 bit locations so the IC can drive all 24 bit map ICs.)

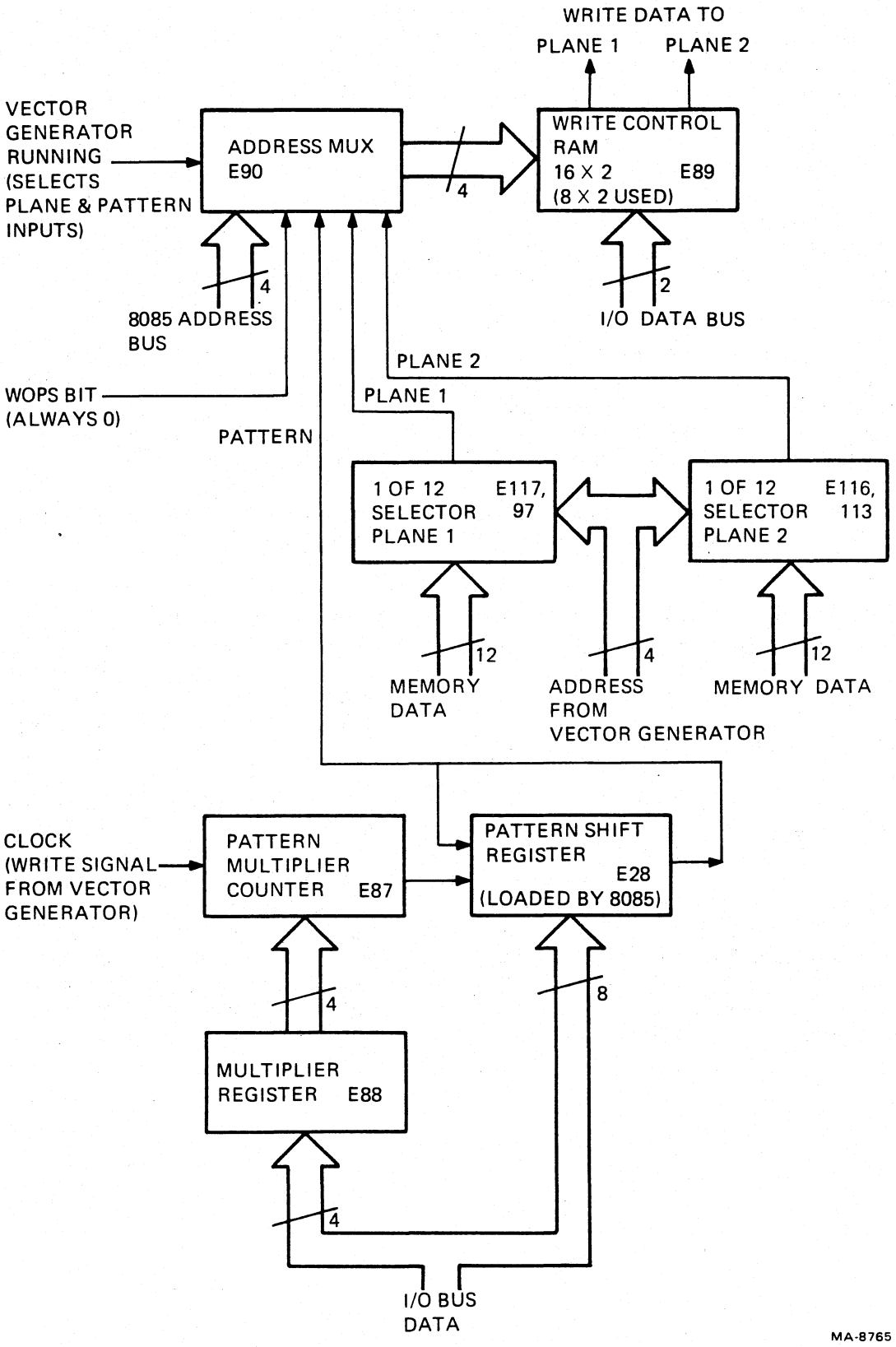


Figure 6-71 Bit Map Write Control Block Diagram

Address multiplexer. When the vector generator is not running, the multiplexor connects the low 4 address bits of the microprocessor bus to the write control RAM. The microprocessor uses the bus addresses to load the RAM according to the user's write mode. When the vector generator is running, the multiplexor connects 2 bit map data bits and 1 pattern register bit as addresses; the multiplexer uses these addresses to read data from the write control RAM to write to the bit map.

Pattern register. The microprocessor loads a pattern into an 8-bit shift register. Each pixel that the vector generator addresses uses 1 pattern register bit as part of the write control process. When the pixel is written, the write pulse to the bit map shifts the register (or increments the multiplier counter, below). The default pattern for vectors is all 1s. The output of the shift register goes to its input so a vector longer than 8 pixels gets a wraparound version of the starting pattern. When a character is drawn, the pattern loaded into the shift register varies according to which scan of the character is drawn.

Pattern multiplier counter. Each bit map write pulse is a clock input for the multiplier counter. The microprocessor loads the counter with a starting count when it loads the pattern register; the pattern register reloads itself with the starting count at the end of each count. If the pattern multiplier is 1, then each count gives an output and shifts the pattern register. Larger pattern multipliers delay shifting the pattern register until the count finishes. This makes the displayed pixel appear wider.

Multiplier register. The microprocessor loads this register with the multiplier value. The register holds the value for loading into the pattern multiplier counter after every finished count and at every pattern register load.

6.7.5.2 Character Writing – Writing a character into the bit map is like writing a vector with the pattern register and pattern multiplier. The ReGIS text command translates an ASCII character code into a set of dot patterns. To do this, the microprocessor reads a character look-up table located in memory. The look-up table consists of a series of character cells, one cell for each ASCII code. Each character cell contains ten 8-bit bytes of pattern data to write as vectors. These pattern vectors compose the character in the bit map and on the screen.

Figure 6-72 shows both the vector generator and pattern register operations for a size 1 character. Each character scan is one short vector drawn with pattern data loaded from the stored information for that scan. When a character is larger than size 1, Figure 6-73 shows the pattern multiplier action. For a size 2 character, the pattern multiplier counts twice before sending a shift clock to the pattern register. Therefore, two sequential pixels have the same data. The vector generator draws lines that are twice as long so all the data can be displayed. The microprocessor counts the number of scans drawn with the same pattern data. For size 2, it loads the pattern register with the next scan of character cell data after two identical scans. Each of these parameters (vector length, pattern multiplication, pattern repetition), plus others such as vector direction, can be controlled with ReGIS commands. The *VT125 User Guide* has complete descriptions of the commands.

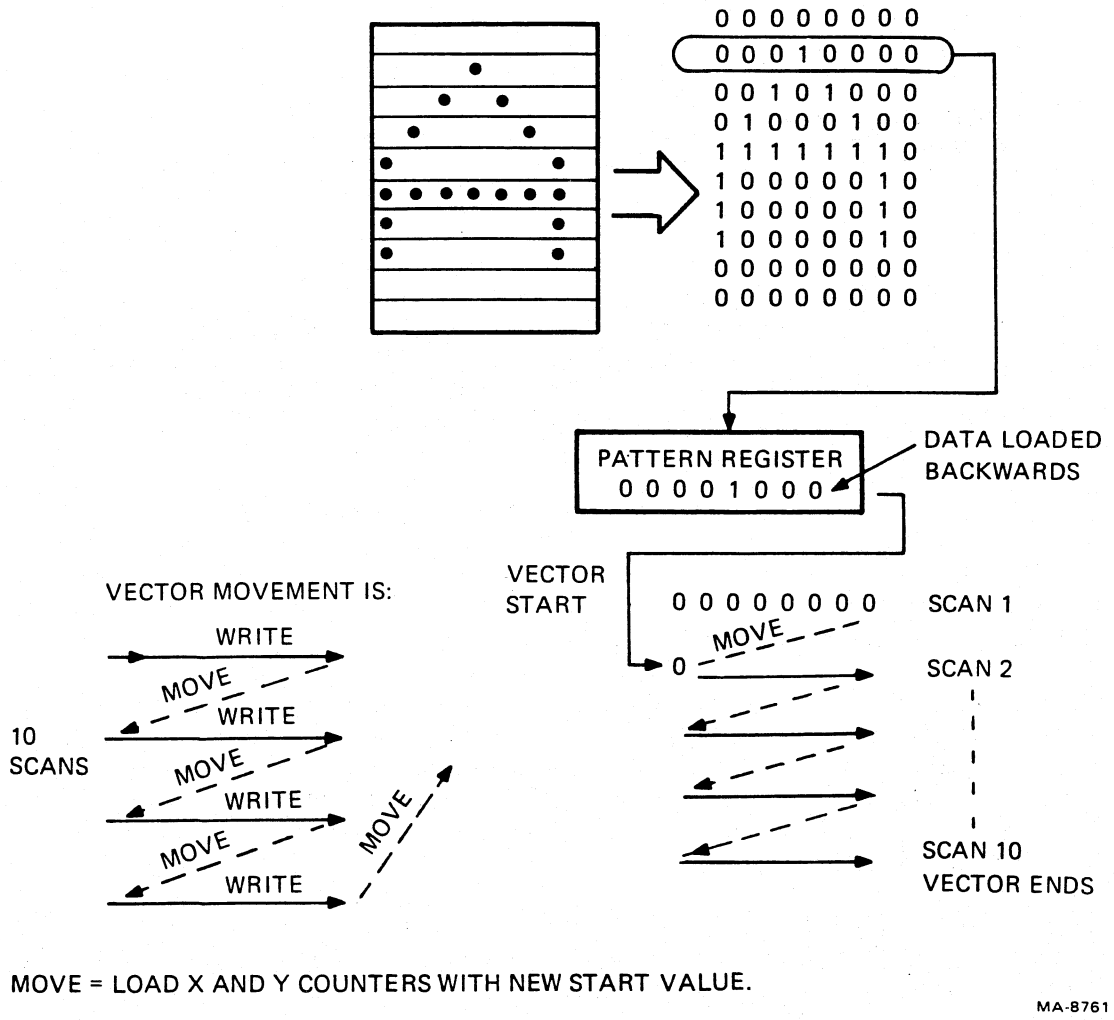


Figure 6-72 Draw a Character

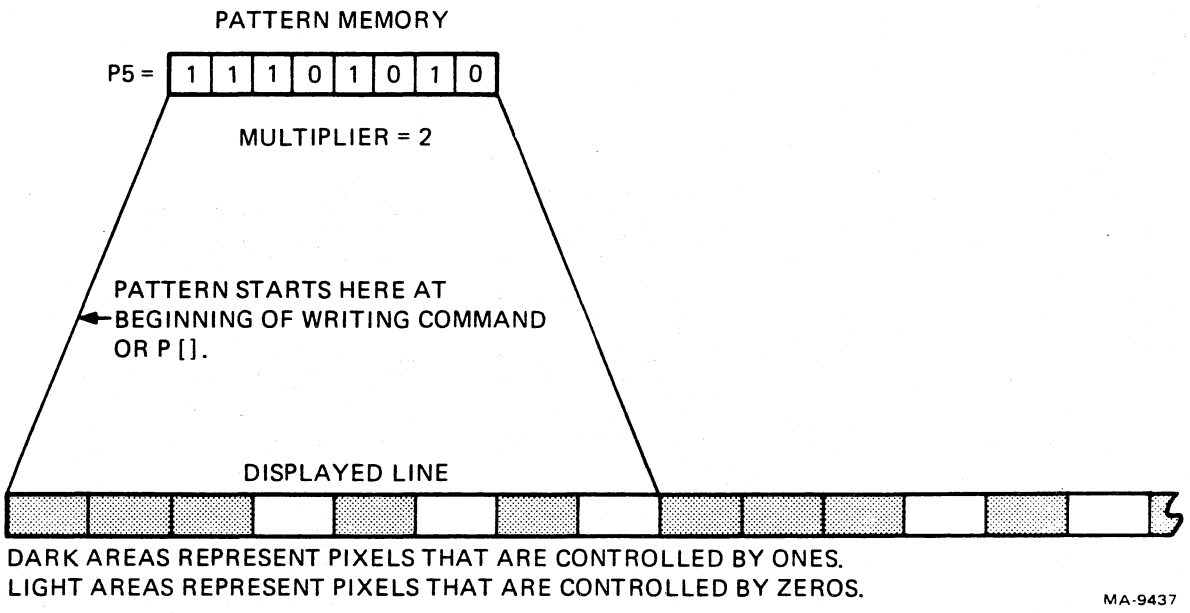


Figure 6-73 Pattern Memory and Multiplier

6.7.6 Bit Map Memory

The bit map has the following parts (Figure 6-74)

Two planes of memory. Each plane is twelve 16K X 1 DRAMs arranged in four rows of 3 DRAMs each. One RAS signal controls each row. For any bit map read, all 4 RAS signals go low at the same time to access all 12 DRAMs. (One CAS signal is common to all the DRAMs.) For a bit map write, only the RAS for the addressed row goes low. There are three write signals to drive three columns of DRAMs. Only the write signal for the addressed DRAM goes low. The intersection of one RAS signal and one write signal is only one DRAM.

Write select/disable circuit. This is a ROM that decodes address inputs to select the group of DRAMs that receive a write signal. If an address would write to a location that is not in the plane, the circuit disables all write outputs. (Such addresses occur when the graphics processor computes a graphic object that overlaps the margins of the display.)

Row/column address multiplexer. This multiplexer is controlled by the WR/RD signal and selects the source of addressing for the bit map. For most write operations, the bit map addresses come from the X and Y multiplexer, supplied by the X and Y position counters in the vector generator. For read operations, the bit map addresses come from the H and V multiplexer, supplied by the horizontal and vertical counters in the timing circuits. Each set of counters provides a total of 14 address bits. RAS TIME high selects one group of seven address signals, while RAS TIME low selects the other group.

The address lines on the multiplexers are scrambled to guarantee refreshes often enough for all the DRAMs. Each raster takes 16.7 ms, but refreshes must be less than 2 ms apart. Therefore, the address lines are arranged so that sequential addresses jump among all DRAMs at least eight times per raster. Then the vector generator address lines are scrambled in the same pattern so a given address on either side of the multiplexer always accesses the same bit. This scrambling method means the RAMs themselves do not have to reflect the H and V orientation of the counters, provided that there are enough unique addresses to cover the screen area. So a bad memory IC does not give a simple pattern on the screen, although a bad shift register line does.

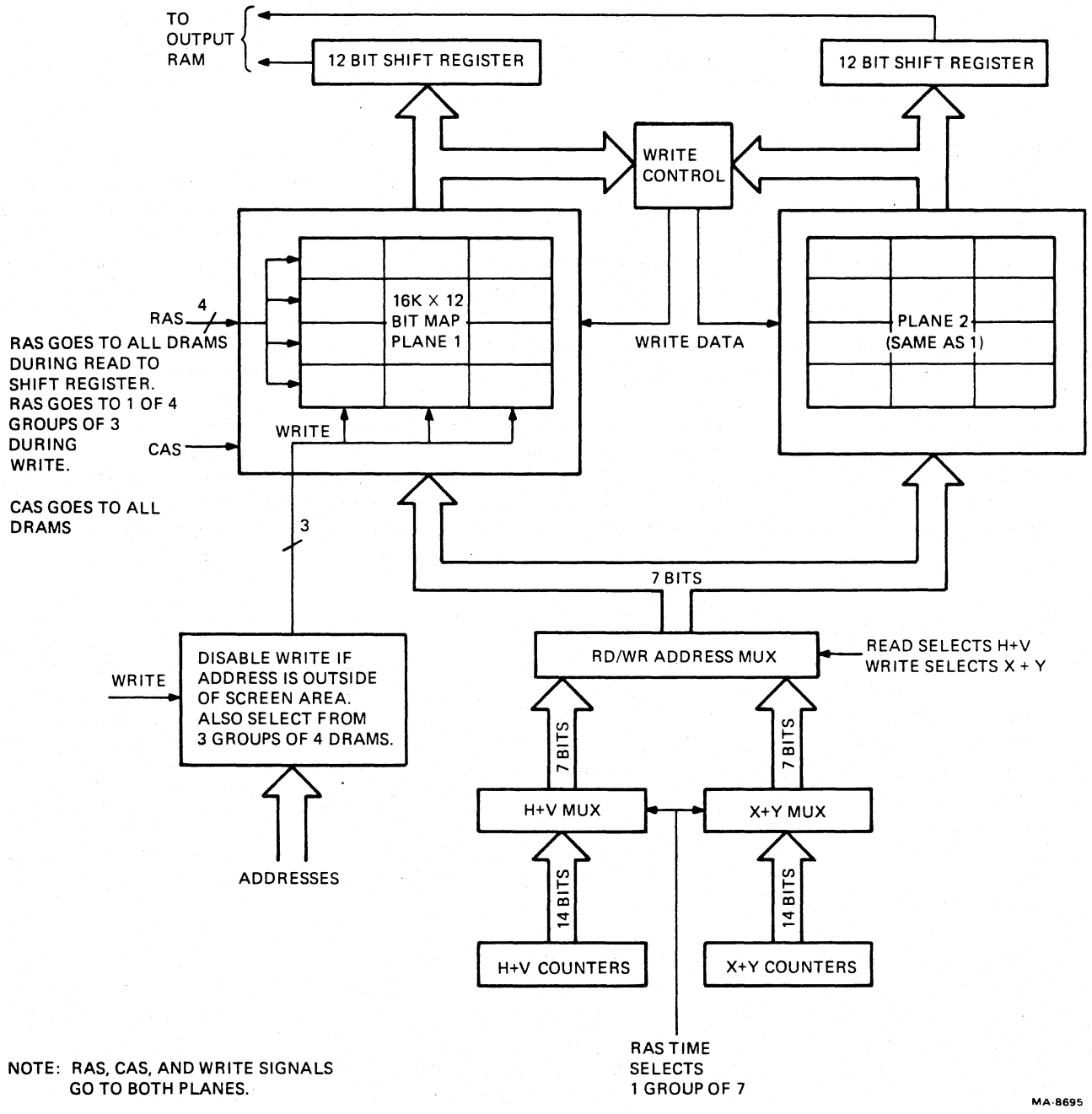


Figure 6-74 Bit Map

Bit map output shift registers. With each bit map read cycle, each memory IC puts 1 bit on its output. The IC outputs for each plane connect directly to the inputs of three 4-bit shift registers. When LD/SHIFT is high, it strobes the inputs into the registers. The right bit in each register appears at the shift output while LD/SHIFT is high. LD/SHIFT is high for one pixel time; this means the first bit appears on the screen at LOAD time, then the other 11 bits shift onto the screen with the shift clock while LD/SHIFT is low.

6.7.7 Output Map

The VT125 displays color and brightness by addressing one of four preset values for each pixel on the screen. The VT125 can display each pixel on the screen with a different hue, lightness, or saturation. However, it can only use four different colors at one time. That is, any pixel can differ from its neighbors, but only four different colors can appear on the screen at one time. This is the tradeoff that the VT125 makes in its memory usage: rather than displaying many different colors at one time but only allowing changes at fixed boundaries that are larger than the pixel size (as in the VK100, which can change only at 12-pixel horizontal boundaries), the VT125 displays a limited set of colors at any one time but allows changes to occur at any boundary down to the individual pixel dimension.

The VT125 displays color and brightness with a bit map memory and an output map. The bit map memory has the same number of addressable locations in it as the writable addresses of the screen display (768 × 256). However, for each addressable location, there are two bits of data. Think of these pairs as existing in two separate but closely connected planes of addressable locations (Figure 6-75). The pairs of bits can be written either one at a time or together. (See Writing Controls in the *VT125 User Guide.*) They represent the four numbers 0, 1, 2, and 3 when their binary values are decoded.

The four numbers are the addresses of four output map locations. Each output map location is 1 byte of a 4-byte RAM. When the graphic memory is displayed, each pixel in the bit map requests that the information in one of the output map locations be sent to the digital to analog converters (DAC). The DACs convert binary data into drive levels for cathode ray tube (CRT) gun drives. Each output map byte has 2 bits for the monochrome monitor in the VT100 part of the terminal (representing four levels of intensity on the monitor screen: dark, dim, normal, bold). Each output map byte also has 2 bits for each of the color guns in the external or alternate RGB color monitor. These bits represent four levels for each of the colors, or a total of 64 different values of hue, lightness, and saturation (HLS). (RGB is required because the National Television Standards Committee (NTSC) color standard does not provide enough bandwidth to display color changes on individual pixels.) You can set the information in each output map by using the mapping command with either RGB, letters, or HLS specifiers. (See the Screen Output Map Definition in the *VT125 User Guide.)*

6.7.8 Output Latches and DAC Converters

Each time a pixel is output from the bit map shift registers, its 2 bits (SHIFT DAT A and B) address a location in the output RAM (E58 and E46). The next SHIFT CLK strobes the data from the addressed location into latches E91 and E94. The data stays in the latch while the RAM is addressed by the next pair of data bits. The latch provides a stable signal to drive the digital to analog converters (DACs). The DACs are open collector inverters that provide paths to ground resistors in the base circuits of the video drive transistors.

Using the green output as an example, reducing the voltage on Q4's base causes more current to pass through Q4 and R77. R77 is the output load resistor; as more current passes through R77, the voltage across it increases. A CRT connected to that voltage gets brighter as the voltage increases. One way to reduce Q4's base voltage is to connect a resistor from the base to ground. The added current through R75 causes a voltage drop at the base. The DAC has two different resistors connected in parallel between the base and common. These resistors are in series with switches (the inverter output transistors) that can disconnect the resistors, or connect one or both resistors, to common. The resistors have different values, so there are four possible voltages at Q4's base. Two bits from the output RAM are inputs to the two inverters (E100) for each color plus the monochrome output.

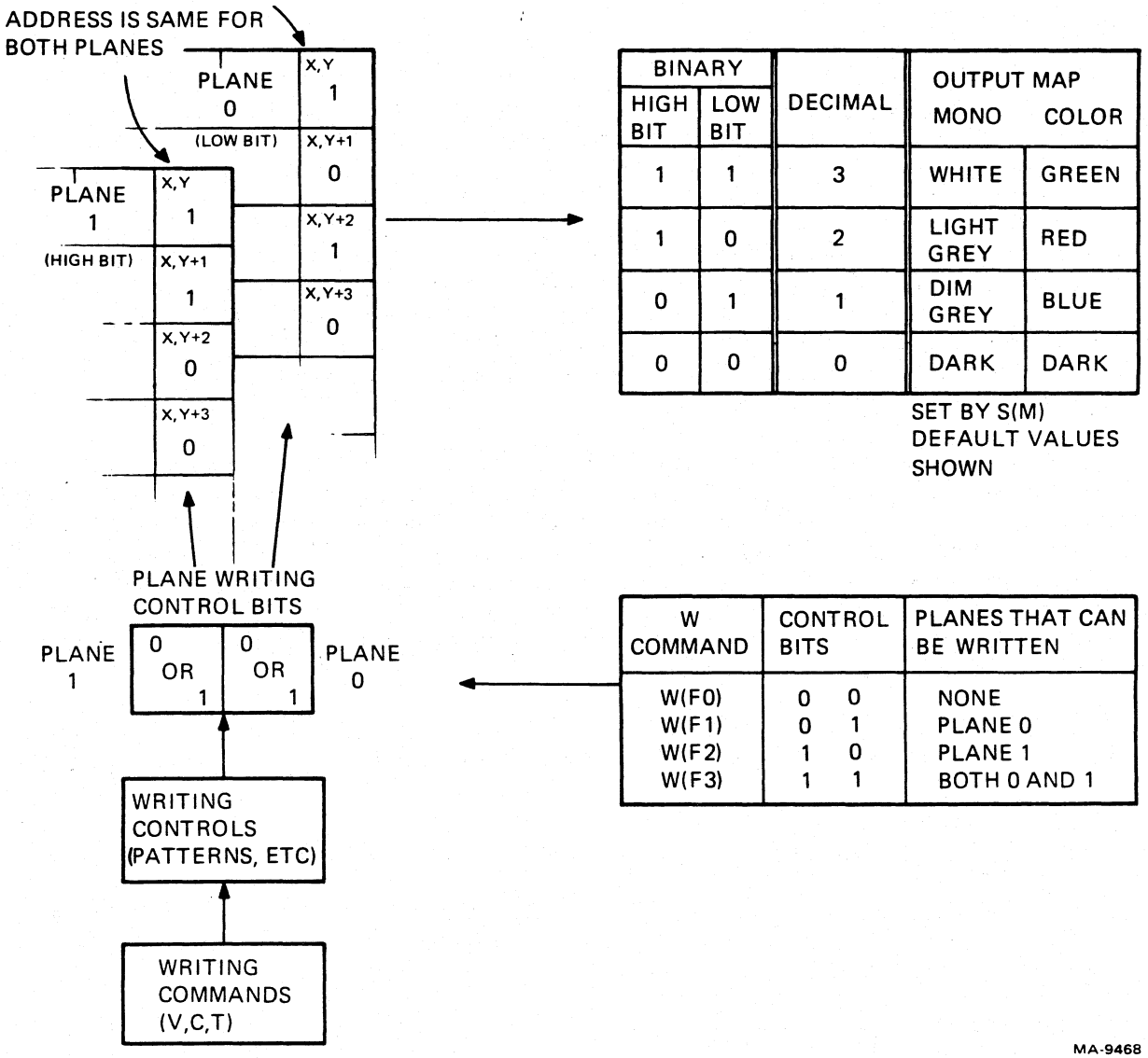


Figure 6-75 Bit Map Planes and the Output Map

6.7.9 STP Board

The STP board (also called paddle board) holds the serial interfaces for the terminal. The interfaces are made of UARTs, a baud rate generator, address decoders, and EIA line drivers and receivers. A switch pack on the board selects the connectors used for the computer port and baud clock sources for two of the UARTs.

6.7.9.1 UARTs – UART E3 communicates between the VT100 terminal controller and the graphics processor. The typical switch setting configuration has the clock for both receive and transmit on E3 coming from a fixed rate signal on the terminal controller (A18-1). The same fixed rate signal returns to the terminal controller UART on A14-2 and A15-2 to drive the internal communications lines at the same fixed rate.

UART E8 communicates between the VT125 graphics processor and the communications port. Its receive and transmit clocks come from the terminal controller through the STP connector (A14-1 and A15-1). These clocks are controlled by the bud rate generator on the terminal controller. If the STP connector does not have a board plugged in, these clocks return to the UART on the terminal controller. But with the STP board installed, these clocks control communications with the host computer and can be set with the SET-UP B controls.

UART E11 communicates between the VT125 graphics processor and the auxiliary port (also called the printer port). This port is more flexible than a printer port because the graphics processor allows full two-way communications over it. For example a digitizing tablet can be connected to it, given host software support; for this reason the words *Auxiliary Port* are used in the VT125 documentation. A baud rate generator provides the baud rates for UART E11 on the STP board. The baud rate generator is the same type on the terminal controller. Switches are set to drive both UART clock inputs from the same generator output, but firmware controls the use of the dual generator. The UART speed and number of bits are set in SET-UP B, switch group 5.

All three UARTs have their receiver ready lines ORed together, and their transmitter ready lines ORed together. The two ORed outputs go to microprocessor interrupt inputs on the graphics processor board.

6.7.10 Firmware

The VT125 firmware includes several sections. The next paragraph describes some of them.

6.7.10.1 Memory and I/O Addresses – The VT125 has 24K bytes of firmware in ROM in addresses 0000H to 5FFFH, with 8K more unused ROM space from 6000H to 7FFFH. The RAM has 16K bytes in addresses 8000H to BFFFH.

The I/O addresses are listed in Table 6-4.

6.7.10.2 Self-Test Processes – The VT125 has verification and diagnostic tests available. ANSI control functions invoke the tests. Some of the tests are VT100 specific, and others are VT125 specific. This section describes the actions of the tests.

VT100 Self-Tests

The VT100 performs all power-up tests (CPU, ROM, RAM, AVO) as usual when you power up or reset (SET-UP 0) the terminal. The VT100 power-up/reset sequence invokes the VT125 power up-test.

You cannot run the VT100 data loopback and EIA modem loopback tests unless you remove the VT125 STP board.

If the "infinite loop" VT100 self-test is invoked from the VT100 keyboard in local mode or if the VT100 escape sequence is sent from a host through the VT125, only the VT100 tests are repeated. Under these conditions, any resulting VT125 tests are meaningless.

Table 6-4 I/O Addresses and Data

Command	Address
Load X Position Register Low Byte	80H
Load X Position Register High Byte	90H
Load Y Position Register Low Byte	A0H
Load Y Position Register High Byte	B0H
Load Error Register	C0H
Load Pattern Register	13H
Load Pattern Multiplier	14H
Clear CLOCK SHIFT Glitch Flag	15H
Load Dμ Register	F0H
Load DVM Register	F1H
Load Direction Register	F2H
Load WOPS Register	F3H
Execute Move Operation	00H Start Data = 01H
Write Dot	01H
Execute Vector Write	02H
Execute Screen Erase	03H
Load Horizontal Minor Offset	10H
Load Horizontal Major Offset	11H
Load Vertical Offset	12H
Load Output RAM (four starting at:)	18H
Load Write Control RAM (8 starting at:)	D0H
Read System Status	20H
VT100 UART Data (R/W)	0EH
VT100 UART Control (R/W)	0FH
Computer UART Data (R/W)	0CH
Computer UART Control (R/W)	0DH
Auxiliary Port UART Data (R/W)	0AH
Auxiliary Port UART Control (R/W)	0BH
Load Auxiliary Port Baud Rates	08H

VT125 Self-Tests

Power-Up Tests – These tests occur whenever you power up or reset the terminal. See Paragraph 6.8.2 for an explanation of error reports.

1. CPU register test – This test verifies that the basic CPU register operations work. If this test fails, the microprocessor tries to flash an error code on the monochrome monitor.

2. ROM checksum test – A checksum is stored in each 4K bytes of ROM (2 for every 8K bytes). The checksum is computed by this procedure: Shift and XOR each byte, starting with an initial value of high ROM address byte + 1; the result should be zero. If this test fails, the microprocessor tries to flash an error code on the monochrome monitor and an encoded ROM number on the color monitor.

3. RAM test – This test performs a worst-case read/write check of all 16K bytes of program RAM. If this test fails, the monochrome monitor flashes an error code and the color monitor flashes an encoded RAM bit number.

4. Vertical sync timeout – This test checks that the vertical sync signal appears repeatedly within approximately 25 ms. If this test fails, the monochrome monitor flashes an error code.

5. Vector timeout – This test checks that none of the vectors drawn in either the bitmap RAM test or the vector generator test take longer than 100 ms. If this test fails, the monochrome monitor flashes an error code.

6. Partial video bitmap RAM test – This test checks that every bit tested in both video bitmap planes can be written to both 1 and 0. This partial test only tests the first eight scan lines of video bitmap RAM; you can test the entire RAM on request. If this test fails, the microprocessor tries to display the message "VT125 BM Error".

7. Vector generator tests – This tests the basic vector functions by drawing a test pattern into the upper-left corner of the display, then verifying it against a predetermined pattern. If this test fails, the microprocessor tries to display the message "VT125 VG Error".

8. Communications test – This test verifies the VT100-to-VT125 communications link by requesting the terminal status from the VT100. If this test fails, the microprocessor tries to display the message "VT125 IC Error". If the VT100 is LOCAL, the message "VT125 Offline" appears on the display.

Requested Tests – The following tests require operator participation, and can only be invoked with the DECTST escape sequence sent to the VT125. (See Paragraph 6.7.)

1. Data loopback test – This test requires an external loopback connector on the host communications port. The test only verifies data leads, and only at the speed selected by the VT100. If this test fails, the message "VT125 EC Error" appears.

2. Printer port loopback test – This test requires an external loopback connector on the printer EIA port. This tests data lines on the printer EIA port. If this test fails, the message "VT125 SC Error" appears.

3. Display test – This test requires operator visual verification. The test cycles through the four intensity levels of each of the three primaries and white, thereby testing the color output RAM.

4. Entire video bitmap RAM test – This test checks that every bit in both video bitmap planes can be written to both one and zero. If this test fails, the microprocessor tries to display the message "VT125 BM Error".

6.7.10.3 Graphics Protocols – The VT125 has three different graphics protocols. Control sequences in the data select the protocol.

ReGIS (remote graphics instruction set) is a graphics descriptor that uses high-level commands to construct basic graphics objects such as lines and curves. Except for the ANSI device control string mechanism for turning graphics on and off, all ReGIS commands use printable ASCII characters and decimal numerical values for option selection and pixel location specifications.

VT105 emulation provides most of the functions of the VT105 graphics terminal for compatibility with existing software. The VT105 has a few built-in processes such as shading and strip charting. Its pixel locations need binary specifications from software in groups of ASCII characters selected for their combined bit patterns.

DECwriter graphics is a protocol for transmitting the complete contents of a bit map. It uses ASCII characters selected for their bit patterns. In the VT125, DECwriter is two different protocols. One protocol converts the VT125 bit map into ASCII characters for transmission to a DECwriter graphics terminal. The other protocol writes incoming DECwriter graphics data into the bit map.

6.7.10.4 Communication Protocols – The VT125 is a complex device that has several separate processes operating at the same time to provide graphics and text over a simple terminal communication line. Figure 6-76 shows a general block diagram of the VT125, divided into two main functional blocks: the graphics processor and the VT100 text terminal that holds the graphics processor. The figure shows two important facts.

1. The keyboard communicates only with the VT100, so LOCAL operation can only cause actions in the VT100, not in the graphics processor.

2. The graphics processor manages all communications between the computer and the VT100, and always uses XON/XOFF. (This SET-UP feature cannot be turned off.)

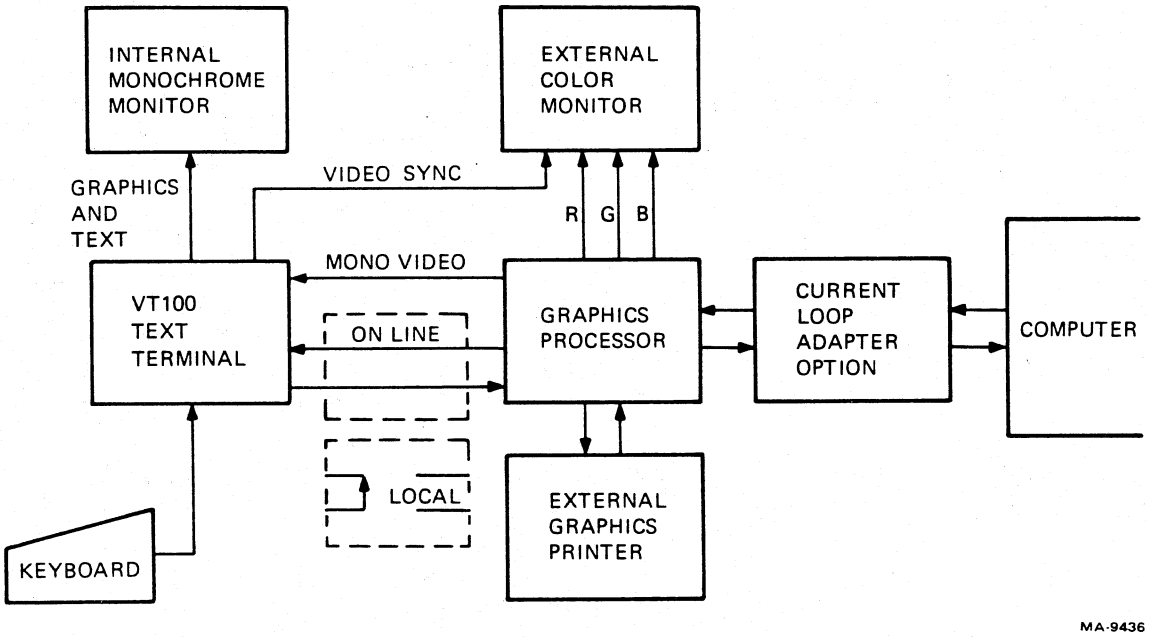


Figure 6-76 VT125 General Block Diagram

Figure 6-77 is a more detailed look at the communication structure in the graphics processor itself. This shows the buffers included for each of the three bidirectional communication ports in the graphics processor. The dispatcher is many processes. It controls the buffers with XON/XOFF. It sets up the data paths from each sending port to each receiving port. And it passes all communications according to ANSI X3.64-1979. That is, it examines data from all ports for instructions to itself. It passes anything that does not apply to the graphics processor to the ports set to receive the data from that source. Among the ports controlled by the dispatcher are the selection of the graphics protocol under ANSI sequence control. The choices in that block of the diagram are ReGIS, VT105 emulation, and DECwriter graphics. The following five figures show the internal connections that are set up for different applications.

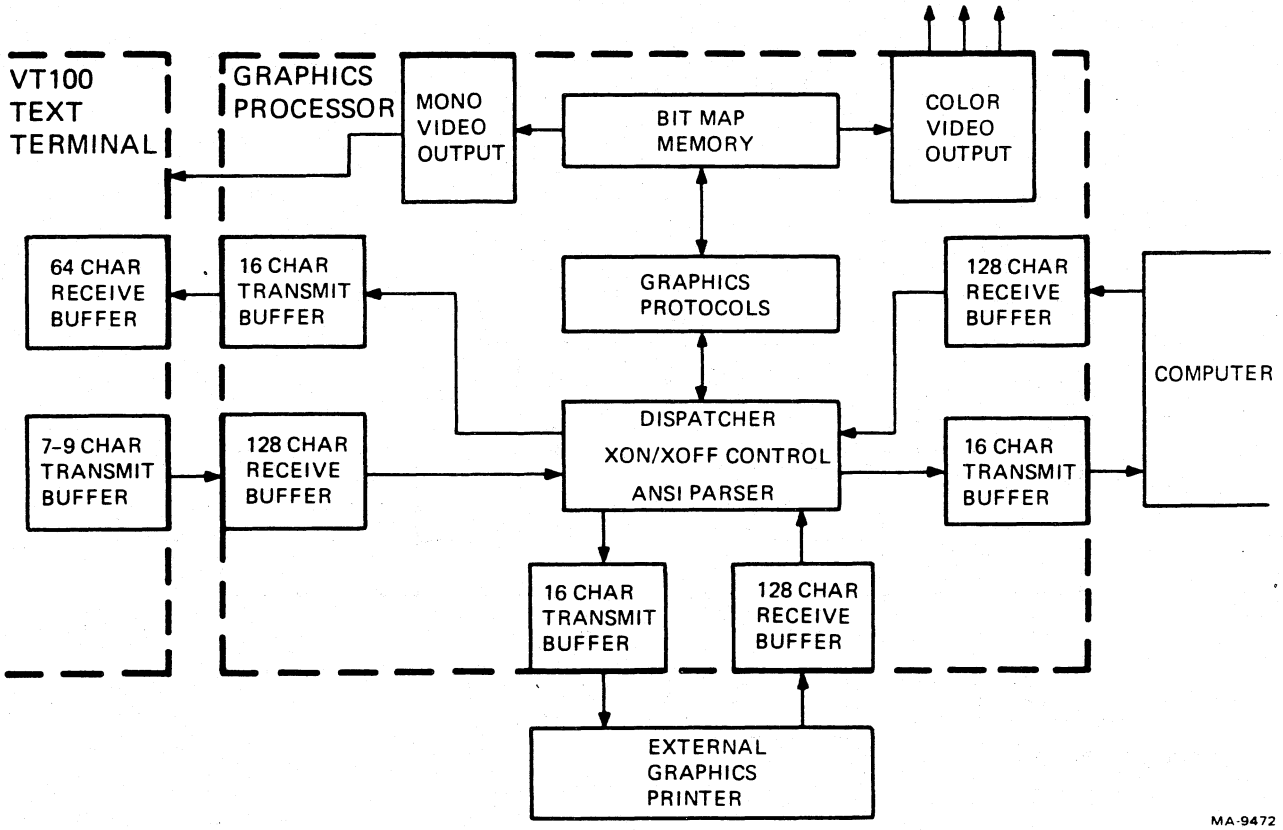


Figure 6-77 VT125 Data Paths

Figure 6-78 shows the VT125 operating as a text-only terminal. If you send XOFF from the keyboard, either by pressing **NO SCROLL** (if AUTO XON/XOFF is on) or by holding down **CTRL** and pressing **S**, the receive buffer in the VT100 fills to the 32-character mark. Then the VT100 sends XOFF to the graphics processor. When the 16-character transmit buffer in the graphics processor fills, it sends XOFF to the dispatcher; then the 128-character receive buffer fills to its 48-character mark. At that point (80 characters later) the graphics processor sends XOFF to the computer.

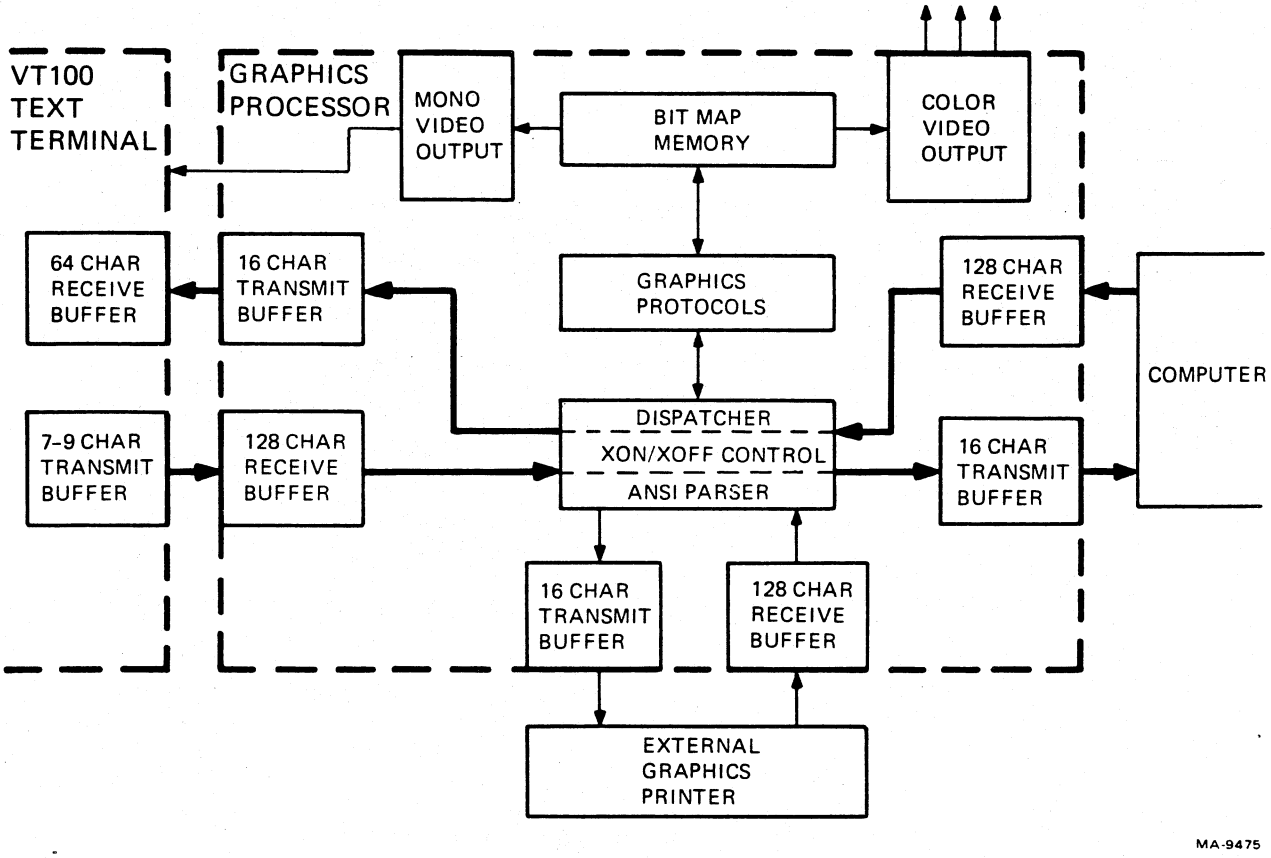


Figure 6-78 VT125 as a Text-Only Terminal

Figure 6-79 shows the VT125 operating as a graphics terminal. A device control string is being sent to the terminal from the computer. The terminal may be in any protocol: ReGIS, VT105, or DECwriter graphics. The keyboard can communicate with the computer, but any screen response to keyboard commands is under the control of the computer's programming.

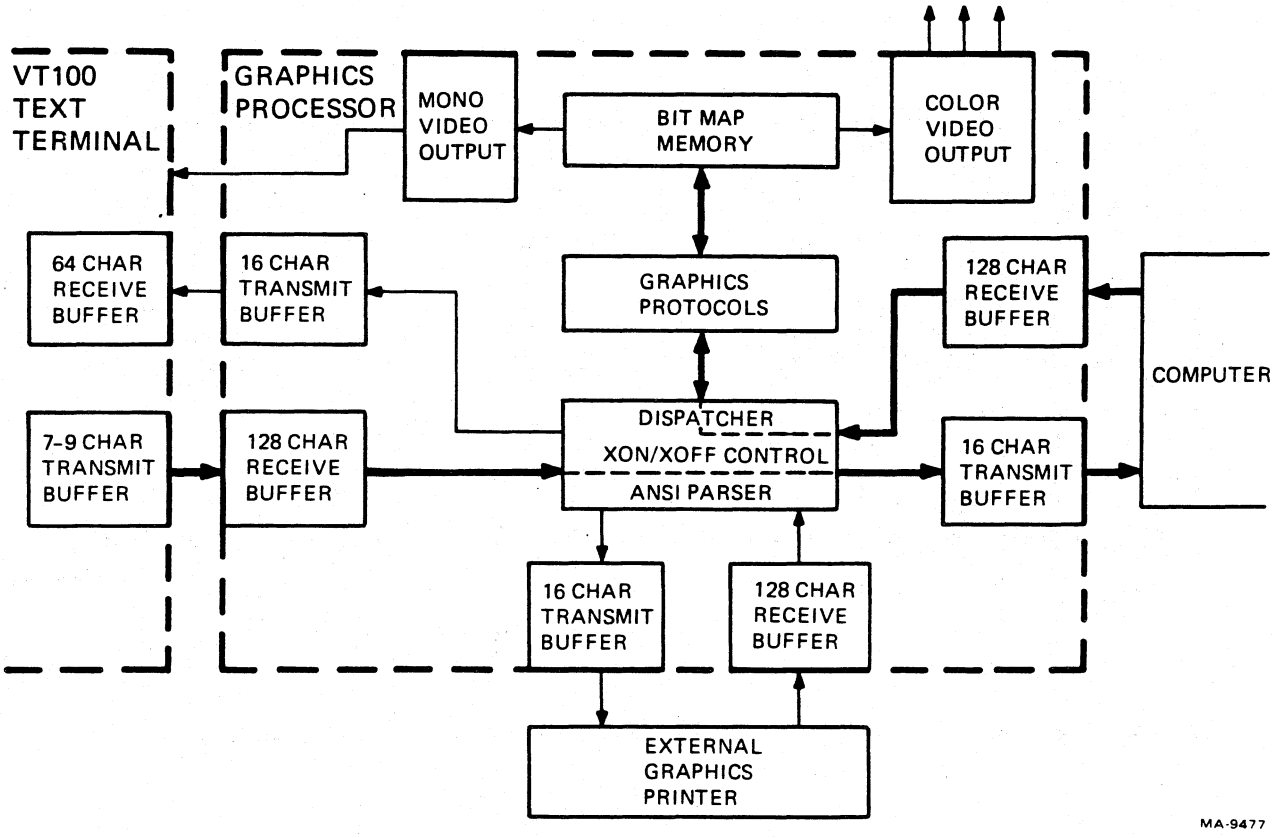


Figure 6-79 VT125 in a Graphics Terminal

Figure 6-80 shows the VT125 operating as a graphics terminal. A device control string is being sent to the terminal from the computer. The graphics protocol commands are being displayed on the screen at the same time. This is a feature of VT125 ReGIS and is not available with the other protocols. The keyboard can communicate with the computer, but any screen response to keyboard commands is under the control of the computer's program.

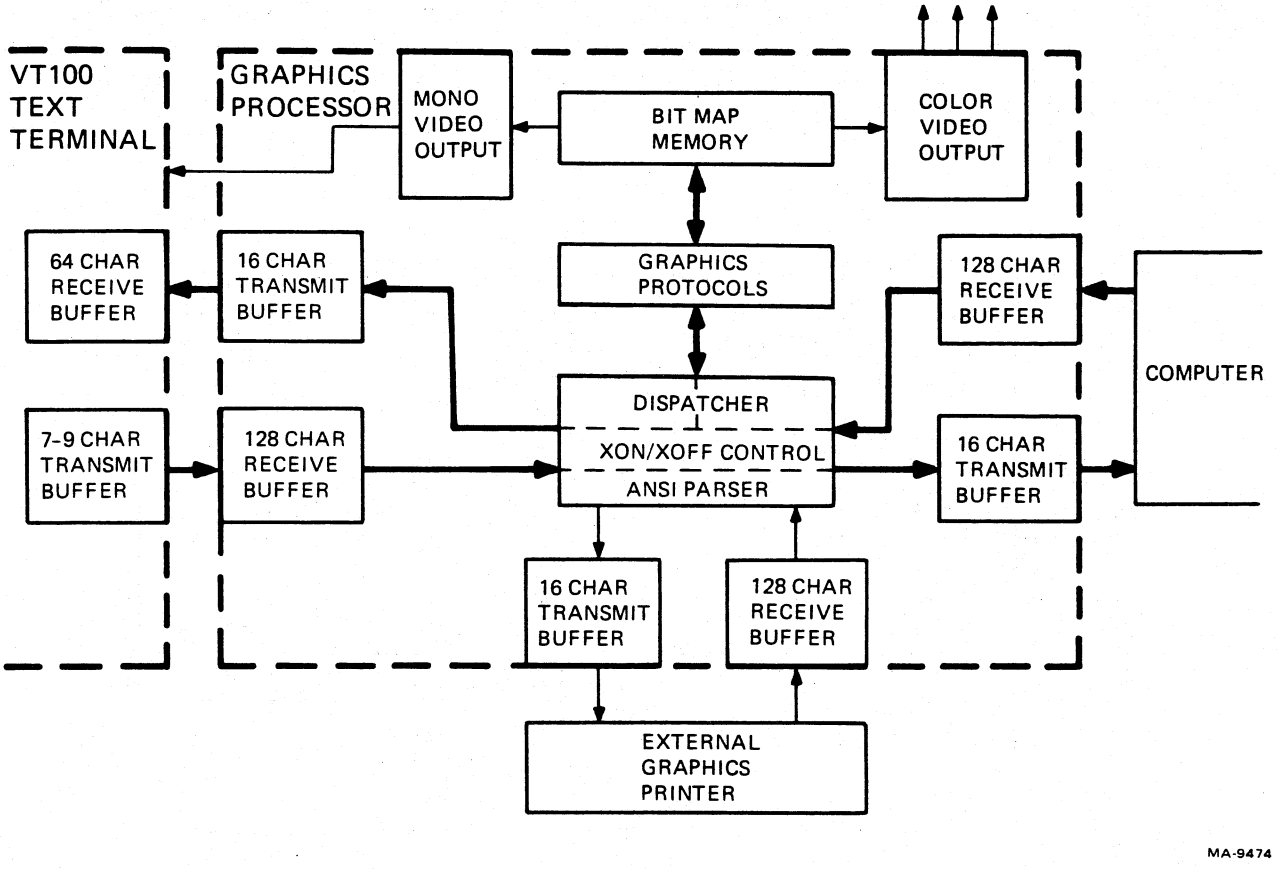


Figure 6-80 VT125 in ReGIS Graphics with Commands on Screen

Figure 6-81 shows the VT125 printing from the screen to the optional graphics printer in DECwriter graphics protocol. This is the result of the screen hardcopy command in ReGIS. The keyboard can communicate with the computer, but the computer cannot communicate with the dispatcher until the print operation is complete. However, if a graphics off command (string terminator: ESC \) immediately follows the hardcopy command, the computer can communicate with the dispatcher during the print operation.

Figure 6-82 shows the VT125 printing from the computer to the optional printer. This is the result of the ANSI media copy command from the computer. The media copy command can turn the VT100 and auxiliary (printer) ports on and off. Therefore, the screen can display the data going to the printer if desired. To print a stored DECwriter graphics protocol file, display it on the screen and use the ReGIS hardcopy command to print it.

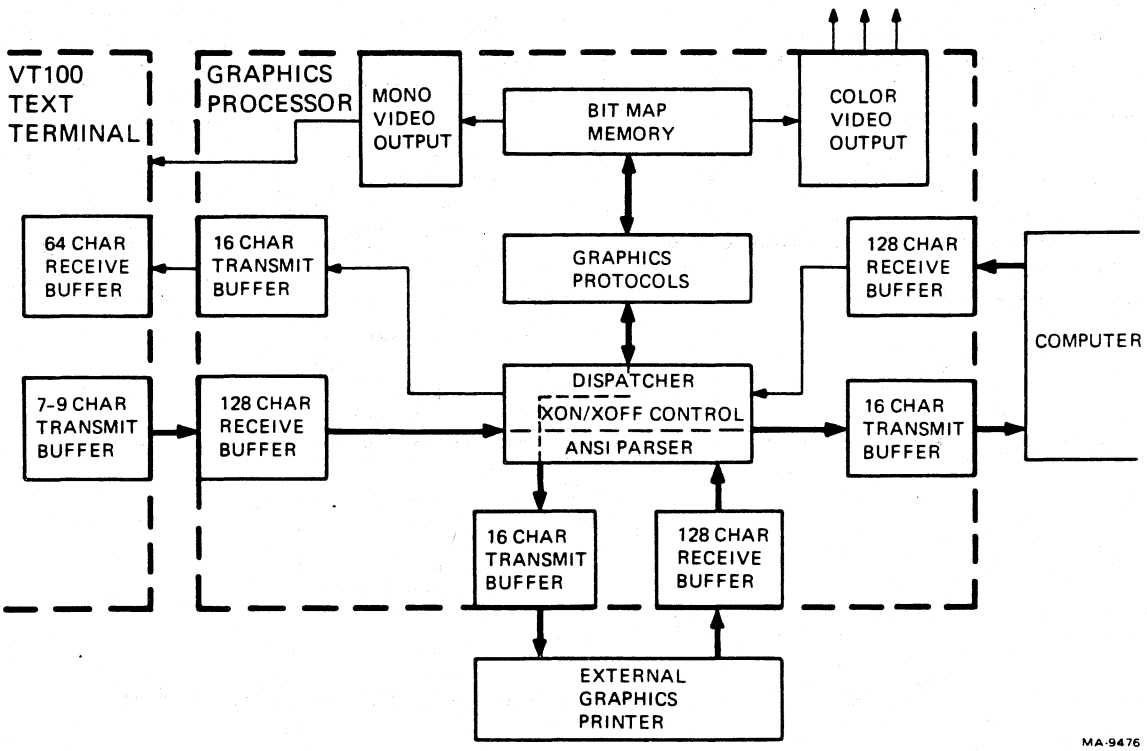


Figure 6-81 VT125 Printing from Screen

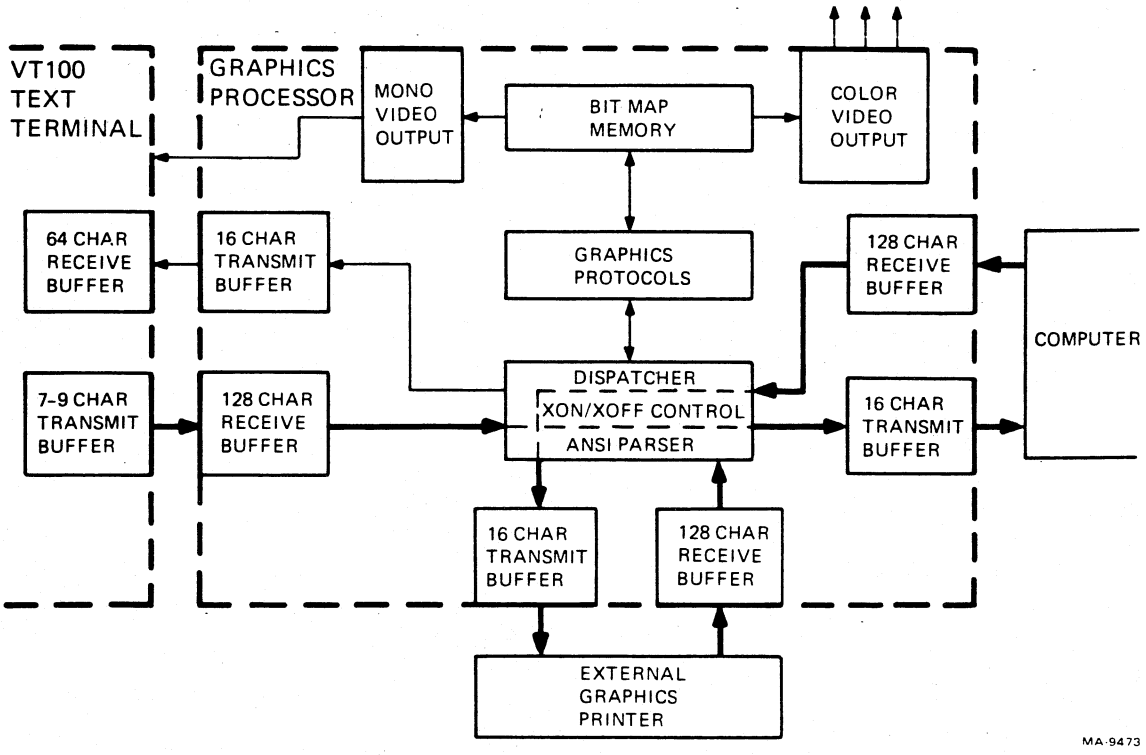


Figure 6-82 VT125 Printing from Computer

6.8 VT125 TESTING AND TROUBLESHOOTING

This section explains the VT125 testing and troubleshooting procedures.

6.8.1 Preparing for Self-Tests

Use this procedure to prepare the terminal for all self-tests except a single power-up test.

1. Turn the power switch off.
2. Disconnect the communication cables from the computer and auxiliary data ports. The computer port communication cable may be either EIA or 20 mA.
3. If a cable is connected to the EIA computer port connector, install an EIA loopback connector on the EIA connector. See Figure 6-83. The EIA loopback connector part number is 12-15336. One loopback connector is shipped with the terminal or upgrade kit.
4. If a cable is connected to the 20 mA connector, the 20 mA current loop adapter option is installed. Install the loopback connector (PN 70-15503-00) included with the option. Do not use the EIA loopback connector at the same time as the current loop connector.
5. To perform the auxiliary port tests, install an EIA loopback connector on the auxiliary port connector. If the communication port is EIA, you need a second EIA loopback connector.
6. Turn the power switch on.
7. Make sure the terminal is ON LINE, with the ANSI/VT52 SET-UP B feature set to ANSI (SET-UP B switch 2-3 = 1).

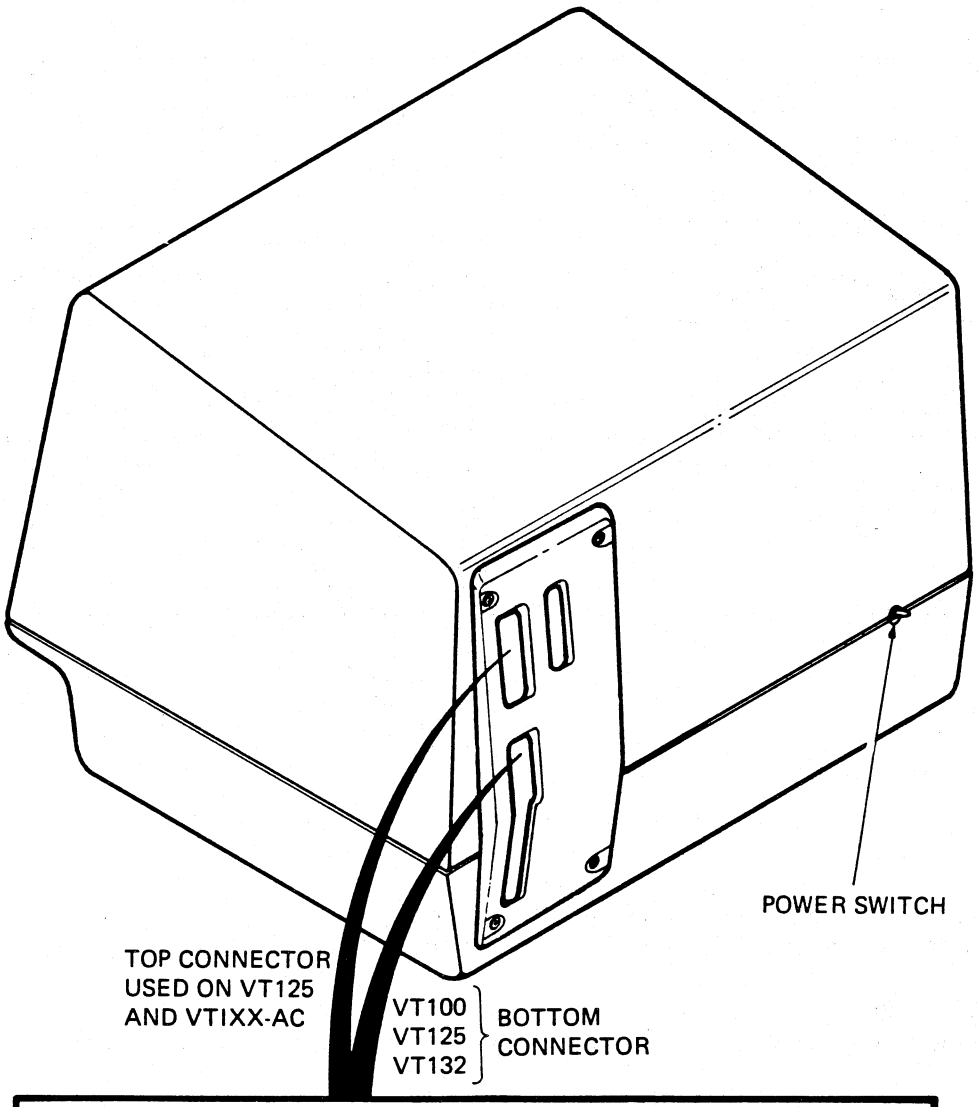


Figure 6-83 EIA Loopback Connector

6.8.2 Error Reporting

This section explains how the VT125 reports VT100 and VT125 errors.

6.8.2.1 VT100 Errors – VT100 errors are reported in the usual VT100 manner, in the LEDs or as a character in the upper-left corner of the display.

6.8.2.2 VT125 Errors – The VT125 reports its self-test results with the graphics display. It reports fatal errors by flashing the monochrome display according to a coded intensity pattern (Table 6-5). Use an oscilloscope to measure the monitor outputs.

On ROM or RAM errors, the color display provides additional information in the form of an encoded color output. Table 6-6 shows the color combinations for each of the possible values from 0 to 7.

You do not have to terminate the video outputs for troubleshooting. However, unless 75-ohm loads are attached, the output voltages are higher than specified. Table 6-7 shows the voltages for both the monochrome composite video output and the RGB outputs when they are not terminated.

The nonfatal errors (terminal still functions partially) try to display an error code as text. This requires a large amount of working code and hardware, and thus may be somewhat meaningless. If, however, enough of the hardware is working, one of the following messages will appear in the center of the display.

VT125 xx Error
VT125 OK
VT125 Offline

xx is an error code representing one of the following error(s).

BM – Video bitmap RAM error
VG – Vector generator error
IC – Internal (VT125-to-VT100) communications error
SC – Serial (auxiliary) port communications error
EC – External (host) communications error

The terminal clears this status message when the next character sent from the host arrives. The VT125 is operational after self-test if no fatal errors occurred. If a nonfatal error occurred, then the VT125 will work as well as possible considering the failure.

Table 6-5 VT125 Fatal Error Indication

Error	Monochrome Display Alternates Between	Color Display Shows	Explanation
1	0 and 1	–	CPU register error
2	0 and 2	ROM address B14-12	ROM checksum error
3	0 and 3	RAM bit number	Program RAM error
4	1 and 2	–	Vertical Sync timeout
5	1 and 3	–	Vector timeout

Table 6-6 ROM and RAM Failure Indications

Number	G	R	B	Color	ROM	RAM
0	0	0	0	Dark	E22	E4
1	0	2	1	Pink	E22	E3
2	1	0	2	Blue	E23	E2
3	1	2	3	Violet	E23	E1
4	2	1	0	Orange	E24	E8
5	2	3	1	Light brown	E24	E7
6	3	1	2	Pale blue	E25*	E6
7	3	3	3	White	E25*	E5

*E25 is not used in the VT125.

Table 6-7 Error Output Signal Levels

Numbered Level	Unterminated Mono	RGB
3	2.0	2.0
2	1.7	1.3
1	1.3	0.5
0	0.6	0

Note: Mono composite sync tip is at 0 volts.

CHAPTER 7
STANDARD TERMINAL PORT

7.1 INTRODUCTION

The standard terminal port (STP) is intended to be a standard interface for terminal options. These options may include communications, graphics, a terminal processor, and mass storage devices.

The STP was originally developed as part of the VT100. Attempts have been made to ensure the generality of the STP, but some compromises toward the VT100 may have been made. Special VT100 considerations are noted in this chapter where applicable.

7.2 DEFINITIONS

The following definitions apply in this discussion:

Active device – A device that either: 1) wishes to take over control of the host communication line; 2) requires all received and transmitted data passed between the host communication line and the terminal controller to be looped through the device; or 3) needs to communicate with the terminal controller directly. One example of an active device is a terminal processor doing local editing, standalone computing, etc.

Host – That which connects to the serial line connector on the outside of the terminal. Normally, this is a computer system (via direct line or otherwise), but might in some cases be another terminal or other device.

Host link – The serial line between the option and the host. The option's line UART is on one end of this link, and the host is on the other.

Local link – The serial line between the terminal controller and option when an option is present. The terminal controller's UART is on one end of this link, and the option's local UART is on the other.

Passive device – Those devices that do not need the capabilities of an active device. A passive device normally only wants to listen to the data stream from the host and to pass data back to the host, but not to interfere with normal terminal or communications line operation. Terminal mass storage, such as a tape cartridge, would fall into this class.

Receive only device – A special case of a passive device that never needs to transmit data to the host, but only to listen to data from the host. Certain types of graphics options fall in this category.

Terminal controller (TC) – The processor in the basic terminal that controls normal terminal operation. This term is used to distinguish it from any other processor that might be packaged into a terminal.

Terminal processor (TP) – An additional processor, not necessary for basic terminal operation, but to add other functions, such as local editing or computing.

SET-UP mode – The terminal mode that allows user to set terminal characteristics.

7.3 OVERVIEW

The STP provides a means of interfacing terminal options. Logically, this interface is similar to that of a serial line splice (Figure 7-1) which is accomplished by breaking the serial line from terminal to host and inserting the option. An internal interface connector is provided for reasons of packaging aesthetics, and additional signals are present to reduce the interface cost. Part of the terminal controller firmware is also dedicated to support the STP, since some information needed by the option is passed as data across the serial line, rather than assigning additional pins on the interface connector. This firmware also allows the option to use the terminal characteristics specified by the user in SET-UP Mode. The STP provides a reasonably cost-effective interface for a large class of terminal options, and is general enough to allow for decoupled evolution of terminals and terminal options.

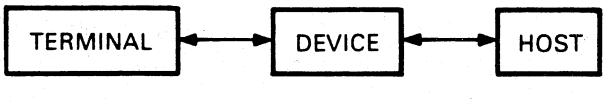


Figure 7-1A Serial Line Splice Connection

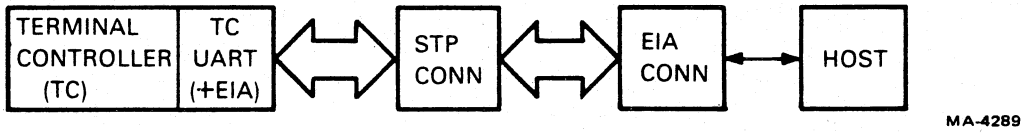
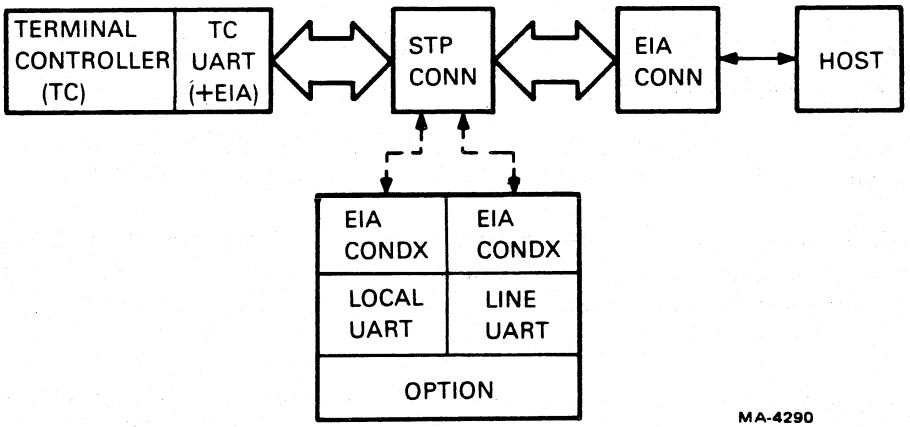


Figure 7-1B STP with No Option Present



7-1C STP with Option Present

7.4 FUNCTIONAL SPECIFICATION

7.4.1 Interface Signal Lines

The signal lines that make up the STP are shown in Figure 7-2. The lines are accessed through a standard 20-pair shorting connector, described in Paragraph 7.6. In general, the signals are standard EIA serial line and modem controls, though some special signals are also present. See Paragraph 7.5 for complete electrical specifications.

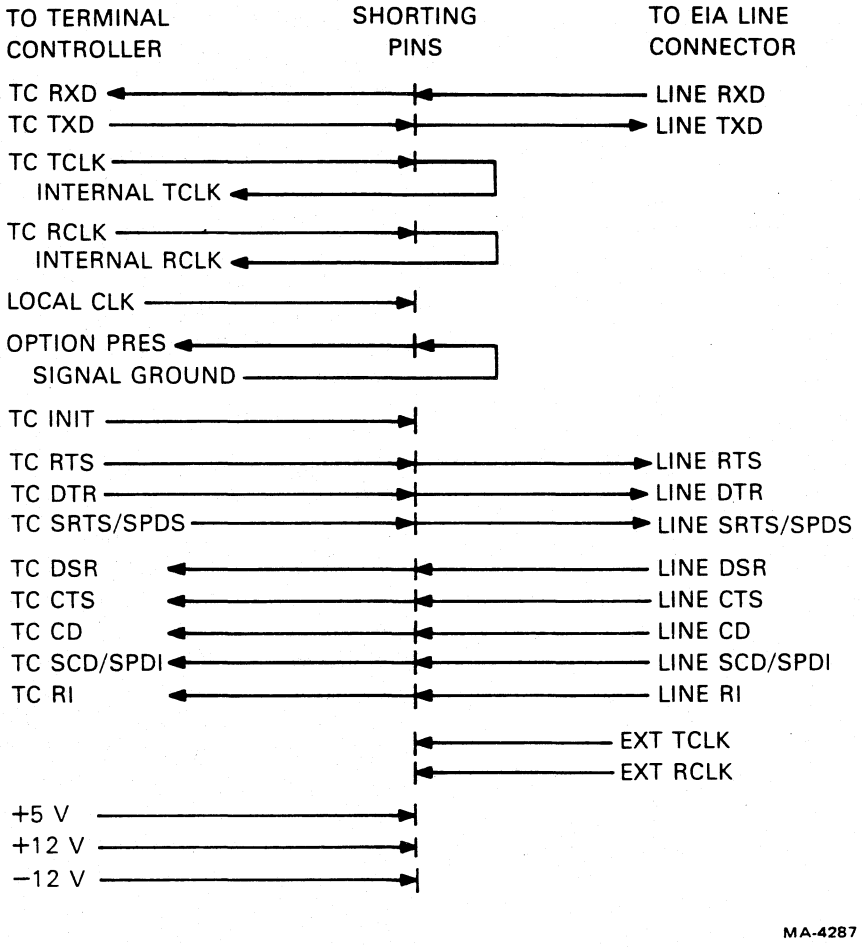


Figure 7-2 STP Signal Lines

Each pair of signals is connected together when no option is present. When an option is plugged in, each connection is broken, though the option may choose to short through any signal it does not wish to control. Note that some signals are used between the terminal controller and option only or between option and external connector only, and so are defined on only one side of the connector. The signals and their meanings are as folllows.

Signal	Type	Meaning
TC RXD	EIA	TC received data. Serial, asynchronous data is passed from host or option to the TC on this line.
LINE RXD	EIA	Line received data. Serial data is passed from host to option or TC on this line.
TC TXD	EIA	TC transmitted data. Serial data is passed from TC to host or option on this line.
LINE TXD	EIA	Line transmitted data. Serial data is passed to host from option or TC on this line.
TC TCLK	TTL	TC transmitter clock. This signal from the TC bit rate generator normally drives the UART that talks to the host. Its frequency is 16 times the bit rate.
INTERNAL TCLK	TTL	Internal transmitter clock. This signal drives the UART associated with the TC. When no option is installed this signal is driven by TC TCLK. With an option installed this signal would normally be driven by either TC TCLK or LOCAL CLK. (Refer to Paragraph 7.4.2.2 for further information.) The baud rate applied to this line may not be more than 19,200 for a VT100.
TC RCLK	TTL	TC receiver clock. Just like TC TCLK.
INTERNAL RCLK	TTL	Internal receiver clock. Just like INTERNAL TCLK (19,200 max. for VT100).
LOCAL CLK	TTL	Local bit rate clock. This is a clock signal provided by the TC which is 16×, a "convenient" data rate for the local (TC to option) link. Normally, this bit rate would be near the highest rate that the TC can handle efficiently. It need not be a standard bit rate, so this clock can be sourced by some timing

Signal	Type	Meaning
		signal that happens to be available in the terminal. The equivalent $\times 16$ baud rate supplied by the VT100 is 15,734 baud (251.744 kHz).
OPTION PRESENT	TTL	Option present. A low on this line means that no option is present, and normal terminal operation is in order. It must be passively pulled up on the TC board. A high on this line indicates the presence of an option and informs the TC to make appropriate changes in its operating modes.
TC INIT	TTL	Initialize. This line notifies the option that a power-up clear or terminal reset has occurred. (See electrical specifications in Paragraph 7.5.)
TC RTS TC DTR TC SRTS/SPDS	EIA	Terminal controller modem control signals. These signals are the standard EIA modem control signals: request to send, data terminal ready, and secondary request to send (or speed select). The option may ignore them, use them itself, or pass them through to the corresponding "LINE" signals.
LINE RTS LINE DTR LINE SRTS/SPDS	EIA	Line modem control signals. EIA modem control signals that go to the host line may be fed from option or from the corresponding "TC" signals. In the VT100, LINE SRTS/SPDS is strapped to pins 11, 19, and 23 on the RS-232-C connector mounted on the terminal.
TC DSR TC CTS TC CD TC SCD/SPDI TC RI	EIA	TC modem status signals. These lines are the standard EIA status signals: data set ready, clear to send, carrier detect, secondary carrier detect (or speed indicator), and ring indicator. The option may source these signals to the TC, or pass through the corresponding "LINE" signals.

Signal	Type	Meaning
LINE DSR LINE CTS LINE CD LINE SCD/SPDI LINE RI	EIA	Line modem status signals. The EIA modem status signals received from the host line connector. May be used by the option, or passed through to the corresponding "TC" signals. In the VT100, LINE SCD/SPDI is connected to Pin 12 of the RS-232-C connector mounted on the terminal. This pin is used for different functions by different modems.
EXT TCLK	EIA	External transmit clock. This signal is provided by a modem or other external device. This pin is connected to pin 15 on the RS-232-C connector mounted on the terminal. It is intended to be used by an option that needs this signal.
EXT RCLK	EIA	External receive clock. This signal is provided by a modem or other external device. This pin is connected to pin 17 on the terminal's RS-232-C connector.
+5 V, +12 V, −12 V	Power	Interface power. (See Paragraph 7.5.2 for further specifications.)
SIGNAL GROUND	Ground	Signal ground.

7.4.2 Protocol Specification

Proper operation with the STP requires some firmware support in the terminal controller. This section specifies the protocol used to communicate between option and terminal controller.

7.4.2.1 Terminal Operation with No Option Present – In standalone terminal operation, all signals on the STP are passed through by the shorting connector. The terminal controller senses the absence of an option and performs its normal function. In SET-UP mode, when the user makes changes to terminal characteristics, these changes take effect in the normal manner. Any escape sequences from the host destined for a nonexistent device are ignored by the terminal controller.

7.4.2.2 Standard Set-Up for Local Link – When an option is present and breaks the serial line as it passes through the STP connector, the option and terminal controller must agree on the line characteristics for the local link. To this end, the assertion of OPTION PRESENT causes the following changes:

Bits/Char	Set to 8 bits per character
Stop Bits	Set to 1 stop bit

Parity	Set to no parity
XOFF	Line synchronization (XON/XOFF) must be supported in both directions on the local link. Note that the TC must accept XOFF as well as source it.

Normally, it is assumed that the option will use the TC TCLK and TC RCLK signals to drive its line UART, while using LOCAL CLK to drive INTERNAL TCLK and INTERNAL RCLK. The option may, however, choose to source another set of clocks to drive the TC UART instead. INTERNAL CLOCKS should not be driven at a frequency higher than 19,200 baud for the VT100. It is recommended that INTERNAL TCLK and INTERNAL RCLK be set to the same rate to avoid XON/XOFF timing problems.

7.4.2.3 Control Sequences for Terminal Parameters – Only two control sequences are specified for STP operation. The first of these reports terminal parameters of interest to the option, while the latter is used to request this information. The formats of these sequences are:

DECREPTPARM – Report Terminal Parameters

ESC [<sol>;<par>;<nbits>;
<xspeed>;<rspeed>;<clkmul>;
<flags> x

DECREQTPARM – Request Terminal Parameters

ESC [<sol> x

The final character for both strings has been chosen as lowercase x (octal code 98, column/row specifier 7/8). This is a DEC Private sequence.

DECREPTPARM is sent by the terminal controller to notify the option (or host) of the status of selected terminal parameters. It may be sent when requested by the host or option, or at the terminal's discretion. DECREPTPARM will be sent upon receipt of a DECREQTPARM, or voluntarily upon leaving SET-UP mode when the terminal sees option present asserted and it has been asked to report unsolicited by a previous host request.

The option is responsible for sensing a terminal power-up or reset, which it may note by the assertion of TC INIT by the terminal.

The meanings of the parameters are as follows:

(* indicates the assumed value if the parameter is not specified.)

Parameter	**Value**	**Meaning**
<sol>	0 or none	This message is a request (DECREQTPARM) and the terminal will be allowed to send unsolicited reports.
	1	This message is a request, and henceforth, the terminal may only report in response to a request.
	2	This message is a report (DECREPTPARM) and the terminal thinks it may report at will, although this particular report may not be voluntary.
	3	This message is a report, and the terminal is only reporting on request.

Parameter	Value	Meaning
<par>	1*	No parity set
	2	Parity is always space (not a VT100 state)
	3	Parity is always mark (not a VT100 state)
	4	Parity is set and odd
	5	Parity is set and even
<nbits>	1*	8 bits per character
	2	7 bits per character
<xspeed>,<rspeed>		Because some terminals have limitations in handling numeric values, baud rates cannot be sent as decimal strings (e.g., 2400). This list of baud rates is basically encoded on multiples of 8 so further speeds can be specified later and left in baud rate order.

Bit Per Sec	Rate	
0	50	
8	75	
16	110	
24	134.5	
32	150	
40	200	
48	300	
56	600	
64	1200	
72	1800	
80	2000	
88	2400	
96	3600	
104	4800	
108	7200	(not a VT100 speed)
112*	9600	
120	19200	

<clkmul>	1*	The bit rate multiplier is 16
	2	The bit rate multiplier is 64
<flags>	0–15	This value communicates 4 bits of user defined information as a decimally encoded binary number. These bits may be assigned in an STP device dependent fashion. Bit weights are 8 4 2 1 from left to right. The default value for these four bits is 0. In the VT100, these bits are switch group 5 of SET-UP B.

If any parameter (except for <sol>) is zero or not present, it should be interpreted as the default value for this parameter. The default for each parameter is marked with an asterisk (*) in the above list. Any parameter out of its defined range must be treated as an error. Additional parameters (beyond these seven) must be ignored without affecting the interpretation of the other parameters. This last restriction allows for future standardization of the additional parameters.

7.4.2.4 Initialization – The option must sense the signal TC INIT from the terminal controller and reset itself to initial state upon reception of this signal. Timing for this signal is specified in Paragraph 7.5.1.2. This signal may be used to reboot a terminal processor if desired. It will be generated at terminal power-up, and in response to a "reset to initial state" or confidence test request from the host or operator.

7.4.2.5 BREAK – The BREAK signal will be transmitted over both the local and host links in the normal manner. If an option which passes characters from the terminal controller to the host without modification, the option must detect the break on the local link and generate a corresponding break on the host link.

If a terminal processor treats the terminal controller as a terminal, BREAK from the terminal controller may be used for a standard purpose such as causing entry into ASCII console microcode. This may require the option to use a UART with an external "framing error" line, or to design in a hardware break detector (counter and gate).

7.5 ELECTRICAL SPECIFICATIONS

7.5.1 Signal Lines

Specifications for the signal (nonpower) lines are a follows.

7.5.1.1 Signal Levels – Two classes of signals are present on the STP connector. The first class are standard EIA levels, and include transmitted and received data, modem control signals, etc. The second class are TTL signals used to control interface operation, and include bit rate clocks, OPTION PRESENT, etc.

For VT100:

All EIA outputs
Mark State -6.0 to -12.0 V
Space State +6.0 to 12.0 V

All EIA inputs
Mark State +0.75 to -25.0 V, -8.3 mA max.
Space State +2.25 to +25.0 V, +8.3 mA max.

All TTL inputs
VIH = 2.0 V max.
IIH = 20 μA max. @ VI = 2.7 V
VIL = 0.8 V max.
IIL = 0.5 mA @ VI = 0.4 V

All TTL outputs
VOH = 2.7 V @ IOH = 0.1 mA
VOL = 0.5 V @ IOL = 3.2 mA

7.5.1.2 Signal Timing – The INIT H signal goes high when the VT100 starts an initialize sequence and goes low when the VT100 is ready to operate. The minimum high time is 100 ms.

LOCAL CLK has the following period for the VT100 as shown in Figure 7-3.

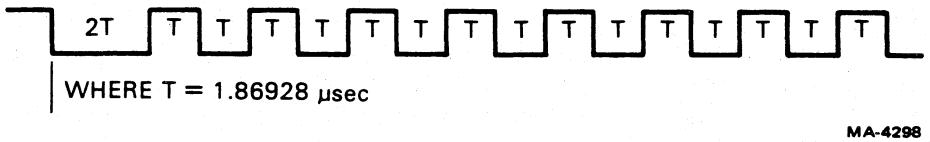


Figure 7-3 Local Clock

7.5.2 Power Supply Lines

Voltage regulation specifications and base product power requirements for the VT100 may be found in Chapter 4. All options drawing power through the STP or 20 mA connectors on the VT100 terminal controller board may draw no more than 0.5 A from any one voltage. Options drawing power from any connector in the VT100 must be sure that their requirements, the needs of other options, and the needs of the base VT100 are consistent with the capability of the VT100 power supply.

7.5.3 Connector Pinout

TC TXD	2	1 LINE TXD
–	-4	3 EXT TCLK
TC RXD	6	5 LINE RXD
TC RTS	8	7 LINE RTS
–	-10	9 EXT RCLK
TC CTS	12	11 LINE CTS
TC DSR	14	13 LINE DSR
TC DTR	16	15 LINE DTR
TC CD	18	17 LINE CD
TC RI	20	19 LINE RI
TC SPDS	22	21 LINE SPDS
TC SPDI	24	23 LINE SPDI
–12 V	26	25 —
TC TCLK	28	27 INTERNAL TCLK
TC RCLK	30	29 INTERNAL RCLK
+12 V	32	31 —
OPTION PRESENT	34	33 SIGNAL GROUND
LOCAL CLK	36	35 —
TC INIT	38	37 —
+5 V	40	39 —

7.6 MECHANICAL SPECIFICATIONS

7.6.1 Shorting Connector

The STP connector, DEC part number 12-14829 consists of 20 pairs of shorting bifurcated contacts, spaced on 0.125 inch centers, with 0.4 inch penetration (Figure 7-4).

7.6.2 STP Connector Card

The card that plugs into the STP connector may serve as just a paddle card with connection to a separate module, or may actually contain circuitry such as a minimum terminal processor. The terminal provides room for a card at least as large as and with finger and connector placement similar to those in Figure 7-5. STP interfaces to be dedicated to a particular terminal family may depart from this specification, but at penalty of future generality.

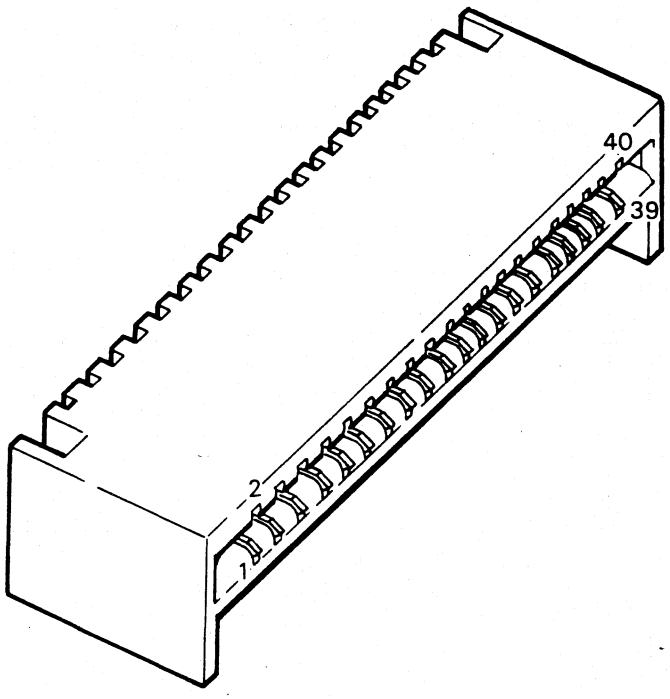


Figure 7-4 STP Connector

7.7 GUIDELINES FOR THE DESIGNER

This section is not, strictly speaking, part of the STP specification. It is meant to provide some indication of how the STP may be used to implement some different terminal configurations. It is not intended to be an exhaustive study of all possible options, nor to dictate particular design decisions. It is hoped, however, that it will be useful to the architect and option designer, and provide some insight into the choices made in specifying the STP.

7.7.1 Use with Receive Only Device

There are two basic ways to implement a receive only device on the STP. One method requires only one UART, the other two. The first method is more limited, however, while the second is more flexible.

7.7.1.1 Single UART Method – In this case, the option shorts through all STP signals and does not assert OPTION PRESENT. It picks up the receive bit rate clock from the STP signal lines and uses only the receive side of its UART to tap off the TC RXD/LINE RXD line. It also watches for TC INIT and may, if desired, monitor the state of the modem control and status lines.

The limitations of this method are:

1. The option may not send XOFF to the host to control the received data rate.

2. The option gets no information or parity status or sense from the terminal controller. It may try to deduce this information from the data it sees, or specify that it may only be used in certain modes, however.

3. The option gets no information on number of bits/char or bit rate multiplier from the terminal controller. Similar to parity problem.

The advantage of this method is its low cost for implementing a receive only device.

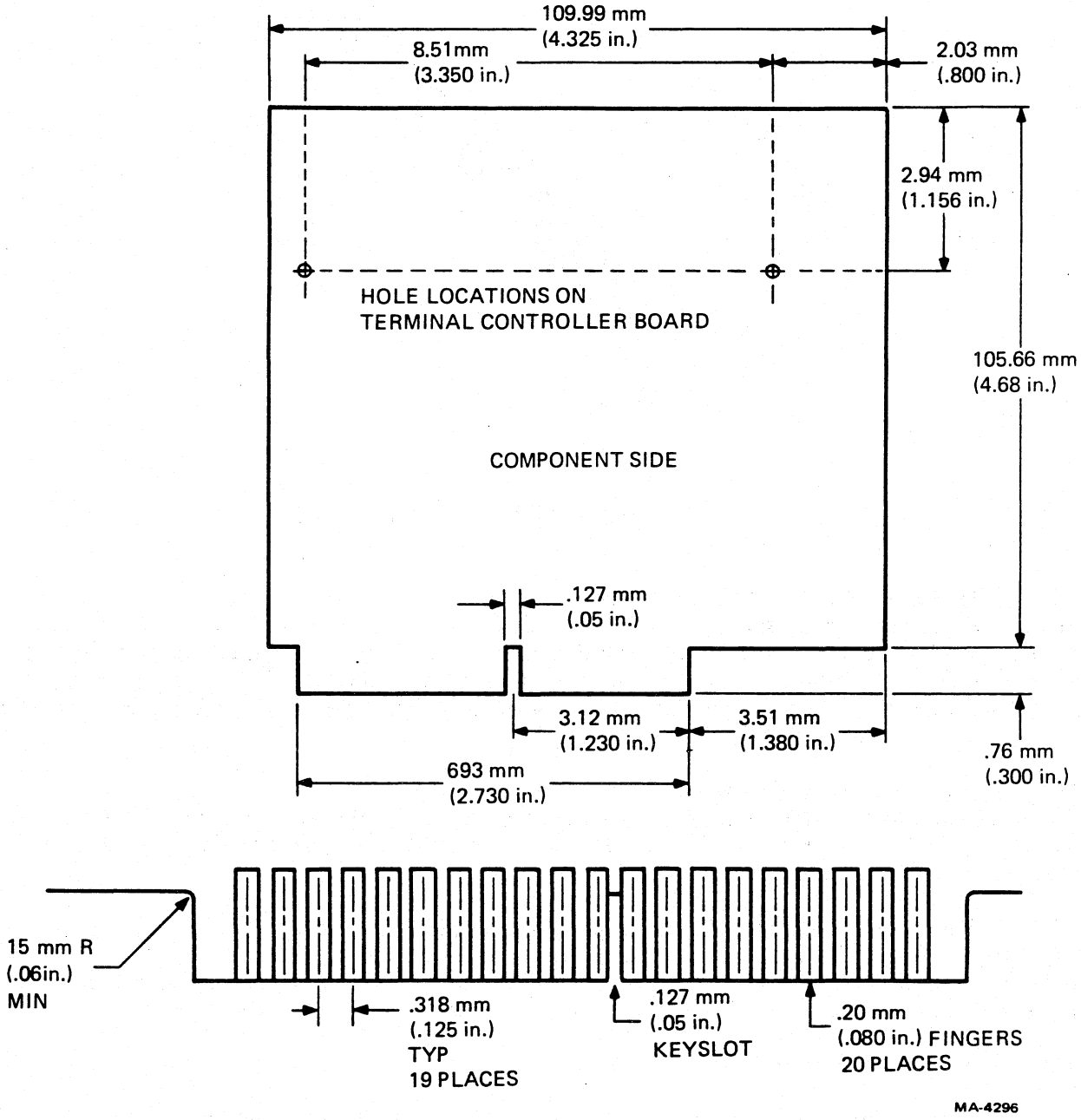


Figure 7-5 STP Option Card

7.7.1.2 Two UART Method – In this case, the option breaks the serial data and clock lines on the STP, while passing through the modem control and status signals without change. It asserts OPTION PRESENT, normally ties LOCAL CLK to INTERNAL TCLK and INTERNAL RCLK as well as to its own local UART, and uses TC TCLK and TC RCLK to drive its own line UART.

In this mode, the option is responsible for implementing XON/XOFF on the host link, if that feature is enabled. It may also XOFF the terminal controller if the data is coming too fast, since the data rates on the local and host links may not be the same. It must, of course, also respond to an XOFF from the terminal controller.

7.7.2 Use with Passive Device

Unlike the receive only device, the passive device option wishes to transmit data on the host link, and must therefore break the serial line as it crosses the STP connector.

The passive device connects to the STP in the same way as the two UART receive only device. It asserts OPTION PRESENT and drives INTERNAL TCLK and INTERNAL RCLK (with either LOCAL CLK or a clock generated by the option itself).

In this mode of operation, the option must parse all valid ANSI sequences it passes from the terminal controller to the host. First, it must recognize DECREPTPARM in order to get the current set of terminal characteristics. Second, it must parse all other ANSI sequences so that it never sends data to the host in the middle of a sequence generated by the terminal controller. Sequences that must be handled correctly are specified in ANSI X3.64-1977, and include: escape sequences, control sequences, control strings, and single shifts.

Since a passive device does not need to talk to the terminal controller, it need not parse ANSI sequences from the host before passing them on to the terminal controller. Note that the terminal controller must accept an XOFF in the middle of a (escape or control) sequence without error. The option need only recognize those sequences which belong to it. As long as these are valid ANSI sequences they will be ignored by the terminal controller.

Because a single terminal may have more than one option, it is required by this specification that any passive device must replicate the standard STP shorting connector. This shorting connector should break the host link on the option before that link returns to the STP connector of the terminal controller (or option) that the device plugs into. (For more detail on these requirements, see Paragraph 7.7.6).

7.7.3 Use with Active Device

There are at least two types of active devices: (1) the terminal processor acting as the CPU in a standalone system packaged in a terminal box, and (2) the terminal processor acting to enhance the terminal functionality, to provide local editing, format and value checking, etc. In the former case, the terminal processor (the active device) views the local link and host link sides of the STP as two separate entities and may, in fact, not even make use of the host link. In the latter case, by contrast, the terminal processor (again the active device) is seen only as augmenting the basic terminal operation, and (in some abstract sense) passes through all the data it handles between host and terminal controller.

7.7.3.1 Terminal Processor as Standalone CPU – In this configuration, the terminal processor treats the local and host links of the STP as two separate devices. It asserts OPTION PRESENT to set the local link to a standard state. It retains control of the host link, though it may listen to DECREPTPARM sequences sent by the terminal controller if this is appropriate to the application. It may use or ignore TC RCLK and TC TCLK as it wishes. If the TP needs "boot" and "console entry" signals, these needs may be met by INIT and local BREAK, respectively.

7.7.3.2 Terminal Processor Augmenting Basic Terminal Operation – In this case, the terminal processor is used to add functionality to the terminal. Logically, communication is between the host and the "terminal" (terminal controller plus terminal processor), rather than between a CPU and two devices as in the standalone CPU case. The terminal processor may intercept the normal data stream to and from the terminal controller, rather than just listening for (and interjecting) special control sequences, as in the passive device case. One example of such an option is a printer graphics option, which would receive graphic instructions, convert them into a bit map representation, and transmit that bit map serially to the printer terminal controller. Another example is that of a multiplexer which might make a CRT terminal into three logical terminals by maintaining cursors in each of three screen areas, routing keyboard input to the proper host task, etc.

7.7.4 Use with Communications Option

This case is similar to the active device configurations discussed in Paragraph 7.7.3. In addition, the option may use the EXT TCLK and EXT RCLK signals. Communication options would not normally need to replicate the STP connector, since there would be no further options between the terminal and the communications line.

7.7.5 Use with an External Processor

As long as control sequences used by the terminal controller to pass information to the terminal processor are present in the terminal controller firmware, there is no reason to prevent an external processor (host) from using them. This applies when the host CPU wishes to act as an enhancement to the terminal, (Paragraph 7.7.3.2), but does not fit into the terminal cabinet. Such a capability is also useful in writing and debugging programs that eventually run in a terminal resident, terminal processor. To allow this operation, a small interface card plugged into the STP does the following:

1. Asserts OPTION PRESENT.

2. Provides a standard bit rate (known to the host) to INTERNAL RCLK and INTERNAL TCLK. TC RCLK and TC TCLK would not be used directly, though DECREPTPARM would advise the host of this information.

3. Passes through RXD, TXD, and all modem control signals. If the host needed to sense and drive all modem signals, a special host interface might be required.

In this way, the host CPU can do a fairly good job of emulating the terminal processor and may replace it in some applications.

7.7.6 Use with More than One Option

While it is believed that multiple options can be supported on the STP, no detailed specifications for such operation are given at this time. All options which plug into the STP must, however, replicate the STP connector on the "host" side of their interfaces, to allow for the addition of other options. The only exceptions to this rule are those devices which must, by their very nature, be the "last" device in the terminal. Examples of such devices are a current loop adapter or modem.

CHAPTER 8
GRAPHICS CONNECTOR

8.1 INTRODUCTION

An 18 pin dual-in-line connector is provided in the VT100 for internal options that generate digital video signals, and may additionally require 8-bit ASCII data forwarded by the VT100 from the communications line as specified below. An option not requiring all 18 signals may use a shorter connector plugged into the appropriate set of holes on the graphics connector.

All signals below are identified as "to the VT100" (T) or "from the VT100" (F).

	Pin Numbers
D7 (F) 1	18 Signal Ground
D6 (F) 2	17 (T) Graphic Video 1 L
D5 (F) 3	16 (F) Vertical Blank L
D4 (F) 4	15 (F) Graphic Write L
D3 (F) 5	14 (F) Horizontal Blank H
D2 (F) 6	13 (F) INIT H
D1 (F) 7	12 (T) Graphic Video 2 L
D0 (F) 8	11 (T) Graphic Flag L
Signal Gnd 9	10 (F) 24.0734 MHz Clock

Signal	**Description**
D7–D0	During the VT100 "Graphic Processor On" mode (see Appendix A for entry and exit), all characters transmitted to the VT100 on the communications line are transferred to these data lines with a graphic write strobe. The only characters not transmitted are the "Graphic Processor Off" escape sequence. (Maximum load = two 74XX loads plus 50 pF.)
24.0734 MHz	VT100 Master Video Clock. (Maximum load = one 74SXX load.)

Signal	Description
Graphic Flag L	On initialization (between the time INIT H goes low and the first character is transmitted to the graphics connector in "Graphic Processor On" mode) the GRAPHIC FLAG will be checked. If the flag is low, the VT100 assumes the presence of an option on the graphics connector and enters "Graphic Processor On" mode normally upon receipt of the appropriate control. If the flag is high, the VT100 assumes that no option is installed and refuses to enter "Graphic Processor On" mode. After initialization a low on the GRAPHIC FLAG indicates that the option is prepared to receive characters from the VT100. A high GRAPHIC FLAG indicates the option is busy, the VT100 stores incoming characters in its buffer and responds to the host in its normal fashion if its buffer becomes full (see Appendix A Communications Protocol). (Input load = one 74LSXX load plus 4.7K ohms to +5 V.)
INIT H	The VT100 asserts this pin high whenever it begins an initialize sequence (power-up or on command) and asserts INIT low whenever it is ready to begin normal operation. The minimum high pulse width is 100 ms. (Maximum load = two 74XX loads plus 50 pF.)
Horizontal Blank H	Asserted high during VT100 blank time. Used for horizontal sync and to indicate the start of VT100 display. Pulse period = 63.556 μs Pulse width = 11.465 μs/80 column mode; 12.088 μs/132 column mode Delay Falling Edge of HORIZONTAL BLANK H to First Dot from VT100 = 500 ns/80 column mode; 250 ns/132 column mode (Maximum load = one 74XX load plus 50 pF.)
Vertical Blank L	Asserted high only during displayed scans on the VT100. In all modes the VT100 displays 240 complete scans/field. The VERTICAL BLANK signal transitions between 1.2 μs and 1.5 μs after the rising edge of HORIZONTAL BLANK H. (Maximum load = one 74XX load plus 50 pF.)
Graphic Video 1 L and 2 L	A truth table for the intensity of the display for different values of these inputs is shown below. The table applies only to areas of the screen that are otherwise black. When graphic data overlaps other data in the VT100, the display is as bright or brighter than the values in the table. **GV1 GV2 Intensity** H H Black L H Dim H L Normal L L Bright (Input load = one 74XX load plus 4.7K ohm to +5 V.)

Signal	Description
Graphic Write L	This pin is pulsed low by the VT100 during valid data on D7–D0. Data (D7–D0) is stable 25 ns before the falling edge of GRAPHIC WRITE and remains stable for 25 ns after the rising edge of GRAPHIC WRITE. The pulse width low of GRAPHIC WRITE is 350 ns ± 50 ns. (Maximum load = two 74XX loads plus 50 pF.)

8.2 HARDCOPY ENABLE

Provision has been made in the VT100 for the future addition of an external hardcopy option to record the screen. Such a device is assumed to monitor the graphics connector to receive the "copy" command and to obtain its picture information from the composite video output. Upon receipt of the escape sequence DECHCP (see Appendix), the VT100 will stop updating the screen but will not cease blinking operations. Following the freeze, the VT100 will write an 8-bit character of all ones (FFH) to the graphics port. The GRAPHIC FLAG should go high when this character is transmitted; and the VT100 will maintain the screen frozen until the flag is seen to be low, at which time the VT100 will resume normal operation.

APPENDIX A
PROGRAMMING INFORMATION

This appendix summarizes the VT100 series video terminal transmitted characters and received character processing. The VT100 terminal normally performs a two-part function. It is an input device to a computer – information entered through the keyboard is sent to the computer. It is simultaneously an output device for the computer; that is, data coming in from the computer is displayed on the video screen. Figure A-1 shows the data flow.

This appendix discusses data flow between the VT100 and the host. Included are the codes generated by the keyboard; the transmission protocol followed by the terminal; and the actions and reactions of the terminal to control codes and escape sequences, in both ANSI and VT52 modes of operation.

The VT100 is an upward and downward software compatible terminal; that is, previous DIGITAL video terminals have DEC private standards for escape sequences. The American Standards Institute (ANSI) has since standardized escape sequences in terminals. ANSI standards allow the manufacturer in implementing each function. This appendix describes how the VT100 responds to the implemented ANSI control functions.

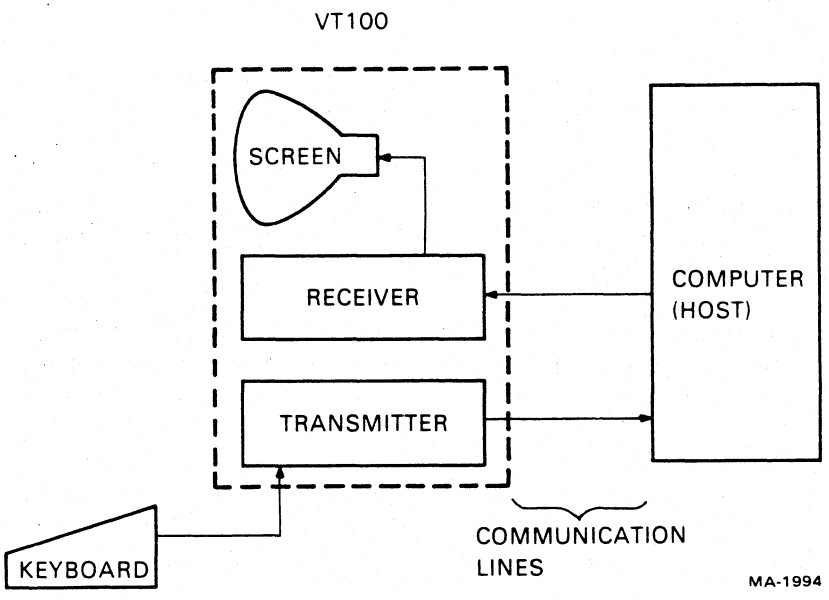


Figure A-1 Terminal Data Flow

The VT100 is compatible with both the previous DEC standard and ANSI standards. Customers may use existing DIGITAL software designed around the VT52 or new VT100 software. The VT100 has a VT52 compatible mode in which the VT100 responds to escape sequences like a VT52. In this mode, most of the new VT100 features cannot be used.

Throughout this discussion references are made to VT52 mode or ANSI mode. These two terms indicate the VT100's software compatibility. All new software should be designed around the VT100 ANSI mode. Future DIGITAL video terminals will not necessarily be committed to VT52 compatibility.

VT100 KEYBOARD

The VT100 keyboard (Figure A-2) has a key arrangement similar to an ordinary office typewriter. In addition to the standard typewriter keys the VT100 has keys and indicators that generate escape and control sequences, cursor control commands, and show the current terminal status.

You use the keyboard to transmit codes to the host. Some keys transmit one or more codes to the host immediately when typed. Other keys such as **CTRL** and **SHIFT** do not transmit codes when typed, but modify the codes transmitted by other keys. When you press a code-transmitting key, the terminal makes a clicking sound to verify it processed the keystroke. If you press two code-transmitting keys together, two codes are transmitted in the order typed. The terminal does not wait for the keys to be lifted, but transmits both codes as soon as possible after the keys are typed. If you press three such keys together, the codes for the first two keys are transmitted immediately; the code for the third is transmitted when one of the first two keys is lifted.

LED Indicators

The keyboard has seven light emitting diodes (LEDs); two are committed to the complementary ON-LINE/LOCAL function. The power-on condition is implicitly shown by one of the two LEDs being on; that is, if the keyboard is connected and power is on, one of these LEDs is on.

A third LED indicates a "keyboard-locked" condition. In this condition the keyboard has been turned off automatically by the terminal due to a full buffer, or by the host through the transmission of an XOFF to the terminal.

You can program the four remaining LEDs and assign any meaning for specific applications. The code sequences to turn these LEDs on or off are discussed later.

SET-UP Key

The **SET-UP** key is at the upper-left corner of the main key array. Operations performed in SET-UP mode can be stored in nonvolatile memory (NVR) so that turning terminal power off does not, by itself, alter the terminal configuration.

The procedures to change the SET-UP features are provided in the operator's information section of this manual. SET-UP features that may be modified by the host are listed in Table A-1 and described in detail under the escape sequences.

Alphabetic and Nonalphabetic Keys

The VT100 transmits lowercase code unless either or both **SHIFT** keys are down, or unless the **CAPS LOCK** key is down. Pressing **CAPS LOCK** locks only the 26 alphabetic keys in the shifted (uppercase) mode. Figure A-3 shows the codes generated by the alphabetic keys.

Each nonalphabetic key can generate two different codes. One code is generated if neither **SHIFT** key is pressed. The other code is generated if either or both **SHIFT** keys are down. Unlike the shift lock key of a typewriter, **CAPS LOCK** does not affect these keys; it affects only the alphabetic keys.

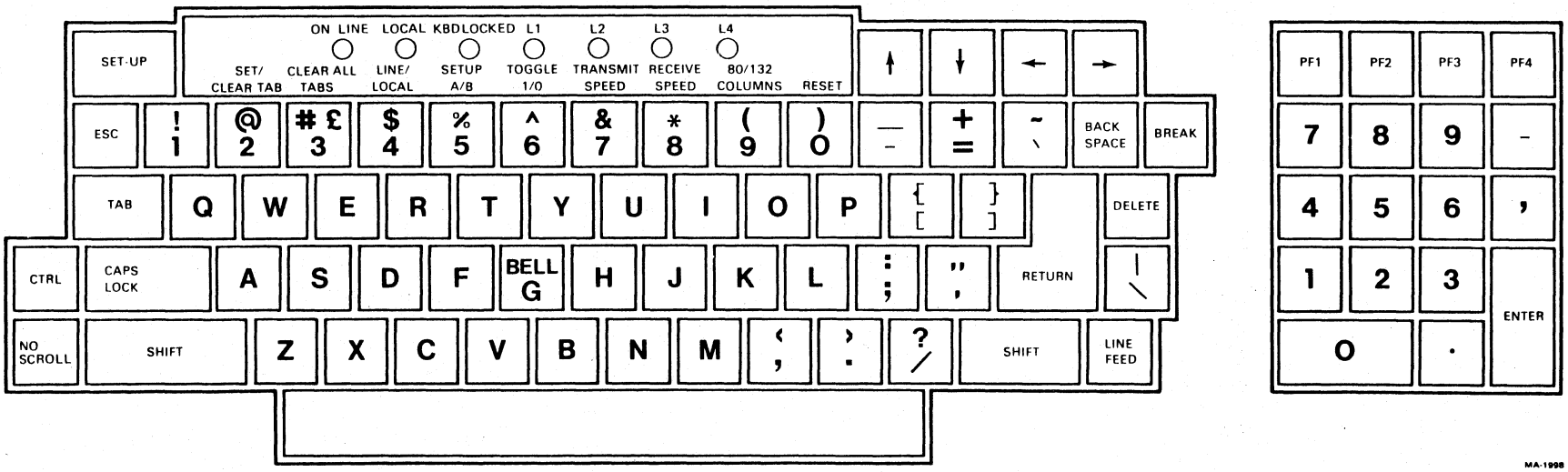


Figure A-2 VT100 Keyboard

Table A-1 SET-UP Features and Machine States

SET-UP Feature or Machine State	Changeable from Host Computer*	Saved in NVR and Changeable in SET-UP
Alternate keypad mode	Yes(DECKPAM/DECKPNM)	No
ANSI/VT52	Yes(DECANM)	Yes
Auto repeat	Yes(DECARM)	Yes
Auto XON XOFF	No	Yes
Bits per character	No	Yes
Characters per line	Yes(DECCOLM)	Yes
Cursor	No	Yes
Cursor key mode	Yes(DECCKM)	No
Graphics mode	Yes(DECGON/DECGOFF)	No
Interlace	Yes(DECINLM)	Yes
New Line	Yes(LNM)	Yes
Keyclick	No	Yes
Margin bell	No	Yes
Origin mode	Yes(DECOM)	No
Parity	No	Yes
Parity sense	No	Yes
Power	No	Yes
Receive speed	No	Yes
Screen	Yes(DECSCNM)	Yes
Scroll	Yes(DECSCLM)	Yes
Tabs	Yes(HTS/TBC)	Yes
Transmit speed	No	Yes
Wraparound	Yes(DECAWM)	Yes
# £ 3 (shifted)	Yes	Yes

*The appropriate control or escape sequence mnemonic is indicated in parentheses.

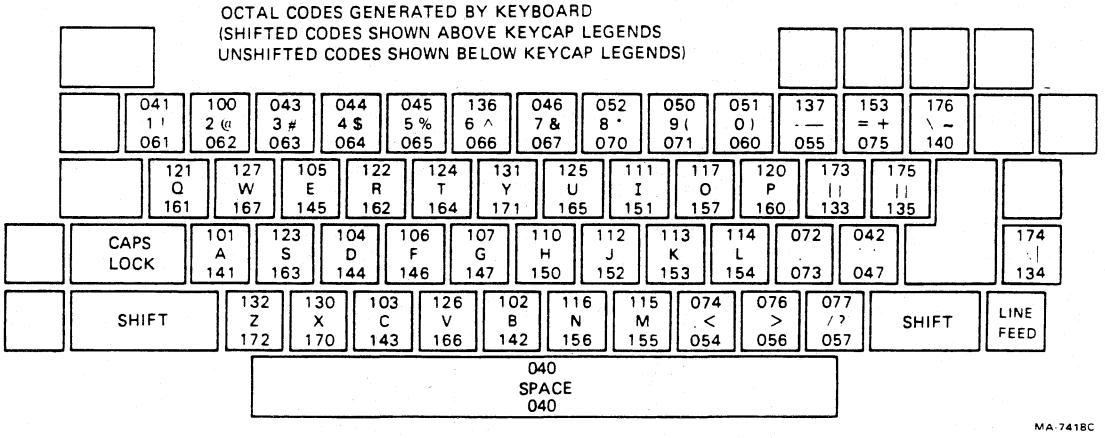


Figure A-3 Standard Key Codes

Table A-2 Function Key Codes

Key	Octal Value of Code Sent or Received by VT100	Action Terminal Would Take if Host Sent That Code
RETURN*	015	Carriage return function
LINE FEED	012	Line feed
BACKSPACE	010	Backspace function
TAB	011	Tab function
SPACE BAR	040	Deposit a space on the screen erasing what was there before
ESC	033	The initial delimiter of an escape sequence – interpret the following character string from the host as a command, rather than displaying it
DELETE	177	Ignored by the VT100

*You can use the new line SET-UP feature to redefine the **RETURN** key so that it issues 015_8 012_8 (carriage return — line feed).

Function Keys

Several keys on the keyboard transmit control codes. Control codes do not produce displayable characters but are codes for functions. If these codes are received by the terminal, the VT100 performs the associated function described in Table A-2.

NO SCROLL – Pressing **NO SCROLL** generates a single XOFF code and inhibits further scrolling. When pressed again the same key generates XON. In practice, if the software recognizes XOFF, the host stops transmitting until you press **NO SCROLL** again to allow scrolling. If the XOFF/XON feature is disabled (SET-UP function), **NO SCROLL** causes no action.

BREAK – Pressing **BREAK** forces the transmission line to its space state for 0.2333 seconds ± 10 percent. If either **SHIFT** key is down, the time increases to 3.5 seconds ± 10 percent.

Pressing **SHIFT** and **BREAK** together provide the long-break-disconnect function. Used with properly configured modems with RS232-C levels, it disconnects both the local and remote data sets. For modems connected via the 20 mA loop, issuing the long space may disconnect the remote data set only.

Pressing **CTRL** and **BREAK** together transmits the answerback message.

BREAK does not function when the VT100 is in LOCAL.

CTRL (Control) – Figure A-4 shows the keys that generate control characters. You can generate control characters in two ways.

1. Hold down **CTRL**, and press any of the unshaded keys in Figure A-4.

2. Press any of the shaded keys in Figure A-4 without using **CTRL**. The shaded keys are dedicated keys that generate control characters without using **CTRL**.

NOTE

You can change the RETURN key character code with the linefeed/new line feature. When off, this feature causes RETURN to generate a single control character (CR). When on, this feature causes RETURN to generate two characters (CR, LF). Also, depending on the auxiliary keypad mode selected, RETURN and ENTER may generate the same control codes.

Auto-Repeating

All keys auto-repeat except: **SET-UP**, **ESC**, **NO SCROLL**, **TAB**, **RETURN**, and any key pressed with **CTRL**. Auto-repeating may be disabled (SET-UP function). Auto-repeating works as follows: when you press a key, its code(s) is sent once, immediately. If you hold down the key for more than one-half second, the code(s) is sent repeatedly at a rate of approximately 30 Hz (less if low transmit baud rates are used) until you release the key.

Cursor Control Keys

The keyboard contains four keys labeled with arrows in each of four directions. These keys transmit escape sequences. If the host echoes these escape sequences back to the terminal, the cursor moves one character up, down, right, or left. Table A-3 describes the escape sequences generated by each key.

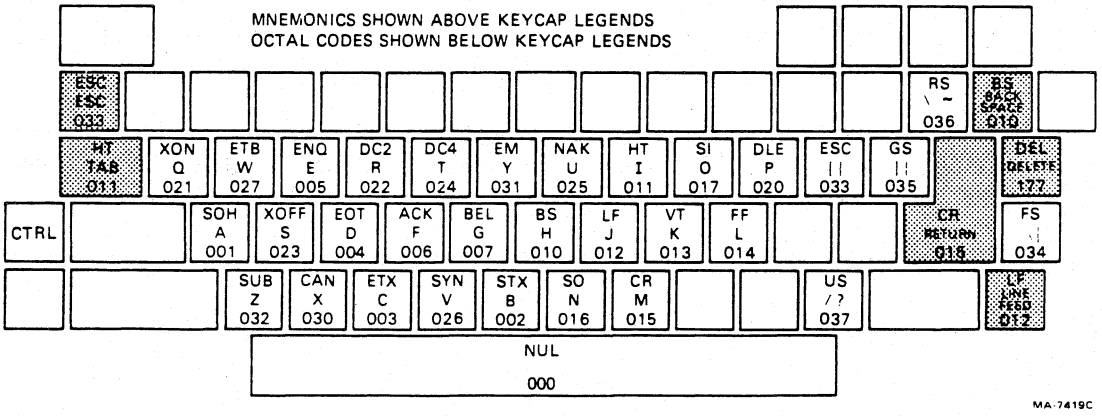


Figure A-4 Function Key Control Codes

Table A-3 Cursor Control Key Codes

Cursor Key	VT52 Mode	ANSI Mode and Cursor Key Mode Reset	ANSI Mode and Cursor Key Mode Set
Up	ESC A	ESC [A	ESC O A
Down	ESC B	ESC [B	ESC O B
Right	ESC C	ESC [C	ESC O C
Left	ESC D	ESC [D	ESC O D

AUXILIARY KEYPAD

The keys on the auxiliary keypad normally transmit codes for the numerals, decimal point, minus sign, and comma. **ENTER** transmits the same code as **RETURN**. The host cannot tell if these keys were pressed on the auxiliary keypad or on the main keyboard. Therefore, software that requires considerable numeric data entry need not be rewritten to use the keypad.

However, if software must distinguish between pressing a key on the auxiliary keypad and pressing the corresponding key on the main keyboard, the host can give the terminal a command to place it in keypad application mode. In keypad application mode all keys on the auxiliary keypad are defined to give escape sequences that may be used by the host as user-defined functions.

The codes sent by the auxiliary keypad for the four combinations of the VT52/ANSI mode and numeric keypad/application mode is listed in Table A-4. None of the keys are affected by pressing **SHIFT**, **CAPS LOCK**, or **CTRL**.

NOTE

In ANSI mode, if the codes are echoed back to the VT100, or if the terminal is in LOCAL, the last character of the sequence is displayed on the screen; for example, PF1 displays a "P."

SPECIAL GRAPHICS CHARACTERS

If you select the special graphics set, the graphics for ASCII codes 137_8 through 176_8 are replaced according to Table A-5. (See the SCS escape sequence.)

NOTE

Codes 152_8–156_8, 161_8 and 164_8–170_8 are used to draw rectangular grids. Each piece of this line drawing set is contiguous with others so that the lines formed are unbroken.

Codes 157_8–163_8 give better vertical resolution than dashes and underlines when drawing graphs. Using these segments 120 $\times$ 132 resolution may be obtained in 132 column mode with the advanced video option installed.

Table A-4 Auxiliary Keypad Codes

	ANSI Mode		VT52 Mode	
Key	Numeric Keypad Mode	Alternate Keypad Mode	Numeric Keypad Mode	Alternate Keypad Mode
0	**0** 060	**ESC O p** 033 117 160	**0** 060	**ESC ? P** 033 077 160
1	**1** 061	**ESC O q** 033 117 161	**1** 060	**ESC ? q** 033 077 161
2	**2** 062	**ESC O r** 033 117 162	**2** 062	**ESC ? r** 033 077 162
3	**3** 063	**ESC O s** 033 117 163	**3** 063	**ESC ? s** 033 077 163
4	**4** 064	**ESC O t** 033 117 164	**4** 064	**ESC ? t** 033 077 164
5	**5** 065	**ESC O u** 033 117 165	**5** 065	**ESC ? u** 033 077 165
6	**6** 066	**ESC O v** 033 117 166	**6** 066	**ESC ? v** 033 077 166
7	**7** 067	**ESC O w** 033 117 167	**7** 067	**ESC ? w** 033 077 167
8	**8** 070	**ESC O x** 033 117 170	**8** 070	**ESC ? x** 033 077 170
9	**9** 071	**ESC O y** 033 117 171	**9** 071	**ESC ? y** 033 077 171
†	**† (minus)** 055	**ESC O m** 033 117 155	**— (minus)*** 055	**ESC ? m** 033 077 155*
,	**, (comma)** 054	**ESC O l** 033 117 154	**, (comma)*** 054	**ESC ? l** 033 077 054†
.	**. (period)** 056	**ESC O n** 033 117 156	**. (period)** 056	**ESC ? n** 033 077 156

Table A-4 Auxiliary Keypad Codes (Cont)

Key	ANSI Mode						VT52 Mode					
	Numeric Keypad Mode			Alternate Keypad Mode			Numeric Keypad Mode			Alternate Keypad Mode		
ENTER†	**CR or** 015	**CR** 015	**LF** 012	**ESC** 033	**O** 117	**M** 115	**CR or** 015	**CR** 015	**LF** 012	**ESC** 033	**?** 077	**M** 115
PF1	**ESC** 033	**O** 117	**P** 120	**ESC** 033	**O** 117	**P** 120	**ESC** 033	**P** 120		**ESC** 033	**?** 077	**P** 120
PF2	**ESC** 033	**O** 117	**Q** 121	**ESC** 033	**O** 117	**Q** 121	**ESC** 033	**Q** 121		**ESC** 033	**?** 077	**Q** 121
PF3	**ESC** 033	**O** 117	**R** 122	**ESC** 033	**O** 117	**R** 122	**ESC** 033	**R** 122		**ESC** 033	**?** 077	**R** 122
PF4	**ESC** 033	**O** 117	**S** 123	**ESC** 033	**O** 117	**S** 123	**ESC** 033	**S*** 123		**ESC** 033	**?** 077	**S*** 123

*These sequences were not available in the VT52. Do not use the PF4, "—" (minus), or "," (comma) keys with VT52 with VT52 software.

†When numeric keypad mode is selected (alternate keypad mode off), the **ENTER** character code can be changed by the line feed/new line feature. When off, this feature causes **ENTER** to generate a single control character (CR, octal 015). When on, this feature causes **ENTER** to generate two characters (CR, octal 015 and LF, octal 012).

Table A-5 Special Graphics Characters

Octal Code	US or UK Set	Special Graphics Set	
137			Blank
140	`	♦	Diamond
141	a	▒	Checkerboard (error indicator)
142	b	␉	HT (horizontal tab)
143	c	␌	FF (form feed)
144	d	␍	CR (carriage return)
145	e	␊	LF (line feed)
146	f	°	Degree symbol
147	g	±	Plus/minus ±
150	h	␤	NL (new line)
151	i	␋	VT (vertical tab)
152	j	┘	Lower-right corner
153	k	┐	Upper-right corner
154	l	┌	Upper-left corner
155	m	└	Lower-left corner
156	n	┼	Crossing lines
157	o	⎺	Horizontal line – scan 1
160	p	⎻	Horizontal line – scan 3
161	q	─	Horizontal line – scan 5
162	r	⎼	Horizontal line – scan 7
163	s	⎽	Horizontal line – scan 9
164	t	├	Left T
165	u	┤	Right T
166	v	┴	Bottom T
167	w	┬	Top T
170	x	│	Vertical bar
171	y	≤	Less than or equal to
172	z	≥	Greater than or equal to
173	{	π	Pi (mathematical)
174	|	≠	Not equal to
175	}	£	UK pound sign
176	~	·	Centered dot

COMMUNICATION PROTOCOLS

Full-Duplex

The terminal can operate at transmission speeds up to 19,200 baud. However, the terminal may not be able to keep up with incoming data. The terminal stores incoming characters in a 64-character buffer (128 characters in later model terminals) and processes them on a first-in/first-out basis. When the content of the buffer reaches 48 characters, the terminal transmits 023_8 (XOFF or DC3). On this signal the host should suspend its transmission to the terminal. Eventually, if the host stops transmitting, the terminal depletes the buffer. When 16 characters remain in the buffer the terminal transmits 021_8 (XON or DC1) to signal the host that it may resume transmission.

If the host fails to respond to an XOFF from the terminal in a timely manner, the buffer continues to fill. When the 64-character capacity of the buffer is exceeded, a condition occurs called buffer overflow. To determine if the buffer will overflow use the following formulas.

No. of chars to overflow = 16 − [3 × (receiver speed/transmit speed)]

Time to respond to XOFF = No. of chars to overflow × (bits/char + parity bit + 2)/receiver speed

Example

The VT100 is transmitting 8-bit characters with no parity at 1200 baud and receiving at 1200 baud. The terminal has just sent an XOFF which the host must respond to within 0.1083 second to avoid a buffer overflow.

No. of chars to overflow = 16 − [(3 × 1200/1200)] = 13 chars

Time to respond to XOFF = 13 × (8+0+2)/1200 = 0.1083 sec

Example

The VT100 is transmitting 7-bit characters with parity at 300 baud and receiving at 1200 baud. The terminal has just sent an XOFF which the host must respond to within 0.0333 second to avoid a buffer overflow.

No. of chars to overflow = 16 − [(3 × 1200/300)] = 4 chars

Time to respond to XOFF = 4 × (7+1+2)/1200 = 0.0333 sec

If the buffer overflows, the VT100 begins to discard incoming characters and the error character is displayed.

Software that does not support receipt of XOFF/XON signals from the terminal can still use the VT100 provided the software never sends the ESC code to the terminal, the baud rate is limited to 4800 or less, and the software does not use smooth scrolling or split screen features.

Two of the terminal functions, Reset and Self-Test, reinitialize the terminal and erase the buffer. Thus if characters are received after the commands to perform these two functions and the characters are placed in the buffer, the characters are destroyed without being processed.

To compensate for this, the host may act in one of two ways.

1. Immediately after sending the terminal the commands to perform either the Reset or Self-Test functions, the host may act as if it had received XOFF from the terminal, thus sending no more characters until it receives XON. The terminal transmits XON only after it completes the specified operation and the XOFF/XON feature is enabled.

2. When the first method cannot be implemented, a delay of no less than 10 seconds may be used to allow the terminal time to complete the invoked function. This method, however, does not guarantee against the loss of data when an invoked function has detected an error. And while this delay is currently adequate, future options may require a change in the time delay.

The XOFF/XON synchronization scheme has an advantage over requiring the host to insert delays or filler characters in its data stream. Requiring a minimum of software support, XON/XOFF ensures that every character or command sent to the VT100 is processed in correct order. It frees interface programs from all timing considerations and results in more reliable operation.

In addition to the buffer-filling condition, there are two other means of transmitting XOFF and XON: the **NO SCROLL** key, and **CTRL-S/CTRL-Q**. If XOFF mode is enabled, the VT100 coordinates these three sources of XOFF and XON so that the desired effect occurs. For example, if the buffer-filling condition causes an XOFF to be sent and then you press **NO SCROLL**, a second XOFF is not sent. Instead of sending an XON when the buffer empties, the VT100 waits until you press **NO SCROLL** again before sending XON.

Also, entering SET-UP mode causes the VT100 to temporarily stop taking characters from the buffer. An XOFF is sent if the buffer becomes nearly full.

CTRL-S and **CTRL-Q** are also synchronized with **NO SCROLL**.

If the XOFF feature is disabled, the buffer-filling condition does not send an XOFF, **NO SCROLL** is disabled, and **CTRL-S** and **CTRL-Q** are transmitted as typed.

The VT100 also recognizes received XOFF and XON. Receipt of XOFF inhibits the VT100 from transmitting any codes except XOFF and XON. From three to seven keystrokes on the keyboard are stored in a keyboard buffer (some keys transmit two or three codes, e.g., cursor controls). If the keyboard buffer overflows, keyclicks stop and the KBD LOCKED LED lights. Transmission resumes upon receipt of XON.

If the user transmits an XOFF to the host (by **CTRL-S** or **NO SCROLL**), the host should not echo any further type-in until the user types XON. This places the burden of not overloading the host's output buffer on the user.

Entering and exiting SET-UP clears the transmit and keyboard locked modes.

TERMINAL CONTROL COMMANDS

The VT100 has many control commands that cause it to take action other than displaying a character on the screen. In this way, the host commands the terminal to move the cursor, change modes, ring the bell, etc. The following paragraphs discuss terminal control commands.

Control Characters

Control characters have values of 000_8–037_8, and 177_8. The control characters recognized by the VT100 are listed in Table A-6. All other control codes have no effect.

Escape Sequences

Table A-7 summarizes the VT100 escape sequences.

Table A-6 Control Characters

Octal Char	Code	Action Taken
NUL	000	Ignored on input (not stored in input buffer; see full duplex protocol).
ENQ	005	Transmit answerback message.
BEL	007	Sound bell tone from keyboard.
BS	010	Move cursor left one character position, unless it is at left margin in which case no action occurs.
HT	011	Move cursor to next tab stop, or to right margin if no further tab stops are present on line.
LF	012	Causes line feed or new line operation. (See new line mode.)
VT	013	Interpreted as LF.
FF	014	Interpreted as LF.
CR	015	Move cursor to left margin on current line.
SO	016	Select G1 character set, as selected by ESC) sequence.
SI	017	Select G0 character set, as selected by ESC(sequence.
XON	021	Causes terminal to resume transmission.
XOFF	023	Causes terminal to stop transmitting all codes except XOFF and XON.
CAN	030	If sent during an escape or control sequence, the sequence is immediately terminated and not executed. It also causes the error character to be displayed.
SUB	032	Interpreted as CAN.
ESC	033	Introduces an escape sequence.
DEL	177	Ignored on input (not stored in input buffer).

Table A-7 VT100 Escape Sequences Summary

Feature	VT52 Compatible Mode
Cursor up	ESC A
Cursor down	ESC B
Cursor right	ESC C
Cursor left	ESC D
Select special graphics character set	ESC F
Select ASCII character set	ESC G
Cursor to home	ESC H
Reverse line feed	ESC I
Erase to end of screen	ESC J
Erase to end of line	ESC K
Direct cursor address	ESC Ylc*
Identify	ESC Z†
Enter alternate keypad mode	ESC =
Exit alternate keypad mode	ESC >
Graphics processor on	ESC 1‡
Graphics processor off	ESC 2‡
Enter ANSI mode	ESC <

*Line and column numbers for direct cursor address are single character codes whose values are the desired number plus 37_8. Line and column numbers start at 1.

†Response to ESC Z is ESC / Z.

‡Ignored except in VT105.

ANSI Compatible Mode

Cursor Movement Commands	
Cursor up	ESC [Pn A
Cursor down	ESC [Pn B
Cursor forward (right)	ESC [Pn C
Cursor backward (left)	ESC [Pn D
Direct cursor addressing	ESC [Pl; Pc H * or ESC [Pl; Pc f *
Index	ESC D
Reverse index	ESC M
Save cursor and attributes	ESC 7
Restore cursor and attributes	ESC 8

*Pl = line number; Pc = column number.

NOTE

Pn refers to a decimal parameter expressed as a string of ASCII digits. Multiple parameters are separated by the semicolon character (073_8). If a parameter is omitted or specified to be 0 the default parameter value is used. For the cursor movement commands, the default parameter value is 1.

Line Size (Double-height and Double-width) Commands

Change this line to double-height top half	ESC#3
Change this line to double-height bottom half	ESC#4
Change this line to single-width single-height	ESC#5
Change this line to double-width single-height	ESC#6

Character Attributes

ESC [Ps;Ps;Ps;....;Ps m

Ps refers to a selective parameter. Multiple parameters are separated by the semicolon character (073_8). The parameters are executed in order and have the following meanings.

0 or none	All attributes off
1	Bold on
4	Underscore on
5	Blink on
7	Reverse video on

Any other parameter values are ignored.

Erasing

From cursor to end of line	ESC [K or ESC [O K
From beginning of line to cursor	ESC [1 K
Entire line containing cursor	ESC [2 K
From cursor to end of screen	ESC [J or ESC [O J
From beginning of screen to cursor	ESC [1 J
Entire screen	ESC [2 J

Programmable LEDs

ESC [Ps; Ps;...Ps q

Ps are selective parameters separated by semicolons (073_8) and executed in order, as follows.

0 or none	All LEDs off
1	LED 1 on
2	LED 2 on
3	LED 3 on
4	LED 4 on

Any other parameter values are ignored.

Character Sets (G0 and G1 Designators)

The G0 and G1 character sets are designated as follows.

Character Set	**G0**	**G1**
United Kingdom (UK)	ESC (A	ESC) A
United States (USASCII)	ESC (B	ESC) B
Special graphics characters and line drawing set	ESC (0	ESC) 0
Alternate character ROM	ESC (1	ESC) 1
Alternate character ROM special graphics characters	ESC (2	ESC) 2

Scrolling Region
ESC [Pt ; Pb r

Pt is the number of the top line of the scrolling region. Pb is the number of the bottom line of the scrolling region and must be greater than Pc.

Tab Stops

Set tab at current column	ESC H
Clear tab at current column	ESC [g or ESC [0 g
Clear all tabs	ESC [3 g

Modes

	To Set		To Reset	
Mode Name	**Mode**	**Sequence**	**Mode**	**Sequence**
Line feed/new line	New line	ESC [20h	Line feed	ESC [20l
Cursor key mode	Application	ESC [?1h	Cursor	ESC [?1l
ANSI/VT52	ANSI	N/A	VT52	ESC [?2l
Column mode	132 column	ESC [?3h	80 column	ESC [?3l
Scrolling mode	Smooth	ESC [?4h	Jump	ESC [?4l
Screen mode	Reverse	ESC [?5h	Normal	ESC [?5l
Origin mode	Relative	ESC [?6h	Absolute	ESC [?6l
Wraparound	On	ESC [?7h	Off	ESC [?7l
Auto repeat	On	ESC [?8h	Off	ESC [?8l
Interlace	On	ESC [?9h	Off	ESC [?9l
Graphics processor option	On	ESC 1	Off	ESC 2
Keypad mode	Application	ESC =	Numeric	ESC >

Reports

Cursor Position Report

Invoked by	ESC [6 n
Response is	ESC [Pl ; Pc R (Pl = line number and Pc = column number)

Status Report

Invoked by	ESC [5 n
Response is	ESC [0 n (terminal ok) ESC [3 n (terminal not ok)

What Are You

Invoked by	ESC [c or ESC [O c
Response is	ESC [? 1 ; Ps c

Ps is the "option present" parameter with the following meaning.

Ps	Meaning
0	Base VT100, no options
1	Processor option (STP)
2	Advanced video option (AVO)
3	AVO and STP
4	Graphics processor option (GO)
5	GO and STP
6	GO and AVO
7	GO, STP, and AVO

Alternately invoked by ESC Z (not recommended). Response is the same.

Reset

Reset executes the power-up reset routine.

ESC c

Confidence Tests

Fill screen with "Es"	ESC # 8
Invoke test(s)	ESC [2 ; Ps y

Ps is the parameter indicating the test to be done and is a decimal number computed by taking the "weight" indicated for each desired test and adding them together.

Test	Weight
Power-up self-test (ROM checksum, RAM, NVR, keyboard and AVO if installed)	1
Data loopback	2 (Loopback connector required)
Repeat selected tests(s) indefinitely (until failure or power off)	8

Valid ANSI Mode Escape Sequences (Detailed)

Definitions – The following listing defines the basic elements of the ANSI mode escape sequences. (See Appendix D for a detailed explanation.)

Control Sequence Introducer (CSI) – An escape sequence that provides supplementary controls and is itself a prefix affecting the interpretation of a limited number of contiguous characters. In the VT100 the CSI is ESC [.

Parameter – (1) A string of one or more decimal characters that represent a single value; (2) The value so represented.

Numeric Parameter – A string of characters that represent a number, designated by Pn. Pn has a range of 0 to 9 (60_8 to 71_8).

Selective Parameter – A string of characters that selects a subfunction from a specified list of subfunctions, designated by Ps. In general, a control sequence with more than one selective parameter causes the same effect as several control sequences, each with one selective parameter; for example, CSI Psa; Psb; Psc F is identical to CSI Psa F CSI Psb F CSI Psc F.

Ps is a string of zero or more characters with a range of 0 to 9 (60_8 to 71_8) with each selective parameter separated from the other by a ; (semicolon, 73_8).

Default – A function-dependent value assumed when no explicit value, or a value of 0, is specified.

Final Character – A character whose bit combination terminates an escape or control sequence.

Escape sequences – All of the following escape and control sequences are transmitted from the host computer to the VT100 unless otherwise noted. All of the escape sequences are a subset of those specified in ANSI X3.64-1977 and ANSI X3.41-1974.

CPR Cursor Position Report – VT100 to Host

Format: ESC [Pn; Pn R **default values: 1**

The CPR sequence reports the active position by using the parameters. This sequence has two parameter values, the first specifying the line and the second specifying the column. The default condition with no parameters present, or parameters of 0, is equivalent to a cursor at home position.

Numbering of lines depends on the state of the Origin mode (DECOM).

This control sequence is solicited by a device status report (DSR) sent from the host.

CUB Cursor Backward – Host to VT100 and VT100 to Host

Editor Function; format: ESC [Pn D **default value: 1**

The CUB sequence moves the active position to the left. The distance moved is determined by the parameter. If the parameter value is 0 or 1, the active position moves one position to the left. If the parameter value is n, the active position moves n positions to the left. If an attempt is made to move the cursor to the left of the left margin, the cursor stops at the left margin.

CUD Cursor Down – Host to VT100 and VT100 to Host

Editor Function; format: ESC [Pn B **default value: 1**

The CUD sequence moves the active position downward without altering the column position. The number of lines moved is determined by the parameter. If the parameter value is 0 or 1, the active position moves one line downward. If the parameter value is n, the active position moves n lines downward. If an attempt is made to move the cursor below the bottom margin, the cursor stops at the bottom margin.

CUF Cursor Forward – Host to VT100 and VT100 to Host

Editor Function; format: ESC [Pn C **default value: 1**

The CUF sequence moves the active position to the right. The distance moved is determined by the parameter. A parameter value of 0 or 1 moves the active position one position to the right. A parameter value of n moves the active position n positions to the right. If an attempt is made to move the cursor to the right of the right margin, the cursor stops at the right margin.

CUP Cursor Position

Editor Function; format: ESC [Pn; Pn H **default value: 1**

The CUP sequence moves the active position to the position specified by the parameters. This sequence has two parameter values, the first specifying the line position and the second specifying the column position. A parameter value of 0 or 1 for the first or second parameter moves the active position to the first line or column in the display, respectively. The default condition with no parameters present is equivalent to a cursor to home action. In the VT100, this control behaves identically with its format effector counterpart, HVP.

The numbering of lines depends on the state of the Origin mode (DECOM).

CUU Cursor Up – Host to VT100 and VT100 to Host

Editor Function; format: ESC [Pn A **default value: 1**

This sequence moves the active position upward without altering the column position. The number of lines moved is determined by the parameter. A parameter value of 0 or 1 moves the active position one line upward. A parameter value of n moves the active position n lines upward. If an attempt is made to move the cursor above the top margin, the cursor stops at the top margin.

DA Device Attributes

Format: ESC [Pn c **default value: 0**

1. The host requests the VT100 to send a device attributes (DA) control sequence to identify itself by sending the DA control sequence with either no parameter or a parameter of 0.

2. Response to the request described above (VT100 to host) is generated by the VT100 as a DA control sequence with the numeric parameters as follows:

Option Present	Sequence Sent
No options	ESC [?1;0c
Processor option (STP)	ESC [?1;1c
Advanced video option (AVO)	ESC [?1;2c
AVO and STP	ESC [?1;3c
Graphics option (GO)	ESC [?1;4c
GO and STP	ESC [?1;5c
GO and AVO	ESC [?1;6c
GO, STP, and AVO	ESC [?1;7c

DECALN Screen Alignment Display (DEC Private)

Format: ESC #8

This command fills the entire screen area with uppercase Es for screen focus and alignment. This command is used by DIGITAL manufacturing and Field Service personnel.

DECANM ANSI/VT52 Mode (DEC Private)

This is a private parameter applicable to set mode (SM) and reset mode (RM) control sequences. The reset state causes only VT52 compatible escape sequences to be interpreted and executed. The set state causes only ANSI "compatible" escape and control sequences to be interpreted and executed.

DECARM Auto Repeat Mode (DEC Private)

This is a private parameter applicable to set mode (SM) and reset mode (RM) control sequences. The reset state causes no keyboard keys to autorepeat. The set state causes certain keyboard keys to autorepeat.

DECAWM Autowrap Mode (DEC Private)

This is a private parameter applicable to set mode (SM) and reset mode (RM) control sequences. The reset state causes any displayable characters received when the cursor is at the right margin to replace any previous characters there. The set state causes these characters to advance to the start of the next line, doing a scroll up if required and permitted.

DECCOLM Column Mode (DEC Private)

This is a private parameter applicable to set mode (SM) and reset mode (RM) control sequences. The reset state causes a maximum of 80 columns on the screen. The set state causes a maximum of 132 columns on the screen.

DECCKM Cursor Keys Mode (DEC Private)

This is a private parameter applicable to set mode (SM) and reset mode (RM) control sequences. This mode is only effective when the terminal is in keypad application mode (see DECKPAM) and the ANSI/VT52 mode (DECANM) is set (see DECANM). Under these conditions, if the cursor key mode is reset, the four cursor function keys send ANSI cursor control commands. If cursor key mode is set, the four cursor function keys send application functions.

DECDHL Double-Height Line (DEC Private)

Format: Top Half: ESC #3, Bottom Half: ESC #4

These sequences cause the line containing the active position to become the top or bottom half of a double-height double-width line. The sequences must be used in pairs on adjacent lines and the same character output must be sent to both lines to form full double-height characters. If the line was single-width single-height, all characters to the right of the center of the screen are lost. The cursor remains over the same character position unless it would be to the right of the right margin, in which case it is moved to the right margin.

DECDWL Double-Width Line (DEC Private)

Format: ESC #6

This sequence causes the line that contains the active position to become double-width, single-height. If the line was single-width, single-height, all characters to the right of screen center are lost. The cursor remains over the same character position unless it would be to the right of the right margin, in which case, it is moved to the right margin.

DECGOFF Graphics Processor OFF (DEC Private)

Format: ESC 2

Turn off the VT105 graphics processor.

NOTE
Some DIGITAL hardcopy terminals interpret this private escape sequence as CLEAR TABS.

DECGON Graphics Processor On (DEC Private)

Format: ESC 1

All subsequent characters are interpreted as commands or data to the VT105 graphics processor option. The terminal remains in this mode until the graphics processor off command is received. This command is ignored if no graphics processor option is installed.

NOTE
Some DIGITAL hardcopy terminals interpret this private escape sequence as SET TAB.

DECHCP Hard Copy (DEC Private)

Format: ESC #7

This sequence causes the screen to cease updating and freeze while the hardcopy output is enabled. The screen resumes normal operation when the hardcopy has been completed. This command is ignored if no hardcopy option is installed.

DECID Identify Terminal (DEC Private)

Format: ESC Z

This sequence causes the same response as the ANSI device attributes (DA). DECID will not be supported in future DIGITAL terminals, therefore, DA should be used by any new software.

DECINLM Interlace Mode (DEC Private)

This is a private parameter applicable to set mode (SM) and reset mode (RM) control sequences. The reset state (noninterlace) causes the video processor to display 240 scan lines per frame. The set state (interlace) causes the video processor to display 480 scan lines per frame. There is no increase in character resolution.

DECKPAM Keypad Application Mode (DEC Private)

Format: ESC =

Auxiliary keypad keys and cursor control keys transmit escape sequences.

DECKPNM Keypad Numeric Mode (DEC Private)

Format: ESC >

Auxiliary keypad keys send ASCII codes corresponding to the characters on the keys. Cursor control keys send cursor controls.

DECLL Load LEDs (DEC Private)

Format: ESC [Ps q **default value: 0**

Load the four programmable LEDs on the keyboard according to the parameter(s).

Parameter	Meaning
0	Clear LEDs 1 through 4
1	Light LED 1
2	Light LED 2
3	Light LED 3
4	Light LED 4

LED numbers are indicated on the keyboard.

DECOM Origin Mode (DEC Private)

This is a private parameter applicable to set mode (SM) and reset mode (RM) control sequences. The reset state causes the origin to be at the upper-left character position on the screen. Line numbers are therefore independent of current margin settings. The cursor may be positioned outside the margins with a cursor position (CUP) or horizontal and vertical position (HVP) control.

The set state causes the origin to be at the upper-left character position within the margins. Line numbers are therefore relative to the current margin settings. The cursor cannot be positioned outside the margins.

The cursor moves to the new home position when this mode is set or reset.

Lines and columns are numbered consecutively, with the origin being line 1, column 1.

DECRC Restore Cursor (DEC Private)

Format: ESC 8

This sequence causes the previously saved cursor position, graphic rendition, and character set to be restored.

DECREPTPARM Report Terminal Parameters

Format: ESC [<sol>; <par>; <nbits>; <xspeed>; <rspeed>; <clkmul>; <flags>x

These sequence parameters are explained below in the DECREQTPARM sequence.

DECREQTPARM Request Terminal Parameters

Format: ESC [<sol>x

This sequence is sent by the terminal controller to notify the host of the status of selected terminal parameters. The status sequence may be sent when requested by the host or at the terminal's discretion. DECREPTPARM is sent upon receipt of a DECREQTPARM.

The meanings of the sequence parameters are:

Parameter	Value	Meaning
<sol>	0 or none	This message is a request (DECREQTPARM). The terminal is allowed to send unsolicited reports.
	1	This message is a request. From now on the terminal may only report in response to a request.
	2	This message is a report (DECREPTPARM).
	3	This message is a report and the terminal is only reporting on request.
<par>	1	No parity set
	4	Parity is set and odd
	5	Parity is set and even
<nbits>	1	8 bits per character
	2	7 bits per character
<xspeed>		Bits per second
<rspeed>	0	50
	8	75
	16	110
	24	134.5
	32	150
	40	200
	48	300
	56	600
	64	1200
	72	1800
	80	2000
	88	2400
	96	3600
	104	4800
	112	9600
	120	19,200
<clkmul>	1	The bit rate multiplier is 16.
<flags>	0–15	This value communicates the four switch values in block 5 of SET UP B, which are only visible to the user when an STP option is installed. These bits may be assigned for an STP device. The four bits are a decimal-encoded binary number.

DECSC Save Cursor (DEC Private)

Format: ESC 7

This sequence causes the cursor position, graphic rendition, and character set to be saved. (See DECRC.)

DECSCLM Scrolling Mode (DEC Private)

This is a private parameter applicable to set mode (SM) and reset mode (RM) control sequences. The reset state causes scrolls to "jump" immediately. The set state causes scrolls to be "smooth" at a maximum rate of six lines per second.

DECSCNM Screen Mode (DEC Private)

This is a private parameter applicable to set mode (SM) and reset mode (RM) control sequences. The reset state causes the screen to be black with white characters. The set state causes the screen to be white with black characters.

DECSTBM Set Top and Bottom Margins (DEC Private)

Format: ESC [Pn; Pn r **default values: (see below)**

This sequence sets the top and bottom margins to define the scrolling region. The first parameter is the line number of the first line in the scrolling region. The second parameter is the line number of the bottom line in the scrolling region. Default is the entire screen (no margins). The minimum size of the scrolling region allowed is two lines, that is, the top margin must be less than the bottom margin.

DECSWL Single-Width Line (DEC Private)

Format: ESC #5

This causes the line that contains the active position to become single-width, single-height. The cursor remains on the same character position. This is the default condition for all new lines on the screen.

DECTST Invoke Confidence Test

Format: ESC [2 ; Ps y

Ps is the parameter indicating the test to be done. Ps is computed by taking the weight indicated for each desired test and adding them together. If Ps is 0, no test is performed but the VT100 is reset.

Test	Weight
Power up self-test (ROM checksum, RAM, NVR keyboard and AVO if installed)	1
Data Loopback	2 (loopback connector required)
Repeat selected test(s) indefinitely (until failure or power off)	8

DSR Device Status Report

Format: ESC [Ps r **default value: 0**

Requests and reports the general status of the VT100 according to the following parameter(s).

Parameter	Meaning
0	Response from VT100 – ready, no malfunctions detected (default)
3	Response from VT100 – malfunction – retry
5	Command from host – please report status (using a DSR control sequence)
6	Command from host – please report active position (using a CPR control sequence)

DSR with a parameter value of 0 or 3 is always sent as a response to a requesting DSR with a parameter value of 5.

ED Erase In Display

Editor Function; format: ESC [Ps J **default value: 0**

This sequence erases some or all characters in the display according to the parameter. Any complete line erased by this sequence returns that line to single-width mode.

Parameter	Meaning
0	Erase from the active position to the end of the screen, inclusive (default).
1	Erase from start of the screen to the active position, inclusive.
2	Erase all of the display — all lines are erased, changed to single-width, and the cursor does not move.

EL Erase In Line

Editor Function; format: ESC [Ps K **default value: 0**

Erases some or all characters in the active line according to the parameter.

Parameter	Meaning
0	Erase from the active position to the end of the line, inclusive (default).
1	Erase from the start of the screen to the active position, inclusive.
2	Erase all of the line, inclusive.

HTS Horizontal Tabulation Set

Format Effector; format: ESC H

Set one horizontal stop at the active position.

HVP Horizontal and Vertical Position

Format Effector, format: ESC [Pn; Pn f **default value: 1**

Moves the active position to the position specified by the parameters. This sequence has two parameter values; the first specifies the line position, the second specifies the column. A parameter value of either zero or one causes the active position to move to the first line or column in the display, respectively. The default condition with no parameters present moves the active position to the home position. In the VT100, this control behaves identically with its editor function counterpart, CUP. Numbering lines and columns depends on the reset or set state of the origin mode (DECOM).

IND Index

Format Effector; format: ESC D

This sequence causes the active position to move downward one line without changing column position. If the active position is at the bottom margin, a scroll up is performed.

LNM Line Feed/New Line Mode

This is a parameter applicable to set mode (SM) and reset mode (RM) control sequences. The reset state causes the interpretation of the line feed (LF), defined in ANSI Standard X3.4-1977, to imply only vertical movement of the active position and causes the return key (CR) to send the single code CR. The set state causes the LF to imply movement to the first position of the following line and causes the return key to send the two codes (CR, LF). This is the new line (NL) option.

This mode does not affect the index (IND), or next line (NEL) format effectors.

NEL Next Line

Format Effector; format: ESC E

This sequence causes the active position to move to the first position on the next line downward. If the active position is at the bottom margin, a scroll up is performed.

RI Reverse Index

Format Effector; format: ESC M

Moves the active position to the same horizontal position on the preceding line. If the active position is at the top margin, a scroll down is performed.

RIS Reset to Initial State

Format: ESC c

Resets the VT100 to its initial state, i.e., the state it has after it is powered on. This also causes the execution of the power-up self test and signal INIT H to be asserted briefly.

RM Reset Mode

Format: ESC [Ps ;Ps ; ...; Ps l **default value: none**

Resets one or more VT100 modes as specified by each selective parameter in the parameter string. Each mode to be reset is specified by a separate parameter. (See modes and set mode (SM) following this section.)

SCS Select Character Set

The appropriate G0 and G1 character sets are selected from the five possible character sets. G0 and G1 are selected by codes SI and SO (shift in and shift out) respectively.

G0 Sets Sequence	G1 Sets Sequence	Meaning
ESC (A	ESC) A	United Kingdom set
ESC (B	ESC) B	ASCII set
ESC (0	ESC) 0	Special graphics
ESC (1	ESC) 1	Alternate character ROM Standard character set
ESC (2	ESC) 2	Alternate character ROM Special graphics

The United Kingdom and ASCII sets conform to the "ISO international register of character sets to be used with escape sequences." The other sets are private character sets. Special graphics means that the graphic characters for the codes 137_8 to 176_8 are replaced with other characters. The specified character set will be used until another SCS is received.

SGR Select Graphic Rendition

Format Effector; format: ESC [Ps; ...; Ps m **default value: 0**

Invoke the graphic rendition specified by the parameter(s). All following characters transmitted to the VT100 are rendered according to the parameter(s) until the next occurrence of SGR.

Parameter	Meaning
0	Attributes off
1	Bold or increased intensity
4	Underscore
5	Blink
7	Negative (reverse) image

All other parameter values are ignored.

Without the advanced video option only one character attribute is possible as determined by the cursor selection. In that case specifying either the underscore or the reverse attribute activates the currently selected attribute.

SM Set Mode

Format: ESC [Ps; ...; Ps h **default value: none**

Causes one or more modes to be set within the VT100 as specified by each selective parameter in the parameter string. Each mode to be set is specified by a separate parameter. A mode is considered set until it is reset by a reset mode (RM) control sequence.

TBC Tabulation Clear

Format Effector; format: ESC [Ps g **default value: 0**

Parameter	Meaning
0	Clear the horizontal tab stop at the active position (the default case).
3	Clear all horizontal tab stops.

Any other parameter values are ignored.

MODES

You can change the following VT100 modes with set mode (SM) and reset mode (RM) controls.

ANSI Specified Modes

Parameter	Mode Mnemonic	Function
0	–	Error (ignored)
20	LNM	Line feed/new line mode

DEC Private Modes

If the first character in the parameter string is ? (77_8), the parameters are interpreted as DEC private parameters according to the following modes.

Parameter	Mode Mnemonic	Function
0	– –	Error (ignored)
1	DECCKM	Cursor key
2	DECANM	ANSI/VT52
3	DECCOLM	Column
4	DECSCLM	Scrolling
5	DECSCNM	Screen
6	DECOM	Origin
7	DECAWM	Auto-wrap
8	DECARM	Auto-repeat
9	DECINLM	Interlace

Any other parameter values are ignored.

The following modes, specified in ANSI X3.64-1977 standard, may be considered to be permanently set, permanently reset, or not applicable, as noted. Refer to that standard for further information concerning these modes.

Mnemonic	Function	State
CRM	Control representation	Reset
EBM	Editing boundary	Reset
ERM	Erasure	Set
FEAM	Format effector action	Reset
FETM	Format effector transfer	Reset
GATM	Guarded area transfer	NA
HEM	Horizontal editing	NA
IRM	Insertion-replacement	Reset
KAM	Keyboard action	Reset
MATM	Multiple area transfer	NA
PUM	Positioning unit	Reset
SATM	Selected area transfer	NA
SRTM	Status reporting transfer	Reset
TSM	Tabulation stop	Reset
TTM	Transfer termination	NA
VEM	Vertical editing	NA

Valid VT52 Mode Escape Sequences (detailed)

Graphics Processor On

Format: ESC 1

All subsequent characters are interpreted as commands to the graphics option until the graphics processor off command is received. This sequence is ignored if no graphics processor is installed.

Graphics Processor Off

Format: ESC 2

Turn off the graphics processor.

Cursor Up

Format: ESC A

Move the active position upward one position without altering the horizontal position. If an attempt is made to move the cursor above the top margin, the cursor stops at the top margin.

Cursor Down

Format: ESC B

Move the active position downward one position without altering the horizontal position. If an attempt is made to move the cursor below the bottom margin, the cursor stops at the bottom margin.

Cursor Right

Format: ESC C

Move the active position to the right. If an attempt is made to move the cursor to the right of the right margin, the cursor stops at the right margin.

Cursor Left

Format: ESC D

Move the active position one position to the left. If an attempt is made to move the cursor to the left of the left margin, the cursor stops at the left margin.

Enter Graphics Mode

Format: ESC F

Selects the special graphics character set.

NOTE
The special graphics characters in the VT100 are different from those in the VT52. (See Table A-8.)

Exit Graphics Mode

Format: ESC G

Selects the standard ASCII character set.

Cursor to Home

Format: ESC H

Move the cursor to the home position.

Reverse Line Feed

Format: ESC I

Move the active position upward one position without altering the column position. If the active position is at the top margin, a scroll down is performed.

Erase to End of Screen

Format: ESC J

Erase all characters from the active position to the end of the screen. The active position is not changed.

Erase to End of Line

Format: ESC K

Erase all characters from the active position to the end of the current line. The active position is not changed.

Table A-8 Special Character and Line Drawing Set and Graphics Mode Comparison

Octal Code	US/UK Set	Special Character and Line Drawing Set	VT52 In Graphics Mode*
137		Blank	Blank
140	`	♦ Diamond	Reserved
141	a	▒ Checkerboard (error indicator)	Solid rectangle
142	b	␉ Horizontal tab	1/
143	c	␌ Form feed	3/
144	d	␍ Carriage return	5/
145	e	␊ Line feed	7/
146	f	° Degree symbol	Degrees
147	g	± Plus/minus	Plus or minus
150	h	␤ New line	Right arrow
151	i	␋ Vertical tab	Ellipsis (dots)
152	j	┘ Lower-right corner	Divide by
153	k	┐ Upper-right corner	Down arrow
154	l	┌ Upper-left corner	Bar at scan 0
155	m	└ Lower-left corner	Bar at scan 1
156	n	┼ Crossing lines	Bar at scan 2
157	o	⎺ Horizontal line – scan 1	Bar at scan 3
160	p	⎻ Horizontal line – scan 3	Bar at scan 4
161	q	─ Horizontal line – scan 5	Bar at scan 5
162	r	⎼ Horizontal line – scan 7	Bar at scan 6
163	s	⎽ Horizontal line – scan 9	Bar at scan 7
164	t	├ Left T	Subscript 0
165	u	┤ Right T	Subscript 1
166	v	┴ Bottom T	Subscript 2
167	w	┬ Top T	Subscript 3
170	x	│ Vertical bar	Subscript 4
171	y	≤ Less than or equal to	Subscript 5
172	z	≥ Greater than or equal to	Subscript 6
173	{	π Pi	Subscript 7
174	|	≠ Not equal to	Subscript 8
175	}	£ UK pound sign	Subscript 9
176	~	· Centered dot	Paragraph

*Not available in VT125

Direct Cursor Address

Format: ESC Y line column

Move the cursor to the specified line and column. The line and column numbers are sent as ASCII codes whose values are the number plus 037_8. For example, 040_8 refers to the first line or column, 050_8 refers to the eighth line or column, etc.

Identify

Format: ESC Z

Causes the terminal to send its identifier escape sequence to the host. The sequence is: ESC / Z.

NOTE
Information regarding options must be obtained in ANSI mode, using the device attributes (DA) control sequence.

Enter Alternate Keypad Mode

Format: ESC =

Auxiliary keypad keys send unique identifiable escape sequences for use by applications programs.

Exit Alternate Keypad Mode

Format: ESC >

Auxiliary keypad keys send ASCII codes for functions or characters on the key.

Enter ANSI Mode

Format: ESC <

All subsequent escape sequences will be interpreted according to ANSI Standards X3.64-1977 and X3.41-1974. The VT52 escape sequence in this section will not be recognized.

VT125 PROGRAMMING SEQUENCES

This section repeats the information on the *VT125 Programming Reference Card* (EK-VT125-RC).

CONTROL CHARACTERS RECEIVED

Name	Character Mnemonic	Octal Code	Function
Null	NUL	000	Ignored when received and used as a fill character.
Enquire	ENQ	005	Transmits the answerback message.
Bell	BEL	007	Generates a bell tone.
Backspace	BS	010	Moves the cursor to the left one character position.
Horizontal Tab	HT	011	Moves the cursor to the next tab stop.
Line Feed	LF	012	Causes a line feed or a new line operation. (Refer to Linefeed/ New Line mode.)
Vertical Tab	VT	013	Processed as LF.
Form Feed	FF	014	Processed as LF.
Carriage Return	CR	015	Moves the cursor to left margin on the current line.
Shift Out	SO	016	Selects the G1 character set, as designated by a Select Character Set sequence.
Shift In	SI	017	Selects the G0 character set, as designated by a Select Character Set sequence.
Device Control 1	DC1	021	Processed as XON. Causes the terminal to continue transmitting characters.

Name	Character Mnemonic	Octal Code	Function
Device Control 3	DC3	023	Processed as XOFF. Causes terminal to stop transmitting all characters except XOFF and XON.
Cancel	CAN	030	If received during an escape or control sequence, the sequence is cancelled and substitution character (▒) is displayed.
Substitute	SUB	032	Processed as CAN.
Escape	ESC	033	Processed as a sequence introducer.
Delete	DEL	177	Ignored when received.

ANSI COMPATIBLE SEQUENCES

Set Mode

Name	Mnemonic	Mode	Sequence
Line feed/new line	LMN	New line	ESC [20 h
Cursor key	DECCKM	Application	ESC [? 1 h
ANSI/VT52	DECANM	ANSI	N/A
Column	DECCOLM	132 column	ESC [? 3 h
Scrolling	DECSCLM	Smooth	ESC [? 4 h
Screen	DECSCNM	Reverse	ESC [? 5 h
Origin	DECOM	Relative	ESC [? 6 h
Auto wrap	DECAWM	On	ESC [? 7 h
Auto repeat	DECARM	On	ESC [? 8 h

Reset Mode

Name	Mnemonic	Mode	Sequence*
Line feed/new line	LMN	Line feed	ESC [20 l
Cursor key	DECCKM	Cursor	ESC [? 1 l
ANSI/VT52	DECANM	VT52	ESC [? 2 l
Column	DECCOLM	80 column	ESC [? 3 l
Scrolling	DECSCLM	Jump	ESC [? 4 l
Screen	DECSCNM	Normal	ESC [? 5 l
Origin	DECOM	Absolute	ESC [? 6 l
Auto wrap	DECAWM	Off	ESC [? 7 l
Auto repeat	DECARM	Off	ESC [? 8 l

* The last character of each sequence is lowercase L (154_8)

Cursor Key Codes Generated

	ANSI Codes		VT52 Codes
Cursor Key (Arrow)	**Reset (Cursor)**	**Set (Application)**	
Up	ESC [A	ESC O A	ESC A
Down	ESC [B	ESC O B	ESC B
Right	ESC [C	ESC O C	ESC C
Left	ESC [D	ESC O D	ESC D

Keypad Character Selection

Name	Mnemonic	Sequence
Alternate	DECKPAM	ESC =
Numeric	DECKPNM	ESC >

Keypad Codes Generated

	ANSI Mode		VT52 Mode	
Key	**Numeric Keypad Mode**	**Alternate Keypad Mode**	**Numeric Keypad Mode**	**Alternate Keypad Mode**
0	0	ESC O p	0	ESC ? p
1	1	ESC O q	1	ESC ? q
2	2	ESC O r	2	ESC ? r
3	3	ESC O s	3	ESC ? s
4	4	ESC O t	4	ESC ? t
5	5	ESC O u	5	ESC ? u
6	6	ESC O v	6	ESC ? v
7	7	ESC O w	7	ESC ? w
8	8	ESC O x	8	ESC ? x
9	9	ESC O y	9	ESC ? y
– (minus)	– (minus)	ESC O m	– (minus)†	ESC ? m†
, (comma)	, (comma)	ESC O l*	, (comma)†	ESC ? l*†
. (period)	. (period)	ESC O n	. (period)	ESC ? n
ENTER‡	CR or CRLF	ESC O M	CR or CRLF	ESC ? M
PF1	ESC O P	ESC O P	ESC P	ESC ? P
PF2	ESC O Q	ESC O Q	ESC Q	ESC ? Q
PF3	ESC O R	ESC O R	ESC R	ESC ? R
PF4	ESC O S	ESC O S	ESC S†	ESC ? S†

* The last character of the sequence is lowercase L (154_8)

† These sequences were not available in the VT52. Do not use the PF4, "–" (minus), or "," (comma) keys with VT52 software.

‡ Line feed/new line off causes ENTER to generate CR (015_8). On causes ENTER to generate CRLF (015_8 012_8).

Select Character Sets SCS

Character Set	G0 Designator	G1 Designator
United Kingdom (UK)	ESC (A	ESC) A
United States (USASCII)	ESC (B	ESC) B
Special characters and line drawing set	ESC (0	ESC) 0
Alternate character ROM	ESC (1	ESC) 1
Alternate character ROM – special characters	ESC (2	ESC) 2

Name	Mnemonic	Sequence
Single Shift 2 Single character shift to G2 (ASCII)	SS2	ESC N
Single Shift 3 Single character shift to G3 (ASCII)	SS3	ESC O

NOTE: The VT125 generates the following control characters differently from previous DIGITAL terminals.

Code	VT125 Keys	Previous Terminal Keys
NUL	CTRL – Space bar	CTRL – @
RS	CTRL – ~	CTRL – ^
US	CTRL – ?	CTRL – _

Character Attributes

Name	Mnemonic	Sequence
Select Graphic Rendition	SGR	–
No attributes	–	ESC [m
No attributes	–	ESC [0 m
Select bold attribute	–	ESC [1 m
Select underline attribute	–	ESC [4 m
Select blink attribute	–	ESC [5 m
Select reverse video attribute	–	ESC [7 m

NOTE: Without advance video option (AVO), only underline or reverse attribute is available.

US/UK Character Set

B7 B6 B5 / BITS B4 B3 B2 B1	ROW	COLUMN 0		COLUMN 1		COLUMN 2		COLUMN 3		COLUMN 4		COLUMN 5		COLUMN 6		COLUMN 7	
0 0 0 0	0	NUL	0 0 0		20 16 10	SP	40 32 20	0	60 48 30	@	100 64 40	P	120 80 50	`	140 96 60	p	160 112 70
0 0 0 1	1		1 1 1	DC1 (XON)	21 17 11	!	41 33 21	1	61 49 31	A	101 65 41	Q	121 81 51	a	141 97 61	q	161 113 71
0 0 1 0	2		2 2 2		22 18 12	"	42 34 22	2	62 50 32	B	102 66 42	R	122 82 52	b	142 98 62	r	162 114 72
0 0 1 1	3		3 3 3	DC3 (XOFF)	23 19 13	* # / £	43 35 23	3	63 51 33	C	103 67 43	S	123 83 53	c	143 99 63	s	163 115 73
0 1 0 0	4		4 4 4		24 20 14	$	44 36 24	4	64 52 34	D	104 68 44	T	124 84 54	d	144 100 64	t	164 116 74
0 1 0 1	5	ENQ	5 5 5		25 21 15	%	45 37 25	5	65 53 35	E	105 69 45	U	125 85 55	e	145 101 65	u	165 117 75
0 1 1 0	6		6 6 6		26 22 16	&	46 38 26	6	66 54 36	F	106 70 46	V	126 86 56	f	146 102 66	v	166 118 76
0 1 1 1	7	BEL	7 7 7		27 23 17	'	47 39 27	7	67 55 37	G	107 71 47	W	127 87 57	g	147 103 67	w	167 119 77
1 0 0 0	8	BS	10 8 8	CAN	30 24 18	(	50 40 28	8	70 56 38	H	110 72 48	X	130 88 58	h	150 104 68	x	170 120 78
1 0 0 1	9	HT	11 9 9		31 25 19	)	51 41 29	9	71 57 39	I	111 73 49	Y	131 89 59	i	151 105 69	y	171 121 79
1 0 1 0	10	LF	12 10 A	SUB	32 26 1A	*	52 42 2A	:	72 58 3A	J	112 74 4A	Z	132 90 5A	j	152 106 6A	z	172 122 7A
1 0 1 1	11	VT	13 11 B	ESC	33 27 1B	+	53 43 2B	;	73 59 3B	K	113 75 4B	[	133 91 5B	k	153 107 6B	{	173 123 7B
1 1 0 0	12	FF	14 12 C		34 28 1C	,	54 44 2C	<	74 60 3C	L	114 76 4C	\	134 92 5C	l	154 108 6C	|	174 124 7C
1 1 0 1	13	CR	15 13 D		35 29 1D	-	55 45 2D	=	75 61 3D	M	115 77 4D	]	135 93 5D	m	155 109 6D	}	175 125 7D
1 1 1 0	14	SO	16 14 E		36 30 1E	.	56 46 2E	>	76 62 3E	N	116 78 4E	^	136 94 5E	n	156 110 6E	~	176 126 7E
1 1 1 1	15	SI	17 15 F		37 31 1F	/	57 47 2F	?	77 63 3F	O	117 79 4F	_	137 95 5F	o	157 111 6F	DEL	177 127 7F

*NOTE DEPENDS ON THE CHARACTER SET SELECTED U.S.=# U.K.=£

KEY

ASCII CHARACTER: ESC — 33 OCTAL / 27 DECIMAL / 1B HEX

Special Characters and Line Drawing Set

BITS b4 b3 b2 b1	ROW	COLUMN 0	1	2	3	4	5	6	7
0 0 0 0	0	NUL	SP	0	@	P	`	p	SCAN 3
0 0 0 1	1		DC1 (XON)	!	1	A	Q	a	q	SCAN 5
0 0 1 0	2			"	2	B	R	b	r	SCAN 7
0 0 1 1	3		DC3 (XOFF)	#	3	C	S	c	s	SCAN 9
0 1 0 0	4			$	4	D	T	d	t	
0 1 0 1	5	ENQ		%	5	E	U	e	u	
0 1 1 0	6			&	6	F	V	f	v	
0 1 1 1	7	BEL		'	7	G	W	g	w	
1 0 0 0	8	BS	CAN	(	8	H	X	h	x	
1 0 0 1	9	HT		)	9	I	Y	i	y	
1 0 1 0	10	LF	SUB	*	:	J	Z	j	z	
1 0 1 1	11	VT	ESC	+	;	K	[	k	{	
1 1 0 0	12	FF		,	<	L	\	l	|	
1 1 0 1	13	CR		-	=	M	]	m	}	
1 1 1 0	14	SO		.	>	N	^	n	~	
1 1 1 1	15	SI		/	?	O	(BLANK)	o	DEL	

KEY

ASCII CHARACTER: ESC | 33 OCTAL | 27 DECIMAL | 1B HEX

Scrolling Region

Name	Mnemonic	Sequence
Set top and bottom margins	DECSTBM	ESC [Pt ; Pb r

Cursor Movement Commands

Name	Mnemonic	Sequence
Cursor up	CUU	ESC [Pn A
Cursor down	CUD	ESC [Pn B
Cursor forward (right)	CUF	ESC [Pn C
Cursor backward (left)	CUB	ESC [Pn D
Cursor position	CUP	ESC [Pl ; Pc H
Cursor position (home)	CUP	ESC [H
Horizontal and vertical position	HVP	ESC [Pl ; Pc f
Horizontal and vertical position (home)	HVP	ESC [f
Index	IND	ESC D
Reverse index	RI	ESC M
Next line	NEL	ESC E
Save cursor (and attributes)	DECSC	ESC 7
Restore cursor (and attributes)	DECRC	ESC 8

Tab Stops

Name	Mnemonic	Sequence
Horizontal tab set (at current column)	HTS	ESC H
Tabulation clear (at current column)	TBC	ESC [g
Tabulation clear (at current column)	TBC	ESC [0 g
Tabulation clear (all tabs)	TBC	ESC [3 g

Line Attributes

Name	Mnemonic	Sequence
Double-height top half	DECDHL	ESC # 3
Double-height bottom half	DECDHL	ESC # 4
Single-width single-height	DECSWL	ESC # 5
Double-width single-height	DECDWL	ESC # 6

Erasing

Name	Mnemonic	Sequence
Erase in line	EL	–
Cursor to end of line	–	ESC [K
Cursor to end of line	–	ESC [0 K
Beginning of line to cursor	–	ESC [1 K
Entire line containing cursor	–	ESC [2 K
Erase in display	ED	–
Cursor to end of screen	–	ESC [J
Cursor to end of screen	–	ESC [0 J
Beginning of screen to cursor	–	ESC [1 J
Entire screen	–	ESC [2 J

Communication and Graphics Protocol Commands

Name	Mnemonic	Sequence
Device control string	DCS	–
Enter ReGIS at previous command level	–	ESC P p
Enter ReGIS at highest command level	–	ESC P 1 p
Enter ReGIS at previous command level with commands to screen	–	ESC P 2 p
Enter ReGIS at highest command level with commands to screen	–	ESC P 3 p
Enter DECwriter graphics	–	ESC P q
Enter VT105 emulator	–	ESC P t
String terminator	ST	–
Exit graphics	–	ESC \
Media copy	MC	–
Turn off computer to auxiliary port	–	ESC [4 i
Turn on computer to auxiliary port	–	ESC [5 i
Turn off computer to screen	–	ESC [6 i
Turn on computer to screen	–	ESC [7 i
Select auxiliary port for ReGIS hardcopy output	–	ESC [? 0 i
Select computer port for ReGIS hardcopy output	–	ESC [? 2 i

Reports

Name	Mnemonic	Sequence
Device status report (request status of VT125)	DSR	ESC [5 n
Response:		
Terminal OK	DSR	ESC [0 n
Terminal not OK	DSR	ESC [3 n
Device status report (request cursor position)	DSR	ESC [6 n
Cursor position report	CPR	ESC [Pl ; Pc R
Device attributes (what are you)	DA	ESC [c
Device attributes (what are you)	DA	ESC [0 c
Identify terminal (what are you)	DECID	ESC Z

NOTE: ESC Z *is not recommended.*

Device attributes response: VT125	DA	See Note.

NOTE: Format is ESC [? 12 ; <vt100> ; <vt125> ; <version> c

<vt100>	5 = no AVO, 7 = AVO
<vt125>	1 = printer, 0 = no printer
<version>	Graphics firmware

Reset

Name	Mnemonic	Sequence
Reset to initial state	RIS	ESC c

NOTE: Do not use VT100 loopback tests with the graphics processor installed. Loopback tests require test connector. Continuous tests end at failure or power-off.

Name	Mnemonic	Sequence
Screen alignment display	DECALN	–
Fill screen with "Es"	–	ESC # 8
Invoke confidence test	DECTST	–
Power-up test	–	ESC [2 ; 1 y
Data loopback test	–	ESC [2 ; 2 y
Power-up and data loopback tests	–	ESC [2 ; 3 y
EIA modem control loopback test	–	ESC [2 ; 4 y
Power-up and EIA loopback tests	–	ESC [2 ; 5 y
Data loopback and EIA loopback tests	–	ESC [2 ; 6 y
Power-up, data loopback, and EIA loopback tests	–	ESC [2 ; 7 y
Repeat power-up test continuously	–	ESC [2 ; 9 y
Repeat data loopback test continuously	–	ESC [2 ; 10 y
Repeat power-up and data loopback tests continuously	–	ESC [2 ; 11 y
Repeat EIA test continuously	–	ESC [2 ; 12 y
Repeat power-up and EIA tests continuously	–	ESC [2 ; 13 y
Repeat data loopback and EIA loopback tests continuously	–	ESC [2 ; 14 y
Repeat power-up, data loopback, and EIA loopback tests continuously	–	ESC [2 ; 15 y

VT125 Tests and Adjustments

NOTE: All tests require loopback connector. Always include power-up test for correct display of error indications.

Name	Mnemonic	Sequence
Invoke confidence test	DECTST	ESC [4 ; 1 ; Ps . . . ; Ps y
VT125 power-up test	–	Ps = 1
VT125 computer port data loopback test	–	Ps = 2
VT125 auxiliary port data loopback test	–	Ps = 3
VT125 display test	–	Ps = 4
VT125 video bit map memory test	–	Ps = 5
Repeat any selected tests continuously until power-off or failure	–	Ps = 9

Keyboard Indicators

Name	Mnemonic	Sequence
Load LEDs	DECLL	–
All off	–	ESC [q
L1 on	–	ESC [1 q
L2 on	–	ESC [2 q
L3 on	–	ESC [3 q
L4 on	–	ESC [4 q

VT52 COMPATIBLE MODE

Mode	Sequence
Enter ANSI mode	ESC <

Keypad Character Selection

Name	Sequence
Enter alternate keypad mode	ESC =
Exit alternate keypad mode (numeric keypad mode)	ESC >

NOTE: VT52 alternate keypad and numeric keypad modes are different from ANSI.

Character Sets

Name	Sequence
Special graphics character set	ESC F*
Select US/UK character set (as determined by the US/UK character SET-UP feature)	ESC G

* Same as special character and line drawing set in ANSI mode.

Cursor Position

Name	Sequence
Cursor up*	ESC A
Cursor down*	ESC B
Cursor right*	ESC C
Cursor left*	ESC D
Cursor to home	ESC H
Direct cursor address	ESC Y Pl Pc†
Reverse line feed	ESC I‡

* Same when sent from the terminal.

† Line and column numbers for direct cursor address are single character codes whose values are the desired number plus 31_{10}. Line and column numbers start at one.

‡ The last character of the sequence is an uppercase i (111_8).

Erasing

Name	Sequence
Erase to end of line	ESC K
Erase to end of screen	ESC J

Reports

Name	Sequence
Identify (what are you)	ESC Z
Response: VT52	ESC / Z

ReGIS COMMAND SUMMARY

Position Command Summary

Command	Function
P [ ]	Reset pattern memory.
[<position>]	Move to <position>.
<pixel vector> or <pv>	Move <multiplier> pixels in <pv> direction.
(B)	Save current location.
(S)	Save dummy location.
(E)	Move to last saved location.
(W (<temp. writing controls>))	P (W (M<multiplier>)).

Vector Command Summary

Command	Function
V [ ]	Draw dot at current position.
[<position>]	Draw vector to <position>.
<pixel vector> or <pv>	Draw <multiplier> pixels in <pv> direction.
(B)	Save current position.
(S)	Save dummy position.
(E)	Draw to last saved position.
(W (<temp. writing controls>))	

Curve Command Summary

Command	Function
C [<position>]	Circle with center at current position, circumference at <position>.
(C)[<position>]	Circle with center at <position>, circumference at current position.
(A<degrees>) [<position>]	Arc with center at current position, starting at <position> for <degrees>.
(A<degrees>C) [<position>]	Arc with center at <position>, starting at current position for <degrees>.
(B) [<pos.>] . . . [<pos.>] (E)	Bounded (closed) curve
(S) [ ] [<pos.>]. . . [<pos.>] [ ] (E)	Unbounded (open) curve
(W(<temp. writing controls>))	

Text Command Summary

Command

T (S <size number>)
(H <height>)
[<spacing>]
(S [<width in pixels>,<height in pixels>])
(M [<width pixel multiplier>,<height pixel multiplier>])
(D <direction angle>)
(D <string tilt> S <size> D <char tilt>)
(T <italic degrees>)
(A <pattern set number>)
((B) <temporary attributes block> (E))
(W(<temp. writing controls>))

Writing Controls Summary

Command				Function		
W (C)				Complement		
(E)				Erase		
(R)				Replace		
(V)				Overlay		
(F <foreground planes>)				0 = no planes 1 = plane 1 2 = plane 2 3 = planes 1 and 2		
				Foreground intensity:		
(I	0	or	(D))	Dark	or	Dark
	1		(R))	Dim grey		Red
	2		(G))	Light grey		Green
	3		(B))	White		Blue
			(C))			Cyan
			(Y))			Yellow
			(M))			Magenta
			(W))			White
or						
(I (H <hue angle> L <lightness percent> S <saturation percent>))						
(M <multiplier>)				Pixels per <pv>		
(N 1)				Negative on		
(N 0)				Negative off		
(S 1)				Shading on		
(S 0)				Shading off		
(S [,shading reference])						
(S 'shading character')						
(P <binary pattern>)				Enter pattern.		
(P <pattern number>)				Use VT125 pattern.		
(P (M <pattern multiplier>))						
(W<i>(P<j>,N<k>))				Custom writing control		

Screen Controls Summary

Command	Function
S <pixel vector> [<position>]	Scroll.
(A [<position>] [<position>])	Display addressing.
(E)	Erase screen.
(H [<position>] [<position>]	Hardcopy (corner positions optional)
(H(P[<position>]))	Set hardcopy offset.

(I	0	or	(D)	)	Background intensity: Dark	or	Dark
	1		(R)	)	Dim grey		Red
	2		(G)	)	Light grey		Green
	3		(B)	)	White		Blue
			(C)	)			Cyan
			(Y)	)			Yellow
			(M)	)			Magenta
			(W)	)			White

or
(I (H <hue angle>
L <lightness percent>
S <saturation percent>))

S(M<n>(<mono HLS>)(A<color HLS>)) Output mapping

(S <scale>)
(S (X<scale> Y<scale>)
(T <ticks>) Time delay

Macrograph

Command	Function
@	Clear all macrographs.
:keyletter character_string @;	Define macrograph.
keyletter	Invoke macrograph.

Character Cell Control Summary

Command	Summary
L (A<integer>)	Select for loading.
(A"<name>")	Give name to set.
"<ASCII char>" <hex pair> . . . <hex pair>;	Load cell.

Report Command Summary

Command	Function
R (L)	Set selected for loading.
(M (<keyletter>))	Contents of macrograph.
(M (=))	Use of storage.
"<free>,<total>"	Reply to use.
(P)	Cursor position.

APPENDIX B
RECOMMENDED SPARES LIST (RSL)

Table B-1 lists the recommended spares for the basic VT100 and all variations.

Table B-1 VT100 Recommended Spares

Qty	Part Number/Description	VT100	VT100WA\B	VT100WC\K	VT1XX\AC	VT105	VT125	VT132
1	30-14590-02 Monitor PCB (Ball)	x	x	–	–	–	–	–
1	30-14590-01 Flyback transformer (Ball)	x	x	–	–	–	–	–
1	70-17362-00 Monitor PCB (Elston)	x	x	x	–	x	x	x
1	70-17363-00 Flyback assembly (Elston)	x	x	x	–	x	x	x
1	70-17364-00 CRT and yoke assembly	x	x	x	–	x	x	x
1	54-13009-00 Terminal controller PCB (not FCC-complying)	x	x	x	–	x	x	x
1	54-13009-03 Terminal controller PCB (FCC-complying)	x	x	x	–	x	x	x
1	54-13097-00 Advanced video PCB	x	x	x	–	x	x	x
1	70-15273 20 mA adapter assembly	x	x	x	–	x	x	x
1	70-15506-0B 20 mA internal cable	x	x	x	–	x	x	x
1	BC05F-15 20 mA cable (15 ft)	x	x	x	–	x	x	x
1	BC05D-10 EIA cable (M-F) (10 ft)	x	x	x	–	x	x	x
1	BC03M-10 EIA cable (null modem)	x	x	x	–	x	x	x
1	70-15765-00 LK keyboard	x	–	–	–	x	x	x
1	70-14652 Cable assembly, keyboard	x	x	x	–	x	x	x
1	12-15050 Speaker	x	x	x	–	x	x	x
1	12-14333-72 LK07 keycap set	x	x	x	–	x	x	x
1	12-14333-91 LK08 keycap set	x	x	x	–	x	x	x
1	74-16355 Keycap removal tool	x	x	x	–	x	x	x
1	70-14979 Power supply assembly	x	x	x	–	x	x	x
1	12-15232 Power switch	x	x	x	–	x	x	x
1	12-16901-00 Voltage select switch	x	x	x	–	x	x	x

Table B-1 VT100 Recommended Spares (Cont)

Qty	Part Number/Description	VT100	VT100WA\B	VT100WC\K	VT1XX\AC	VT105	VT125	VT132
10	90-07217 Fuse 3 Amp	x	x	x	–	x	x	x
1	17-0083-09 Line cord, 115 V	x	x	x	–	x	x	x
1	17-0083-10 Line cord, 230 V	x	x	x	–	x	x	x
1	70-14978-01 DC power dist. cable	x	x	x	–	x	–	x
1	70-14978-03 DC power dist. cable	x	x	x	–	x	x	x
2	12-12405-00 Card guide	x	x	x	–	x	x	x
5	90-10007 Retainer ring*	x	x	x	–	x	x	x
5	90-09747-01 Support*, chassis	x	x	x	–	x	x	x
5	90-10016-00 Cable clamp*	x	x	x	–	x	x	x
15	90-09964 Plunger*, chassis mounting	x	x	x	–	x	x	x
15	90-09966-01 Grommet*, chassis	x	x	x	–	x	x	x
5	12-14811 Captive screw*	x	x	x	–	x	x	x
15	12-14740-00 Plunger*, base mounting	x	x	x	–	x	x	x
15	90-09965-00 Plunger*, base mounting	x	x	x	–	x	x	x
5	90-09747-03 Standoff*, AVO	x	x	x	–	x	x	x
15	90-09966-02 Grommet*, base	x	x	x	–	x	x	x
5	12-14817 Mounting screw*	x	x	x	–	x	x	x
5	90-09624-00 Feet*	x	x	x	–	x	x	x
1	12-12893 Fuse holder*	x	x	x	–	x	x	x
5	90-09680-04 Screw*, tap 6 × 1/2 hex	x	x	x	–	x	x	x
5	90-09701-00 Screw*, 6-32 × 5/16	x	x	x	–	x	x	x
1	94-03220-03 CRT mask, alignment	x	x	x	–	x	x	x
1	94-03270-03 CRT mask, char. alignment	x	x	x	–	x	x	x
1	29-23189-00 Shaft extender	x	x	x	–	x	x	x
1	29-23190-00 Alignment tool, monitor	x	x	x	–	x	x	x
1	29-23187 Kit, carrying case	x	x	x	–	x	x	x
1	99-05812 IC container	x	x	x	x	x	x	x
1	12-15336 Loopback connector, RS232C	x	x	x	x	x	x	x
1	70-15503-00 Loopback connector, 20 mA	x	x	x	–	x	x	x
1	70-15765† Word processor keyboard	–	x	x	–	–	–	–
1	54-14260-00 STP board	–	–	–	x	–	–	–
1	M7071 Waveform generator module	–	–	–	–	x	–	–
1	70-08612-0F Cable	–	–	–	–	x	–	–
1	54-14277 Mono graphics board	–	–	–	–	–	x	–
1	54-14275 STP paddle board	–	–	–	–	–	x	–
1	70-16165-1E 24-pin flat cable	–	–	–	–	–	x	–
1	70-18396-YA 16-pin flat cable	–	–	–	–	–	x	–
1	12-14333-U3 Keycap, DELETE	–	–	–	–	–	–	x
1	12-14333-U4 Keycap, INSERT LINE/PF1	–	–	–	–	–	–	x
1	12-14333-U5 Keycap, DELETE LINE/PF2	–	–	–	–	–	–	x
1	12-14333-U6 Keycap, CHAR INSERT/PF3	–	–	–	–	–	–	x

Table B-1 VT100 Recommended Spares (Cont)

Qty	Part Number/Description	VT100	VT100WA\B	VT100WC\K	VT1XX\AC	VT105	VT125	VT132
1	12-14333-WK Keycap, CLEAR/HOME	–	–	–	–	–	–	x
1	12-14333-U8 Keycap, BACK TAB/,	–	–	–	–	–	–	x
1	12-14333-U9 Keycap, DELETE CHAR/.	–	–	–	–	–	–	x
1	12-14333-W0 Keycap, PRINT/ENTER	–	–	–	–	–	–	x
1	12-14333-W1 Keycap, (EDIT)/PF4	–	–	–	–	–	–	x
1	12-14333-U0 Keycap, PRINT/ENTER	–	–	–	x	–	–	–
1	23-061E2-00 ROM, basic video	x	x	–	–	x	x	–
1	23-032E2-00 ROM, basic video	x	x	–	–	x	x	–
1	23-033E2-00 ROM, basic video	x	x	–	–	x	x	–
1	23-034E2-00 ROM, basic video	x	x	–	–	x	x	–
1	23-069E2-00 ROM, AVO	–	x	–	–	–	–	–
1	23-180E2 ROM, basic video	–	–	–	–	–	–	x
1	23-181E2 ROM, basic video	–	–	–	–	–	–	x
1	23-182E2 ROM, basic video	–	–	–	–	–	–	x
1	23-183E2 ROM, basic video	–	–	–	–	–	–	x
1	23-236E2 ROM, advanced video	–	–	–	–	–	–	x
1	23-237E2 ROM, advanced video	–	–	–	–	–	–	x
1	23-238E2 ROM, advanced video	–	–	–	–	–	–	x
1	23-239E2 ROM, advanced video	–	–	–	–	–	–	x
1	23-095E2 ROM, basic video	–	–	x	–	–	–	–
1	23-096E2 ROM, basic video	–	–	x	–	–	–	–
1	23-139E2 ROM, basic video	–	–	x	–	–	–	–
1	23-140E2 ROM, basic video	–	–	x	–	–	–	–
1	23-186E2 ROM, advanced video	–	–	–	x	–	–	–
1	23-187E2 ROM, advanced video	–	–	–	x	–	–	–
1	23-152E2 ROM, advanced video	–	–	x	–	–	–	–
1	23-094E2 ROM, character generator (E9)	–	–	x	–	–	–	–
2	90-09306-00 Fiber spacer*	–	–	–	x	–	x	–
10	90-09185-00 Jumpers*	–	–	–	–	–	–	–

*These items are expendable.

†Use the following chart to determine the correct last two digits of the part number.

Terminal	Language	Part Number
VT100WA/WB	Word Processing	70-15765-03
VT100WC/WD	French Canadian	70-15765-05
VT100WE/WF	French	70-15765-06
VT100WG/WH	Dutch	70-15765-07
VT100WJ/WK	German	70-15765-08

APPENDIX C
GLOSSARY OF TERMS AND ABBREVIATIONS

20 mA – Value of current used for current loop communications option; also, the name of the option.

75 ohm – Source and terminating impedance for video inputs and outputs.

7FH – Hexadecimal value representing 0111 1111 in binary; the terminator at the end of each line of characters; also, the last keyboard address, always returned at the end of a scan.

8080 – The microprocessor device.

8224 – The clock generator device.

8228 – The system controller and bus driver device.

8251 – The PUSART.

A0,A1,...,Ax – Address bus.

Active – For the current loop option, the interface supplies switched current to transmit, and to receive, detects changes as the remote sender switches the current supplied by the active device. For the STP, the STP device intercepts the interface signals, acts on them, and then can either withhold them or pass them on to the terminal controller or the host.

Active Position – The active column and active line position in which the next displayable character will be placed. The active line is the line in which the cursor is presently located. The active column is the cursor location on the active line.

ADDR – Address

ADDR CNT – Address count. Signal that drives the address counters in the video processor.

ADDR CNT ON – Address count on. Signal inside the DC011 that controls the output of Address Count signals.

ADDR LD – Address load. Signal that loads the address bytes from the end of a line into the pre-settable address counters; also stores line attributes.

Advanced video option – Optional circuit board that contains extra screen RAM, extra attribute RAM, and program ROM sockets and decoders.

ALT CHAR SET – Alternate character set. If the AVO is present, a ROM with a different character set can be installed in a socket on the terminal controller, and selected with a control function.

ANSI – American National Standards Institute

ANSI mode – A mode in which the terminal recognizes and responds only to control functions whose syntax and meaning follow ANSI specifications.

ASCII – American Standards Committee for Information Interchange

Asynchronous – For serial data transmission; method allows sender and receiver to operate with non-identical clocks.

Attribute – A display feature such as blinking characters, double width lines, or reverse screen.

AVO – Advanced Video Option

Base attribute – The one attribute that characters on the screen can have when the AVO is not present. Selectable at SET-UP to be either reverse or underline.

Baud rate – Rate of data exchange on a serial interface.

Bipolar – A kind of transistor construction used in TTL and high speed LSI.

Bit map – A large memory with as many addresses as the display has cartesian coordinates. There is a one-to-one correspondence between pixels on the screen and addresses in the memory.

Blink – An attribute that makes a character blink.

Bold – An attribute that makes a character brighter.

Bottom half – In a double height line, this is asserted for the bottom half of the line.

Bus – A group of wires carrying several separate but related signals.

Byte – Eight bits treated as a unit.

C/D – Command/Data. Control line to the PUSART.

Caps lock – A key that forces alphabetics to uppercase without affecting numeric and symbolic keys.

Cathode – The element that is driven to control intensity of the electron beam in the CRT.

CHAR CLK – Character Clock. A clock in the video processor with a period equal to the time between characters on the display. Varies according to 80 or 132 column mode.

Character – A pattern of dots on the CRT screen representing an ASCII character; a pattern which represents an element of written language or mathematics; a group of 7 or 8 bits representing a control or graphic entity. In serial-by-bit transmission, a character is transferred from low-order bit to high-order bit.

Character generator – A ROM that translates character codes into patterns for display.

Character position – That portion of a display that is displaying or is capable of displaying a graphic symbol.

Checksum – A number created specifically to detect errors in stored or exchanged data.

Column mode – The number of characters positions provided on a line – 80 or 132.

COMP SYNC – Composite Sync signal

Composite sync – The signal that coordinates the motion of the electron beam in a video monitor that is external to the VT100.

Control – The term "control" refers to a "control function." A control function is implemented through the use of a control character, escape sequence, control sequence, or control string.

Control (key) – Produces control characters when pressed with other keys.

Control chip – The DC012

Control character – A single character whose occurrence in a particular context initiates, modifies, or stops a control function. The value of a control character is in the range 0 through 1FH and 7FH in a 7-bit environment.

Control function – A special action the terminal can perform to affect recording, processing, transmitting, or interpreting data. Also, the sequence of characters that cause the action.

Control Q – An ASCII control character meaning XON.

Control S – An ASCII control character meaning XOFF.

Control sequence – A sequence of characters used for control purposes to perform a control function. A control sequence is a string of characters that begins with the control sequence introducer (CSI) and ends with the first occurrence of a final character (40H—7EH). A control sequence may contain 0 or more parameter characters (30H—3FH) and/or intermediate characters (20H–2FH).

Control sequence introducer – A prefix to a control sequence that provides supplementary control functions. The CSI for the VT100 series is ESC [(1BH 5BH).

Control string – A string of characters used to perform a control function and delimited by an opening and closing delimiter character.

CPU – Central processing unit. Generally means host.

CRT – Cathode ray tube. The display device in a monitor.

CSI – Control sequence introducer

Current loop – The 20 mA interface option.

Cursor – A blinking underline or blinking reverse field indicating the active position.

D0,D1,...,Dx – Individual lines on the data bus.

DB bus – The bidirectionally buffered data bus.

DC011 – Timing chip for the video processor. Produces timing signals, clocks, and line buffer addressing.

DC012 – Control chip for the video processor. Controls DMAs and generation of character video.

DCA – Direct cursor addressing

DEC – Prefix for DEC private control functions.

Default – Parameters provided when no choice is made by the user.

Demultiplexer – Routes a signal to one of several outputs according to control signals.

DH – Double height

Direct drive – Controls movement of electron beam in the CRT with separate horizontal and vertical signals rather than combining the control signals into the single composite video signal.

Direct memory access – An action by which the video processor can read data directly from the microprocessor's memory.

DMA – Direct memory access

DMA ENABLE – A signal allowing a DMA to occur.

DO bus – The buffered write-only (output-only) data bus.

Dot – The smallest displayable unit of information on the screen.

DOT CLK – The fastest clock in the video processor; clocks the video shift register. Varies with 80 or 132 column mode.

Dot stretcher – In the DC012, adds one dot to each row of contiguous dots. Ensures that bandwidth requirement of CRT is met.

Double height – Makes each line display in 20 scans instead of the regular 10.

Double width – Makes each character display in 20 dots instead of the regular 10.

DSR – Data Set Ready

DTR – Data Terminal Ready

DW – Double Width

E4 – Normal character set ROM

E9 – Alternate character set ROM

E11 – Line buffer D4–D7

E15 – Character latch buffer

E16 – Character generator latch

E17 – Line buffer D0–D3

E20 – Screen RAM character latch

E21 – Address counter A8–A11

E25 – Address counter A4–A7

E30 – Address counter A0–A3

E60 – Programmable baud rate generator

EAROM – Electrically alterable read-only memory – the NVR.

EIA – Electronic Industries Association; used to refer to the EIA standard voltage I/O interface, RS-232-C.

ER1400 – Nonvolatile RAM

ESC – Escape character (ASCII 1BH)

Escape character (ESC) – A control character that provides code extension and that is itself a prefix affecting the interpretation of a limited number of contiguous characters.

Escape sequence – A sequence of characters used for control purposes to perform a control function. The sequence begins with an (1BH) control character and ends with the first occurrence of a final character (30H–7EH). An escape sequence may have 0 or more intermediate characters (20H–2FH) preceding the final character.

Exclusive-OR – A logical function that provides an output only when one or the other input signal is present but not when both or neither are present.

EXT – External

Field – That part of a video image displayed during one vertical sweep of the CRT beam from the top of the screen to the bottom.

Fill line – A terminator and a pair of address bytes. Synchronizes the DMA process in the video processor without requiring a full line of memory.

Firmware – The microprocessor program.

Flag – An internal signal to the microprocessor.

Flyback transformer – Generates high voltages in the CRT monitor.

Frame – A complete video image.

Graphics – A kind of display showing lines and shapes rather than alphanumerics.

Halt – A condition in the microprocessor when no instructions are performed.

Hard copy – Computer output that can be carried away from the output device in human-readable form.

Hardware – The electrical and mechanical structure of a device.

HOLD REQ – Hold request. A signal asking the microprocessor to give up use of the address, data, and control buses to the video processor.

HORIZ BLANK – Horizontal blank. Signal that turns the electron beam off during the horizontal retrace interval.

HORIZ DRIVE – Horizontal drive. Direct drive signal from the video processor that synchronizes horizontal deflection in the internal monitor.

HORIZONTAL TIME – Gating signal inside the DC012.

Host – The computer that the VT100 communicates with.

Hysteresis – A characteristic of detection circuits that makes the threshold of detection different for different directions of change of the input signal.

IC – Integrated circuit.

Idle – On a communication line, a state when no information is being exchanged.

INIT – Initialize. Signal that informs options and internal devices that the VT100 has performed a reset operation.

INTA – Interrupt acknowledge. Signal the 8080 produces to indicate it is ready for a RST instruction containing an interrupt vector. The signal enables the outputs on the interrupt vector buffer.

Interlace – A kind of video display where the information from two fields is displayed by offsetting the vertical position of one field slightly from the other so the scans of one field appear between the scans of the other.

Interrupt – A signal to the microprocessor to get it to set aside its current work to take care of a high priority task. Such tasks include getting data from a communication line before it disappears.

I/O RD – Input/output read. A microprocessor control bus signal.

I/O WR – Input/output write. A microprocessor control bus signal.

I/O – Input/output. A general word that refers to data transfers between the microprocessor and devices under microprocessor control, like sensors and indicators.

ISO – International Standards Organization

Jump – In firmware, a movement to a nonsequential instruction. In a display, a form of scrolling where lines of characters on the screen move up or down by the height of a character line in one operation (compare to smooth scrolling).

KEY DOWN – Signal in the keyboard that causes the transmission of a key address to the terminal.

Keypad – Generally refers to the cluster of 18 numeric and special function keys on the right side of the keyboard.

Latch – A device that can store data.

LATOFS – Line address offset table. Used by the firmware to determine the display order of the lines.

LBA – Line buffer address. Output from the DC011 to address character location in the video processor's line memory.

LC – Inductor-capacitor

LED – Light emitting diode. A light source (usually red). There are seven at the top of the keyboard.

Line – A line of either 80 or 132 characters. Characters do not have to be present for the line to exist in memory.

Line attribute – An attribute that affects the entire line, such as double width.

Line buffer – Memory that stores the current line for display during the nine non-DMA scans.

Local – A condition in which the output from the keyboard goes directly to the screen without going to the host.

LSI – Large scale integration. Very complex circuitry packed into small packages. The DC011, DC012, and 8080 are examples.

Mark – One state of a communication line. Generally defined as a low signal level or the presence of current flow. See also Space.

Mask-programmed – Programmed as part of the manufacturing process and not changeable.

Matrix – An arrangement that allows addressing of many individual points with few address lines. Used in the keyboard switch array.

MEM DISABLE – Memory disable. Signal used by the AVO to disable main memory outputs when other memory is being addressed.

MEM RD – Memory read. A microprocessor control bus signal.

MEM WR – Memory write. A microprocessor control bus signal.

Microprocessor – The 8080 and associated devices. Controls VT100 operation.

MNOS – Metal nitride oxide semiconductor. The semiconductor technology used in the nonvolatile RAM.

Mode instruction – Command to the PUSART that sets up the basic operating protocol.

Modem – A device that converts the VT100's EIA output to audio tones that can pass over telephone lines.

Modulus – The largest unique value in a counter. If incremented beyond its modulus, a counter returns to 0 and counts up again.

MOS – Metal oxide semiconductor. A class of devices distinct from bipolar.

ms – Millisecond

Multiplexer – A device that selects from several inputs to give one output.

MUX – Multiplexer

New scroll zone – A signal inside the DC012 that indicates the beginning of a scroll zone and commands a new DMA.

NMOS – N-channel metal oxide semiconductor. Class of device used in the 8080 and 8251 and 2114 (memory chip).

NO SCROLL – A key that stops new data from entering the screen.

Nonvolatile RAM – Writable memory that does not lose its data when power is off.

NTSC – National Television Standards Committee

NVR – Nonvolatile RAM

Offset – The number of scans a line is moved from the normal display position in a given frame during a smooth scroll. Also, the rearrangement of line display order according to LATOFS.

On line – A condition in which all keyboard information passes to the host computer and the screen receives its data from the host.

Overrun error – Occurs in the PUSART if the microprocessor did not read a character before the next one arrived on top of it.

Parallel – Data path where all bits travel simultaneously on separate wires.

Parity – An error detection system based on the number of bits set in each data byte.

Parity error – An error condition indicating that at least one of the bits in a byte changed.

Parser – A process that separates a sequence into its component parts.

Passive – For the current loop option, the interface accepts current from outside and passes it or blocks it to transmit; to receive, it detects changes in the incoming current. For the STP, the option plugged into the STP examines the data on the interface and can add messages of its own, but cannot change the data passing between the terminal controller and the host.

Pn – Parameter

Pop – The microprocessor retrieves data from the stack.

Port – A place where data can enter or exit a device.

Pulse width modulation – Encoding of data by varying the duty cycle of a continuous clock.

PUSART – Programmable universal synchronous/asynchronous receiver/transmitter. The communication device in the VT100.

Push – The microprocessor puts data in the stack.

PWM – Pulse width modulation

RAM – Random access memory (also known as read/write memory).

Raster – On a CRT screen, the effect of continuous vertical and horizontal deflections of the electron beam covering the full height and width of the screen. If the beam is turned off, the raster is not visible.

RC – Resistor-capacitor

RCLK – Receive clock

Ready – A control line that forces a wait state in the 8080. Not used in the VT100.

Recall – A routine that sets SET-UP data from the NVR.

Refresh – The process of repeatedly rewriting the screen with data so it appears to to be constantly lit.

Reset – Setting a device to a starting condition, often for clearing errors.

Restart – Instruction the 8080 performs when interrupted.

Retrace – Rapid movement of the turned-off CRT beam from the end of one pass to the beginning of another.

Reverse video – A character attribute: characters are seen as dark areas in fields of light.

Reverse screen – A screen attribute: the entire screen is normally rendered as black characters on a white background.

RO – Receive-only

Rollover – Ability to accept more than one key pressed at the same time.

ROM – Read only memory

Routine – Set of instructions to the microprocessor that makes it perform a particular function.

RS-170 – An EIA standard that dictates television signal characteristics.

RS-232-C – An EIA standard that dictates data interface characteristics.

RSL – Recommended spares list

RST – Restart instruction

RTS – Request to send – modem control signal.

RxD – Receive data – PUSART

RxRDY – Receiver ready – PUSART

Save – Process of storing SET-UP data in the NVR.

Scan – One horizontal pass of the CRT beam; also, the character information displayed in that pass.

Scan count – The video processor keeps count to help decide when to initiate a DMA and to provide addresses for the character generator ROM.

SCD – Secondary carrier detect. A modem control signal.

Schmidt trigger – A device that accepts a slowly varying signal to an input with hysteresis in its threshold of detection. It outputs clean transitions when the input passes the threshold of detection in either direction.

Scratch RAM – That portion of RAM used for microprocessor operations.

Screen – Face of CRT on which data are displayed.

Screen attribute – Applies to the entire display area: reverse screen, smooth scrolling.

Screen RAM – That portion of RAM used for display storage.

Scroll – Upward or downward movement of data on the screen.

SEL 8–12K – Select memory in the range 2000H to 2FFFH.

SEL ATT RAM – Select attribute RAM. Signal for reading and writing data in the attribute RAM on the AVO under microprocessor control.

Serial – Transmission of data bit-by-bit over a single data line.

SET-UP – Special mode of terminal operation for entering operating parameters from the keyboard.

SET-UP specifications – Those terminal operating parameters entered from the keyboard or changeable from the host.

SHUFAD – Shuffle address. The pointer address location that changes during a shuffle.

SHUFDT – Shuffle data. The pointer address stored in SHUFAD during a shuffle.

Shuffle – The process of quickly rearranging pointer addresses when a line scrolls off or on the screen.

SILIN – The address where the next character enters the SILO.

SILO – A Scratch RAM area where data coming from the communication port is buffered on a first-in/first-out basis.

SILOUT – The address where the next character exits the SILO.

Smooth scroll – Scrolling in which the data on the screen moves only one scan per frame.

Soft copy – Computer output that only exists as light on a screen.

Space – One state of a communication line. Generally defined as a high signal level or the absence of current. (See also Mark.)

SPDI – Speed indicator. A modem control signal.

SPDS – Speed select. A modem control signal.

Split screen – Display operation where one part of the screen can scroll while another part remains stationary.

SR – Shift register. The device that performs parallel to serial conversion of data from the character generator ROM to the CRT. Also, the parallel-to-serial (or s-to-p converter) in UARTs and PUSARTs.

SRTS – Secondary request to send. A modem control signal.

Stack – Area of scratch RAM where the microprocessor places its current status while processing an interrupt or subroutine call.

Start bit – The first bit in a serial, asynchronous byte transmission, always a space.

Status byte – A byte of information about the operation of the 8080 that it outputs during the first machine cycle of an instruction. The byte is latched and decoded into control signals by the 8228 system controller.

Stop bit – The last bit in a serial, asynchronous byte transmission, always a mark.

STP – Standard terminal port

Strobe – A signal (usually brief) that commands a device to perform a function.

STSTB – Status strobe. Signal output by the 8080 to latch the status byte into the 8228.

Sync – Any signal that allows one device to operate precisely in step with another. Particularly applies to synchronization of the electron beam in a monitor to the video data that modulates the beam.

Synchronous – Processes that occur in synchronism.

TBMT – Transmit buffer empty. A signal from the keyboard UART.

TC – Terminal controller. The main VT100 circuit board.

TCLK – Transmit clock

Terminator – A character mixed in with screen data that signals the end of a line and causes the video processor to advance to the next line.

Threshold of detection – That value of input that causes a detector's output to change state.

Timing chip – The DC011

Toggle – To alternate the state of a device between two values.

Top half – In a double height line, this is asserted for the top half of the line.

TP – Terminal processor. A hypothetical nonvideo processor built into the VT100 cabinet.

Tristate – A device output that can sink current, source current, or become high impedance and not affect the circuits connected to it.

Tx ENable – Transmitter enable. A bit in the PUSART command instruction.

TxD – Transmitter data. PUSART serial data output.

TxEmpty – Transmitter empty. PUSART control output.

TxRDY – Transmitter ready. PUSART control output.

UART – Universal asynchronous receiver-transmitter. Wire-programmed device used in the keyboard interface.

Underline – A character attribute that forces scan 9 to show during a character.

μs – Microsecond

Vector – The address of the first instruction for an interrupt handling routine.

VERT BLANK – Vertical blank. Signal that turns off the CRT beam during the vertical interval.

VERT DRIVE – Vertical drive. Direct drive signal from the video processor that synchronizes vertical deflection in the monitor.

VERT RESET – Signal that occurs at the bottom of the screen to start the video processor at the top.

Vertical interval – The portion of a raster when the beam is turned off and returning to the top of the screen.

VID WR 1 – Video Write 1. Signal to load control data into the DC011.

VID WR 2 – Video Write 2. Signal to load control data into the DC012.

Video processor – The circuitry that converts character codes stored in RAM into video signals that display as graphic characters on the screen.

VID IN – Video input (to the DC012).

VID OUT – Video output (two outputs from the DC012).

VSR LD – Video shift register load. A signal that determines whether the video shift register performs a parallel load or a shift when clocked.

VT52 – The DIGITAL video terminal that preceded the VT100. It responded to escape sequences conforming to an internal DIGITAL standard.

Wait – Displayed message for operator during NVR operations. Also, an indefinite state in the 8080 controlled by Ready (and not used in the VT100).

Wire-ANDed – TTL devices with open-collector outputs can be tied together to form a logical AND gate at the outputs.

WRITE LB – Write line buffer. Signal that writes a character into the line buffer.

XMIT flag – Transmit flag. Signal to microprocessor from TxRDY at PUSART.

XOFF – Control character that asks the sender to stop sending.

XON – Control character that asks the sender to resume sending.

APPENDIX D
ANSI CODE EXTENSION TECHNIQUES

GENERAL

This appendix describes the ANSI code extension techniques as defined in ANSI standards X3.41-1974 and X3.64-1979 (ISO 2022 and 6429). (Refer to Chapter 1 for ANSI standards ordering information.) The description is based on the functions used in the VT100 and LA120 families of terminals. There are many special cases and details in the specifications that are not described here.

CLASSES OF CHARACTERS

The ANSI system is based on the use of classes of characters for specific purposes. The classes are determined by the character position in the ASCII table (Figure D-1). This table and the ANSI system can work for either a 7-bit or an 8-bit character environment. Current terminals support only 7-bit characters.

CONTROL FUNCTIONS

Control functions are all control characters and groups of characters (strings) that control terminal operation but are not displayed on the screen. Not all control functions perform an action in every device that understands ANSI, but each device can understand all control functions and discard any that do not apply to it. Therefore, each device is said to perform a subset of the ANSI functions.

ANSI COMPLIANCE

Different devices use different subsets. Therefore, compliance with ANSI does not mean compatibility between devices. Compliance only means that a given action, if defined in the ANSI standard, is caused by the same control function in all devices. If an ANSI device does not perform an action that has a control function defined in the ANSI standard, it cannot use that control function for any other purpose.

For example, ESC c is the Reset sequence for devices meeting ANSI and having a remote reset function. If a device does not have this function, it may not use ESC c for any other purpose. ESC 7 (Save Cursor Position), however, is a private sequence and may be used for other purposes by devices from other manufacturers. But within DIGITAL each private sequence is registered in an internal standard so that all DIGITAL products use each sequence for only one purpose.

CONTROL CHARACTERS

A control character is a single character which (when received by the terminal) starts, modifies, or stops a control function. The value of a control character is in the octal range of 0 through 37 and 177.

Appendix A of this document explains the control characters understood by the terminal. All other control character codes are ignored.

This terminal can perform some actions usually caused by control character codes from the 8-bit ASCII environment, which this terminal does not understand. It does this by understanding certain combinations of 7-bit codes, which other sections of this appendix will explain.

B7 B6 B5 / BITS B4 B3 B2 B1 / ROW	0 0 0 / COLUMN 0		0 0 1 / 1		0 1 0 / 2		0 1 1 / 3		1 0 0 / 4		1 0 1 / 5		1 1 0 / 6		1 1 1 / 7	
0 0 0 0 / 0	NUL	0 0 0	DLE	20 16 10	SP	40 32 20	0	60 48 30	@	100 64 40	P	120 80 50	`	140 96 60	p	160 112 70
0 0 0 1 / 1	SOH	1 1 1	DC1 (XON)	21 17 11	!	41 33 21	1	61 49 31	A	101 65 41	Q	121 81 51	a	141 97 61	q	161 113 71
0 0 1 0 / 2	STX	2 2 2	DC2	22 18 12	"	42 34 22	2	62 50 32	B	102 66 42	R	122 82 52	b	142 98 62	r	162 114 72
0 0 1 1 / 3	ETX	3 3 3	DC3 (XOFF)	23 19 13	#	43 35 23	3	63 51 33	C	103 67 43	S	123 83 53	c	143 99 63	s	163 115 73
0 1 0 0 / 4	EOT	4 4 4	DC4	24 20 14	$	44 36 24	4	64 52 34	D	104 68 44	T	124 84 54	d	144 100 64	t	164 116 74
0 1 0 1 / 5	ENQ	5 5 5	NAK	25 21 15	%	45 37 25	5	65 53 35	E	105 69 45	U	125 85 55	e	145 101 65	u	165 117 75
0 1 1 0 / 6	ACK	6 6 6	SYN	26 22 16	&	46 38 26	6	66 54 36	F	106 70 46	V	126 86 56	f	146 102 66	v	166 118 76
0 1 1 1 / 7	BEL	7 7 7	ETB	27 23 17	'	47 39 27	7	67 55 37	G	107 71 47	W	127 87 57	g	147 103 67	w	167 119 77
1 0 0 0 / 8	BS	10 8 8	CAN	30 24 18	(	50 40 28	8	70 56 38	H	110 72 48	X	130 88 58	h	150 104 68	x	170 120 78
1 0 0 1 / 9	HT	11 9 9	EM	31 25 19	)	51 41 29	9	71 57 39	I	111 73 49	Y	131 89 59	i	151 105 69	y	171 121 79
1 0 1 0 / 10	LF	12 10 A	SUB	32 26 1A	*	52 42 2A	:	72 58 3A	J	112 74 4A	Z	132 90 5A	j	152 106 6A	z	172 122 7A
1 0 1 1 / 11	VT	13 11 B	ESC	33 27 1B	+	53 43 2B	;	73 59 3B	K	113 75 4B	[	133 91 5B	k	153 107 6B	{	173 123 7B
1 1 0 0 / 12	FF	14 12 C	FS	34 28 1C	,	54 44 2C	<	74 60 3C	L	114 76 4C	\	134 92 5C	l	154 108 6C	|	174 124 7C
1 1 0 1 / 13	CR	15 13 D	GS	35 29 1D	-	55 45 2D	=	75 61 3D	M	115 77 4D	]	135 93 5D	m	155 109 6D	}	175 125 7D
1 1 1 0 / 14	SO	16 14 E	RS	36 30 1E	.	56 46 2E	>	76 62 3E	N	116 78 4E	^	136 94 5E	n	156 110 6E	~	176 126 7E
1 1 1 1 / 15	SI	17 15 F	US	37 31 1F	/	57 47 2F	?	77 63 3F	O	117 79 4F	_	137 95 5F	o	157 111 6F	DEL	177 127 7F

KEY

ASCII CHARACTER: ESC | 33 OCTAL | 27 DECIMAL | 1B HEX

MA-7246

Figure D-1 ASCII Table

ESCAPE SEQUENCES

The Escape or ESC character (033_8) is a control character that causes the terminal to wait for more characters that are not in the control character numerical range. This character is defined by ANSI standard X3.4-1977 as Introducer. If the terminal receives this character, it waits for more characters to follow within certain numerical ranges to form an escape sequence as defined in ANSI X3.41-1974 and ANSI X3.64-1979.

The format of an escape sequence is:

ESC	**I...I**	**F**
033 Escape sequence introducer	040-057 Intermediate characters (Any number of codes – 0 or more)	060-176 Final character (One code)

If following characters are in the range 040 – 057(8) (column 2), they are called intermediate characters. The device accepts and stores them.

If a following character is in the range 060 – 176(8) (columns 3 to 7), it is a final character. The final character signals the end of an escape sequence which the device then analyzes. Final characters from column 3 are for private control functions for use in a specific device. Final characters from columns 4 – 7 are for ANSI standardized control functions.

Some two-character escape sequences perform the same actions as some 8-bit single-character control functions. The VT100 family supports six of these. (Refer to Appendix A.)

1. ESC [is CSI
2. ESC D is IND
3. ESC E is NEL
4. ESC M is RI
5. ESC N is SS2
6. ESC O is SS3

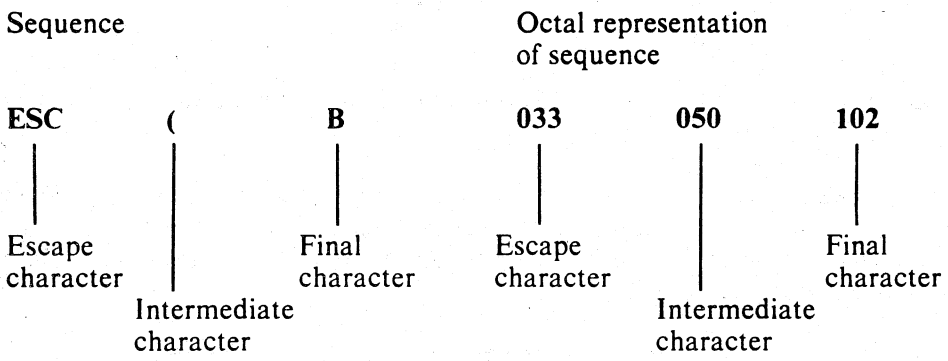
The VT125 also supports ESC P, which is DCS and ESC \, which is ST. (Refer to Communication and Graphic Protocol Controls in the *VT125 User Guide*.)

The intermediate and final characters are taken together to define the function of the sequence. Then the device performs the action and accepts more data. If the action defined by the escape sequence does not apply to the device, the device ignores the complete sequence and accepts more data.

Escape sequence examples (all examples have added spaces between characters to make them easier to read).

ESC H	=	Set tab at active position
ESC (B	=	Designate G0 character set as ASCII
ESC # 6	=	Double width line (VT100)(6 = DIGITAL private)
ESC (0	=	Designate G0 character set as DIGITAL private special graphics character set (0 = private)

Example sequence: Designate G0 character set as ASCII
Select Character Set (SCS) = ESC (B



CONTROL SEQUENCES

The string ESC [is a two-character escape sequence and represents the 8-bit control character Control Sequence Introducer (CSI). CSI precedes all control sequences in the same way that the ESC introducer precedes all escape sequences. ESC [allows the extended functions of the 8-bit control sequence environment to work in the 7-bit environment of current terminals. The control sequence is defined in ANSI X3.64-1979.

The format of a control sequence is as follows.

CSI	**P...P**	**I...I**	**F**
033 133 Control sequence introducer	060-077 Column 3 parameter (0 or more codes)	040-057 Column 2 intermediate (0 or more codes)	100-176 Column 4-7 final (One code)

A device parses this sequence without considering its meaning. That is, characters are stored in classes only according to their range of values. Then, the device interprets these characters by value according to their classes. The intermediate and final characters are taken together to define the function of the sequence. In the range of final characters, 100 – 157 (columns 4 – 6) are reserved for standardization by ANSI, while 160 – 176 (column 7) are reserved for private use.

Parameters

Parameters modify the action or interpretation of the function. The parameters are from column 3 and may be any combination of the characters 0 – 9 (060 – 071) with each parameter separated from the others by ; (073). (The other characters in column 3 are : (072) which is reserved, and <=>? (074 – 077) which are assigned for private use and mean that the following parameters have a private interpretation.) Any leading zero in a parameter is ignored; this also applies to the parameter value 0. Therefore, a sequence with no parameter is the same as a sequence with a parameter of 0 and both are understood as having the default value for that parameter in the sequence.

A single parameter that modifies the action of a control function is called a numeric parameter and has the abbreviation Pn. (Example: Cursor Up, ESC [Pn A, where Pn is number of lines.) A parameter that defines the action of a control function by selecting from a list of possible actions is called a selective parameter and has the abbreviation Ps. (Example: Set Mode, ESC [Ps h, where Ps selects the mode to be set.) Control functions that have selective parameters can accept multiple parameters to allow several actions to be commanded with a single control function.

A sequence with multiple parameters has several Ps separated by ; characters (Ps;Ps;Ps). This is called a parameter string. If the parameters apply to the screen image, their abbreviations indicate this: Pt;Pb for top and bottom, and Pl;Pc for line and column.

Character 077 (?) at the beginning of a parameter string means that the parameters are private parameters. That means the control sequence is standardized but the function that it controls is private, for example, set and reset mode control functions. Some control functions are defined to have a default value for a parameter. The default value is assumed when no parameter character is included in a sequence.

Examples with Octal Equivalents

ESC	**[**	**3**	**g**
033	133	063	147

The above sequence clears all tabs.

ESC	**[**	**g**
033	133	147

The above sequence clears all tabs at active position (default value = 0).

ESC	**[**	**1**	**6**	**;**	**3**	**2**	**u**
033	133	061	066	073	063	062	165

The above sequence sets tabs at columns 16, 32 (LA120) (u = private).

ESC	[	?	2	;	3	h
033	133	077	062	073	063	150

The above sequence sets modes 2 and 3 (? = private).

ESC	[	2	0	h
033	133	062	060	150

The above sequence sets line feed/new line mode (parameter = 20).

ESC	[	2	;	1	y
033	133	062	073	061	171

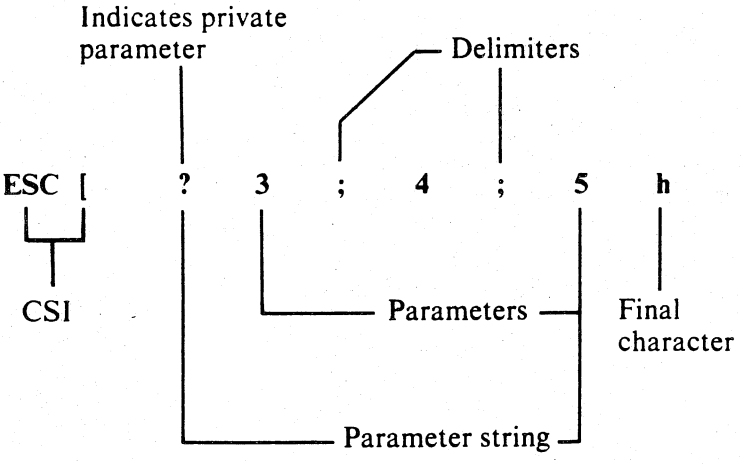
The above sequence runs power-up self-test (VT100) (y = private).

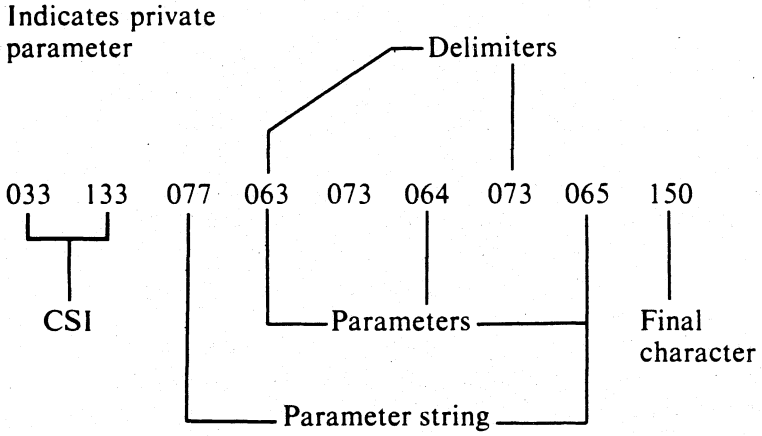
NOTE

There are no examples of control sequences with intermediate characters because current terminals do not have any control functions in that format. However, new software written to understand the ANSI syntax should be able to parse sequences with intermediate characters. Future DIGITAL terminal products may use intermediate characters.

Example Sequence: Control sequence to set modes for 132 column mode, smooth scrolling, and reverse screen

ESC[?3;4;5h





Alternate sequences that will do the same thing:

ESC[?3hESC[?4hESC[?5h Parameters can be split into separate control sequences.

ESC[?03;004;5h Leading zeroes are ignored.

ERROR RECOVERY

The ANSI standards do not define error recovery techniques for incorrect control functions. These errors include out of range parameters, invalid control functions, and control characters embedded in control functions. The VT100 family recovers from errors with as much correct function as possible rather than discard any error. For example, if the VT100 receives a sequence asking it to move the cursor beyond the right margin, it moves the cursor to the right margin. In the LA120, a command to move beyond the right margin is ignored and the active position stays unchanged.

If a control character appears within a sequence, the VT100 performs the function of the control character (for example, a carriage return) as if it had been received before the beginning of the sequence. However, CAN and SUB appearing in a sequence stop the processing of the sequence at that point. The terminal returns to regular character processing and displays any characters remaining in the sequence.

An unrecognizable control function is ignored. Unsupported control functions (any apparently valid sequences that are not listed in this document) are generally ignored but may produce unpredictable responses.

NOTE

Some programmers have used error condition actions in a given terminal to get the actions they wanted. This is not a safe practice in the ANSI environment because there is no guarantee that different ANSI-complying terminals will handle an error the same way. Using error conditions would limit the transportability of code.

CHARACTER SETS AND SELECTION

G0, G1, C0, C1 Character Sets

The ANSI and ISO standards provide extensions to the range of graphic and control character sets in a terminal, in addition to the extension of control functions described in the preceding section.

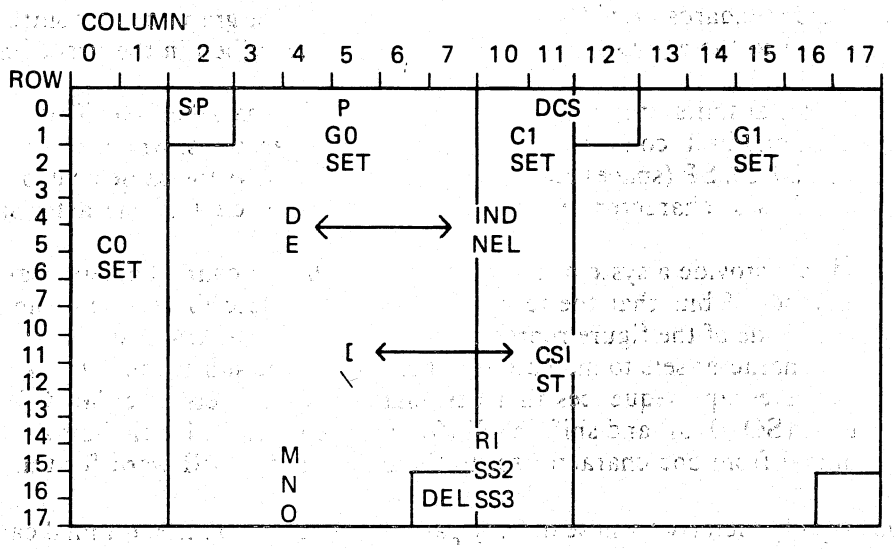
A typical terminal transmits and receives the 7-bit ASCII character set. This character set has an eight-column chart, and in it, columns 0 and 1 are control characters, while the rest of the set is graphics (except SP and DEL). SP (space) and DEL (delete) are always the same control characters with the same codes, regardless of character set and so they are independent of character set selection.

The ANSI standards provide a system to allow the use of larger character sets in any terminal, without increasing the number of bits that the terminal must use to describe each unique character. Refer to Figure D-2. The left side of the figure represents the familiar 7-bit ASCII character set. G0 and G1 are labels attached to character sets to indicate how the sets can be substituted. The ANSI word for this is designate. There are escape sequences that designate character sets as either G0 or G1. The control characters shift out (SO (016)) and shift in (SI (017)), when included with 7-bit ASCII data, switch the display of a terminal from one character set to the other. The ANSI word for this is invoke.

In the VT100, any character set whose display patterns are stored in the terminal can become either G0 or G1. SO always invokes the G1 set and SI invokes the G0 set. Sets can be invoked or designated at any time and in any order. Some character sets have been internationally registered, while others are private for use in a given terminal.

In the VT100, the C0 control character set is normally available. There are escape sequences that cause the actions of single control functions of the C1 set on a one time basis. The ESC character followed by a final character from columns 4 or 5 causes the action of a control function that is also caused by a single 8-bit character in the C1 set. Figure D-2 shows how ESC [causes the CSI function and ESC D causes the IND function from the C1 set. The other C1 characters that are supported in the VT100 family of terminals are also shown.

Figure D-3 shows a schematic representation of the Shift Out and Shift In concept. This figure shows how G0 and G1 character sets are designated by escape sequences and invoked by the SO and SI characters.



C0, C1 = CONTROL CHARACTER SETS
G0, G1 = GRAPHIC CHARACTER SETS
DCS, ST = VT125, VK100 ONLY

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Figure D-2 8-Bit ASCII Chart

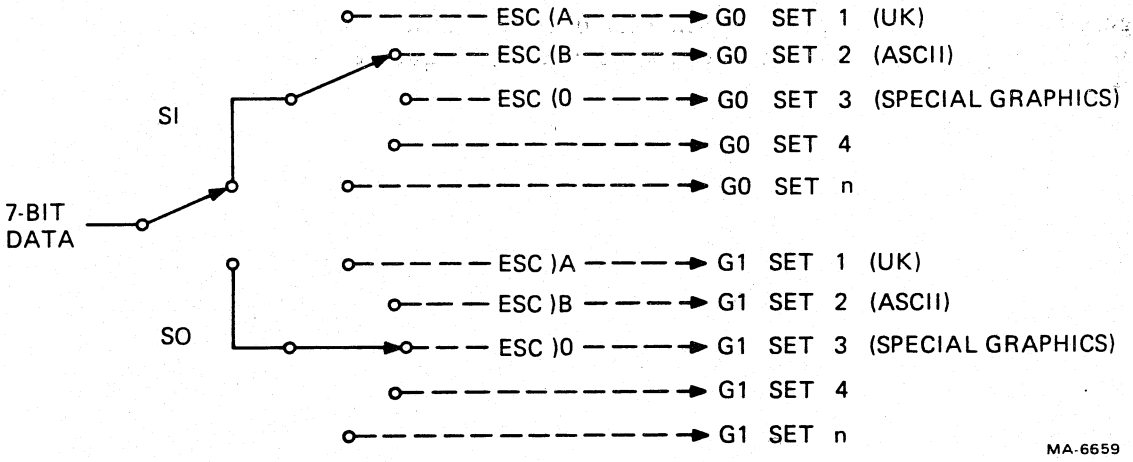

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Figure D-3 Shift Out and Shift In

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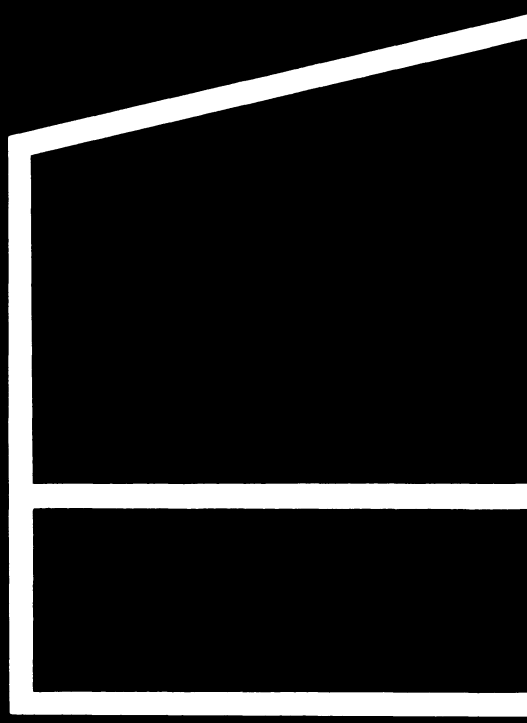
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